



LM397 Single General-Purpose Voltage Comparator

1 Features

- $T_A = 25^\circ\text{C}$. Typical Values Unless Otherwise Specified.
- 5-Pin SOT-23 Package
- Industrial Operating Range -40°C to $+85^\circ\text{C}$
- Single or Dual Power Supplies
- Wide Supply Voltage Range 5 V to 30 V
- Low Supply Current 300 μA
- Low Input Bias Current 7 nA
- Low Input Offset Current ± 1 nA
- Low Input Offset Voltage ± 2 mV
- Response Time 440 ns (50-mV Overdrive)
- Input Common-Mode Voltage 0 to $V_S - 1.5$ V

2 Applications

- A/D Converters
- Pulse, Square-Wave Generators
- Peak Detector
- Industrial Applications

3 Description

The LM397 device is a single voltage comparator with an input common mode that includes ground. The LM397 is designed to operate from a single 5-V to 30-V power supply or a split power supply. Its low supply current is virtually independent of the magnitude of the supply voltage.

The LM397 features an open-collector output stage. This allows the connection of an external resistor at the output. The output can directly interface with TTL, CMOS and other logic levels, by tying the resistor to different voltage levels (level translator).

The LM397 is available in the space-saving 5-Pin SOT-23 package and is pin-compatible to TI's TL331, a single differential comparator.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM397	SOT-23 (5)	2.90 mm $\times$ 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit

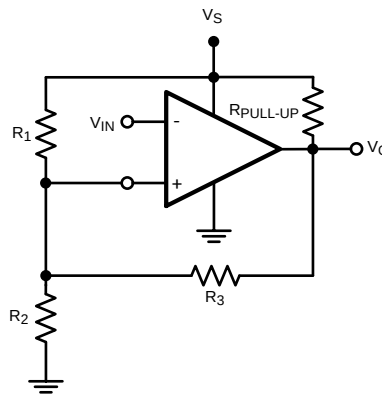


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2015) to Revision F Page

- Changed incorrect Pin Functions table entries. Pins 4 and 5 were swapped. **3**

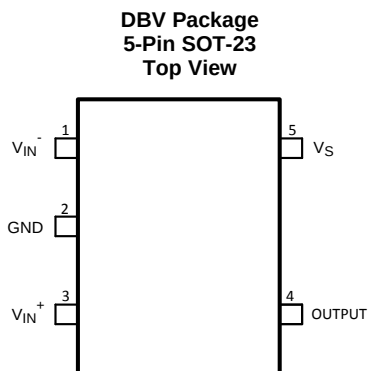
Changes from Revision D (March 2013) to Revision E Page

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. **1**

Changes from Revision C (March 2013) to Revision D Page

- Changed layout of National Data Sheet to TI format

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	P	Ground
OUTPUT	4	O	Output
V_{IN+}	3	I	Noninverting Input
V_{IN-}	1	I	Inverting Input
V_S	5	P	Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

			MIN	MAX	UNIT
V _{IN} differential			30	30	V
Supply voltages			±15	30	V
Voltage at input pins			−0.3	30	V
Junction temperature ⁽³⁾				150	°C
Soldering information	Infrared or Convection (20 sec.)			235	°C
	Wave Soldering (10 sec.)			260	°C
Storage Temperature, T _{stg}			−65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾⁽²⁾	±2000
	Machine Model ⁽¹⁾⁽²⁾	±200

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage, V _S	5	30	V
Temperature ⁽¹⁾	–40	85	°C

- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM397	UNIT
		DBV (SOT-23)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	186	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	92.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	38.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	5.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	38.4	°C/W

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

6.5 Electrical Characteristics

Unless otherwise specified, all limits are ensured for $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V^- = 0\text{ V}$, $V_{CM} = V^+/2 = V_O$.

PARAMETER		TEST CONDITIONS		MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
V_{OS}	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}$, $V_O = 1.4\text{ V}$, $V_{CM} = 0\text{ V}$	$T_A = 25^\circ\text{C}$		2	7	mV
			At the temperature extremes			10	
I_{OS}	Input offset current	$V_O = 1.4\text{ V}$, $V_{CM} = 0\text{ V}$	$T_A = 25^\circ\text{C}$		1.6	50	nA
			At the temperature extremes			250	
I_B	Input bias current	$V_O = 1.4\text{ V}$, $V_{CM} = 0\text{ V}$	$T_A = 25^\circ\text{C}$		10	250	nA
			At the temperature extremes			400	
I_S	Supply current	$R_L = \text{open}$, $V_S = 5\text{ V}$			0.25	0.7	mA
		$R_L = \text{open}$, $V_S = 30\text{ V}$			0.3	2	
I_O	Output sink current	$V_{IN}^+ = 1\text{ V}$, $V_{IN}^- = 0\text{ V}$, $V_O = 1.5\text{ V}$		6	13		mA
$I_{LEAKAGE}$	Output leakage current	$V_{IN}^+ = 1\text{ V}$, $V_{IN}^- = 0\text{ V}$, $V_O = 5\text{ V}$			0.1		nA
		$V_{IN}^+ = 1\text{ V}$, $V_{IN}^- = 0\text{ V}$, $V_O = 30\text{ V}$			1		μA
V_{OL}	Output voltage low	$I_O = -4\text{ mA}$, $V_{IN}^+ = 0\text{ V}$, $V_{IN}^- = 1\text{ V}$	$T_A = 25^\circ\text{C}$		180	400	mV
			At the temperature extremes			700	
V_{CM}	Common-mode input voltage range	$V_S = 5\text{ V to }30\text{ V}^{(3)}$	$T_A = 25^\circ\text{C}$	0		$V_S - 1.5$	V
			At the temperature extremes	0		$V_S - 2$	
A_V	Voltage gain	$V_S = 15\text{ V}$, $V_O = 1.4\text{ V to }11.4\text{ V}$, $R_L > 15\text{ k}\Omega$ connected to V_S			120		V/mV
t_{PHL}	Propagation delay (high to low)	Input overdrive = 5 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$			900		ns
		Input overdrive = 50 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$			250		
t_{PLH}	Propagation delay (low to high)	Input Overdrive = 5 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$			940		μs
		Input overdrive = 50 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$			440		ns

- (1) All limits are specified by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (3) The input common-mode voltage of either input should not be permitted to go below the negative rail by more than 0.3V. The upper end of the common-mode voltage range is $V_S - 1.5\text{ V}$ at 25°C .

6.6 Typical Characteristics

$T_A = 25^\circ\text{C}$. Unless otherwise specified.

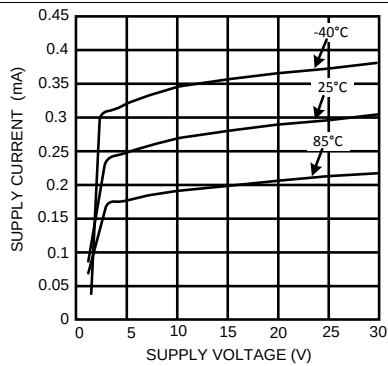


Figure 1. Supply Current vs Supply Voltage

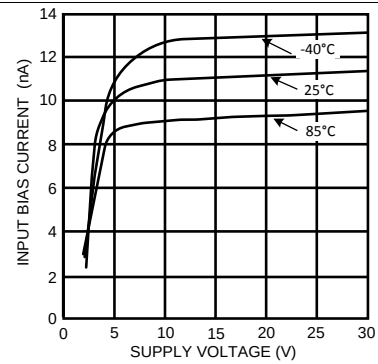


Figure 2. Input Bias Current vs Supply Current

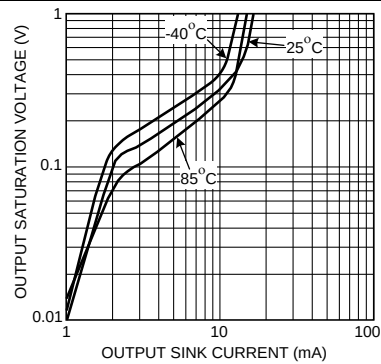


Figure 3. Output Saturation Voltage vs Output Sink Current

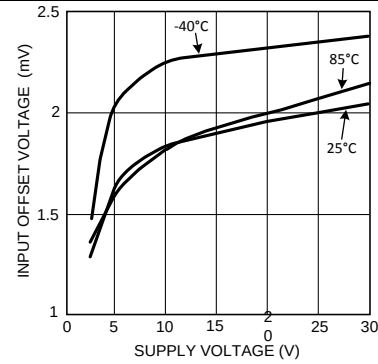


Figure 4. Input Offset Voltage vs Supply Voltage

7 Detailed Description

7.1 Overview

A comparator is often used to convert an analog signal to a digital signal. The comparator compares an input voltage (V_{IN}) at the noninverting pin to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF} the output (V_O) is low (V_{OL}). However, if V_{IN} is greater than V_{REF} , the output voltage (V_O) is high (V_{OH}). Refer to [Figure 6](#).

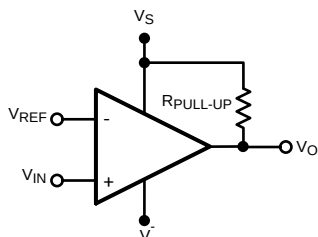


Figure 5. Basic Comparator

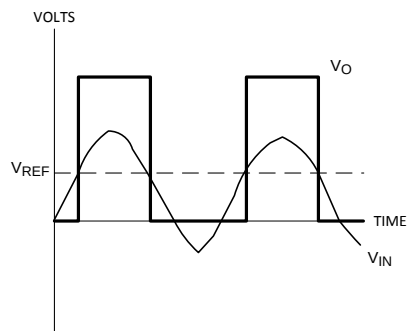
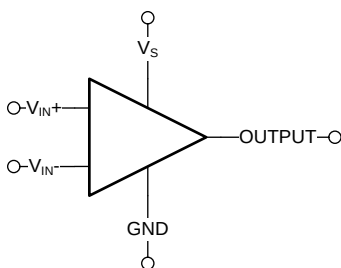


Figure 6. Basic Comparator Output

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stage

The LM397 has a bipolar input stage. The input common-mode voltage range is from 0 to ($V_S - 1.5$ V).

7.3.2 Output Stage

The LM397 has an open-collector grounded-emitter NPN output transistor for the output stage. This requires an external pullup resistor connected between the positive supply voltage and the output. The external pullup resistor should be high enough resistance so to avoid excessive power dissipation. In addition, the pullup resistor should be low enough resistance to enable the comparator to switch with the load circuitry connected. Because it is an open-collector output stage, several comparator outputs can be connected together to create an OR'ing function output. With an open collector, the output can be used as a simple SPST switch to ground. The amount of current which the output can sink is approximately 10 mA. When the maximum current limit is reached, the output transistor will saturate and the output will rise rapidly ([Figure 7](#)).

Feature Description (continued)

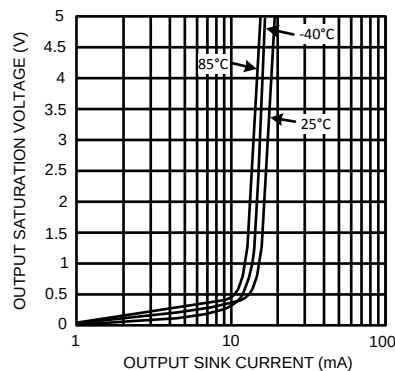


Figure 7. Output Saturation Voltage vs Output Sink Current

7.4 Device Functional Modes

7.4.1 Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near the input offset voltage of the comparator. This tends to occur when the voltage on the input is equal or very close to the other input voltage. Adding hysteresis can prevent this problem. Hysteresis creates two switching thresholds (one for the rising input voltage and the other for the falling input voltage). Hysteresis is the voltage difference between the two switching thresholds. When both inputs are nearly equal, hysteresis causes one input to effectively move quickly pass the other. Thus, effectively moving the input out of region that oscillation may occur.

For an inverting configured comparator, hysteresis can be added with a three resistor network and positive feedback. When input voltage (V_{IN}) at the inverting node is less than non-inverting node (V_T), the output is high. The equivalent circuit for the three resistor network is R_1 in parallel with R_3 and in series with R_2 . The lower threshold voltage V_{T1} is calculated by [Equation 1](#):

$$V_{T1} = ((V_S R_2) / (((R_1 R_3) / (R_1 + R_3)) + R_2)) \quad (1)$$

When V_{IN} is greater than V_T , the output voltage is low. The equivalent circuit for the three resistor network is R_2 in parallel with R_3 and in series with R_1 . The upper threshold voltage V_{T2} is calculated by [Equation 2](#):

$$V_{T2} = V_S ((R_2 R_3) / (R_2 + R_3)) / (R_1 + ((R_2 R_3) / (R_2 + R_3))) \quad (2)$$

The hysteresis is defined in [Equation 3](#):

$$\Delta V_{IN} = V_{T1} - V_{T2} \quad (3)$$

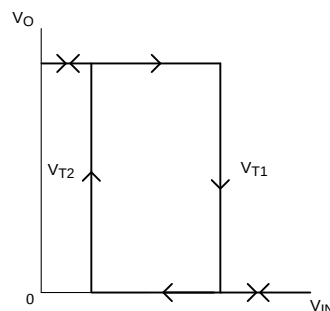


Figure 8. Inverting Configured Comparator - LM397

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LM397 will typically be used to compare a single signal to a reference or two signals against each other.

8.2 Typical Application

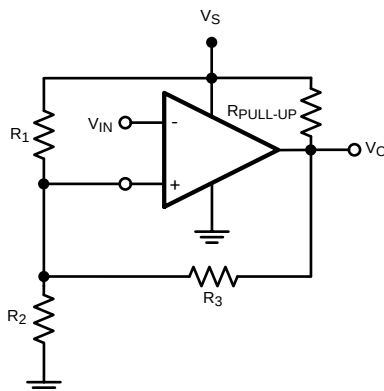


Figure 9. Inverting Comparator With Hysteresis

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0 V to $V_S - 1.5$ V
Supply voltage	5 V to 30 V
Logic supply voltage (R_{PULLUP} voltage)	5 V to 30 V
Output current (V_{LOGIC}/R_{PULLUP})	1 μ A to 20 mA
Input overdrive voltage	100 mV
Reference voltage	5.5 V

8.2.2 Detailed Design Procedure

When using TL331 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{CM}) must be taken in to account. If temperature operation is above or below 25°C the V_{CM} can range from 0 V to $V_S - 1.5$ V. This limits the input voltage range to as high as $V_S - 1.5$ V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

- When both IN– and IN+ are both within the common mode range:
 - If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
- When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
- When IN– and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage. To make an accurate comparison; the overdrive voltage should be higher than the input offset voltage. Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive.

8.2.2.3 Output and Drive Current

Output current is determined by the pullup resistance (R_{PULLUP}) and V_S voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use Figure 3 to determine V_{OL} based on the output current. The output current can also effect the transient response.

8.2.3 Application Curves

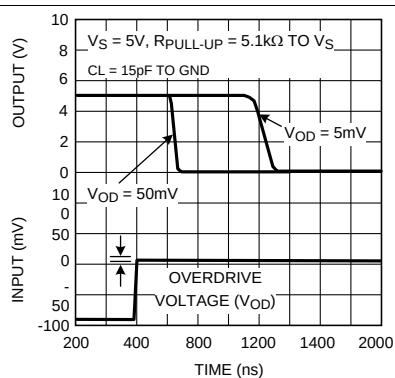


Figure 10. Response Time for Various Input Overdrives – t_{PHL}

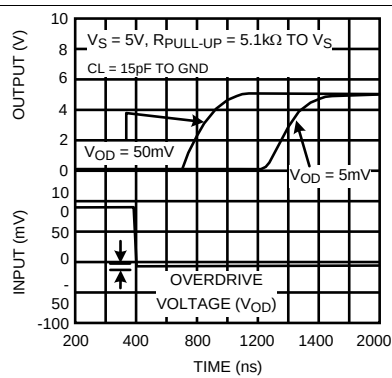


Figure 11. Response Time for Various Input Overdrives – t_{PLH}

9 Power Supply Recommendations

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement; see the [Layout Guidelines](#) section.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit-board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the LM397.
- To minimize supply noise, place a decoupling capacitor (0.1- μ F ceramic, surface-mount capacitor) as close as possible to V_S as shown in [Figure 12](#).
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the top-side ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

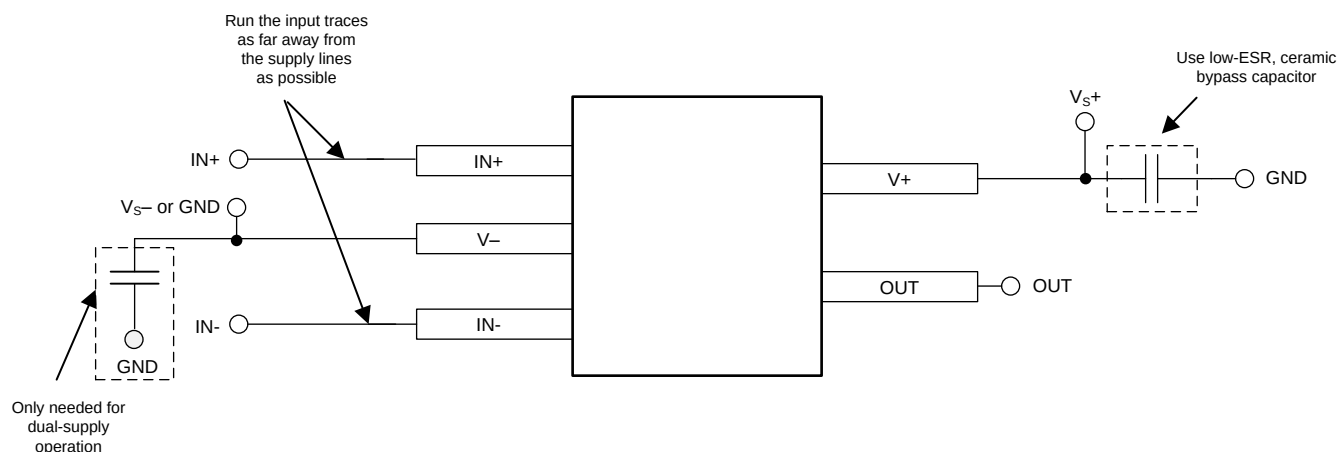


Figure 12. Comparator Board Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM397MF	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 85	C397
LM397MF/NOPB	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C397
LM397MF/NOPB.B	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C397
LM397MFX/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C397
LM397MFX/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C397

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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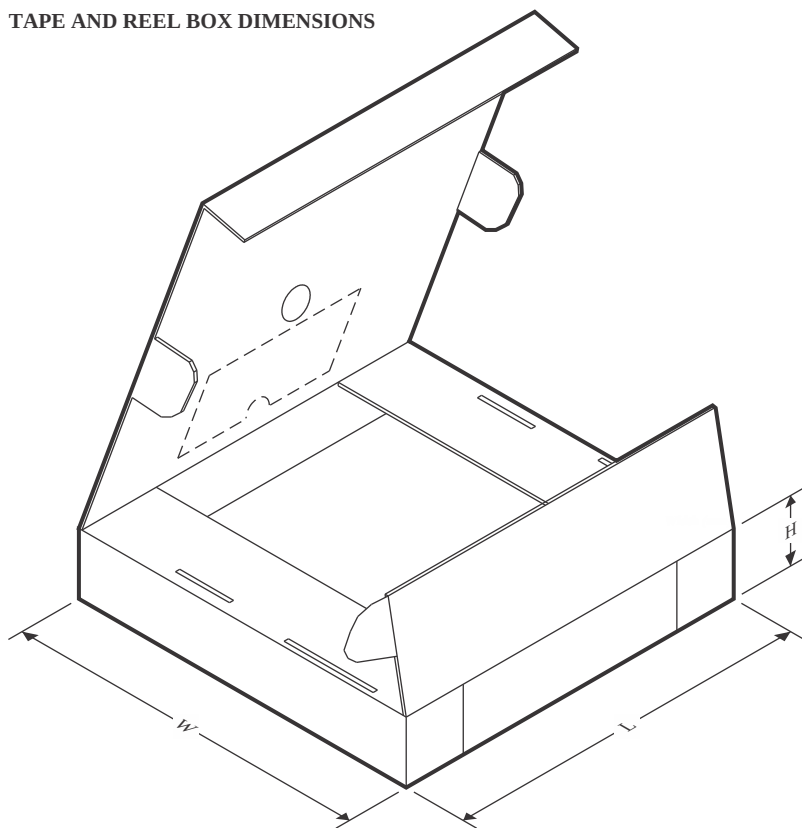
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM397MF/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM397MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM397MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM397MFX/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

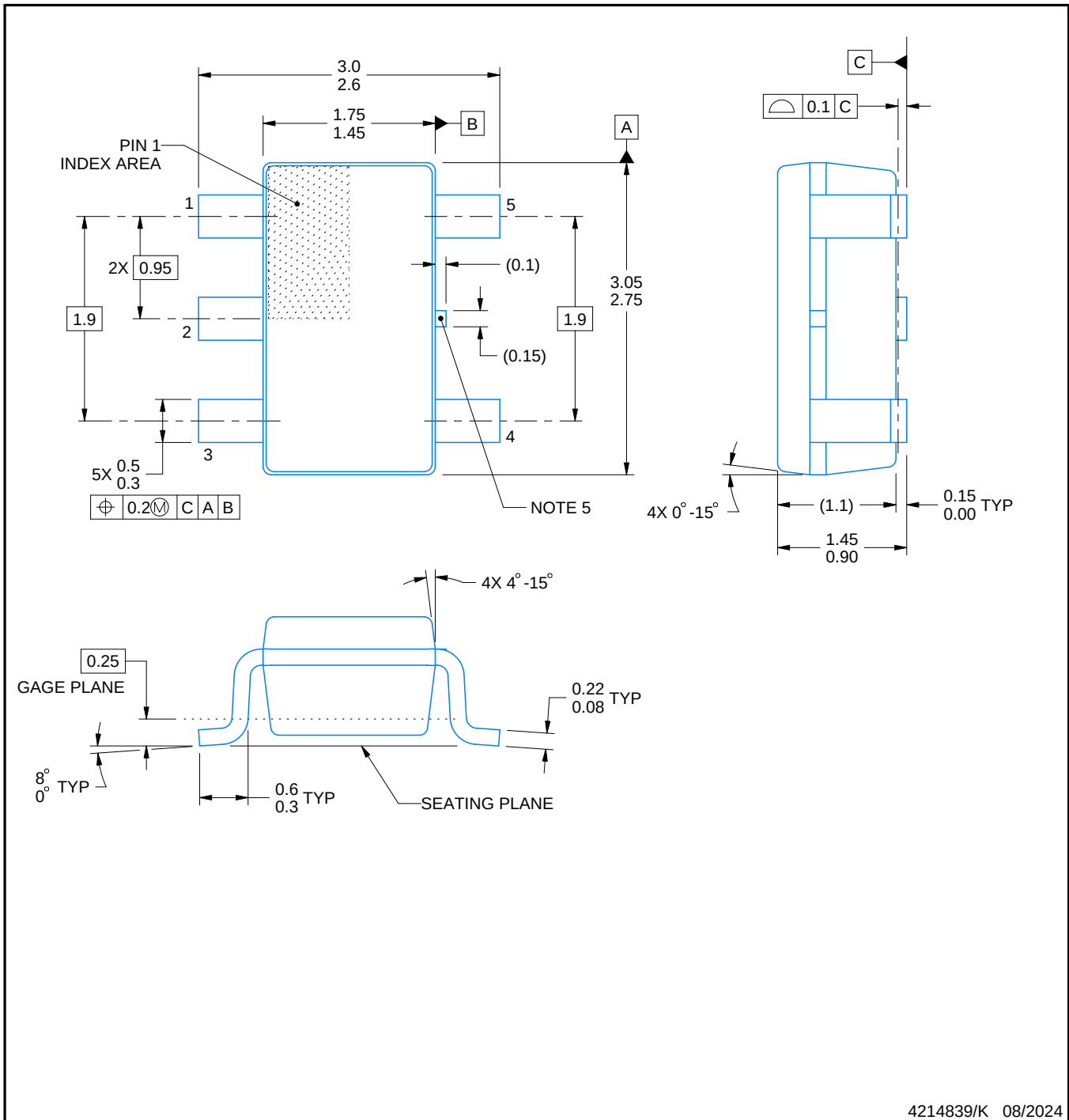


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM397MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM397MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM397MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM397MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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NOTES:

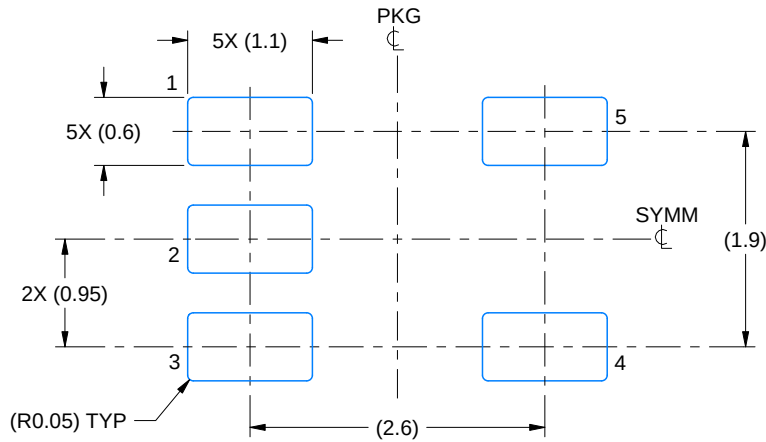
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

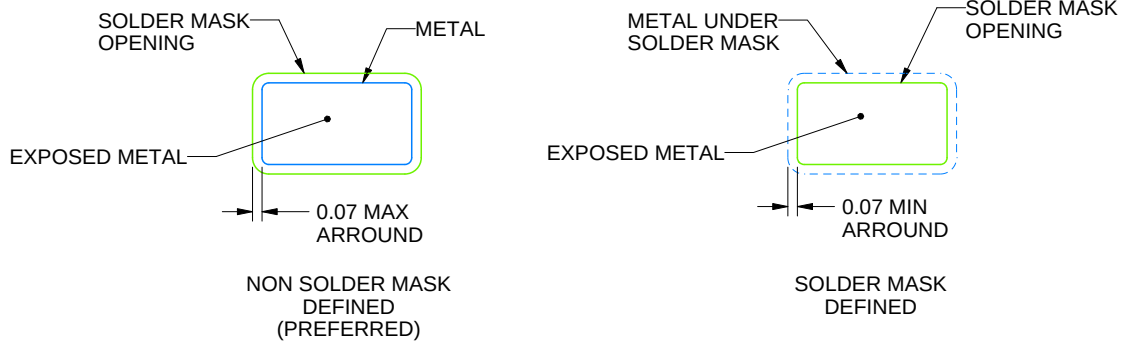
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

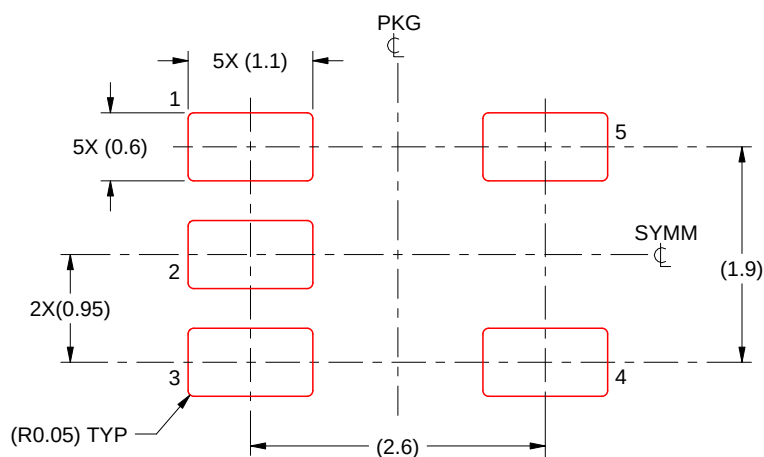
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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