

LM4060-Q1 Automotive 20ppm/°C Maximum Drift High Precision Shunt Voltage Reference

1 Features

- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature T_A
- Low operating current:
 - 40 μA typical
- Initial accuracy: $\pm 0.05\%$ (maximum)
- Temperature coefficient:
 - 6ppm/°C typical for -40°C to 125°C
- Wide operating current range up to 50mA
- No output capacitor required
- Capable of driving capacitive loads up to 4.7 μF
- Output voltages options:
 - 1.25V, 1.5V, 1.6V, 1.65V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V
- Low output noise:
 - 10Hz to 1kHz: 26ppm_{rms}
 - Output 1/f noise (0.1Hz to 10Hz): 9ppm_{P-P}
- Long-term stability: 40ppm at 500 hours
- Specified temperature range -40°C to 125°C
- Small footprint 3-pin SOT-23 package
- Pin-to-pin compatible with LM4040-N-Q1, TL4050-Q1, and LM4050-N-Q1

2 Applications

- [High voltage battery system](#)
- [Onboard charger](#)
- [DC/DC converter system](#)
- [Traction inverter](#)
- [ADAS domain controller](#)

3 Description

The LM4060-Q1 is a family of high-precision shunt voltage references. The LM4060-Q1 family offers low 20ppm/°C temperature coefficient and 0.05% high precision initial accuracy. The LM4060 design eliminates the need for an external stabilizing capacitor and provides stability with capacitive loads up to 4.7 μF . The LM4060-Q1 is offered in several fixed reverse breakdown voltages: 1.25V, 1.5V, 1.6V, 1.65V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V. The flexible voltage options make the LM4060-Q1 a companion device for ADCs, DACs, and level shifting signal conditioning circuits.

The LM4060-Q1 supports a maximum operating current up to 50mA to support a wide range of loads. The wide load current support allows for powering of ADCs, DACs, and MCUs while providing a stable voltage reference. The LM4060-Q1 functionality is similar to a Zener diode where the cathode voltage is constant above the minimum operating current. The LM4060-Q1 can be powered from a wide input supply voltage but an external resistor is required.

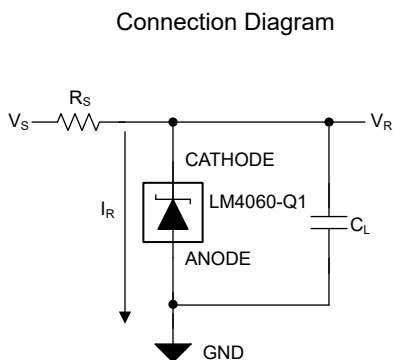
The LM4060-Q1 is specified for -40°C and 125°C , which enables operation across various industrial applications.

Package Information

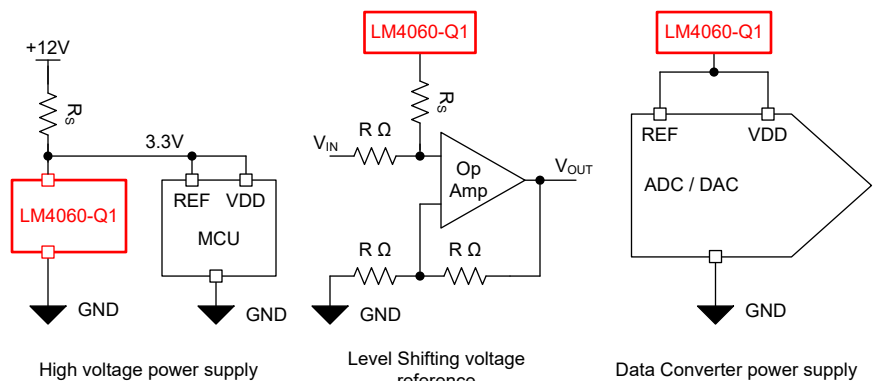
PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LM4060-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm

(1) For more information, see [Section 12](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Use Cases



LM4060-Q1 Use Case



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4 Device Comparison Table

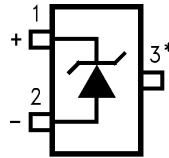
The LM4060-Q1 has multiple voltage options available. Use [Table 4-1](#) as the part number decoding table for all devices. For devices marked preview, contact TI sales representatives or on TI's [E2E](#) forum for details and availability of other options.

Table 4-1. Device Comparison Table

ORDERABLE PART NAME	V _R
LM4060A12EDBZRQ1	1.25V
LM4060A15EDBZRQ1 ⁽¹⁾	1.5V
LM4060A16EDBZRQ1 ⁽¹⁾	1.6V
LM4060A165DBZRQ1 ⁽¹⁾	1.65V
LM4060A18EDBZRQ1 ⁽¹⁾	1.8V
LM4060A20EDBZRQ1	2.048V
LM4060A25EDBZRQ1	2.5V
LM4060A30EDBZRQ1	3.0V
LM4060A33EDBZRQ1	3.3V
LM4060A41EDBZRQ1 ⁽¹⁾	4.096V
LM4060A50EDBZRQ1	5.0V

(1) Preview Information (not Production Data).

5 Pin Configuration and Functions



*This pin must be left floating or connected to pin 2.

**Figure 5-1. DBZ Package
3-Pin SOT-23
Top View**

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Cathode	1	I/O	Shunt current and input voltage
Anode	2	O	Common pin, normally connected to ground
DNC	3	—	This pin must be left floating or connected to pin 2.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
I_R	Reverse Current		55	mA
T_J	Maximum Junction Temperature		150	C
Tstg	Storage Temperature	-65	150	C

- (1) Stresses above these ratings can cause permanent damage. Exposure to absolute maximum conditions for extended periods can degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

conditions apply over the operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_R	Continuous Cathode Current Range	I_{RMIN}	50	mA
T_J	Junction Temperature	-40	125	C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM4060-Q1	UNIT
		DBZ	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229.8	C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.7	C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.4	C/W
Ψ_{JT}	Junction-to-top characterization resistance	16.5	C/W
Ψ_{JB}	Junction-to-board characterization resistance	98.6	C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating conditions, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_R	Reverse breakdown voltage Accuracy	$I_R = 100\mu\text{A}$		-0.05		0.05	%
V_R	Output voltage temperature coefficient ⁽¹⁾	$I_R = 100\mu\text{A}$	$T_J = -40^\circ\text{C}$ to 125°C		6	20	ppm/ $^\circ\text{C}$
$I_{R\text{MIN}}$	Minimum cathode current		$T_J = -40^\circ\text{C}$ to 125°C		35	50	μA
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{R\text{MIN}} < I_R < 50\text{mA}$	$T_J = -40^\circ\text{C}$ to 125°C			50	ppm/mA
Z_R	Reverse Dynamic Impedance ⁽²⁾	$I_R = 1\text{mA}$, $F = 120\text{Hz}$, $I_{AC} = 0.1 I_R$			0.55	1.5	Ω
$e_{\text{np-p}}$	Low frequency noise	$I_R = 100\mu\text{A}$, $0.1\text{Hz} \leq f \leq 10\text{Hz}$			9		$\mu\text{V}_{\text{p-p}}/\text{V}$
e_N	Wideband Noise	$I_R = 100\mu\text{A}$, $10\text{Hz} \leq f \leq 10\text{kHz}$			27		ppm _{rms}
V_{HYST}	Thermal Hysteresis	$V_R = 3.3\text{V}$	$T_A = 25^\circ\text{C}$, -40°C , 125°C , 25°C (cycle 1)		130		ppm
V_{HYST}	Thermal Hysteresis	$V_R = 3.3\text{V}$	$T_A = 25^\circ\text{C}$, -40°C , 125°C , 25°C (cycle 2)		20		ppm
C_L	Stable output capacitor range		$T_J = -40^\circ\text{C}$ to 125°C			4.7	μF
t_{ST}	Settling Time	$I_R = 100\mu\text{A}$, $C_L = 0\mu\text{F}$, 99% of V_R			2000		μs
t_{ST}	Settling Time	$I_R = 1\text{mA}$, $C_L = 1\mu\text{F}$, 99% of V_R			6		mS

- (1) The temperature coefficient parameter for V_R is calculated using the box method which is the difference between the maximum and minimum values obtained over the rated temperature range. For more details on V_R and how it relates to the average temperature coefficient, see [Parameter Measurement Information](#).
- (2) The dynamic impedance is defined by $|Z_R| = \Delta V_R/\Delta I_R$. For more details on $|Z_R|$ and how it relates to V_R , see [Parameter Measurement Information](#).

6.6 Typical Characteristics

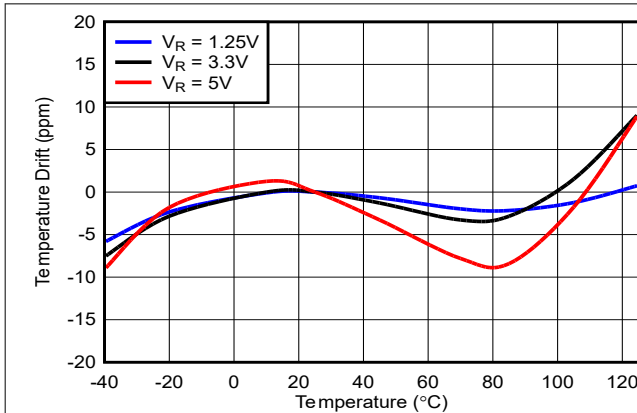


Figure 6-1. Temperature Drift

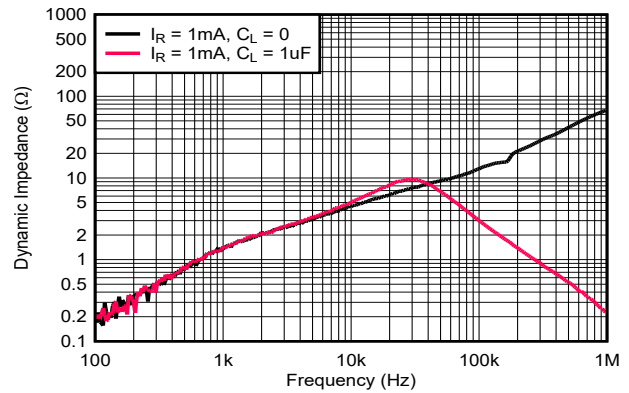


Figure 6-2. Output Impedance vs Frequency, $V_R = 1.25V$

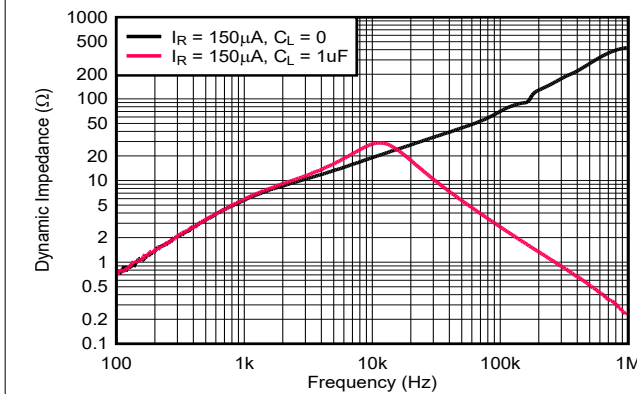


Figure 6-3. Output Impedance vs Frequency, $V_R = 1.25V$

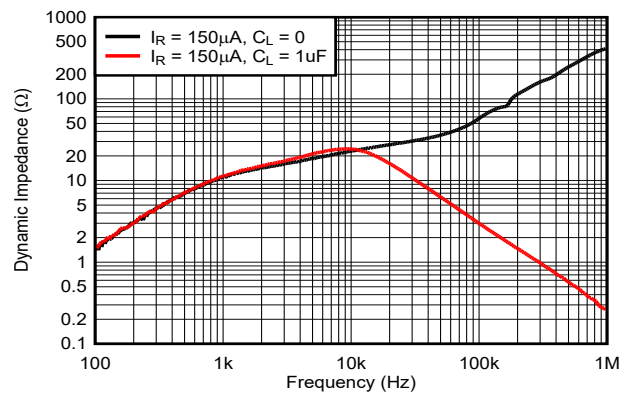


Figure 6-4. Output Impedance vs Frequency, $V_R = 3.3V$

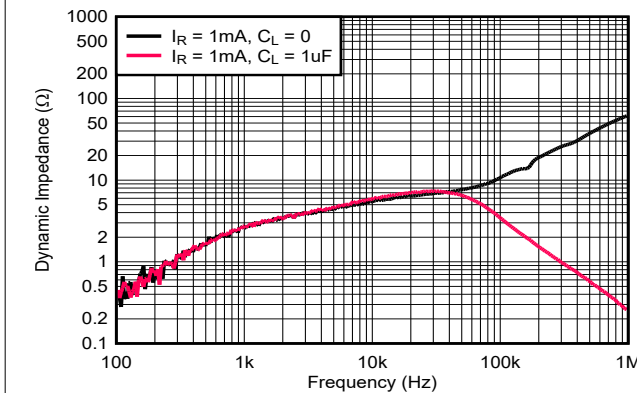


Figure 6-5. Output Impedance vs Frequency, $V_R = 3.3V$

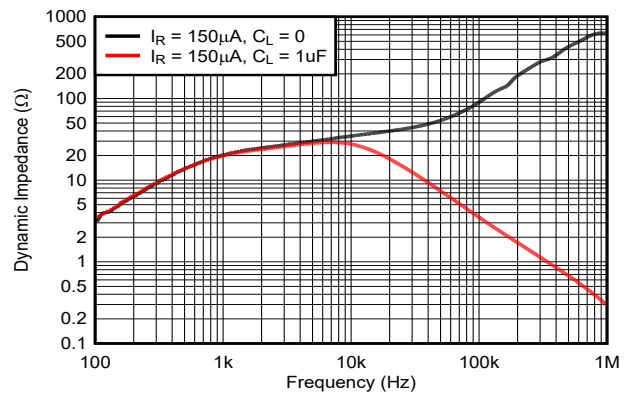


Figure 6-6. Output Impedance vs Frequency, $V_R = 5V$

6.6 Typical Characteristics (continued)

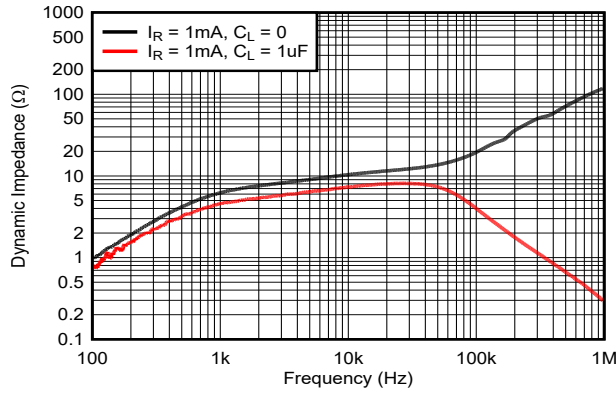


Figure 6-7. Output Impedance vs Frequency, $V_R = 5V$

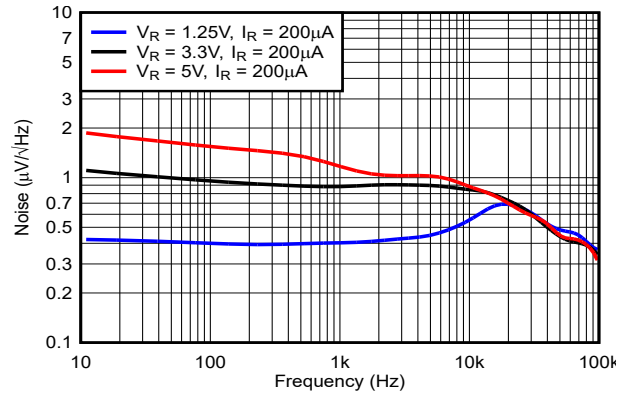


Figure 6-8. Noise Spectral Density

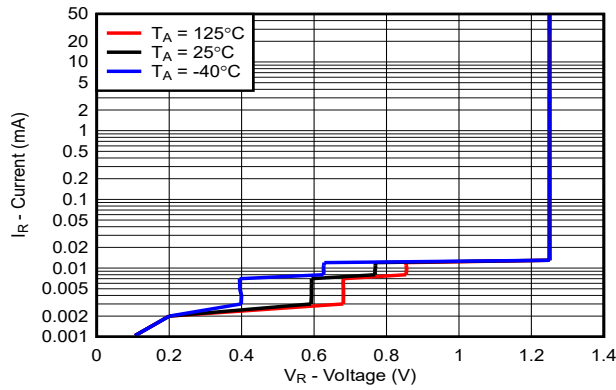


Figure 6-9. Minimum Operating Voltage, $V_R = 1.25V$

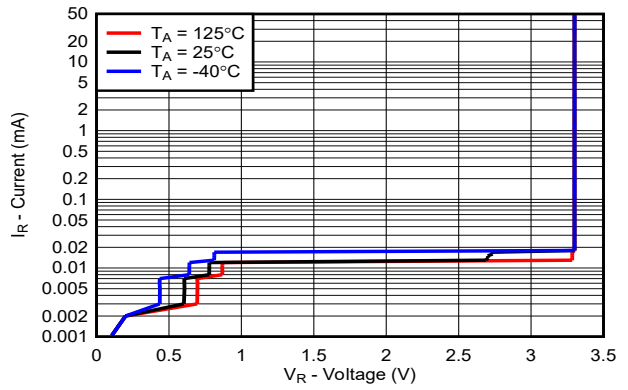


Figure 6-10. Minimum Operating Voltage, $V_R = 3.3V$

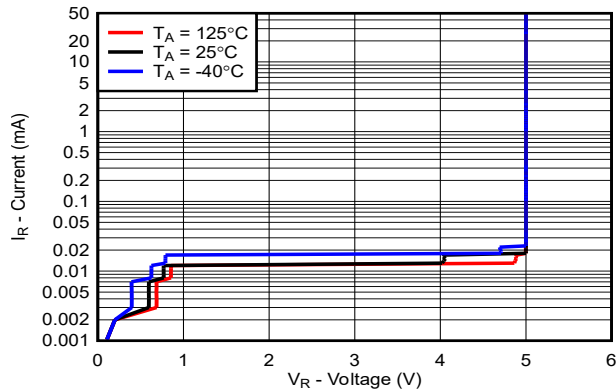


Figure 6-11. Minimum Operating Voltage, $V_R = 5V$

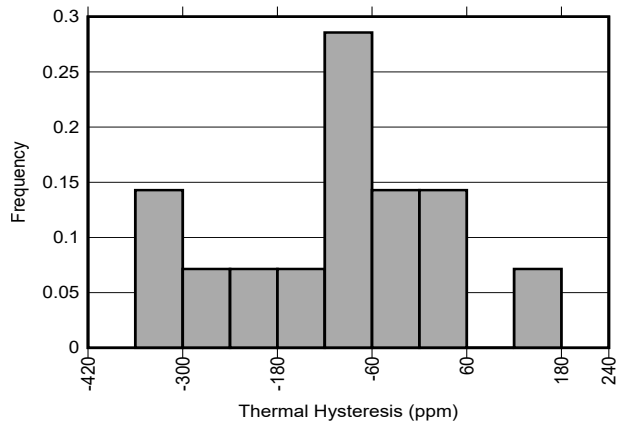


Figure 6-12. Thermal Hysteresis - Cycle 1

6.6 Typical Characteristics (continued)

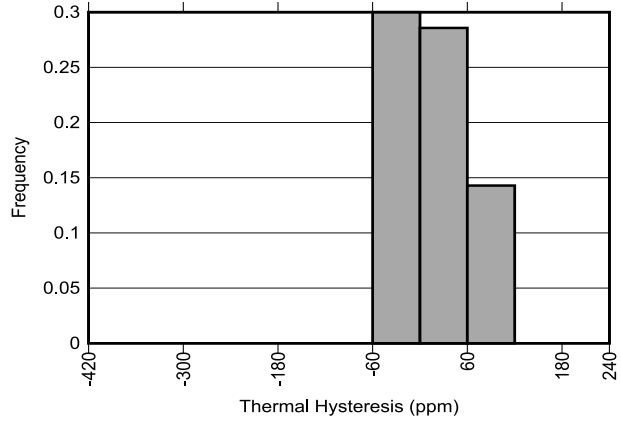


Figure 6-13. Thermal Hysteresis - Cycle 2

7 Parameter Measurement Information

7.1 Temperature Coefficient

The LM4060-Q1 temperature coefficient is calculated using the box method. The box method temperature coefficient of V_R is defined in [Figure 7-1](#). The box method temperature coefficient is an average of the full operating temperature range and therefore any subsection of the rated operating temperature range can yield a value that is greater or less than the average. For more details on temperature coefficient, refer to the [Voltage Reference Selection Basics white paper](#).

$$TC_{\text{BOX}} = 10^6 \left(\frac{V_{R\text{MAX}}|_T - V_{R\text{MIN}}|_T}{V_{R|T(25^\circ\text{C})}} \right) \left(\frac{1}{T_{\text{MAX}} - T_{\text{MIN}}} \right)$$

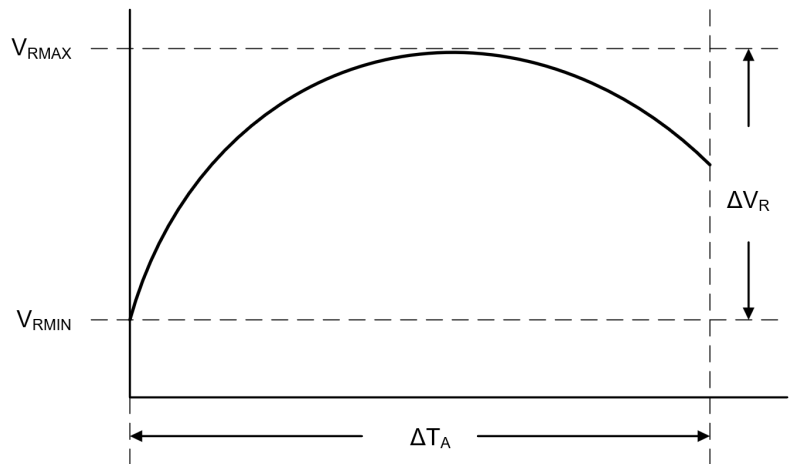


Figure 7-1. Temperature Coefficient

7.2 Solder Heat Shift

The materials used in the manufacturing of the LM4060-Q1 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 32 devices were soldered on one printed circuit board using lead-free solder paste and the paste manufacturer suggested reflow profile. [Figure 7-2](#) shows the reflow profile. The printed circuit board is comprised of FR4 material. The board thickness is 1.66mm and the area is 174mm × 135mm.

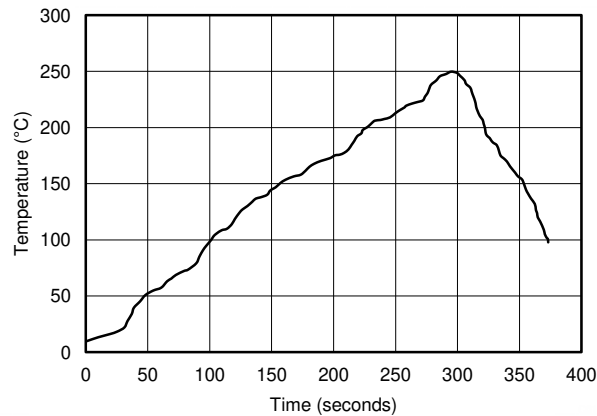


Figure 7-2. Reflow Profile

The reference output voltage is measured before and after the reflow process; [Figure 7-3](#) shows the typical shift. Although all tested units exhibit very low shifts (< 0.04%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board (PCB). An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize the exposure to thermal stress.

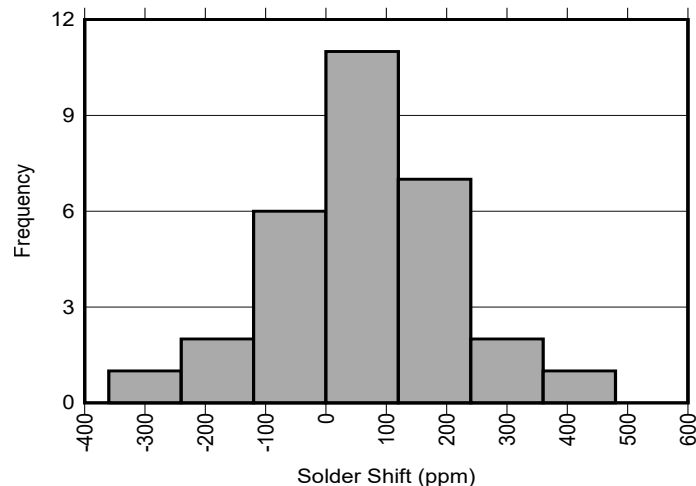


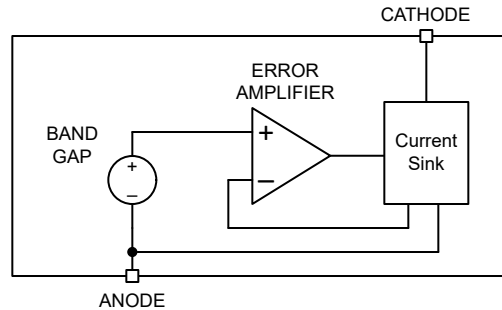
Figure 7-3. Solder Heat Shift Distribution, V_{REF} (%)

8 Detailed Description

8.1 Overview

The LM4060-Q1 is a family of high-precision shunt voltage references. The LM4060-Q1 family offers low 20ppm/°C temperature coefficient and 0.05% high precision initial accuracy. The LM4060 design eliminates the need for an external stabilizing capacitor and provides stability with capacitive loads up to 4.7μF.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Current (I_R)

In a conventional shunt regulator application (Figure 8-1), an external series resistor (R_S) is connected between the supply voltage and the LM4060-Q1. R_S determines the current that flows through the load (I_L) and the LM4060-Q1 (I_R). Since load current and supply voltage varies, R_S has to be small enough to supply at least the maximum I_{RMIN} (spec. table) to the LM4060-Q1 even when the supply voltage is at the minimum and the load current is at the maximum value. When the supply voltage is at the maximum and I_L is at the minimum, R_S has to be large enough so that the current flowing through the LM4060 is less than 50mA.

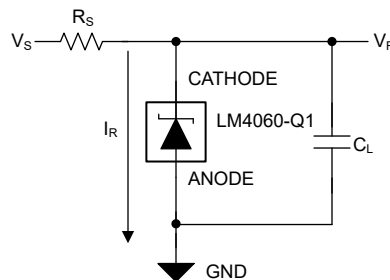


Figure 8-1. LM4060-Q1 Typical Diagram

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_R), and the LM4060-Q1 reverse breakdown voltage, V_R .

$$R_S = \frac{V_S - V_R}{I_L + I_R} \quad (1)$$

8.4 Device Functional Modes

The LM4060-Q1 operates in closed loop due to the fact that the feedback is internal to the device. Additionally, the output voltage cannot be adjusted for the same reason. The output voltage is regulated in a closed loop, provided the R_S (see Figure 8-1) resistor is sized to deliver the current to the cathode within the limits specified for operation.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

The following sections describe in detail how to properly use this device. As this device has many applications and setups, there are many situations that this data sheet cannot characterize in detail and vary from these applications depending on the requirements of the final application.

9.2.1 Design: LM4060-Q1 Precision Power Supply and Voltage Reference

The LM4060-Q1 combination of high-precision with high current sink can be the power supply and voltage reference to a MCU. In [Figure 9-1](#), the device is able to support the load current required by both the MCU VDD pin and REF pin. The main design consideration is the R_S resistor that needs to be sized to reduce current draw but supply the load under all conditions.

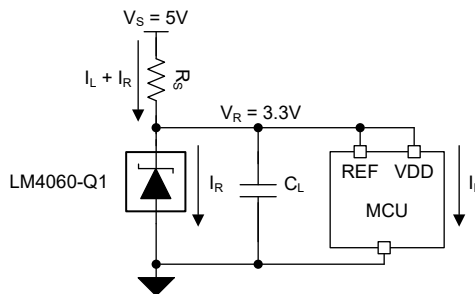


Figure 9-1. LM4060-Q1 Voltage Reference with MCU Load

9.2.1.1 Design Requirements

For this design the goal is to design R_S to minimize current consumption and function worst case conditions. Use the parameters listed in [Table 9-1](#) as the input parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	4.8V to 5.2V
Input voltage typical	5V
Output voltage	3.3V
Minimum cathode current	60 μ A
Typical MCU VDD current	12mA
Maximum MCU VDD current	20mA
Typical MCU REF current	130 μ A
Maximum MCU REF current	150 μ A

9.2.1.2 Detailed Design Procedure

R_S sets the cathode current of the shunt reference and is calculated using Equation 2. The resistor R_S must be selected such that current I_R remains in the operational region of the part for the entire V_S range and load current range I_L .

$$R_S = \frac{V_S - V_R}{I_L + I_R} \quad (2)$$

The two extremes to consider are V_S at the minimum, and the load at the maximum, where R_S must be small enough for I_R to remain above I_{RMIN} . For this design, design I_R with a small margin of current for a total of 0.1mA. This design makes the maximum R_S required to maintain operation at the worst case conditions to be 74Ω.

$$R_{SMAX} = \frac{V_{SMIN} - V_R}{I_{LMAX} + I_R} = \frac{4.8V - 3.3V}{20mA + 0.15mA + 0.1mA} = 74\Omega \quad (3)$$

The other extreme is V_S at the maximum, and the load at the minimum, where R_S must be large enough to maintain $I_R < I_{RMAX}$. For this design, the assumption is that the load is off. The calculated I_{RMAX} is 25.6mA, which is less than the maximum the device can support.

$$I_{RMAX} = \frac{V_{SMAX} - V_R}{R_S} - I_{LMIN} = \frac{5.2V - 3.3V}{74\Omega} = 25.6mA \quad (4)$$

The same equation above is used to find out the typical current the device sinks.

$$I_R = \frac{V_S - V_R}{R_S} - I_L = \frac{5V - 3.3V}{74\Omega} - 12mA - 0.13mA = 10.8mA \quad (5)$$

9.2.1.3 Application Curves

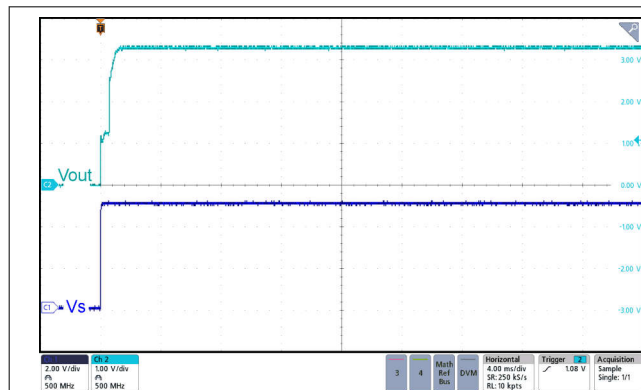


Figure 9-2. LM4060-Q1 Start-Up With $C_L = \text{Open}$, $I_R = 0\text{mA}$, Variant: LM4060A33EDBZRQ1

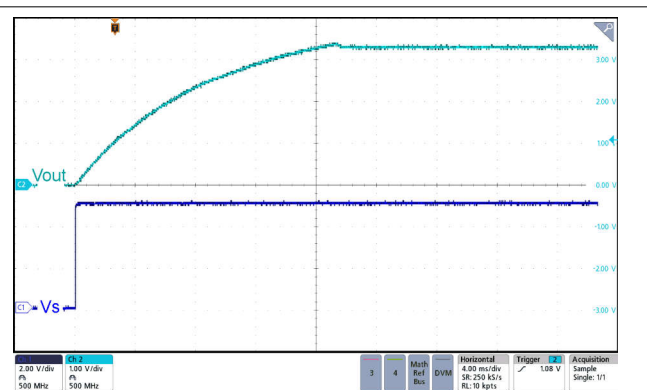


Figure 9-3. LM4060-Q1 Start-Up With $C_L = 1\mu\text{F}$, $I_R = 0\text{mA}$, Variant: LM4060A33EDBZRQ1

9.3 Power Supply Recommendations

Noise on the power supply input to R_S can affect output noise performance. Noise performance can be reduced by using an optional bypass capacitor at the input side of R_S and Ground. TI recommends a 0.1 μ F ceramic capacitor or higher.

9.3.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

Use [Equation 6](#) to calculate the maximum continuous allowable power dissipation for the device in a given package:

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (6)$$

[Equation 7](#) calculates the actual power being dissipated in the device:

$$P_D = V_R \times I_R \quad (7)$$

[Equation 6](#) and [Equation 7](#) establish the relationship between the maximum power dissipation allowed due to thermal consideration and the continuous current capability of the device. Use these two equations to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) can be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) have to be derated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part and package in the application ($R_{\theta JA}$), as given by [Equation 8](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (8)$$

9.4 Layout

9.4.1 Layout Guidelines

Place R_S as close to the cathode as possible. If an input and output capacitor is used, place this as close to the reference as possible.

9.4.2 Layout Example

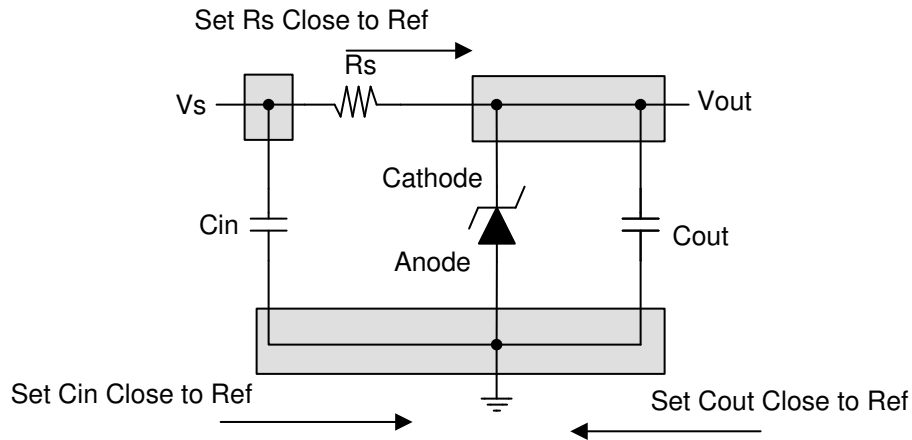


Figure 9-4. Layout Recommendation

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Documentation Support

10.2.1 Related Documentation

Texas Instruments, [Voltage Reference Selection Basics white paper](#)

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4060A12EDBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P25Q
LM4060A25EDBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2P5XQ
LM4060A30EDBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3P0XQ
LM4060A33EDBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3P3XQ
LM4060A50EDBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5P0XQ

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM4060-Q1 :

- Catalog : [LM4060](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

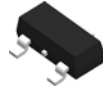
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4060A12EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A25EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A30EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A33EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A50EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4060A12EDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A25EDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A30EDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A33EDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A50EDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

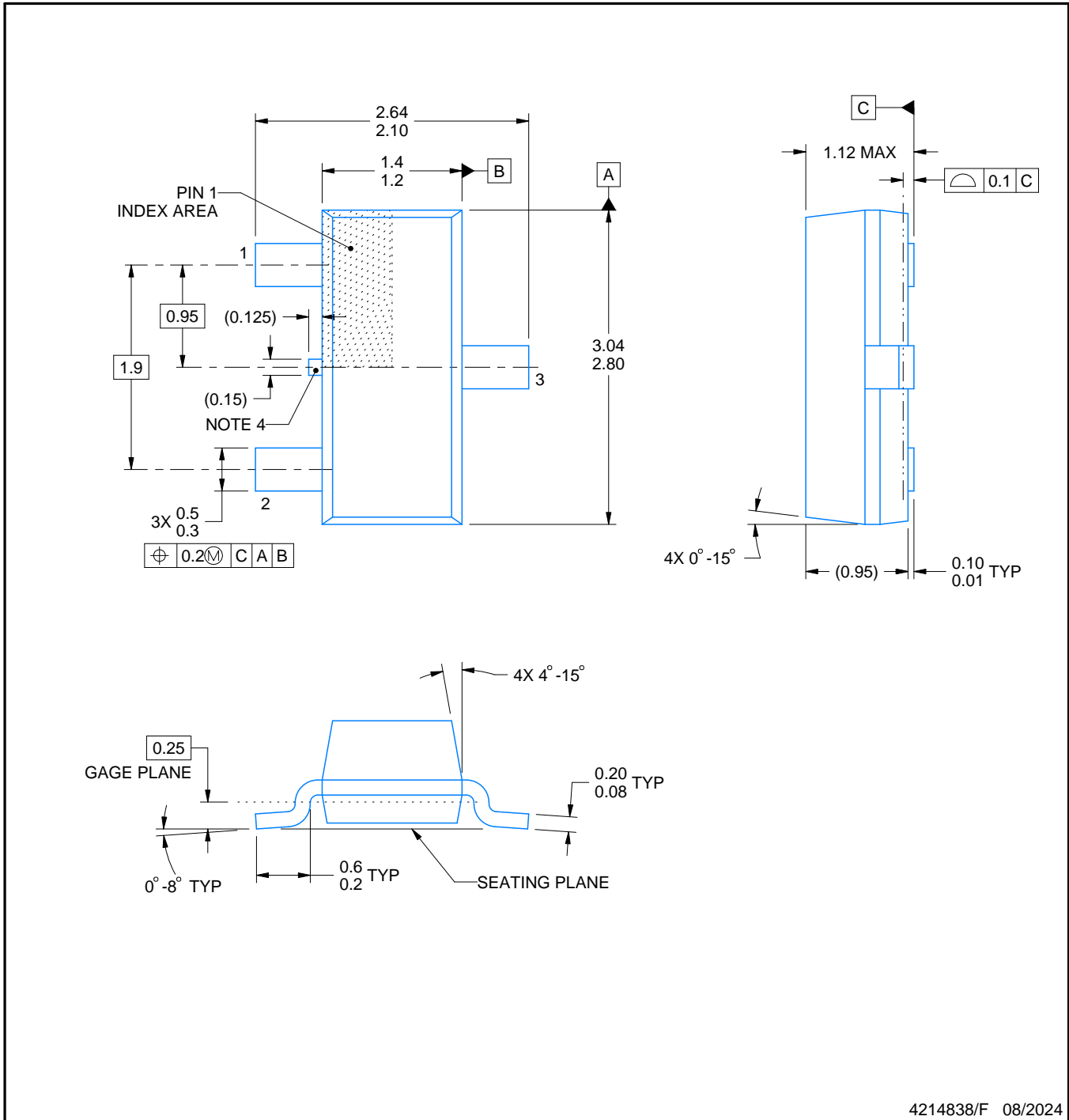
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

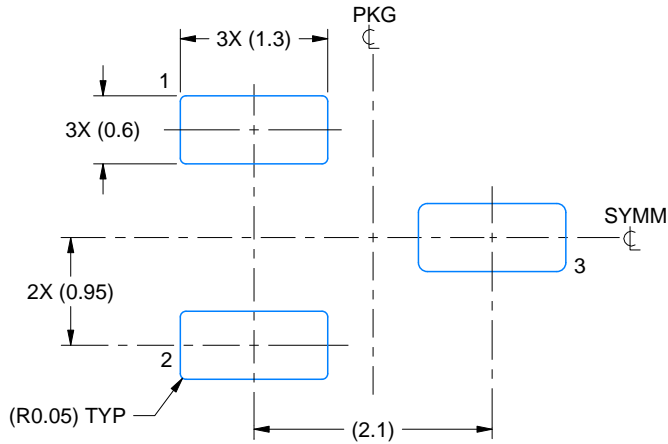
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

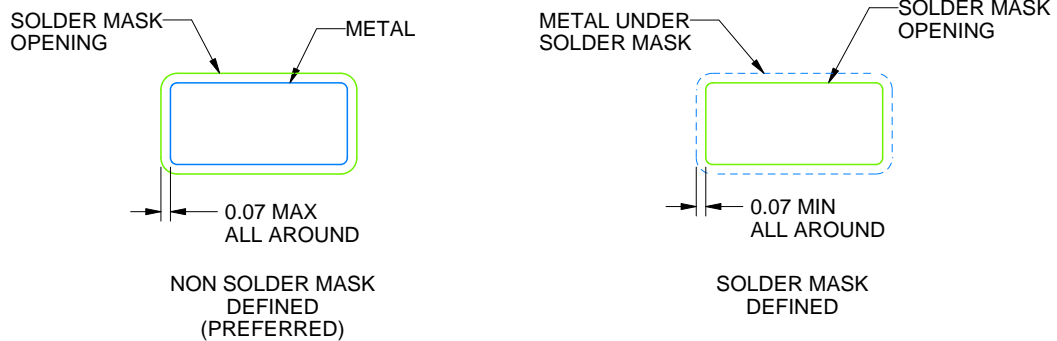
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

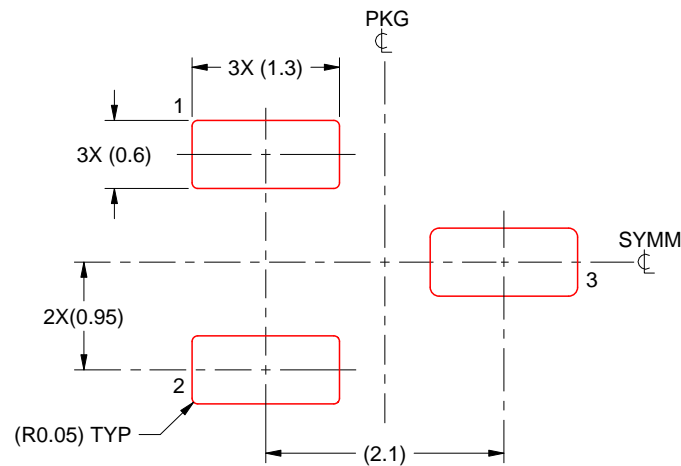
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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