LM4865 Boomer® Audio Power Amplifier Series 750 mW Audio Power Amplifier with DC Volume Control and Headphone Switch

Check for Samples: LM4865

FEATURES

- **DC Voltage Volume Control**
- **Headphone Amplifier Mode**
- **"Click and Pop" Suppression**
- **Shutdown Control When Volume Control Pin Is Low**
- **Thermal Shutdown Protection**

APPLICATIONS

- **GSM Phones and Accessories, DECT, Office Phones**
- **Hand Held Radio**
- **Other Portable Audio Devices**

KEY SPECIFICATION

- **P_O at 1.0% THD+N Into 8Ω SOIC, Micro SMD 750 mW (typ)**
- **P_O at 10% THD+N Into 8Ω SOIC, Micro SMD 1W (typ)**
- **Shutdown Current 0.7µA(typ)**
- **Supply Voltage Range 2.7V to 5.5 V**

CONNECTION DIAGRAMS

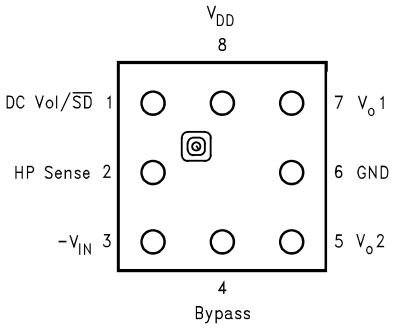

Figure 1. Micro SMD Package (Top View)

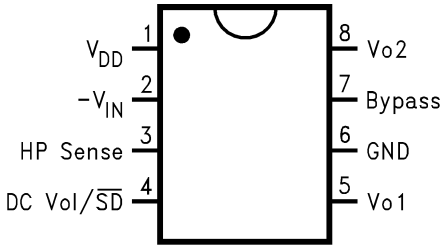

Figure 2. Small Outline Package (SOIC) (Top View)
Mini Small Outline Package (VSSOP)
See Package Number D, DGK

DESCRIPTION

The LM4865 is a mono bridged audio power amplifier with DC voltage volume control. The LM4865 is capable of delivering 750mW of continuous average power into an 8Ω load with less than 1% THD when powered by a 5V power supply. Switching between bridged speaker mode and headphone (single ended) mode is accomplished using the headphone sense pin. To conserve power in portable applications, the LM4865's micropower shutdown mode (I_Q = 0.7µA, typ) is activated when less than 300mV is applied to the DC Vol/$\overline{SD}$ pin.

Boomer audio power amplifiers are designed specifically to provide high power audio output while maintaining high fidelity. They require few external components and operate on low supply voltages.

TYPICAL APPLICATION

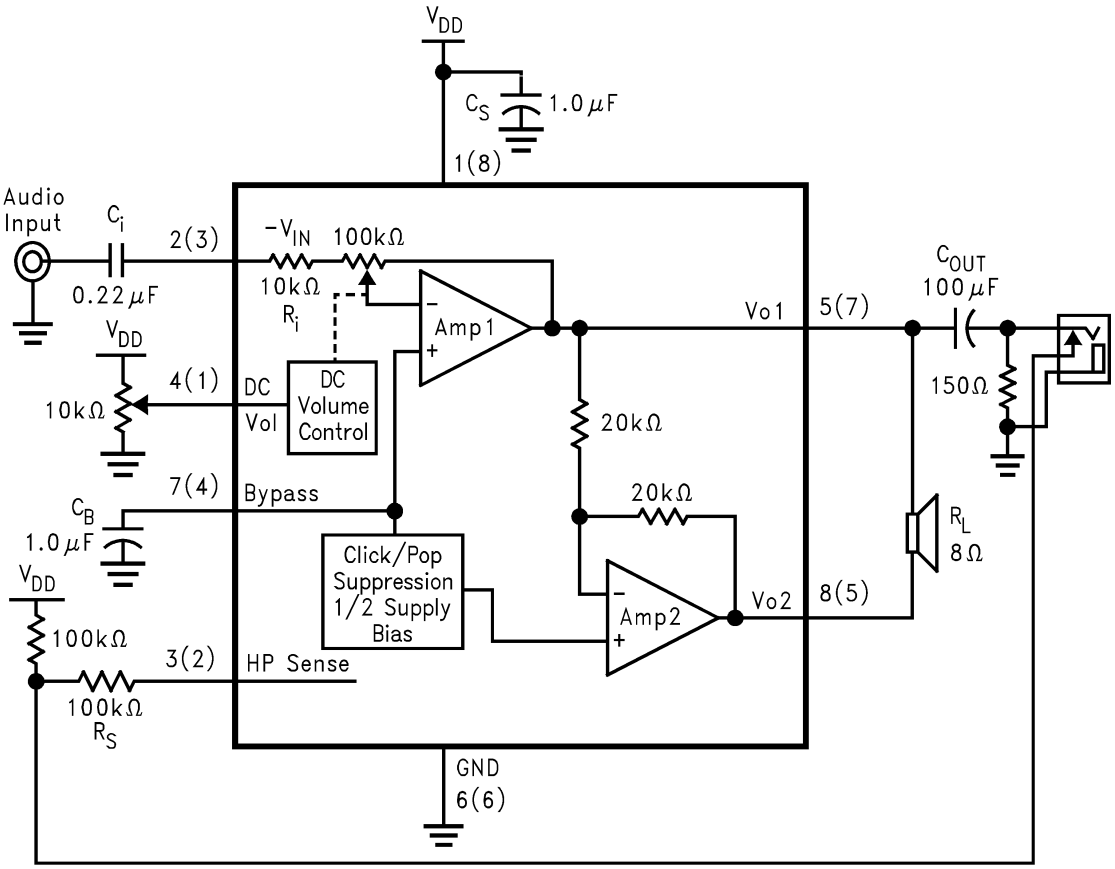

Figure 3. Typical Audio Amplifier Application Circuit
(Numbers in ( ) are specific to the micro SMD package)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation (3)		Internally Limited
ESD Susceptibility (4)		2000V
ESD Susceptibility (5)		200V
Junction Temperature		150°C
Soldering Information	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JC} (SOIC)	35°C/W
	θ_{JA} (SOIC)	150°C/W
	θ_{JC} (VSSOP)	56°C/W
	θ_{JA} (VSSOP)	190°C/W
	θ_{JA} (micro SMD)	150°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value, however, is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4865M, T_{JMAX} = 150°C.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF–240pF discharged through all pins.

OPERATING RATINGS

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ +85°C
Supply Voltage		2.7V ≤ V_{DD} ≤ 5.5V

ELECTRICAL CHARACTERISTICS (1)(2)

The following specifications apply for V_{DD} = 5V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4865			
			Min(3)	Typical(4)	Max(3)	Units
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, HP Sense = 0V		4	7	mA
		V_{IN} = 0V, I_O - 0A, HP Sense = 5V		3.5	6	mA
I_{SD}	Shutdown Current	$V_{PIN4} \leq$ 0.3V		0.7		µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V		5	50	mV
P_O	Output Power	THD = 1% (max), HP Sense < 0.8V, f = 1kHz, R_L = 8Ω	500	750		mW
		THD = 10% (max), HP Sense < 0.8V, f = 1kHz, R_L = 8Ω		1.0		W
		THD + N = 1%, HP Sense > 4V, f = 1kHz, R_L = 32Ω		80		mW
		THD = 10%, HP Sense > 4V, f = 1kHz, R_L = 32Ω		110		mW
THD+N	Total Harmonic Distortion + Noise	P_O = 300 mWrms, f = 20Hz–20kHz, R_L = 8Ω		0.6		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVrms, R_L = 8Ω, C_B = 1.0 µF, f = 1kHz		50		dB
$Gain_{RANGE}$	Single-Ended Gain Range	Gain with $V_{PIN4} \geq$ 4.0V, (80% of V_{DD})	18.8	20		dB
		Gain with $V_{PIN4} \leq$ 0.9V, (18% of V_{DD})	−70	−72		dB
V_{IH}	HP Sense High Input Voltage		4			V
V_{IL}	HP Sense Low Input Voltage				0.8	V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value, however, is a good indication of device performance.
(3) Limits are ensured to AOQL (Average Outgoing Quality Level).
(4) Typicals are measured at 25°C and represent the parametric norm.

EXTERNAL COMPONENTS DESCRIPTION

(Figure 3)

Components		Functional Description
1.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. It also creates a highpass filter with the internal R_i. The designer should note that10kOhm<(Ri)<110kOhm.Therefore $f_c = 1/(2\pi R_i C_i)$. Refer to the section, PROPERLY SELECTING EXTERNAL COMPONENTS , for an explanation of how to determine the value of C_i.
2.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
3.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPERLY SELECTING EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency

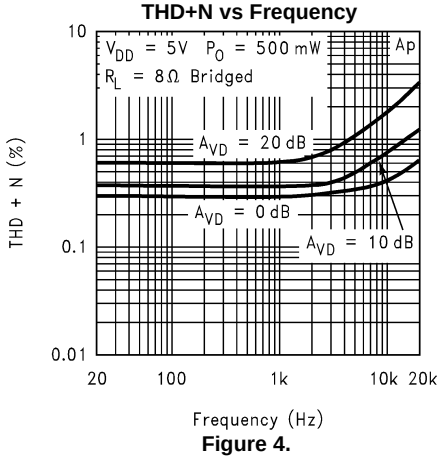

Figure 4.

THD+N vs Frequency

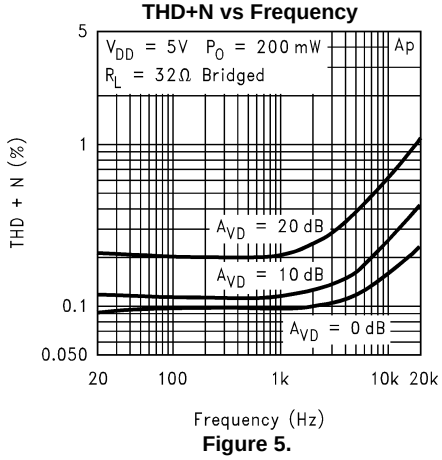

Figure 5.

THD+N vs Output Power

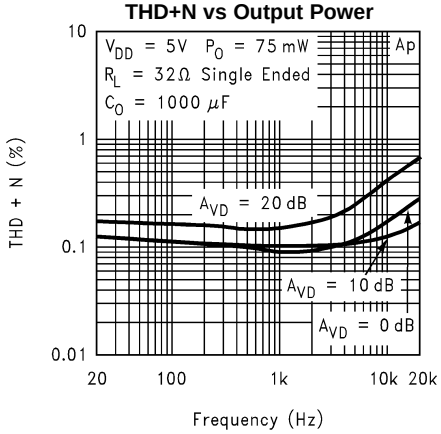

Figure 6.

THD+N vs Output Power

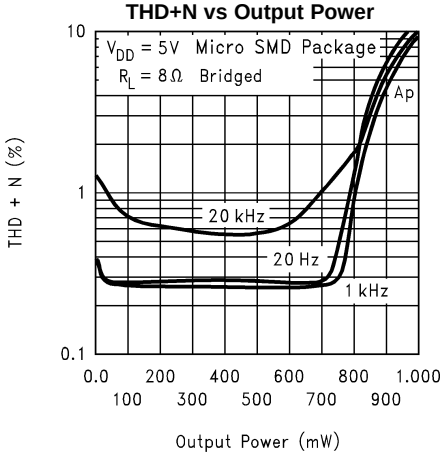

Figure 7.

THD+N vs Output Power

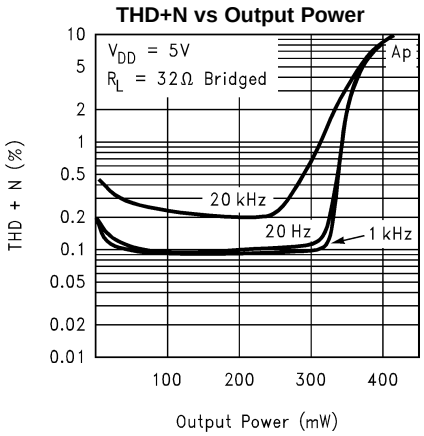

Figure 8.

THD+N vs Output Power

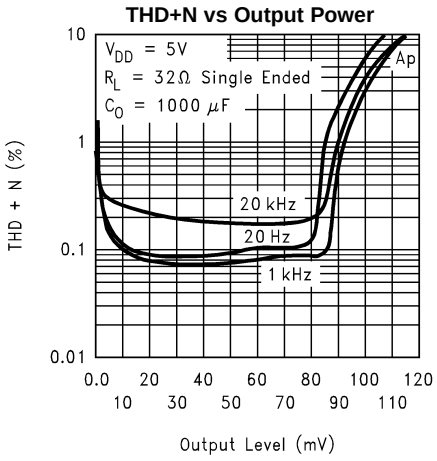

Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Dissipation vs Load Resistance

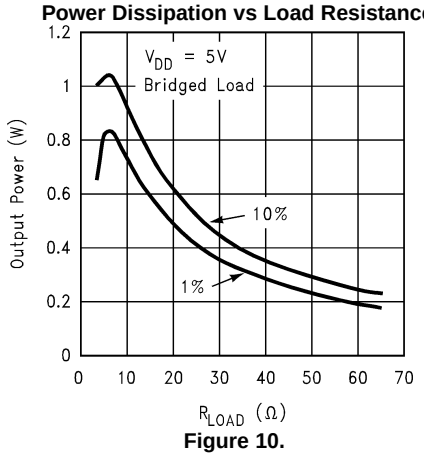

Figure 10.

Power Dissipation vs Output Power

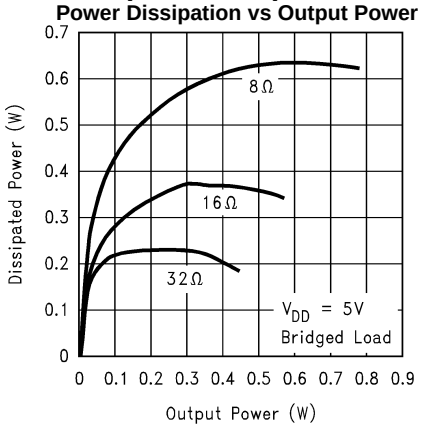

Figure 11.

Power Derating Curve

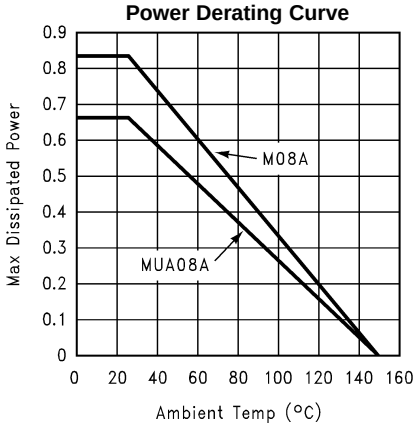

Figure 12.

Clipping Voltage vs RL

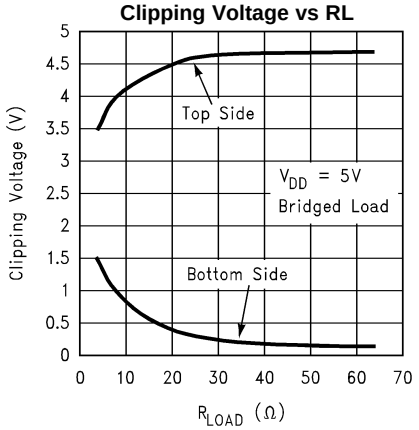

Figure 13.

Noise Floor

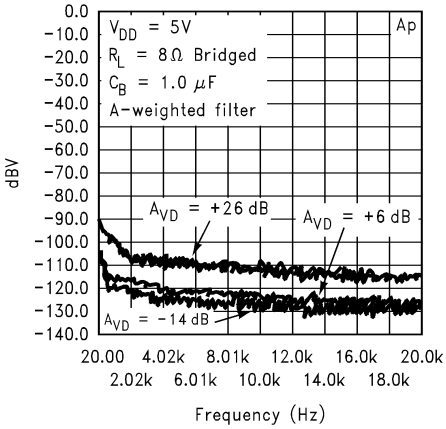

Figure 14.

Frequency Response vs Input Capacitor Size

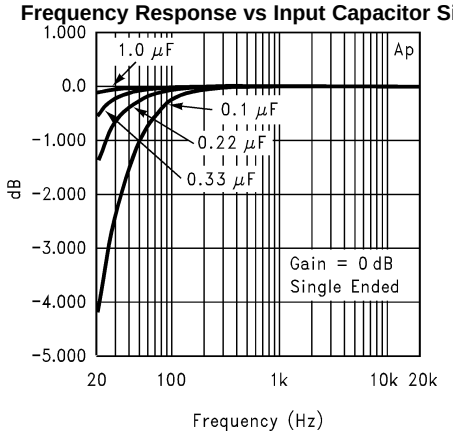

Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Supply Rejection Ratio

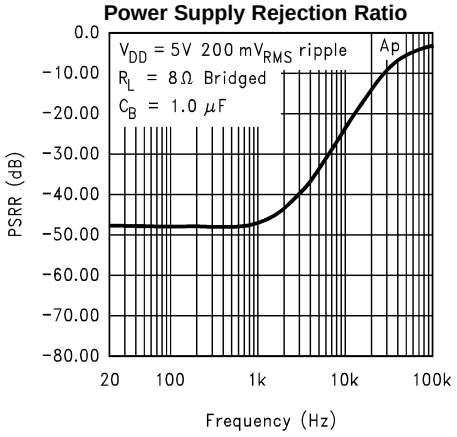

Figure 16.

Attenuation Level vs DC-Vol Amplitude

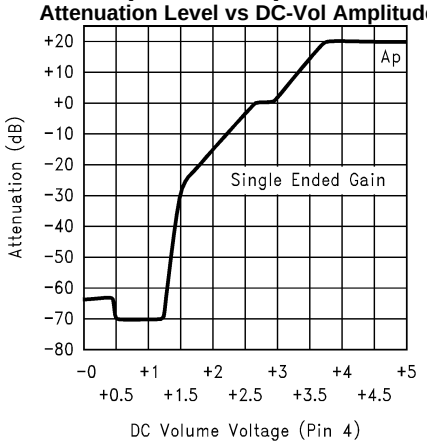

Figure 17.

THD+N vs Frequency

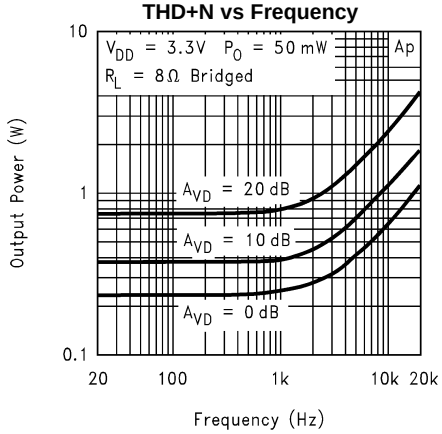

Figure 18.

THD+N vs Frequency

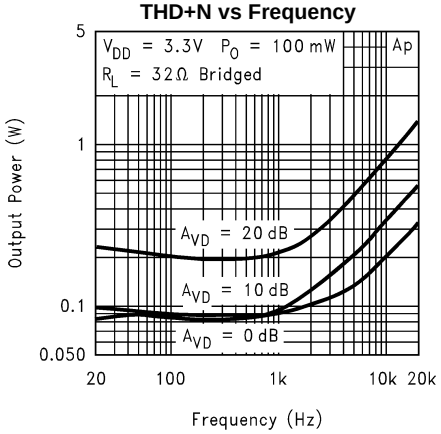

Figure 19.

THD+N vs Frequency

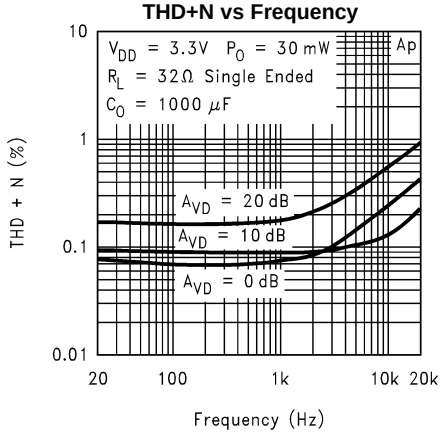

Figure 20.

THD+N vs Output Power

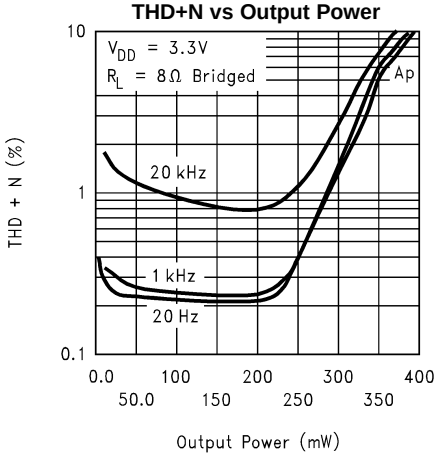

Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power

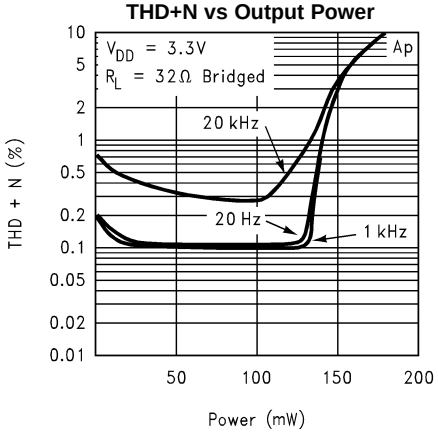

Figure 22.

THD+N vs Output Power

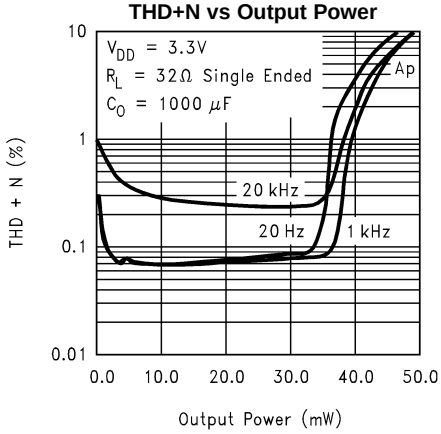

Figure 23.

Output Power vs Load Resistance

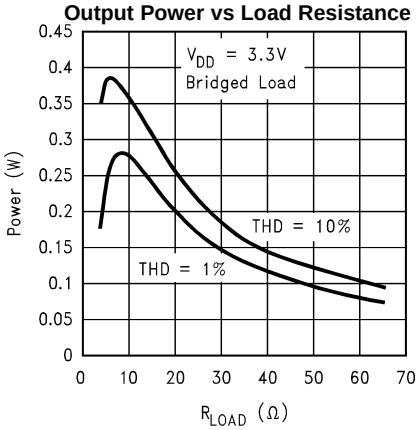

Figure 24.

Clipping Voltage vs Supply Voltage

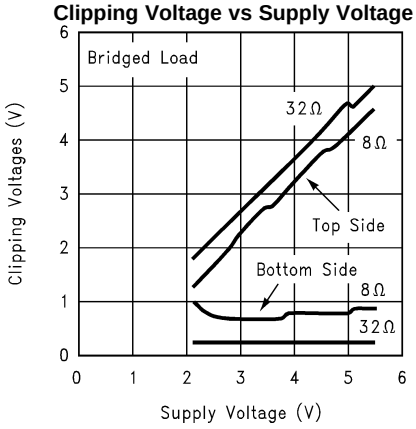

Figure 25.

Output Power vs Supply Voltage

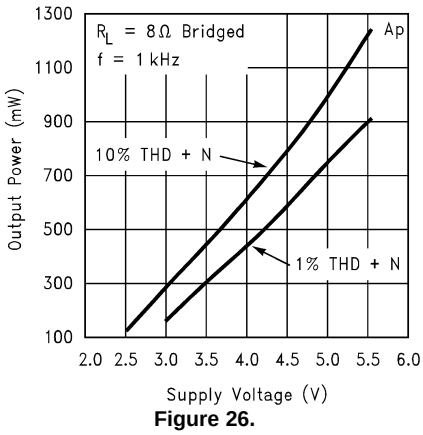

Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Power vs Supply Voltage

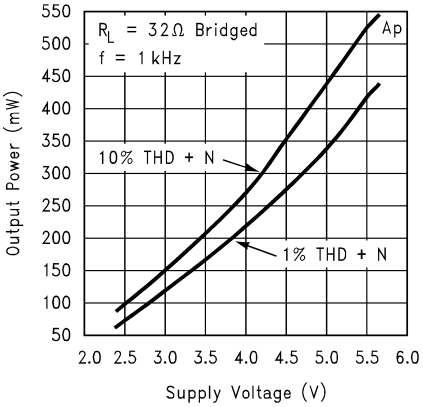

Figure 27.

Supply Current vs Supply Voltage

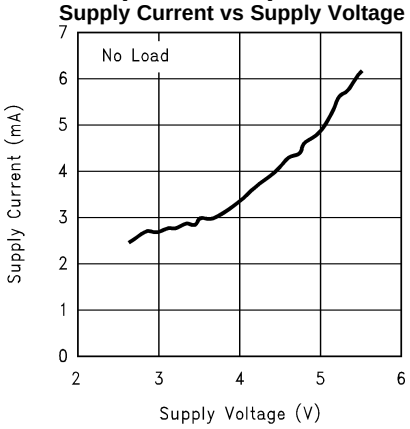

Figure 28.

APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 3, the LM4865 consists of two operational amplifiers internally. An external DC voltage sets the closed-loop gain of the first amplifier, whereas two internal 20kΩ resistors set the second amplifier's gain at -1. The LM4865 can be used to drive a speaker connected between the two amplifier outputs or a monaural headphone connected between V_O1 and GND.

Figure 3 shows that the output of Amp1 serves as the input to Amp2. This results in both amplifiers producing signals that are identical in magnitude, but 180° out of phase.

Taking advantage of this phase difference, a load placed between V_O1 and V_O2 is driven differentially (commonly referred to as “bridge mode“). This mode is different from single-ended driven loads that are connected between a single amplifier's output and ground.

Bridge mode has a distinct advantage over the single-ended configuration: its differential drive to the load doubles the output swing for a specified supply voltage. This results in four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output assumes that the amplifier is not current limited or the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across load. This results from biasing V_O1 and V_O2 at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single supply amplifier's half-supply bias voltage across the load. The current flow created by the half-supply bias voltage increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful bridged or single-ended amplifier. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \tag{1}$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation point for a bridge amplifier operating at the same given conditions.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \tag{2}$$

The LM4865 has two operational amplifiers in one package and the maximum internal power dissipation is 4 times that of a single-ended amplifier. However, even with this substantial increase in power dissipation, the LM4865 does not require heatsinking. From Equation 2, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 633 mW. The maximum power dissipation point obtained from Equation 2 must not be greater than the power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} – T_A)/\theta_{JA} \tag{3}$$

For the micro SMD and SOIC packages, θ_{JA} = 150°C/W. The VSSOP package has a 190°C/W θ_{JA}. T_{JMAX} = 150°C for the LM4865. For a given ambient temperature T_A, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 2 is greater than that of Equation 3, then either decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. For a typical application using the micro SMD or SOIC packaged LM4865, a 5V power supply, and an 8Ω load, the maximum ambient temperature that does not violate the maximum junction temperature is approximately 55°C. The maximum ambient temperature for the VSSOP package with the same conditions is approximately 30°C. These results further assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power decreases. Refer to the TYPICAL PERFORMANCE CHARACTERISTICS curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitors connected to the bypass and power supply pins should be placed as close to the LM4865 as possible. The capacitor connected between the bypass pin and ground improves the internal bias voltage's stability, producing improved PSRR. The improvements to PSRR increase as the bypass pin capacitor value increases. Typical applications employ a 5V regulator with 10µF and a 0.1µF filter capacitors that aid in supply stability. Their presence, however does not eliminate the need for bypassing the supply nodes of the LM4865. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, PROPERLY SELECTING EXTERNAL COMPONENTS), system cost, and size constraints.

DC VOLTAGE VOLUME CONTROL

The LM4865 has internal volume control that is controlled by the DC voltage applied its DC Vol/$\overline{SD}$ pin (pin 5 on the micro SMD and pin 4 on the VSSOP and SOIC packages). The volume control's input range is from GND to V_{DD}. A graph showing a typical volume response versus input control voltage is shown in the TYPICAL PERFORMANCE CHARACTERISTICS section. The DC Vol/$\overline{SD}$ pin also functions as the control pin for the LM4865's micropower shutdown feature. See the MUTE AND SHUTDOWN FUNCTION section for more information.

Like all volume controls, the LM4865's internal volume control is set while listening to an amplified signal that is applied to an external speaker. The actual voltage applied to the DC Vol/$\overline{SD}$ pin is a result of the volume a listener desires. As such, the volume control is designed for use in a feedback system that includes human ears and preferences. This feedback system operates quite well without the need for accurate gain. The user simply sets the volume to the desired level as determined by their ear, without regard to the actual DC voltage that produces the volume. Therefore, the accuracy of the volume control is not critical, as long as volume changes monotonically and step size is small enough to reach a desired volume that is not too loud or too soft. Since gain accuracy is not critical, there will be volume variation from part-to-part even with the same applied DC control voltage. The gain of a given LM4865 can be set with a fixed external voltage, but another LM4865 may require a different control voltage to achieve the same gain. Figure 29 is a curve showing the volume variation of twenty typical LM4865s as the voltage applied to the DC Vol/$\overline{SD}$ pin is varied. For gains greater than unity, the typical part-to-part variation can be as large as 8dB for the same control voltage.

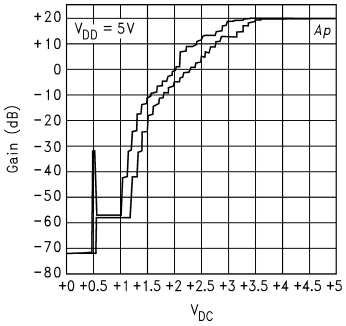

Figure 29. Typical Part-to-Part Gain Variation as a Function of DC-Vol Control Voltage

MUTE AND SHUTDOWN FUNCTION

The LM4865's mute and shutdown functions are controlled through the DC Vol/$\overline{SD}$ pin. Mute is activated by applying a voltage in the range of 500mV to 1V. A typical attenuation of 75dB is achieved is while mute is active. The LM4865's micropower shutdown mode turns off the amplifier's bias circuitry. The micropower shutdown mode is activated by applying less than 300mV_{DC} to the DC Vol/$\overline{SD}$ pin. When shutdown is active, they supply current is reduced to 0.7µA (typ). A degree of uncertainty exists when the voltage applied to the DC Vol/$\overline{SD}$ pin is in the range of 300mV to 500mV. The LM4865 can be in mute, still fully powered, or in micropower shutdown and fully muted. In mute mode, the LM4865 draws the typical quiescent supply current. The DC Vol/$\overline{SD}$ pin should be tied to GND for best shutdown mode performance. As the DC Vol/$\overline{SD}$ is increased above 0.5V the amplifier will follow the attenuation curve in TYPICAL PERFORMANCE CHARACTERISTICS.

HP-Sense FUNCTION

Applying a voltage between 4V and V_{CC} to the LM4865's HP-Sense headphone control pin turns off Amp2 and mutes a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 30 shows the implementation of the LM4865's headphone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP-Sense pin (pin 3) at approximately 50mV. This 50mV enables the LM4865 and places it in bridged mode operation.

While the LM4865 operates in bridged mode, the DC potential across the load is essentially 0V. Since the HP-Sense threshold is set at 4V, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from V_O1 and allows R1 to pull the HP Sense pin up to V_{CC}. This enables the headphone function, turns off Amp2, and mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistor R2. Resistor R2 has negligible effect on output drive capability since the typical impedance of headphones is 32Ω. The output coupling capacitor blocks the amplifier's half supply DC voltage, protecting the headphones.

A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP Sense pin, a bridge-connected speaker is muted and Amp1 drives the headphones.

PROPERLY SELECTING EXTERNAL COMPONENTS

Optimizing the LM4865's performance requires properly selecting external components. Though the LM4865 operates well when using external components having wide tolerances, the best performance is achieved by optimizing component values.

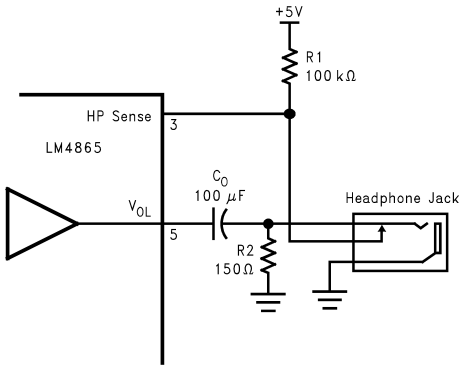

Figure 30. Headphone Circuit

Input Capacitor Value Selection

Amplification of the lowest audio frequencies requires high value input coupling capacitors. These high value capacitors can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. In application 5 using speakers with this limited frequency response, a large input capacitor will offer little improvement in system performance.

Figure 3 shows that the nominal input impedance (R_{IN}) is 10kΩ at maximum volume and 110kΩ at minimum volume. Together, the input capacitor, C_i, and R_{IN}, produce a -3dB high pass filter cutoff frequency that is found using Equation 4.

$$f_{-3\,dB} = \frac{1}{2\pi R_{IN} C_i} \tag{4}$$

As the volume changes from minimum to maximum, R_{IN} decrease from 110kΩ to 10kΩ. Equation 4 reveals that the -3dB frequency will increase as the volume increases. The nominal value of C_i for lowest desired frequency response should be calculated with R_{IN} = 10kΩ . As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation 4 is 0.1µF. The 0.22µF C_i shown in Figure 3 is optimized for a speaker whose response extends down to 75Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of the bypass capacitor C_B. Since C_B determines how fast the LM4865 turns on, its value is the most critical when minimizing turn-on pops. The slower the LM4865's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF, along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a clickless and popless shutdown function. Choosing C_i as small as possible helps minimize clicks and pops.

CLICK AND POP CIRCUITRY

The LM4865 contains circuitry that minimizes turn-on and shutdown transients or "clicks and pops". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4865's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the bypass pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the bypass pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the bypass pin is stable, the device becomes fully operational and the gain is set by the external voltage applied to the DC Vol/$\overline{SD}$ pin.

Although the bypass pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of CB and the turn-on time. Shown below are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	20ms
0.1µF	200ms
0.22µF	420ms
0.47µF	840ms
1.0µF	2sec

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops". In a single-ended configuration, the output coupling capacitor, C_{OUT}, is of particular concern. This capacitor discharges through an internal 20kΩ resistor. Depending on the size of C_{OUT}, the time constant can be relatively large. To reduce transients in single-ended mode, an external 1kΩ - 5kΩ resistor can be placed in parallel with the internal 20kΩ resistor. The tradeoff for using this resistor is increased quiescent current.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 31 through Figure 33 show the recommended two-layer PC board layout that is optimized for the SOIC-8 packaged LM4865 and associated external components. Figure 34 through Figure 38 show the recommended four-layer PC board layout for the micro SMD packaged LM4865. A four-layer board is recommended when using the micro SMD packaged LM4865: the two inner layers, one connected to the GND pin, the other to the V_{DD} pin, provide heatsinking. Both layouts are designed for use with an external 5V supply, 8Ω speakers, and 32Ω headphones. The schematic for both recommended PC board layouts is Figure 3.

Both circuit boards are easy to use. Apply a 5V supply voltage and ground to the board's V_{DD} and GND pads, respectively. Connect a speaker with an 8Ω minimum impedance between the board's -OUT and +OUT pads. For headphone use, the layout has provisions for a headphone jack, J1. When a jack is connected as shown, inserting a headphone plug automatically switches off the external speaker.

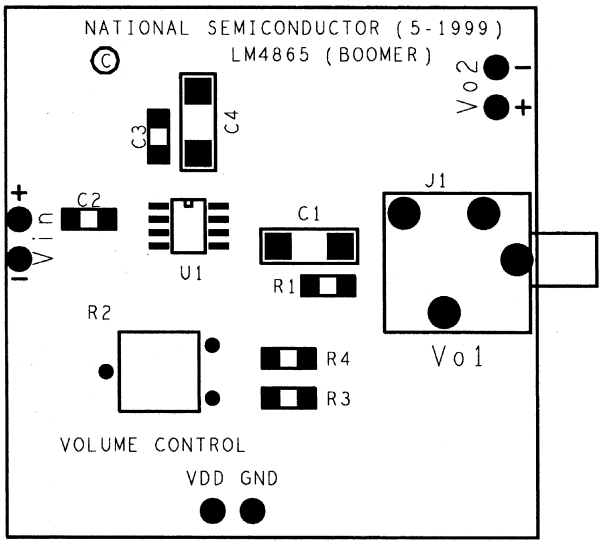

Figure 31. Recommended SOIC PC Board Layout: Component Side Silkscreen

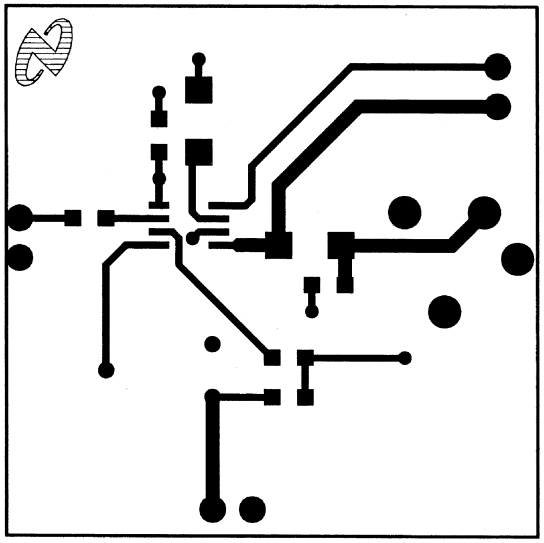

Figure 32. Recommended SOIC PC Board Layout: Component Side Layout

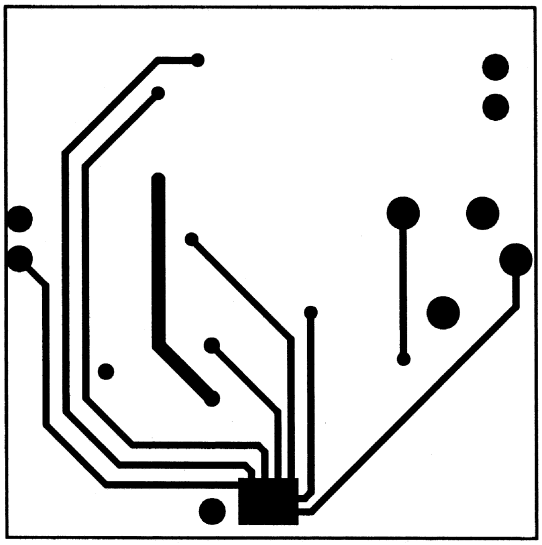

Figure 33. Recommended SOIC PC Board Layout: Bottom Side Layout

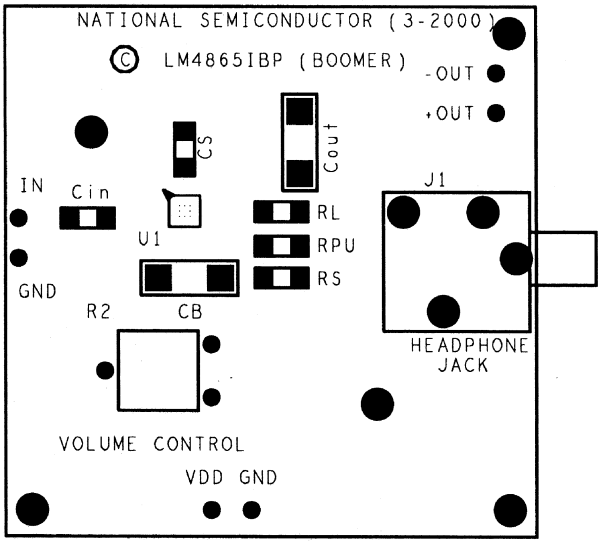

Figure 34. Recommended micro SMD PC Board Layout: Component Side Silkscreen

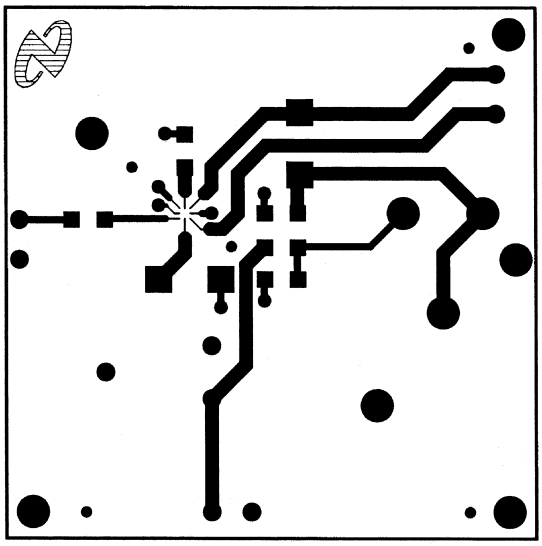

Figure 35. Recommended Micro SMD PC Board Layout: Component Side Layout

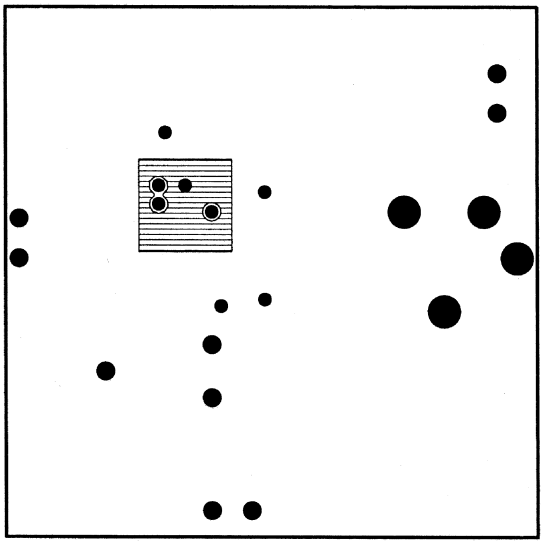

Figure 36. Recommended Micro SMD PC Board Layout: Inner Layer V_{CC} Layout

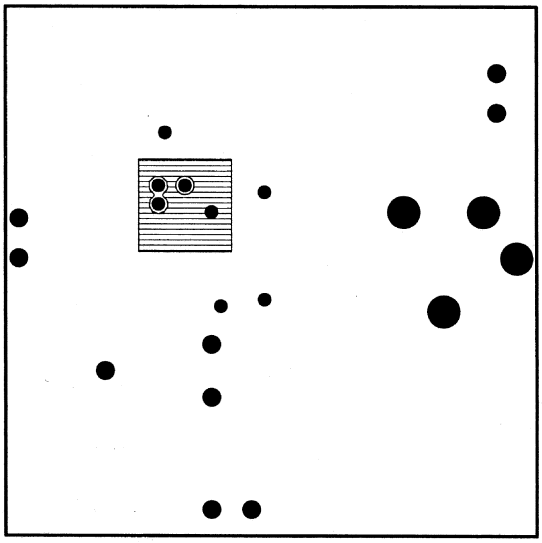

Figure 37. Recommended Micro SMD PC Board Layout: Inner Layer Ground Layout

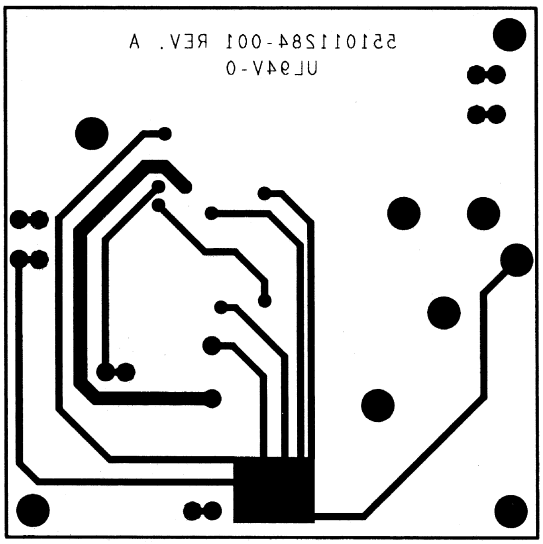

Figure 38. Recommended Micro SMD PC Board Layout: Bottom Side Layout

REVISION HISTORY

Changes from Revision F (May 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4865M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM48 65M	Samples
LM4865MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	Z65	Samples
LM4865MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	Z65	Samples
LM4865MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM48 65M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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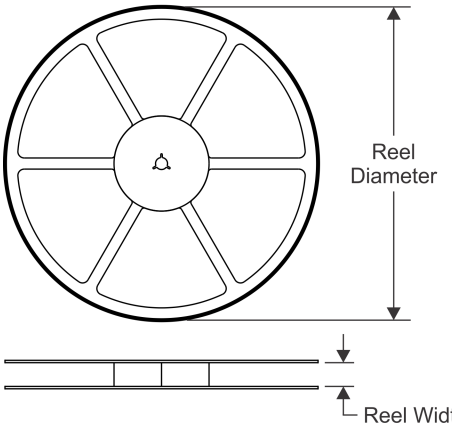
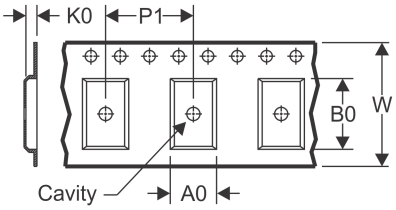
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

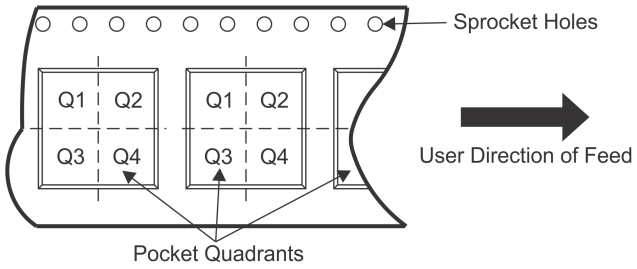


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

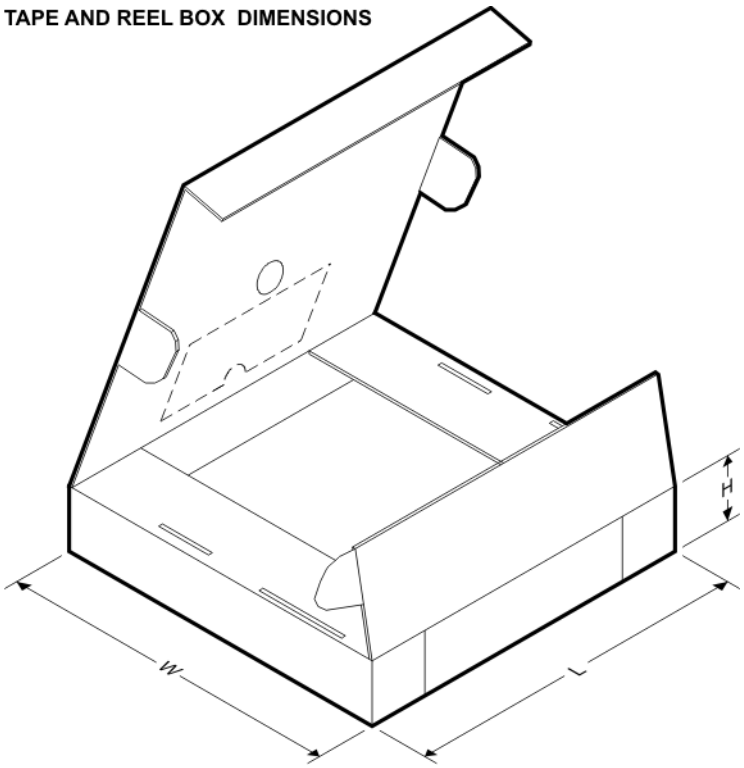
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4865MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4865MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4865MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

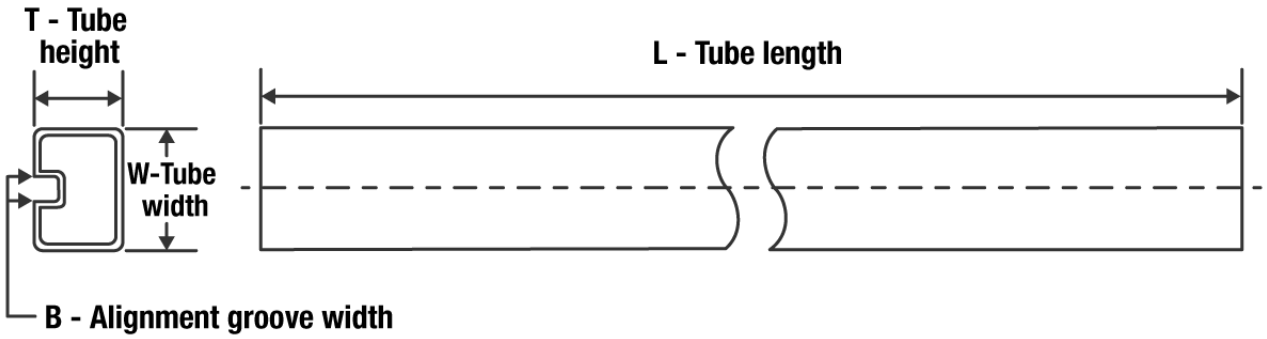
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4865MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4865MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM4865MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

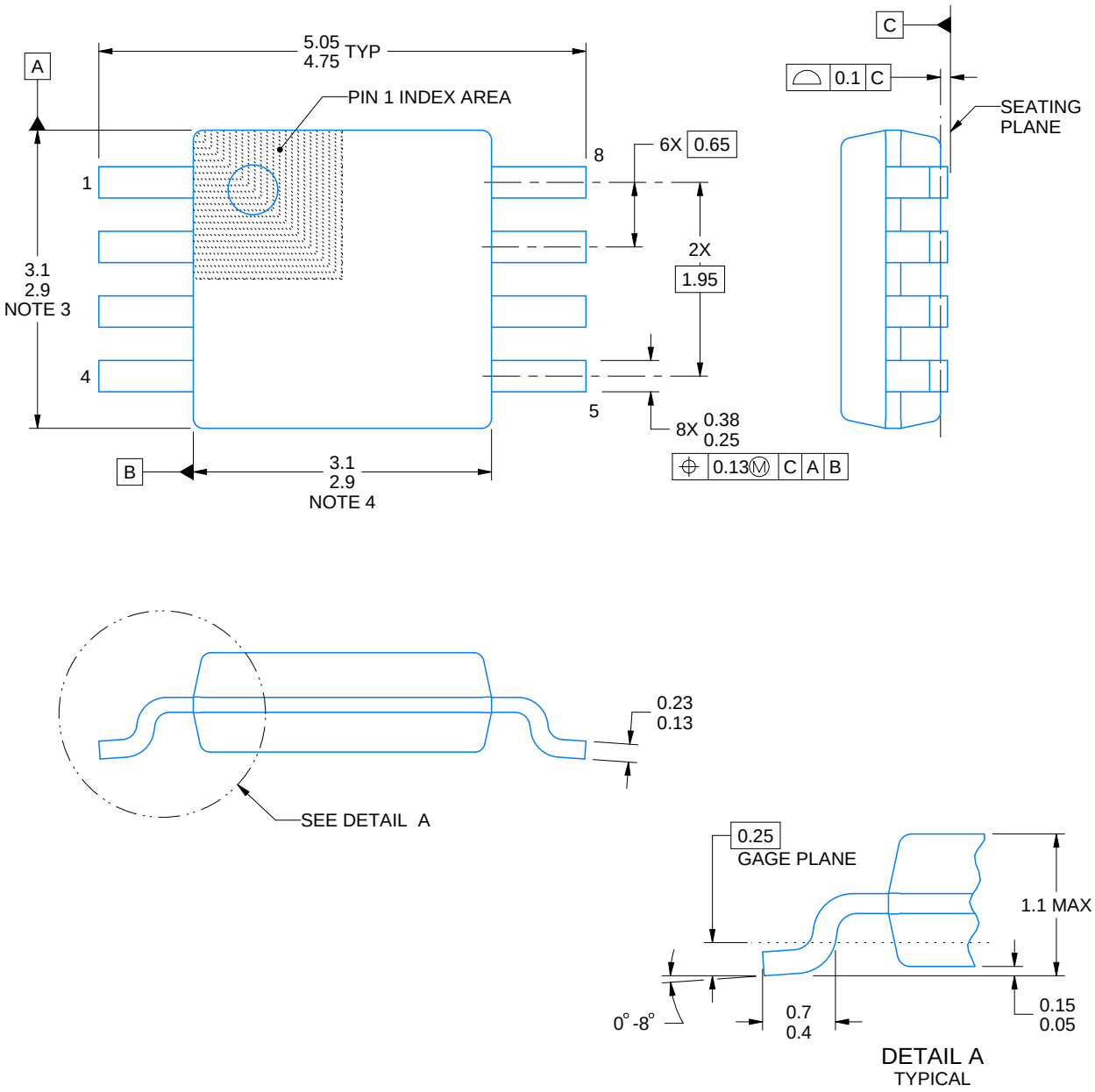
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4865M/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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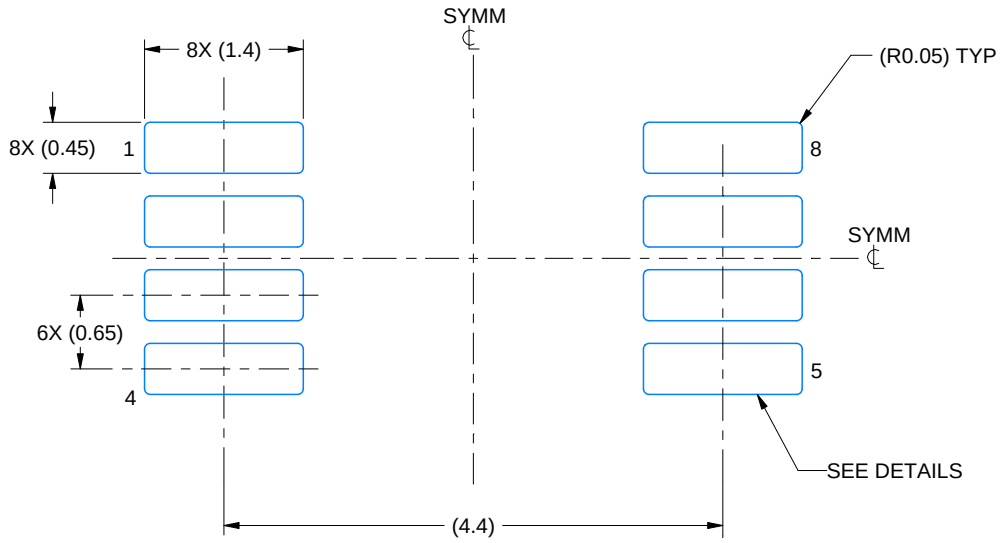
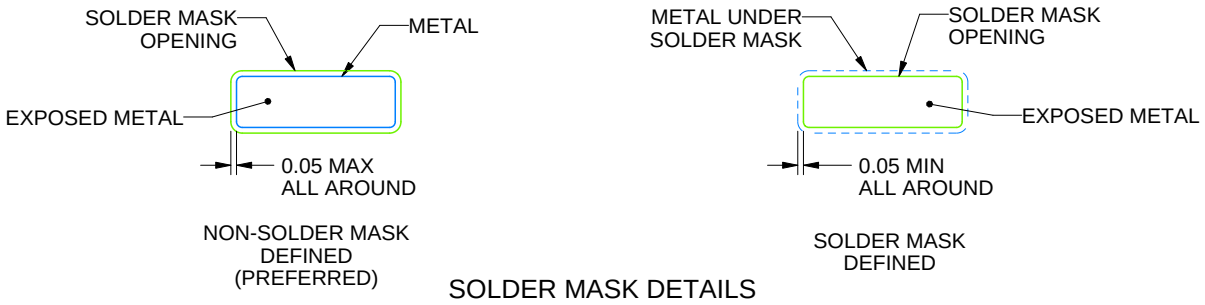
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

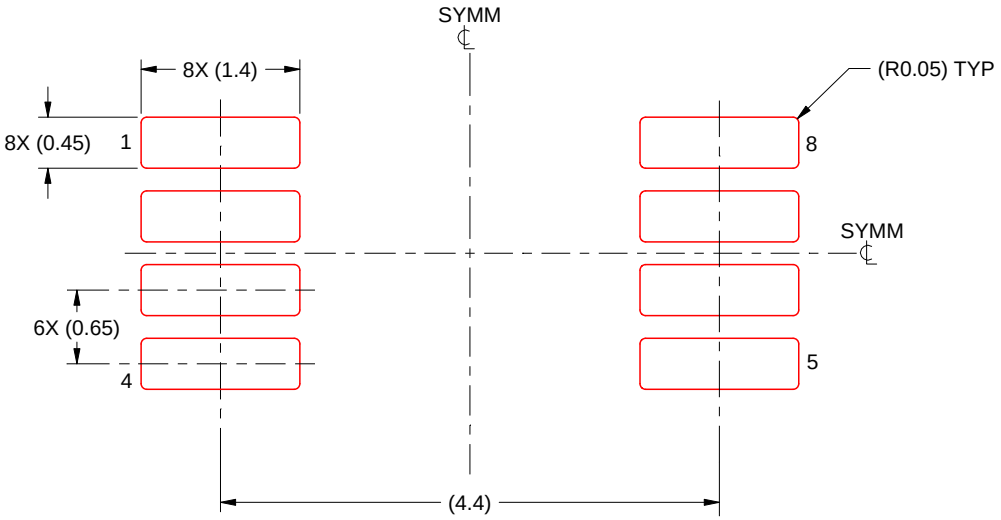


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

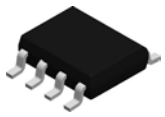


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

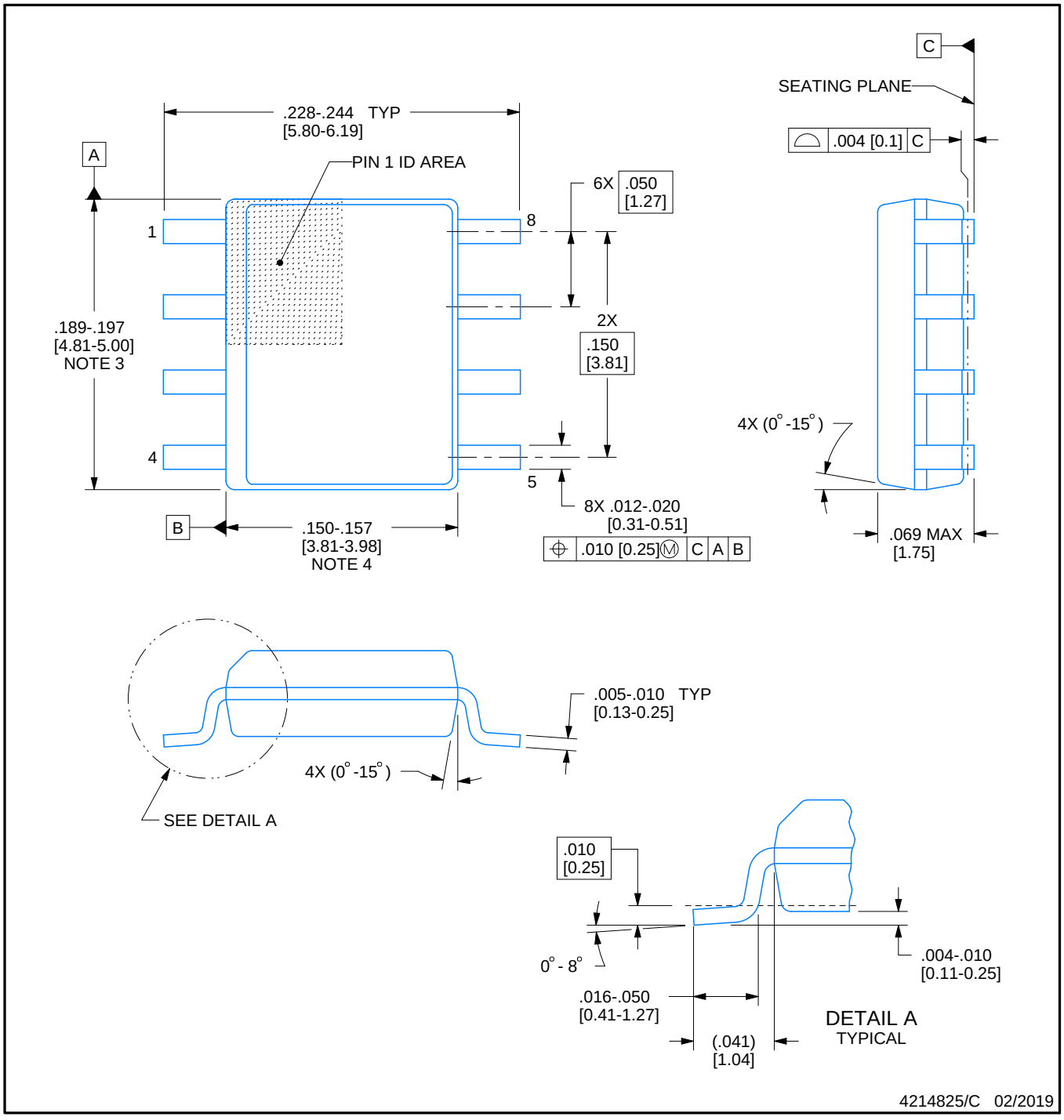


PACKAGE OUTLINE

D0008A

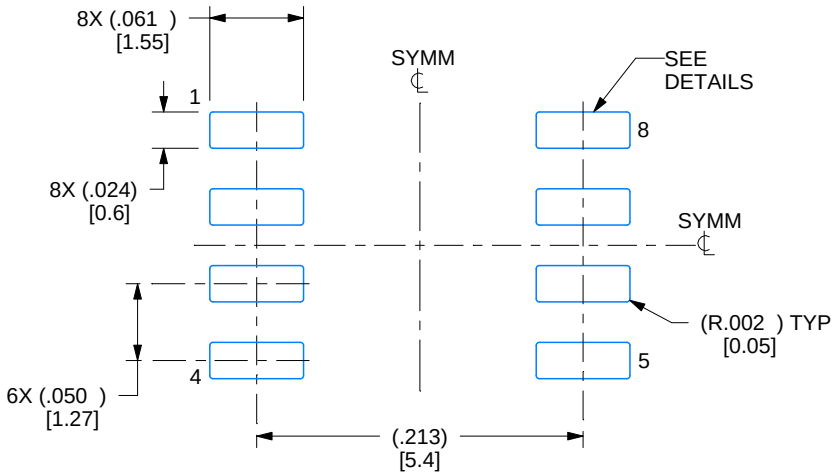
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

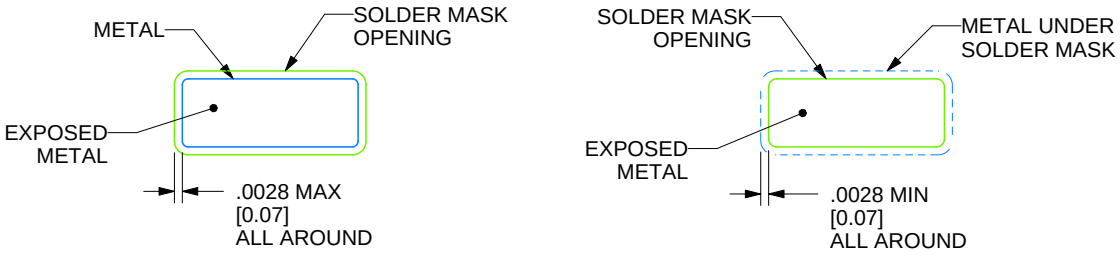


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

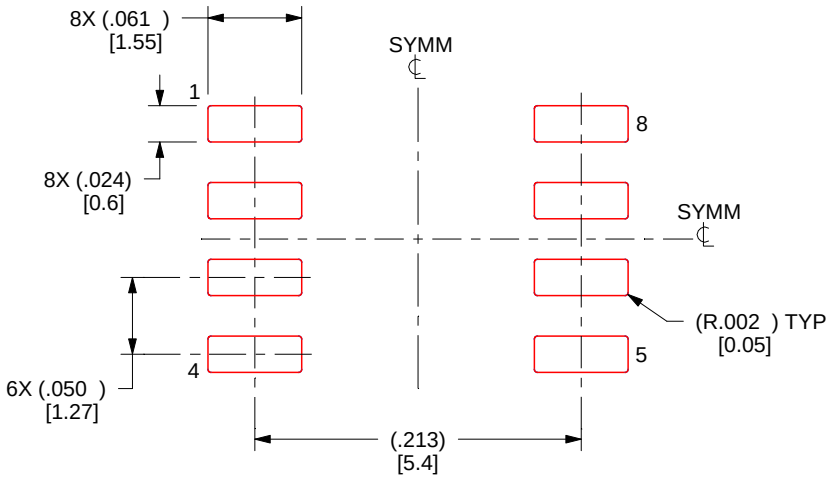
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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