LM49151 Boomer™ Audio Power Amplifier Series Mono Class D Audio Subsystem with Earpiece Driver, Ground Referenced Headphone Amplifiers, Speaker Protection and No Clip with Clip Control

Check for Samples: LM49151

FEATURES

- **E^2S Class D Amplifier**
- **Ground Referenced Outputs — Eliminates Output Coupling Capacitors**
- **I^2C Programmable No Clip Function with Clip Control**
- **Voltage Limiter Speaker Protection**
- **I^2C Volume and Mode Control**
- **Ear Piece Amplifier**
- **Advanced Click-and-Pop Suppression**
- **Low Supply Current**
- **Micro-Power Shutdown**
- **20-bump DSBGA Package**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Notebook PCs**
- **Portable Electronics Devices**
- **MP3 Players**

KEY SPECIFICATIONS

- **Output Power at V_{DD} = 3.3V THD+N ≤ 1%**
  - **LS Mode, R_L = 8Ω 520mW (Typ)**
  - **HP Mode, R_L = 32Ω 40mW (Typ)**
- **Output Power at V_{DD} = 5V THD+N ≤ 1%**
  - **LS Mode, R_L = 8Ω 1.25W (Typ)**
  - **HP Mode, R_L = 32Ω 42mW (Typ)**
- **Output Offset**
  - **LS Mode 15 6mV (Typ)**
  - **HP Mode 15 2mV (Typ)**

DESCRIPTION

The LM49151 is a fully integrated audio subsystem designed for portable handheld applications such as cellular phones. The LM49151 combines a 1.25W mono E^2S class D amplifier, 125mW Class AB earpiece driver, 42mW/channel stereo ground referenced headphone drivers, volume control, input mixer/multiplexer, and speaker protection into a single device.

The LM49151 class D speaker amplifier features Texas Instruments' unique Automatic Level Control (ALC) that provides both a I^2C programmable no-clip feature with Clip Controls and speaker protection. The E^2S (Enhanced Emission Suppression) class D amplifier features a patented, ultra low EMI PWM architecture that significantly reduces RF emissions while preserving audio quality and efficiency while delivering 1.25W into an 8Ω load with <1% THD+N with a 5V supply. The 42mW/channel headphone drivers feature Texas Instruments' ground referenced architecture that creates a ground-referenced output from a single supply, eliminating the need for bulky and expensive DC-blocking capacitors, saving space and minimizing system cost.

The LM49151 features separate volume controls for the loudspeaker and headphone inputs. Mode selection, shutdown control, and volume are controlled through an I^2C compatible interface. The LM49151's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown.

Typical Application

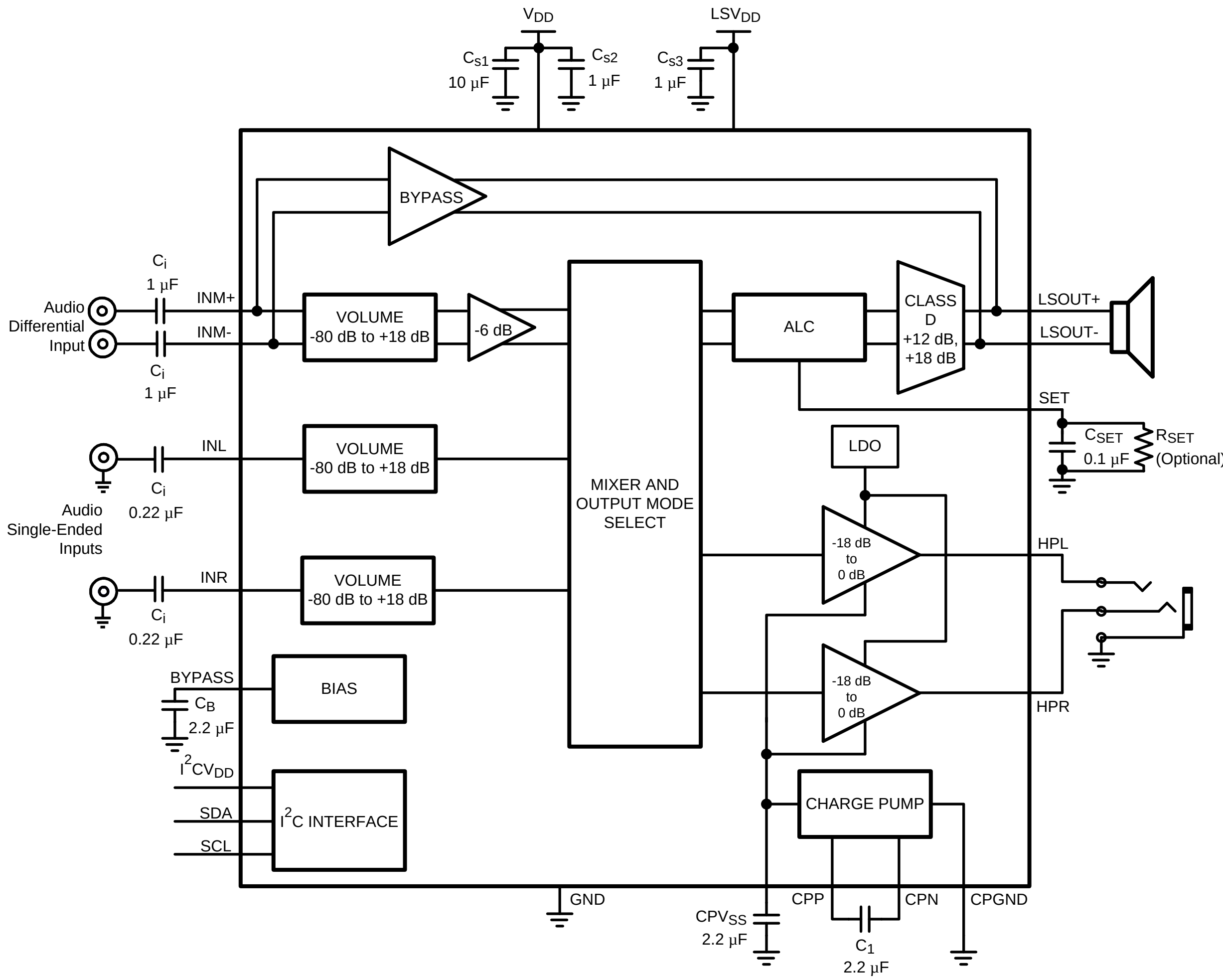

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

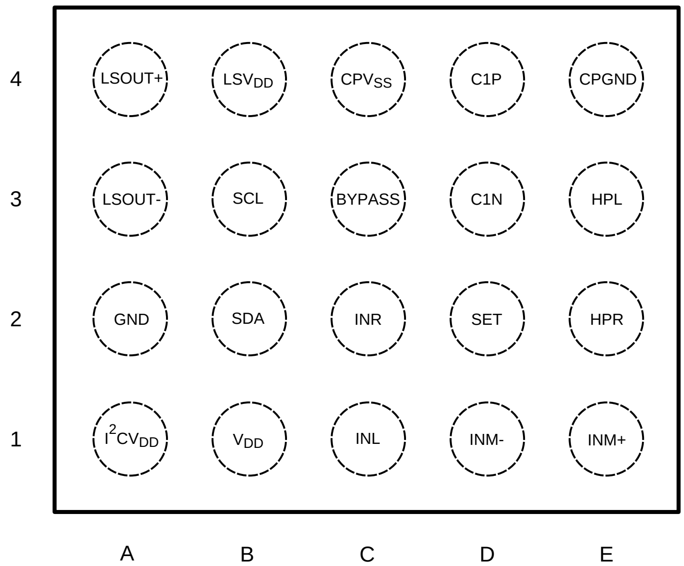

Figure 2. 20 Bump DSBGA Package
Top View
(See Package Number YZR0020)

BUMP DESCRIPTIONS

Bump	Name	Description
A1	I^2CV_{DD}	I^2C Power Supply
A2	GND	Ground
A3	LSOUT-	Inverting Loudspeaker Output
A4	LSOUT+	Non-Inverting Loudspeaker Output
B1	V_{DD}	Analog Power Supply
B2	SDA	I^2C Data Input
B3	SCL	I^2C Clock Input
B4	LSV_{DD}	Loudspeaker Power Supply
C1	INL	Left Channel Input
C2	INR	Right Channel Input
C3	BYPASS	Mid-Rail Supply Bypass
C4	CPV_{SS}	Charge Pump Output
D1	INM-	Mono Channel Inverting Input
D2	SET	ALC Timing Control
D3	CPN	Charge Pump Flying Capacitor - Negative Terminal
D4	CPP	Charge Pump Flying Capacitor - Positive Terminal
E1	INM+	Mono Channel Non-Inverting Input
E2	HPR	Right Channel Headphone Amplifier Output
E3	HPL	Left Channel Headphone Amplifier Output
E4	CPGND	Charge Pump Ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2][3]

Supply Voltage [1]		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3 to V_{DD} +0.3
Power Dissipation [4]		Internally Limited
ESD Rating [5]		2.0kV
ESD Rating [6]		200V
Junction Temperature		150°C
Soldering Information	See AN-1112 (SNVA009) "DSBGA Wafer Level Chip Scale Package"	
Thermal Resistance	θ_{JA} (typ) - YZR0020	46.1°C/W

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
(5) Human body model, applicable std. JESD22-A114C.
(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_{DD}, LSV_{DD})	2.7V ≤ V_{DD} ≤ 5.5V
Supply Voltage (I^2CV_{DD})	1.7V ≤ I^2CV_{DD} ≤ 5.5V
	I^2CV_{DD} ≤ V_{DD}

Electrical Characteristics 3.3V [1][2]

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB R_L = 8Ω+30µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151		Units (Limits)
			Typical (3)	Limits (4)	
I_{DD}	Supply Current	V_{IN} = 0, No Load			
		LS mode 1	3.7	5.5	mA (max)
		LS Mode 1, ALC enabled	4	6	mA (max)
		HP Mode 8	4.9	7	mA (max)
		EP Bypass Mode	0.8	1.3	mA (max)
		LS+HP Mode 5 and 10	7	10.5	mA (max)
		LS Mode 1, GAMP_SD = 1	3		mA
		HP Mode 8, GAMP_SD = 1	4.3		mA

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(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Datasheet min/max specification limits are specified by test or statistical analysis.

Electrical Characteristics 3.3V[(1)(2)] (continued)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB R_L = 8Ω+30µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151 Typical (3)	LM49151 Limits (4)	Units (Limits)
I_{SD}	Shutdown Current		0.04	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0			
		LS Mode 5, mono input	10		mV
		HP Mode 5, mono input	2	6	mV (max)
		EP Bypass Mode, 1mono input	0.8	5	mV (max)
		LS Mode 10, stereo input	10		mV
		HP Mode 10, stereo input	2	6	mV (max)
		LS Mode 15, stereo + mono input	10		mV
		HP Mode 15, stereo + mono input	2	6	mV (max)
t_{WU}	Wake Up Time	HP Mode, C_{BYPASS} = 2.2µF Normal, TURN_ON_TIME = 0 Fast, TURN_ON_TIME = 1	 27 15		 ms ms
A_{VOL}	Volume Control	Minimum Gain Setting	–80		dB (min) dB (max)
		Maximum Gain Setting	18		dB
	Volume Control Step Error		±0.2		dB
A_V	Gain	LS Mode			
		Gain 0	12		dB
		Gain 1	18		dB
		HP Mode			
		Gain 0	0		dB
		Gain 1	–1.5		dB
		Gain 2	–3		dB
		Gain 3	–6		dB
		Gain 4	–9		dB
		Gain 5	–12		dB
		Gain 6	–15		dB
		Gain 7	–18		dB
A_{VMUTE}	Mute Attention	LS Output, HP Mode P_{OUT} = 20mW	–96		dB
		HP Output, LS Mode P_{OUT} = 250mW	–96		dB
R_{IN}	Input Resistance	MONO, RIN, LIN, Inputs			
		Maximum Gain Setting	13	11 15.5	kΩ (min) kΩ (max)
		Minimum Gain Setting	110	90 130	kΩ (min) kΩ (max)
		EP Bypass Mode	62	50 80	kΩ (min) kΩ (max)
P_O	Output Power	f = 1kHz, THD+N = 1% Two channels in phase			
		LS Mode 1	520	450	mW (min)
		HP Mode 8, R_L = 16Ω	40		mW
		HP Mode 8, R_L = 32Ω	40	30	mW (min)
		EP Bypass Mode, R_L = 8Ω	35	26	mW (min)

Electrical Characteristics 3.3V[1][2] (continued)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB R_L = 8Ω+30µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151 Typical (3)	LM49151 Limits (4)	Units (Limits)
THD+N	Total Harmonic Distortion + Noise	f = 1kHz			
		LS Mode 1, P_O = 250mW	0.02		%
		HP Mode 8, P_O = 20mW	0.015		%
		EP Bypass Mode, R_L = 8Ω	0.15		%
PSRR	Power Supply Rejection Ratio	f = 217Hz, V_{RIPPLE} = 200mV_{PP}; C_B = 2.2µF All audio inputs terminated to AC GND, output referred			
		LS Mode 1, mono input	72		dB
		LS Mode 2, stereo input	67		dB
		LS mode 3, mono + stereo input	71		dB
		HP Mode 4, mono input	91		dB
		HP Mode 8, stereo input	83		dB
		HP Mode 12, mono + stereo input	81		dB
		EP Bypass Mode, mono input	95		dB
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz, mono input			
		LS Mode 1	55		dB
		HP Mode 4	61		dB
		EP Bypass Mode	55		dB
η	Efficiency	LS Mode, P_O = 500mW	88		%
X_{TALK}	Crosstalk	HP Mode 8, P_O = 12mW, R_L = 32Ω, f = 1kHz	78		dB
ε_{OS}	Output Noise	A-weighted, Inputs AC GND			
		LS Mode 1, mono input	40		µV
		LS Mode 2, stereo input	47		µV
		LS Mode 3, mono + stereo input	48		µV
		HP Mode 4, mono input	9		µV
		HP Mode 8, stereo input	10		µV
		HP Mode 12, mono + stereo input	11		µV
		EP Bypass Mode, mono input	10		µV
SNR	Signal to Noise Ratio	LS Mode 1, P_O = 500mW HP Mode 4, P_O = 40mW	90 102		dB dB
T_A	Attack Time	ATTACK_TIME = 00	0.75		ms
T_R	Release Time	RELEASE_TIME = 00	1		s
V_{LIMIT}	Output Voltage Limit	LS Mode 1, THD+N ≤ 1%, VOLTAGE_LEVEL 001 010 011	 4 4.8 5.6		 V_{P-P} V_{P-P} V_{P-P}

Electrical Characteristics 5.0V(1)(2)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB R_L = 8Ω+30µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151		Units (Limits)
			Typical (3)	Limits (4)	
I_{DD}	Supply Current	V_{IN} = 0, No Load			
		LS mode 1, ALC disabled	4.6		mA
		LS Mode 1, ALC enabled	5.0		mA
		HP Mode 8	5.0		mA
		EP Bypass Mode	0.9		mA
		LS+HP Mode 5 and 10	7.7		mA
		LS Mode 1, GAMP_SD = 1	3.7		mA
		HP Mode 8, GAMP_SD = 1	4.4		mA
I_{SD}	Shutdown Current		0.04	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0			
		LS Mode 5, mono input	10		mV
		HP Mode 5, mono input	2	6	mV (max)
		EP Bypass Mode, mono input	1.2	5	mV (max)
		LS Mode 10, stereo input	10		mV
		HP Mode 10, stereo input	2	6	mV (max)
		LS Mode 15, stereo + mono input	10		mV
		HP Mode 15, stereo + mono input	2	6	mV (max)
t_{WU}	Wake Up Time	HP Mode, C_{BYPASS} = 2.2µF Normal, TURN_ON_TIME = 0 Fast, TURN_ON_TIME = 1	 27 15		 ms ms
A_{VOL}	Volume Control	Minimum Gain Setting	–80		dB (min) dB (max)
		Maximum Gain Setting	18		dB
	Volume Control Step Error		±0.2		dB
A_V	Gain	LS Mode			
		Gain 0	12		dB
		Gain 1	18		dB
		HP Mode			
		Gain 0	0		dB
		Gain 1	–1.5		dB
		Gain 2	–3		dB
		Gain 3	–6		dB
		Gain 4	–9		dB
		Gain 5	–12		dB
		Gain 6	–15		dB
		Gain 7	–18		dB

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(4) Datasheet min/max specification limits are specified by test or statistical analysis.

Electrical Characteristics 5.0V(1)(2) (continued)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB R_L = 8Ω+30µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151		Units (Limits)
			Typical (3)	Limits (4)	
A_{VMUTE}	Mute Attention	LS Output, HP Mode P_{OUT} = 20mW	–96		dB
		HP Output, LS Mode P_{OUT} = 250mW	–96		dB
R_{IN}	Input Resistance	MONO, RIN, LIN, Inputs			
		Maximum Gain Setting	13		kΩ
		Minimum Gain Setting	110		kΩ
		EP Bypass Mode	62		kΩ
P_O	Output Power	f = 1kHz, THD+N = 1% Two channels in phase			
		LS Mode 1	1.25		W
		HP Mode 8, R_L = 16Ω	42		mW
		HP Mode 8, R_L = 32Ω	43		mW
		EP Bypass Mode, R_L = 8Ω	137		mW
THD+N	Total Harmonic Distortion + Noise	f = 1kHz			
		LS Mode 1, P_O = 600mW	0.015		%
		HP Mode 8, P_O = 20mW	0.01		%
		EP Bypass Mode, P_O = 60mW	0.09		%
PSRR	Power Supply Rejection Ratio	f = 217Hz, V_{RIPPLE} = 200mV_{PP}; C_B = 2.2µF All audio inputs terminated to AC GND, output referred			
		LS Mode 1, mono input, A_V = 6dB	75		dB
		LS Mode 2, stereo input, A_V = 6dB	71		dB
		LS mode 3, mono + stereo input, A_V = 6dB	71		dB
		HP Mode 4, mono input	91		dB
		HP Mode 8, stereo input	80		dB
		HP Mode 12, mono + stereo input	79		dB
		EP Bypass Mode, mono input	97		dB
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz, mono input			
		LS Mode 1	55		dB
		HP Mode 4	61		dB
		EP Bypass Mode	55		dB
η	Efficiency	LS Mode, P_O = 1W	88		%
X_{TALK}	Crosstalk	HP Mode 8, P_O = 12mW, R_L = 32Ω, f = 1kHz	78		dB
ε_{OS}	Output Noise	A-weighted, Inputs AC GND			
		LS Mode 1, mono input	41		µV
		LS Mode 2, stereo input	41		µV
		LS Mode 3, mono + stereo input	43		µV
		HP Mode 4, mono input	9		µV
		HP Mode 8, stereo input	10		µV
		HP Mode 12, mono + stereo input	12		µV
		EP Bypass Mode, mono input	11		µV
SNR	Signal to Noise Ratio	LS Mode 1, P_O = 1.25W HP Mode 4, P_O = 40mW	96 102		dB dB

Electrical Characteristics 5.0V(1)(2) (continued)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB R_L = 8Ω+30µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151		Units (Limits)
			Typical (3)	Limits (4)	
V_{LIMIT}	Output Voltage Limit	LS Mode 1, THD+N ≤ 1%, VOLTAGE_LEVEL 001 010 011 101 110	4 4.8 5.6 6.4 7.2 8		V_{P-P} V_{P-P} V_{P-P} V_{P-P} V_{P-P} V_{P-P}

I²C Interface Characteristics V_{DD} = 5V, 2.2V ≤ I^2CV_{DD} ≤ 5.5V(1)(2)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN = 12dB, HPGAIN = 0dB R_L = 8Ω+30µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), CSET = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151		Units (Limits)
			Typical	Limits (3)	
t_1	SCL Period			2.5	µs (min)
t_2	SDA Setup Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
t_6	SDA Data Hold Time			100	ns (min)
V_{IH}	Input High Voltage			$0.7xI^2CV_{DD}$	V (min)
V_{IL}	Input Low Voltage			$0.3xI^2CV_{DD}$	V (max)

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I^2C Interface Characteristics V_{DD} = 3.3V, 1.7V ≤ I^2CV_{DD} ≤ 2.2V (1)(2)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB R_L = 8Ω (Loudspeaker), R_L = 32Ω (Headphone), R_L = 8Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LM49151		Units (Limits)
			Typical	Limits (3)	
t_1	SCL Period Time			2.5	µs (min)
t_2	SCL Setup Time			250	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	I^2C Data Hold Time			250	ns (min)
V_{IH}	Input Voltage High			$0.7xI^2CV_{DD}$	V (min)
V_{IL}	Input Voltage Low			$0.3xI^2CV_{DD}$	V (max)

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Typical Performance Characteristics(1)

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω+30µH, P_{OUT} = 250mW
Speaker Mode 1

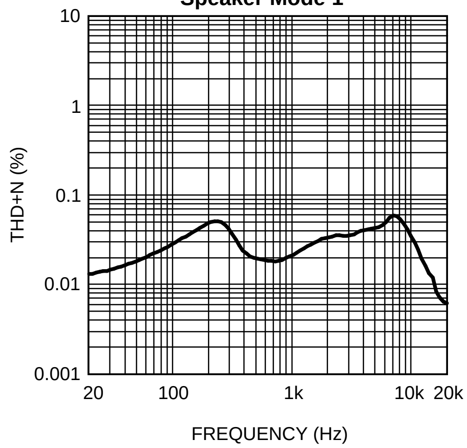

Figure 3.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_{OUT} = 20mW
Headphone Mode 8

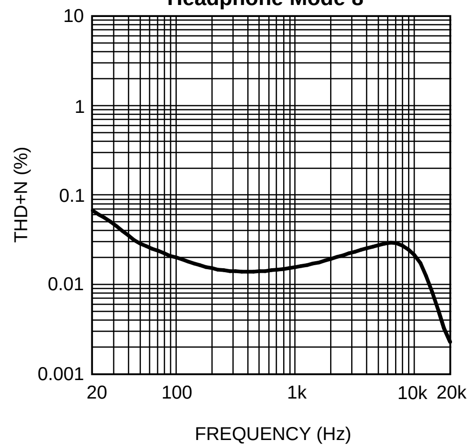

Figure 4.

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 8Ω+30µH, P_{OUT} = 300mW
Speaker Mode 1

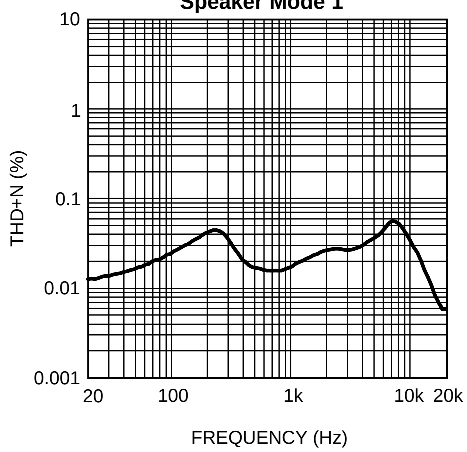

Figure 5.

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω, P_{OUT} = 20mW
Headphone Mode 8

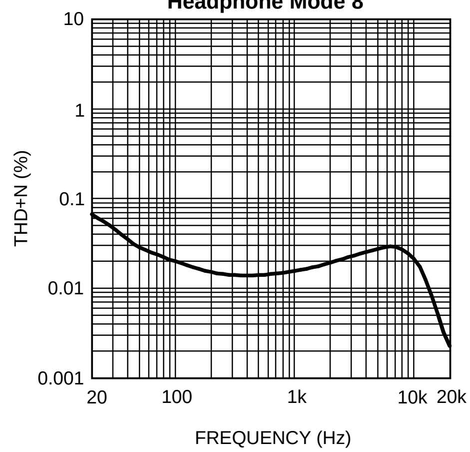

Figure 6.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω+30µH, P_{OUT} = 600mW
Speaker Mode 1

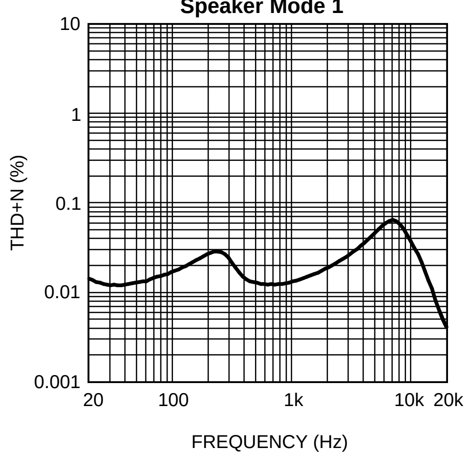

Figure 7.

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_{OUT} = 20mW
Headphone Mode 8

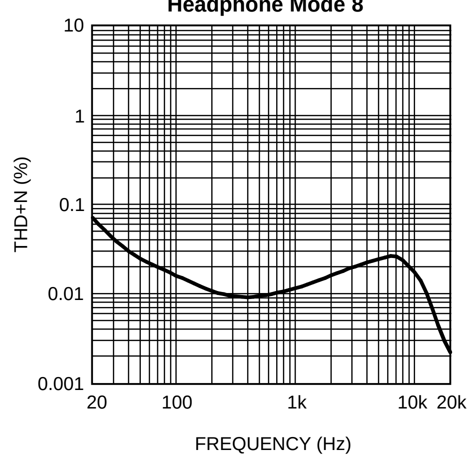

Figure 8.

(1) Data taken with BW = 22kHz except where specified.

Typical Performance Characteristics[(1)] (continued)

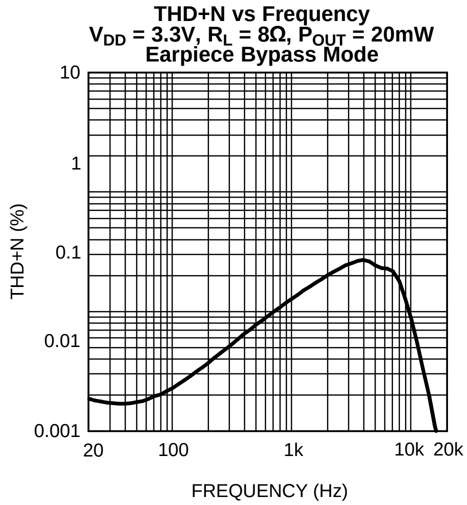

Figure 9.

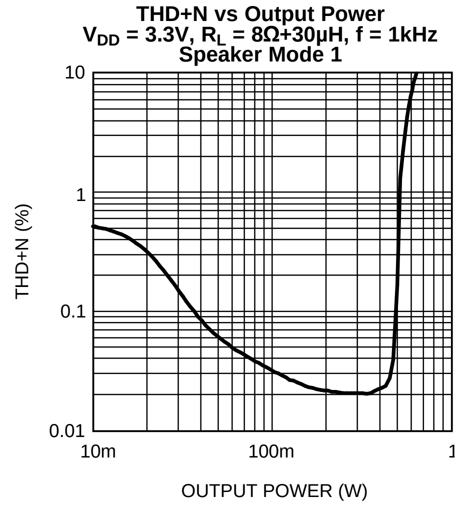

Figure 10.

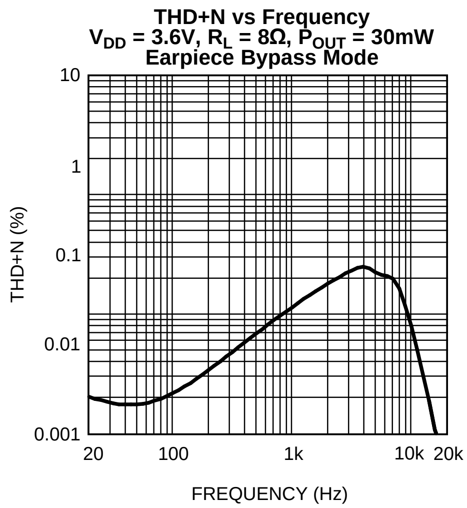

Figure 11.

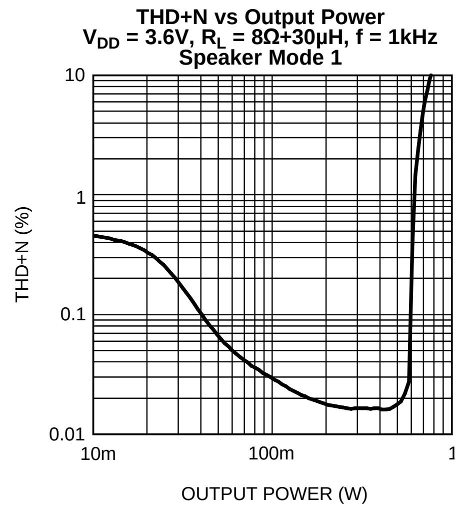

Figure 12.

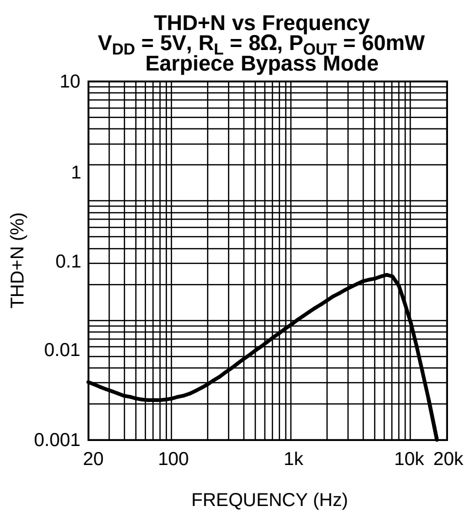

Figure 13.

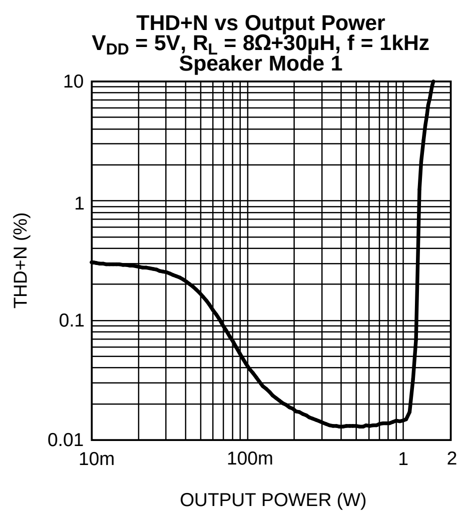

Figure 14.

Typical Performance Characteristics[1] (continued)

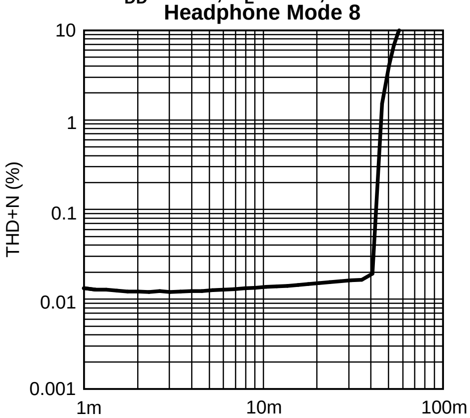

Figure 15.

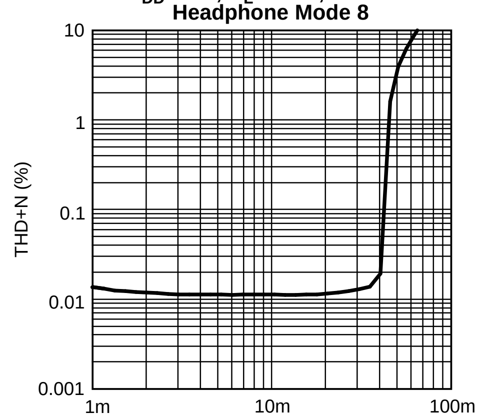

Figure 16.

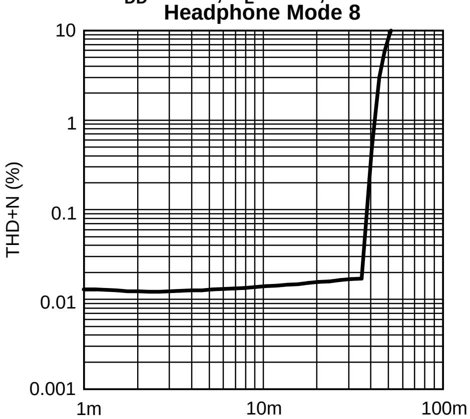

Figure 17.

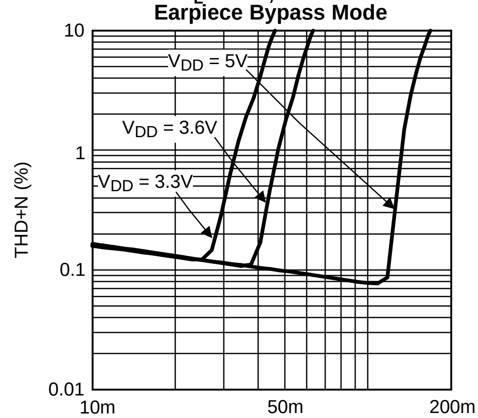

Figure 18.

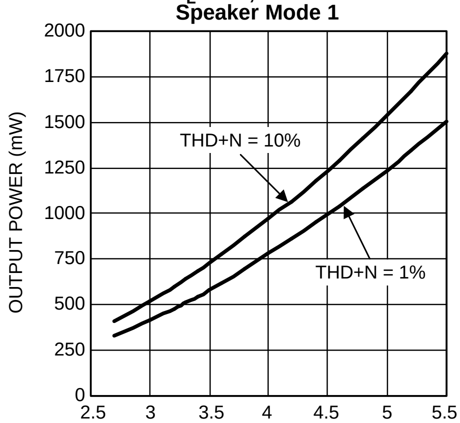

Figure 19.

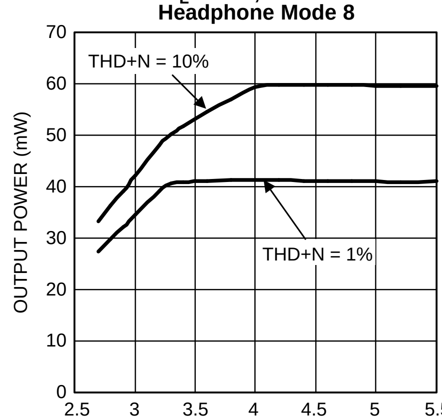

Figure 20.

Typical Performance Characteristics(1) (continued)

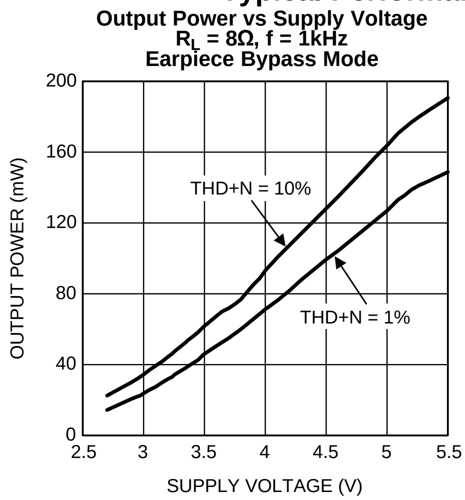

Figure 21.

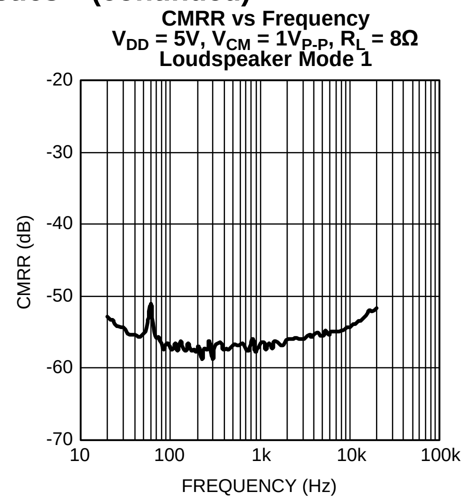

Figure 22.

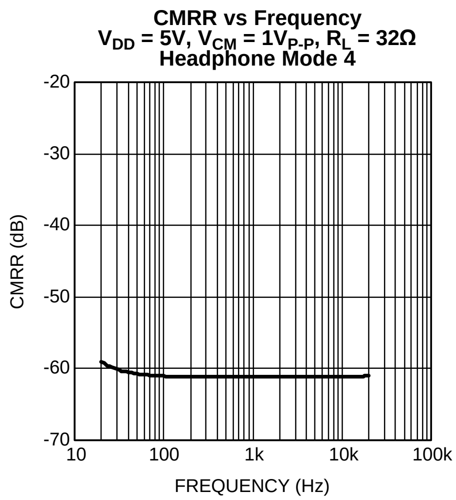

Figure 23.

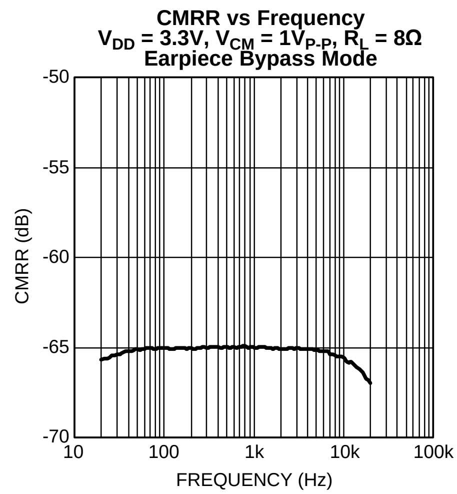

Figure 24.

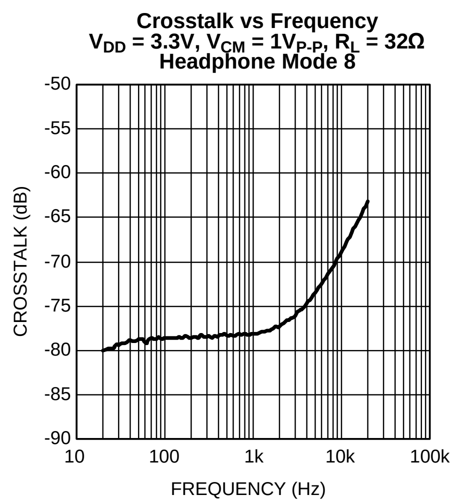

Figure 25.

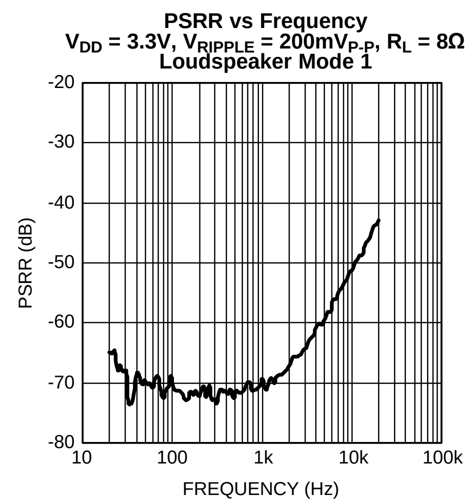

Figure 26.

Typical Performance Characteristics[1] (continued)

PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
Loudspeaker Mode 2

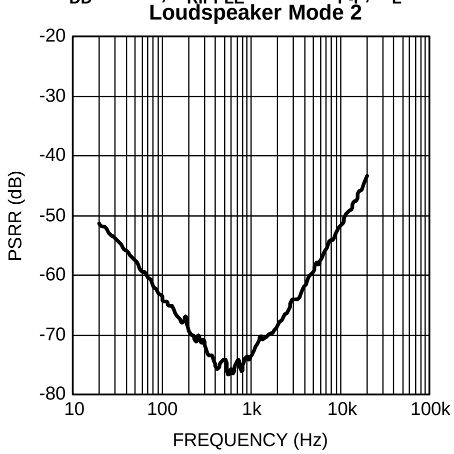

Figure 27.

PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω
Headphone Mode 4

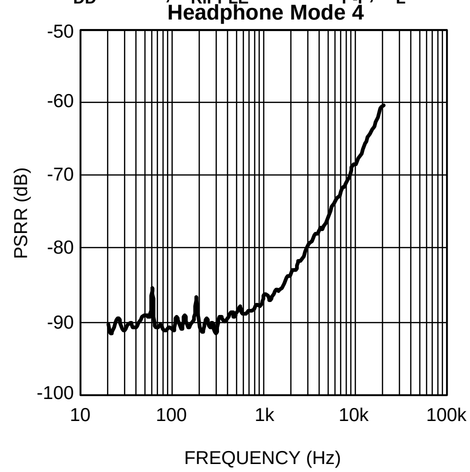

Figure 28.

PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω
Headphone Mode 8

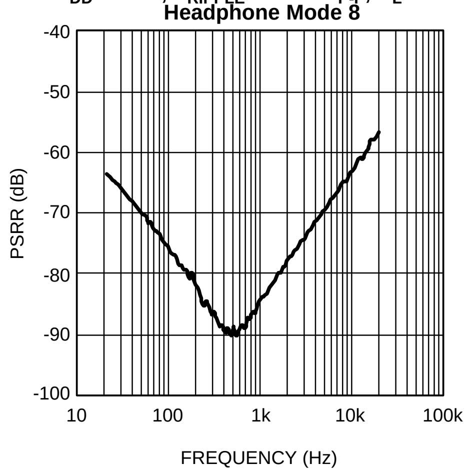

Figure 29.

PSRR vs Frequency
V_{DD} = 3.3V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
Earpiece Bypass Mode

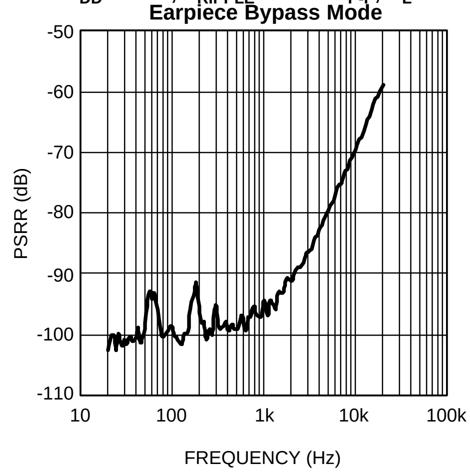

Figure 30.

Efficiency vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Speaker Mode 1

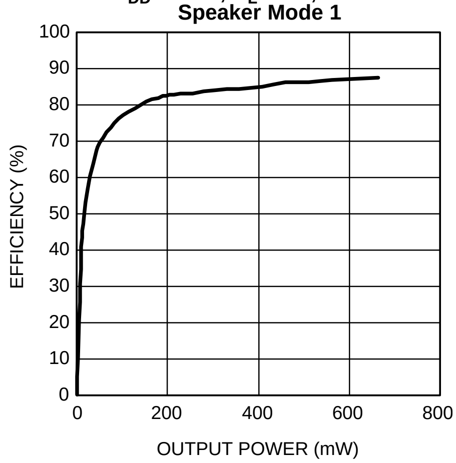

Figure 31.

Efficiency vs Output Power
V_{DD} = 3.6V, R_L = 8Ω, f = 1kHz
Speaker Mode 1

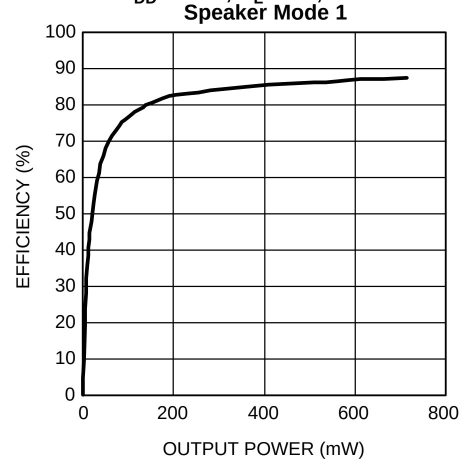

Figure 32.

Typical Performance Characteristics[(1)] (continued)

Efficiency vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Speaker Mode 1

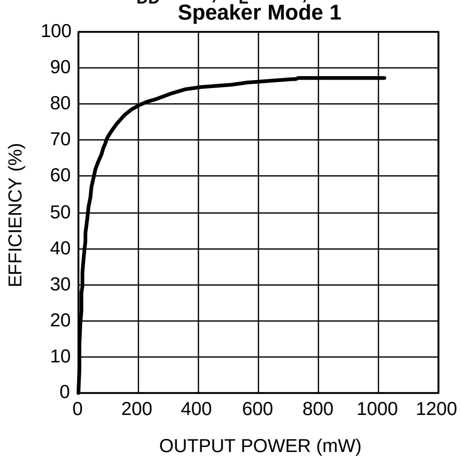

Figure 33.

Power Dissipation vs Output Power
R_L = 8Ω, f = 1kHz
Speaker Mode 1

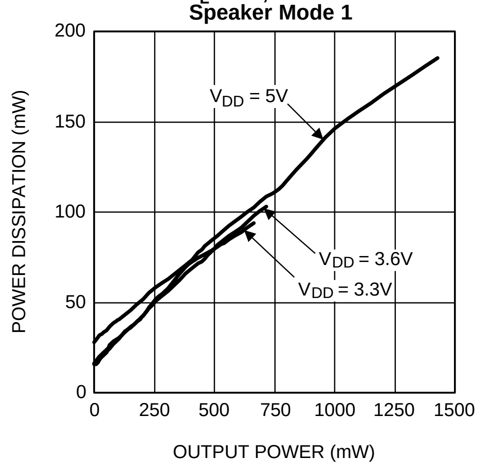

Figure 34.

Power Dissipation vs Output Power
R_L = 32Ω, f = 1kHz
Headphone Mode 8

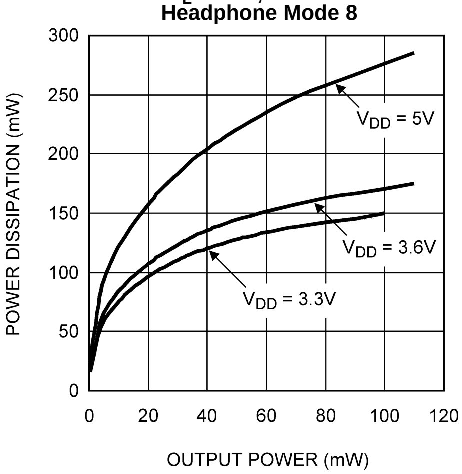

Figure 35.

Power Dissipation vs Output Power
R_L = 32Ω, f = 1kHz
Earpiece Bypass Mode

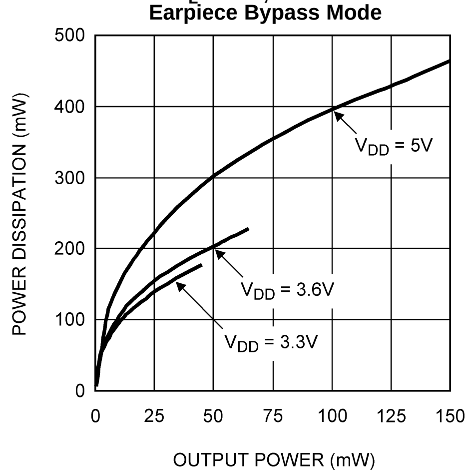

Figure 36.

Supply Current vs Supply Voltage
Headphone Mode 8, No Load

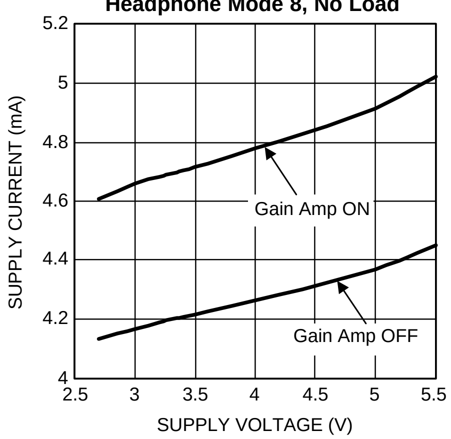

Figure 37.

Supply Current vs Supply Voltage
Earpiece Bypass Mode, No Load

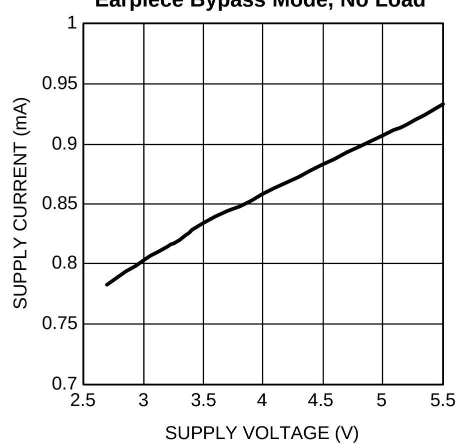

Figure 38.

Typical Performance Characteristics(1) (continued)

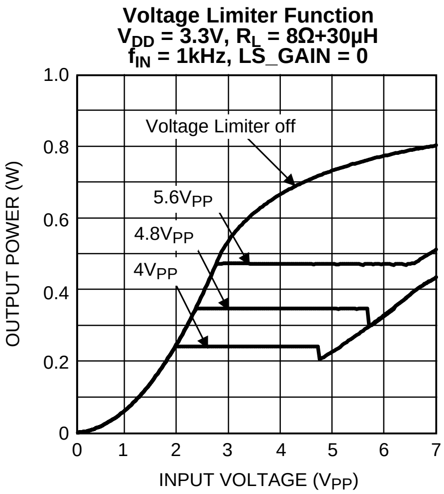

Figure 39.

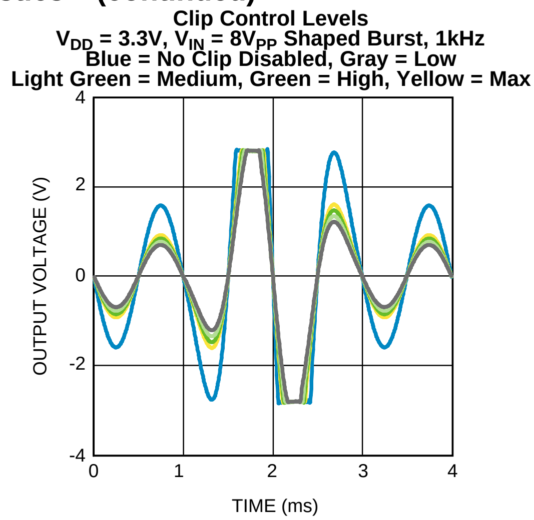

Figure 40.

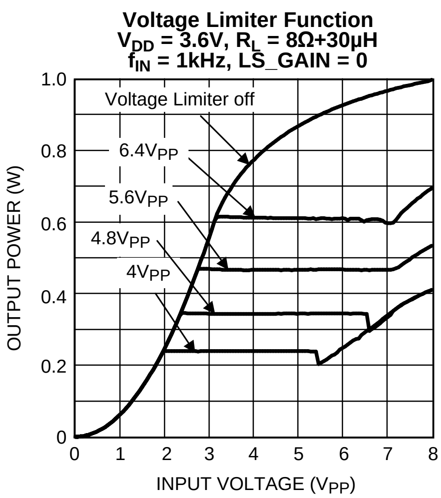

Figure 41.

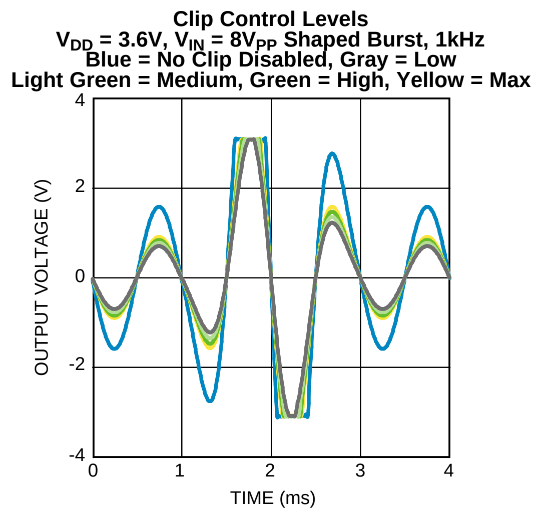

Figure 42.

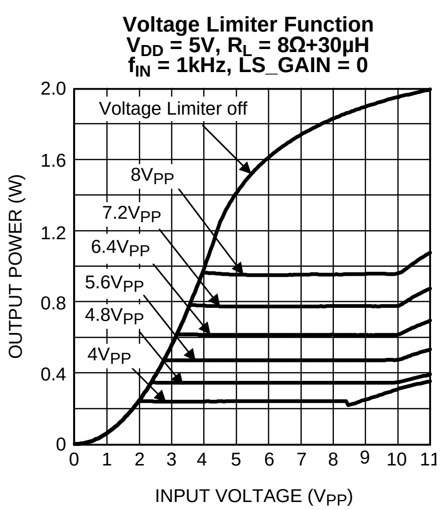

Figure 43.

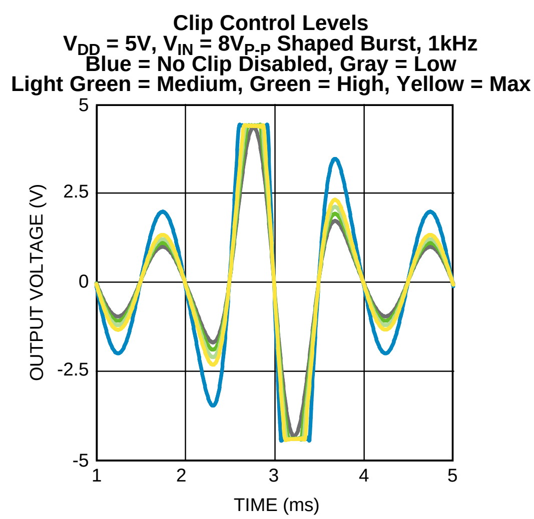

Figure 44.

Typical Performance Characteristics[1] (continued)

No Clip Function
V_{DD} = 3.3V, R_{LIN} = 8Ω+30µH, f_{IN} = 1kHz, LS_GAIN = 0
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

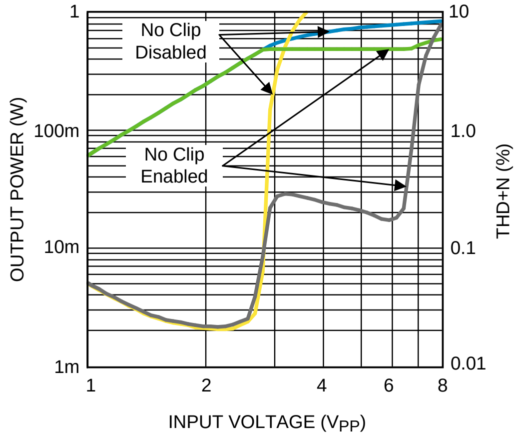

Figure 45.

No Clip Function
V_{DD} = 3.3V, R_{LIN} = 8Ω+30µH, f_{IN} = 1kHz, LS_GAIN = 1
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

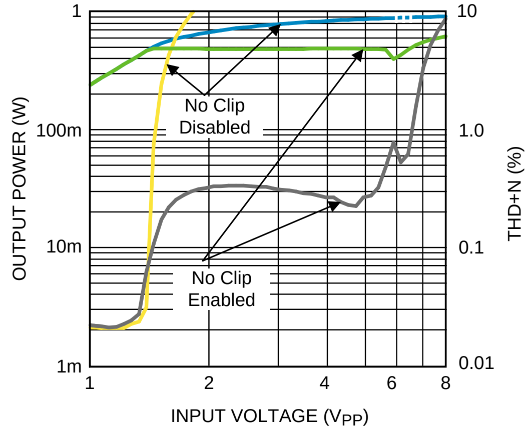

Figure 46.

No Clip Function
V_{DD} = 3.6V, R_{LIN} = 8Ω+30µH, f_{IN} = 1kHz, LS_GAIN = 0
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

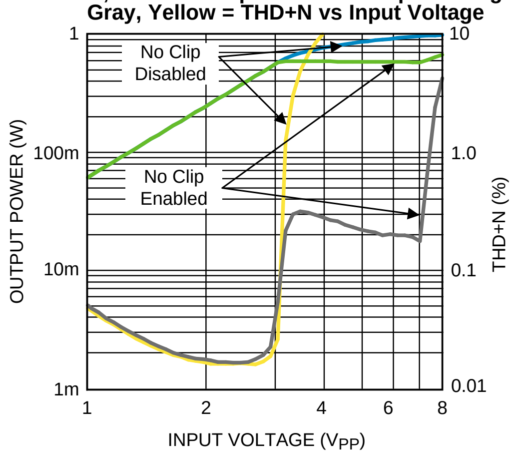

Figure 47.

No Clip Function
V_{DD} = 3.6V, R_{LIN} = 8Ω+30µH, f_{IN} = 1kHz, LS_GAIN = 1
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

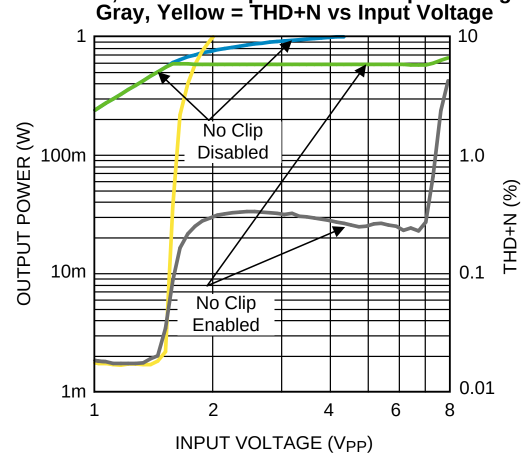

Figure 48.

No Clip Function
V_{DD} = 5V, R_{LIN} = 8Ω+30µH, f_{IN} = 1kHz, LS_GAIN = 0
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

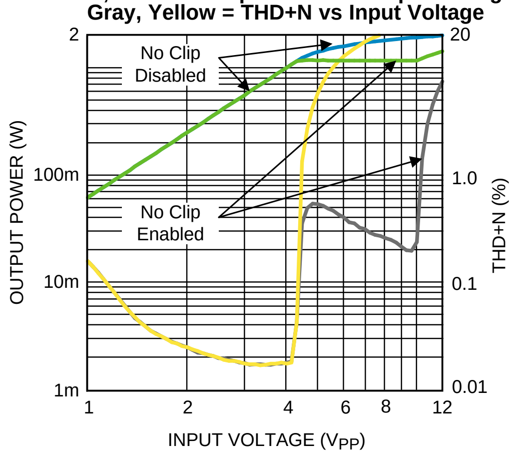

Figure 49.

No Clip Function
V_{DD} = 5V, R_{LIN} = 8Ω+30µH, f_{IN} = 1kHz, LS_GAIN = 1
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

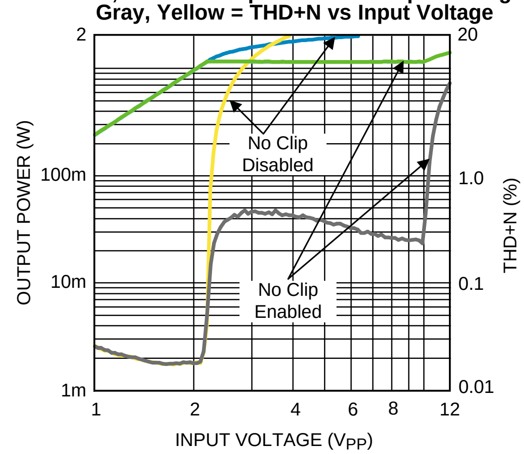

Figure 50.

APPLICATION INFORMATION

WRITE-ONLY I^2C COMPATIBLE INTERFACE

The LM49151 is controlled through an I^2C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The SCL and SDA lines are uni-directional write only interface. The LM49151 and the master can communicate at clock rates up to 400kHz. Figure 51 shows the I^2C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49151 is a slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 52). Each data word and device address transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 53). The LM49151 device address is 11111000.

I^2C BUS FORMAT

The bus format for the I^2C interface is shown in Figure 53. The bus format diagram is broken up into six major sections: The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own address. The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH. After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM49151 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM49151. The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH. After the data byte is sent, the master must check for another acknowledge to see if the LM49151 received the data. If the master has more data bytes to send to the LM49151, then the master can repeat the previous two steps until all data bytes have been sent. The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

I^2C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

The LM49151's I^2C interface is powered up through the I^2CV_{DD} pin. The LM49151 I^2C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I^2C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

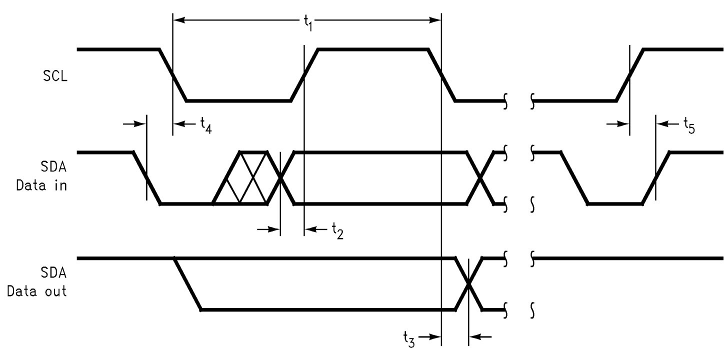

Figure 51. I^2C Timing Diagram

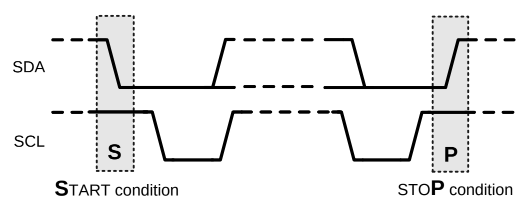

Figure 52. Start and Stop Diagram

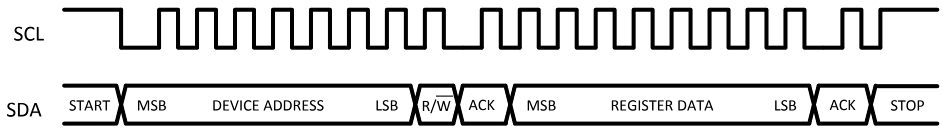

Figure 53. Example I²C Write Cycle

DEVICE ADDRESS REGISTER

Table 1. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 ($\overline{W}$)
Device Address	1	1	1	1	1	0	0	0

I²C CONTROL REGISTER

Table 2. I²C Control

	B7	B6	B5	B4	B3	B2	B1	B0
Shutdown Control	0	0	0	GAMP_SD	HPR_SD	I^2CV_{DD}_SD	TURN_ON _TIME	PWR_ON
Mode Control	0	0	1	EP_BYPASS	MODE_CONTROL			
Voltage Limit Control	0	1	0	ATTACK_TIME		VOLTAGE_LEVEL		
No Clip Control	0	1	1	RELEASE TIME		OUTPUT_CLIP_CONTROL		
Gain Control	1	0	0	INPUT_MUTE	LS_GAIN	HP_GAIN		
Mono Volume Control	1	0	1	MONO_VOL				
Stereo Volume Control	1	1	0	STEREO_VOL				
SS Control	1	1	1	0	0	0	0	SS_EN

SHUTDOWN CONTROL REGISTER

This register is used to control shutdown operation of the device.

Table 3. Shutdown Control

Bit	Name	Value	Description
B0	PWR_ON	This enables or disables the device.	
		PWR_ON	Status
		0	Device disabled
		1	Device enabled
B1	TURN_ON_TIME	This control the turn on time of the device.	
		TURN_ON_TIME	Status
		0	Normal turn on time (27ms)
		1	Fast turn on time (15ms)
B2	I^2CV_{DD}_SD	I^2CV_{DD}_SD	Status
		0	I^2CV_{DD} acts as an active low RESET input. If I^2CV_{DD} drops below 1.1V, the device resets and the I²C registers are restored to their default state.
		1	Normal Operation. I^2CV_{DD} voltage does not reset the device.
B3	HPR_SD	This disables the right headphone output.	
		HPR_SD	Status
		0	Normal Operation
		1	Headphone right disabled

Table 3. Shutdown Control (continued)

Bit	Name	Value	Description
B4	GAMP_SD	This disables the gain amplifiers that are not in use to minimize I_{DD}. This setting is recommended for output modes 1, 2, 4, 5, 8, 10.	
		GAMP_SD	Status
		0	Normal operation
		1	Disable the unused gain amplifiers

MODE CONTROL REGISTER

This register is used to control shutdown operation of the device.

Table 4. Output Mode Selection (see legend below(1))

Bits	Field	Description				
B3:B0	MODE _CONTROL	This set the different mixers output modes.				
		Mode_ Control	Mode	Loudspeaker	Headphone Right	Headphone Left
		0000	0	SD	SD	SD
		0001	1	G_M x M	SD	SD
		0010	2	2 x (G_L x L + G_R x R)	SD	SD
		0011	3	2 x (G_L x L + G_R x R) + G_M x M	SD	SD
		0100	4	SD	G_M x M/2	G_M x M/2
		0101	5	GM x M	G_M x M/2	G_M x M/2
		0110	6	2 x (GL x L + GR x R)	G_M x M/2	G_M x M/2
		0111	7	2 x (GL x L + GR x R) + GM x M	G_M x M/2	G_M x M/2
		1000	8	SD	G_R x R	G_L x L
		1001	9	GM x M	G_R x R	G_L x L
		1010	10	2 x (G_L x L + G_R x R)	G_R x R	G_L x L
		1011	11	2 x (G_L x L + G_R x R) + G_M x M	G_R x R	G_L x L
		1100	12	SD	G_R x R + G_M x M/2	G_L x L + G_M x M/2
		1101	13	G_M x M	G_R x R + G_M x M/2	G_L x L + G_M x M/2
		1110	14	2 x (G_L x L + G_R x R)	G_R x R + G_M x M/2	G_L x L + G_M x M/2
		1111	15	2 x (G_L x L + G_R x R) + G_M x M	G_R x R + G_M x M/2	G_L x L + G_M x M/2
B4	EP_BYPASS	This makes the loudspeaker and headphone amplifiers into shutdown mode and enables receiver bypass path.				
		0	Normal output mode operation			
		1	Enable the receiver bypass path			

(1) M: Mono differential input
R: Right channel stereo input
L: Left channel stereo input
SD: Shutdown
G_M : Differential input gain path
G_R: Right channel input gain path
G_L: Left channel input gain path

VOLTAGE LIMIT CONTROL REGISTER

This register is used to control output voltage limiter settings and attack time of the automatic level circuit:

Table 5. Voltage Limit Control

Bits	Field	Description	
B2:B0	VOLTAGE_LEVEL	This sets the output voltage limit level.	
		000	Voltage limit disabled
		001	$V_{TH(VLIM)} = 4V_{P-P}$
		010	$V_{TH(VLIM)} = 4.8V_{P-P}$
		011	$V_{TH(VLIM)} = 5.6V_{P-P}$
		100	$V_{TH(VLIM)} = 6.4V_{P-P}$
		101	$V_{TH(VLIM)} = 7.2V_{P-P}$
		110	$V_{TH(VLIM)} = 8V_{P-P}$
		111	Voltage limit disabled
B4:B3	ATTACK _TIME	This sets the Attack time of automatic level control circuit. It is based on characterization data and C_{SET} = 0.1µF (see ATTACK TIME section)	
		00	0.75ms
		01	1ms
		10	1.5ms
		11	2ms

NO CLIP CONTROL REGISTER

This register is used to control output clip control settings and release time of the automatic level circuit:

Table 6. No Clip Control

Bits	Field	Description	
B2:B0	OUTPUT_CLIP_CONTROL	This sets the output clip limit level.	
		000	No Clip disabled, output clip control disabled
		001	No Clip enabled, output clip control disabled
		010	Low
		011	Medium
		100	High
		101	Max
		110	No Clip enabled, output clip control disabled
		111	No Clip enabled, output clip control disabled
B4:B3	RELEASE_TIME	This sets the release time of automatic level control circuit. It is based on characterization data and C_{SET} = 0.1µF (see RELEASE TIME section)	
		00	1s
		01	0.8s
		10	0.65s
		11	0.4s

GAIN CONTROL REGISTER

This register is used to control gain level for on the outputs:

Table 7. Gain Control

Bits	Field	Description	
B2:B0	HP_GAIN	This sets the headphone output gain level.	
		000	0dB
		001	–1.5dB
		010	–3dB
		011	–6dB
		100	–9dB
		101	–12dB
		110	–15dB
		111	–18dB
B3	LS_GAIN	This sets the loudspeaker output gain level.	
		0	12dB
		1	18dB
B4	INPUT_MUTE	This sets the inputs into lower power mute mode.	
		0	Normal operation
		1	Device inputs are in mute mode

VOLUME CONTROL REGISTER

These registers are used to control output volume control levels for Loudspeaker and Headphone:

Table 8. LS GAIN / HP GAIN

Bits	Field	Description	
B4:B0	MONO_VOL STEREO_VOL	This programs the Earpiece, Loudspeaker, and Headphone volume level.	
		VOL	Level (dB)
		00000	MUTE
		00001	–46.5
		00010	–40.5
		00011	–34.5
		00100	–30
		00101	–27
		00110	–24
		00111	–21
		01000	–18
		01001	–15
		01010	–13.5
		01011	–12
		01100	–10.5
		01101	–9
		01110	–7.5
		01111	–6
		10000	–4.5
		10001	–3
		10010	–1.5
		10011	0
		10100	1.5
		10101	3
		10110	4.5
		10111	6
		11000	7.5
		11001	9
		11010	10.5
		11011	12
		11100	13.5
		11101	15
		11110	16.5
		11111	18

SPREAD SPECTRUM CONTROL REGISTER

This register controls the spread spectrum mode of the class D amplifier:

Table 9. SS Control

Bits	Field	Description	
B0	SS_ENB	This sets the spread spectrum mode of the Class D amplifier.	
		0	Spread Spectrum Disabled
		1	Spread Spectrum Enabled

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49151 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49151 can be used without input coupling capacitors when configured with a differential input signal.

INPUT MIXER/MULTIPLEXER

The LM49151 includes a comprehensive mixer multiplexer controlled through the I^2C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49151. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. Table 5 (MODE CONTROL) shows how the input signals are mixed together for each possible input selection.

SHUTDOWN FUNCTION

The LM49151 features the following shutdown controls: Bit B4 (GAMP_SD) of the SHUTDOWN CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the I_{DD} to be minimized. Bit B0 (PWR_ON) of the SHUTDOWN CONTROL register is the global shutdown control for the entire device. Set PWR_ON = 0 for normal operation. PWR_ON = 1 overrides any other shutdown control bit.

CLASS D AMPLIFIER

The LM49151 features a mono class D audio power amplifier with a filterless modulation scheme that reduces external component count, conserving board space and reducing system cost. With no signal applied, the outputs (LSOUT+ and LSOUT-) switch between VDD and GND with 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With an input signal applied, the duty cycle (pulse width) of the class D output changes. For increasing output voltage, the duty cycle of LSOUT+ increases, while the duty cycle of LSOUT- decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage.

ENHANCED EMISSIONS SUPPRESSION (E^2S)

The LM49151 class D amplifier features Texas Instruments' patent-pending E^2S system that reduces EMI, while maintaining high quality audio reproduction and efficiency. The E^2S system features selectable spread spectrum and advanced edge rate control (ERC). The LM49151 class D ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduces RF emissions, while maximizing THD+N and efficiency performance.

FIXED FREQUENCY

The LM49151 class D amplifier features two modulation schemes, a fixed frequency mode and a spread spectrum mode. Select the fixed frequency mode by setting bit B0 (SS_EN) of the SS CONTROL register to 0. In fixed frequency mode, the loudspeaker outputs switch at a constant 300kHz. The output spectrum consists of the 300kHz fundamental and its associated harmonics.

SPREAD SPECTRUM

The selectable spread spectrum mode minimizes the need for output filters, ferrite beads or chokes. In spread spectrum mode, the switching frequency varies randomly by 30% about a 300kHz center frequency, reducing the wideband spectral content, improving EMI emission radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR. Set bit B0 (SS_EN) of the SS CONTROL register to 1 to enable spread spectrum mode.

GROUND REFERENCED HEADPHONE AMPLIFIER

The LM49151 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor from a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49151 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49151 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

EARPIECE (EP) BYPASS

When B4 of MODE_CONTROL register is set to 1, earpiece amplifier is enabled and differential inputs are passed down to speaker outputs. This in turn disables the class D amplifier.

AUTOMATIC LIMITER CONTROL (ALC)

When enabled, the ALC continuously monitors and adjusts the gain of the loudspeaker amplifier signal path if necessary. The ALC serves two functions: voltage limiter/speaker protection and output clip prevention (No-Clip) with four clip controls levels. The voltage limiter/speaker protection prevents an output overload condition by maintaining the loudspeaker output signal below a preset amplitude (See VOLTAGE LIMITER section). The No Clip feature monitors the output signal and maintains audio quality by preventing the loudspeaker output from exceeding the amplifier's headroom (see NO CLIP/OUTPUT CLIP CONTROL section). The voltage limiter thresholds, clip control levels, attack and release times are configured through the I^2C interface.

VOLTAGE LIMITER

The voltage limiter function of the ALC monitors and prevents the audio signal from exceeding the voltage limit threshold (Figure 54). The voltage limit threshold ($V_{TH(VLIM)}$) is set by bits B2:B0 in the Voltage Limit Threshold Register (see Table 6). Although the ALC reduces the gain of the speaker path to maintain the audio signal below the voltage limit threshold, it is still possible to overdrive the speaker output in which case loudspeaker output will exceed the voltage limit threshold and cause clipping on the output, and speaker damage is possible. Please see the ALC HEADROOM section for further details.

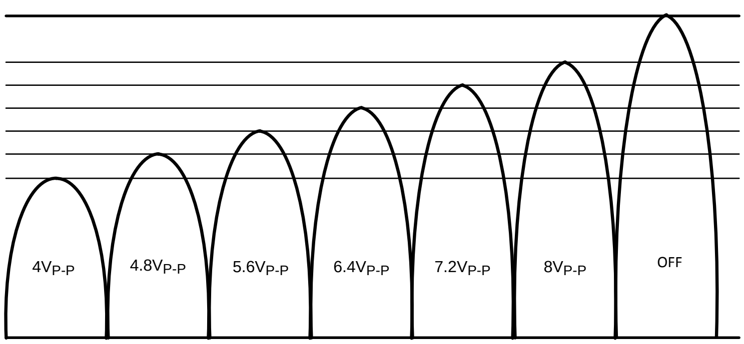

Figure 54. Voltage Limit Output Level

NO CLIP/OUTPUT CLIP CONTROL

The LM49151 No Clip circuitry detects when the loudspeaker output is near clipping and reduces the signal gain to prevent output clipping and preserve audio quality (Figure 55). Although the ALC reduces the gain of the speaker path to prevent output clipping, it is still possible to overdrive the speaker output. Please see the ALC HEADROOM section for further details.

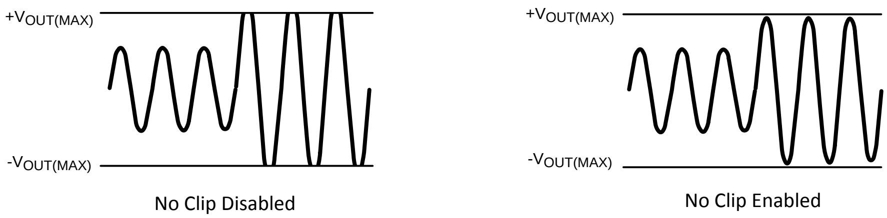

Figure 55. No Clip Function

The LM49151 also features an output clip control that allows a certain amount of clipping at the output in order to increase the loudspeaker output power. The clip level is set by B2:B0 in the No Clip Control Register (see Table 7). The clip control works by allowing the output to enter clipping before the ALC turns on and maintains the output level. The clip control has four levels: low, medium, high and max. The low and max clip level control settings give the lowest distortion and highest distortion respectively on the output (see Figure 56). The actual output level of the device will depend upon the supply voltage, and the output power will depend upon the load impedance.

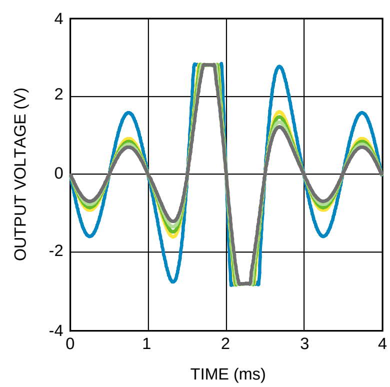

Figure 56. Clip Control Levels
V_{DD} = 3.3V, V_{IN} = 8V_{PP} Shaped Burst, 1kHz
Blue = No Clip Disabled, Gray = Low, Light Green = Medium
Green = High, Yellow = Max

ALC HEADROOM

When either voltage limiter or no clip is enabled, it is still possible to drive LM49151 into clipping by overdriving the input volume stage of the signal path beyond its output dynamic range. In this case, clipping occurs at the input volume stage, and although ALC is active, the gain reduction will have no effect on the output clipping. The maximum input that can safely pass through the input volume stage can be calculated by following formula:

$$V_{IN} \leq \frac{V_{DD}}{\text{Av (volume gain)}} \quad (1)$$

So in the case of 0 dB volume gain, audio input has to be less than V_{DD} for both voltage limiter or No clip settings.

When voltage limiter is enabled, ALC can reach its max attenuation for lower voltage limit levels as shown in the Figure 57. Typically, after the ALC started working, with 6 dB of audio input change ALC is well within its regulation. Voltage limiter Input headroom can be increased by switching to the LS_GAIN to 18dB in the Gain Control Register (see Table 7).

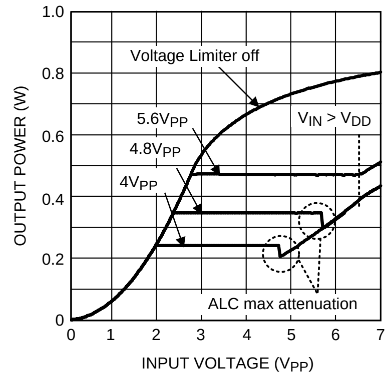

Figure 57. Voltage Limiter Function
V_{DD} = 3.3V, R_L = 8Ω+30µH
f_{IN} = 1kHz, LS_GAIN = 0

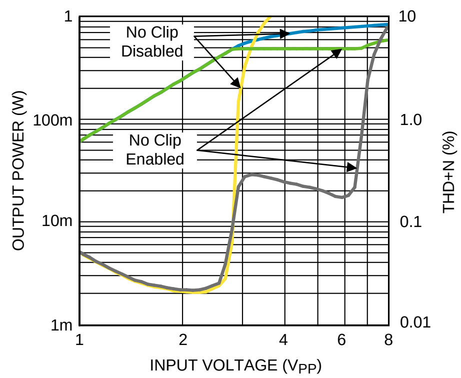

Figure 58. No Clip Function
V_{DD} = 3.3V, R_L = 8Ω+30µH
f_{IN} = 1kHz, LS_GAIN = 0
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

When No Clip is enabled, class D speaker output reduces when it's about to enter clipping region and power stay constant as long as V_{IN} is less than V_{DD} for 0 dB volume gain (see Figure 58). For example, in the case of V_{DD} = 3.3V, there is a 6 dB of headroom for the change in input. Please see the ALC typical performance curves for additional plots relating to different supply voltages and LS_GAIN settings for specific application parameters.

ATTACK TIME

Attack time (t_{ATK}) is the time it takes for the gain to be reduced by 6dB (LS_GAIN=0) once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of C_{SET} and the attack time coefficient as given by Equation 2:

$$t_{ATK} = 20k\Omega C_{SET} / \alpha_{ATK} \quad (s) \tag{2}$$

Where α_{ATK} is the attack time coefficient (Table 10) set by bits B4:B3 in the Voltage Limit Control Register (see Table 7). The attack time coefficient allows the user to set a nominal attack time. The internal 20kΩ resistor is subject to temperature change, and it has tolerance between -11% to +20%.

Table 10. Attack Time Coefficient

B5	B4	α_{ATK}
0	0	2.667
0	1	2
1	0	1.333
1	1	1

RELEASE TIME

Release time (t_{RL}) is the time it takes for the gain to return from 6dB (LS_GAIN=0) to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of C_{SET} and release time coefficient as given by Equation 3:

$$t_{RL} = 20M\Omega C_{SET} / \alpha_{RL} \quad (s) \tag{3}$$

where α_{RL} is the release time coefficient (Table 11) set by bits B4:B3 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20MΩ is subject to temperature change, and it has tolerance between -11% to +20%.

Table 11. Release Time Coefficient

B5	B4	α_{RL}
0	0	2
0	1	2.5
1	0	3
1	1	5

PROPER SELECTION OF EXTERNAL COMPONENTS

ALC Timing (C_{SET}) Capacitor Selection

The recommended range value of C_{SET} is between .01µF to 1µF. Lowering the value below .01µF can increase the attack time but LM49151 ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD+N and audio quality will be severely affected.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C_1)

The flying capacitor (C_1), see Figure 1, affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the RDS(ON) of the charge pump switches and the ESR of C1 and CPV_{SS} dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Hold Capacitor (CPV_{SS})

The value and ESR of the hold capacitor (CPV_{SS}) directly affects the ripple on CPV_{SS}. (see Figure 1) Increasing the value of CPV_{SS} reduces output ripple. Decreasing the ESR of CPV_{SS} reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49151. The input capacitors create a high-pass filter with the input resistors RIN. The -3dB point of the high-pass filter is found using Equation 4 below.

$$f = 1/\ 2\pi R_{IN} C_{IN} \quad \text{(Hz)} \tag{4}$$

Where the value of R_{IN} is given in the Electrical Characteristics Table.

High-pass filtering the audio signal helps protect the speakers. When the LM49151 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

Revision History

Rev	Date	Description
0.01	02/12/09	Initial PDF.
0.02	02/23/09	Text edits.
0.03	03/05/09	Text edits.
0.04	03/24/09	Text edits and added more graphs.
0.05	03/25/09	Cosmetic fixes.
0.06	03/26/09	Released 1–4 pages.
0.07	04/01/09	Text edits.
0.08	04/09/09	Text edits and edited the Ordering Information table.
0.09	04/15/09	Text edits.
0.10	05/19/09	Text edits.
0.11	09/04/09	Text edits.
0.12	09/18/09	Text edits.
0.13	10/29/09	Fixed typos on Table 4.
0.14	08/20/12	Full D/S to be released.
F	03/21/2013	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM49151TL/NOPB	Active	Production	DSBGA (YZR) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GL7
LM49151TL/NOPB.A	Active	Production	DSBGA (YZR) | 20	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GL7
LM49151TLX/NOPB	Active	Production	DSBGA (YZR) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GL7
LM49151TLX/NOPB.A	Active	Production	DSBGA (YZR) | 20	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GL7

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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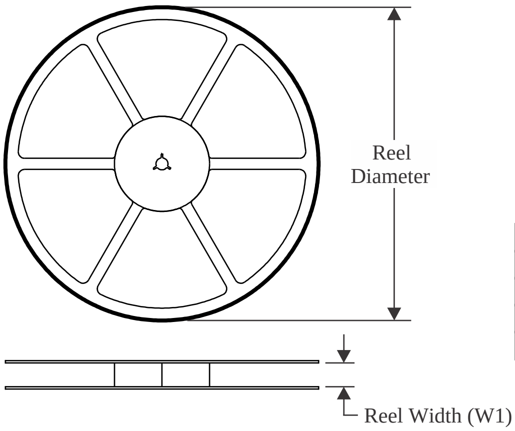
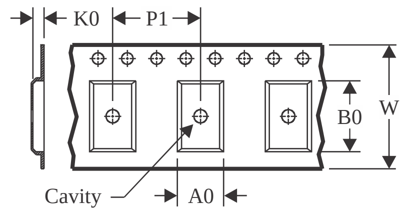
TAPE AND REEL INFORMATION

REEL DIMENSIONS

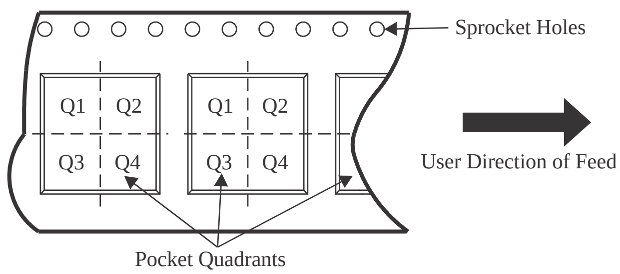


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

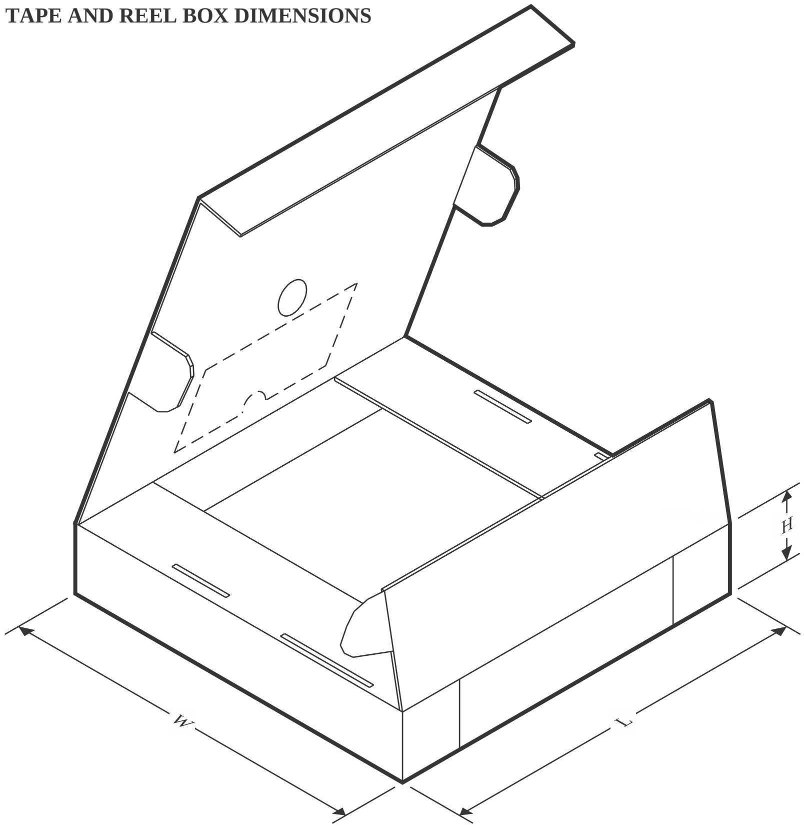
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49151TL/NOPB	DSBGA	YZR	20	250	178.0	8.4	2.34	2.85	0.76	4.0	8.0	Q1
LM49151TLX/NOPB	DSBGA	YZR	20	3000	178.0	8.4	2.34	2.85	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49151TL/NOPB	DSBGA	YZR	20	250	208.0	191.0	35.0
LM49151TLX/NOPB	DSBGA	YZR	20	3000	208.0	191.0	35.0