LM56 Dual Output Low Power Thermostat

Check for Samples: LM56

FEATURES

- **Digital Outputs Support TTL Logic Levels**
- **Internal Temperature Sensor**
- **2 Internal Comparators with Hysteresis**
- **Internal Voltage Reference**
- **Available in 8-pin SOIC and VSSOP Packages**

APPLICATIONS

- **Microprocessor Thermal Management**
- **Appliances**
- **Portable Battery Powered 3.0V or 5V Systems**
- **Fan Control**
- **Industrial Process Control**
- **HVAC Systems**
- **Remote Temperature Sensing**
- **Electronic System Protection**

DESCRIPTION

The LM56 is a precision low power thermostat. Two stable temperature trip points (V_{T1} and V_{T2}) are generated by dividing down the LM56 1.250V bandgap voltage reference using 3 external resistors. The LM56 has two digital outputs. OUT1 goes LOW when the temperature exceeds T1 and goes HIGH when the the temperature goes below ($T1–T_{HYST}$). Similarly, OUT2 goes LOW when the temperature exceeds T2 and goes HIGH when the temperature goes below ($T2–T_{HYST}$). T_{HYST} is an internally set 5°C typical hysteresis.

The LM56 is available in an 8-lead VSSOP surface mount package and an 8-lead SOIC.

Table 1. Key Specifications

	VALUE	UNIT
Power Supply Voltage	2.7V–10	V
Power Supply Current	230	µA (max)
V_{REF}	1.250	V ±1% (max)
Hysteresis Temperature	5	°C
Internal Temperature Sensor Output Voltage	(+6.20 mV/°C x T) + 395 mV	mV

Table 2. Temperature Trip Point Accuracy

	LM56BIM	LM56CIM
+25°C	±2°C (max)	±3°C (max)
+25°C to +85°C	±2°C (max)	±3°C (max)
−40°C to +125°C	±3°C (max)	±4°C (max)

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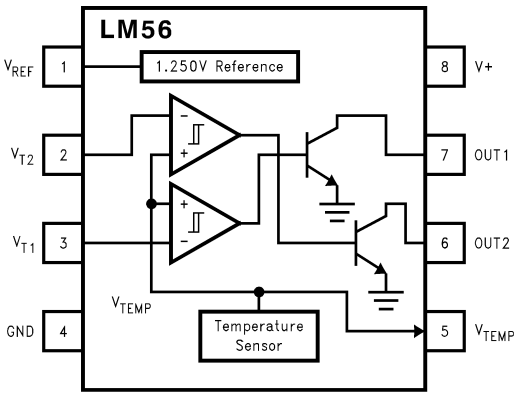
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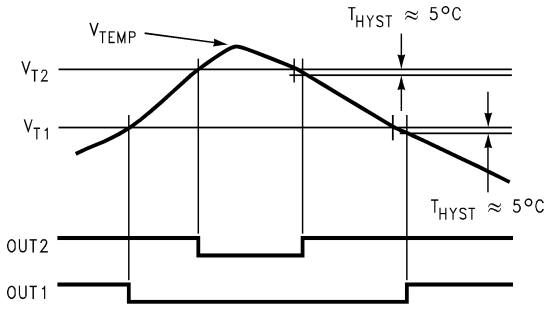
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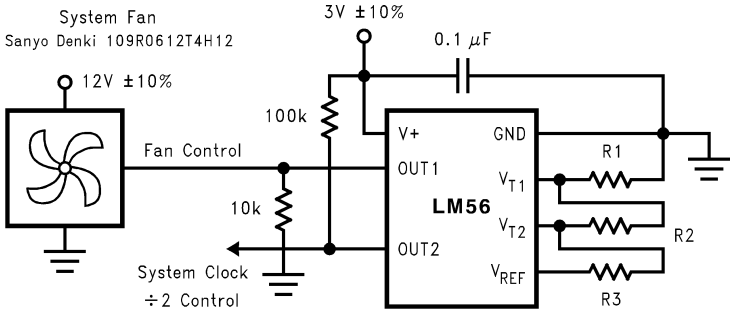
Simplified Block Diagram and Connection Diagram

Block Diagram





Typical Application



V_{T1} = 1.250V x (R1)/(R1 + R2 + R3)
V_{T2} = 1.250V x (R1 + R2)/(R1 + R2 + R3)
where:
(R1 + R2 + R3) = 27 kΩ and
$V_{T1 \text{ or } T2}$ = [6.20 mV/°C x T] + 395 mV therefore:
R1 = V_{T1}/(1.25V) x 27 kΩ
R2 = (V_{T2}/(1.25V) x 27 kΩ) − R1
R3 = 27 kΩ − R1 − R2

Figure 1. Microprocessor Thermal Management

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1]

Input Voltage		12V
Input Current at any pin[2]		5 mA
Package Input Current[2]		20 mA
Package Dissipation at T_A = 25°C[3]		900 mW
ESD Susceptibility[4]	Human Body Model - Pin 3 Only	800V
	All other pins	1000V
	Machine Model	125V
	Storage Temperature	−65°C to + 150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the LM56 Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) When the input voltage (V_I) at any pin exceeds the power supply (V_I < GND or V_I > V^+), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance) and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax}–T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 125°C. For this device the typical thermal resistance (θ_{JA}) of the different package types when board mounted follow:
(4) The human body model is a 100 pF capacitor discharge through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Ratings[1][2][3]

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM56BIM, LM56CIM	−40°C ≤ T_A ≤ +125°C
Positive Supply Voltage (V^+)	+2.7V to +10V
Maximum V_{OUT1} and V_{OUT2}	+10V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the LM56 Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Soldering process must comply with Reflow Temperature Profile specifications. Refer to http://www.ti.com/packaging.
(3) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Package Type	θ_{JA}
D0008A	110°C/W
DGK0008A	250°C/W

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LM56 Electrical Characteristics

The following specifications apply for V^+ = 2.7 V_{DC}, and V_{REF} load current = 50 µA unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Typical (1)	LM56BIM Limits (2)	LM56CIM Limits (2)	Units (Limits)
Temperature Sensor						
	Trip Point Accuracy (Includes V_{REF}, Comparator Offset, and Temperature Sensitivity errors)			±2	±3	°C (max)
		+25°C ≤ T_A ≤ +85°C		±2	±3	°C (max)
		−40°C ≤ T_A ≤ +125°C		**±3**	**±4**	°C (max)
	Trip Point Hysteresis	T_A = −40°C	4	3	3	°C (min)
				6	6	°C (max)
		T_A = +25°C	5	3.5	3.5	°C (min)
				6.5	6.5	°C (max)
		T_A = +85°C	6	4.5	4.5	°C (min)
				7.5	7.5	°C (max)
		T_A = +125°C	6	4	4	°C (min)
				8	8	°C (max)
	Internal Temperature Sensitivity		+6.20			mV/°C
	Temperature Sensitivity Error			±2	±3	°C (max)
				±3	**±4**	°C (max)
	Output Impedance	−1 µA ≤ I_L ≤ +40 µA		**1500**	**1500**	Ω (max)
	Line Regulation	+3.0V ≤ V^+ ≤ +10V, +25 °C ≤ T_A ≤ +85 °C		–0.72/+0.36	–0.72/+0.36	mV/V (max)
		+3.0V ≤ V^+ ≤ +10V, −40 °C ≤ T_A <25 °C		–1.14/+0.61	–1.14/+0.61	mV/V (max)
		+2.7V ≤ V^+ ≤ +3.3V		**±2.3**	**±2.3**	mV (max)
V_{T1} and V_{T2} Analog Inputs						
I_{BIAS}	Analog Input Bias Current		150	**300**	**300**	nA (max)
V_{IN}	Analog Input Voltage Range		V^+ − 1			V
			GND			V
V_{OS}	Comparator Offset		2	**8**	**8**	mV (max)
V_{REF} Output						
V_{REF}	V_{REF} Nominal		1.250V			V
	V_{REF} Error			**±1**	**±1**	% (max)
				±12.5	**±12.5**	mV (max)
$\Delta V_{REF}/\Delta V^+$	Line Regulation	+3.0V ≤ V^+ ≤ +10V	0.13	**0.25**	**0.25**	mV/V (max)
		+2.7V ≤ V^+ ≤ +3.3V	0.15	**1.1**	**1.1**	mV (max)
$\Delta V_{REF}/\Delta I_L$	Load Regulation Sourcing	+30 µA ≤ I_L ≤ +50 µA		**0.15**	**0.15**	mV/µA (max)

(1) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(2) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Units (Limits)
V^+ Power Supply					
I_S	Supply Current	V^+ = +10V		**230**	µA (max)
		V^+ = +2.7V		**230**	µA (max)
Digital Outputs					
$I_{OUT("1")}$	Logical "1" Output Leakage Current	V^+ = +5.0V		**1**	µA (max)
$V_{OUT("0")}$	Logical "0" Output Voltage	I_{OUT} = +50 µA		**0.4**	V (max)

(1) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(2) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

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Typical Performance Characteristics

Quiescent Current vs Temperature

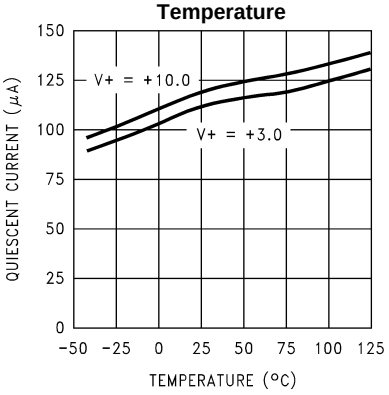


Figure 2.

V_{REF} Output Voltage vs Load Current

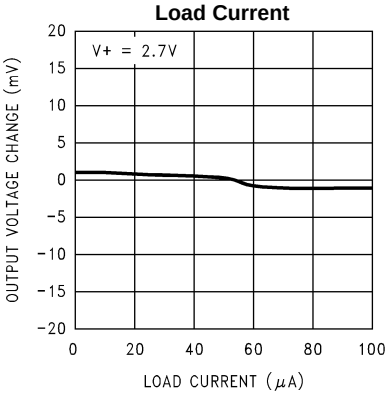


Figure 3.

OUT1 and OUT2 Voltage Levels vs Load Current

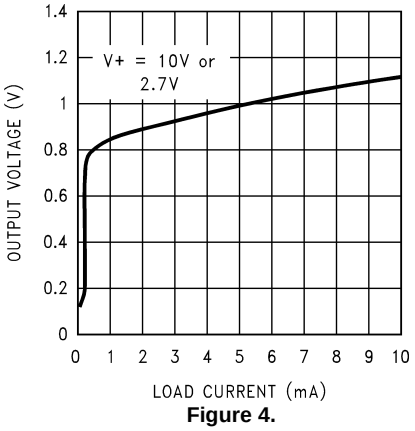


Figure 4.

Trip Point Hysteresis vs Temperature

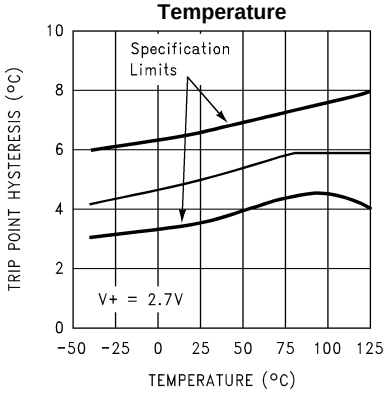


Figure 5.

Temperature Sensor Output Voltage vs Temperature

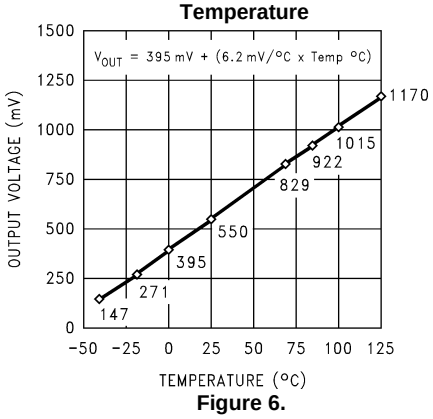


Figure 6.

Temperature Sensor Output Accuracy vs Temperature

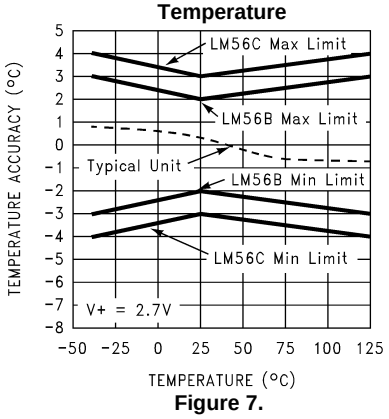


Figure 7.

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Typical Performance Characteristics (continued)

Trip Point Accuracy vs Temperature

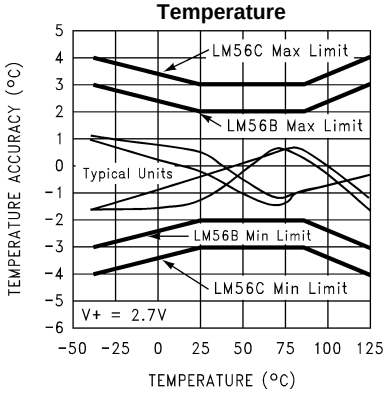


Figure 8.

Comparator Bias Current vs Temperature

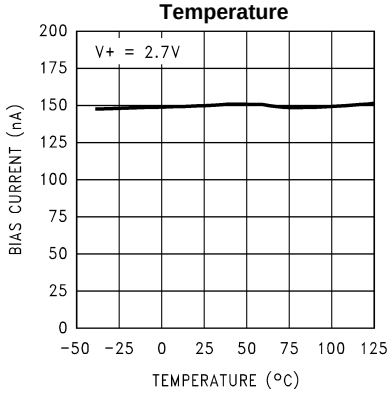


Figure 9.

OUT1 and OUT2 Leakage Current vs Temperature

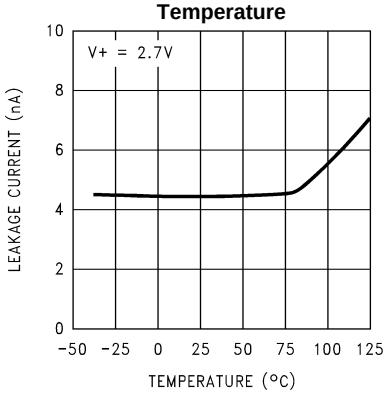


Figure 10.

V_{TEMP} Output Line Regulation vs Temperature

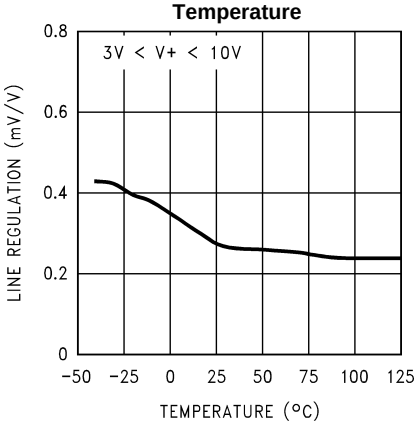


Figure 11.

V_{REF} Start-Up Response

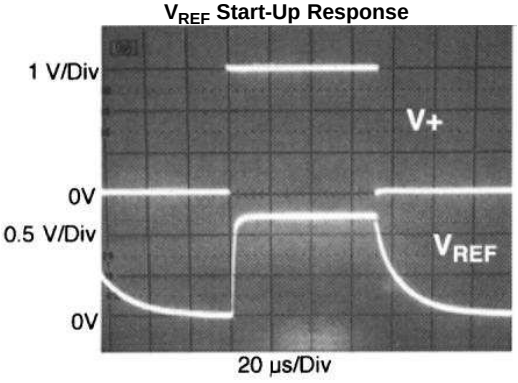


Figure 12.

V_{TEMP} Start-Up Response

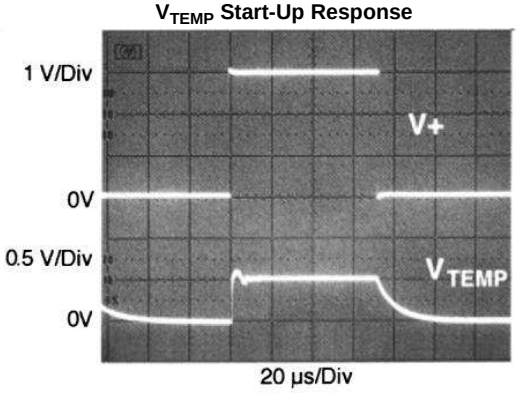
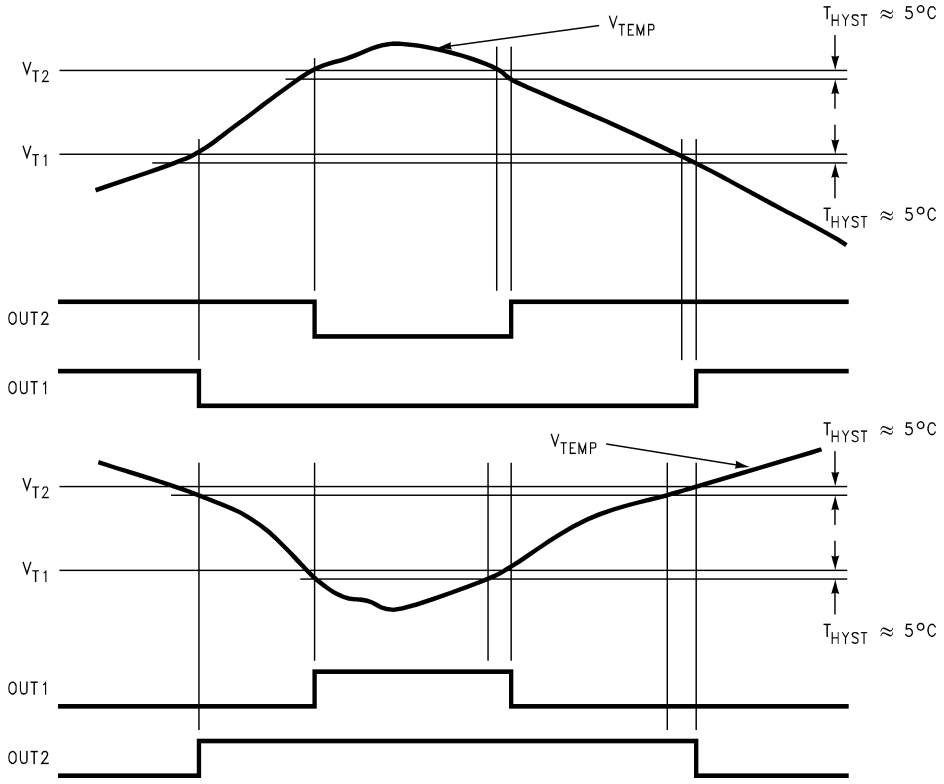


Figure 13.

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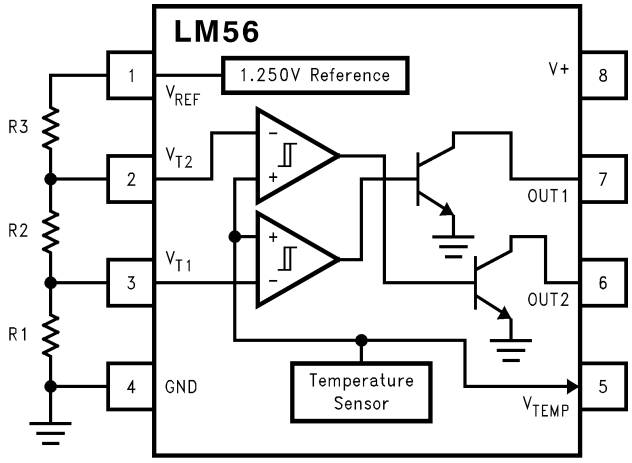
FUNCTIONAL DESCRIPTION



Pin Functions

V^+	This is the positive supply voltage pin. This pin should be bypassed with a 0.1 µF capacitor to ground.
GND	This is the ground pin.
V_{REF}	This is the 1.250V bandgap voltage reference output pin. In order to maintain trip point accuracy this pin should source a 50 µA load.
V_{TEMP}	This is the temperature sensor output pin.
OUT1	This is an open collector digital output. OUT1 is active LOW. It goes LOW when the temperature is greater than T_1 and goes HIGH when the temperature drops below T_1– 5°C. This output is not intended to directly drive a fan motor.
OUT2	This is an open collector digital output. OUT2 is active LOW. It goes LOW when the temperature is greater than the T_2 set point and goes HIGH when the temperature is less than T_2– 5°C. This output is not intended to directly drive a fan motor.
V_{T1}	This is the input pin for the temperature trip point voltage for OUT1.
V_{T2}	This is the input pin for the low temperature trip point voltage for OUT2.

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V_{T1} = 1.250V x (R1)/(R1 + R2 + R3)
V_{T2} = 1.250V x (R1 + R2)/(R1 + R2 + R3)
where:
(R1 + R2 + R3) = 27 kΩ and
$V_{T1\ or\ T2}$ = [6.20 mV/°C x T] + 395 mV therefore:
R1 = V_{T1}/(1.25V) x 27 kΩ
R2 = (V_{T2}/(1.25V) x 27 k)Ω–R1
R3 = 27 kΩ − R1 − R2

Application Hints

LM56 TRIP POINT ACCURACY SPECIFICATION

For simplicity the following is an analysis of the trip point accuracy using the single output configuration shown in Figure 14 with a set point of 82°C.

Trip Point Error Voltage = V_{TPE},

Comparator Offset Error for V_{T1E}

Temperature Sensor Error = V_{TSE}

Reference Output Error = V_{RE}

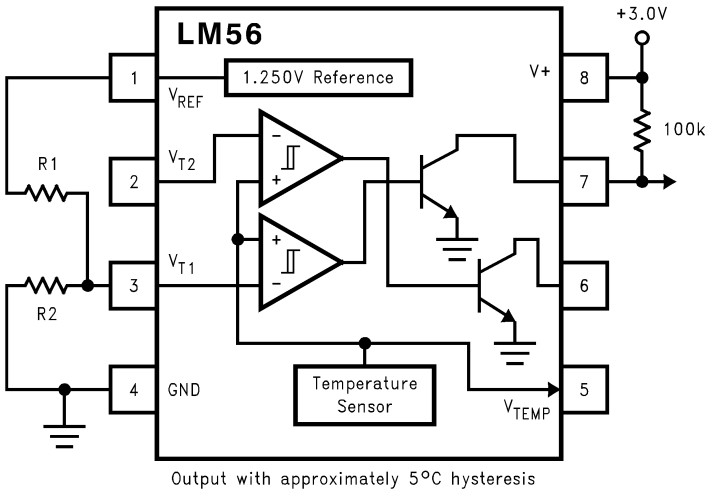


Figure 14. Single Output Configuration

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1. $V_{TPE} = \pm V_{T1E} - V_{TSE} + V_{RE}$

Where:

2. $V_{T1E} = \pm 8$ mV (max)

3. $V_{TSE} = (6.20\ mV/°C) \times (\pm 3°C) = \pm 18.6$ mV

4. $V_{RE} = 1.250V \times (\pm 0.01)\ R2/(R1 + R2)$

Using Equations from Figure 1.

$V_{T1} = 1.25V \times R2/(R1 + R2) = 6.20\ mV/°C)(82°C) + 395$ mV

Solving for $R2/(R1 + R2) = 0.7227$

then,

5. $V_{RE} = 1.250V \times (\pm 0.01)\ R2/(R1 + R2) = (0.0125) \times (0.7227) = \pm 9.03$ mV

The individual errors do not add algebraically because, the odds of all the errors being at their extremes are rare. This is proven by the fact the specification for the trip point accuracy stated in the LM56 Electrical Characteristics for the temperature range of −40°C to +125°C, for example, is specified at ±3°C for the LM56BIM. Note this trip point error specification does not include any error introduced by the tolerance of the actual resistors used, nor any error introduced by power supply variation.

If the resistors have a ±0.5% tolerance, an additional error of ±0.4°C will be introduced. This error will increase to ±0.8°C when both external resistors have a ±1% tolerance.

BIAS CURRENT EFFECT ON TRIP POINT ACCURACY

Bias current for the comparator inputs is 300 nA (max) each, over the specified temperature range and will not introduce considerable error if the sum of the resistor values are kept to about 27 kΩ as shown in the typical application of Figure 1. This bias current of one comparator input will not flow if the temperature is well below the trip point level. As the temperature approaches trip point level the bias current will start to flow into the resistor network. When the temperature sensor output is equal to the trip point level the bias current will be 150 nA (max). Once the temperature is well above the trip point level the bias current will be 300 nA (max). Therefore, the first trip point will be affected by 150 nA of bias current. The leakage current is very small when the comparator input transistor of the different pair is off (see Figure 15).

The effect of the bias current on the first trip point can be defined by the following equations:

$$K1 = \frac{R1}{R1 + R2 + R3}$$

$$V_{T1} = K1 \times V_{REF} + K1 \times (R2 + R3) \times \frac{I_B}{2} \quad (1)$$

where $I_B = 300$ nA (the maximum specified error).

The effect of the bias current on the second trip point can be defined by the following equations:

$$K2 = \frac{R1 + R2}{R1 + R2 + R3}$$

$$V_{T2} = K2 \times V_{REF} + \left(K1 + \frac{K2}{2}\right) \times R3 \times I_B \quad (2)$$

where $I_B = 300$ nA (the maximum specified error).

The closer the two trip points are to each other the more significant the error is. Worst case would be when $V_{T1} = V_{T2} = V_{REF}/2$.

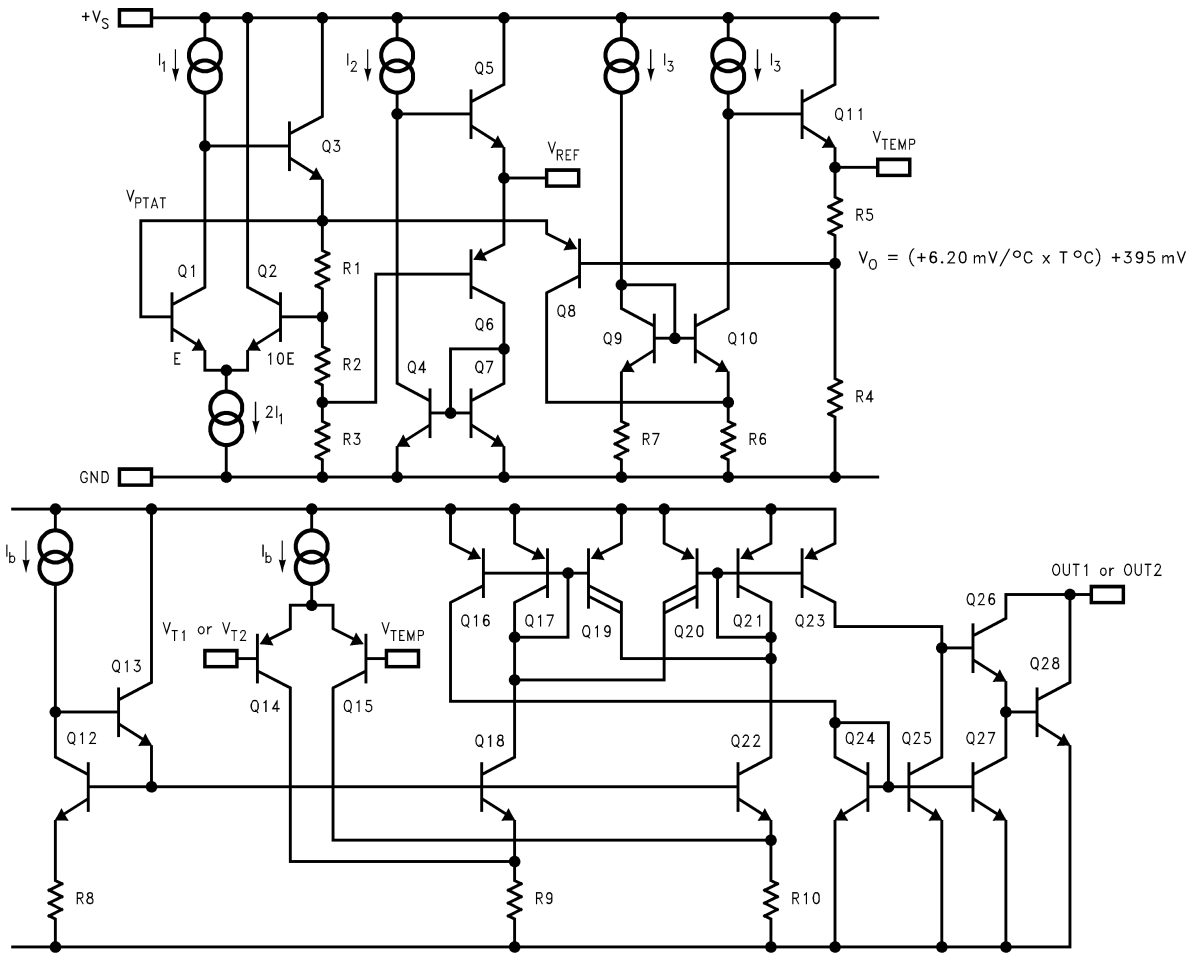


Figure 15. Simplified Schematic

MOUNTING CONSIDERATIONS

The majority of the temperature that the LM56 is measuring is the temperature of its leads. Therefore, when the LM56 is placed on a printed circuit board, it is not sensing the temperature of the ambient air. It is actually sensing the temperature difference of the air and the lands and printed circuit board that the leads are attached to. The most accurate temperature sensing is obtained when the ambient temperature is equivalent to the LM56's lead temperature.

As with any IC, the LM56 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit operates at cold temperatures where condensation can occur. Printed-circuit coatings are often used to ensure that moisture cannot corrode the LM56 or its connections.

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V_{REF} AND V_{TEMP} CAPACITIVE LOADING

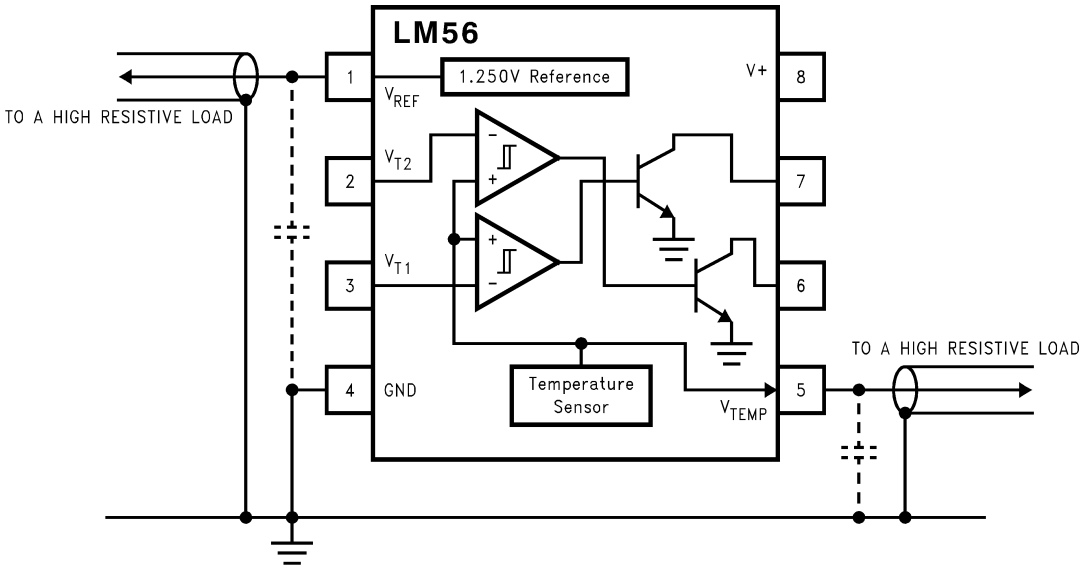


Figure 16. Loading of V_{REF} and V_{TEMP}

The LM56 V_{REF} and V_{TEMP} outputs handle capacitive loading well. Without any special precautions, these outputs can drive any capacitive load as shown in *Figure 16*.

NOISY ENVIRONMENTS

Over the specified temperature range the LM56 V_{TEMP}output has a maximum output impedance of 1500Ω. In an extremely noisy environment it may be necessary to add some filtering to minimize noise pickup. It is recommended that 0.1 µF be added from V^+ to GND to bypass the power supply voltage, as shown in Figure 16. In a noisy environment it may be necessary to add a capacitor from the V_{TEMP} output to ground. A 1 µF output capacitor with the 1500Ω output impedance will form a 106 Hz lowpass filter. Since the thermal time constant of the V_{TEMP} output is much slower than the 9.4 ms time constant formed by the RC, the overall response time of the V_{TEMP} output will not be significantly affected. For much larger capacitors this additional time lag will increase the overall response time of the LM56.

APPLICATIONS CIRCUITS

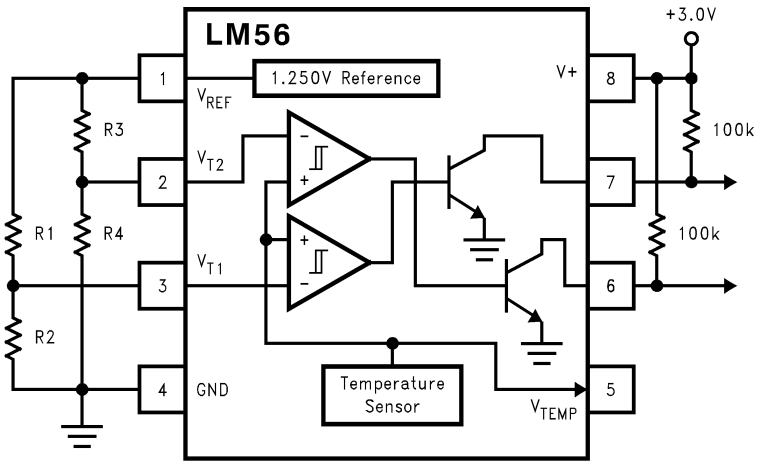


Figure 17. Reducing Errors Caused by Bias Current

The circuit shown in Figure 17 will reduce the effective bias current error for V_{T2} as discussed in Section 3.0 to be equivalent to the error term of V_{T1}. For this circuit the effect of the bias current on the first trip point can be defined by the following equations:

$$K1 = \frac{R2}{R1 + R2}$$

$$V_{T1} = K1 \times V_{REF} + K1 \times (R1) \times \frac{I_B}{2} \quad (3)$$

where I_B = 300 nA (the maximum specified error).

Similarly, bias current affect on V_{T2} can be defined by:

$$K2 = \frac{R4}{R3 + R4}$$

$$V_{T1} = K2 \times V_{REF} + K1 \times (R3) \times \frac{I_B}{2} \quad (4)$$

where I_B = 300 nA (the maximum specified error).

The current shown in Figure 18 is a simple overtemperature detector for power devices. In this example, an audio power amplifier IC is bolted to a heat sink and an LM56 Celsius temperature sensor is mounted on a PC board that is bolted to the heat sink near the power amplifier. To ensure that the sensing element is at the same temperature as the heat sink, the sensor's leads are mounted to pads that have feed throughs to the back side of the PC board. Since the LM56 is sensing the temperature of the actual PC board the back side of the PC board also has large ground plane to help conduct the heat to the device. The comparator's output goes low if the heat sink temperature rises above a threshold set by R1, R2, and the voltage reference. This fault detection output from the comparator now can be used to turn on a cooling fan. The circuit as shown in design to turn the fan on when heat sink temperature exceeds about 80°C, and to turn the fan off when the heat sink temperature falls below approximately 75°C.

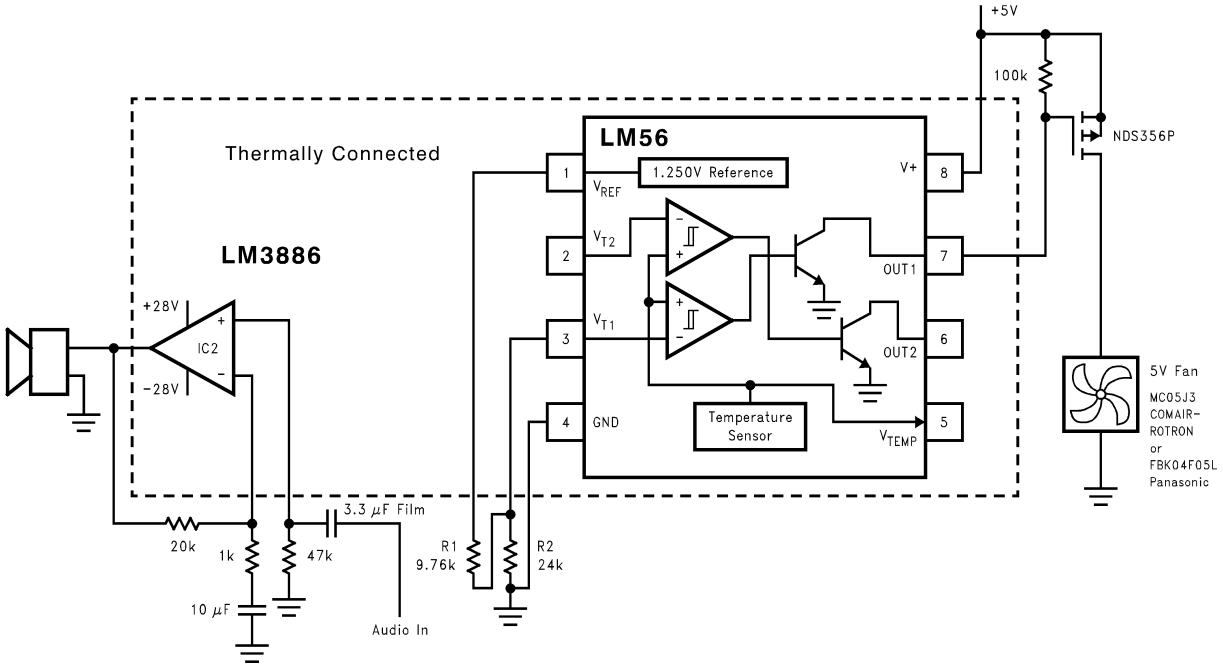


Figure 18. Audio Power Amplifier Overtemperature Detector

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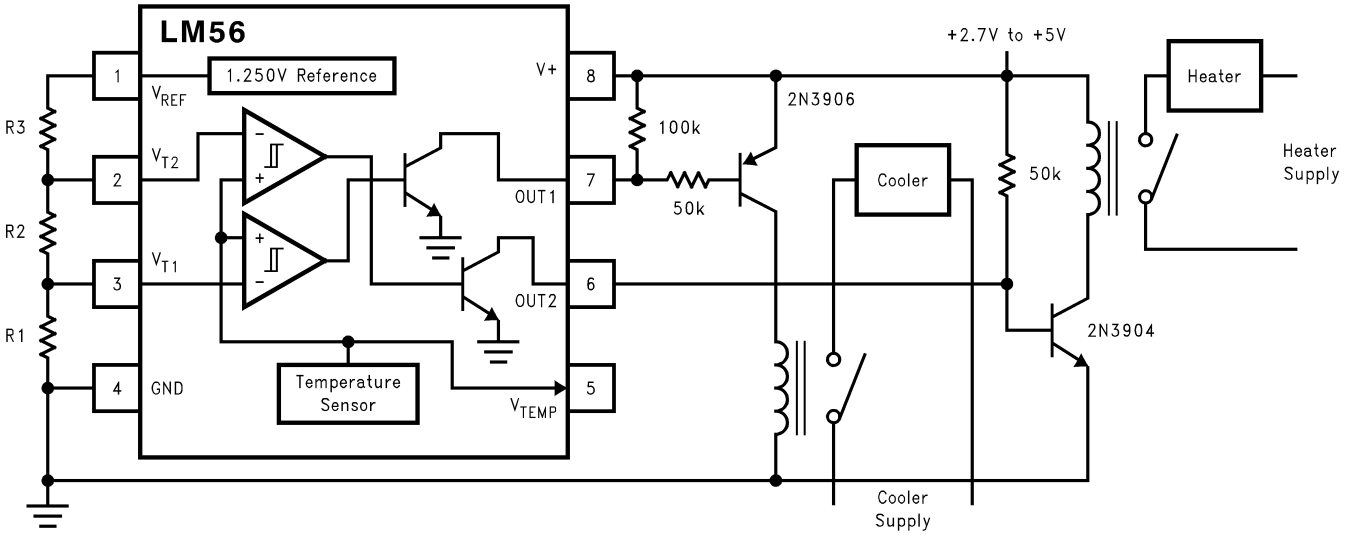


Figure 19. Simple Thermostat

REVISION HISTORY

Changes from Revision F (February 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	13

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM56BIM	NRND	Production	SOIC (D) | 8	95 | TUBE	No	SNPB	Level-1-235C-UNLIM	-40 to 125	LM56 BIM
LM56BIM.B	NRND	Production	SOIC (D) | 8	95 | TUBE	No	SNPB	Level-1-235C-UNLIM	-40 to 125	LM56 BIM
LM56BIM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LM56 BIM
LM56BIMM/NOPB	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	T02B
LM56BIMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02B
LM56BIMMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02B
LM56BIMMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02B
LM56BIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM56 BIM
LM56BIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM56 BIM
LM56BIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM56 BIM
LM56CIM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LM56 CIM
LM56CIMM/NOPB	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	T02C
LM56CIMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02C
LM56CIMMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02C
LM56CIMMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T02C
LM56CIMX	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	No	SNPB	Level-1-235C-UNLIM	-40 to 125	LM56 CIM
LM56CIMX.B	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	No	SNPB	Level-1-235C-UNLIM	-40 to 125	LM56 CIM
LM56CIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM56 CIM
LM56CIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM56 CIM
LM56CIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM56 CIM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

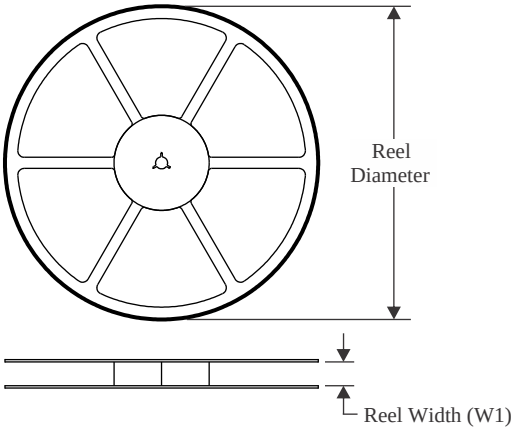
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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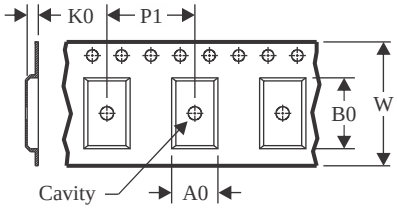
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

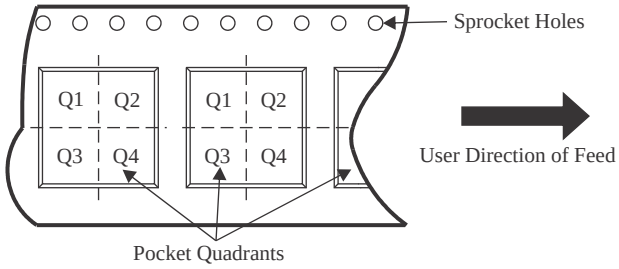


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

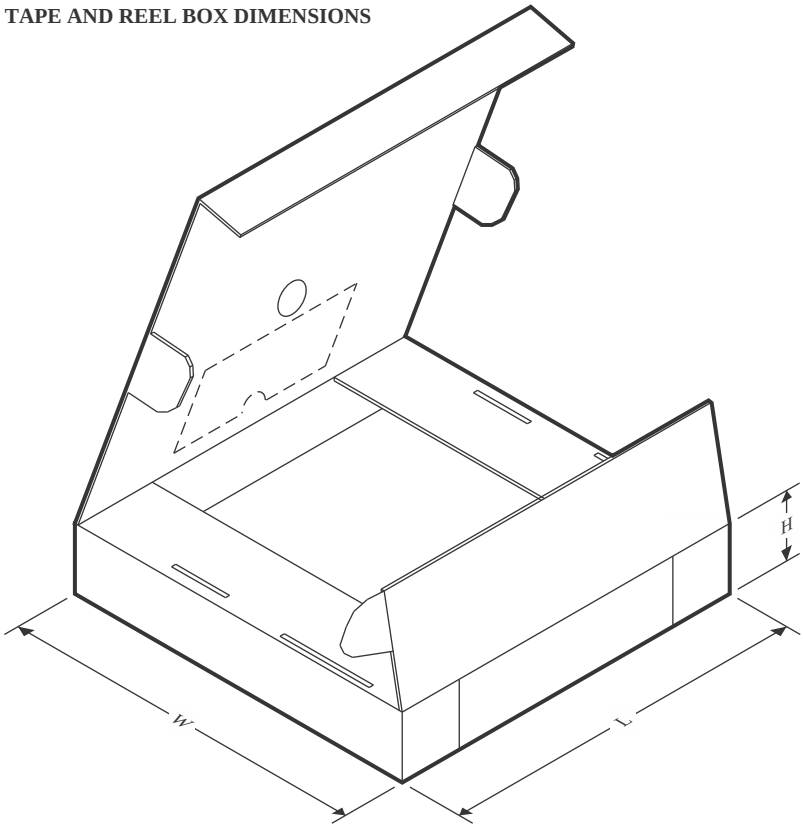
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM56BIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM56BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM56CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM56CIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

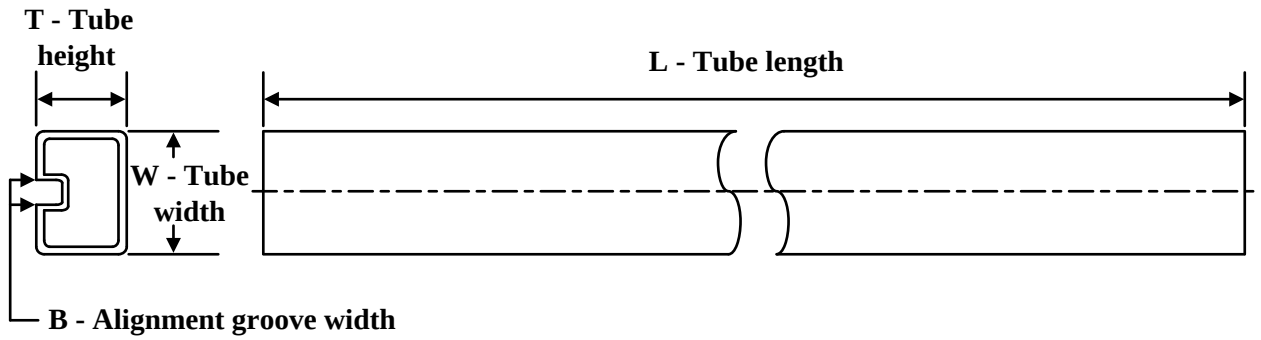
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM56BIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM56BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM56CIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM56CIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

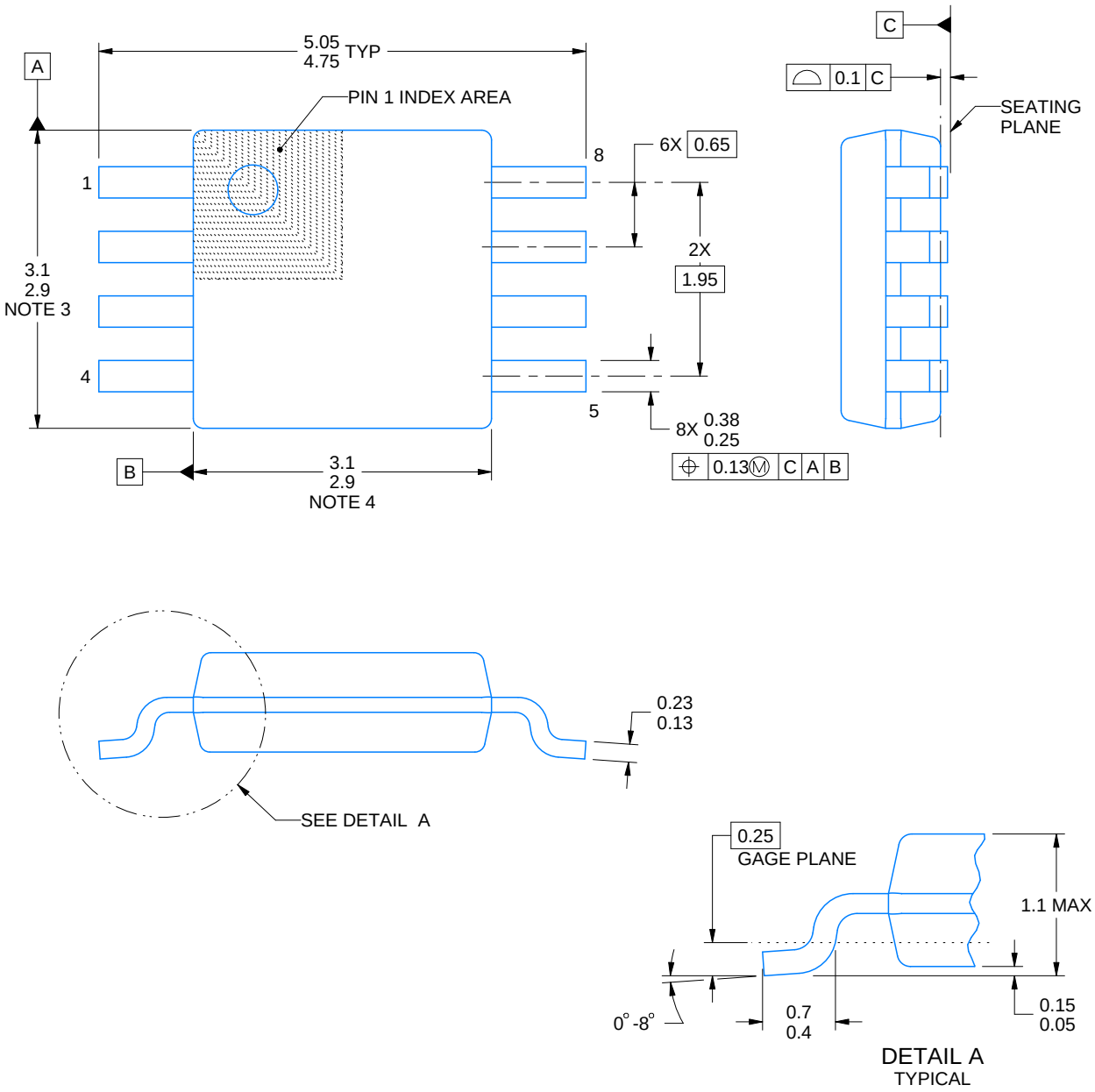
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM56BIM	D	SOIC	8	95	495	8	4064	3.05
LM56BIM	D	SOIC	8	95	495	8	4064	3.05
LM56BIM.B	D	SOIC	8	95	495	8	4064	3.05
LM56BIM.B	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

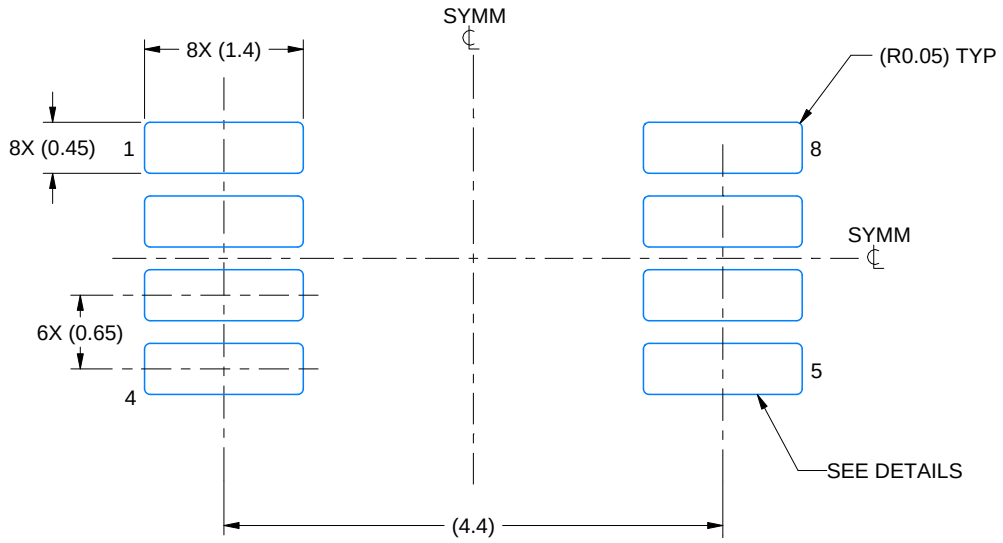
SMALL OUTLINE PACKAGE



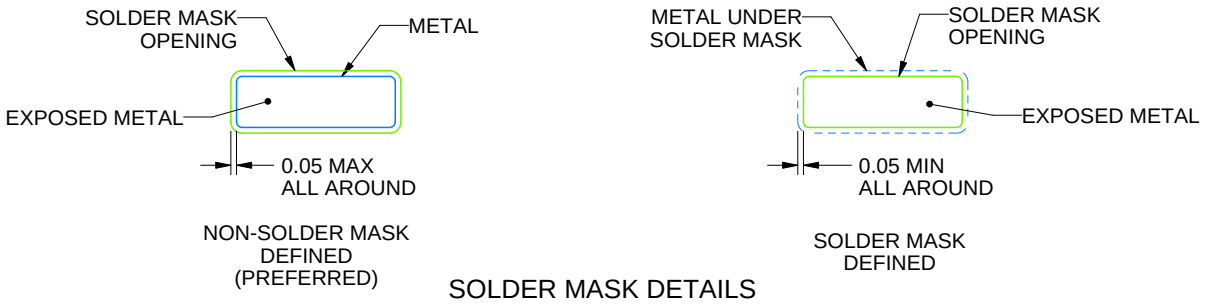
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

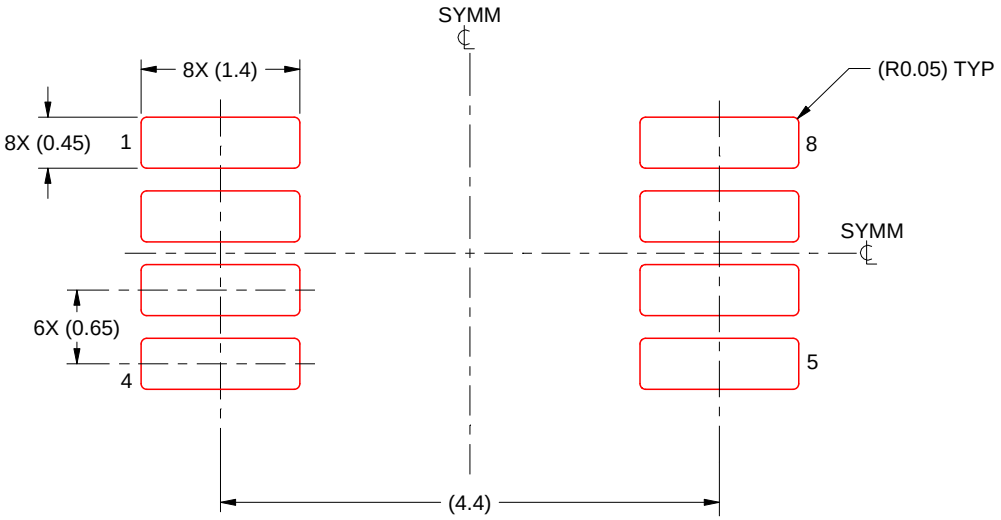


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

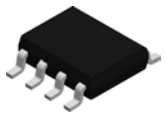


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

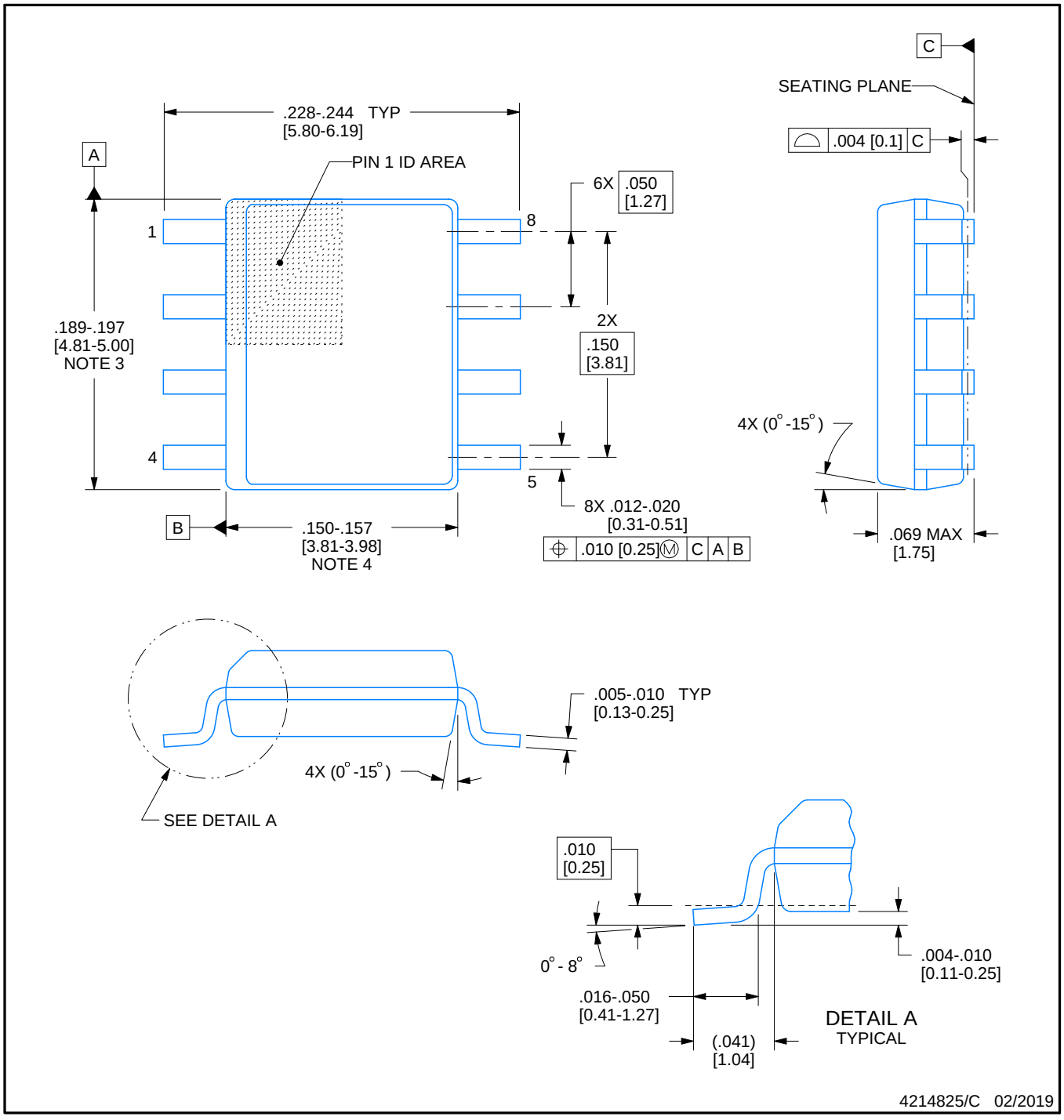


PACKAGE OUTLINE

D0008A

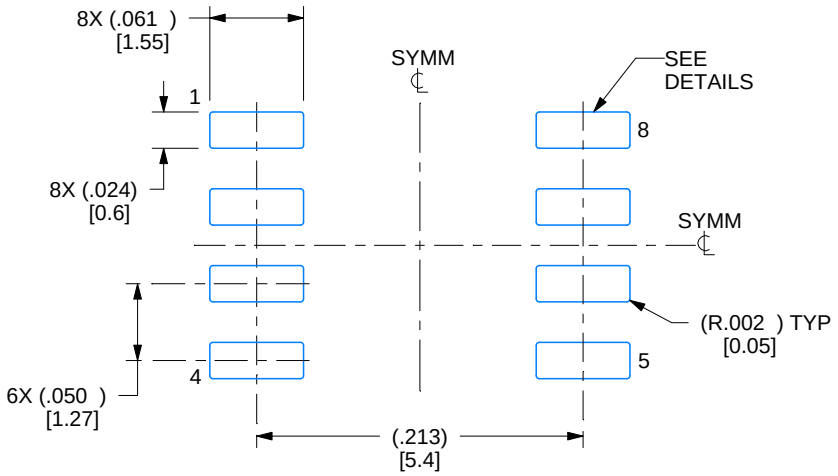
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

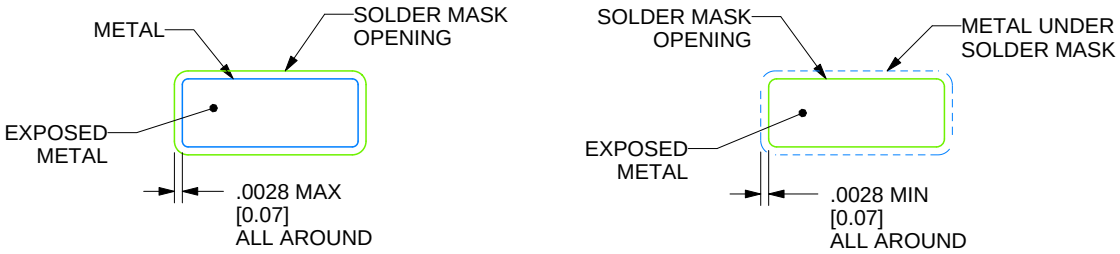


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

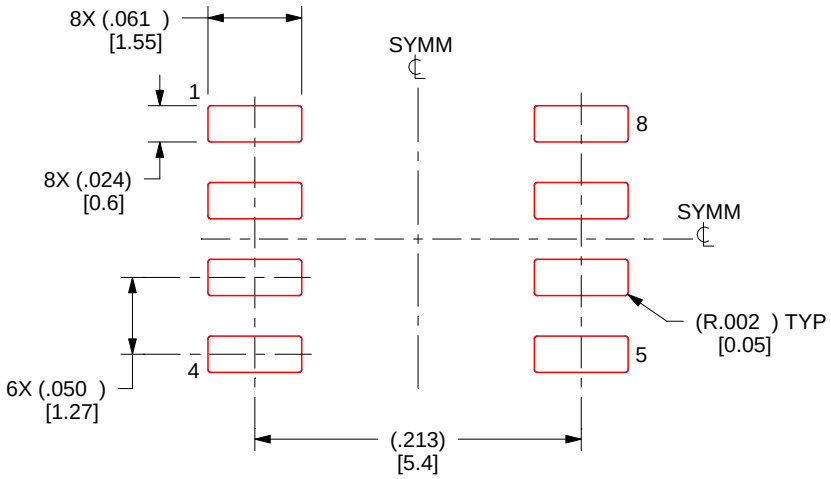
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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