LM7301 Low Power, 4-MHz GBW, Rail-to-Rail Input-Output Operational Amplifier in SOT-23 Package

1 Features

- At V_S = 5V (Typical Unless Otherwise Noted)
- Tiny, Space-Saving, 5-Pin SOT-23 Package
- Greater than Rail-to-Rail Input CMVR: −0.1V to 5.1V
- Rail-to-Rail Output Swing: 007V to 4.93V
- Wide Gain-Bandwidth: 4.5MHz
- Low Supply Current: 0.56mA
- Wide Supply Range: 2.7V to 32V
- High PSRR: 104dB
- High CMRR: 93dB
- Excellent Gain: 97dB

2 Applications

- Portable Instrumentation
- Signal Conditioning Amplifiers/ADC Buffers
- Active Filters
- Modems
- PCMCIA Cards

3 Description

The LM7301 provides high performance in a wide range of applications. The LM7301 offers greater than rail-to-rail input range, full rail-to-rail output swing, large capacitive load driving ability, and low distortion.

With only 0.56mA supply current, the 4.5MHz gain-bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

The LM7301 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

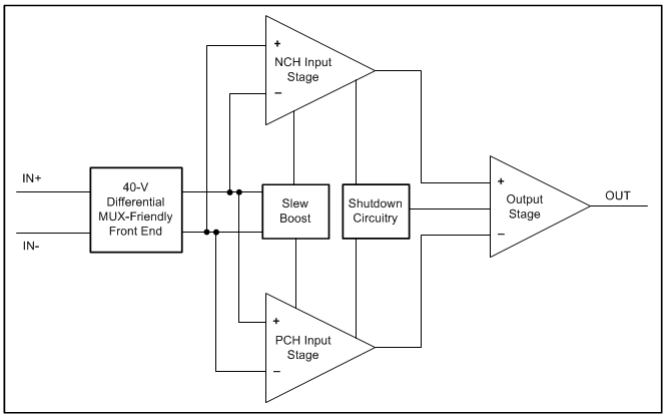
Operating on supplies of 2.7V to 32V, the LM7301 is excellent for a very wide range of applications in low power systems.

Placing the amplifier right at the signal source reduces board size and simplifies signal routing. The LM7301 fits easily on low profile PCMCIA cards.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM7301	SOIC (8)	4.90mm × 3.91mm
	SOT-23 (5)	2.90mm × 1.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Pin Configuration and Functions

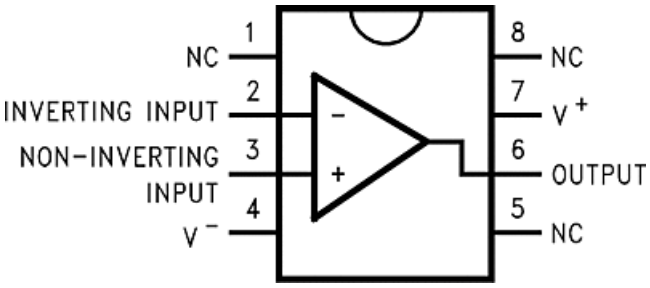


Figure 4-1. D Package 8-Pin SOIC Top View

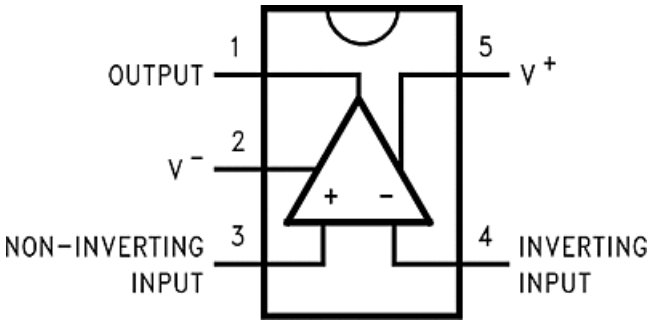


Figure 4-2. DBV Package 5-Pin SOT-23 Top View

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN	2	4	I	Inverting input voltage
+IN	3	3	I	Noninverting input voltage
N/C	1, 5, 8	—	—	No connection
OUT	6	1	O	Output
V–	4	2	I	Negative supply
V+	7	5	I	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
Differential input voltage		15	V
Voltage at input and output pin	(V^+) + 0.3	(V^-) – 0.3	V
Supply voltage $(V^+ - V^-)$		35	V
Current at input pin		±10	mA
Current at output pin(2)		±20	mA
Current at power supply pin		25	mA
Junction temperature, T_J (3)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V

(1) JEDEC document JEP155 states that 2500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Supply voltage		2.7		32	V
Operating temperature (3)		–40		85	°C
Package thermal resistance ($R_{\theta JA}$)(3)	5-pin SOT-23	325		325	°C/W
	8-pin SOIC	165		165	°C/W

5.4 Thermal Information

THERMAL METRIC(1)		LM7301		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169	120	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122	65	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17	16	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the TI application note *Semiconductor and IC Package Thermal Metrics*.

5.5 Electrical Characteristics: 2.7V to 32V DC

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1MΩ to V^+/2 unless noted that limits apply at the temperature extremes.(5) (4) (6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A = 25°C			0.03	6	mV
		T_A = T_J				8	
TCV_{OS}	Input offset voltage average drift	T_A = T_J			2		µV/°C
I_B	Input bias current	V_{CM} = 0V	T_A = 25°C		0.01	200	nA
			T_A = T_J			250	
		V_{CM} = 5V	T_A = 25°C		0.01	−75	
			T_A = T_J			−85	
I_{OS}	Input offset current	V_{CM} = 0V	T_A = 25°C		0.01	70	nA
			T_A = T_J			80	
		V_{CM} = 5V	T_A = 25°C		0.01	55	
			T_A = T_J			65	
R_{IN}	Input resistance, CM	0V ≤ V_{CM} ≤ 5V			540		GΩ
CMRR	Common mode rejection ratio	0V ≤ V_{CM} ≤ 5V	T_A = 25°C	70	88		dB
			T_A = T_J	67			
		0V ≤ V_{CM} ≤ 3.5V			93		
PSRR	Power supply rejection ratio	2.7V ≤ V^+ ≤ 30V	T_A = 25°C	87	104		dB
			T_A = T_J	84			
V_{CM}	Input common-mode voltage range	CMRR ≥ 65dB			5.1		V
					−0.1		
A_V	Large signal voltage gain	R_L = 10kΩ V_O = 4V_{PP}	T_A = 25°C	14	71		V/mV
			T_A = T_J	10			
V_O	Output swing	R_L = 10kΩ	T_A = 25°C		0.07	0.12	V
					4.93		
			T_A = T_J	4.88		0.15	
				4.85			
		R_L = 2kΩ	T_A = 25°C		0.14	0.2	
						0.22	
			T_A = T_J	4.80	4.87		
				4.78			
I_{SC}	Output short-circuit current	Sourcing	T_A = 25°C	8	75		mA
			T_A = T_J	5.5			
		Sinking	T_A = 25°C	6	75		
			T_A = T_J	5			
I_S	Supply current	T_A = 25°C			0.56	1.1	mA
		T_A = T_J				1.24	

5.6 Electrical Characteristics: AC

T_A = 25°C, V^+ = 2.2 V to 30 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$[6]

PARAMETER		TEST CONDITIONS	TYP [4]	UNIT
SR	Slew rate[1]	±4-V Step at V_S ±6 V	21	V/µs
GBW	Gain-bandwidth product	f = 100 kHz, R_L = 10 kΩ	4	MHz
e_n	Input-referred voltage noise	f = 1 kHz	36	nV/√Hz
i_n	Input-referred current noise	f = 1 kHz	0.24	pA/√Hz
T.H.D.	Total harmonic distortion	f = 10 kHz	0.006%	

(1) Refer Section 5.10 for more details.

5.7 Electrical Characteristics: 30-V DC

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 30 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$ unless noted that limits apply at the temperature[6]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage				0.04	6	mV
						8	
TCV_{OS}	Input offset voltage average drift	T_A = T_J			2		µV/°C
I_B	Input bias current	V_{CM} = 0V	T_A = 25°C		0.01	300	nA
			T_A = T_J			500	
		V_{CM} = 30V	T_A = 25°C	−100	−0.01		
			T_A = T_J	−200			
I_{OS}	Input offset current	V_{CM} = 0V	T_A = 25°C		0.01	90	nA
			T_A = T_J			190	
		V_{CM} = 30V	T_A = 25°C		0.01	65	
			T_A = T_J			135	
R_{IN}	Input resistance	0V ≤ V_{CM} ≤ 30V			540		GΩ
CMRR	Common mode rejection ratio	0V ≤ V_{CM} ≤ 30V	T_A = 25°C	80	104		dB
			T_A = T_J	78			
		0V ≤ V_{CM} ≤ 27V	T_A = 25°C	90	115		
			T_A = T_J	88			
PSRR	Power supply rejection ratio	2.7V ≤ V^+ ≤ 30V	T_A = 25°C	87	104		dB
			T_A = T_J	84			
V_{CM}	Input common-mode voltage range	CMRR > 80dB			30.1		V
					−0.1		
A_V	Large signal voltage gain	R_L = 10kΩ V_O = 28V_{PP}	T_A = 25°C	30	105		V/mV
			T_A = T_J	20			
V_O	Output swing	R_L = 10kΩ	T_A = 25°C		0.16	0.275	V
			T_A = T_J			0.375	
			T_A = 25°C	29.75	29.8		
			T_A = T_J	28.65			
I_{SC}	Output short-circuit current	Sourcing[3]	T_A = 25°C	8.8	75		mA
			T_A = T_J	6.5			
		Sinking[3]	T_A = 25°C	8.2	75		
			T_A = T_J	6			

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 30 V, V^- = 0 V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2 unless noted that limits apply at the temperature[6]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Supply current	T_A = 25°C		0.56	1.3	mA
		T_A = T_J			1.35	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(5) All limits are ensured by testing or statistical analysis.
(6) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that $T_J = T_A$. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

5.8 Typical Characteristics

T_A = 25°C, R_L = 1MΩ unless otherwise specified

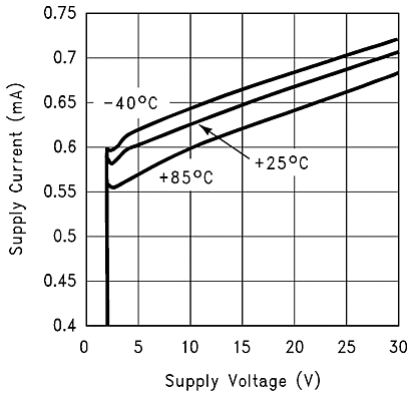


Figure 5-1. Supply Current vs Supply Voltage

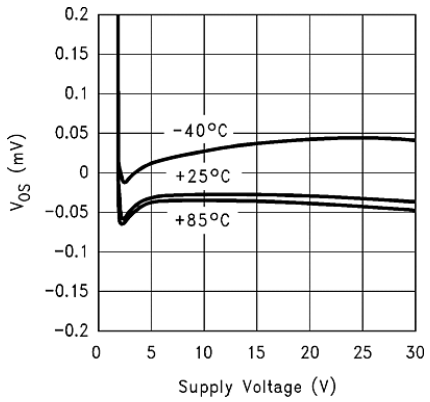


Figure 5-2. V_{OS} vs Supply Voltage

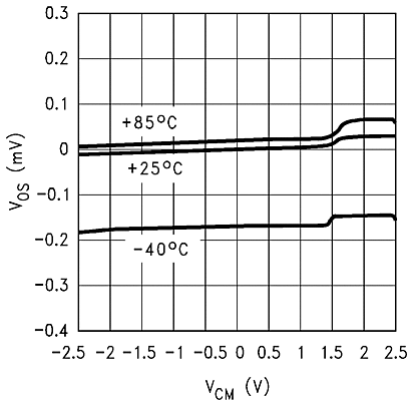


Figure 5-3. V_{OS} vs V_{CM} V_S = ±2.5 V

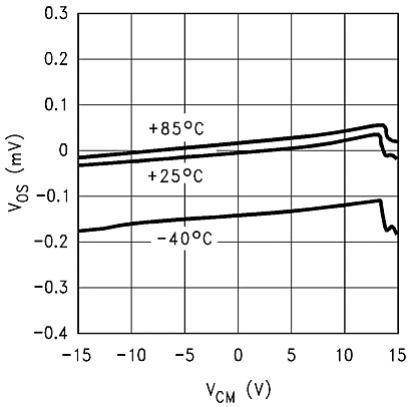


Figure 5-4. V_{OS} vs V_{CM} V_S = ±15 V

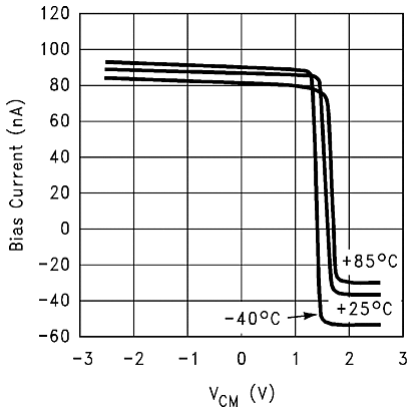


Figure 5-5. Inverting Input Bias Current vs Common Mode Voltage V_S = ±2.5 V,Old Die

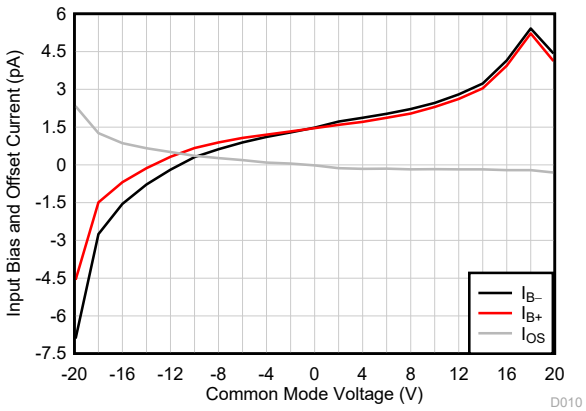


Figure 5-6. Input Bias Current vs Common-Mode Voltage V_S= ±20V, New Die

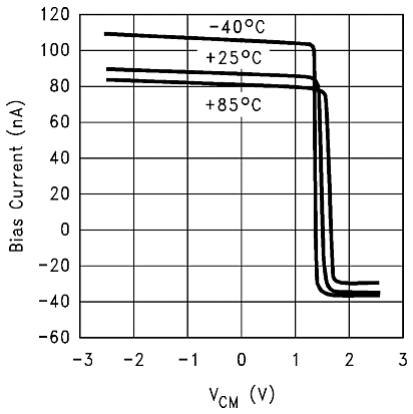


Figure 5-7. Noninverting Input Bias Current vs Common Mode Voltage V_S = ±2.5 V, Old Die

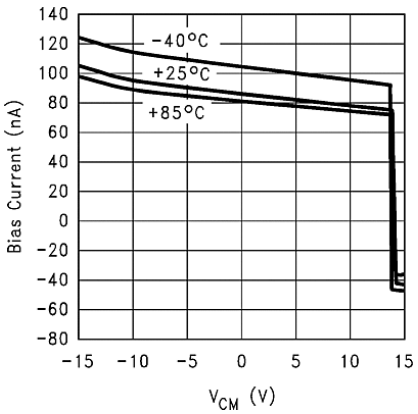


Figure 5-8. Noninverting Input Bias Current vs Common Mode Voltage V_S = ±15 V

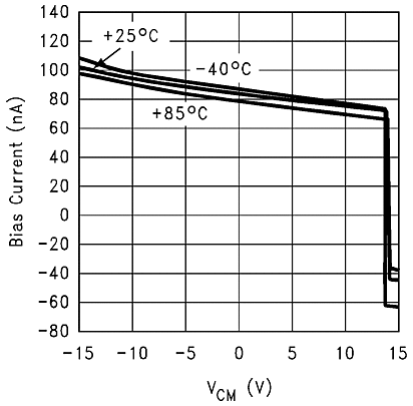


Figure 5-9. Inverting Input Bias Current vs Common Mode Voltage V_S = ±15 V

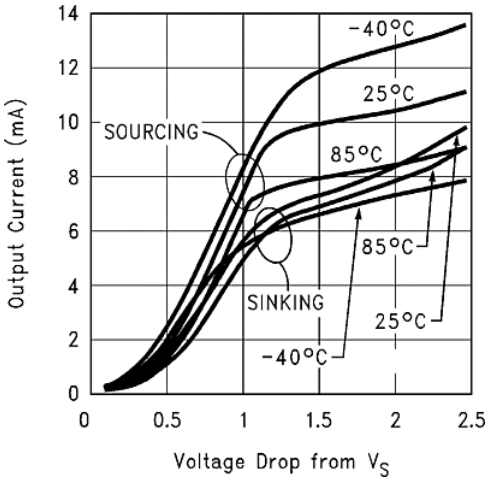


Figure 5-10. V_O vs I_O V_S = ±2.5 V

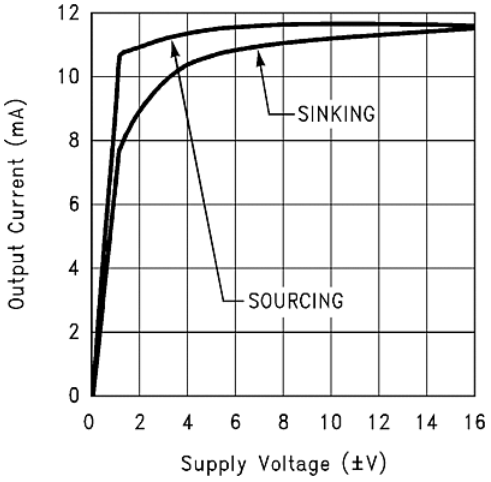


Figure 5-11. Short-Circuit Current vs Supply Voltage

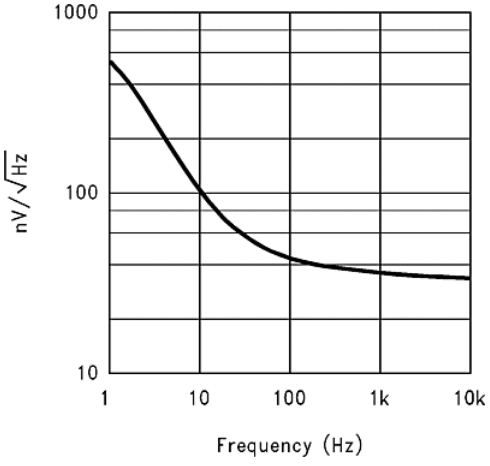


Figure 5-12. Voltage Noise vs Frequency

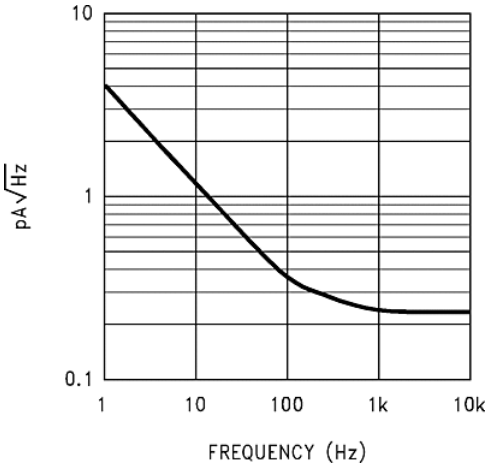


Figure 5-13. Current Noise vs Frequency

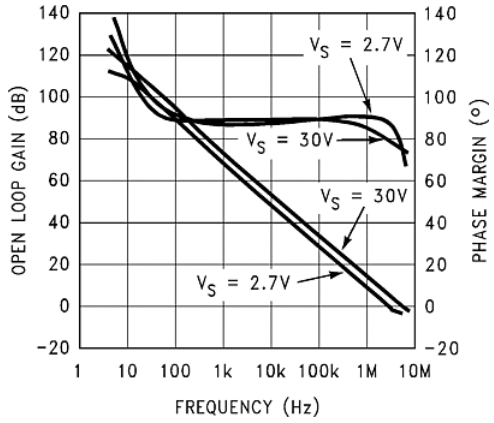


Figure 5-14. Gain and Phase

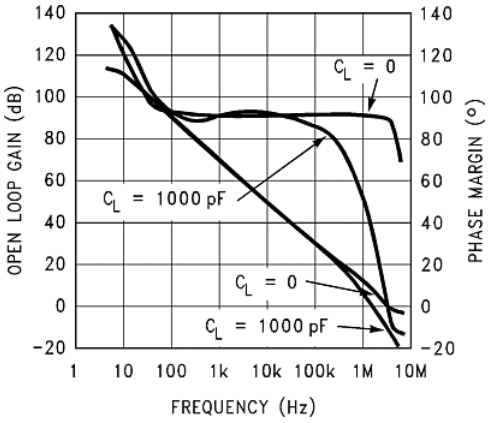
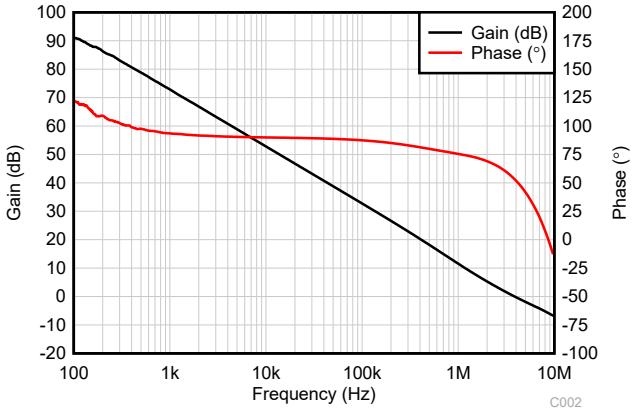


Figure 5-15. Gain and Phase, 2.7V Supply



C_L = 20pF

Figure 5-16. Open-Loop Gain and Phase vs Frequency V_S= ±20V R_L= 10Ω, New Die

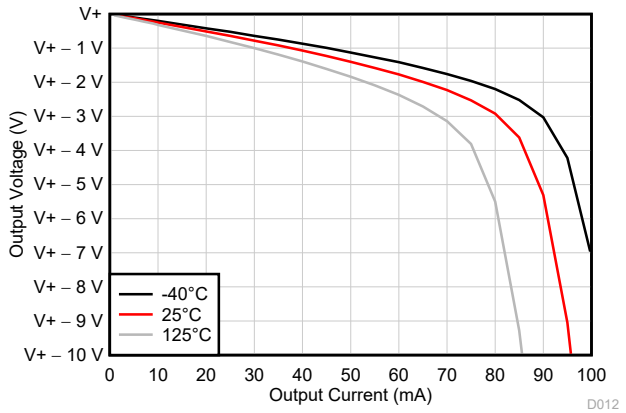


Figure 5-17. Output Voltage Swing vs Output Current (Sourcing) V_S= ±20V, New Die

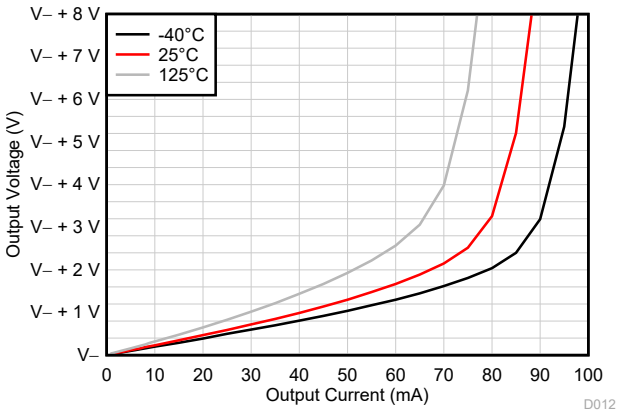


Figure 5-18. Output Voltage Swing vs Output Current (Sinking) V_S= ±20V, New Die

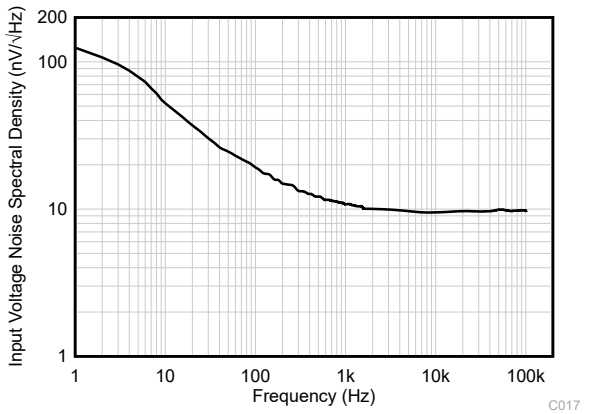


Figure 5-19. Input Voltage Noise Spectral Density vs Frequency V_S= ±20V, New Die

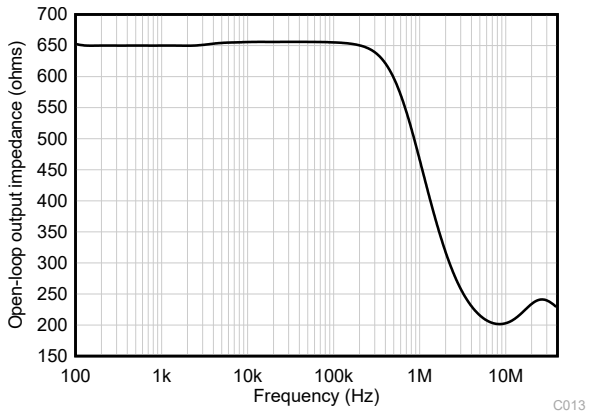


Figure 5-20. Open-Loop Output Impedance vs Frequency V_S= ±20V, New Die

5.9 Old Versus New Die Comparison

As of the publication of revision J of this data sheet, Texas Instruments has moved manufacturing of the die for LM7301 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “GF6”, for the new die CSO is “RFB”. The old die information is maintained in this data sheet for comparison purposes, but all new manufacturing has moved to the new die.

Description	Old Die	New Die
Minimum supply voltage	2.2V	2.7V
Input bias current (typ)	90nA	10pA
Current between inputs (Differential input voltage between input and inverting input = 2V)	230µA (two diodes and 2.5kΩ resistance between inputs)	< 100pA
Output voltage slew architecture	Standard slew architecture	Slew-boosted architecture, can impact signal distortion above 100kHz, 0.8Vp

5.10 Slew rate

The output rate of change strongly depends on the input differential voltage. The maximum output rate of change is known as the slew rate. Figure 5-21 shows a generic simplified block diagram of an operational amplifier with the Miller compensation capacitor C_M and measured data of the Output Rate of Change vs Input Differential Voltage (V_{ID}). With slew boost architectures the compensation capacitor, C_M known as the miller capacitor, is charged in 3 discrete regions with varying current I_{C_M} , where the output rate of change is $\frac{dV_{out}}{dt} \approx \frac{I_{C_M}}{C_M}$. Note $I_{C_M} = I_{gm\_max} + I_{boost}$.

1. Small signal output rate of change (linear region): $\frac{dV_{out}}{dt} \approx \frac{I_{gm}}{C_M}$; $I_{boost} = 0$ mA and $I_{gm} < I_{gm\_max}$
   - Note that the relationship between V_{ID} and I_{gm} is linear in this region. See the green region in Figure 5-21. Typically, small signals are less than 100mV. For this device the small signal region is approximately 20mV and less.
2. Moderate input differential voltages (nonlinear region): $Natural\_SR \approx \frac{I_{gm\_max}}{C_M}$; $I_{boost} = 0$ mA and $I_{gm} = I_{gm\_max}$

- There is a rising slope as I_{gm} approaches I_{gm_Max} . See the blue region in Figure 5-21. For this device the natural slew is 0.5V/µs and occurs for input signals of 20mV to 150mV.

3. Large input differential voltages (nonlinear region): $Boosted\_SR \approx \frac{I_{gm\_max} + I_{boost}}{C_M}$.
   - The slew boost circuitry is activated and additional current I_{boost} helps charge the compensation capacitor quickly. See the red region in Figure 5-21. For this device the boosted slew rate is 30V/µs and occurs for input signals greater than 150mV. Technically the boosted slew is increasing from approximately 150mV to 1V, and for input signals greater than 1V the max the slew boost is achieved.

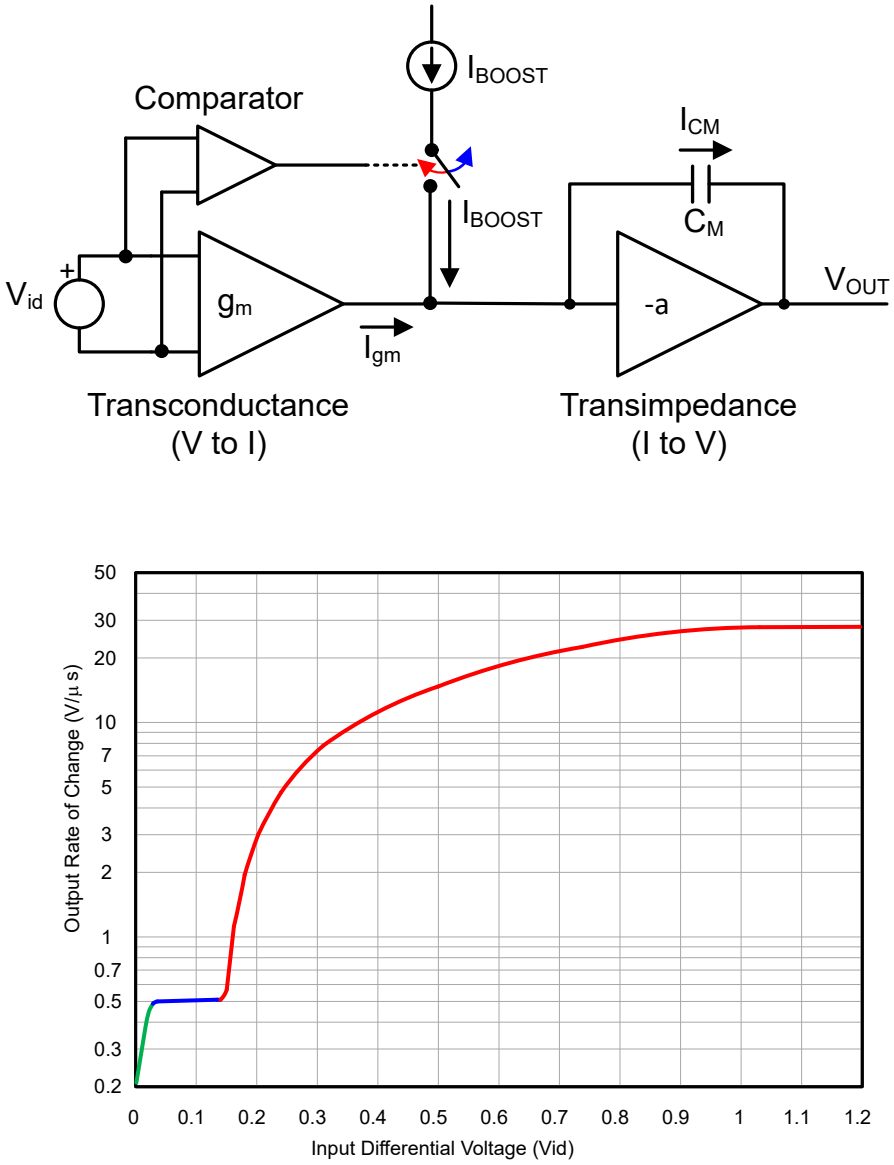


Figure 5-21. Simplified block diagram of an operational amplifier with Miller compensation capacitor and measured data of the Output Rate of Change vs Input Differential Voltage

Figure 5-22 below shows the Output Rate of Change vs Input Differential Voltage comparison of the New device vs the Old device.

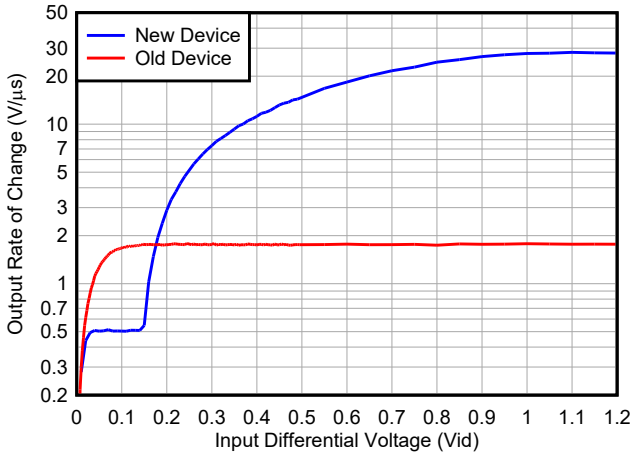


Figure 5-22. Output Rate of Change vs Input Differential Voltage comparison of the New device vs the Old device.

6 Power Supply Recommendations

The LM7301 is specified for operation from 2.7V to 32V (±1.35V to ±16V). Being a rail-to-rail input and output device, any operating voltage conditions within the supply voltage range can be accommodated.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

7 Layout

7.1 Layout Guidelines

For best operational performance of the device, TI recommends good printed-circuit board (PCB) layout practices. Low-loss, 0.1-µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single supply applications.

7.2 Layout Example

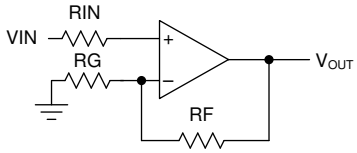


Figure 7-1. Schematic Representation

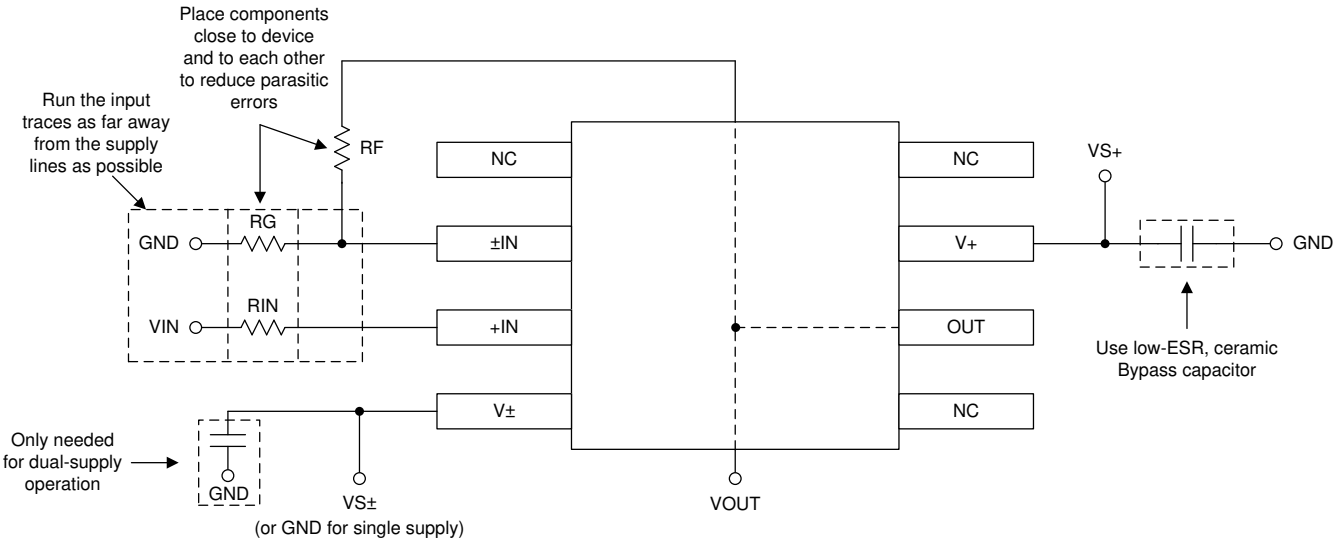


Figure 7-2. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.2 Trademarks

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8.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2016) to Revision J (January 2026)	Page
• Updated Greater than Rail-to-Rail Input CMVR values from -0.25V to -0.1V and 5.2V to 5.1V	1
• Updated Wide Gain-Bandwidth from 4MHz to 4.5MHz	1
• Updated Low Supply Current from 0.6mA to 0.56mA	1
• Updated Wide Supply Range value from 1.8V to 2.7V	1
• Updated Gain-Bandwidth from 4MHz to 4.5MHz	1
• Updated Supply Current from 0.6mA to 0.56mA	1
• Updated Supply Range value from 1.8V to 2.7V	1
• Removed Gain and Phase plot and "Gain and Phase, 2.7V Supply" plot	1
• Updated Supply min value from 1.8V to 2.7V	4
• Updated 5V DC to 2.7V to 32V DC	5
• Updated Input bias currents for 25°C typical to 0.01nA	5
• Updated Input offest currents for 25°C typical to 0.01nA	5
• Updated Input resistance typical from 39MΩ to 540GΩ	5
• Updated Output short-circuit current" typical for 25°C to 75mA	5
• Updated Supply current typical for 25°C from 0.6mA to 0.56mA	5
• Updated Power supply rejection ratio range from 2.2V to 2.7V	5
• Changed Slew rate value from 1.25V/µs to 21V/µs	6
• Deleted *Electrical Characteristics 2.2-V DC*	6
• Updated Input bias currents for 25°C typical to 0.01nA	6
• Updated Input offest currents for 25°C typical to 0.01nA	6
• Updated Input resistance typical from 200MΩ to 540GΩ	6
• Updated Output short-circuit current typical for 25°C to 75mA	6
• Updated Supply current typical for 25°C from 0.72mA to 0.56mA	6
• Updated Power supply rejection ratio range from 2.2V to 2.7V	6
• Added Input Bias Current vs Common-Mode Voltage V_S= ±20V, New Die plot	8
• Added Open-Loop Gain and Phase vs Frequency V_S= ±20V R_L= 10Ω, New Die plot	8
• Added Output Voltage Swing vs Output Current (Sinking) V_S= ±20V, New Die plot	8
• Added Output Voltage Swing vs Output Current (Sourcing) V_S= ±20V, New Die plot	8
• Added Input Voltage Noise Spectral Density vs Frequency V_S= ±20V, New Die plot	8
• Added Open-Loop Output Impedance vs Frequency V_S= ±20V, New Die plot	8
• Added *Old Versus New Die Comparison*	11
• Deleted *Detailed description* and *Application and Implementation* sections	11

Changes from Revision H (March 2013) to Revision I (April 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM7301IM5/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A04A
LM7301IM5/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A04A
LM7301IM5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	A04A
LM7301IM5X/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A04A
LM7301IM5X/NOPBG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A04A
LM7301IM5X/NOPBG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A04A
LM7301IMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM73 01IM
LM7301IMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM73 01IM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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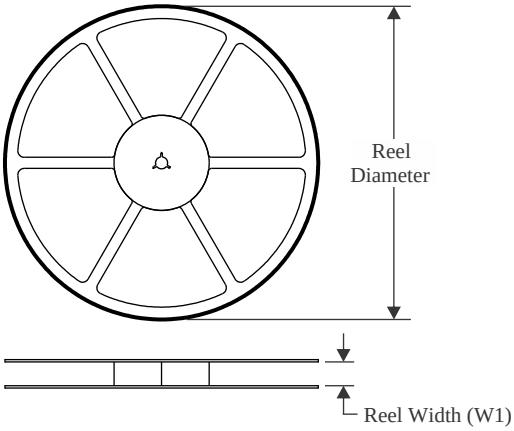
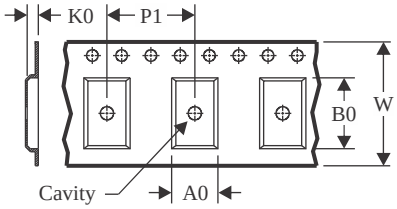
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

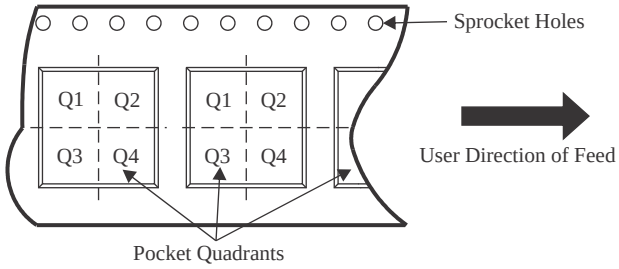


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

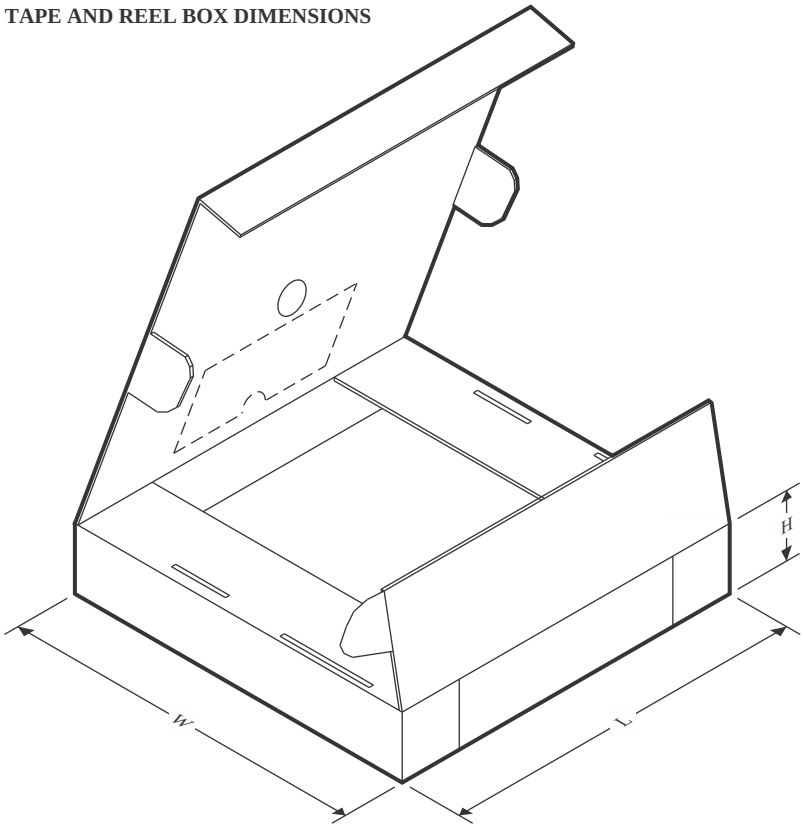
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7301IM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5X/NOPBG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

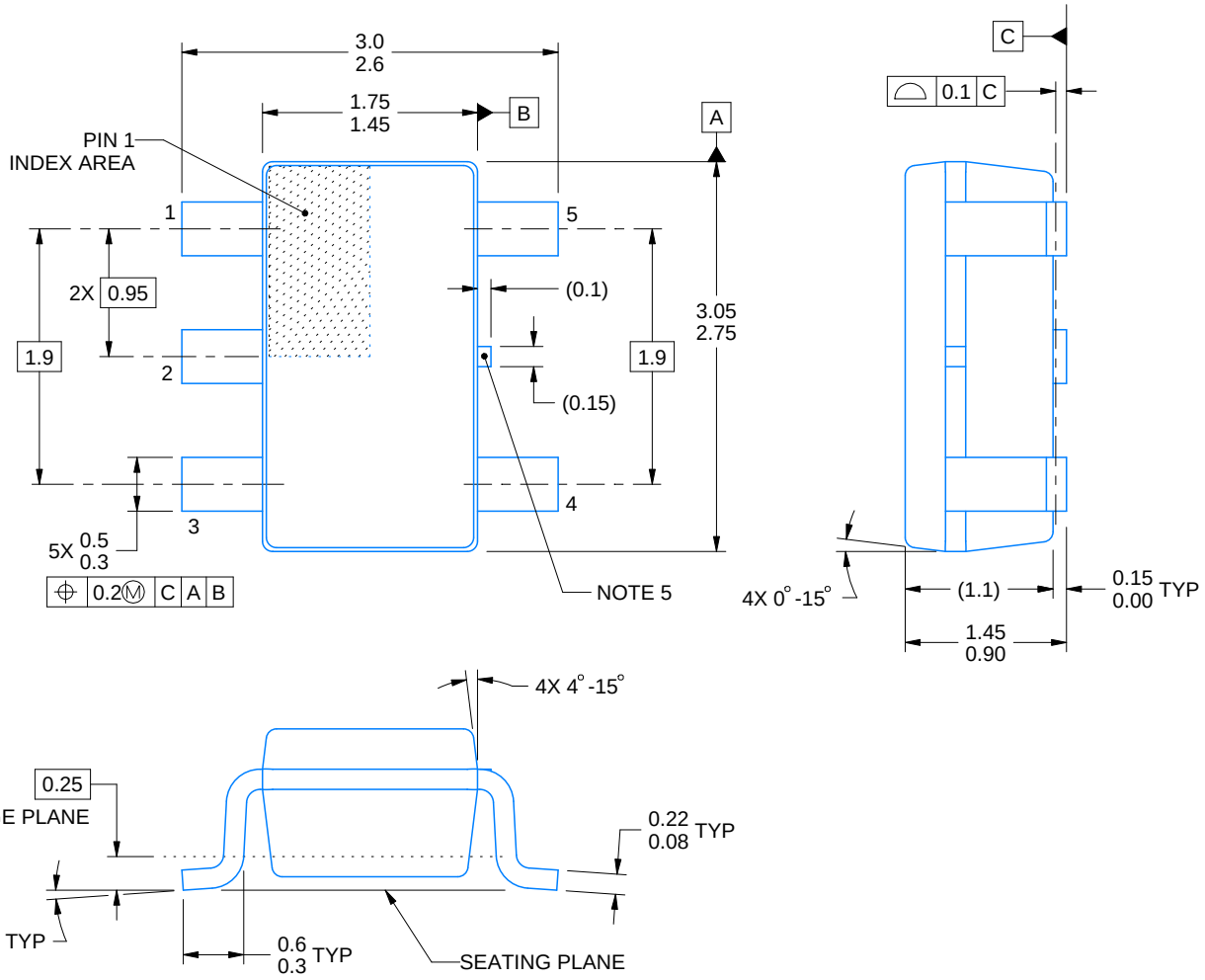
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7301IM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM7301IM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM7301IM5X/NOPBG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7301IMX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

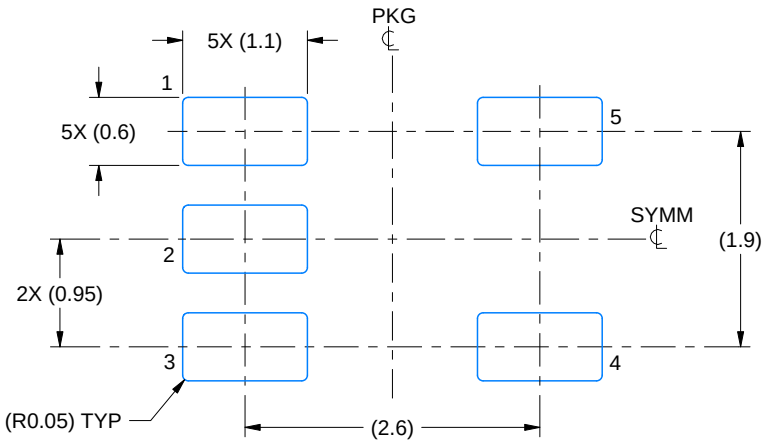
SMALL OUTLINE TRANSISTOR



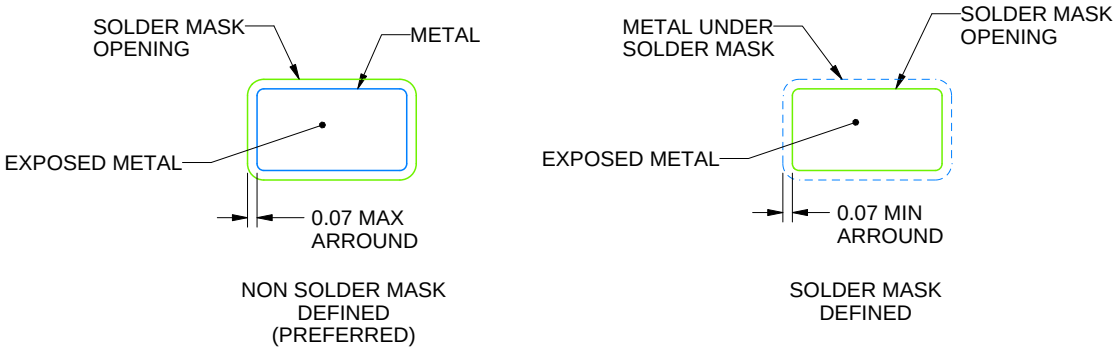
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

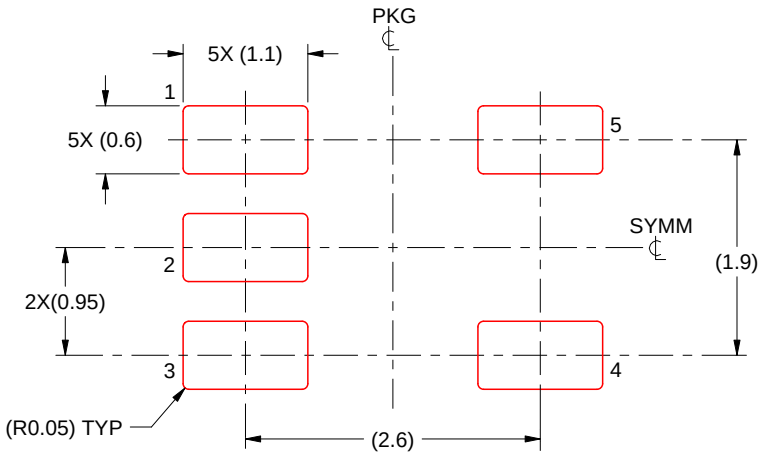


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

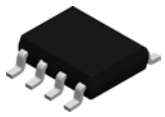


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

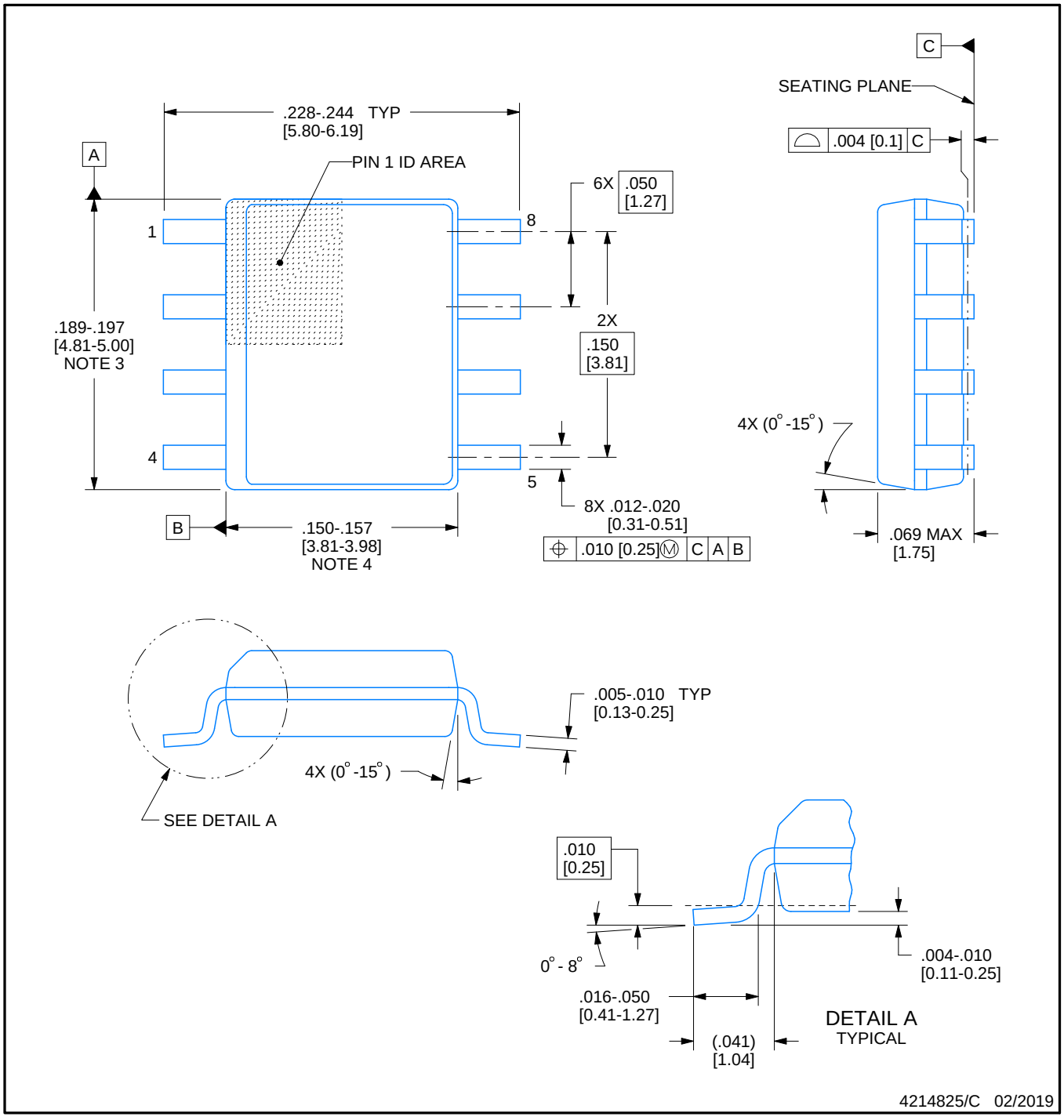


PACKAGE OUTLINE

D0008A

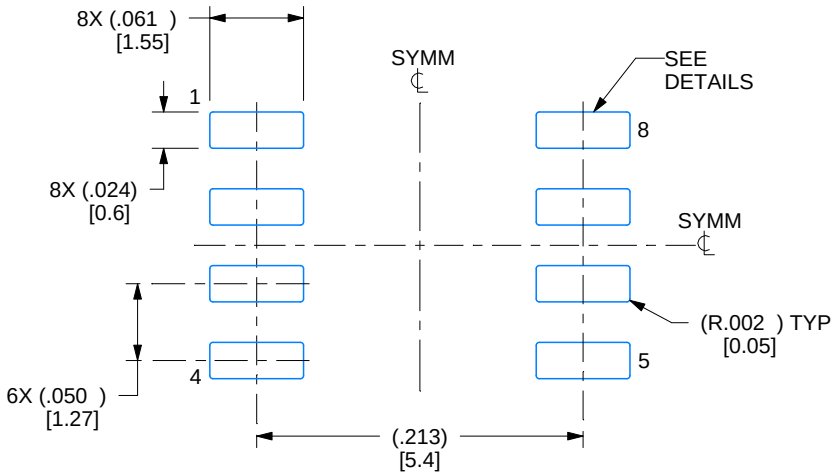
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

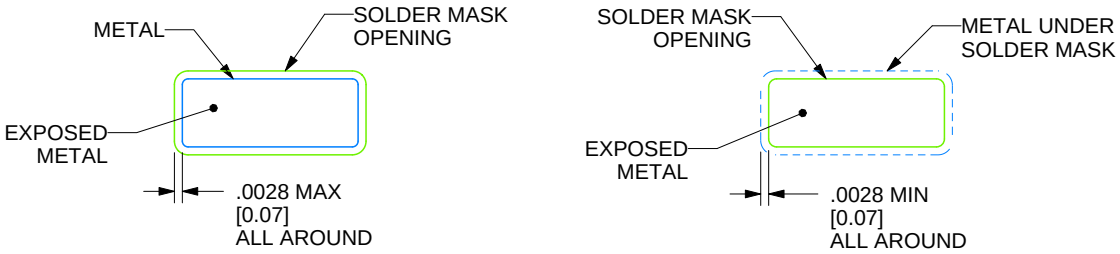


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

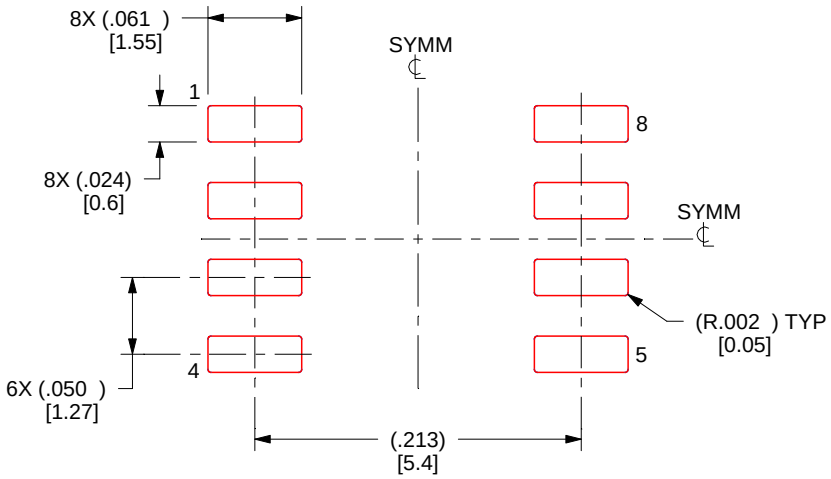
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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