LM95010 Digital Temperature Sensor with SensorPath® Bus

1 Features

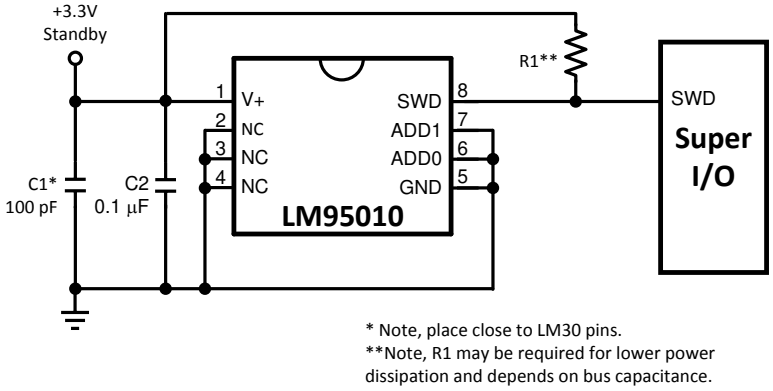
- SensorPath Bus
  - 4 Hardware Programmable Addresses
- Temperature Sensing
  - 0.25 °C Resolution
  - 127.75 °C Maximum Temperature Reading
- 8-Lead VSSOP Package
- Key Specifications:
  - Temperature Sensor Accuracy ±2°C (max)
  - Temperature Range −20 to +125°C
  - Power Supply Voltage +3.0 to +3.6 V
  - Power Supply Current 0.5 mA (typ)
  - Conversion Time 14 to 1456 ms

2 Applications

- Microprocessor Based Equipment
  - (Motherboards, Base-stations, Routers, ATMs, Point of Sale, …)
- Power Supplies

3 Description

The LM95010 is a digital output temperature sensor that has single-wire interface compatible with the SensorPath interface. It uses a ΔV_{be} analog temperature sensing technique that generates a differential voltage that is proportional to temperature. This voltage is digitized using a Sigma-Delta analog-to-digital converter. The LM95010 is part of a hardware monitor system, comprised of two parts: the PC System Health Controller (Master), such as a Super I/O, and up to seven slaves of which four can be LM95010s. Using SensorPath, the LM95010 will be controlled by the master and report to the master its own die temperature. SensorPath data is pulse width encoded, thereby allowing the LM95010 to be easily connected to many general purpose micro-controllers.



LM95010 connection to SensorPath master such as a Super I/O.

Table of Contents

4 Pin Configuration and Functions

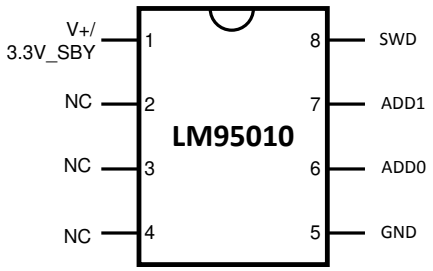


Figure 4-1. 8-Lead VSSOP See DGK Package

Table 4-1. Pin Descriptions

Pin Number	Pin Name	Type	Description	Typical Connection
1	V+/3.3V SB	Power	Positive power supply pin +3.3V pin.	Should be powered by +3.3V Standby power. This pin should be bypassed with a 0.1 µF capacitor. A bulk capacitance of approximately 10 µF needs to be in the near vicinity of the LM95010.
2-4	NC			Must be grounded.
5	GND	Power	Ground	System ground
6	ADD0	Input	Address select input that assigns the serial bus device number	10kΩ resistor to V+ or GND; must never be left floating
7	ADD1	Input	Address select input that assigns the serial bus device number	10kΩ resistor to V+ or GND; must never be left floating
8	SWD	Input/ Output	Single-wire Data, SensorPath serial interface line; Open-drain output	Super I/O with 1.25kΩ pull-up to 3.3V

5 Specifications

5.1 Absolute Maximum Ratings

See (1) (2)

Supply Voltage (V^+)		−0.5 V to 6.0 V
Voltage on Pin 2		−0.3 V to (V+ + 0.3 V)
Voltage on all other Pins		−0.5 V to 6.0 V
Input Current per Pin(3)		5 mA
Package Input Current (3)		30 mA
Package Power Dissipation		(4)
Output Sink Current		10 mA
Storage Temperature		−65 °C to +150 °C
ESD Susceptibility (5)	Human Body Model	2000 V
	Machine Model	200 V
Soldering Information, Lead Temperature		
VSSOP Package (6)	Vapor Phase (60 seconds)	215 °C
	Infrared (15 seconds)	220 °C

(1) All voltages are measured with respect to GND, unless otherwise noted.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V+), the current at that pin should be limited to 5 mA. Parasitic components and/or ESD protection circuitry are shown below for the LM95010's pins. The nominal breakdown voltage of D3 is 6.5 V. SNP stands for snap-back device. Devices that are connected to a particular pin are marked with a "✓" in Table 1.
(4) Thermal resistance junction-to-ambient when attached to a printed circuit board with 2 oz. foil is 210 °C/W.
(5) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin. See Figure 5-1 for the ESD Protection Input Structure.
(6) See the URL "http://www.ti.com/packaging/" for other recommendations and methods of soldering surface mount devices.

5.2 Operating Ratings

See (1) (2)

Temperature Range for Electrical Characteristics	$T_{MIN} \le T_A \le T_{MAX}$
LM95010CIMM	−20 °C ≤ T_A ≤ +125 °C
Operating Temperature Range	−20 °C ≤ T_A ≤ +125 °C
Supply Voltage Range (V+)	+3.0 V to +3.6 V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise noted.

5.3 DC Electrical Characteristics

The following specifications apply for V+ = 3.0 V_{DC} to 3.6 V_{DC}, unless otherwise specified in the conditions. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits T_A = +25 °C.

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Units (Limit)
POWER SUPPLY CHARACTERISTICS					
V+	Power Supply Voltage		3.3	**3.0** **3.6**	V (min) V (max)
$I+_{AVG}$	Average Power Supply Current	SensorPath Bus Inactive (3)	500	**750**	µA (max)
$I+_{Peak}$	Peak Power Supply Current	SensorPath Bus Inactive (3)	1.6		mA
	Power-On Reset Threshold Voltage			**1.6**	V (min)
				2.8	V (max)
TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS					
	Temperature Error	T_A = −20 °C and +125 °C (4)	±1	±3	°C (max)
		+25 °C ≤ T_A ≤ +60 °C (4)		±2	°C (max)
	Temperature Resolution		10		Bits
			0.25		°C
SWD and ADD DIGITAL INPUT CHARACTERISTICS					
V_{IH}	SWD Logical High Input Voltage			2.1	V (min)
				V+ + 0.5	V (max)
V_{IL}	SWD Logical Low Input Voltage			0.8	V (max)
		T_A = 0 °C to +85 °C		-0.5	V (min)
				-0.3	V (min)
V_{IH}	ADD Logical High Input Voltage			90% x V+	V (min)
V_{IL}	ADD Logical Low Input Voltage			10% x V+	V (max)
V_{HYST}	SWD Input Hysteresis		300		mV
I_L	SWD and ADD Input Leakage Current	GND ≤V_{IN} ≤ V+	±0.005	±10	µA (max)
	SWD Input Leakage Current with V+ Open or Grounded	GND ≤V_{IN} ≤ 3.6 V, and V+ Open or GND	±0.005		µA
C_{IN}	Digital Input Capacitance		10		pF
SWD DIGITAL OUTPUT CHARACTERISTICS					
V_{OL}	Open-drain Output Logic “Low” Voltage	I_{OL} = 4 mA		0.4	V (max)
		I_{OL} = 50 µA		0.2	V (max)
I_{OH}	Open-drain Output Off Current		±0.005	±10	µA (max)
C_{OUT}	Digital Output Capacitance		10		pF

(1) “Typicals” are at T_A = 25 °C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.
(2) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(3) The supply current will not increase substantially with SensorPath transactions.
(4) Temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM95010 and the thermal resistance. See Note 4 in Absolute Maximum Ratings table for thermal resistance to be used in the self-heating calculation.

5.4 AC Electrical Characteristics

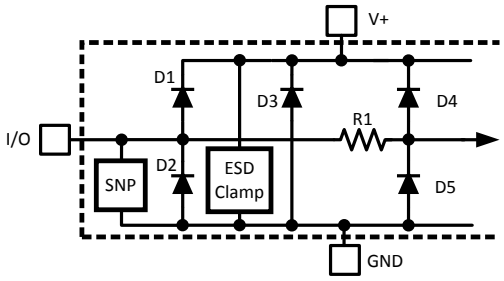
The following specification apply for V+ = +3.0V_{DC} to +3.6V_{DC}, unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25 °C. The SensorPath Characteristics conform to the SensorPath specification. Please refer to that specification for further details.

HARDWARE MONITOR CHARACTERISTICS					
Symbol	**Parameter**	**Conditions**	**Typical (1)**	**Limits (2)**	**Units (Limits)**
t_{CONV}	Total Monitoring Cycle Time (3)	Default	182	163.8	ms (min)
				200.2	ms (max)
SensorPath Bus CHARACTERISTICS					
t_f	SWD fall time (4)	$R_{pull-up}$= 1.25 kΩ ±30%, C_L= 400 pF		**300**	ns (max)
t_r	SWD rise time (5)	$R_{pull-up}$= 1.25 kΩ±30%, C_L= 400 pF		**1000**	ns (max)
t_{INACT}	Minimum inactive time (bus at high level) ensured by the LM95010 before an Attention Request			**11**	µs (min)
t_{Mtr0}	Master drive for Data Bit 0 write and for Data Bit 0-1 read			**11.8**	µs (min)
				17.0	µs (max)
t_{Mtr1}	Master drive for Data Bit 1 write			**35.4**	µs (min)
				48.9	µs (max)
t_{SFEdet}	Time allowed for LM95010 activity detection			**9.6**	µs (max)
t_{SLout1}	LM95010 drive for Data Bit 1 read by master			**28.3**	µs (min)
				38.3	µs (max)
t_{MtrS}	Master drive for Start Bit			**80**	µs (min)
				109	µs (max)
t_{SLoutA}	LM95010 drive for Attention Request			**165**	µs (min)
				228	µs (max)
t_{RST}	Master or LM95010 drive for Reset			**354**	µs (min)
t_{RST_MAX}	Maximum drive of SWD by an LM95010, after the power supply is raised above 3V			**500**	ms (max)

(1) "Typicals" are at T_A = 25 °C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.
(2) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(3) This specification is provided only to indicate how often temperature data is updated once enabled.
(4) The output fall time is measured from $V_{IH\ min}$ to $V_{IL\ max}$. The output fall time is ensured by design.
(5) The output rise time is measured from $V_{IL\ max}$ to $V_{IH\ min}$. The output rise time is ensured by design.

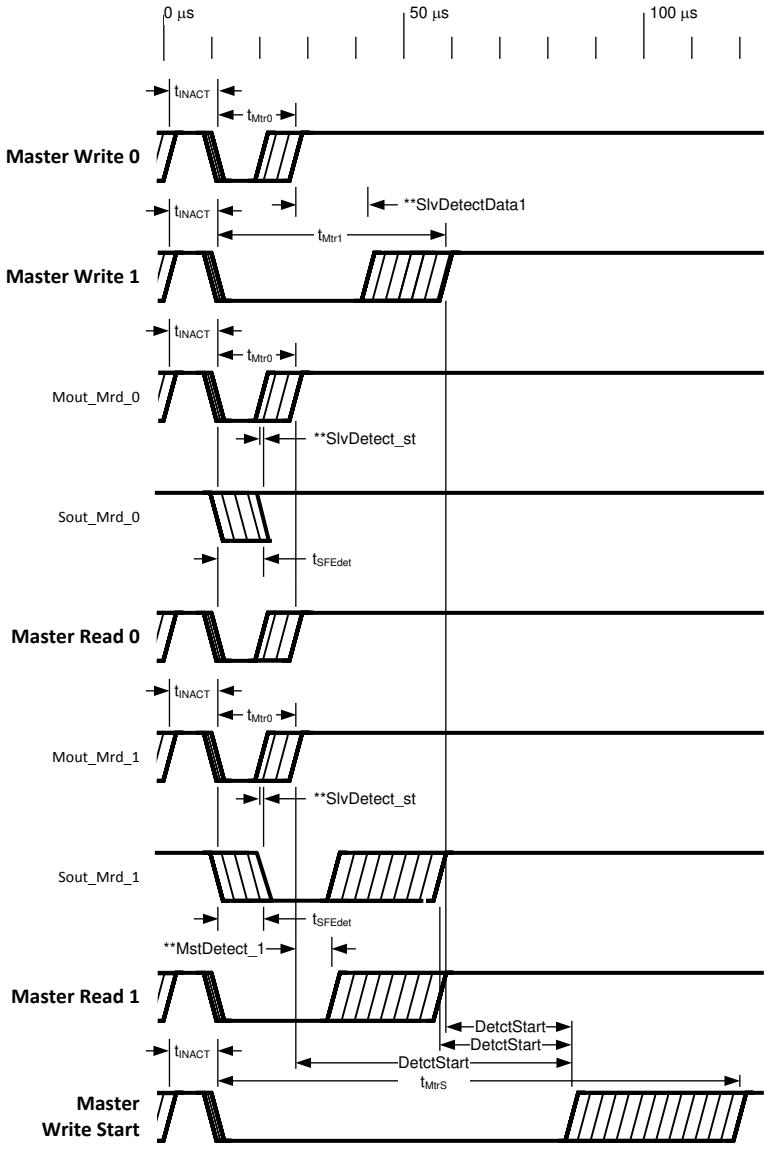
Table 1

Pin Name	PIN #	D1	D2	D3	D4	D5	R1	SNP	ESD CLAMP
V+/3.3V SB	1			✓					✓
NC	2	✓	✓	✓	✓	✓	✓		✓
NC	3								
NC	4		✓	✓		✓	✓	✓	
ADD0	6		✓	✓		✓	✓	✓	
ADD1	7		✓	✓				✓	
SWD	8		✓	✓		✓	✓	✓	



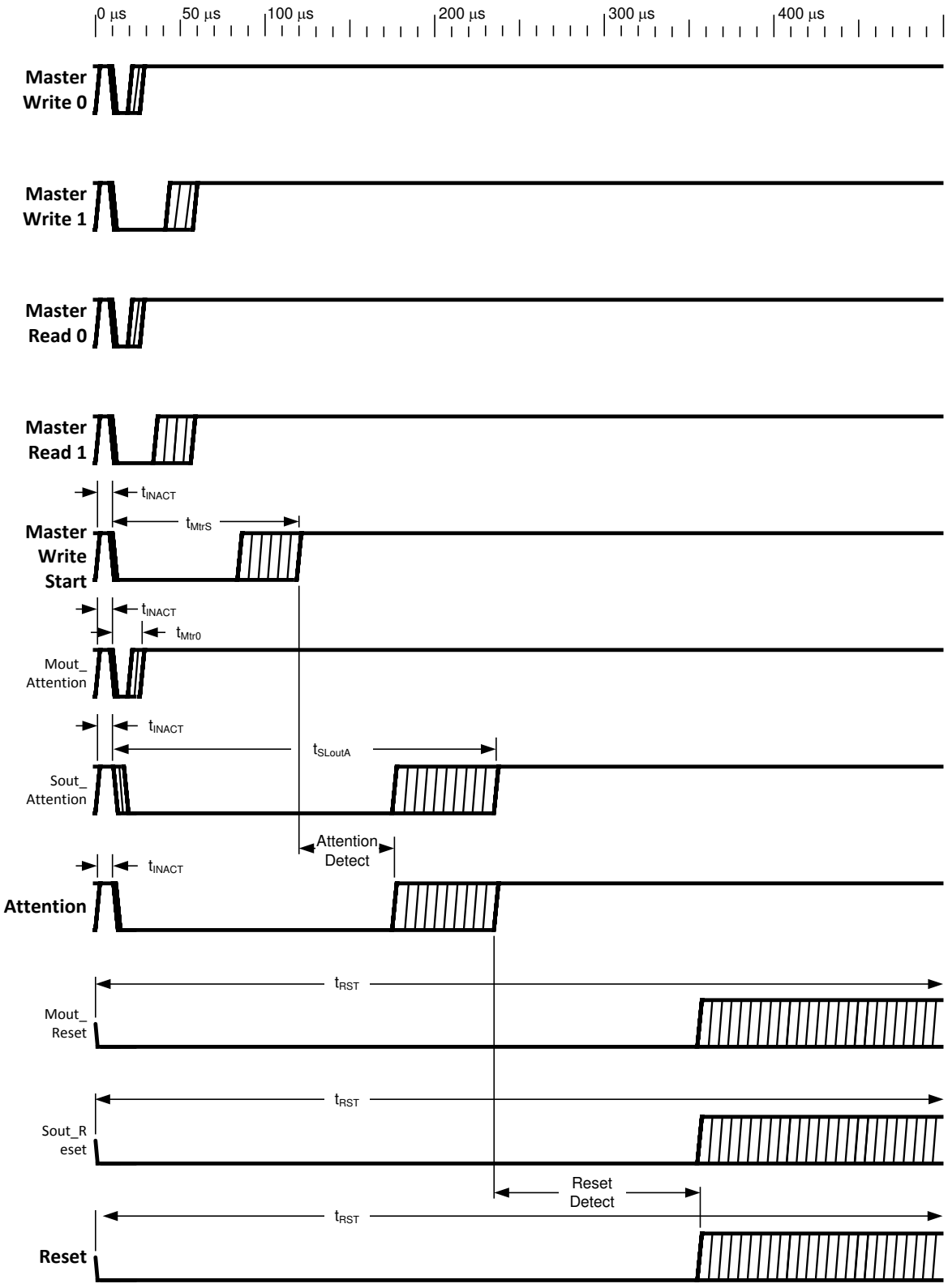
Devices that are connected to a particular pin are marked with a "✓" in the table above.

Figure 5-1. ESD Protection Input Structure



See Section 6.3.2 for further details.

Figure 5-2. Timing for Data Bits 0, 1 and Start Bit



See Section 6.3.2 for further details.

Figure 5-3. Timing for Attention Request and Reset

5.5 Typical Performance Characteristics

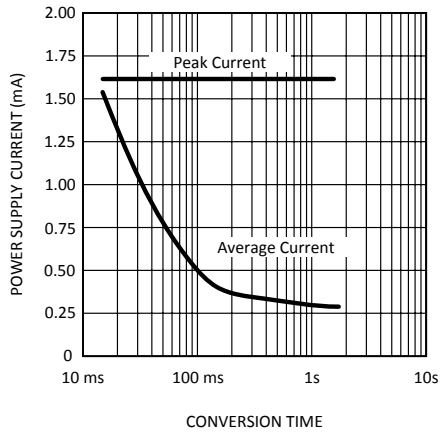


Figure 5-4. Conversion Rate Effect on Power Supply Current

6 Detailed Description

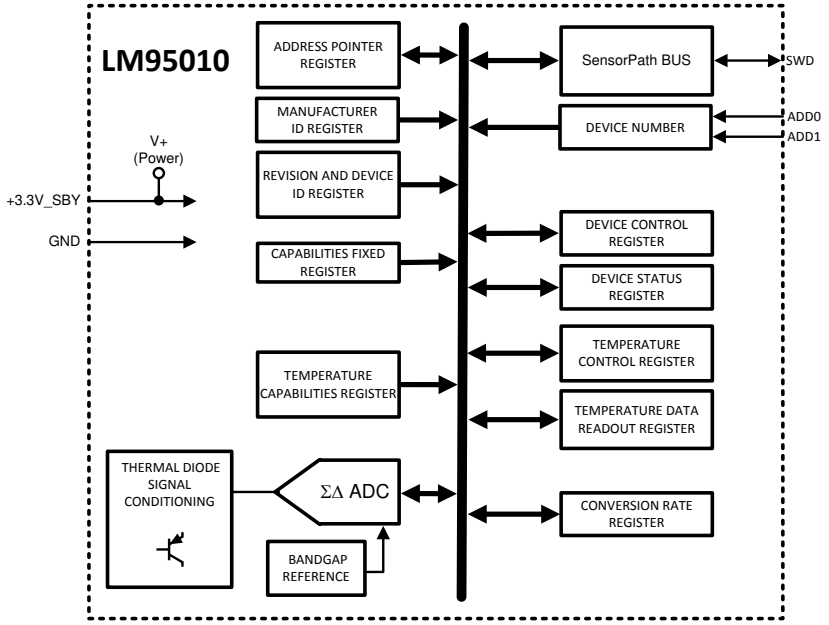
6.1 Overview

The LM95010 is based on a ΔV_{be} temperature sensing method. A differential voltage, representing temperature, is digitized using a Sigma-Delta analog to digital converter. The digital temperature data can be retrieved over a simple single-wire interface called SensorPath. SensorPath is optimized for hardware monitoring. TI offers a royalty-free license in connection with its intellectual property rights in the SensorPath bus.

The LM95010 has 2 address pins that allow up to 4 LM95010s to be connected to one SensorPath bus. The physical interface of SensorPath's SWD signal is identical to the familiar industry standard SMBus SMBDAT signal. The digital information is encoded in the pulse width of the signal being transmitted. Every bit can be synchronized by the master simplifying the implementation of the master when implemented with a microcontroller. For microcontroller's with greater functionality an asynchronous attention signal can be transmitted by the LM95010 to interrupt the microcontroller and notify it that temperature data has been updated in the readout register.

To optimize the LM95010's power consumption to the system requirements, the LM95010 has a shutdown mode as well as it supports multiple conversion rates.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 SensorPath BUS SWD

SWD is the Single Wire Data line used for communication. SensorPath uses 3.3V single-ended signaling, with a pull-up resistor and open-drain low-side drive (see Figure 6-1). For timing purposes SensorPath is designed for capacitive loads (C_L) of up to 400pF. Note that in many cases a 3.3V standby rail of the PC will be used as a power supply for both the sensor and the master. Logic high and low voltage levels for SWD are TTL compatible. The master may provide an internal pull-up resistor. In this case the external resistor is not needed. The minimum value of the pull-up resistor must take into account the maximum allowable output load current of 4mA.

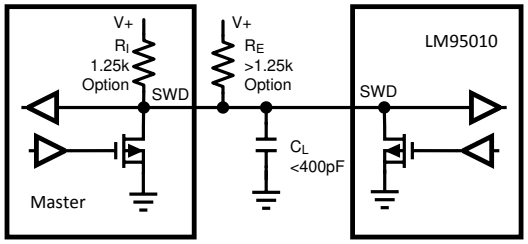


Figure 6-1. SensorPath SWD simplified schematic

6.3.2 SensorPath BIT SIGNALING

Signals are transmitted over SensorPath using pulse-width encoding. There are five types of "bit signals":

- Data Bit 0
- Data Bit 1
- Start Bit
- Attention Request
- Reset

All the "bit signals" involve driving the bus to a low level. The duration of the low level differentiates between the different "bit-signals". Each "bit signal" has a fixed pulse width. SensorPath supports a Bus Reset Operation and Clock Training sequence that allows the slave device to synchronize its internal clock rate to the master. Since the LM95010 meets the ±15% timing requirements of SensorPath, the LM95010 does not require the Clock Training sequence and does support this feature. This section defines the "bit signal" behavior in all the modes. Please refer to the timing diagrams in Electrical Characteristics (Figure 5-2 and Figure 5-3) while going through this section. Note that the timing diagrams for the different types of "bit signals" are shown together to better highlight the timing relationships between them. However, the different types of "bit signals" appear on SWD at different points in time. These timing diagrams show the signals as driven by the master and the LM95010 slave as well as the signal as seen when probing SWD. Signals labels that begin with the label Mout_ depict a drive by the master. Signals labels that begin with the label Slv_ depict the drive by the LM95010. All other signals show what would be seen when probing SWD for a particular function (e.g. "Master Wr 0" is the Master transmitting a Data Bit with the value of 0).

6.3.3 Bus Inactive

The bus is inactive when the SWD signal is high for a period of at least t_{INACT}. The bus is inactive between each "bit signal".

6.3.4 Data Bit 0 and 1

All Data Bit signal transfers are started by the master. A Data Bit 0 is indicated by a "short" pulse; a Data Bit 1 is indicated by a longer pulse. The direction of the bit is relative to the master, as follows:

- Data Write - a Data Bit transferred from the master to the LM95010.
- Data Read - a Data Bit transferred from the LM95010 to the master.

A master must monitor the bus as inactive before starting a Data Bit (read or Write).

A master initiates a data write by driving the bus active (low level) for the period that matches the data value (t_{Mtr0} or t_{Mtr1} for a write of "0" or "1", respectively). The LM95010 will detect that the SWD becomes active within a period of t_{SFEdet}, and will start measuring the duration of that the SWD is active in order to detect the data value.

A master initiates a data read by driving the bus for a period of t_{Mtr0}. The LM95010 will detect that the SWD have become active within a period of t_{SFEdet}. For a data read of "0", the LM95010 will not drive the SWD. For a data read of "1" the LM95010 will start within t_{SFEdet} to drive the SWD low for a period of t_{SLout1}. Both master and LM95010 must monitor the time at which the bus becomes inactive to identify a data read of "0" or "1".

During each Data Bit, both the master and all the LM95010s must monitor the bus (the master for Attention Request and Reset; at the LM95010s for Start Bit, Attention Request and Reset) by measuring the time SWD is active (low). If a Start Bit, Attention Requests or Reset "bit signal" is detected, the current "bit signal" is not treated as a Data Bit.

Note that the bit rate of the protocol varies depending on the data transferred. Thus, the LM95010 has a value of "0" in reserved or unused register bits for bus bandwidth efficiency.

6.3.5 Start Bit

A master must monitor the bus as inactive before beginning a Start Bit.

The master uses a Start Bit to indicate the beginning of a transfer. LM95010s will monitor for Start Bits all the time, to allow synchronization of transactions with the master. If a Start Bit occurs in the middle of a transaction, the LM95010 being addressed will abort the current transaction. In this case the transaction is not "completed" by the LM95010 (see Section 6.3.8).

During each Start Bit, both the master and all the LM95010s must monitor the bus for Attention Request and Reset, by measuring the time SWD is active (low). If an Attention Request or Reset condition is detected, the current "bit signal" is not treated as a Start Bit. The master may attempt to send the Start Bit at a later time.

6.3.6 Attention Request

The LM95010 may initiate an Attention Request when the SensorPath bus is inactive.

Note that a Data Bit, or Start Bit, from the master may start simultaneously with an Attention Request from the LM95010. In addition, two LM95010s may start an Attention Request simultaneously. Due to its length, the Attention Request has priority over any other "bit signal", except Reset. Conflict with Data Bits and Start Bits are detected by all the devices, to allow the bits to be ignored and re-issued by their originator.

The LM95010 will either check to see that the bus is inactive before starting an Attention Request, or start the Attention Request with the t_{SFEdet} time interval after SWD becomes active. The LM95010 will drive the signal low for t_{SLoutA} time. After this, both the master and the LM95010 must monitor the bus for a Reset Condition. If a Reset condition is detected, the current "bit signal" is not treated as an Attention Request.

After Reset, an Attention Request can not be sent before the master has sent 14 Data Bits on the bus. See Section 6.3.13 for further details on Attention Request generation.

6.3.7 Bus Reset

The LM95010 issues a Reset at power up. The master must also generate a Bus Reset at power-up for at least the minimum reset time, it must not rely on the LM95010. SensorPath puts no limitation on the maximum reset time of the master. Following a Bus Reset, the LM95010 may generate an Attention Request only after the master has sent 14 Data Bits on the bus. See Section 6.3.13 for further details on Attention Request generation.

6.3.8 SensorPath BUS TRANSACTIONS

SensorPath is designed to work with a single master and up to seven slave devices. Each slave has a unique address. The LM95010's supports up to 4 device addresses that are selected by the state of the address pins ADD0 and ADD1. The Register Set of the LM95010 is defined in Section 7.

6.3.9 Bus Reset Operation

A Bus Reset Operation is global on the bus and affects only the communication interface of all the devices connected to it. The Bus Reset operation does not affect either the contents of the device registers, or device operation, to the extent defined in LM95010 Register Set, see Section 7.

The Bus Reset operation is performed by generating a Reset signal on the bus. The master must apply Reset after power-up, and before it starts operation. The Reset signal end will be monitored by all the LM95010s on the bus.

After the Reset Signal Section 6.3.2 requires that the master send a sequence of 8 Data Bits with a value of "0", without a preceding Start Bit. This is required to enable slaves that "train" their clocks to the bit timing. The LM95010 does not require nor does it support clock training.

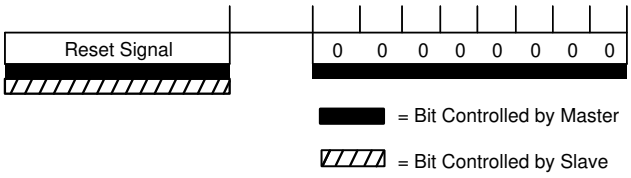


Figure 6-2. Bus Reset Transaction

6.3.10 Read Transaction

During a read transaction, the master reads data from a register at a specified address within a slave. A read transaction begins with a Start Bit and ends with an ACK bit, as shown in Figure 6-3.

- **Device Number** This is the address of the LM95010 device accessed. Address "000" is a broadcast address and can be responded to by all the slave devices. The LM95010 ignores the broadcast address during a read transaction.
- **Internal Address** The address of a register within the LM95010 that is read.
- **Read/ $\overline{\text{Write}}$ (R/ $\overline{\text{W}}$)** A "1" indicates a read transaction.
- **Data Bits** During a read transaction the data bits are driven by the LM95010. Data is transferred serially with the most significant bit first. This allows throughput optimization based on the information that needs to be read.
  - The LM95010 supports 8-bit or 16-bit data fields, as described in Section 7.
- **Even Parity (EP)** This bit is based on all preceding bits (device number, internal address, read/ $\overline{\text{write}}$ and data bits) and the parity bit itself. The parity -number of 1's - of all the preceding bits and the parity bit must be even - i.e., the result must be 0. During a read transaction, the EP bit is sent by the LM95010 to the master to allow the master to check the received data before using it.
- **Acknowledge (ACK)** During a read transaction the ACK bit is sent by the master indicating that the EP bit was received and was found to be correct, when compared to the data preceding it, and that no conflict was detected on the bus (excluding Attention Request - Section 6.3.13). A read transfer is considered "complete" only when the ACK bit is received. A transaction that was not positively acknowledged is not considered "complete" by the LM95010 and following are performed:
  - The BER bit in the LM95010 Device Status register is set
  - The LM95010 generates an Attention Request before, or together with the Start Bit of the next transaction

  A transaction that was not positively acknowledged is also not considered "complete" by the master (i.e. internal operations related to the transaction are not performed). The transaction may be repeated by the master, after detecting the source of the Attention Request (the LM95010 that has a set BER bit in the Device Status register). Note that the SensorPath protocol neither forces, nor automates re-execution of the transaction by the master.The values of the ACK bit are:
  - 1: Data was received correctly
  - 0: An error was detected (no-acknowledge).

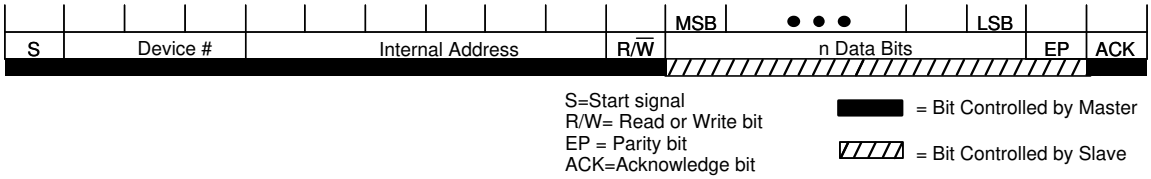


Figure 6-3. Read Transaction, master reads data from LM95010

6.3.11 Write Transaction

In a write transaction, the master writes data to a register at a specified address in the LM95010. A write transaction begins with a Start Bit and ends with an ACK Data Bit, as show in Figure 6-4.

- **Device Number** This is the address of the slave device accessed. Address "000" is a broadcast address and is responded to by all the slave devices. The LM95010 responds to broadcast messages to the Device Control Register.
- **Internal Address** This is the register address in the LM95010 that will be written.
- **Read/ $\overline{\text{Write}}$ (R/ $\overline{\text{W}}$)** A "0" data bit directs a write transaction.
- **Data Bits** This is the data written to the LM95010 register, are driven by the master. Data is transferred serially with the most significant bit first. The number of data bits may vary from one address to another, based on the size of the register in the LM95010. This allows throughput optimization based on the information that needs to be written.
  - The LM95010 supports 8-bit or 16-bit data fields, as described in Section 7.

- **Even Parity (EP)** This data bit is based on all preceding bits (Device Number, Internal Address, Read/ $\overline{\text{Write}}$ and Data bits) and the Even Parity bit itself. The parity (number of 1's) of all the preceding bits and the parity bit must be even - i.e. the result must be 0. During a write transaction, the EP bit is sent by the master to the LM95010 to allow the LM95010 to check the received data before using it.
- **Acknowledge (ACK)** During the write transaction the ACK bit is sent by the LM95010 indicating to the master that the EP was received and was found correct, and that no conflict was detected on the bus (excluding Attention Request - see Section 6.3.13). A write transfer is considered "completed" only when the ACK bit is generated. A transaction that was not positively acknowledged is not considered complete by the LM95010 (i.e. internal operation related to the transaction are not performed) and the following are performed:
  - The BER bit in the LM95010 Device Status register is set;
  - The LM95010 generates an Attention Request before, or together with the Start Bit of the next transaction

  A transaction that was not positively acknowledged is also not considered "complete" by the master (i.e. internal operations related to the transaction are not performed). The transaction may be repeated by the master, after detecting the source of the Attention Request (the LM95010 that has a set BER bit in the Device Status register). Note that the SensorPath protocol neither forces, nor automates re-execution of the transaction by the master.The values of the ACK bit are:
  - 1: Data was received correctly;
  - 0: An error was detected (no-acknowledge).

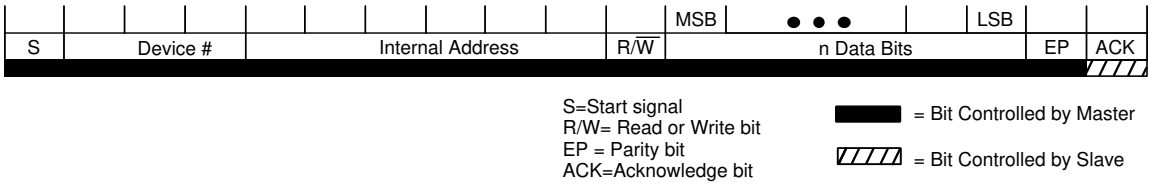


Figure 6-4. Write Transaction, master write data to LM95010

6.3.12 Read and Write Transaction Exceptions

This section describes master and LM95010 handling of special bus conditions, encountered during either Read or Write transactions.

If an LM95010 receives a Start Bit in the middle of a transaction, it aborts the current transaction (the LM95010 does not "complete" the current transaction) and begins a new transaction. Although not recommend for SensorPath normal operation, this situation is legitimate, therefore it is not flagged as an error by the LM95010 and Attention Request is not generated in response to it. The master generating the Start Bit, is responsible for handling the not "complete" transaction at a "higher level".

If LM95010 receives more than the expected number of data bits (defined by the size of the accessed register), it ignores the unnecessary bits. In this case, if both master and LM95010 identify correct EP and ACK bits they "complete" the transaction. However, in most cases, the additional data bits differ from the correct EP and ACK bits. In this case, both the master and the LM95010 do not "complete" the transaction. In addition, the LM95010 performs the following:

- the BER bit in the LM95010 Device Status register is set
- the LM95010 generates an Attention Request

If the LM95010 receives less than the expected number of data bits (defined by the size of the accessed register), it waits indefinitely for the missing bits to be sent by the master. If then the master sends the missing bits, together with the correct EP/ACK bits, both master and LM95010 "complete" the transaction. However, if the master starts a new transaction generating a Start Bit, the LM95010 aborts the current transaction (the LM95010 does not "complete" the current transaction) and begins the new transaction. The master is not notified by the LM95010 of the incomplete transaction.

6.3.13 Attention Request Transaction

Attention Request is generated by the LM95010 when it needs the attention of the master. The master and all LM95010s must monitor the Attention Request to allow bit re-sending in case of simultaneous start with a Data Bit or Start Bit transfer. Refer to Section 6.3.6 of the data sheet.

The LM95010 will generate an Attention Request using the following rules:

1. A Function event that sets the Status Flag has occurred and Attention Request is enabled **and**
2. The "physical" condition for an Attention Request is met (i.e., the bus is inactive), **and**
3. At the first time 2 is met after 1 occurred, there has not been an Attention request on the bus since a read of the Device Status register, **or** since a Bus Reset.

OR

1. A bus error event occurred, **and**
2. the "physical" condition for an Attention Request is met (i.e., the bus is inactive), **and**
3. At the first time 2. is met after 1 occurred, there has not been a Bus Reset.

All devices (master or slave) must monitor the bus for an Attention Request signal. The following notes clarify the intended system operation that uses the Attention Request Indication.

- Masters are expected to use the attention request as a trigger to read results from the LM95010. This is done in a sequence that covers all LM95010s. This sequence is referred to as "master sensor read sequence".
- After an Attention Request is sent by an LM95010 until after the next read from the Device Status register the LM95010 does not send Attention Requests for a function event since it is ensured that the master will read the Status register as part of the master sensor read sequence. Note that the LM95010 will send an attention for BER, regardless of the Status register read, to help the master with any error recovery operations and prevent deadlocks.
- A master must record the Attention Request event. It must then scan all slave devices in the system by reading their Device Status register and must handle any pending event in them before it may assume that there are no more events to handle.

Note

There is no indication of which slave has sent the request. The requirement that multiple requests are not sent allows the master to know within one scan of register reads that there are no more pending events.

7 Register Set

7.1 Fixed Number Setting

The LM95010 device number is defined by strapping of the ADD0 and ADD1 pins. The LM95010 will wake (after Device Reset) with the Device Number field of the Device Number register set to the address as designated in Section 7.4. It is the responsibility of the system designer to avoid having two devices with the same Device Number on the bus.

Devices should be detected by the master by a read operation of the Device Number register. The read returns "000" if there is no device at that address on the bus (the EP bit must be ignored).

7.2 Register Set Summary

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
000 000	Device Number	R	*	Not Available								Reserved					See Table 7-1		
												0	0	0	0	0			
000 001	Manufacturer ID	R	100Bh	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1
000 010	Device ID	R	21h	RevID					Device ID										
				0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
000 011	Capabilities Fixed	R	1h	Reserved												Function 1			
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
000 100	Device Status	R	0h	Not Available								BER	0	0	ERF 1	0	0	0	SF1
000 101	Device Control	R/W	0h	Reserved											EnF 1	Res	Low Pwr	Shut down	Reset
				0	0	0	0	0	0	0	0	0	0	0		0			
001 000	Temperature Capabilities	R	014Ah	Reserved							Int Sens	Rout Size	Sign	10Bits			0.25°C Resolution		
				0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	0
001 001	Temperature Data Readout	R		MSb Sign	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5 °C	LSb 0.25 °C	Reserved					
														0	0	0	0	0	0
001 010	Temperature Control	R/W	0h	Reserved														EN0	ATE
				0	0	0	0	0	0	0	0	0	0	0	0	0	0		
001 011 -011 111	Reserved	R		Undefined															
100 000	Conversion Rate	R/W	2h	Not Available								0	0	0	0	0	0	Conversion Rate	
100 001 - 111 111	Undefined Registers	R		Undefined															

* Depends on state of ADD pins see Table 7-1.

7.3 Device Reset Operation

A Device Reset operation is performed in the following conditions:

- At device power-up.
- When the Reset bit in the Device Control register is set to 1 (see Section 7.9).

The Device Reset operation performs the following:

- Aborts any device operation in progress and restarts device operation.
- Sets all device registers to their "Reset" (default) value.

7.4 Device Number (Addr 00o)

This register is used to specify a unique address for each device on the bus.

Reg Add	Register Name	R/W	POR Val	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
000 000	Device Number	R	4h-1h	Reserved					AS2	AS1	AS0
				0	0	0	0	0			

The value of AS2:AS0 is determined by the setting of the ADD0 and ADD1 input pins:

Table 7-1. Device Number Assignment

[ADD1:ADD0]	[AS2:AS0]
00	001
01	010
10	011
11	100

The value of AS2:AS0 will directly change and follow the value determined by ADD1:ADD0. Since this is a read only register the value of the address cannot be changed by software.

7.5 Manufacturer ID (Addr 01o)

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
000 001	Manufacturer ID	R	100Bh	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1

The manufacturer ID matches that assigned by the PCI SIG. This register may be used to identify the manufacturer of the device in order to perform manufacturer specific operations.

7.6 Device ID (Addr 02o)

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
000 010	Device ID	R	21h	RevID					DeviceID										
				0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

The device ID is defined by the manufacturer of the device and is unique for each device produced by a manufacturer. Bits 15-11 identify the revision number of die and will be incremented upon revision of the device.

Bit	Type	Description
10-0	RO	**DeviceID (Device ID Value)** A fixed value that identifies the device.
15-11	RO	**RevID (Revision ID Value)** A fixed value that identifies the device revision.

7.7 Capabilities Fixed (Addr 03o)

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
000 011	Capabilities Fixed	R	1h	Reserved												FuncDescriptor1			
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The value of this register defines the capabilities of the LM95010. The LM95010 supports only one function, that of Temperature Measurement type. Please refer to Section 6.3.2 for further details on other FuncDescriptor values.

7.8 Device Status (Addr 04o)

This register is set to the reset value by a Device Reset.

Reg Add	Register Name	R/W	POR Val	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
000 100	Device Status	R	0h	BER	0	0	ERF1	0	0	0	SF1

Bit	Type	Description
0	RO	**SF1 (Status Function 1).** This bit is set by a Function Event within Function 1. Event details are function dependent and are described within the function. SF1 is cleared by Device Reset or by handling the event within the function (seeSection 7.10 for further details). 0: Status flag for Function 1 is inactive (no event). 1: Status flag for Function 1 is active indicating that a Function Event has occurred.
3-1	RO	**Not supported.** Will always read "0".
4	RO	**ERF1 (Error Function 1)** This bit is set in response to an error indication within Function 1. ERF1 is cleared by Device Reset or by handling the error condition within the function (see Section 7.10 for further details). 0: No error occurred in Function 1. 1: Error occurred in Function 1.
6-5	RO	**Not supported.** Will always read "0".
7	RO	**BER (Bus Error).** This bit is set when the device either generates, or receives an error indication in the ACK bit of the transaction (i.e., no-acknowledge). BER is cleared by Device Reset or by reading the Device Status register. 0: No transaction error occurred. 1: An ACK bit error (no-acknowledge) occurred during the last transaction.

7.9 Device Control (Addr 05o)

This register responds to a broadcast write command (DeviceNumber 000). Write using broadcast address is ignored by bits 15-2. This register is set to the reset value by a Device Reset.

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
000 101	Device Control	R/W	0h	Reserved											EnF1	Res	Low Pwr	Shutdown	Reset
				0	0	0	0	0	0	0	0	0	0	0					

Bit	Type	Description
0	R/W	**Reset (Device Reset).** When set to "1" this bit initiates a Device Reset operation (See Section 7.3). This bit self-clears after the Device Reset operation is completed. 0: Normal device operation. (default) 1: Device Reset The LM95010 does not require a Device Reset command after power.
1	R/W	**Shutdown (Shutdown Mode).** When set to "1" this bit stops the operation of all functions and places the device in the lowest power consumption mode. 0: Device in Active Mode. (default) 1: Device in Shutdown Mode.
2	R/W	**LowPwr (Low-Power Mode).** When set to "1" this bit slows the operation of all functions and places the device in a low power consumption mode. In Low-Power Mode, the conversion rate of the LM95010 is effected see Section 7.15 for further details. 0: Device in Active Mode. (default) 1: Device in Low-Power Mode.
3	RO	**Not supported.** Will always read "0".
4	R/W	**EnF1 (Enable Function 1).** When bit is set to "1" this bit Function 1 is enabled for operation. A function may require setup before this bit is set. The function registers can be accessed even when the function is disabled. 0: Function 1 is disabled. (default) 1: Function is enabled.
15-5	RO	**Not supported.** Will always read "0".

7.10 Temperature Measurement Function (TYPE - 0001)

This section defines the register structure and operation of a Temperature Measurement function as it applies to the LM95010. The FuncDescriptor value of this function is ‘0001’.

7.11 Operation

The Temperature Measurement function as implemented in the LM95010 supports one temperature zone, the LM95010's internal temperature (LM95010's junction temperature). Since the LM95010 only supports one temperature measurement the Sensor Scan function as defined in Section 6.3.2 only applies to one temperature sensor. A temperature scan is enabled by the SensorEnable bit (EN0). The minimum scan rate is recommended to be 4Hz (i.e. the measurement data is updated at least once in 250 ms), see Section 7.15 for further details. In Low-Power Mode, the scan rate is four time lower than the scan rate in Active Mode. The scan rate effects the bus bandwidth required to read the results. The sampling rate of the temperature measurements can also be controlled via the Conversion Rate register, see Section 7.15 for further details.

Data Readout When a new result is stored in the Readout register a Function Event is generated. Reading the Readout register clears the Status Function 1 flag (SF1). The result is available in the Readout register waiting for the master to read it during the master sensor read sequence. If a new result is ready before the previous result has been read, the new result overwrites the previous result and the Error Function 1 flag (ERF1) is set (indicating an overrun event). Reading the Readout register clears also the Error Function 1 flag (ERF1). The Readout register contains the temperature data, and the sensor number. Since the LM95010 only supports one temperature zone the sensor number field will always report zero. Other fields in the Readout register as defined by the Section 6.3.2 are not supported.

Readout Resolution The resolution of the readout is defined in the Temperature Capabilities register. The resolution of the LM95010 is fixed and cannot be modified by software.

Function Event The Temperature Measurement function generates a Function Event whenever a temperature conversion cycle is completed and new data is stored in the Readout Register. When the new data is stored into the Readout register the SF1 bit in the device Status register is set to "1" and remains set, until it is cleared by reading the Readout register. An Attention Request is generated on the bus, only if it is enabled by the Attention Enable bit (ATE) in the Temperature Control register.

Setup Before Enabling No setup is required for the Temperature Measurement function before the function is enabled.

7.12 Temperature Capabilities (Addr 10o)

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
001 000	Temperature Capabilities	R	014Ah	Reserved							Int Sens	Rout Size	Sign	10Bits	0.25°C Resolution				
				0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	0

This register defines the format of the temperature data in the readout register. The LM95010 only supports one format as defined by the values of this register.

Bit	Type	Description
2-0	R	**Resolution.** This field defines the value of 1 LSb of the Temperature Readout field in the Readout Register. The SensorPath specification defines many different weights for the temperature LSb. The LM95010 supports a resolution of 0.25 °C and thus a value of 010 for this field. For a full definition of this field please refer to the SensorPath specification.
5-3	R	**Number of Bits.** This field defines the total number of significant bits of the Temperature Readout field in the Readout register. The total number of osignificant bits includes the number of bits representing the interger part of the temperature data and the fractional part of it, as defined by the Resolution field. The LM95010 supports 10 bits and thus a value of 001 for this field. For a full definition of this field please refer to the SensorPath specification.
6	R	**Sign (Signed Data).** Defines the type of data in the Temperature Readout field of the Readout register. 0: Unsigned, positive fixed point value. 1: Signed, 2's complement fixed point value. (value for the LM95010)
7	R	**RoutSize (Readout Register size).** Defines the total size of the Readout register. 0: 16 bits. (LM95010 default) 1: 24 bits.
8	R/W	**IntSens (Internal Sensor Support).** Indicates if the device supports internal temperature measurements, as the LM95010 does. 0: No internal temperature measurement 1: Internal temperature sensor implemented. (value for the LM95010)
15-9	RO	**Reserved.** Will always read "0".

7.13 Temperature Data Readout (Addr 11o)

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
001 001	Temperature Data Readout	R		MSb Sign	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5 °C	LSb 0.25 °C	Reserved					
														0	0	0	0	0	0

The LM95010's temperature data format is two's complement and has 10-bits of resolution with the LSb having a weight of 0.25 °C. The LM95010 can resolve temperature between +127.75 °C and -128 °C, inclusive. It can measure temperatures between +127.75 °C and −20 °C with an accuracy of ±3.0 °C.

Table 7-2. Temperature Data Format

Decimal	Binary	Hex
+127.75 °C	01 1111 1111	1FFh
+100.00 °C	01 1001 0000	190h
+1.00 °C	00 0000 0100	004h
+0.25 °C	00 0000 0001	001h

Table 7-2. Temperature Data Format (continued)

Decimal	Binary	Hex
0 °C	00 0000 0000	000h
-0.25 °C	11 1111 1111	3FFh
-1.00 °C	11 1111 1100	3FCh
-20.00 °C	11 1011 0000	3 B0h
-39.75 °C	11 0110 0001	361h
-40.00 °C	11 0110 0000	360h
-128.00 °C	10 0000 0000	200h

7.14 Temperature Control (Addr 12o)

This register is set to the reset value by a Device Reset.

Reg Add	Register Name	R/W	POR Val	Bit 15 MSb	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
001 010	Temperature Control	R/W	Reserved															EN0	ATE
			0h	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit	Type	Description
0	R	**ATE (Attention Enable).** When set, this bit enables an Attention Request signal to generated by the LM95010, if the EN0 bit is set. 0: Attention Request disabled (from enabled Temperature Sensor- default) 1: Attention Request enabled
1	R	**EN0 (Enable Sensor).** When this bit is set, the Temperature Sensor is enabled for temperature measurements. 0: Temperature Sensor disabled (default) 1: Temperature Sensor enabled
15-2	R	**Reserved.** Will allways read "0".

7.15 Conversion Rate (Addr 40o)

Reg Add	Register Name	R/W	POR Val	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb
100 000	Conversion Rate	R/W	2h	0	0	0	0	0	0	Conversion Rate	

LowPwr	Conversion Rate[1:0]	Typical Conversion Rate (ms)
0	00	14
1	00	91
0	01	91
1	01	364
0	10	182 (default)
1	10	728
0	11	364
1	11	1456

The temperature conversion rate is controlled by this register as well as the Low Power Bit of Device Control Register. This register is not defined by the SensorPath specification. Therefore, it must be accessed during BIOS run time. The conversion rate is dependent on system physical requirements and limitations. The thermal response time of the VSSOP package is one such requirement.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Mounting Considerations

The LM95010 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface. The temperature that the LM95010 is reading will typically be within +0.2 °C of the surface temperature to which the LM95010's leads are attached to.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature measured would be at an intermediate temperature between the surface temperature and the air temperature.

Alternatively, the LM95010 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM95010 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to ensure that moisture cannot corrode the LM95010 or its connections.

The thermal resistance junction to ambient (θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. For the LM95010 the equation used to calculate the rise in the die temperature is as follows:

$$T_J = T_A + \theta_{JA} \times [(V^+ \times I_Q) + (V_{OL} \times I_{OL})] \quad (1)$$

where

- I_Q is the quiescent current (500 µA typ.)
- V_{OL} is the logic "Low" output level of SWD
- I_{OL} is the load current on SWD

Since the LM95010's junction temperature is the actual temperature being measured care should be taken to minimize the load current that the LM95010 is require to drive. When mounted to a PCB, with 2 oz. copper foil, the LM95010's thermal resistance is typically 210 °C/W.

9 Device and Documentation Support

9.1 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
SensorPath® is a registered trademark of TI.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E (November 2023)	Page
• Updated format to match new TI layout and flow. Tables, figures and cross-references use a new numbering sequence throughout the document	1

Changes from Revision C (May 2004) to Revision D (March 2013)	Page
• Changed layout of National Data Sheet to TI format	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM95010CIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-20 to 125	T19C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

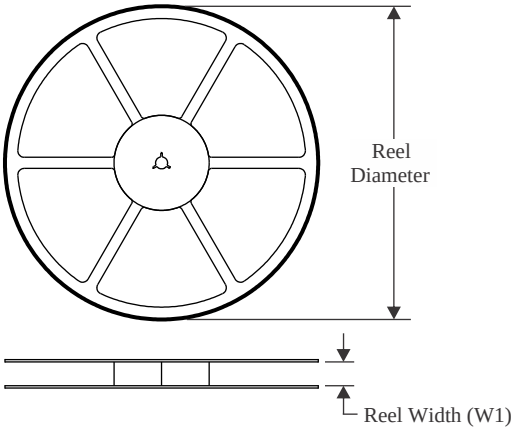
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

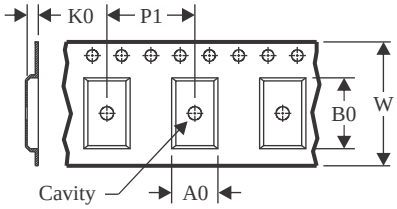
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

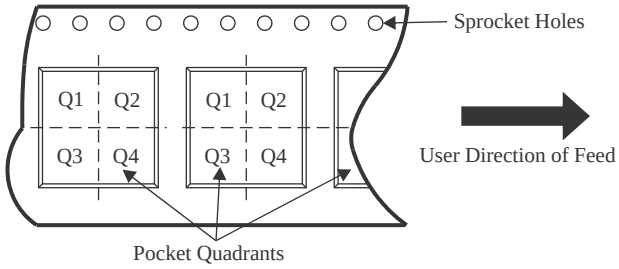


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

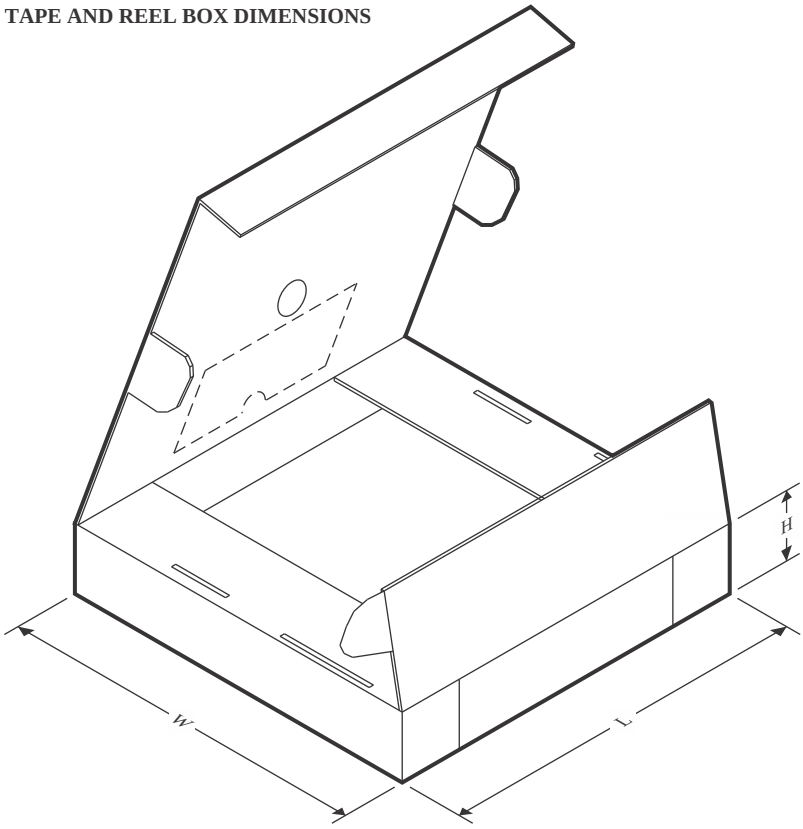
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM95010CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

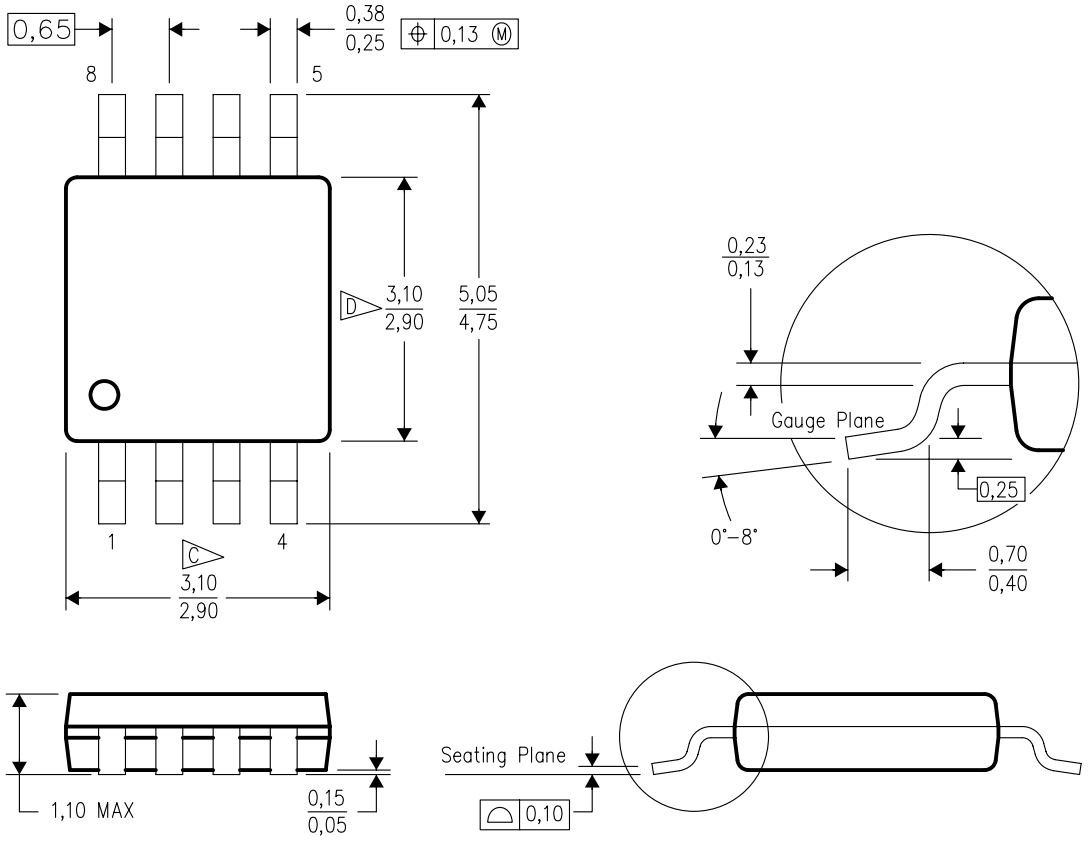
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM95010CIMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

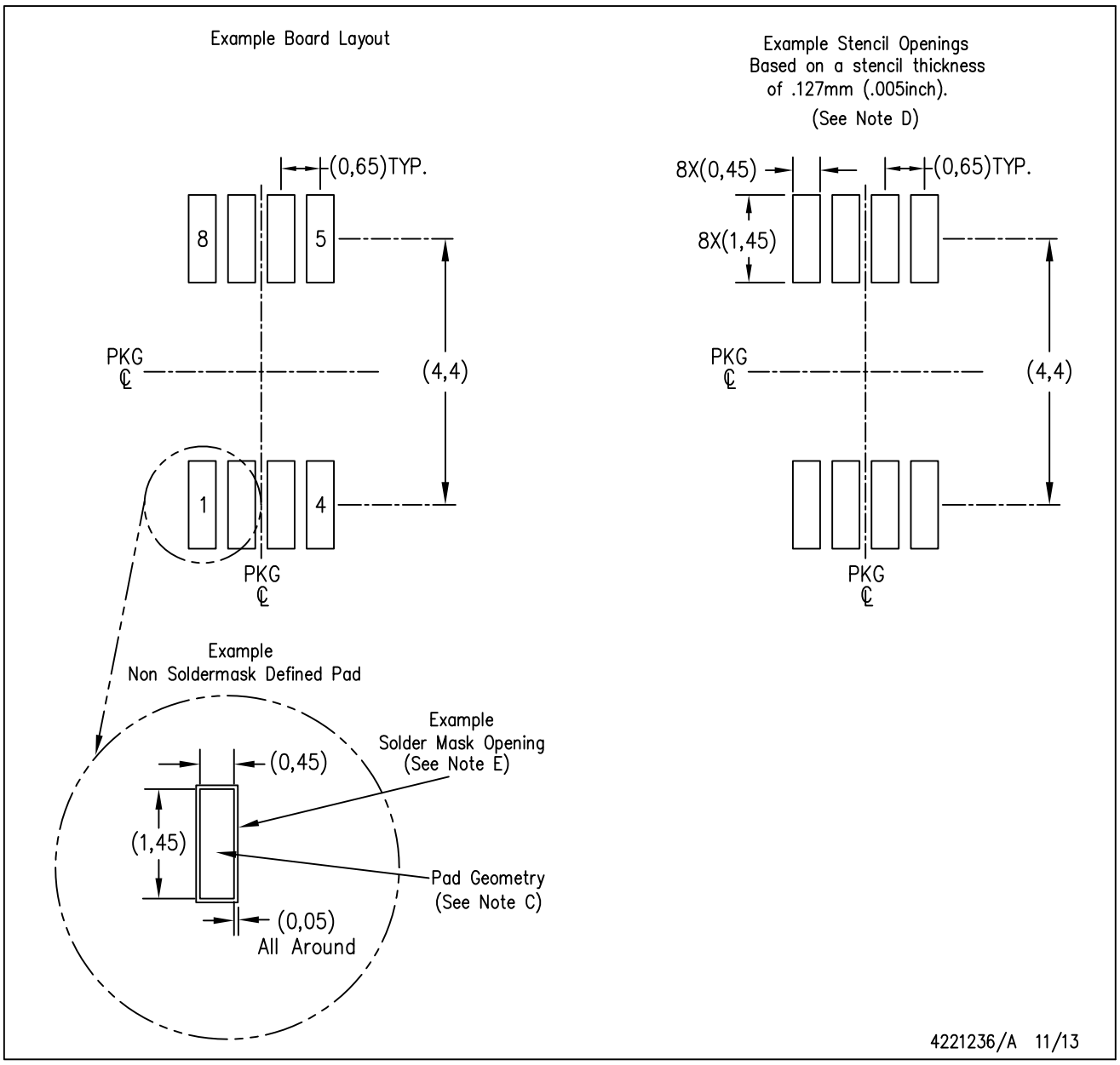
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265