LM98620 10-Bit 70 MSPS 6 Channel Imaging Signal Processor with LVDS Output

1 Features

- 3.3 V Single Supply Operation
- CDS or S/H Processing
- 35 MHz Channel Rate
- Enhanced ESD Protection on Timing, Control and LVDS Pins
- Low Power CMOS Design
- 12 Terminal to 16 Terminal (Selectable) LVDS Serialized Data Output
- 4-Wire Serial Interface
- 2 Channel Symmetrical Architecture
- Independent Gain and Offset Correction for Each Channel
- Digital Black Level Calibration for Each Channel
- Digital White Level Calibration for Each Channel
- Programmable Input Clamp
- **Key Specifications**
  - Maximum Input Level:
    - 1.2 Vp-p (CDS Gain = 1.0)
    - 0.58 Vp-p (CDS Gain = 2.1)
  - Input Sample Rate:
    - 5 to 35 MSPS - 6ch mode
    - 10 to 35 MSPS - 3ch mode
  - PGA Gain Range: 1x to 10x (0 to 20 dB)
  - CDS/SH Gain Settings: 1x or 2.1x
  - Total Channel Gain: 1x to 21x (0 to 26 dB)
  - PGA Gain Resolution: 8 bits - Analog
  - ADC Resolution: 10 bits
  - ADC Sampling Rate: 10 to 70 MSPS
  - SNR: 68.5 dB (Gain = 1x)
  - Offset DAC Range:
    - ±111 mV or ±59.5 mV - FDAC
    - ±281 mV - CDAC
  - Offset DAC Resolution:
    - ±10 bits - FDAC
    - ±4 bits - CDAC
  - Supply Voltage: 3.0 V to 3.6 V
  - Power Dissipation: 1.02 W (typical)

2 Applications

- High Performance Digital Color Copiers
- Scanners
- Other Image Processing Applications

3 Description

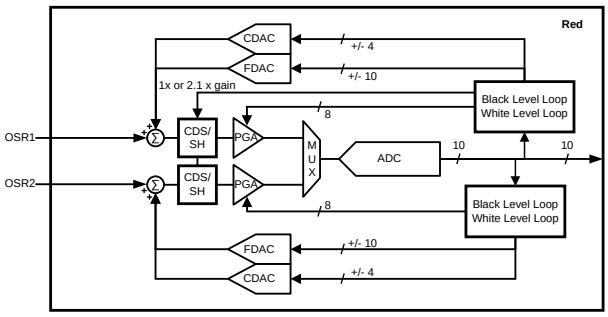
The LM98620 is a fully integrated, 10-Bit, 70 MSPS signal processing solution for high performance digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative six channel architecture utilizing Correlated Double Sampling (CDS), or Sample and Hold (SH) type sampling. Gain settings of 1x or 2x are available in the CDS/SH input stage. Each channel has a dedicated 1x to 10x (8 bit) PGA that allows accurate gain adjustment. The Digital White Level auto calibration loop can automatically set the PGA value to achieve a selected white target level. Each channel also has a ±4 bit coarse and ±10-bit fine analog offset correction DAC that allows offset correction before the sample-and-hold amplifier. These correction values can be controlled by an automated Digital Black Level correction loop. The PGA and offset DACs for each channel are programmed independently allowing unique values of gain and offset for each of the six channels. A 2-to-1 multiplexing scheme routes the signals to three 70 MHz high performance ADCs. The fully differential processing channels achieve exceptional noise immunity, having a very low noise floor of –68.5dB. The 10-bit analog-to-digital converters have excellent dynamic performance, making the LM98620 transparent in the image reproduction chain.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM98620	TQFP (80)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2014) to Revision C — **Page**

- Added data sheet flow and layout to conform with new TI standards. Added the following sections: Applications and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Added footnote "When the input voltage..." to Absolute Maximum Ratings table ... 5

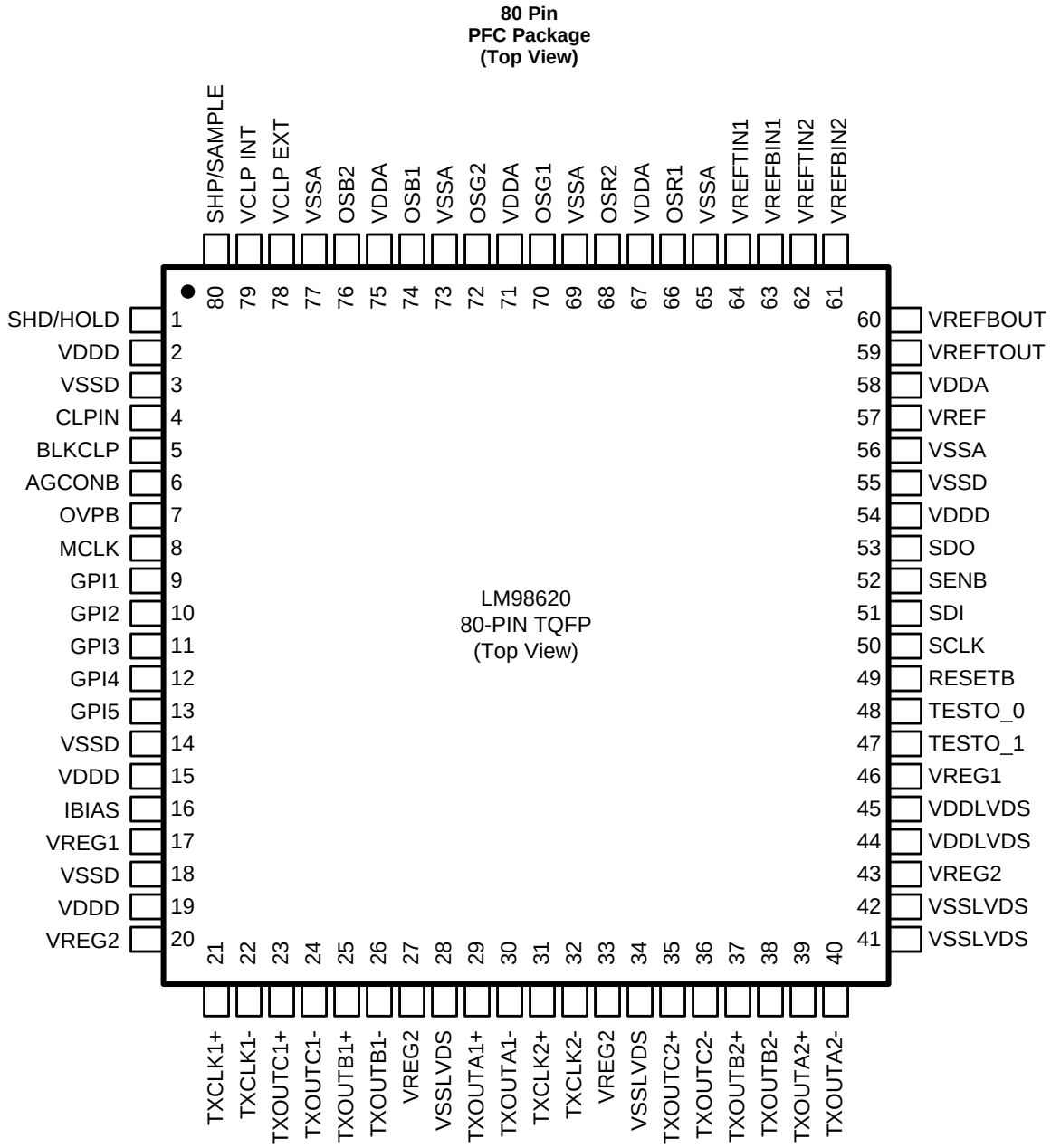
Changes from Revision A (December 2013) to Revision B — **Page**

- Changed format of data sheet to conform with TI standards. ... 1

Changes from Original (February 2008) to Revision A — **Page**

- Added sections to make full data sheet from template. ... 1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE(1)	PULLUP PULLDOWN	DESCRIPTION
NAME	NUMBER			
SHD/HOLD	1	DI		Data Clamp Pulse/Hold Input
VDDD	2, 15, 19, 54	PI		Digital Power Supply
VSSD	3, 14, 18, 55	PI		Digital Power Supply Ground
CLPIN	4	DI		Input Pulse that Invokes the Input Clamp Switch
BLKCLP	5	DI	PD 108 kΩ	Input Pulse that Invokes the Black Calibration Loop
AGC_ONB	6	DI	PU 108 kΩ	Input Pulse that Invokes the White Calibration Loop. Tie high to disable White Clamp. Pulse Low to initiate White Clamp. (Active Low)
OVPB	7	DI		Over Voltage Protection Enable (Active Low). Enables OS input protections switches to ground during system power up. Should be tied high after AFE and CCD voltages have stabilized.
MCLK	8	DI		Master Clock Input
GPI1-5	9 to 13	DI		General Purpose Inputs 1 – 5, mapped into LVDS output data
IBIAS	16	AO		Optional IBIAS resistor connection. To minimize device to device power consumption variation, connect an 11k Ω 1% resistor to VSSA. If no resistor is used, the internal bias and power supply currents will be subject to normal device to device variation.
VREG1	17, 46	PO		Decoupling connection for VREG1 – Approx. 1.8 V output(2)
				Decoupling connection for VREG2 – Approx. 1.8 V output(2)
VREG2	20, 27, 33, 43	PO		
TXCLK1	21, 22	DO		Differential LVDS Output Clock 1
TXOUTC1	23, 24	DO		Differential LVDS Output Data C1
TXOUTB1	25, 26	DO		Differential LVDS Output Data B1
VSSLVDS	28, 34, 41, 42	PI		LVDS Power Supply Ground
TXOUTA1	29, 30	DO		Differential LVDS Output Data A1
TXCLK2	31, 32	DO		Differential LVDS Output Clock 2
TXOUTC2	35, 36	DO		Differential LVDS Output Data C2
TXOUTB2	37, 38	DO		Differential LVDS Output Data B2
TXOUTA2	39, 40	DO		Differential LVDS Output Data A2
VDDLVDS	44, 45	PI		LVDS Power Supply
TESTO_1	47	DO		Digital Test Output
TESTO_0	48	DO		Digital Test Output
RESETB	49	DI	PU 108 kΩ	Master Reset Input(Active Low)
SCLK	50	DI		Serial Clock for the 4-wire Serial Interface
SDI	51	DI		Serial Data for the 4-wire Serial Interface
SENB	52	DI	PU 108 kΩ	Serial Enable (Active Low) for the 4-wire Serial Interface
SDO	53	DO		Serial Output Data for the 4-wire Serial Interface
VSSA	56, 65, 69, 73, 77	PI		Analog Power Supply Ground
VREF	57	AO		Reference Voltage Bypass – Approx. 1.2 V output(2)
VDDA	58, 67, 71, 75	PI		Analog Power Supply
VREFTOUT	59	AO		Top Reference Bypass. Connect to bypass capacitors (see *Applications and Implementation*) and VREFTINx. – Approx. 2.23 V output.(2)

(1) **KEY**: **A** – Analog, **D** – Digital, **P** – Power, **I** – Input, **O** – Output, **PD** – Pull-down resistor to VSSD. **PU** – Pull-up resistor to VDDD.
(2) Voltages provided for debugging only. Not a guaranteed specification.

Pin Functions (continued)

PIN		TYPE(1)	PULLUP PULLDOWN	DESCRIPTION
NAME	NUMBER			
VREFBOUT	60	AO		Bottom Reference Bypass. Connect to bypass capacitors (see *Applications and Implementation*) and VREFBINx. – Approx. 0.98 V output.(3)
VREFBIN2	61	AI		Bottom Reference Input Voltage for the ADC. Connect to VREFBOUT.
VREFTIN2	62	AI		Top Reference Input Voltage for the ADC. Connect to VREFTOUT.
VREFBIN1	63	AI		Bottom Reference Input Voltage for the AFE. Connect to VREFBOUT.
VREFTIN1	64	AI		Top Reference Input Voltage for the AFE. Connect to VREFTOUT.
OSR1	66	AI		Input Voltage 1 for the Red Channel
OSR2	68	AI		Input Voltage 2 for the Red Channel
OSG1	70	AI		Input Voltage 1 for the Green Channel
OSG2	72	AI		Input Voltage 2 for the Green Channel
OSB1	74	AI		Input Voltage 1 for the Blue Channel
OSB2	76	AI		Input Voltage 2 for the Blue Channel
VCLP_EXT	78	AI		External Clamp Voltage (Connect to VCLP_INT or customer supplied reference voltage
VCLP_INT	79	AO		Internally Generated V-Clamp Voltage. Connect to bypass capacitors and VCLK_EXT. – Approx. 1.65 V output(3)
SHP/SAMPLE	80	DI		Pedestal Clamp Pulse/Sample Input.

(3) Voltages provided for debugging only. Not a guaranteed specification.

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage	–0.3	4.2	V
Voltage at any Pin (except VREG1, VREG2)	–0.3	VDDA + 0.3	V
Voltage at VREG1, VREG2	–0.3	2.1	V
Continuous Input Current at any Pin(2)		±25	mA
Continuous Input Package Current(2)		±50	mA
Maximum Junction Temperature (Powered)	$T_{J\_ABS\_MAX}$ = +135		°C
Specified Ambient Temperature Range	0 ≤ T A ≤ +70		°C
Maximum Junction Temperature	$T_{J\_OP\_MAX}$ = +110		°C

(1) Absolute maximum ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.
(2) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < (GND - 0.3 V) or V_{IN} > (V_{DDA} + 0.3 V)), the DC current at that pin should be limited to ±25 mA. The 50 mA DC maximum package input current means that a maximum of two pins can simultaneously have input currents that equal 25 mA.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$ (1)(2)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (3)		2500	V
		Machine Model (MM)		250	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (4)		1000	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin. Charged device model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.
(a) Higher 7500V human body model rating and 750V machine model rating for the following pins: SHP, SHD, CLPIN, BLKCLP, AGC_ONB, OVPB, MCLK, RESETB, SENB, SCLK, SDI, SDO, TXCLK1, TXCLK2, TXOUTA1, TXOUTB1, TXOUTC1, TXOUTA2, TXOUTB2, TXOUTC2.
(3) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(4) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Analog Supply Voltage Range	+3.0		+3.6	V
Digital Supply Voltage Range	+3.0		+3.6	V
LVDS Supply Voltage Range	+3.0		+3.6	V
DC Power Supply Voltage Relationships (1)	VDDD ≥ VDDA, VDDD ≥ VDDLVDS			V
Voltage at any Digital I/O pin	0		VDDD	V
Voltage at any Analog Input pin	0		VDDA	V
Voltage at any LVDS I/O pin	0		VDDLVDS	V

(1) Static voltage levels on VDDD must be at the same voltage or slightly higher than VDDLVDS or VDDA. Therefore, driving all three power supplies from a common linear voltage regulator is recommended. Please see Figure 1.

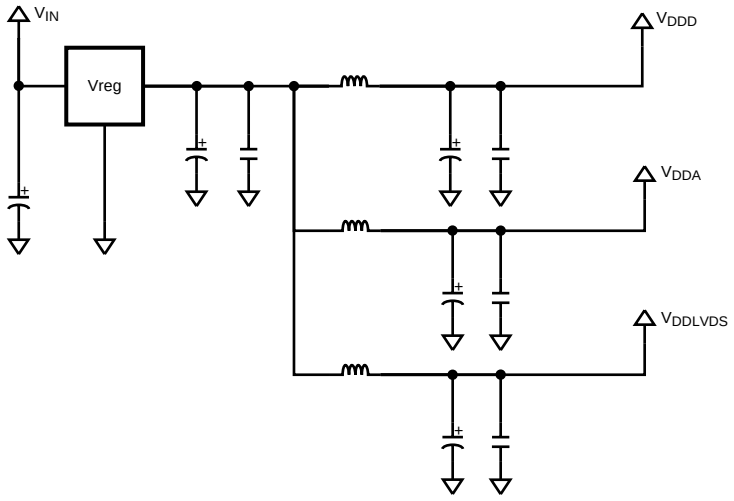


Figure 1. Recommended Setup

6.4 Thermal Information

THERMAL METRIC[1]		LM98620VHB TQFP 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).
The following specifications apply for VDDA = VDDD = VDDLVDS = 3.3 V; F_{MCLK} = F_{ADCCLK}= 70 Ms/s; 6 Channel Mode unless otherwise noted.

PARAMETER		TEST CONDITIONS	$T_A = T_{MIN}$ to T_{MAX}			T_A = +25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ADC/AFE									
	Resolution	No missing codes			10				bits
INL	Integral Non-Linearity	Gain = 1x	-1.5%		1.8%	-0.6% to 0.8%			
		Gain = 6x				-1.4% to 1.4%			
DNL	Differential Non-Linearity	Gain = 1x	-0.99		1.6	-0.4 to 0.4			lsb
		Gain = 6x				-0.6 to 0.7			
SNR	Signal-to-Noise Ratio[1]	Gain = 1x				68.5			dB
		Gain = 6x				58.5			
	Analog Input Range (OSx Inputs)	Negative Polarity:							
		• Peak-to-peak, CDS gain = 1x	1.12		1.28	1.2			V
		• Peak-to-peak, CDS gain = 2.1x	0.54		0.62	0.58			
		Positive Polarity:							
		• Peak-to-peak, CDS gain = 1x				1.2			V
	Analog Input Leakage (Osx inputs)	GND < Vin < VDDA Source Follower Enabled – OVP off	–250		200	±25			nA
R_{CLAMP}	Input Clamp Impedance	(See [2])				43			Ω
	Conversion Ratio	CDS/SH Gain Setting = 1x PGA gain setting = Min	0.79		0.91	0.85			lsb/mV
	Conversion Ratio Color to Color[3] Error					0.24%			
	Conversion Ratio Ch1 to Ch2 Error					0.13%			
	Crosstalk – Color to Color	R1,B1 to G1; R1,G1 to B1, and so forth. R2, B2, to G2; R2, G2, to B2, and so forth. Gain = 20x setting				0.07%			
	Crosstalk – Ch1 to Ch1	R1 to R2, R2 to R1, G1 to G2, G2 to G1, B1 to B2, B2 to B1 Gain = 20x setting				0.2%			

(1) SNR = 20log(1024/Output Noise(lsb rms)) with input = DC.
(2) This parameter specified by simulation and/or bench evaluation and not production tested.
(3) For conversion ratio min/max, variation and error, Conversion ratio is: (Digital Max – Digital Min)/(Vin Max – Vin Min). Measured at gain setting of 1x

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).
The following specifications apply for VDDA = VDDD = VDDLVDS = 3.3 V; F_{MCLK} = F_{ADCCLK}= 70 Ms/s; 6 Channel Mode unless otherwise noted.

PARAMETER		TEST CONDITIONS	$T_A = T_{MIN}$ to T_{MAX}			T_A = +25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Power Consumption	Active Mode:							
		• Total Power			1119		1020		mW
		• IDDA			240				mA
		• IDDD			58				mA
		• IDDLVDS			41				mA
	Power Consumption	Power-Down Mode:							
		• MCLK Active			191		159		mW
		• MCLK Stopped			47		23		mW
PGA (8 bits) Gain = 283/(283-M)									
	PGA Gain Range(4)	Gain at max setting/ Gain at min setting	19.5		20.9		20		dB
	PGA Stepsize						0.3		dB
	PGA Monotonicity				Mono-tonic				
	PGA Error (Difference from ideal curve)						<0.6%		
CDS/SH									
	CDS/SH Gain	Gain at 2.1x / Gain at 1x					6.4		dB
			2		2.13		2.1		V/V
Offset FDAC (±10 bits)									
	DAC Full Scale (input referred)	Large FDAC range	103		120		111		±mV
		Small FDAC range	54		66		59.5		
	DAC Monotonicity				Mono-tonic				
Offset CDAC (± 4 bits)									
	DAC Full Scale (input referred)		259		302		281		±mV
	DAC Monotonicity				Mono-tonic				
BLACK CALIBRATION LOOP									
	Target Output Level				127	0			lsb
WHITE CALIBRATION LOOP									
	Target Output Level		512		1023				lsb
	Window Size				2,4,8, 16,32				# Pixels
LOGIC I/O DC PARAMETERS									
V_{IH}	Logic Input High Threshold	SHP, SHD, CLPIN, BLKCLP, AGC_ONB, OVPB, MCLK, GPIn, SCLK, SDI, SENB	2.0						V
V_{IL}	Logic Input Low Threshold	SHP, SHD, CLPIN, BLKCLP, AGC_ONB, OVPB, MCLK, GPIn, SCLK, SDI, SENB			0.8				V
I_{IN}	Logic Input Leakage		–100		100		±25		nA
V_{OH}	Logic Output Voltage High	VDDD = 3.6 V, Iout = –0.5 mA	3.3				3.5		V
		VDDD = 3.0 V, Iout = –0.5 mA	2.7				2.9		

(4) PGA gain range is: [(ADC_OUT(PGA @ 1111111111)) / (ADC_OUT(PGA @ 0000000000))]

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).
The following specifications apply for VDDA = VDDD = VDDLVDS = 3.3 V; F_{MCLK} = F_{ADCCLK}= 70 Ms/s; 6 Channel Mode unless otherwise noted.

PARAMETER		TEST CONDITIONS	$T_A = T_{MIN}$ to T_{MAX}			T_A = +25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	Logic Output Voltage Low	VDDD = 3.6 V, Iout = 1.6 mA			0.3		0.15		V
		VDDD = 3.0 V, Iout = 1.6 mA			0.3		0.15		
V_{REB}	Power On Reset Threshold						1.4		V
LVDS DC PARAMETERS									
V_{OD}	Differential Output Voltage		210		420		300		mV
ΔV_{OD}	Change in Diff. Output Voltage				17		2.5		mV
V_{OS}	Offset Voltage		1.17		1.28		1.2		V
ΔV_{OS}	Change in Offset Voltage				13		2.5		mV
I_{OS}	Output Short Circuit Current	TXCLKx			6.7		5		mA
		TXOUTxx			8.9		7		

6.6 Timing Requirements, AFE/ADC Timing

		TEST CONDITIONS	$T_A = T_{MIN}$ to T_{MAX}			T_A = +25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{MCLK}	MCLK frequency	6 channel mode	10		70				MHz
		3 channel mode	10		35				
DC	MCLK Duty Cycle					40%		60%	
S_{MAX}	Input Sampling Rate – maximum				35				MS/s
S_{MIN}	Input Sampling Rate – minimum		5						MS/s
			10						
t_{RESET}	RESETB Pulse Width		2						t_{MCLK}
t_{RESET_CLR}	RESETB Clear Time (1)				3				t_{MCLK}
t_{MNS}	Min Sample Falling Edge Setting	SH2b (t_{SHD} = 8.2 ns), MCLK= ADCCLK/2):							
		• ADCCLK = 20 MHz			5		4		Decimal Setting
		• ADCCLK = 70 MHz					12	14	
t_{MXS}	Max Sample Falling Edge Setting	SH2b (t_{SHD} = 8.2 ns), MCLK = ADCCLK/2:							
		• ADCCLK = 20 MHz	27				29		Decimal Setting
		• ADCCLK = 70 MHz	23				25		
t_{MXE}	Sample Falling Edge Max Error	SH2b, Register 0x36 = Min to Max (MCLK = ADCCLK/2):							
		• ADCCLK = 20 MHz					+0.2/ –0.3		ns
		• ADCCLK = 70 MHz					+0.2/ –0.4		ns
t_{SFED}	Sample Falling Edge Delay (MCLK rising edge to OSx voltage step)	SH2b, Register 0x36 = 16d (MCLK = ADCCLK/2):							
		ADCCLK = 70 MHz					13		ns
t_{SHD}	SHP/SHD high period	(See (1))					8.2		ns

(1) This parameter specified by simulation and/or bench evaluation and not production tested.

Timing Requirements, AFE/ADC Timing (continued)

		TEST CONDITIONS	$T_A = T_{MIN}$ to T_{MAX}			T_A = +25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{MCS_MIN}	MCLK high to SAMPLE high (minimum) (See (2))	SH3 Mode – ADC Rate MCLK			15		11		ns
		SH2a Mode			15.5		11.7		
		SH1b Mode			6		3.5		
		CDSb Mode			6		3.3		
t_{HMC_MIN}	HOLD high to MCLK high (minimum) (See (2))	SH3 Mode – ADC Rate MCLK			2.5		–1		ns
		SH2a Mode			1.5		–2.4		
		SH1b Mode			1		–4.5		
		CDSb Mode			1		–5.5		
t_{MCH_MIN}	MCLK high to HOLD high (Minimum)	SH3 Mode – ADC Rate MCLK			6		2		ns
t_{AD}	Aperture delay						5		ns
	Aperture delay variation						0.6		ns
t_{CLPIN}, t_{BLKCLP}	CLPIN/BLKCLP Pulse Width	(high or low)	2						t_{MCLK}
t_{IS}	CLPIN/BLKCLP/GPIn Setup		3						ns
t_{IH}	CLPIN/BLKCLP/GPIn Hold		3						ns
t_{C_B}	CLPIN neg. edge to BLKCLP start (See (3))	6 Channel mode					16		Pixels
		3 Channel mode					10		
t_{GPI_LAT}	GPIn Latency (See (3))	6 Channel – ADC Rate MCLK					3		t_{MCLK}
		6 Channel – Pixel Rate MCLK					1.5		
		3 Channel – ADC = Pixel Rate MCLK					3		
$t_{LAT(1)}$	6 Channel Mode	ADC Rate MCLK					11		t_{MCLK}
	Channel 1 Latency	Pixel Rate MCLK					5.5		
$t_{LAT(2)}$	6 Channel Mode	ADC Rate MCLK					12		t_{MCLK}
	Channel 2 Latency	Pixel Rate MCLK					6		
t_{LAT}	3 Channel Mode Latency	ADC=Pixel Rate MCLK					11		t_{MCLK}

(2) Measured with AFEPHASE = 11. For other AFEPHASE settings,these sample input timings will shift earlier with respect to MCLK as follows. (tHMC will increase by these amounts, t_{MCH} will decrease by these amounts):
  (a) AFEPHASE = 10 – Earlier by ¼ pixel period
  (b) AFEPHASE = 01 – Earlier by ½ pixel period
  (c) AFEPHASE = 00 – Earlier by ¾ pixel period
(3) This parameter specified by simulation and/or bench evaluation and not production tested.

6.7 Timing Requirements, Serial Interface Timing

		TEST CONDITIONS	$T_A = T_{MIN}$ to T_{MAX}			UNIT
			MIN	TYP	MAX	
t_{CP}	SCLK period		50			ns
t_{WH}	SCLK High width		20			ns
t_{WL}	SCLK Low width		20			ns
t_{IS}	SDI Setup time		5			ns
t_{IH}	SDI Hold time		5			ns
t_{SENSC}	SENB low before SCLK rising		5			ns
t_{SCSEN}	SENB high after SCLK rising		5			ns
t_{SENW}	SENB high width		5			t_{MCLK}
t_{OD}	SDO Output delay		2		10	ns

6.8 Timing Requirements, LVDS Output Timing

		TEST CONDITIONS	$T_A = T_{MIN}$ to T_{MAX}			T_A = +25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{TXCLK}	LVDS TXCLK Frequency		10		70				MHz
t_{TXCLK}	LVDS TXCLK Period		14.3		100				ns
LLHT	LVDS Low to High Transition Time	(See (1))					0.75		ns
LHLT	LVDS High to Low Transition Time	(See (1))					0.75		ns
TCCS	TxOUT Channel to Channel Skew	70 MHz TXCLK (See (2))					250		ps
TPPos0	Transmitter Output Pulse Pos. Bit 0	70 MHz TXCLK (2)	-0.26		0.1		-0.06		ns
		10 MHz TXCLK (3)	-0.44		0.48		0		
TPPos1	Transmitter Output Pulse Pos. Bit 1	70 MHz TXCLK (2)	1.47		2.46		2		ns
		10 MHz TXCLK (3)	8.56		20		14.2		
TPPos2	Transmitter Output Pulse Pos. Bit 2	70 MHz TXCLK (2)	3.64		4.49		4.1		ns
		10 MHz TXCLK (3)	24.1		35.2		29.7		
TPPos3	Transmitter Output Pulse Pos. Bit 3	70 MHz TXCLK (2)	5.42		6.33		5.9		ns
		10 MHz TXCLK (3)	37.9		49.3		43.7		
TPPos4	Transmitter Output Pulse Pos. Bit 4	70 MHz TXCLK (2)	7.56		8.38		8		ns
		10 MHz TXCLK (3)	52.5		63.1		57.9		
TPPos5	Transmitter Output Pulse Pos. Bit 5	70 MHz TXCLK (2)	9.56		10.33		10		ns
		10 MHz TXCLK (3)	67.7		76.9		72.4		
TPPos6	Transmitter Output Pulse Pos. Bit 6	70 MHz TXCLK (2)	11.82		12.53		12.2		ns
		10 MHz TXCLK (3)	81.8		90.2		85.9		

(1) This parameter specified by simulation and/or bench evaluation and not production tested.
(2) TPPos0 to TPPos6 values are given for 70 MHz TXCLK frequency. These values are ensured by characterization and are not production tested.
(3) TPPos0 to TPPos6 values are given for 10 MHz TXCLK frequency. These values are ensured by characterization and are not production tested.

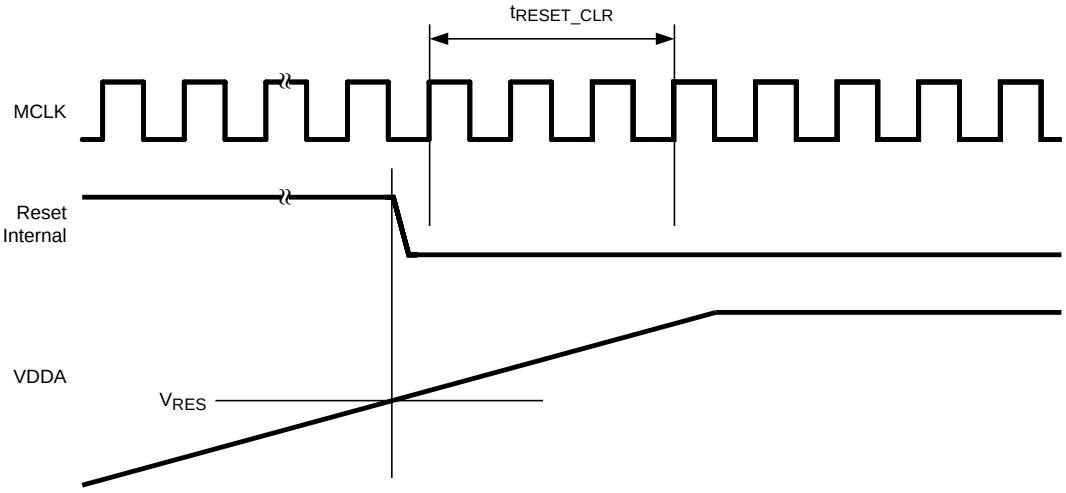


Figure 2. Power on Reset (POR)

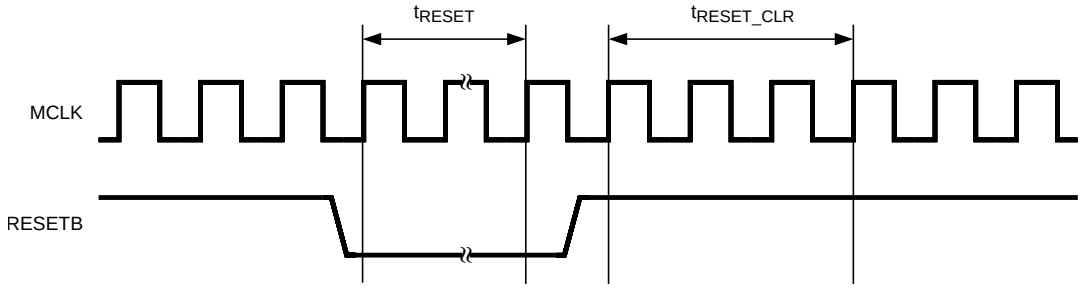
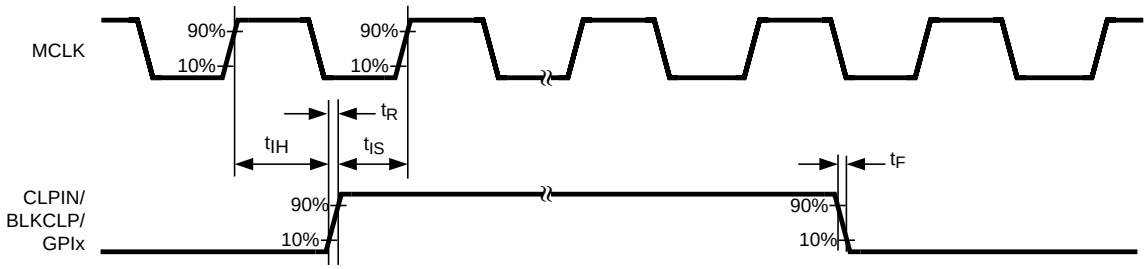
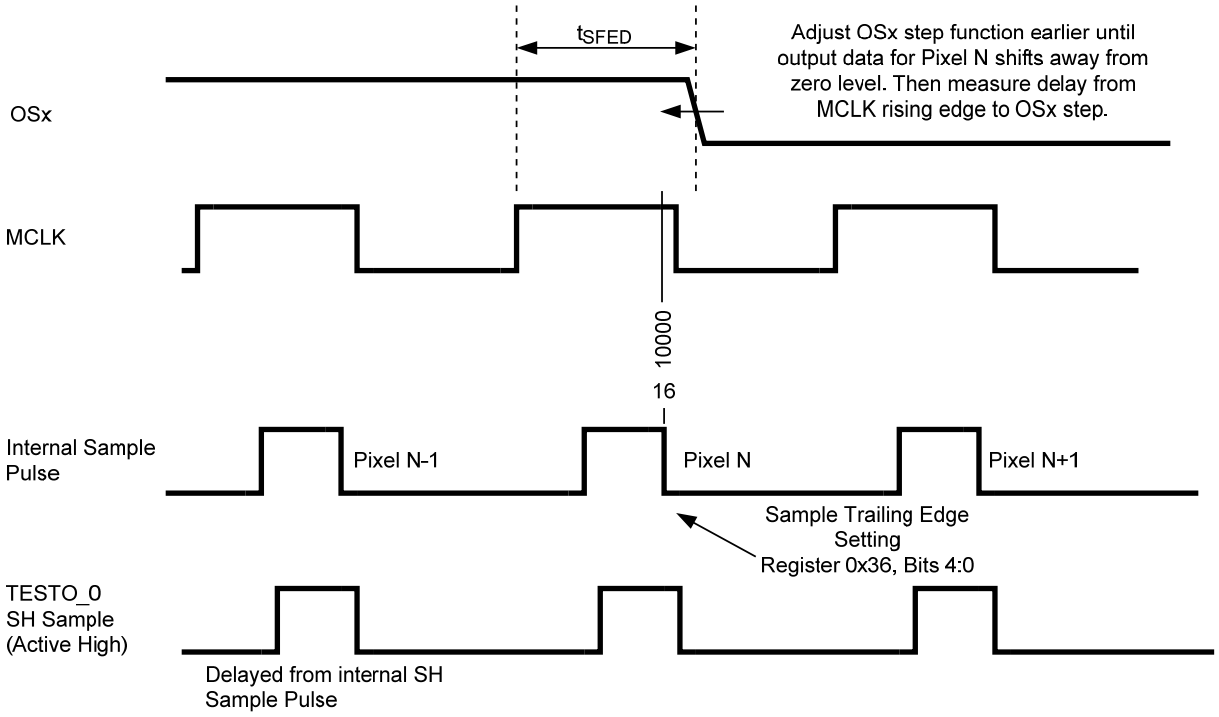


Figure 3. RESETB Input Timing



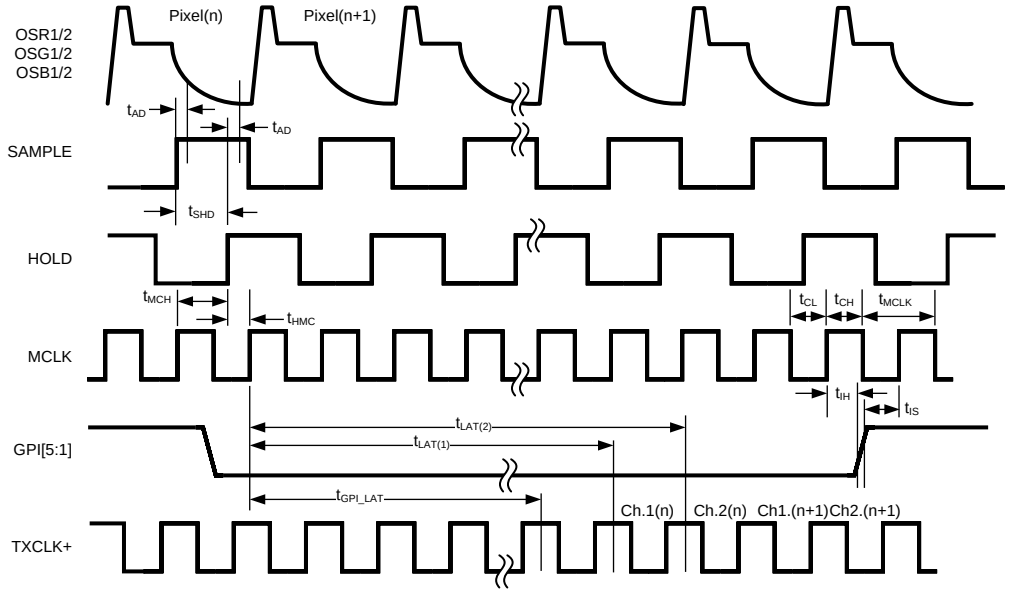
Note: CLPIN, BLKCLP and GPIx are all sampled or latched on the rising edge of MCLK

Figure 4. Input Setup and Hold Timing



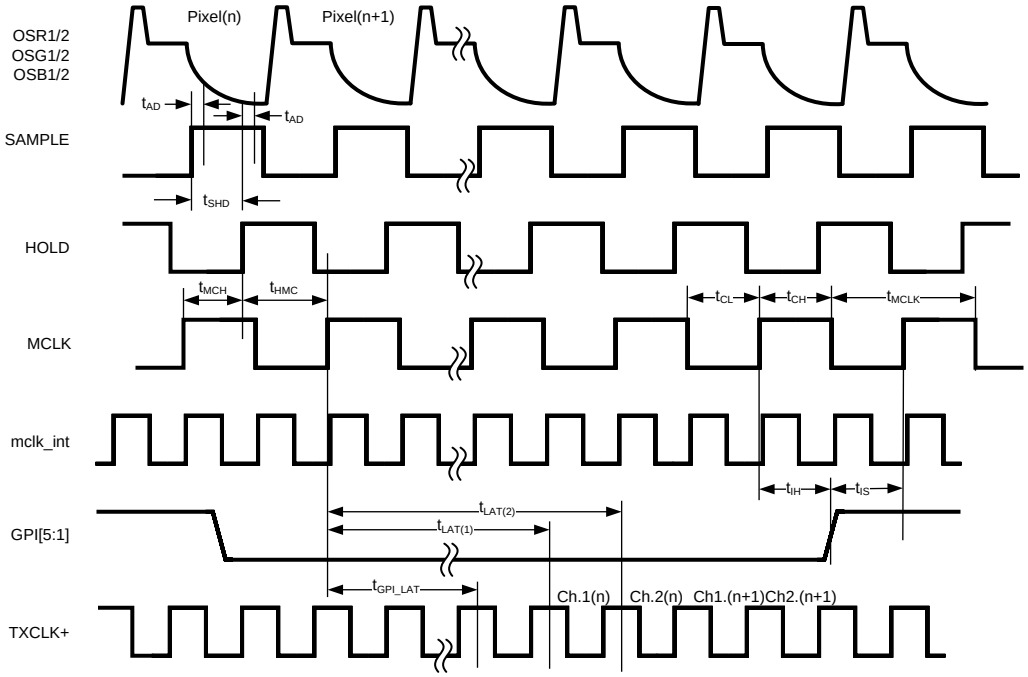
AFEPHASE = 11, SAMPLE Falling Edge = 16d

Figure 5. Sample Falling Edge Delay



Above timing relationships between SAMPLE, HOLD and MCLK are for AFEPHASE = 11.
For other AFEPHASE settings, the sampling timing can move earlier by ¼, ½ or ¾ pixel period with respect to MCLK, but the latency as shown above will remain constant.

Figure 6. Output Latency and Timing – 6 Channel Mode – ADC Rate MCLK



Above timing relationships between SAMPLE, HOLD and MCLK are for AFEPHASE = 11.
For other AFEPHASE settings, the sampling timing can move earlier by ¼, ½ or ¾ pixel period with respect to MCLK, but the latency as shown above will remain constant.

Figure 7. Output Latency and Timing – 6 Channel Mode – Pixel Rate MCLK

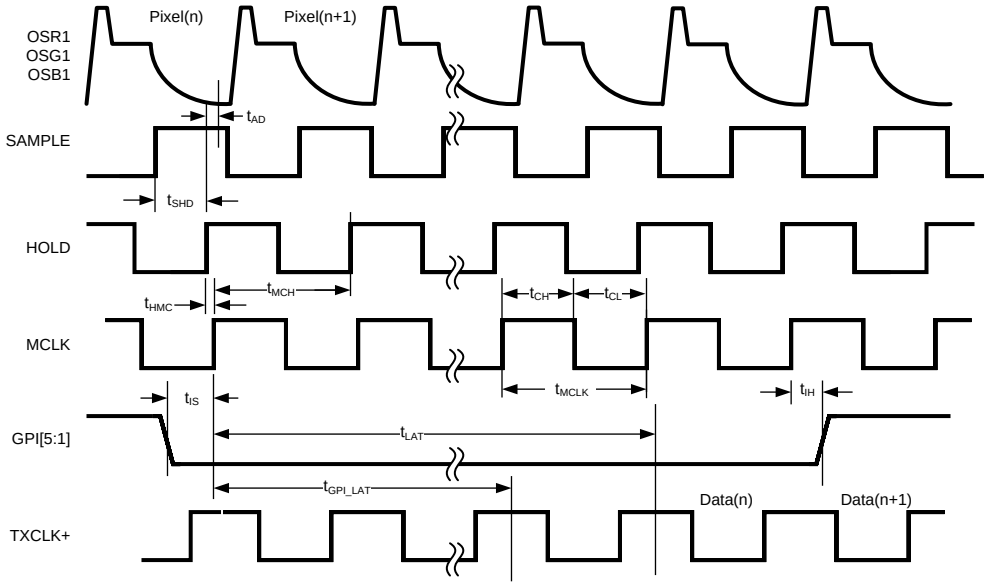


Figure 8. Output Latency and Timing – 3 Channel Mode

6.9 LVDS TIming

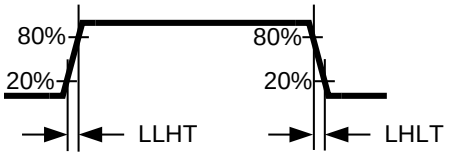
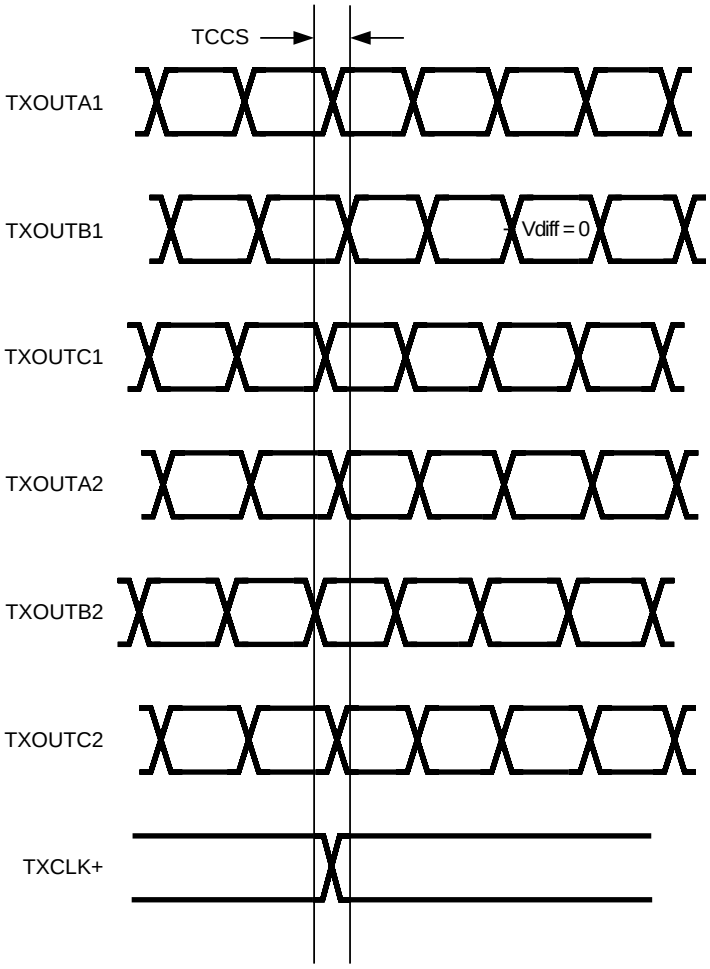


Figure 9. LVDS Transition Times



Measurements at Vdiff = 0V
TCCS measured between earliest and latest LVDS edges and TxCLK Differential Low to High Edge

Figure 10. LVDS Channel to Channel Skew

LVDS TIming (continued)

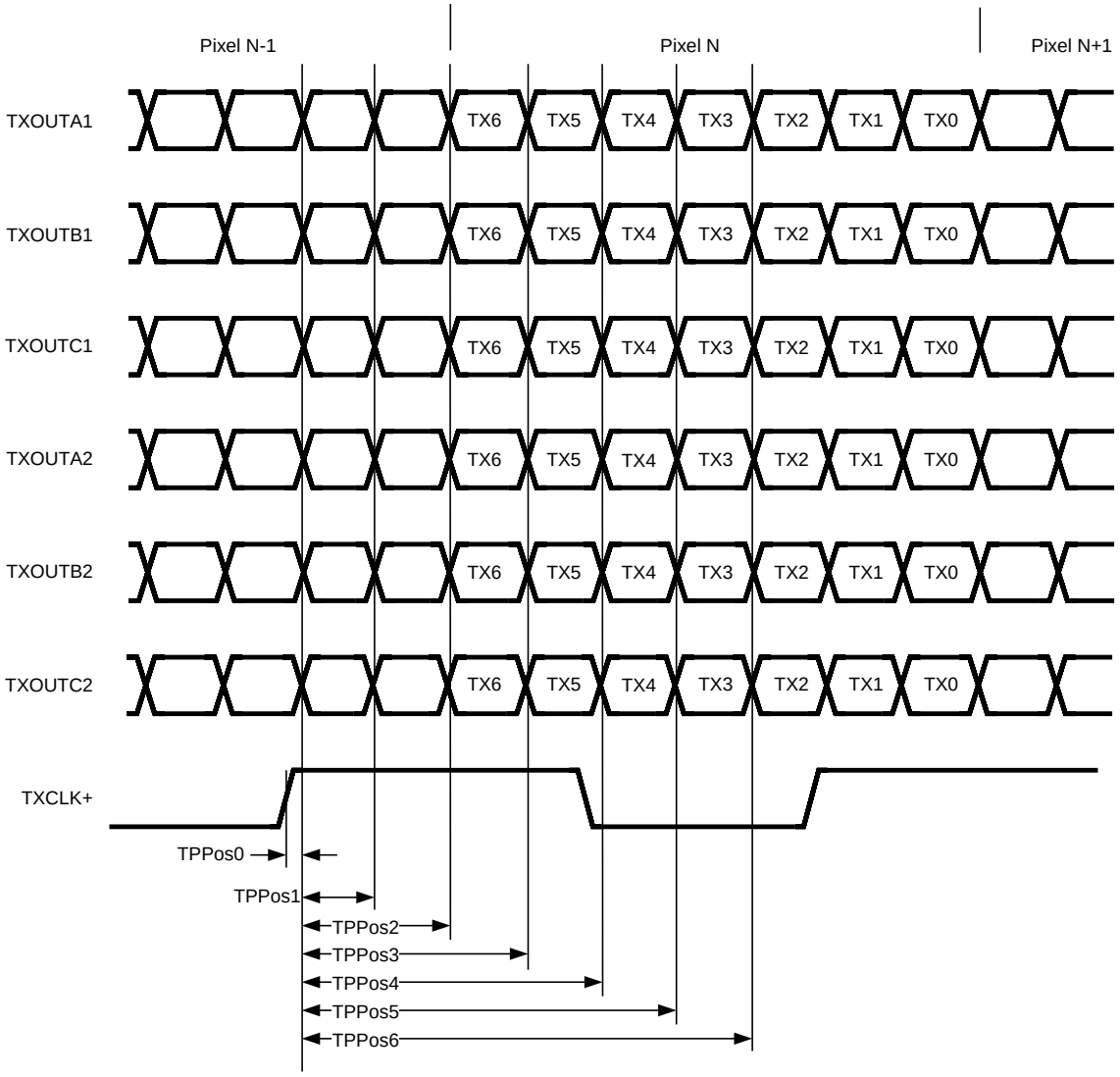
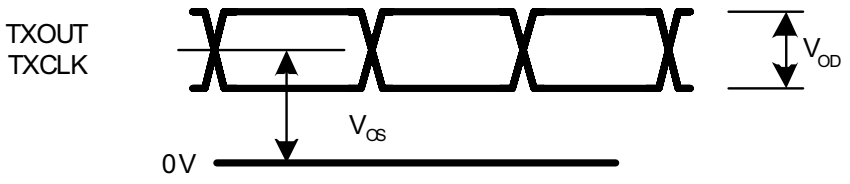


Figure 11. LVDS Output Pulse Positions



Note: LVDS Output Referenced to 0V or VSSLVDS

Figure 12. LVDS DC Parameters

6.10 User Input Based Timing

NOTE

Note: 4 (6 Channel Mode) or 2 (3 Channel Mode) AFEPHASE settings are available to provide flexibility of sample timing.

For ease of use, AFEPHASE = 11 is the default setting in 6 channel mode, and AFEPHASE = X1 is the default setting for 3 channel mode, as shown in select diagrams.

Specified values for these timings are measured at AFEPHASE = 11. For other AFEPHASE settings,these sample input timings will shift earlier with respect to MCLK as follows:

- AFEPHASE = 10 – Earlier by ¼ pixel period
- AFEPHASE = 01 – Earlier by ½ pixel period
- AFEPHASE = 00 – Earlier by ¾ pixel period

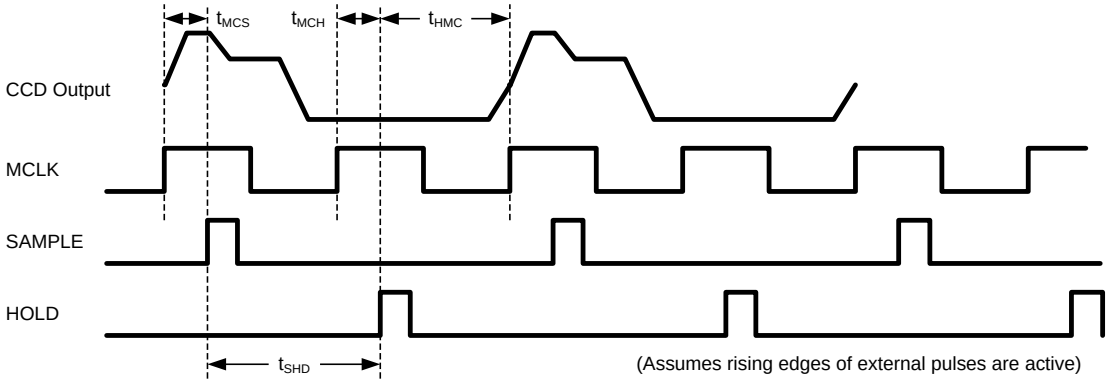


Figure 13. SH3 Timing Mode – ADC Rate Clock Input

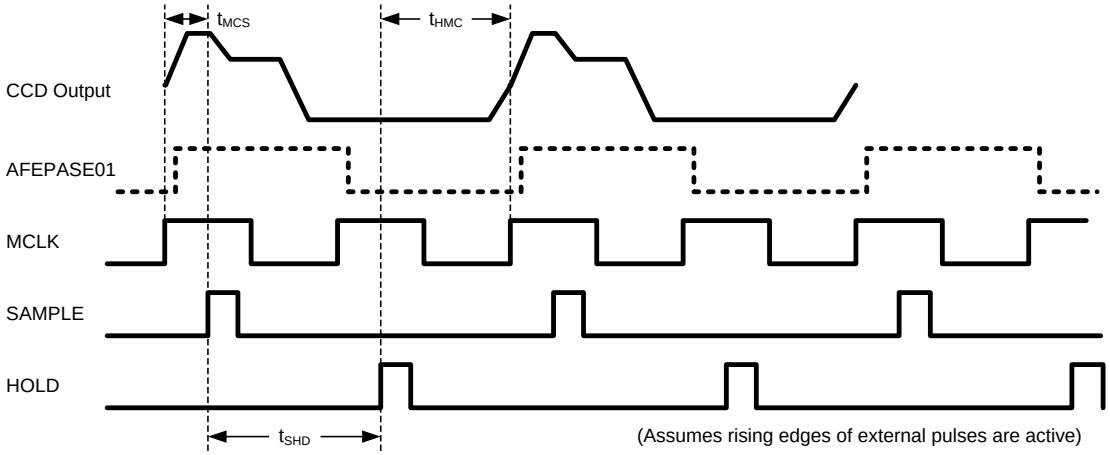


Figure 14. SH2 Timing Mode – ADC Rate Clock Input

User Input Based Timing (continued)

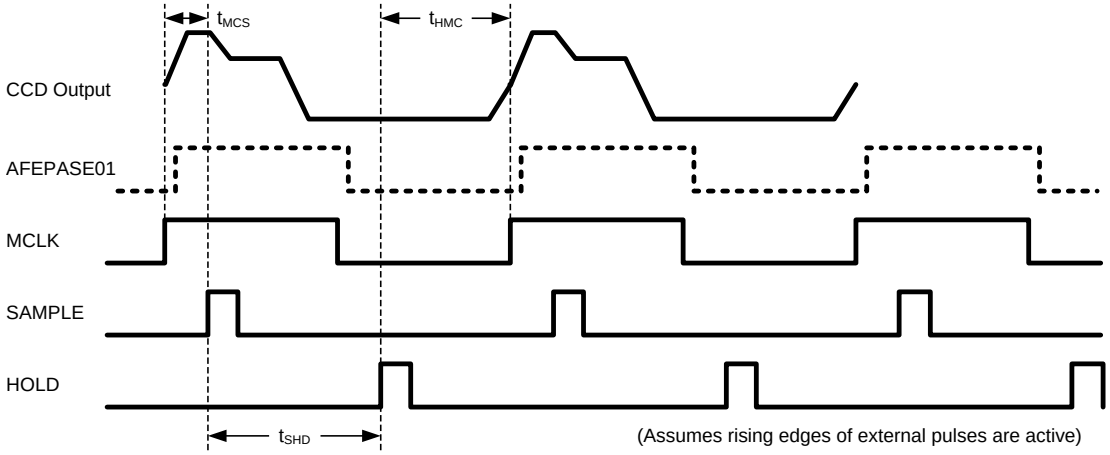


Figure 15. SH2 Timing Mode – Pixel Rate Clock Input

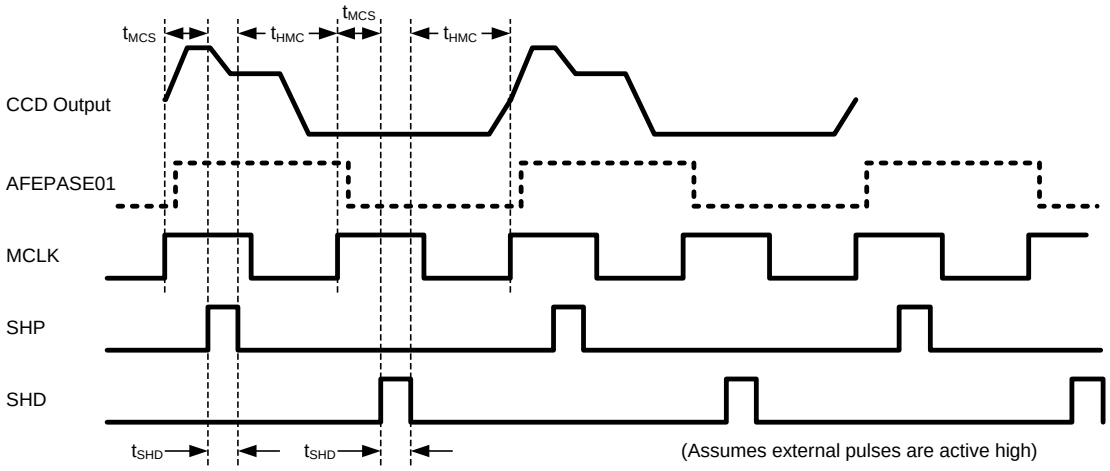


Figure 16. SH1b/CDSb Timing Mode – ADC Rate Clock Input

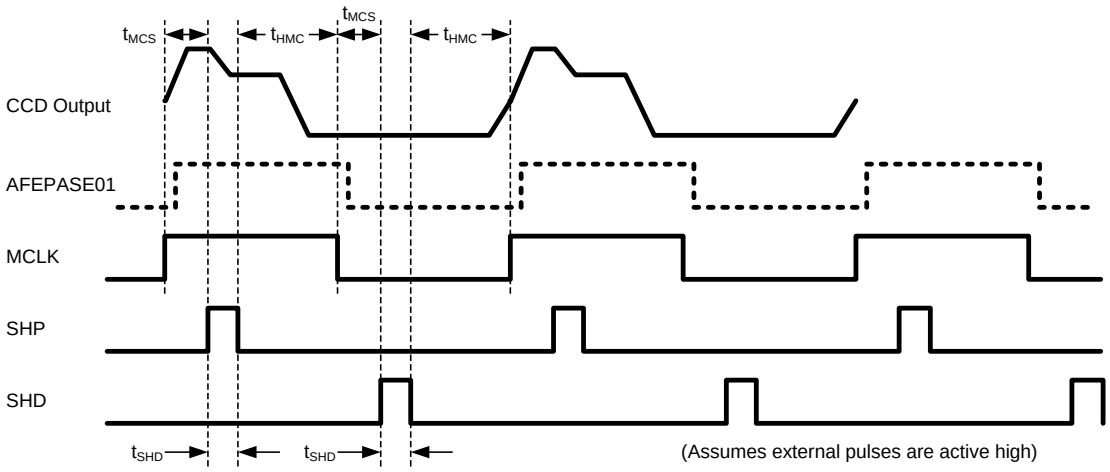


Figure 17. SH1b/CDSb Timing Mode – Pixel Rate Clock Input

7 Detailed Description

7.1 Overview

The PGA and offset DACs for each channel are programmed independently allowing unique values of gain and offset for each of the six channels. A 2-to-1 multiplexing scheme routes the signals to three 70 MHz high performance ADCs. The fully differential processing channels achieve exceptional noise immunity, having a very low noise floor of –68.5dB. The 10-bit analog-to-digital converters have excellent dynamic performance, making the LM98620 transparent in the image reproduction chain.

7.2 Functional Block Diagram

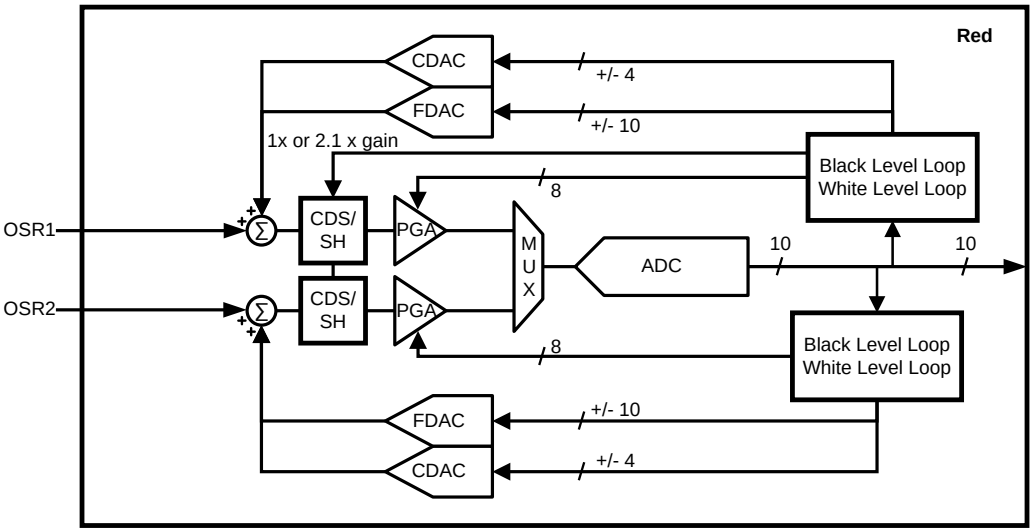


Figure 18. Channel Block Diagram

Functional Block Diagram (continued)

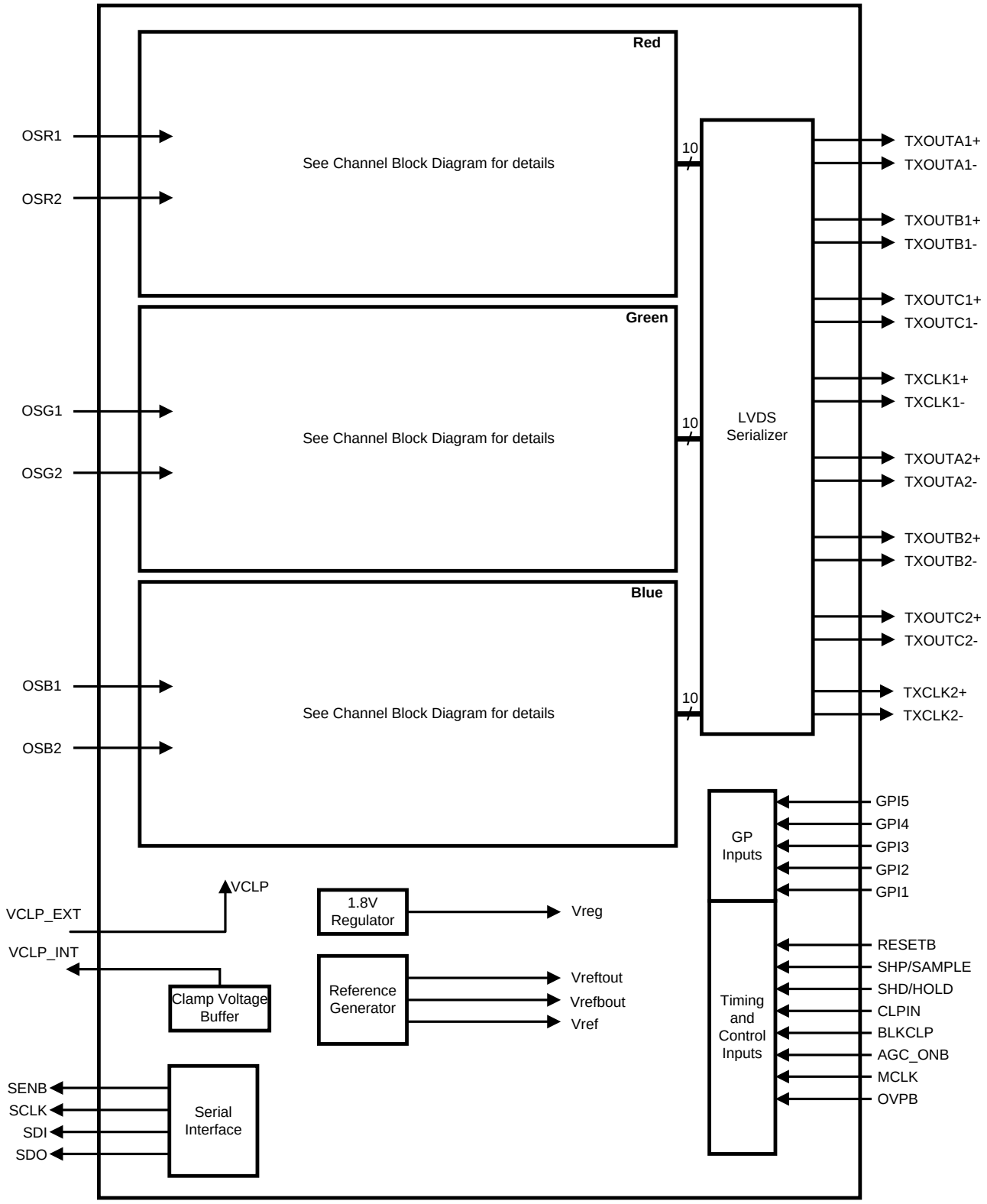


Figure 19. Chip Block Diagram

7.3 Feature Description

7.3.1 Input Clamping and Biasing Circuitry

Many sensor input signals will be at a different common mode voltage than that of the LM98620 input circuitry. In these applications, AC coupling is used to block the DC voltage difference between the source and the AFE inputs. Input clamp circuits are used to set the AFE input at the proper common mode voltage.

Initial coarse clamping should be done using the PIB (Passive Input Bias) and/or AIB (Active Input Bias) circuitry. Setting the PIB enable bit connects 1 kΩ pull-up and pull-down resistors to the inputs to rapidly charge them to $V_{DDA}/2$. Setting the AIB bit connects the VCLPEXT reference voltage to the inputs via low impedance switches. Either method will bring the input voltage very close to the desired level of $V_{DDA}/2$.

The AIB and PIB must be disabled during normal operations.

During image capture, black level clamping is done by connecting the input pins to an internal reference voltage through a low impedance switch. The clamp is turned on periodically to correct any droop in the DC input voltage and minimize conversion errors.

The clamp switch will be turned on during the “Black” portion of the input signal when the input is at a known voltage level. The clamp will connect the inputs to a reference level of approximately 1.65 V. Optionally, a customer supplied reference voltage can be applied at the VCLPEXT pin. If an external reference is used, it must be capable of driving the 6 OS coupling capacitors through 6 internal resistors of 20 Ω. The alternative is to use a weaker buffer, with a large external capacitance (> the sum of the OS coupling capacitors). Clamp timing is controlled by the CLPIN input signal in combination with the register bit ANDen and the internal SAMPLE timing signal.

CLPIN can directly control the internal Clamp, or the combination of CLPIN and SAMPLE can be used. Clamping only during SAMPLE ensures that the input is clamped to the “Black” level rather than the average of “Black”, “Reset” and reset noise feed through signals.

Feature Description (continued)

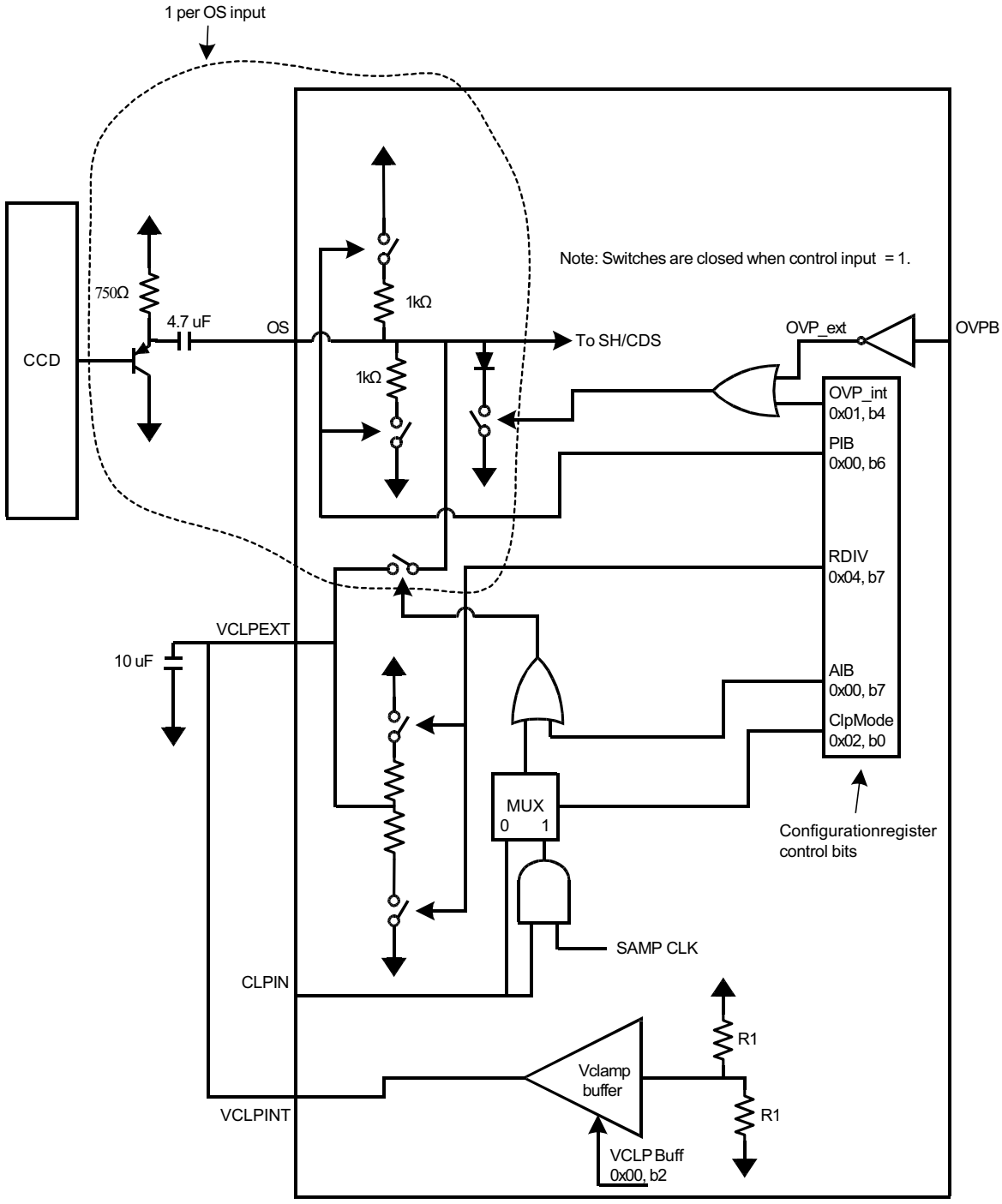
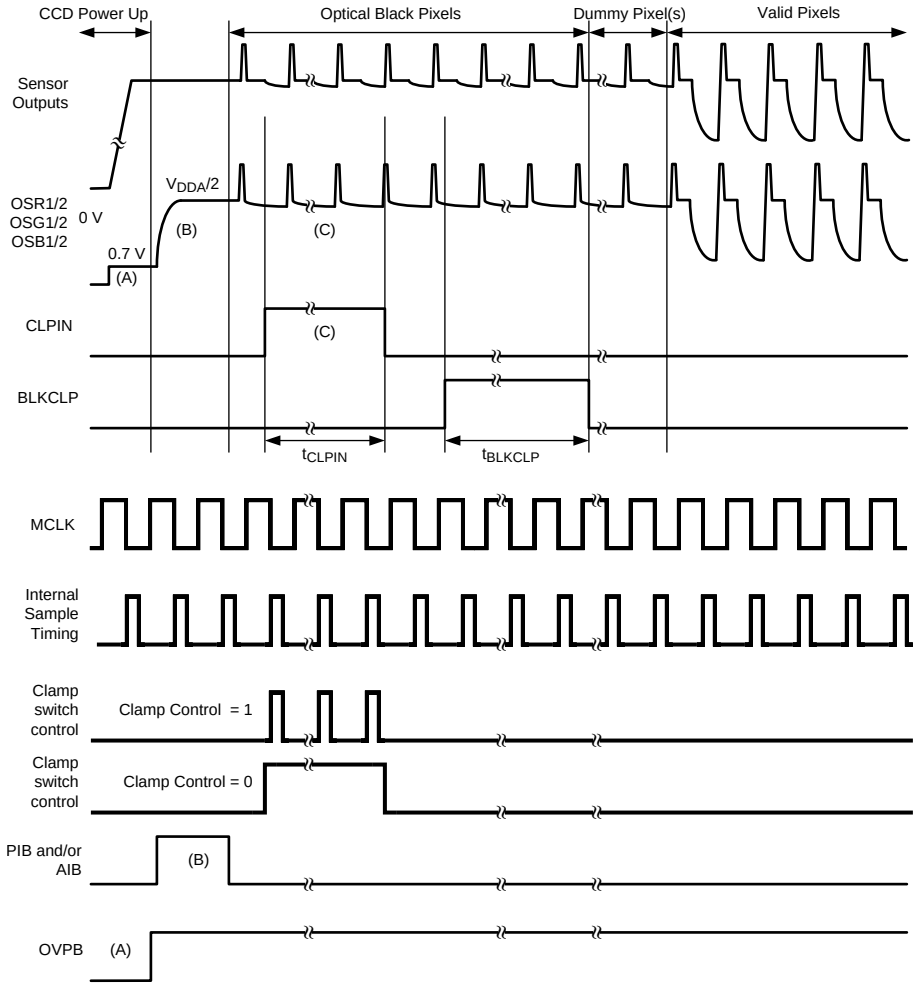


Figure 20. Input Protection and Clamping and Biasing Circuitry

Feature Description (continued)



Note: Waveforms not to scale.

A. During initial system power up, the OVP clamp circuit will be enabled. This provides a path for current to flow as the sensor is powered up, and the large common mode voltage output of the sensor reaches a steady state value. Once the sensor voltages have stabilized, the OVP circuit can be disabled. At this point the OS inputs will still be approximately 0.7 V above ground. Settling to 99% of final voltage will take approximately 18 ms for a 4.7 uF capacitance, assuming a 750 Ω diode/switch impedance.

B. Then, the PIB and/or AIB circuits should be enabled to bring the OS inputs up to approximately VDDA/2 volts. After the OS voltages have charged to this level, the PIB and AIB biasing should be turned off. Settling to within 1mV of VDDA/2 will take approximately 18 ms for a 4.7 uF capacitance, assuming a 500 Ω charging resistance.

C. During image acquisition, accurate DC clamping is provided by the CLPIN switch. This switch is enabled when the CLPIN input is asserted. In most applications, the Clamp Control bit (Register 0x03, b3) should be set to gate the CLPIN signal with the internal sampling pulse. This will ensure that clamping is only done during the image portion of the optical black pixels. Settling to 1mV for a 10mV ΔV between the pedestal and black will take: (1/(%dwell) x 1/(% samp time) x Rsw x Cin x 5).

Settling Time = (1/(32/7600 pixels)) x 1/(50%) x 40 Ω x 4.7 uF x 5 = 447 ms.

Smaller input capacitors will result in proportionally smaller settling times for all clamping modes.

Figure 21. Input Protection Clamping and Biasing – Operation Example

Feature Description (continued)

7.3.2 Input Signal Polarity Select

The LM98620 can accept input signals with negative polarity (default) as output by CCD type sensors, and (when operated in the Sample and Hold modes) can also be configured to accept signals with positive polarity as output by some CIS type sensors.

The input signal polarity selection is found at Page 0, Register 0x03, Bit 7 of the configuration registers. Changing this bit from 0 (default) to 1 selects the positive polarity mode.

*Negative Polarity mode works in both CDS and Sample and Hold modes.

*Positive Polarity mode is only functional in the Sample and Hold modes.

7.3.3 Input Connections for 3 Channel Operation

For three channel only applications, the unused inputs should be connected with 10k Ω resistors to VCLP_EXT to minimize noise coupling into the active inputs.

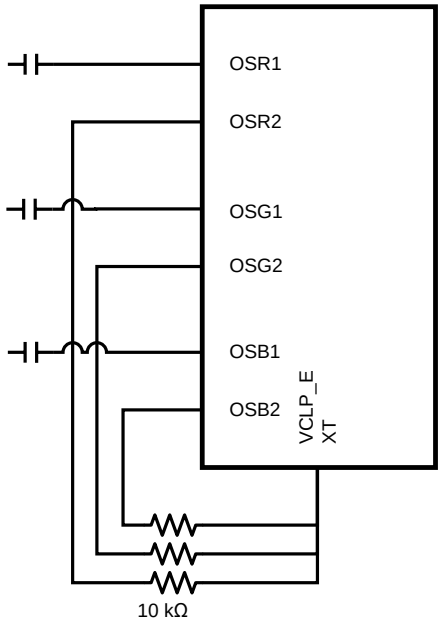


Figure 22. Unused Input Connection

Feature Description (continued)

7.3.4 AFE References

A low noise reference structure is incorporated in the LM98620.

Outputs (VREFTOUT approx. 2.23 V, VREFBOUT approx. 0.98 V) and inputs (VREFTIN1, VREFTIN2, VREFBIN1, VREFBIN2) are provided to allow decoupling capacitors to be connected. VREFTOUT should be connected to VREFTIN1 and VREFTIN2. VREFBOUT should be connected to VREFBIN1 and VREFBIN2. Recommended capacitance is 1.0 uF between the top and bottom reference source, with 0.1 uF to AGND from both the top and bottom reference source. Connection and decoupling capacitor traces should all be as short as possible, and digital signals should be kept away from this area. Internal connections from VREFTOUT to VREFTIN1,2 and VREFBOUT to VREFBIN1,2 are present to reduce the impedance between outputs and inputs, but external connections should still be used for the best performance.

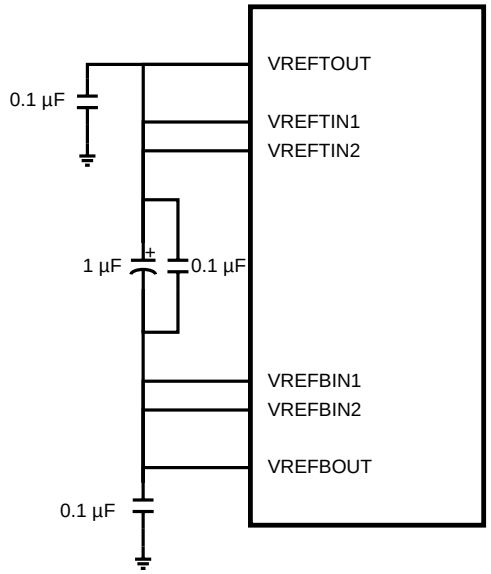


Figure 23. Reference Decoupling Example

7.3.5 Offset Control

Analog offset is provided before the ADC.

Two offset DACs are used to provide a coarse (CDAC) and fine (FDAC) offset that is applied prior to the CDS/SH stage.

- The offset CDAC (Coarse DAC) provides ± 280 mV with ± 4 bits of resolution in offset binary format.
- The offset FDAC (Fine DAC) provides ± 110 mV (Large FDAC range) or ± 59.5 mV (Small FDAC range) with ± 10 bits of resolution in offset binary format. The FDAC range is controlled by the FDAC range bit for each color channel, in Register 0x03h, bits 3, 4, 5.

Table 1. The Offset CDAC and Offset FDAC

CDAC (5bit) OFFSET BINARY FORMAT			FDAC (11 bit) OFFSET BINARY FORMAT			
Hex.	Dec.	Offset Voltage (mV)	Hex.	Dec.	Offset Voltage (mV)	Offset Voltage (mV)
1F	+15	+280	7FF	+1023	110	59.5
11	+1	+18.67	401	+1	0.108	0.058
10	0	0	400	0	0	0
0F	–1	–18.67	3FF	–1	–0.108	–0.058
1	–15	–280	0	–1023	–110	–59.5
0	–16	–280	0	–1024	–110	–59.5

Table 2. CDAC Step Sizes

CDS/SH+PGA Gain	CDAC LSB	ADC LSB
1x	1	16
10x	1	159
20x	1	317

Table 3. FDAC Step Sizes

FDAC Range	CDS/SH+PGA Gain	FDAC LSB	ADC LSB
1x	1x	1	1 / 20
1x	10x	1	1 / 2
1x	20x	1	1
2x	1x	1	1 / 11
2x	10x	1	0.91
2x	20x	1	1.8

7.3.6 Black Level Calibration (Offset)

Black level correction may be performed through one of two available methods: automatic or manual.

7.3.6.1 Manual Offset Adjustment

The manual method is intended for use with processing systems where the desired black level correction loop is external to the LM98620. In this mode the external processor controls the Black Level Offset registers.

Offset adjustment should be done using the average data from multiple Black pixels. The offset will be adjusted to set the Black pixel data as close as possible to the desired target value.

First the CDAC is adjusted until the error is reduced as much as possible given the CDAC step size for the current channel gain. (1 CDAC lsb = (16 to 320) ADC lsb depending on gain). Once the error is minimized with the CDAC, the FDAC is used to further converge the Black pixel data towards the target value.

After changing the channel gain, it may be desirable to repeat the offset adjustment.

7.3.6.2 Automatic Offset Adjustment

Note: During Automatic Offset Adjustment, the CDAC and FDAC register settings are Read Only.

During automatic black level calibration, the CDAC (coarse analog offset DAC) is used to bring the black level as close to the target as possible given the CDAC resolution.

Then the FDAC (Fine analog offset DAC) is applied to further converge the output to the desired black level target.

Two basic modes are available.

- CDAC and FDAC enabled – Used to converge to accurate Black target level as quickly as possible.
- FDAC Only mode – Used to maintain Black target level while avoiding large changes to offset. In FDAC only mode, the CDAC value is fixed, and the automatic adjustments only affect the FDAC.

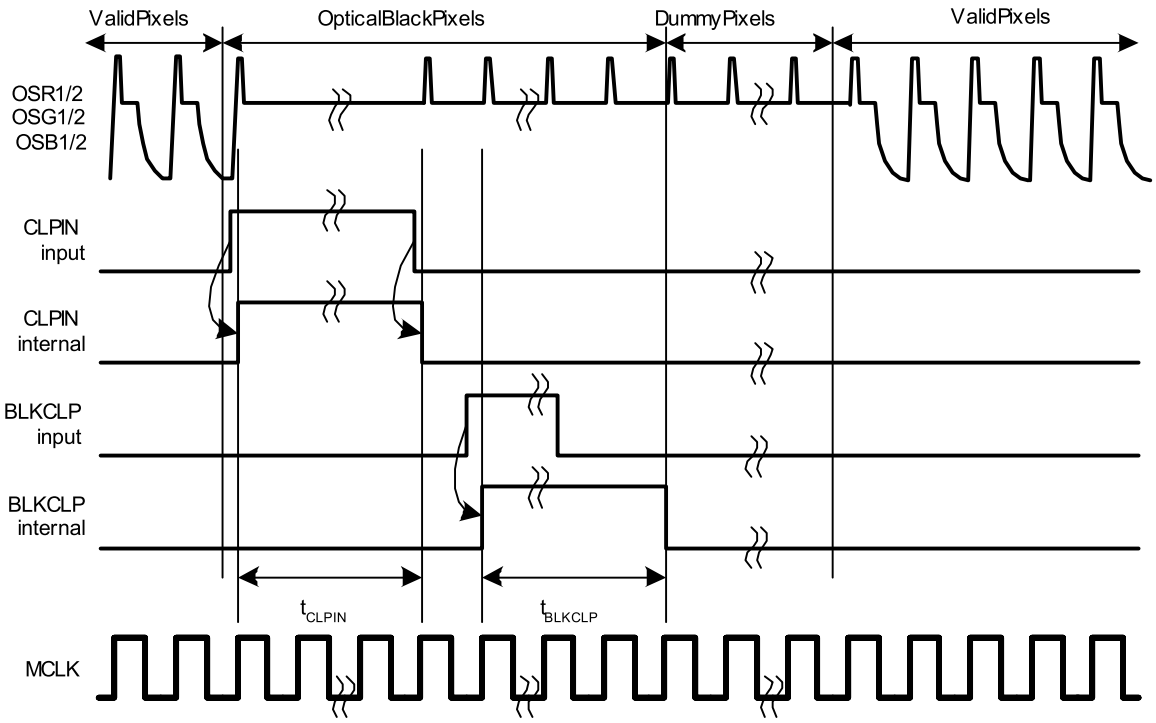
CDAC and FDAC mode should be used to set the gain after power up and between scanning operations. FDAC Only mode should be used during scanning, to prevent large changes in offset from occurring in the image data.

Use of the automatic mode involves enabling the black level offset auto-calibration bit in the black level clamp control register through the serial interface.

The ADC output value is averaged over the programmed number of pixels and subtracted from the desired black level code stored in the target black level register. The result of the subtraction may then be integrated by a preset scaling factor, effectively smoothing any sharp transitions present in the black level signal, before the resulting calculated offset is finally applied. The offset integration scaling factor is stored in the black level loop control register. The integration scaling values range from offset/2 to offset/128.

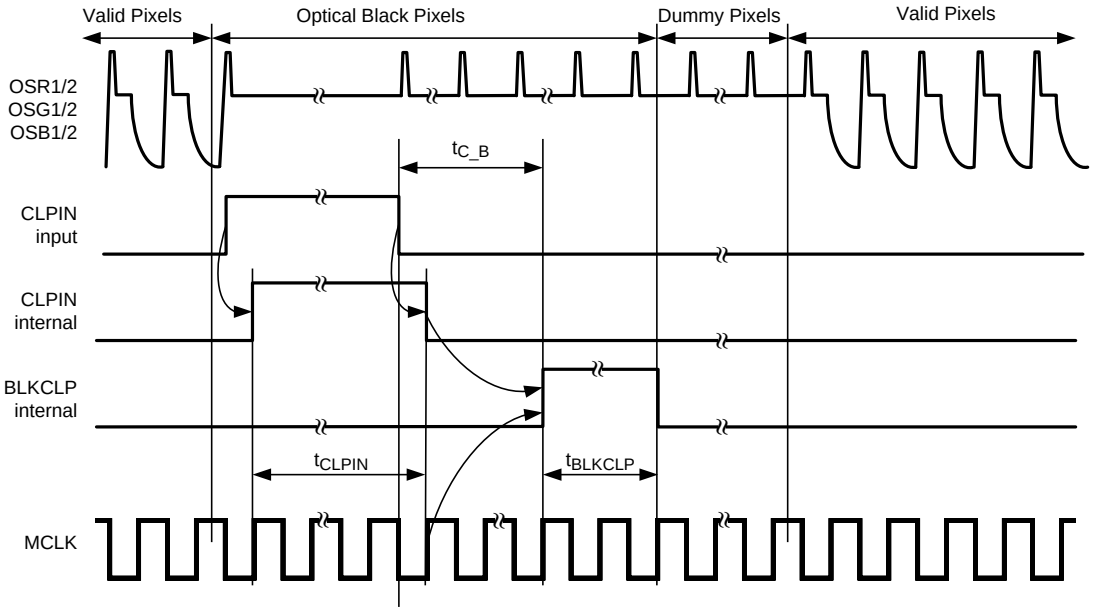
High Speed mode can be enabled to provide rapid initial convergence, with slower, more accurate convergence to the target value. High Speed mode is enabled by setting Register 0x23, Bit 1 = 1. The High Speed Mode offset integration value is set at Register 0x23, Bit 4. Two other parameters control the regions of operation around the target black value. The High Speed Mode Threshold and Hysteresis registers control the points where the transition from High Speed Mode to normal mode is made. When operating in High Speed Mode, the chip will transition to normal mode when Black Error < High Speed Threshold. When operating in Normal Mode, the chip will transition to High Speed Mode when Black Error > (High Speed Threshold + Hysteresis).

In automatic mode, the black level is determined from the ADC output during the Optical Black Pixels. The BLKCLP input pin is used to identify when the black pixels are being input to the IC. The rising edge of the BLKCLP input signal signals the beginning of the Optical Black Pixels. Alternatively, the Auto BLKCLP Pulse Generation (Register 0x23h, Bit 3) can be set to 1 to generate this signal internally. In that case, the BLKCLP pulse will begin 16 (6 channel mode) or 10 (3 channel mode) pixels after the falling edge of the CLPIN signal. Regardless of the source providing the BLKCLP start signal, the BLKCLP pulse duration is controlled by the Pixel Averaging setting in the BLKCLP_CTRL Register (0x24h, Bits 5:3).



NOTE: t_{BLKCLP} is controlled by BLKCLP_CTRL Register (0x24h, Bits 7:3)

Figure 24. Manual BLKCLP Example



Note: t_{BLKCLP} is controlled by BLKCLP_CTRL Register (0x24h, Bits 7:3)

Figure 25. Automatic BLKCLP Example

7.3.7 Gain Control

The PGA provides a range from 1x to 10x gain with 8 bits of resolution. The gain curve is nominally:

Gain = 283/(283-M) (1)

where

- M is the 8 bit gain setting value from 0 to 255.

In addition, the CDS/SH stage provides a 1x or 2x gain, giving an overall channel gain or 1x to 20x (0 dB to 26 dB).

7.3.8 White Level Calibration (AGC - Automatic Gain Control)

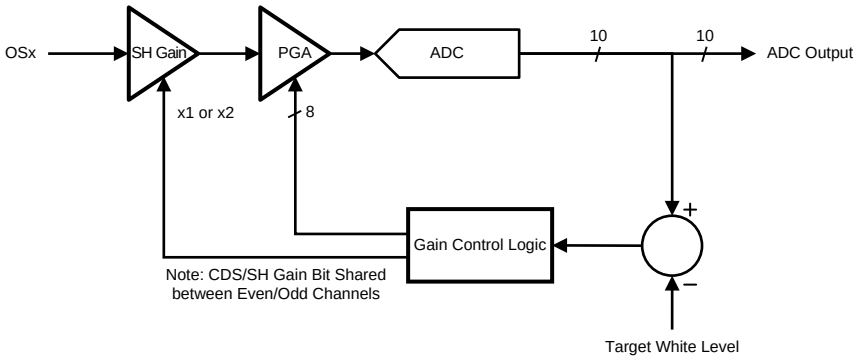


Figure 26. White Level Calibration (AGC - Automatic Gain Control)

During Automatic Gain Adjustment, the PGA and CDS/SH gain settings are Read Only.

The white calibration loop allows the LM98620 to automatically set the gain for the desired maximum ADC output. A digital input pin or configuration register bit is used to start the loop. This would normally be done once per page, or as needed for the particular system design. When triggered, the loop processes the output data during the defined white pixel range. The pixel range can be selected from a minimum of 1 pixel to a maximum of 65535 pixels. The starting pixel can be selected via the PK_DET_ST register at 0x2Ah, 0x2Bh and is referred to the rising edge of either the CLPIN or BLKCLP signal. The number of pixels is selected by the PK_DET_WID register at 0x2Ch, 0x2Dh.

During processing, a moving window average is performed. The size of the window is set by the PK_AVE register at 0x29, Bits 2:0. The window size is adjustable from 1 (no averaging) to 32 pixels. As each window average is calculated, the value is compared to the previous Peak White value (at the start of the line, the initial Peak White value is set to 0). If the new average is larger than the previous Peak White value, the Peak White value is replaced with the new average value. The window position is then incremented by 1 pixel and the process is repeated until the window average has processed all PK_DET_WID pixels.

If the AGC_ONB input is pulsed, the white calibration loop will operate for a fixed number of lines at the beginning of the scan. This duration is selected via the AGCDuration register at 0x2Eh Valid settings are from 1 to 255 decimal. A duration setting of 0 will cause the loop to not run.

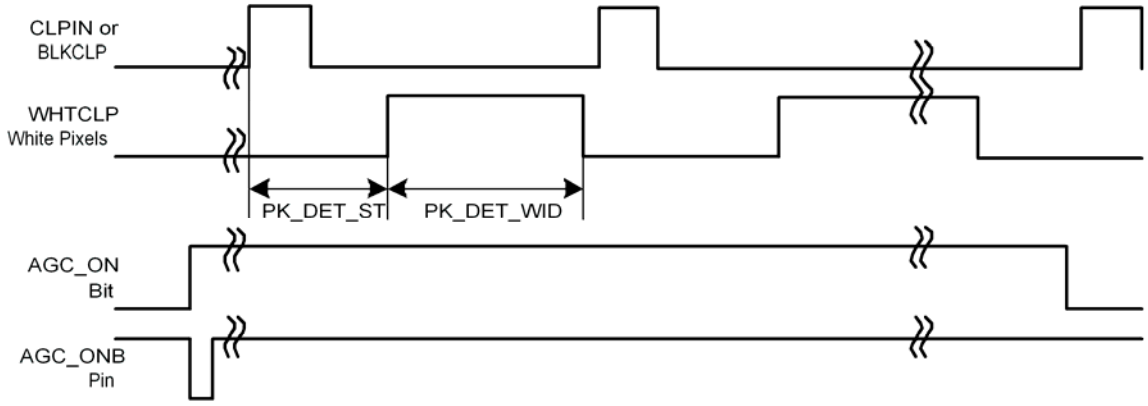


Figure 27. White Calibration Using AGC_ONB

When the AGC_ONB input is pulsed, the register bit AGC_ON is set. The AGC_ON bit is cleared when the loop is terminated, which is when the number of lines allocated for the loop are exhausted. The AGC_ONB pin should be asserted for minimum of two pixels and should be deasserted before the loop is complete and the AGC_ON register bit is cleared.

Register 0x01, Bit 5 selects the polarity of the AGC_ONB input. The default is 0 for active low.

When the AGC loop begins operation, the AGC STATUS at Register 0x33, will be automatically cleared (as long as the serial interface mode bit at Register 0x01, Bit 3 is set to 1, MCLK present). At the end of the AGC loop operation, the AGC STATUS register can be read to check that the loop successfully converged for all channels. The status value should be 0x00 to indicate no Convergence Errors.

While the AGC loop is operating, a timing source is needed to provide a consistent reference point at the beginning of each line of pixels. Register 0x28, Bit 5 is used to select either the CLPIN or BLKCLP as the timing source. If Bit 5 = 0, the timing reference is the rising edge of CLPIN. If Bit 5 = 1, the timing reference is the rising edge of BLKCLP. The register setting PK_DET_ST selects the number of pixel after this timing reference that pixel averaging begins. The register setting PK_DET_WID selects the number of pixels after PK_DET_ST that are processed.

The purpose of the white loop is to find the correct gain setting so the brightest white pixels are at a specific ADC code target. The target value is set in the AGCTargetMSB and AGCTargetLSB registers. The target value is calculated from the register value as shown:

AGC_TARG = 512d + (AGCTargetMSB[7:0]+AGCTargetLSB[7])

Table 4. White Loop Register Initialization

AGCTargetMSB (REGISTER 0x2F)	AGCTargetLSB (REGISTER 0x30)	AGC_TARG BINARY	AGC_TARG DECIMAL
11111111	1	1111111111	1023
11111111	0	1111111110	1022
10000000	1	1100000001	769
10000000	0	1100000000	768
00000000	1	1000000001	513
00000000	0	1000000000	512

7.4 Device Functional Modes

7.4.1 AFEPHASEn Details for SHP/SHD Input Mode

The SHP (sample reference) and SHD (sample signal) inputs are combined with the selected AFEPHASEn signal to generate the internal CLAMP and SAMPLE signals respectively. The SHP signal is ANDed with AFEPHASEn. The SHD signal is ANDed with the inverted AFEPHASEn signal.

The best performance will be achieved by selecting the AFEPHASEn timing that has the high period completely overlapping the SHP input timing, and the low period completely overlapping the SHD timing.

7.4.2 AFEPHASEn Details for SAMPLE and HOLD Input Mode

In Sample/Hold mode, the SAMPLE and HOLD inputs are used. The rising edge of SAMPLE defines the start of the sample control pulse, and the rising edge of HOLD defines the end of the sample control pulse. This sample control pulse is then gated by the low period of the AFEPHASEn signal to generate the resulting SAMPLE signal used internally.

The AFEPHASEn signal which has the low period completely overlapping the sample control pulse will give the best performance.

7.4.3 AFEPHASEn: 6 Channel and 3 Channel Modes

In 6 Channel Mode, there are two full cycles of ADCCLK for each sensor pixel period. This allows the two AFE channels to be multiplexed into the single ADC. In this mode, there are 4 possible AFEPHASEn timings available.

In 3 Channel Mode, there is only one cycle of MCLK and ADCCLK per pixel period. Because of this, there are only 2 choices for AFEPHASEn, as shown in the following diagrams.

7.4.4 LM98620 AFEPHASE Synchronization

There are three main modes of operation for the LM98620

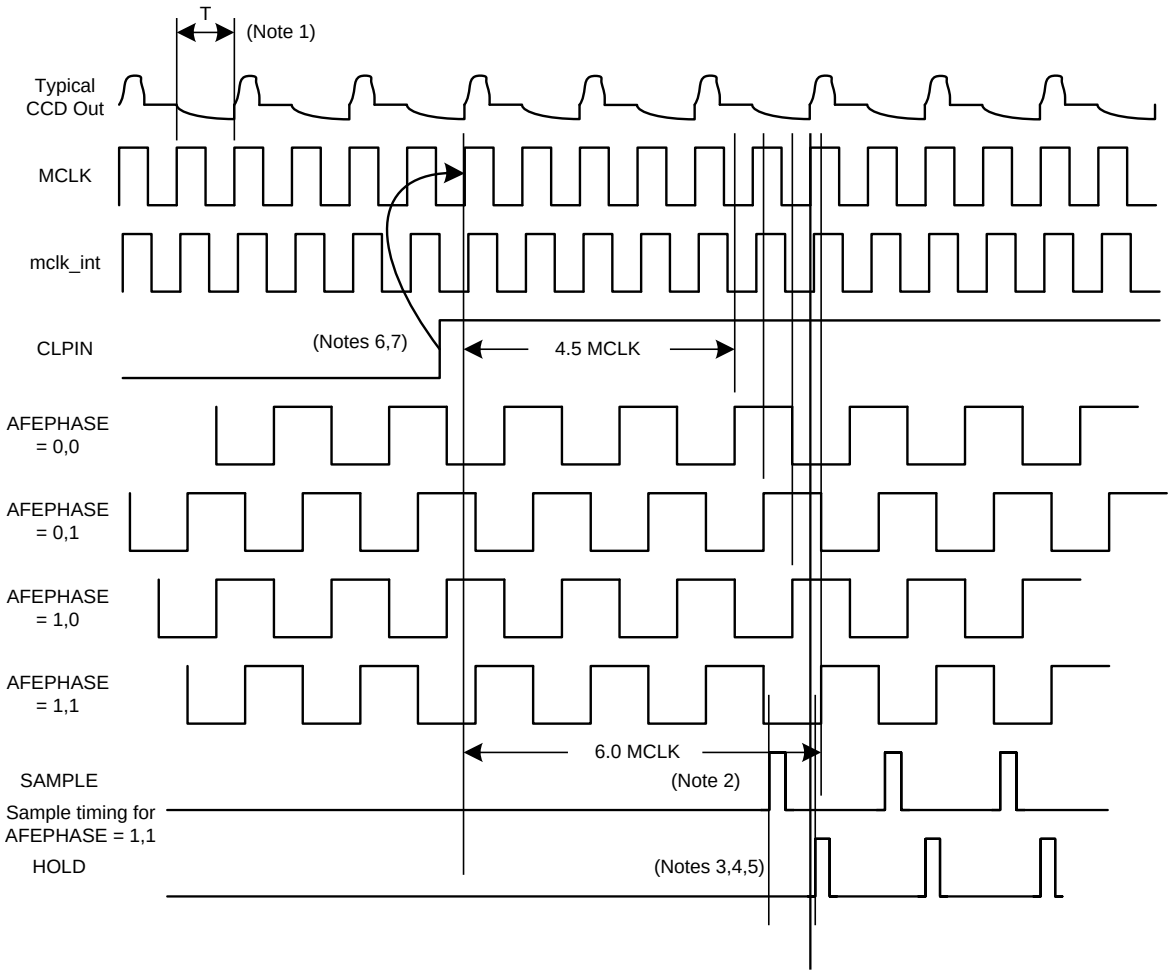
1. 6 channel mode using ADC Rate MCLK – Clock Doubler is bypassed
2. 6 channel mode using Pixel Rate MCLK – Clock Doubler is used
3. 3 channel mode using Pixel Rate MCLK – Clock Doubler is bypassed

In case #1, where an ADC rate (2x of pixel rate) clock is input, the LM98620 needs one additional signal to ensure synchronization between the internal sampling phases and the pixel rate input signal.

This synchronization is done using the CLPIN input signal in combination with MCLK. The CLPIN input generates an internal reset signal that sets the internal AFEPHASE state machine into a known relationship with MCLK and CLPIN. This ensures the AFEPHASE sampling is synchronized to the host sensor timing.

The following diagrams indicate the phase relationship between MCLK and AFEPHASE when CLPIN is used for synchronization:

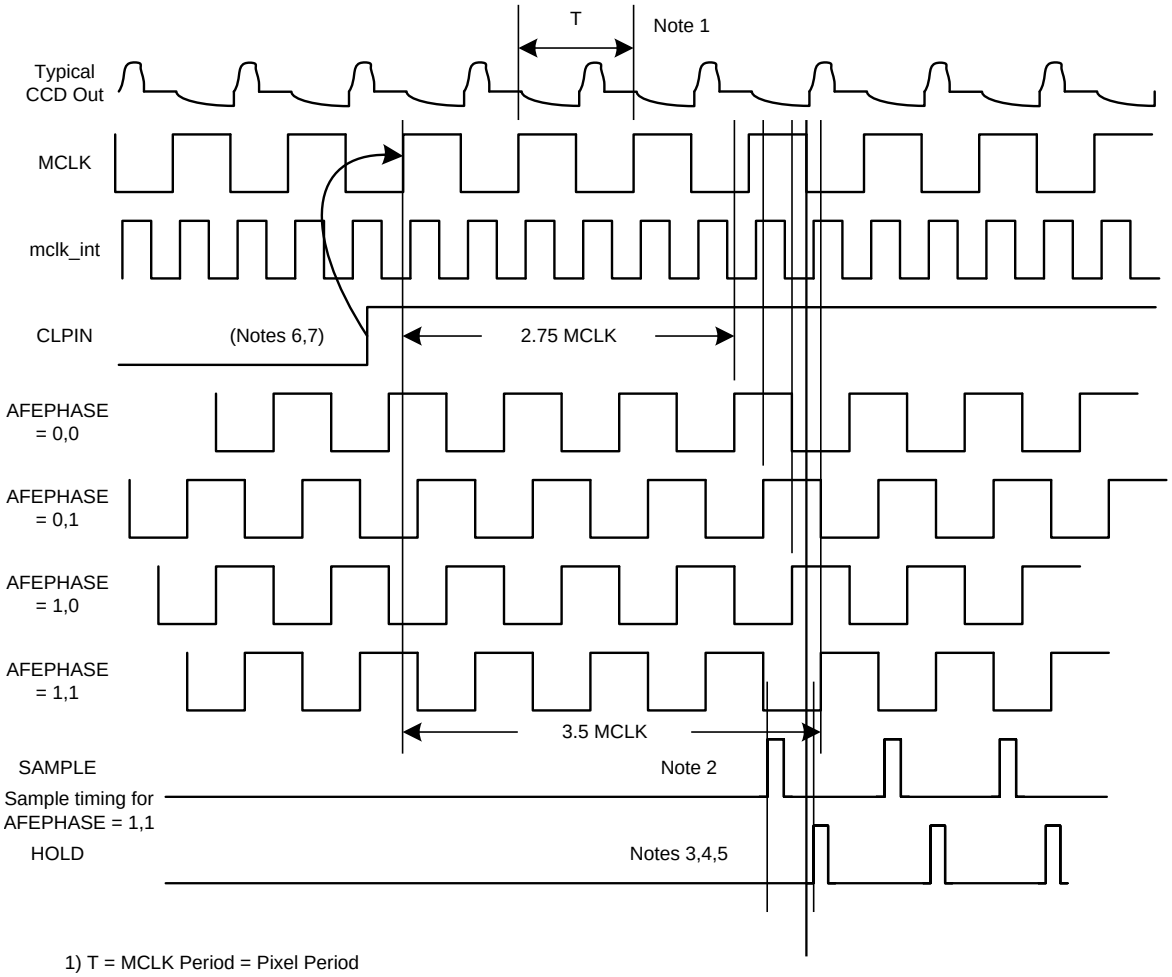
Device Functional Modes (continued)



1) T = MCLK Period = 1/2 Pixel Period
2) Rising edge of SAMPLE must be at least 8 ns before rising edge of HOLD
3) Rising edge of HOLD can be up to t_{MCH} after rising edge of MCLK (AFEPHASE = 1,1)
4) In SH1a,SH1b modes, the rising edge of HOLD can be up to t_{HMC} before the rising edge of MCLK (AFEPHASE = 1,1)
5) In SH2 mode, HOLD can be up to t_{HMC} ns before the rising edge of MCLK (AFEPHASE=1,1)
6) CLPIN must be high or low for at least 2 input MCLK cycles
7) CLPIN is latched by the rising or falling edge of MCLK selectable by Register 0x04h, Bit 5.

Figure 28. 6 Channel Mode – ADC Rate MCLK

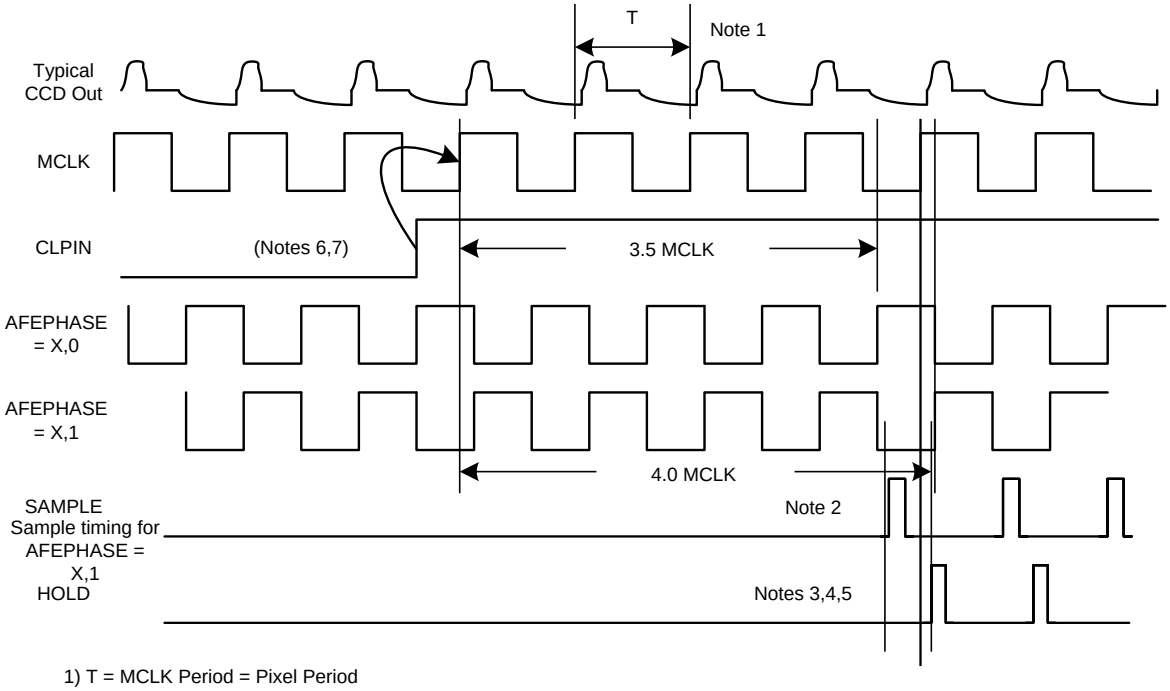
Device Functional Modes (continued)



1) T = MCLK Period = Pixel Period
2) Rising edge of SAMPLE must be at least 8 ns before rising edge of HOLD
3) Rising edge of HOLD can be up to t_{MCH} after falling edge of MCLK (AFEPHASE = 1,1)
4) In SH1a,SH1b modes, the rising edge of HOLD can be up to t_{HMC} before the falling edge of MCLK (AFEPHASE = 1,1)
5) In SH2 mode, HOLD can be up to t_{HMC} before the rising edge of MCLK (AFEPHASE=1,1)
6) CLPIN must be high or low for at least 2 input MCLK cycles
7) CLPIN is latched by the rising or falling edge of MCLK selectable by Register 0x04h, Bit 5.

Figure 29. 6 Channel Mode – Pixel Rate MCLK

Device Functional Modes (continued)



1) T = MCLK Period = Pixel Period
2) Rising edge of SAMPLE must be at least 8 ns before rising edge of HOLD
3) Rising edge of HOLD can be up to t_{MCH} after falling edge of MCLK (AFEPHASE = 1,1)
4) In SH1a,SH1b modes, the rising edge of HOLD can be up to t_{HMC} before the falling edge of MCLK (AFEPHASE = 1,1)
5) In SH2 mode, HOLD can be up to t_{HMC} before the rising edge of MCLK (AFEPHASE=1,1)
6) CLPIN must be high or low for at least 2 input MCLK cycles
7) CLPIN is latched by the rising or falling edge of MCLK selectable by Register 0x04h, Bit 5.

Figure 30. 3 Channel Mode – Pixel = ADC Rate MCLK

7.5 Programming

7.5.1 Using Black Pixel Average

In most applications, the Black Pixel Average bit should be set.

During loop operation, the ADC_MAX or average maximum ADC value is found during the white pixels. The Black Pixel Average value is then subtracted from this ADC_MAX value to find the present white value. This ADC_WHT value is then used for comparison to the target white pixel value TARG_WHT. This is done to eliminate the effects that changes in the system gain will have on the Black Pixel Average value. As gain is increased or decreased, the previously calibrated Black Pixel Average value will change also. When the white loop operation is complete, the gain is set to provide the proper white level referenced to the Black Pixel Average value. Then the Black Loop will be run once more to set the Black Pixel Average at the desired level, and the White level will still be calibrated to the proper level.

In addition, the following registers should be initialized before starting the loop:

Table 5. White Loop Register Initialization

REGISTER	FUNCTION
PK_DET_ST (0x2Ah, 0x2Bh)	Start of the white pixel averaging in pixels from rising edge of CLPIN or BLKCLP
PK_DET_WID (0x2Ch, 0x2Dh)	Number of pixels in each line over which white pixels are averaged
AGCDuration (0x2Eh)	Duration in number of lines the loop should run. If set to 0, the loop will not run. Valid settings are 1 to 255.
AGCTarget (0x2Fh, 0x30h)	AGC target, between 512 to 1023
AGCTolerance (0x31h)	Allowed error margin from the target value
AGC_BLKINT (0x32h)	Black Offset Integration, if used
AGC_CONFIG (0x28h)	Select reference edge CLPIN or BLKCLP rising edge, Enable/Disable AGC_ONB Pin, Incremental Search Enable, Black Offset Enable

After all registers are initialized, the AGC_ON bit (0x28h, b0) can be set, or the AGC_ONB pin can be pulsed to start the white loop.

7.5.2 Sample Timing Control

Sample timing is controlled through the combination of the selected internal AFEPHASEn signal, and programmed internal sample timing signals. Optionally, external sampling timing signals can be applied on the SAMPLE/SHP and HOLD/SHD input pins.

The different input timing modes are selected by bits in Registers 0x00, 0x02, 0x04 and 0x05 as shown in Table 6. Settings other than those shown are not valid:

Table 6. Input Timing Modes

MODE	REG 0x05[7]	REG 0x04[1]	REG 0x02[7]	REG 0x02[3:2]	REG 0x02[1]	REG 0x00[0]	DESCRIPTION
SH3	0	0	1	(See (1))	0	0	Sample and Hold mode, clocked by SAMPLE and HOLD clocks (2)
SH2a	0	1	1		0	0	Sample and Hold mode, clocked by SAMPLE and HOLD clocks (3)
SH2b (Default)	**1**	**1**	**1**		**0**	**0**	**Sample and Hold mode, clocked by DLL (3)**
SH1a	0	1	0		1	0	Sample and Hold mode, clocked by AFEPHASE (3)
SH1b	0	1	1		1	0	Sample and Hold mode, clocked by SHD (3)
CDSa	0	1	0		1	1	CDS mode, sampled by AFEPHASE (3)
CDSb	0	1	1		1	1	CDS mode, sampled by SHP and SHD clocks (3)

(1) AFEPHASE bits should be set to “11” in SH3 mode
(2) AFEPHASE is automatically set by the HOLD input timing
(3) AFEPHASE synchronizes with CLPIN input

7.5.3 DLL Based Sample Timing Settings

The internal DLL settings determine the position of internally generated sampling pulses. These pulses can only be used for the SH2b timing mode. The register bits to select sampling modes are shown in Table 6.

Once SH2b mode is selected, the sample timing settings can be set. The timing settings consist of the following:

AFEPHASE – Register 0x02, Bits 3:2 – This sets the coarse sample timing framework with respect to the input MCLK. In 6 channel modes, there are 4 possible AFEPHASE settings. Each setting is offset from the adjacent ones by ¼ pixel period.

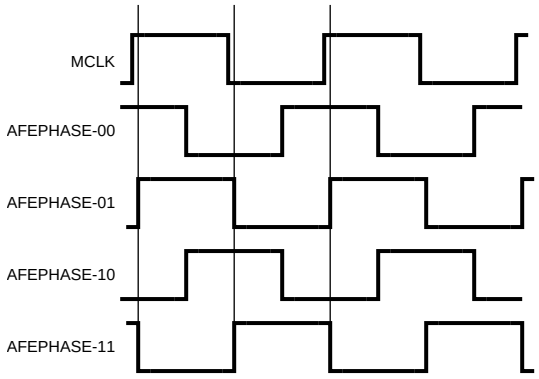


Figure 31. 4 AFEPHASE Selections – Coarse Sample Timing Adjust – (Pixel Rate MCLK Shown)

Sample Trailing Edge Position – Register 0x36, Bits 4:0

This sets the end of the sampling pulse. There are 32 DLL settings within one AFEPHASE cycle or pixel period. The five bit values that correspond to these 32 settings as shown below:

***(Please note that the 5 bit digital code sequence has changed from that of sample silicon versions. Initial version had the MSbit inverted from a normal sequence. A0 silicon has a normal sequence from 00000 to 11111)**

- 00000: delay 0/32 of Tpixel from Pixel Clock
- 00001: delay 1/32 of Tpixel from Pixel Clock
- …
- 01111: delay 15/32 of Tpixel from Pixel Clock
- 10000: delay 16/32 of Tpixel from Pixel Clock
- …
- 11111: delay 31/32 of Tpixel from Pixel Clock

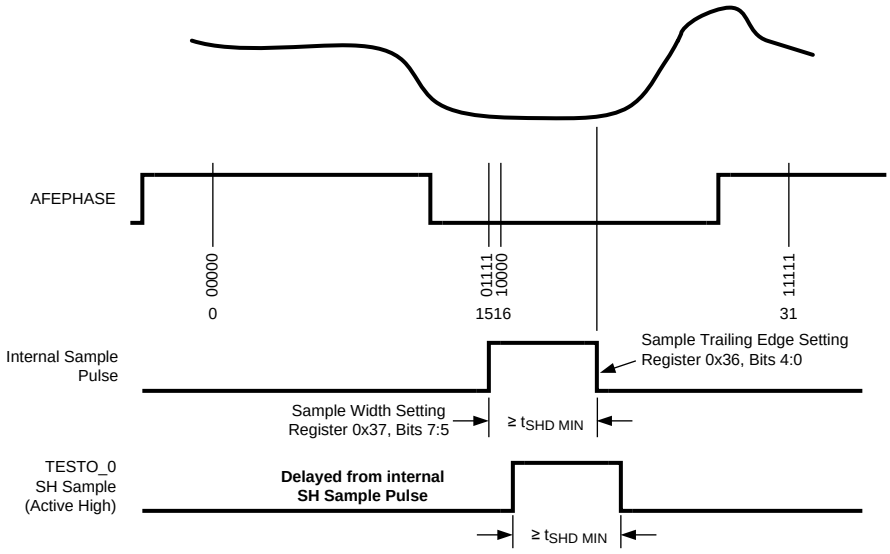


Figure 32. 32 Possible Settings Within AFEPHASE Period

7.5.4 Allowed Range of Sample Trailing Edge Settings (Typical)

NOTE: The 5 bit digital code sequence has changed from that of sample silicon versions

Table 7. Sample Trailing Edge Settings

REGISTER 0x36, Bits 4:0		
F_{ADCCLK}	*MIN	*MAX
70 MHz	12	25
20 MHz	4	29

Sample Width – Register 0x37, Bits 7:5

This selects the width of the Sampling pulse. To achieve rated performance, this parameter must be set to give a minimum of 8 ns width. The proper value can be calculated based on the operating frequency as follows:

Tbit = 1/32 x Tpixel

Min Width Setting = 8ns / Tbit

Min Width Setting = 8ns / (Tpixel/32) = 256 ns / Tpixel ns (rounded up to next even value)

Table 8. Minimum Width Settings

Fpixel (MHz)	Tpixel (ns)	MIN WIDTH SETTING	REGISTER 0x37, BITS 7:5
10	100	4	1
15	66.7	4	1
20	50	6	10
25	40	8	11
30	33.3	8	11
35	28.6	10	100
40	25	12	101

7.5.5 External Sample Timing Inputs

In modes SH1a and CDSa, the internal Sample or Clamp and Sample timing signals are generated from the selected AFEPHASEn signal.

In modes SH1b and CDSb, the input SHD or SHD and SHP signals are ‘gated’ by the internal AFEPHASEn signal to create the internal Sample and Clamp signals.

In mode SH2, the SAMPLE and HOLD timing signals are directly input to the sampling stage of the AFE. Subsequent stages are still clocked by the selected AFEPHASEn and MCLK.

In mode SH3, the SAMPLE and HOLD timing signals are directly input to the sampling stage of the AFE, and **are also used to set the internal AFEPHASE timing for subsequent stages**. In this mode, **CLPIN is not required to set the AFEPHASE timing.**

Please refer to the following timing diagrams to see the recommended relationship between the sample timing inputs and the internal AFEPHASEn signal.

7.5.6 Test Mode Outputs

In test mode, the internal CLAMP and SAMPLE (CDS Mode) or SAMPLE (S/H Mode) timing signals are output on the TESTO_0 and TESTO_1 pins. This enables easy confirmation of the actual internal timing configuration. The TESTO pins are enabled by setting Register 0x00h, Bit 1, = 1. Otherwise these outputs are Tristate.

Table 9 describes the signals present on the TESTO_0 and TESTO_1 outputs in the different timing modes:

Table 9. Test Mode Outputs

SAMPLE MODE	TESTO_0	TESTO_1
SH2a, SH2b, SH3	SH Sample Signal	PGA SampleB (active low)
SH1a, SH1b	SH Sample Signal	SH Sample Signal
CDSa, CDSb	Sample Signal Level	Sample Reference Level

7.5.7 LVDS Data Output

AFE data is output on a serialized LVDS interface. Several different serializing modes are available, with 5 or 6 pairs used for data transfer.

6 pair modes allow the use of the standard, DS90CR218A, or DS90CR364 deserializer ICs.

5 pair modes permit usage with a single 5 channel deserializer. In this mode, the unused data pair can be left open circuit to minimize power consumption and component cost. Also, to maximize layout flexibility, both TXCLK pairs are active. The unused TXCLK pair can be left open circuit to again minimize power consumption.

7.5.8 LVDS Serialization

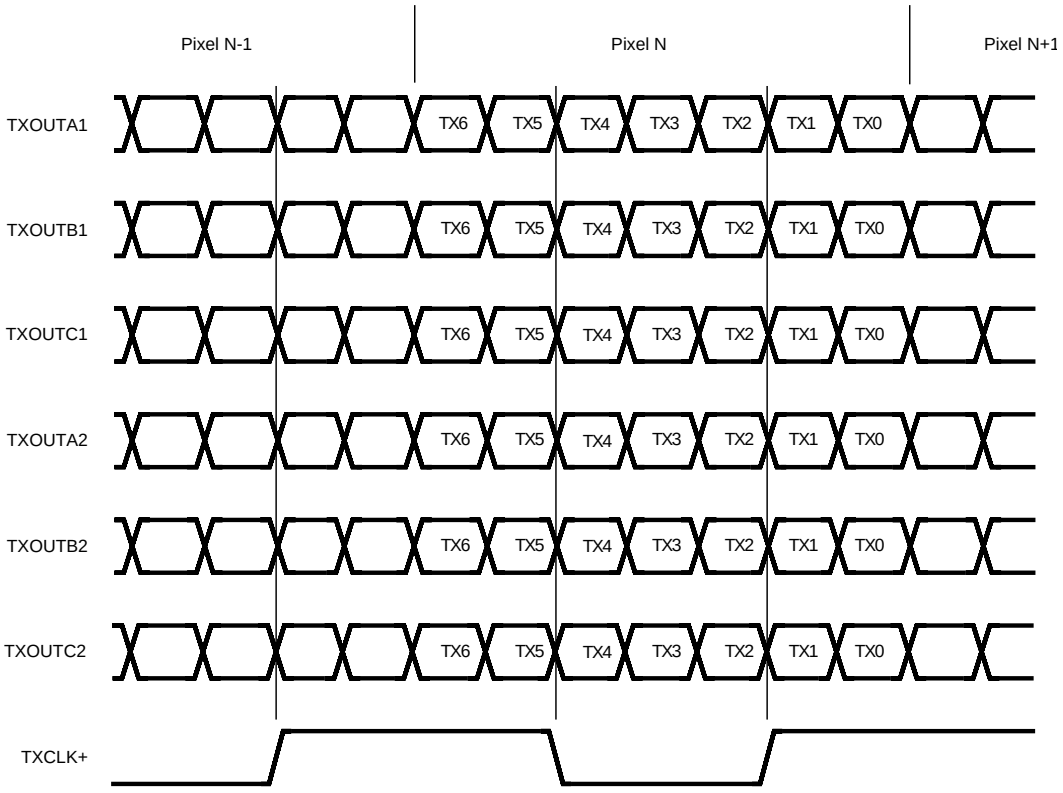


Figure 33. LVDS Serialization

Table 10. Bit Formats

BIT	Tx6	Tx5	Tx4	Tx3	Tx2	Tx1	Tx0
FORMAT 1 R-G-B							
TXOUTA1+/-	0	0	0	0	0	0	0
TXOUTB1+/-	R[4]	R[5]	R[6]	R[7]	R[8]	R[9]	GPI[5]
TXOUTC1+/-	GPI[1]	GPI[2]	GPI[3]	R[0]	R[1]	r[2]	R[3]
TXOUTA2+/-	B[3]	B[4]	B[5]	B[6]	B[7]	B[8]	B[9]
TXOUTB2+/-	G[6]	G[7]	G[8]	G[9]	B[0]	B[1]	B[2]
TXOUTC2+/-	GPI[4]	G[0]	G[1]	G[2]	G[3]	G[4]	G[5]
TXCLK1+/- TXCLK2+/-	1	1	0	0	0	1	1
FORMAT 1 B-G-R	This mode swaps the Red Color and Blue Color data bits.						
TXOUTA1+/-	0	0	0	0	0	0	0
TXOUTB1+/-	B[4]	B[5]	B[6]	B[7]	B[8]	B[9]	GPI[5]
TXOUTC1+/-	GPI[1]	GPI[2]	GPI[3]	B[0]	B[1]	B[2]	B[3]
TXOUTA2+/-	R[3]	R[4]	R[5]	R[6]	R[7]	R[8]	R[9]
TXOUTB2+/-	G[6]	G[7]	G[8]	G[9]	R[0]	R[1]	R[2]
TXOUTC2+/-	GPI[4]	G[0]	G[1]	G[2]	G[3]	G[4]	G[5]
TXCLK1+/- TXCLK2+/-	1	1	0	0	0	1	1
FORMAT 2a R-G-B							
TXOUTA1+/-	0	0	0	0	0	0	0
TXOUTB1+/-	R[3]	R[2]	R[1]	R[0]	GPI[1]	GPI[2]	GPI[3]
TXOUTC1+/-	GPI[5]	R[9]	R[8]	R[7]	R[6]	R[5]	R[4]
TXOUTA2+/-	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	GPI[4]
TXOUTB2+/-	B[2]	B[1]	B[0]	G[9]	G[8]	G[7]	G[6]
TXOUTC2+/-	B[9]	B[8]	B[7]	B[6]	B[5]	B[4]	B[3]
TXCLK1+/-	1	1	0	0	0	1	1
TXCLK2+/-							
FORMAT 2a B-G-R	This mode swaps the Red Color and Blue Color data bits.						
TXOUTA1+/-	0	0	0	0	0	0	0
TXOUTB1+/-	B[3]	B[2]	B[1]	B[0]	GPI[1]	GPI[2]	GPI[3]
TXOUTC1+/-	GPI[5]	B[9]	B[8]	B[7]	B[6]	B[5]	B[4]
TXOUTA2+/-	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	GPI[4]
TXOUTB2+/-	R[2]	R[1]	R[0]	R[9]	G[8]	G[7]	G[6]
TXOUTC2+/-	R[9]	R[8]	R[7]	R[6]	R[5]	R[4]	R[3]
TXCLK1+/- TXCLK2+/-	1	1	0	0	0	1	1
FORMAT 2b R-G-B							
TXOUTA1+/-	R[3]	R[4]	R[5]	R[6]	R[7]	R[8]	R[9]
TXOUTB1+/-	1	1	1	GPI[1]	R[0]	R[1]	R[2]
TXOUTC1+/-	1	1	1	GPI[5]	GPI[4]	GPI[3]	GPI[2]
TXOUTA2+/-	B[3]	B[4]	B[5]	B[6]	B[7]	B[8]	B[9]
TXOUTB2+/-	G[6]	G[7]	G[8]	G[9]	B[0]	B[1]	B[2]
TXOUTC2+/-	GPI[1]	G[0]	G[1]	G[2]	G[3]	G[4]	G[5]
TXCLK1+/- TXCLK2+/-	1	1	0	0	0	1	1

Table 10. Bit Formats (continued)

BIT	Tx6	Tx5	Tx4	Tx3	Tx2	Tx1	Tx0
FORMAT 2b B-G-R	This mode swaps the Red Color and Blue Color data bits.						
TXOUTA1+/-	B[3]	B[4]	B[5]	B[6]	B[7]	B[8]	B[9]
TXOUTB1+/-	1	1	1	GPI[1]	B[0]	B[1]	B[2]
TXOUTC1+/-	1	1	1	GPI[5]	GPI[4]	GPI[3]	GPI[2]
TXOUTA2+/-	R[3]	R[4]	R[5]	R[6]	R[7]	R[8]	R[9]
TXOUTB2+/-	G[6]	G[7]	G[8]	G[9]	R[0]	R[1]	R[2]
TXOUTC2+/-	GPI[1]	G[0]	G[1]	G[2]	G[3]	G[4]	G[5]
TXCLK1+/- TXCLK2+/-	1	1	0	0	0	1	1

7.5.9 Output Data Test Pattern Generation

Special test patterns will be generated to help in testing data processing. Four basic types of waveform can be generated and they are:

- Fixed Pattern
- Horizontal Gradiation Pattern
- Vertical Gradiation Pattern (sub-scan)
- Lattice Pattern

By varying the parameters, waveforms of different timing and amplitude can be created. Parameters for the test patterns are programmable and the following registers are defined:

PK_DET_ST: This register defines the start of the Valid Pixel region from the rising edge of CLPIN or BLKCLP, in Pixels.
*PK_DET_ST = REG_PK_DET_ST + 6, or the register setting value plus 6.

PK_DET_WID: This register defines the duration (pixels) of the Valid Pixel region.

PATSW: Enable/Disable test pattern output.

PATMODE: Sets which test pattern mode is used

00 = Fixed code

01 = Horizontal Gradiation

10 = Vertical Gradiation

11 = Lattice

PATREGSEL: Test pattern can be initiated on a single color or all three colors at the same time. When only one color is selected, the other colors are set to maximum 1023 code.

00 = All colors

01 = Red

10 = Green

11 = Blue

TESTPLVL: Output code 0 to 1023. In Fixed Pattern it is code output during the Valid Pixel range. During Horizontal Gradation and Vertical Gradation it is used as the initial code. In Lattice Pattern it is the level during the Valid Pixel range except for the first pixel every PATW pixels in the horizontal range and for first line every PATW lines.

PATW: Gradation pitch, this is interval at which the pattern Code Step provided in PATS register is applied.

PATS: Pattern Code Step, this contains the code step increment applied every PATW interval.

LINE_INT: Test pattern output delay. This defines the delays in number of lines between Red to Green and Green to Blue. This sequence is fixed, R->G->B, and when this register is 0, all colors switch simultaneously. This delay is used only on the initial start and the sequence of colors is fixed.

7.5.9.1 Fixed Pattern

Outputs fixed code in the TESTPLVL register during Valid Pixel range.

7.5.9.2 Horizontal Gradation

Code in the TESTPLVL is outputted initially in the PATW pixels of the Valid Pixel region, and then code is incremented by PATS value every PATW pixels for the rest of the active region. If the code reaches the maximum (less than or equal to 1023), it is reset to the initial value in TESTPLVL and pattern repeated. Same sequence is repeated for the all the lines.

7.5.9.3 Vertical Gradation

Code in the TESTPLVL is outputted initially in the first PATW lines of the scan and fixed for all of the Valid Pixel region, and then the code is incremented by PATS value every PATW lines and the new code is applied during active region till the next increment. This is repeated till code reaches the maximum (less than or equal to 1023) then the code is reset to the initial value and the sequence repeated.

7.5.9.4 Lattice Pattern

This is combination of Horizontal and Vertical Gradation pattern. Here the register PATW defines interval in pixels for horizontal scan and in lines for the vertical scan. At start of the test the output is set to PATS level for the whole first line and every line at PATW interval. In rest of the lines of the output goes to PATS for the first pixel then goes TESTPLVL for PATW-1 pixels, then goes back to PATS for one pixel and then to TESTPLVL for PATW-1 pixels, the cycle repeats till the end of line.

All test pattern generation continues once initiated by setting of PATSW till it is reset.

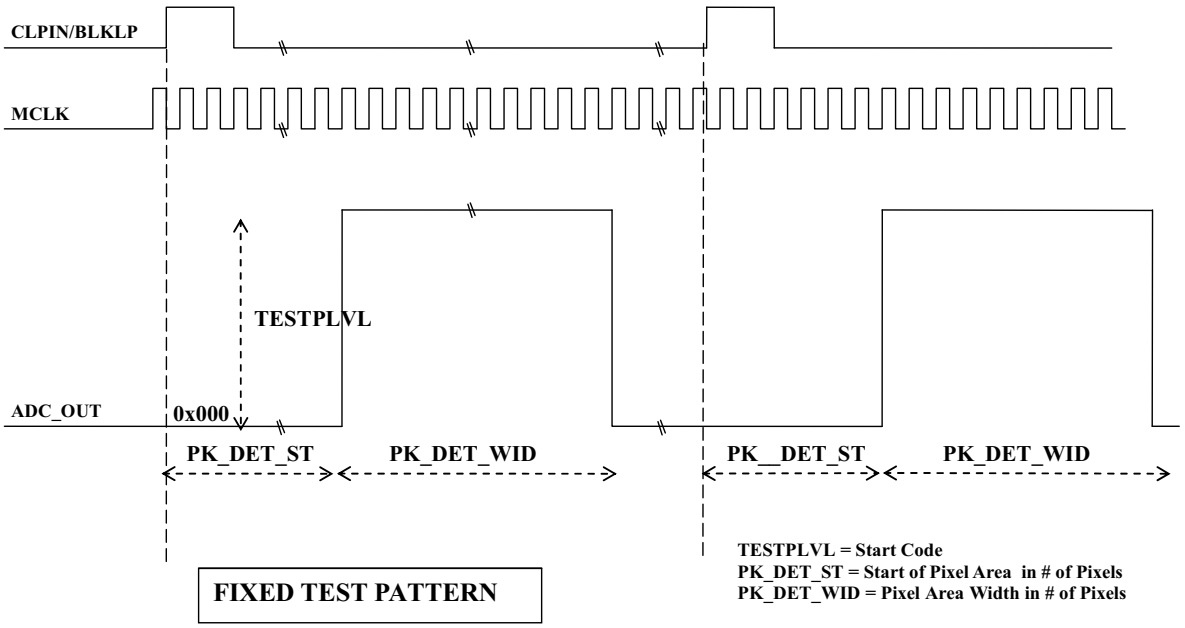


Figure 34. Fixed Test Pattern

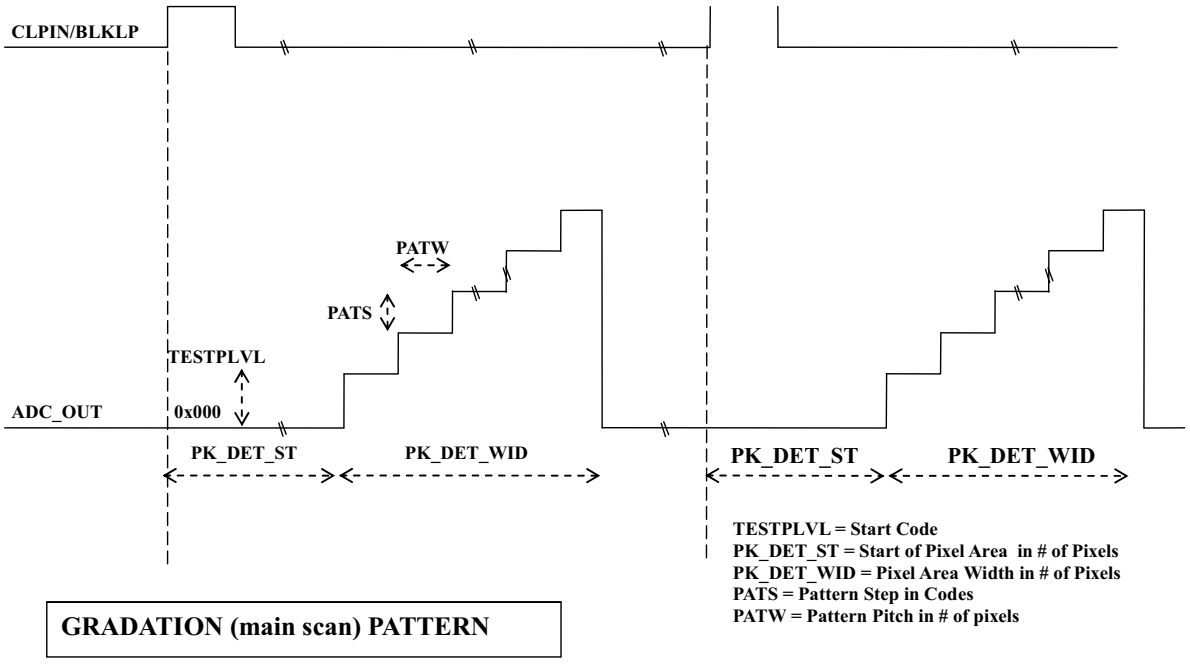


Figure 35. Gradiation (Main Scan) Pattern

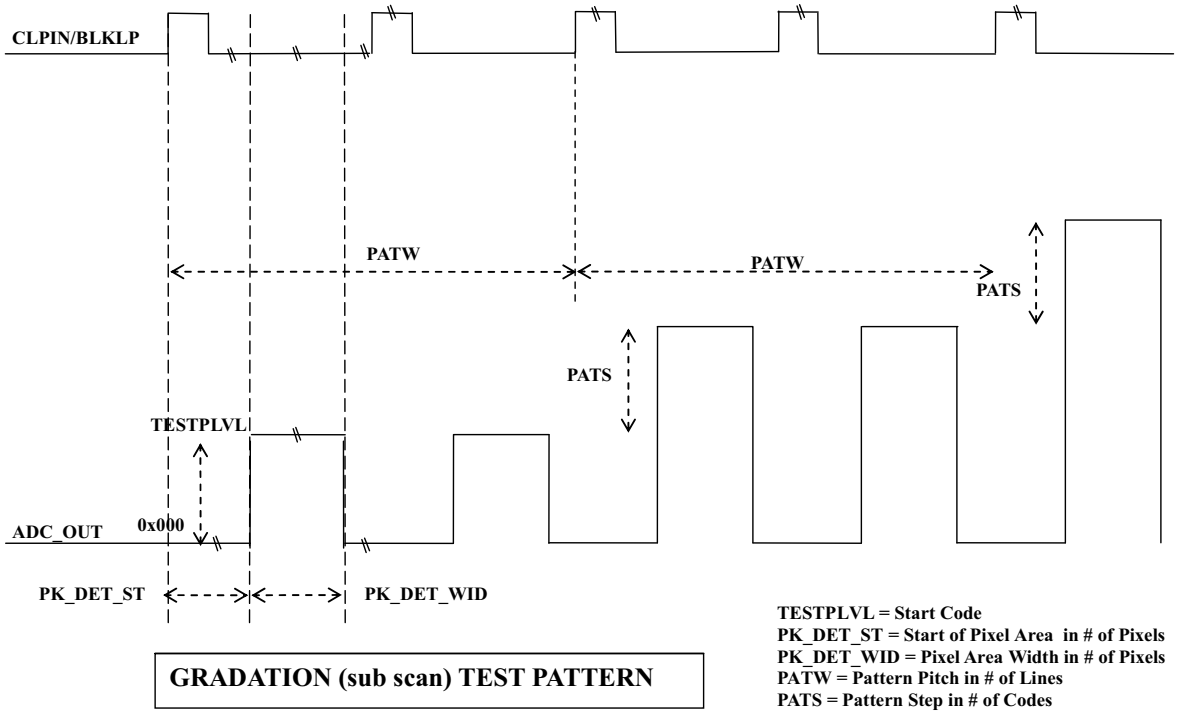


Figure 36. Gradiation (Sub Scan) Pattern

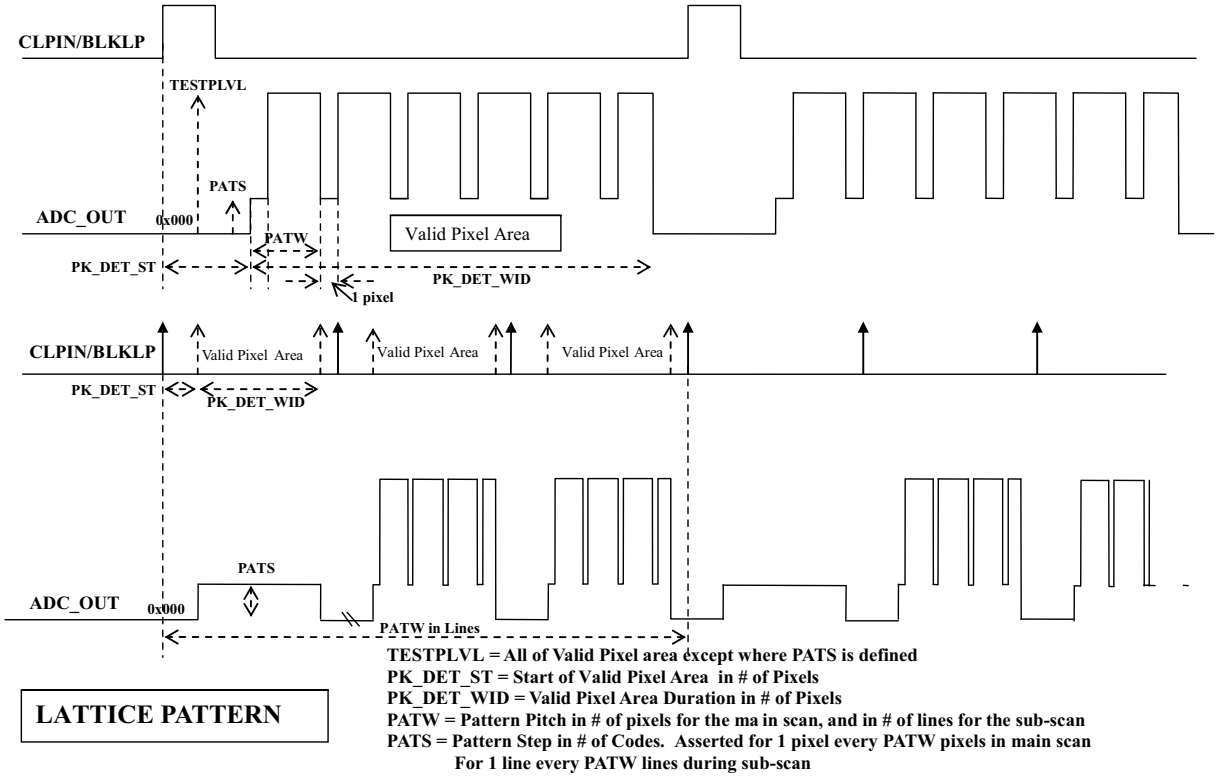


Figure 37. Lattice Pattern

7.5.9.5 Serial Interface

The serial control interface is based on the common Microwire interface with a few specific timing details, as shown below. Bits A5, A4, A3, A2, A1, A0 select the configuration register currently being written to or read within the flat register space.

NOTE

After the device is powered up and a stable MCLK in the range of FMCLK Min to Max is applied, the Serial Interface Mode (Register 0x01, Bit 3) must be set to 1 for Normal Operation.

7.5.9.6 Serial Write

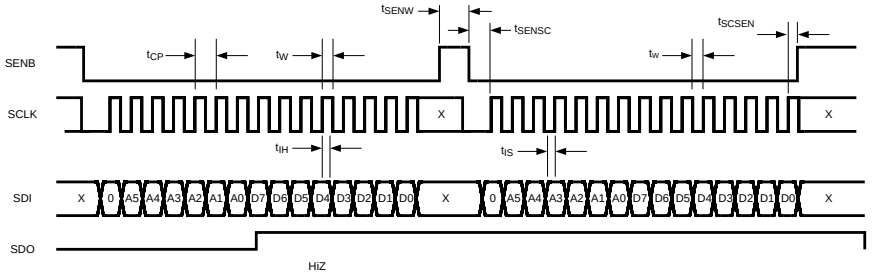


Figure 38. Serial Write

- The positive edge of SCLK is used to receive data on SDI.
- Last 15 bits of data before SEN toggled high will be loaded into AFE.
- A command whose length is less than 15 bits will be discarded.
- SDO will be Hi-Z during write operation.
- At the second cycle shown above, either read or write command is possible.
- The MODE bit must be “0” when writing to registers.
- A Write command consists of one MODE bit, 6 address bits and 8 data bits.
- While SEN is high, the AFE will accept either high or low with respect to SCLK and SDI.

7.5.9.7 Serial Read

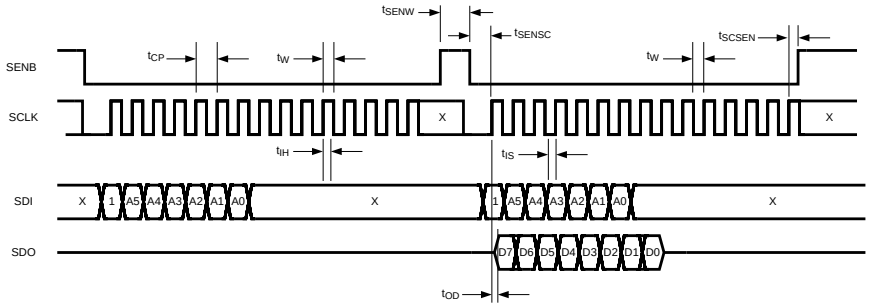


Figure 39. Serial Read

- The positive edge of SCLK is used to receive data on SDI.
- Last 15 bits of data before SEN goes high will be loaded.
- Command whose length is less than 15 bits will be discarded.
- Readout data will appear on SDO at the second cycle above.
- The readout data is clocked at the positive edge of SCLK.
- SDO is Hi-Z except when read out data appears on SDO.
- At the second cycle shown above, either read or write command is possible.
- The MODE bit must be “1” when reading from registers.
- A Read command will contain one MODE bit, 6 address bits and 8 dummy data bits which are ignored.
- While SEN is high, the AFE will accept either high or low with respect to SCLK and SDI.

7.6 Register Maps

Table 11. Configuration Registers Summary Table

HEX ADDRESS (A5-A0)	REGISTER NAME	COMMENTS
0x00 to 0x06	Configuration 0 – 6	Configuration settings
0x07	Device Revision	
0x08	GA_R1	OS_R1 (Red Even) Channel Gain & Offset Registers (CDS / SH Gain is NOT located here)
0x09	C_OFFS_R1	
0x0A	F_OFFS_R1_MSB	
0x0B	F_OFFS_R1_LSB	
0x0C	GA_R2	OS_R2 (Red Odd) Channel Gain & Offset Registers
0x0D	C_OFFS_R2	
0x0E	F_OFFS_R2_MSB	
0x0F	F_OFFS_R2_LSB	
0x10 to 0x13		OS_G1 (Green Even) Channel Gain & Offset Registers
0x14 to 0x17		OS_G2 (Green Odd) Channel Gain & Offset Registers
0x18 to 0x1B		OS_B1 (Blue Even) Channel Gain & Offset Registers
0x1C to 0x1F		OS_B2 (Blue Odd) Channel Gain & Offset Registers
0x20	TARG_BLK_R	
0x21	TARG_BLK_G	
0x22	TARG_BLK_B	
0x23	Black Level Loop Control	
0x24	Black Level Loop Settings	
0x25	CDAC Threshold for BLK LP MSB	
0x25	CDAC Threshold for BLK LP LSB	
0x27	Black Loop Fast Mode	

Register Maps (continued)

Table 11. Configuration Registers Summary Table (continued)

HEX ADDRESS (A5-A0)	REGISTER NAME	COMMENTS
0x28	White Level Loop Control	
0x29	PK_AVG	
0x2A	REG_PK_DET_ST_MSB	
0x2B	REG_PK_DET_ST_LSB	
0x2C	PK_DET_WID_MSB	
0x2D	PK_DET_WID_LSB	
0x2E	AGCDuration	
0x2F	AGCTargetMSB	
0x30	AGCTargetLSB	
0x31	AGCTolerance	
0x32	AGC_BLKINT	
0x33	AGC STATUS	
0x34 to 0x37	TBD	
0x38	Test Pattern Mode	
0x39	Test Pattern Settings 1	
0x3A	Test Pattern Settings 2	
0x3B	PATW	
0x3C	PATS	
0x3D	LINE_INTVL	
0x3E	Reserved	
0x3F	Reserved	

Table 12. Configuration Registers Details

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x00 - 0x07 CONFIGURATION REGISTERS			
0x00	ANLG_CONFG	0x2C	Main Configuration [7] = Active Input Bias (AIB) - Used for initial DC biasing of OS inputs. Disabled during image capture. • (0:Disabled, 1:OSx connected to VREF_EXT during input clamping) [6] = Passive Input Bias (PIB) - Used for initial DC biasing of OS inputs. Disabled during image capture. • (0:Disabled, 1:Osx connected to Vdd/2 resistor ladder during input clamping) [5] = Source Follower Enable - Used to provide higher impedance at OS inputs. Should be enabled for most applications. • (0:Disabled, 1:Enabled) [4] = Analog Power Down • (0:Normal, 1:Powered Down) [3] = Input Mode Select • (0:3-channel; 1:6-channel) • In 3-ch mode, OSR1, OSG1, OSB1 inputs are used. [2] = VCLP Internal Buffer Disable • (0:Enable VCLP Buffer, 1:Disable VCLP Buffer) [1] = Sample Timing Pulses routed to TESTO outputs • (0:Tristate, 1:Enable) • CDSa & CDSb modes: • SH SAMPLE Timing routed to TESTO_0 • SH CLAMP Timing routed to TESTO_1 • SH1a & SH1b modes: • SH SAMPLE Timing routed to TESTO_0 & TESTO_1 • SH2 & SH3 modes: • SH SAMPLE Timing routed to TESTO_0 • PGA SAMPLE Timing routed to TESTO_1 [0] = Sampling Mode Control • See Table 6 in *Sample Timing Control*.
0x01	INTF_CONFG	0x04	Interface Configuration [7:6] – Reserved [5] = AGC_ON pin polarity • 0 = Active LOW, 1= Active HIGH [4] = OVP Input Protection Enable (clamp signal inputs to 1 diode drop) • (0:*Disabled, 1:Enabled) • *Only disabled if OVPB input pin is at logic 1. [3] = Serial Interface Mode – **Note: After the device is powered up and a stable MCLK in the range of FMCLK Min to Max is applied, this value must be set to 1 for Normal Operation.** • (0:Startup-Default, 1:Normal Operation) [2:1] = LVDS output format • 00:Mode 1, 5 pair output • 01:Mode 2a, 5 pair output • 10:Mode 2b, 6 pair output [0] = Red/Blue data swap (0:normal, 1:R/B swapped)

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x02	CLP_CONFG Sample Timing Control	0x9D	Clamp Control [7] = Sampling Mode Control • See Table 6 in *Sample Timing Control*. [6] = SAMPLE edge selection • (0: Rising, 1:Falling) [5] = HOLD edge selection • (0: Rising, 1:Falling) [4] = SHP/SHD input polarity select • (0:Active Low, 1:Active High) [3:2] = AFEPHASEn setting (00 to 11) • (Default is 11 in 6 channel mode) • (Default is X1 in 3 channel mode) Value is 11, but upper bit is ignored in 3 channel mode. [1] = Sampling Mode Control • See Table 6 in *Sample Timing Control*. [0] = Clamp Control • (0:CLPIN input, 1:Clamp gated by internal sampling pulse)
0x03	CDSG_CONFIG CDS / SH Gain Enable FDAC Range Select	0x00	FDAC Range, CDS Gain Selection [7] = Input Signal Polarity • 0: Negative polarity • 1: Positive polarity (Sample and Hold mode only) [6] = Reserved (must be kept at the Power-on-Default value) [5] = Blue Channel FDAC Range Select [4] = Green Channel FDAC Range Select [3] = Red Channel FDAC Range Select • 0: 1 CDAC LSB = 321 FDAC LSBs (Range = ± 64 mV) • 1: 1 CDAC LSB = 176 FDAC LSBs (Range = ±117 mV) [2] = Blue Channels 1 & 2 Gain Enable (0:1x; 1:2.1x-typ) [1] = Green Channels 1 & 2 Gain Enable (0:1x; 1:2.1x-typ) [0] = Red Channels 1 & 2 Gain Enable (0:1x; 1:2.1x-typ)

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x04	Main Configuration 4	0x83	[7] = pbufen (passive buffer enable) • 0: disable resistor divider at VCLP_ext • 1: enable resistor divider at VCLP_ext [6] = pd_ref • Power down VREFT/VREFB buffer only • 0: buffer = power up • 1: buffer = power down [5] = CLPIN Sampling Edge Select • 0: sampled by the rising edge of MCLK • 1: sampled by the falling edge of MCLK [4] = Digital Inputs Sampling Edge Select • 0: sampled by the rising edge of MCLK • 1: sampled by the falling edge of MCLK [3:2] = Clock Range Select (TXCLK and ADCCLK are the same frequency. In 6 channel mode, TXCLK and ADCCLK are 2x the pixel rate.) • 11,10: TXCLK/ADCCLK running at 10MHz – 20MHz • 01: TXCLK/ADCCLK running at 20MHz – 40MHz • 00: TXCLK/ADCCLK running at 40MHz – 65MHz [1] = Sampling Mode Control • See Table 6 in *Sample Timing Control*. for details. • 1: SH3 mode is disabled. • 0: SH3 mode is enabled [0] = clock doubler select • 1: TXCLK and ADCCLK are 2x MCLK • 0: TXCLK and ADCCLK are same freq. as MCLK
0x05	Main Configuration 5	0xF7	[7] = Sampling Mode • 0: Sampling Clocks from SHP/SHD pins • 1: Sampling Clocks from internal DLL [6:0] = Reserved (load with default values)
0x06	SRESET	0x00	Soft Reset [1] – FSM Reset, programmable registers are not disturbed. [0] – REG Reset, reset all FSM, except micro-wire interface, and programmable registers
0x07	Device Revision	0xA0	Read Only. This number reflects the device revision and updated every time any major or minor change is made to the silicon.
0x08 – 0x0F RED CHANNEL PGA GAIN, CDAC and FDAC OFFSETS			
0x08	GA_R1	0x00	[7:0] = Red Channel 1 PGA Gain • Gain = 283/(283 - [7:0]) • Gain range is from 1x to 10x
0x09	C_OFFS_R1	0x10	[4:0] = Red Channel 1 Offset DAC Code • Offset binary format
0x0A	F_OFFS_R1	0x80	[7:0] = Red Channel 1 Fine Offset DAC code [10:3] • Offset binary format
0x0B	F_OFFS_R1 LSB	0x00	[7:5] = Red Channel 1 Fine Offset DAC code [2:0] [4:0] = Reserved
0x0C	GA_R2	0x00	[7:0] = Red Channel 2 PGA Gain • Gain = 283/(283 - [7:0]) • Gain range is from 1x to 10x

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x0D	C_OFFS_R2	0x10	[4:0] = Red Channel 2 Offset DAC Code • Offset binary format
0x0E	F_OFFS_R2	0x80	[7:0] = Red Channel 2 Fine Offset DAC code [10:3] • Offset binary format
0x0F	F_OFFS_R2 LSB	0x00	[7:5] = Red Channel 2 Fine Offset DAC code [2:0] [4:0] = Reserved
0x10 – 0x17 GREEN CHANNEL PGA GAIN, CDAC and FDAC OFFSETS			
0x10	GA_G1	0x00	[7:0] = Green Channel 1 PGA Gain • Gain = 283/(283 - [7:0]) • Gain range is from 1x to 10x
0x11	C_OFFS_G1	0x10	[4:0] = Green Channel 1 Offset DAC Code • Offset binary format
0x12	F_OFFS_G1	0x80	[7:0] = Green Channel 1 Fine Offset DAC code [10:3] • Offset binary format
0x13	F_OFFS_G1 LSB	0x00	[7:5] = Green Channel 1 Fine Offset DAC code [2:0] [4:0] = Reserved
0x14	GA_G2	0x00	[7:0] = Green Channel 2 PGA Gain • Gain = 283/(283 - [7:0]) • Gain range is from 1x to 10x
0x15	C_OFFS_G2	0x10	[4:0] = Green Channel 2 Offset DAC Code • Offset binary format
0x16	F_OFFS_G2	0x80	[7:0] = Green Channel 2 Fine Offset DAC code [10:3] • Offset binary format
0x17	F_OFFS_G2 LSB	0x00	[7:5] = Green Channel 2 Fine Offset DAC code [2:0] [4:0] = Reserved
0x18 – 0x1F BLUE CHANNEL PGA GAIN, CDAC and FDAC OFFSETS			
0x18	GA_B1	0x00	[7:0] = Blue Channel 1 PGA Gain • Gain = 283/(283 - [7:0]) • Gain range is from 1x to 10x
0x19	C_OFFS_B1	0x10	[4:0] = Blue Channel 1 Offset DAC Code • Offset binary format
0x1A	F_OFFS_B1	0x80	[7:0] = Blue Channel 1 Fine Offset DAC code [10:3] • Offset binary format
0x1B	F_OFFS_B1 LSB	0x00	[7:5] = Blue Channel 1 Fine Offset DAC code [2:0] [4:0] = Reserved
0x1C	GA_B2	0x00	[7:0] = Blue Channel 2 PGA Gain • Gain = 283/(283 - [7:0]) • Gain range is from 1x to 10x
0x1D	C_OFFS_B2	0x10	[4:0] = Blue Channel 2 Offset DAC Code • Offset binary format
0x1E	F_OFFS_B2	0x80	[7:0] = Blue Channel 2 Fine Offset DAC code [10:3] • Offset binary format
0x1F	F_OFFS_B2 LSB	0x00	[7:5] = Blue Channel 2 Fine Offset DAC code [2:0] [4:0] = Reserved

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x20 - 0x27 BLACK LEVEL OFFSET CALIBRATION REGISTERS			
0x20	TARG_BLK_R	0x20	[7] = Reserved [6:0] = Target black level – Red Channel
0x21	TARG_BLK_G	0x20	[7] = Reserved [6:0] = Target black level – Green Channel
0x22	TARG_BLK_B	0x20	[7] = Reserved [6:0] = Target black level – Blue Channel
0x23	BLKCLP_CTL0	0x0C	Black Level Loop Control [7:6] = # of lines black clamp compensation applied. • 00 – infinite # of lines (default) • 01 – 16 lines • 10 – 32 lines • 11 – 64 lines [5] = Reserved [4] = High Speed Mode Offset Integration Select • 1: Divide-by-2 • 0: Divide-by-4/3 [3] = Auto BLKCLP Pulse Generation (0:Disable, 1:Enable) [2] = Auto black loop Enable (0:Disable. 1:Enable) [1] = High Speed Mode Enable [0] = Auto black loop mode • 1: Update FDAC offset correction only • 0: Update CDAC and FDAC Offset Corrections

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x24	BLKCLP_CTRL1	0x84	Digital Black Level Clamp Control • [7:3] = Pixel Averaging • 00000 4 pixels • 00001 8 pixels • 00010 12 pixels • 00011 16 pixels • 00100 20 pixels • 00101 24 pixels • 00110 28 pixels • 10000 32 pixels • 10001 64 pixels • 10010 96 pixels • 10011 128 pixels • 10100 160 pixels • 10101 192 pixels • 10110 224 pixels • 10111 256 pixels • 11000 288 pixels • 11001 320 pixels • 11010 352 pixels • 11011 384 pixels • 11100 416 pixels • 11101 448 pixels • 11110 480 pixels • 11111 512 pixels • other combinations are Reserved • [2:0] = Offset Integration • 000:Divide-by-2 • 001:Divide-by-4 • 010:Divide-by-8 • 011:Divide-by-16 • 100:Divide-by-32 • 101:Divide-by-64 • 110:Divide-by-128 • Reserved
0x25	CDAC_THLD_MSB	0x50	CDAC Threshold for BLK LP MSB Default value is 320d, so loop will change FDAC by 320 to compensate for change of 1 in CDAC. [7:0] = Threshold[9:2]
0x26	CDAC_THLD_LSB	0x40	CDAC Threshold for BLK LP LSB [7:6] = Threshold[1:0] [5:0] = Reserved. Set to 0.
0x27	High Speed Mode	0x88	[7:5] = High Speed Mode Hysteresis [4:0] = High Speed Mode Threshold

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x28 – 0x37 WHITE LEVEL GAIN CALIBRATION REGISTERS			
0x28	AGC_CONFG	0x40	[7] = Incremental Search Enable • 0: Binary Search • 1: Incremental Search [6] = Black Offset Enable • 0: Do not Use BLK_AVG during White Level Gain Calibration Loop • 1: Use BLK_AVG as offset during White Level Gain Calibration Loop (Recommended) [5] = CLPIN or BLKCLP White Loop Trigger Select • 0: CLPIN initiates White Loop each line • 1: BLKCLP initiates White Loop each line [4] = AGC_ON pin disable • = 0 Enable use of AGC_ON pin • = 1 Disable use of AGC_ON pin to start white calb. loop [3:1] = Reserved [0] = AGC_ON. Write to 1 to enable White Level Loop. (0:Ready, 1:Enabled) White Loop can also be enabled by asserting AGC_ON pin if pin is enabled via. Register 0x28, b4.
0x29	PK_AVE	0x04	Number of pixels in running average during white calibration loop [2:0] = • 000:No average (1 pixel) • 001:2 pixels • 010:4 pixels • 011:8 pixels • 100:16 pixels • 101:32 pixels
0x2A	REG_PK_DET _ST_M SB	0x00	Starting pixel for peak detection. 16 bit value. Number of pixels after rising edge trigger event. (CLPIN or BLKCLP) (0 to 65535) Actual delay PK_DET_ST = REG_PK_DET_ST + 6
0x2B	REG_PK_DET _ST_L SB	0x00	
0x2C	PK_DET_WID_MSB	0x00	Duration of peak detection after PK_DET_ST. 16 bit value (0 to 65535)
0x2D	PK_DET_WID_LSB	0x00	
0x2E	AGCDuration	0x10	[7:0] = Number of lines for AGC to operate. Loop will run continuously if AGC_ON pin is held high. (0 to 255)
0x2F	AGCTargetMSB	0xE0	[7:0] = MSB of Target Value for AGC loop (Default AGCTarget=960d) AGC_TARG = 512d + (AGCTargetMSB[7:0],AGCTargetLSB[7])
0x30	AGCTargetLSB	0x00	[7] = LSb of Target Value for AGC loop [6:0] = Reserved
0x31	AGCTolerance	0x28	[7:6] = Reserved [5:0] = Allowable error for AGC loop

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x32	AGC_BLKINT	0x00	AGC Offset Integration [2:0] = Offset Integration setting for the Black Level Loop while the AGC is on (that is, white level loop) • 000:Divide-by-2 • 001:Divide-by-4 • 010:Divide-by-8 • 011:Divide-by-16 • 100:Divide-by-32 • 101:Divide-by-64 • 110:Divide-by-128 • Reserved
0x33	AGC STATUS	0x00	AGC Status – Read Only [7:6] = 0 [5] = Convergence Error Blue Ch2 [4] = Convergence Error Blue Ch1 [3] = Convergence Error Green Ch2 [2] = Convergence Error Green Ch1 [1] = Convergence Error Red Ch2 [0] = Convergence Error Red Ch1
0x34	Reserved	0x32	Must be kept with Power-on-default values.
0x35	Reserved	0x54	Must be kept with Power-on-default values.
0x36	DLL Sample Position	0x1F	Must be kept with Power-on-default values. [7:5] Reserved. Set to 000 [4:0] = Sample Pulse Falling Edge Position • [4:0]: delay [4:0]/32 of Tpixel from Pixel Clock • 00000: delay 0/32 of Tpixel from Pixel Clock • 00001: delay 1/32 of Tpixel from Pixel Clock • … • 11111: delay 31/32 of Tpixel from Pixel Clock
0x37	DLL Sample Width	0x60	[7:5] = Sample Pulse Width • 000: 2/32 of Tpixel • 001: 4/32 of Tpixel • 010: 6/32 of Tpixel • 011: 8/32 of Tpixel • 100: 10/32 of Tpixel • 101: 12/32 of Tpixel • 110: 14/32 of Tpixel • 111: 16/32 of Tpixel • [4:0] = Reserved

Table 12. Configuration Registers Details (continued)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x38 to 0x3F USER TEST PATTERNS REGISTERS			
0x38	TEST_PAT_CTL	0x00	Test Pattern Mode [7] = Test Pattern Enable (PATSW) • (0:Normal Data Output, 1:Test Pattern Output Enabled) [6:5] = Test Pattern Mode Select (PTRMODE) • 00:Fixed Code • 01:Gradation Pattern (Main Scanning). • 10:Gradation Pattern (Sub Scanning) • 11:Grid Pattern [4:3] = Test Pattern Output Channel (PTRGBSEL) • 00:All colors • 01:Red (Other color data at 1023d) • 10:Green (Other color data at 1023d) • 11:Blue (Other color data at 1023d) [2:0] = Reserved
0x39	TESTPLVL_MSB	0x00	[7:0] = 8 MSb of fixed output code (TESTPLVL)
0x3A	TESTPLVL_LSB	0x00	[7:6] = 2 LSb of fixed output code (TESTPLVL)
0x3B	PATW	0x00	[7:0] = Gradation Pattern Pitch (0 to 255 lines)
0x3C	PATS	0x00	[7:0] = Gradation Pattern Increment Step (0 to 255)
0x3D	LINE_INTVL	0x00	[3:0] = Test Pattern Output Color Delay, Red to Green, Green to Blue (0 to 15 line delay)
0x3E	Reserved		
0x3F	PAGE_SEL for Page Control	0x00	Select Register Pages • 0x00: Page 0 • 0x80: Page 128 (DLL features)

Table 13. DLL Configuration Registers Summary Table

HEX ADDRESS (A5-A0)	REGISTER NAME	COMMENTS
0x00	OS_R1 Sample Falling Edge Position	
0x01	OS_R2 Sample Falling Edge Position	
0x02	OS_G1 Sample Falling Edge Position	
0x03	OS_G2 Sample Falling Edge Position	
0x04	OS_B1 Sample Falling Edge Position	
0x05	OS_B2 Sample Falling Edge Position	
0x06	Reserved	
0x07	Reserved	
0x08	Reserved	
0x09	Reserved	
0x0A	Reserved	
0x0B	Reserved	
0x0C	Reserved	
0x0D	Reserved	
0x0E	Reserved	
0x0F	Reserved	
0x10 - 0x3E	Reserved	
0x3F	Page Select	

Table 14. DLL Configuration Registers Details (Page 128)

ADDRESS (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x00 - 0x07 SAMPLE FALLING EDGE POSITION REGISTERS			
0x00	OS_R1 Sample Falling Edge Position	0x1F	[7:5] = Reserved [4:0] = OS_R1 Sample Falling Edge Position • [4:0]: delay [4:0]/32 of Tpixel from Pixel Clock • 00000: delay 0/32 of Tpixel from Pixel Clock • 00001: delay 1/32 of Tpixel from Pixel Clock • … • 11111: delay 31/32 of Tpixel from Pixel Clock
0x01	OS_R2 Sample Falling Edge Position	0x1F	Same as OS_R1
0x02	OS_G1 Sample Falling Edge Position	0x1F	Same as OS_R1
0x03	OS_G2 Sample Falling Edge Position	0x1F	Same as OS_R1
0x04	OS_B1 Sample Falling Edge Position	0x1F	Same as OS_R1
0x05	OS_B2 Sample Falling Edge Position	0x1F	Same as OS_R1
0x06	Reserved		
0x07	Reserved		
0x08	Reserved		
0x09	Reserved		
0x0A	Reserved		
0x0B	Reserved		
0x0C	Reserved		
0x0D	Reserved		
0x0E	Reserved		
0x0F	Reserved		
0x10 – 0x3E	Reserved		
0x3F	PAGE_SEL for Page Control	0x00	Select Register Pages • 0x00: Page 0 • 0x80: Page 128 (DLL features)

8 Applications and Implementation

8.1 Application Information

The white loop provides two different techniques for converging to the target value, Binary Search, and Incremental Search.

The Binary Search algorithm is intended to provide a rapid convergence to the target value. During initial operation, large changes in the channel gain are allowed. After each line, the allowed change is reduced significantly. For final convergence, the algorithm switches to the Incremental Search mode, to achieve low error.

The Incremental or Linear Search algorithm is intended to provide a low error, but will converge more slowly than the Binary method. The changes (if any) in channel gain are always done in 1 lsb increments to provide low overshoot and high accuracy of convergence.

8.2 Typical Applications

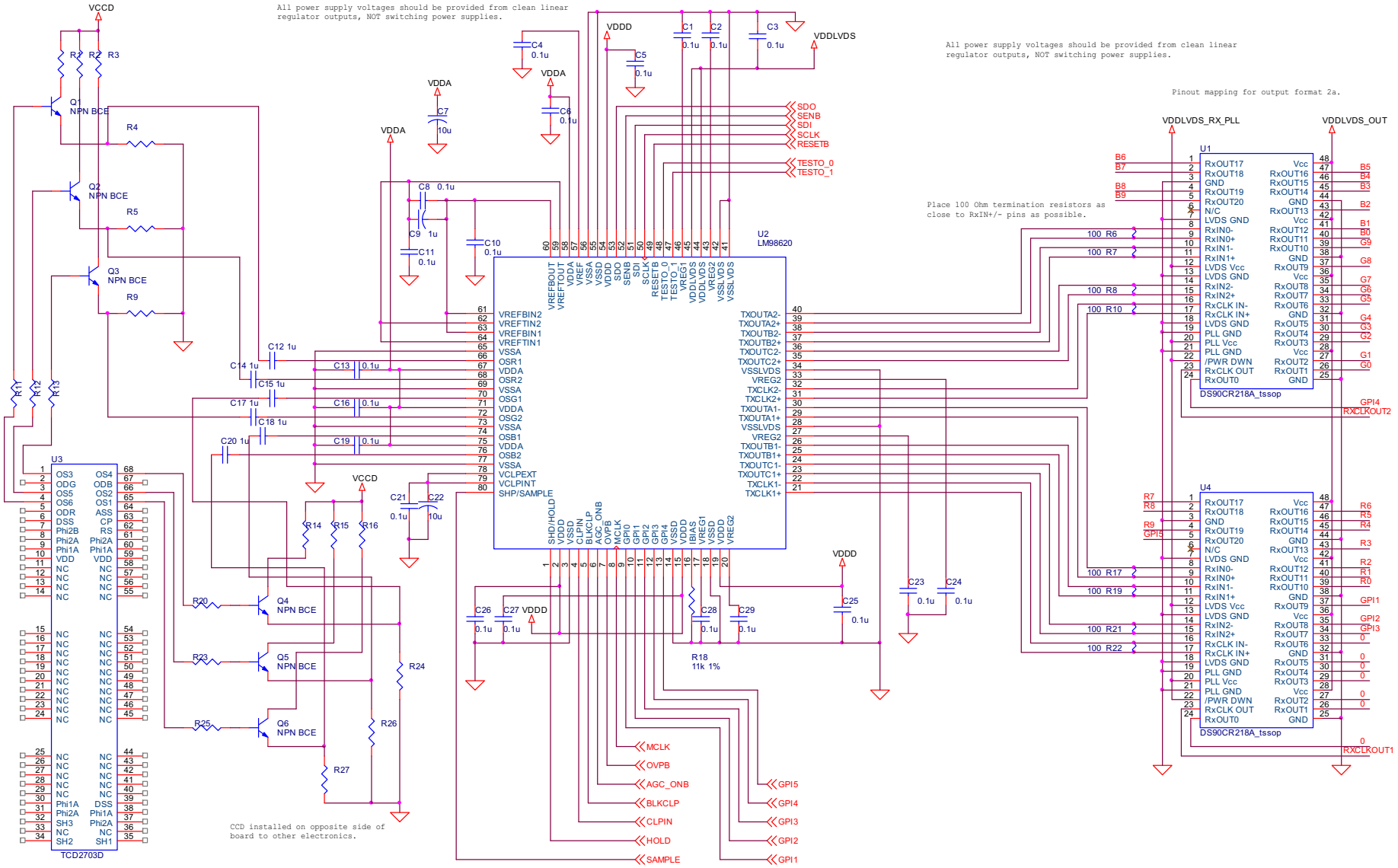


Figure 40. Example Circuit

8.2.1 Design Requirements

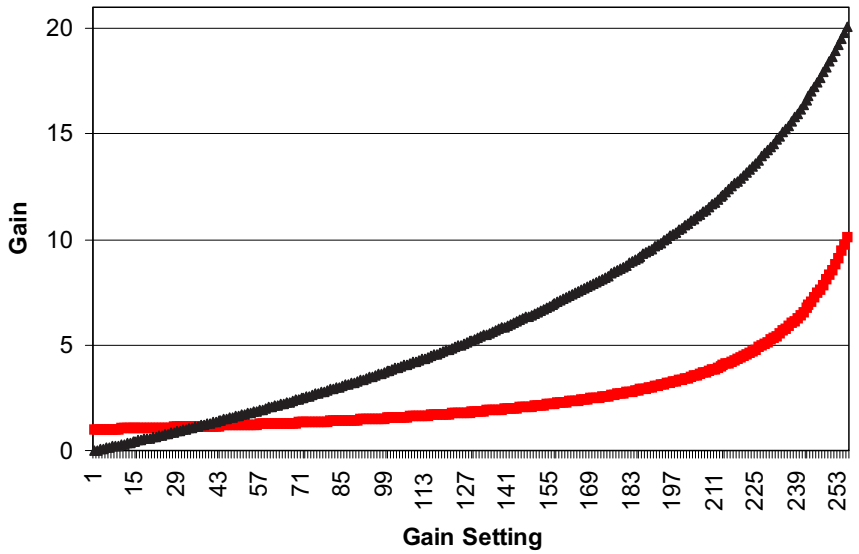
See Figure 40 for an example circuit and the required minimum circuitry around the LM98620.

- All power supply voltages should be provided from clean linear regulator outputs, NOT switching power supplies.
- Place 100 Ω termination resistors as close to RxIN+/- pins as possible.

8.2.2 Detailed Design Procedure

1. 3.3 V Power for Analog, Digital, and LVDS supplies. It is recommended to use a common LDO regulator for all 3.3V supplies, using EMI filter devices and dedicated decoupling to isolate any noise between buses.
2. Input Timing Signals (Ground referenced logic signal with: 2.0 V < VHigh < 3.3 V)
   (a) MCLK: Continuous clock signal at pixel rate or ADC rate of LM98620
   (b) CLPIN: Once per scan line signal used to control initial of input clamp for DC restoration of AC coupled CCD input signals
   (c) BLKCLP: Once per scan line signal used to indicate beginning of black pixels for Black (Offset) Level Calibration
   (d) AGC_ONB – Input signal used to initiate start of White (Gain) Calibration
   (e) SHP/SAMPLE: Once per pixel signal used to control pixel sample timing
   (f) SHD/HOLD: Once per pixel signal used to control pixel sample timing
3. Optional General Purpose logic inputs. Can be used to transfer low speed digital status information from the imaging board to the data processing module
   (a) GPI1-5
4. CCD signals at OS Inputs – These are connected to the outputs from the CCD sensor emitter follower buffer circuits. The signals are AC coupled to the AFE inputs using 0.1 uF capacitors.
5. Serial control interface from data processing module to LM98620 (Ground referenced logic signal with: 2.0 V < V_{high} < 3.3 V):
   (a) SENB – Serial enable to LM98620
   (b) SCLK – Serial clock input to LM98620
   (c) SDI – Data input to LM98620
   (d) SDO – Data output from LM98620
6. Serialized LVDS data pairs connected to FPGA or LVDS deserializer chip on data processing module
7. Adjust and reconfigure the configuration register settings as needed

8.2.3 Application Performance Plots



8-Bit PGA Gain
PGA Gain = 283/(283-M)
M = 0 to 255

Min Gain = 1.0
Max Gain = 10
Max Step = 0.300 dB

Remaining Gain of 2x in CDS
Black = Gain in dB
Red = Gain by Ratio

Figure 41. PGA Gain Curve

9 Power Supply Recommendations

9.1 Over Voltage Protection on OS Inputs

The OS inputs are protected from damage caused by transients from the sensor circuitry during power up/down. When the chip is not powered, or has just been powered up, the OS inputs are clamped to VBSSAB with PMOS devices. The protective clamp circuits are disabled by applying a high level to the OVPB input pin and setting the OVP enable bit to its default state of 0.

The maximum voltage and input current specifications for the OS inputs when OVP is enabled are the same as those listed in *Absolute Maximum Ratings*(1).

Positive input signals will be clamped by the internal switch through a diode to VSSA. Negative input signals will be clamped by the internal ESD protection diode to one diode drop below VSSD. Typically this will be about 0.7V below ground.

Table 15. Over Voltage Protection Input Clamping

OVPB INPUT PIN	OVP ENABLE BIT (REGISTER 0x01, BIT 4)	OVER VOLTAGE PROTECTION INPUT CLAMPING
0	0	Enabled
1	0	Disabled
0	1	Enabled
1	1	Enabled

(1) Absolute maximum ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.

10 Layout

10.1 Layout Guidelines

1. Use Figure 42 configuration for powering the device.

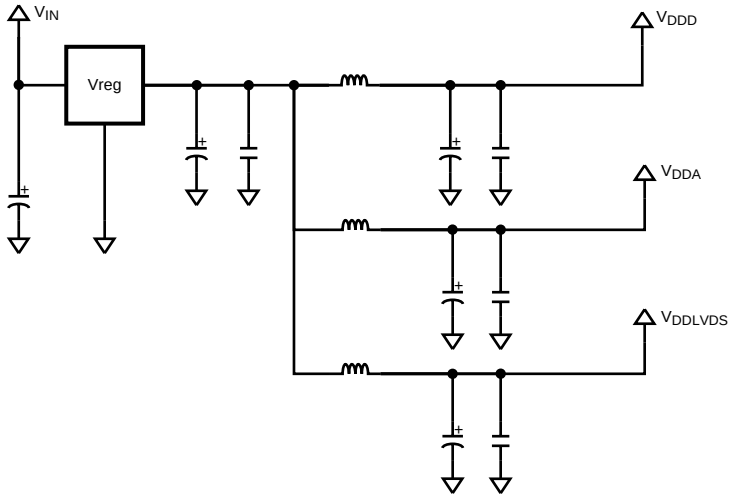


Figure 42. Recommended Setup for Powering Device

2. Place decoupling cap(s) next to every supply pin to the ground plane close by.
3. Use a multi-layer boards as shown in Figure 43 to ease routing, and to provide a low inductance ground plane.
4. Beware of via inductance and when necessary increase the number and / or diameter of vias to reduce inductance
5. Use ground plane “keep out” areas under sensitive nodes to minimize parasitic capacitance

10.2 Layout Examples

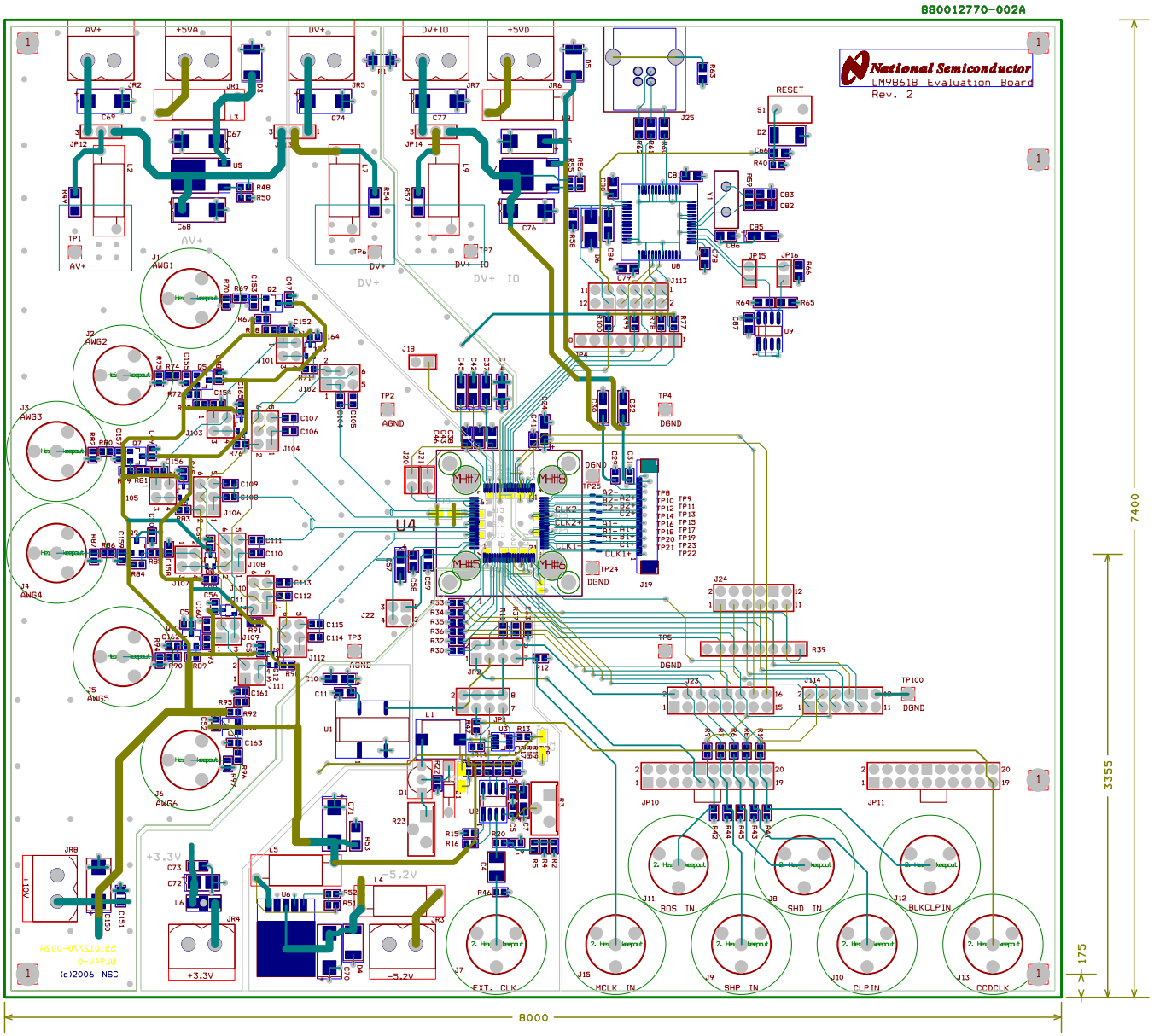


Figure 43. LM98620 Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM98620VHB/NOPB	Active	Production	TQFP (PFC) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	LM98620VHB
LM98620VHB/NOPB.A	Active	Production	TQFP (PFC) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	LM98620VHB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

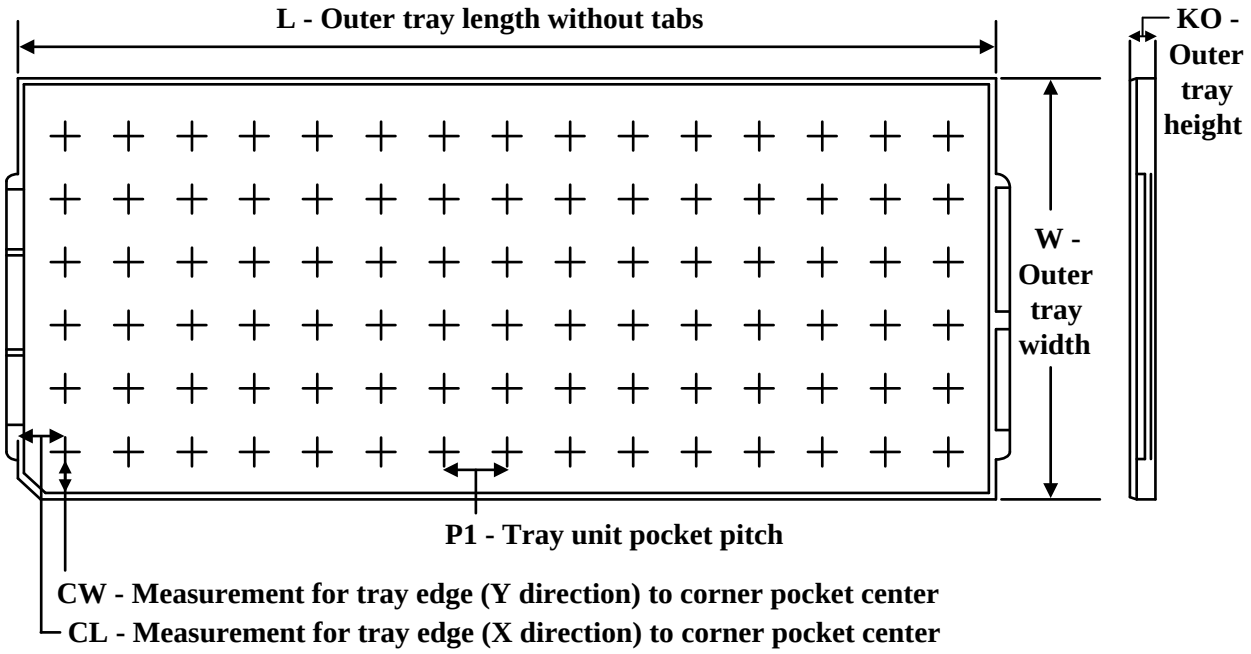
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

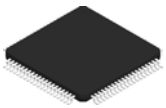
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LM98620VHB/NOPB	PFC	TQFP	80	119	7X17	150	322.6	135.9	7620	17.9	14.3	13.95
LM98620VHB/NOPB.A	PFC	TQFP	80	119	7X17	150	322.6	135.9	7620	17.9	14.3	13.95

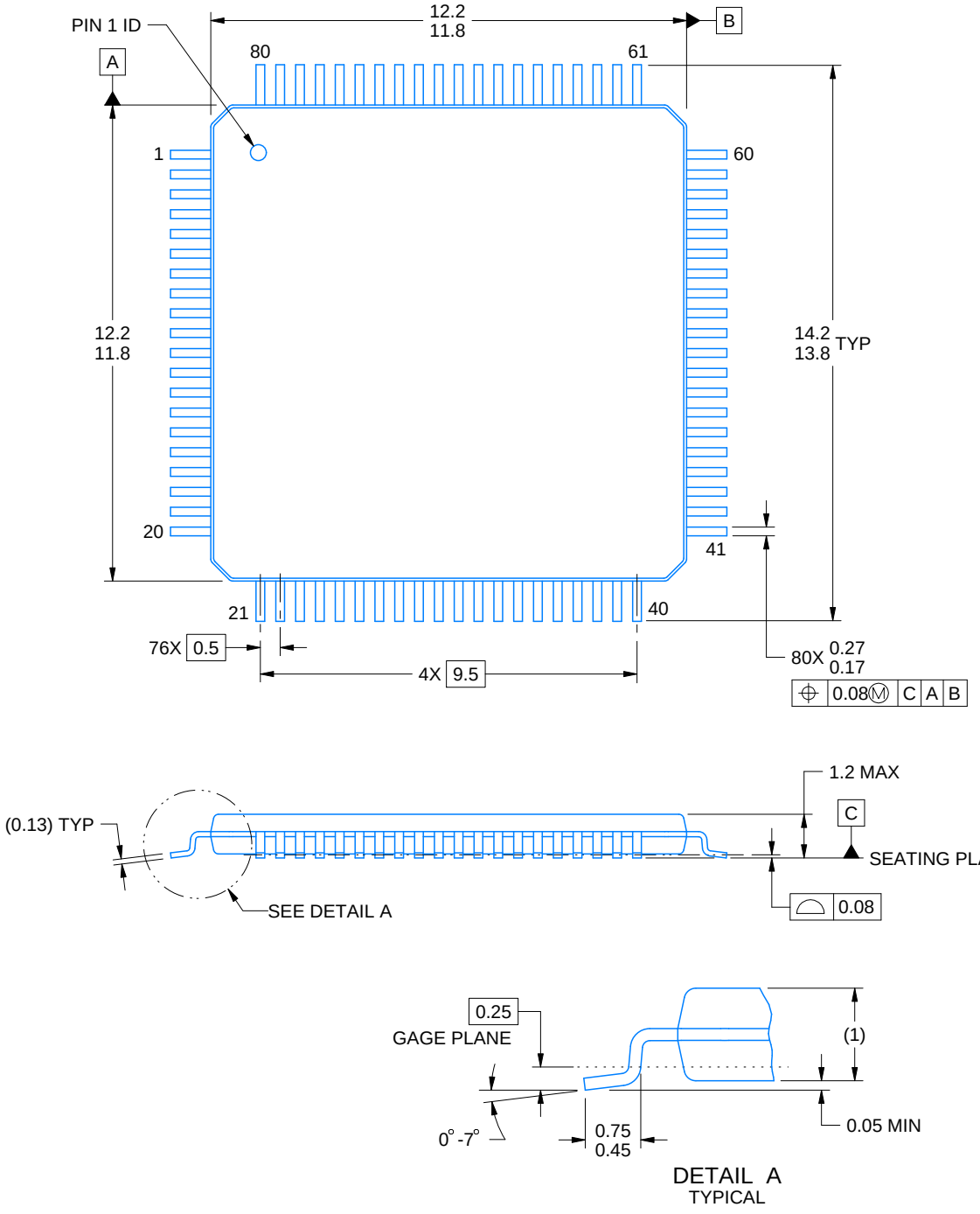


PACKAGE OUTLINE

PFC0080A

TQFP - 1.2 mm max height

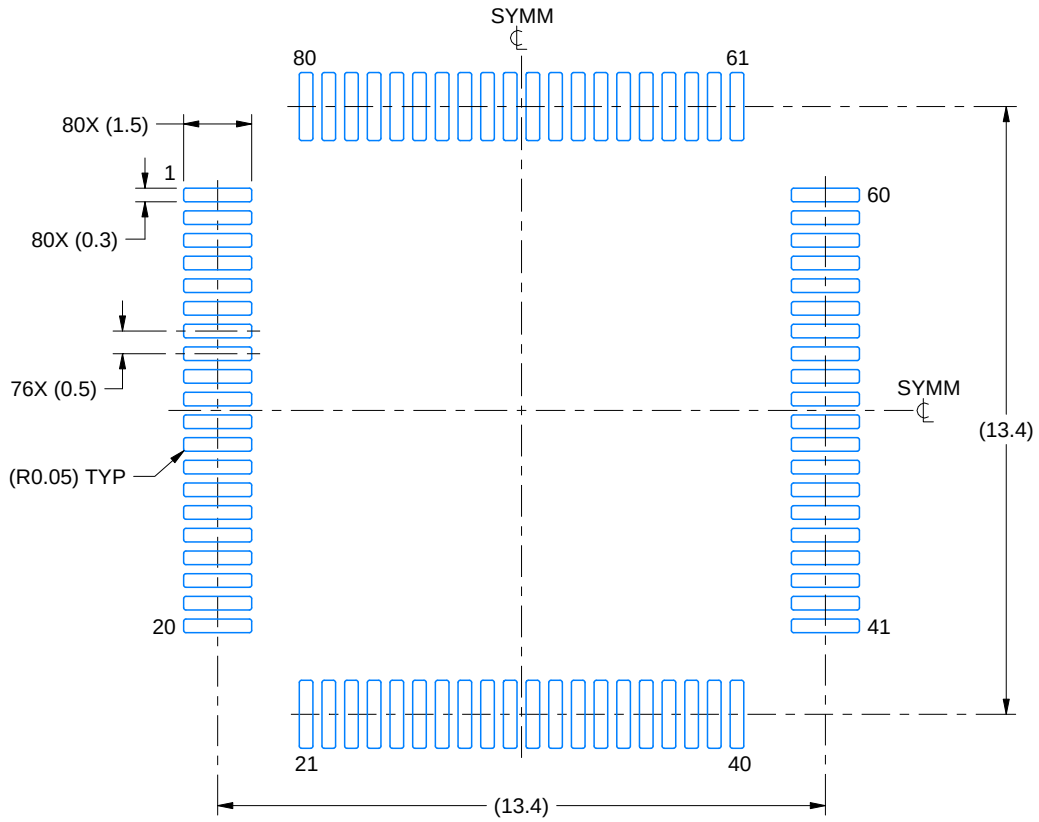
PLASTIC QUAD FLATPACK



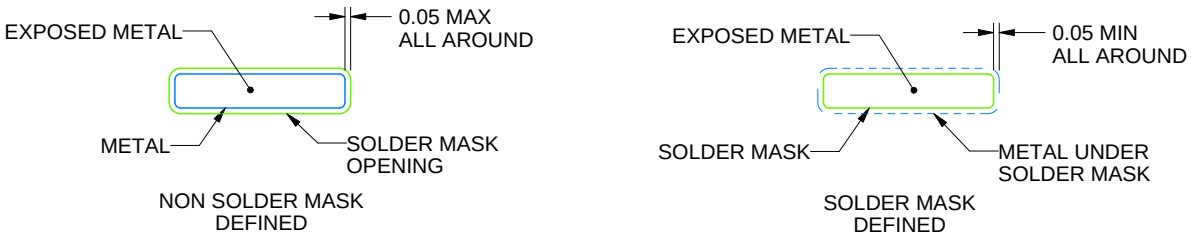
4215165/B 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

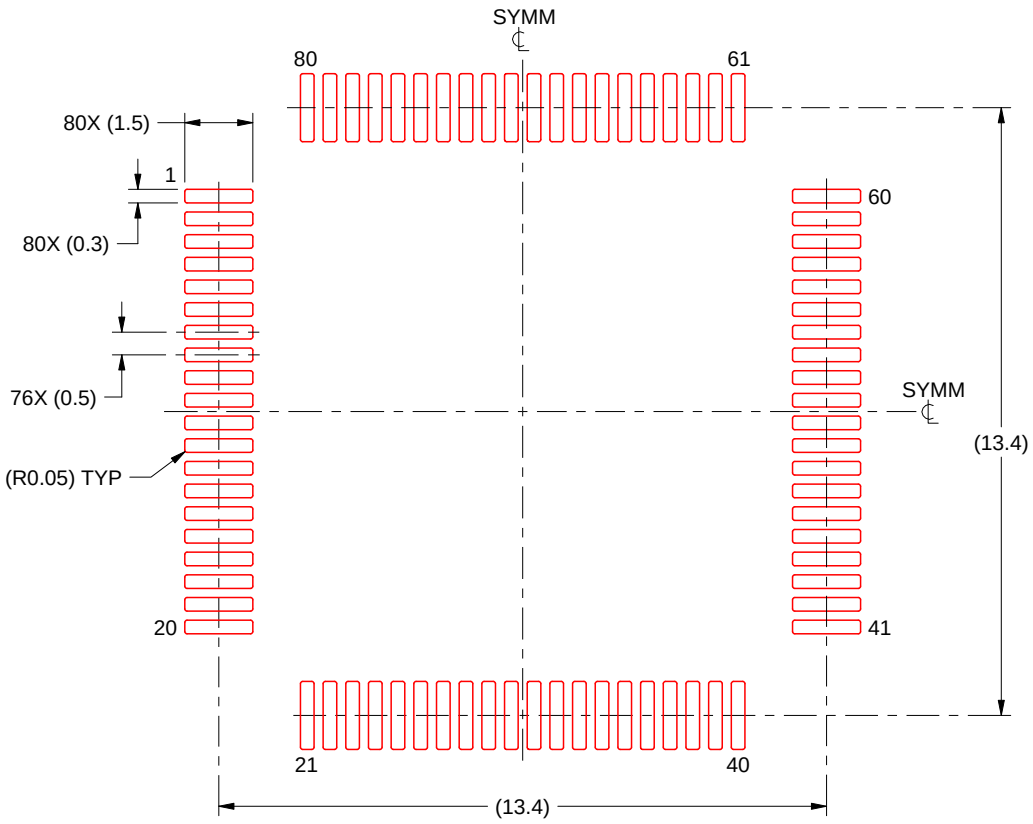


SOLDER MASK DETAILS

4215165/B 06/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215165/B 06/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025