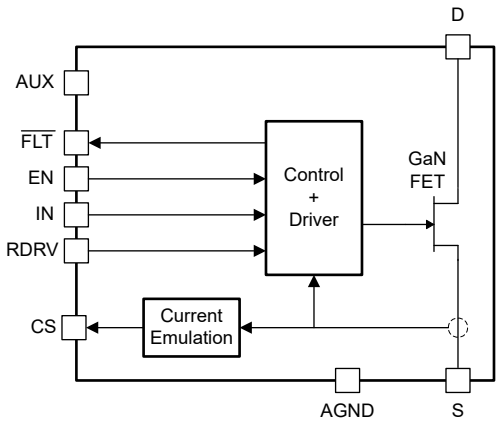
LMG3624 700V, 155mΩ, GaN FET With Integrated Driver and Current-Sense Emulation

1 Features

- GaN power FET: 700V, 155mΩ,
- Integrated gate driver with low propagation delays and adjustable turn-on slew-rate control
- Current-sense emulation with high bandwidth and high accuracy
- Cycle-by-cycle overcurrent protection
- Overtemperature protection with $\overline{\text{FLT}}$ pin reporting
- AUX quiescent current: 240µA
- AUX standby quiescent current: 50µA
- Maximum supply and input logic pin voltage: 26V
- 8mm × 5.3mm QFN package with thermal pad

2 Applications

- AC/DC adapters and chargers
- Mobile wall charger design
- USB wall power outlet
- Auxiliary-power supplies
- SMPS power supply for TV
- LED Power Supply



Simplified Block Diagram

3 Description

The LMG3624 is a 700V 155mΩ GaN power FET intended for switch-mode power-supply applications. The LMG3624 simplifies design and reduces component count by integrating the GaN FET and gate driver in a 8mm × 5.3mm VQFN package.

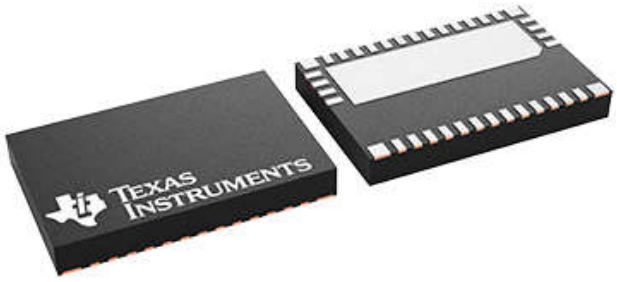
Programmable turn-on slew rates provide EMI and ringing control. The current-sense emulation reduces power dissipation compared to the traditional current-sense resistor and allows the low-side thermal pad to be connected to the cooling PCB power ground.

The LMG3624 supports converter light-load efficiency requirements and burst-mode operation with low quiescent currents and fast start-up times. Protection features include under-voltage lockout (UVLO), cycle-by-cycle current limit , and overtemperature protection. Overtemperature protection is reported with the open-drain $\overline{\text{FLT}}$ pin.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG3624	REQ (VQFN, 38)	8mm × 5.3mm
LMG3624Y		

(1) For more information, see the Mechanical, Packaging, and Orderable Information section.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



38-Pin VQFN

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4 Pin Configuration and Functions

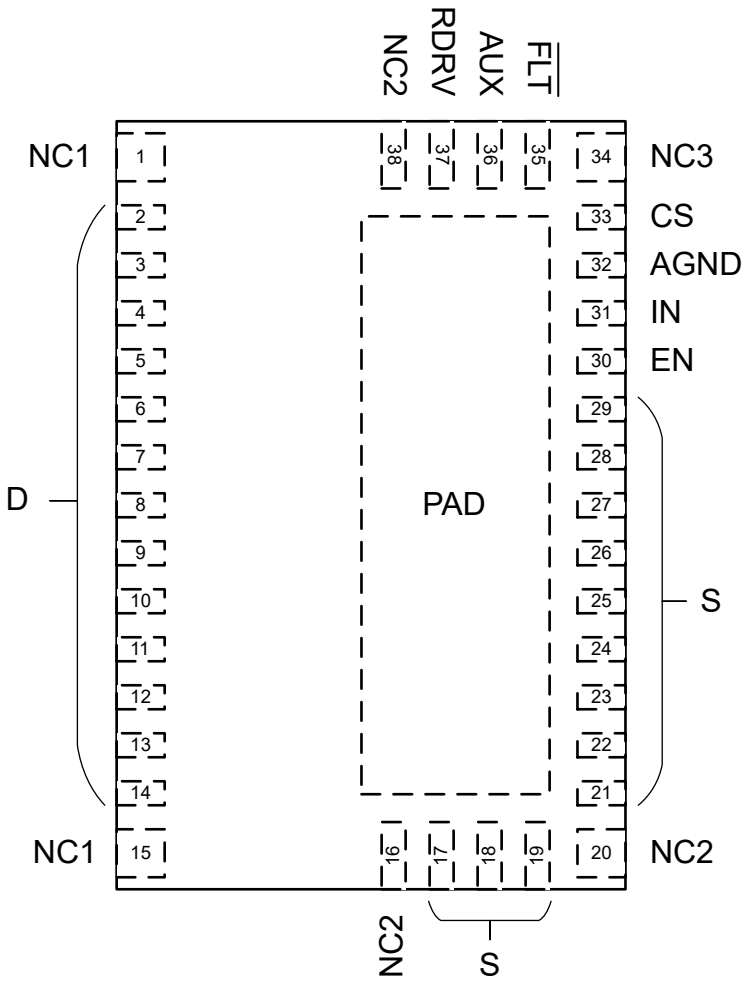


Figure 4-1. REQ Package, 38-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	32	GND	Analog ground. Internally connected to S, PAD, and NC2.
AUX	36	P	Auxiliary voltage rail. Device supply voltage. Connect a local bypass capacitor between AUX and AGND.
CS	33	O	Current-sense emulation output. Outputs scaled replica of the GaN FET current. Feed output current into a resistor to create a current sense voltage signal. Reference the resistor to the power supply controller IC local ground. This function replaces the external current sense resistor that is used in series with the FET source.
D	2-14	P	GaN FET drain. Internally connected to NC1.
EN	30	I	Enable. Used to toggle between active and standby modes. The standby mode has reduced quiescent current to support converter light load efficiency targets. There is a forward based ESD diode from EN to AUX so avoid driving EN higher than AUX.
$\overline{\text{FLT}}$	35	O	Active-low fault output. Open-drain output that asserts during overtemperature protection.
IN	31	I	Gate-drive control input. There is a forward based ESD diode from IN to AUX so avoid driving IN higher than AUX.
NC1	1, 15	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to D.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC2	16, 20, 38	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to AGND, S and, PAD.
NC3	34	NC	Used to anchor QFN package to PCB. Pin must be soldered to a PCB landing pad. The PCB landing pad is non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Pin not connected internally.
PAD	—	—	Thermal pad. Internally connected to S, AGND, and NC2. All the S current can conduct with PAD (PAD = S).
RDRV	37	I	Drive strength control resistor. Set a resistance between RDRV and AGND to program the GaN FET turn-on slew rate.
S	17-19, 21-29	P	GaN FET source. Internally connects to AGND, PAD, and NC2.

(1) I = input, O = output, I/O = input or output, GND = ground, P = power, NC = no connect.

5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to AGND(1)

			MIN	MAX	UNIT
V_{DS}	Drain-source (D to S) voltage, FET off(2)			700	V
$V_{DS(surge)}$	Drain-source (D to S) voltage, FET switching, surge condition(3)			720	V
$V_{DS(tr)(surge)}$	Drain-source (D to S) transient ringing peak voltage, FET off, surge condition(3)			800	V
	Pin voltage	AUX	–0.3	30	V
		EN, IN, $\overline{FLT}$	–0.3	V_{AUX} + 0.3	V
		CS	–0.3	5.5	V
		RDRV	–0.3	4	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on		–6.6	Internally limited	A
$I_{D(pulse)(oc)}$	Drain (D to S) pulsed current during overcurrent response time(4)			16	A
$I_{S(cnts)}$	Source (S to D) continuous current, FET off			6.6	A
	Positive sink current	CS		10	mA
		$\overline{FLT}$ (while asserted)		Internally limited	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See Section 7.3.1 section for more information on the GaN power FET switching capability. t1 < 400ns in Section 7.3.1.
(3) t1 < 100ns in Section 7.3.1.
(4) GaN power FET may self-limit below this value if it enters saturation.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 1 through 15	±1000	V
			Pins 16 through 38	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to AGND

			MIN	NOM	MAX	UNIT
	Supply voltage	AUX	10		26	V
	Input voltage	EN, IN	0		V_{AUX}	V
	Pull-up voltage on open-drain output	$\overline{FLT}$	0		V_{AUX}	V
V_{IH}	High-level input voltage	EN, IN	2.5			V
V_{IL}	Low-level input voltage				0.6	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on		–5.4		5.4	A
C_{AUX}	AUX to AGND capacitance from external bypass capacitor		0.030			µF
R_{RDRV}	RDRV to AGND resistance from external slew-rate control resistor to configure below slew rate settings					
	slew rate setting 0 (slowest)		90	120	open	kΩ
	slew rate setting 1		42.5	47	51.5	kΩ
	slew rate setting 2		20	22	24	kΩ
	slew rate setting 3 (fastest)		0	5.6	11	kΩ

5.4 Thermal Information

THERMAL METRIC[1]		LMG3624 REQ (VQFN) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.67	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

1) Symbol definitions: I_D = D to S current; I_S = S to D current; $I_{CS(src)}$ = current out of CS; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; V_{DS} = 520V; 10V ≤ V_{AUX} ≤ 26V; V_{EN} = 5V; V_{IN} = 0V; R_{RDRV} = 0Ω; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$R_{DS(on)}$	Drain-source (D to S) on resistance	V_{IN} = 5V, I_D = 3A, T_J = 25°C		155	220	mΩ
		V_{IN} = 5V, I_D = 3A, T_J = 125°C		276		
I_{DSS}	Drain (D to S) leakage current	V_{DS} = 650V, T_J = 25°C		2		µA
		V_{DS} = 650V, T_J = 125°C		10		
Q_{OSS}	Output (D to S) charge	V_{DS} = 400V		20.0		nC
C_{OSS}	Output (D to S) capacitance			29		pF
E_{OSS}	Output (D to S) capacitance stored energy			2.69		µJ
$C_{OSS,er}$	Energy related effective output (D to S) capacitance			33.3		pF
$C_{OSS,tr}$	Time related effective output (D to S) capacitance	V_{DS} = 0V to 400V		49.3		pF
Q_{RR}	Reverse recovery charge			0		nC
OVERCURRENT PROTECTION						
$I_{T(OC)}$	Overcurrent fault – threshold current		5.4	6	6.6	A
CS						
	Current sense gain ($I_{CS(src)}$ / I_D)	V_{IN} = 5V, 0V ≤ V_{CS} ≤ 2V, 0A ≤ I_D < $I_{T(OC)}$		0.965		mA/A
	Current sense input offset current	V_{IN} = 5V, 0V ≤ V_{CS} ≤ 2V, 0A ≤ I_D < $I_{T(OC)}$	–55		55	mA
	Initial held output after overcurrent fault occurs while IN remains high	V_{IN} = 5V, 0V ≤ V_{CS} ≤ 2V			7	mA
$I_{CS(src)(OC)(final)}$	Final held output after overcurrent fault occurs while IN remains high	V_{IN} = 5V, 0V ≤ V_{CS} ≤ 2V	10	12	15.5	mA
	Output clamp voltage	V_{IN} = 5V, I_D = 5.2A, CS sinking 5mA from external source		2.55		V
EN, IN						
V_{IT+}	Positive-going input threshold voltage		1.7		2.45	V
$V_{IT–}$	Negative-going input threshold voltage		0.7		1.3	V
	Input threshold voltage hysteresis			1		V
	Pull-down input resistance	0V ≤ V_{PIN} ≤ 3V	200	400	600	kΩ
	Pull-down input current	10V ≤ V_{PIN} ≤ 26V; V_{AUX} = 26V		10		µA

5.5 Electrical Characteristics (continued)

1) Symbol definitions: I_D = D to S current; I_S = S to D current; $I_{CS(src)}$ = current out of CS; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; V_{DS} = 520V; 10V ≤ V_{AUX} ≤ 26V; V_{EN} = 5V; V_{IN} = 0V; R_{RDRV} = 0Ω; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERTEMPERATURE PROTECTION						
	Temperature fault – postive-going threshold temperature		145	165		°C
	Temperature fault – negative-going threshold temperature			145		°C
	Temperature fault – threshold temperature hysteresis			20		°C
$\overline{FLT}$						
	Low-level output voltage	$\overline{FLT}$ sinking 1mA while asserted			200	mV
	Off-state sink current	$V_{\overline{FLT}}$ = V_{AUX} while de-asserted			1	µA
AUX						
$V_{AUX,T+}$ (UVLO)	UVLO – positive-going threshold voltage		8.9	9.3	9.7	V
	UVLO – negative-going threshold voltage		8.6	9.0	9.4	V
	UVLO – threshold voltage hysteresis			250		mV
	Standby quiescent current	V_{EN} = 0V		50	80	µA
	Quiescent current			240	360	µA
	Operating current	V_{IN} = 0V or 5V, V_{DS} = 0V, I_D = 0A, f_{IN} = 500kHz		2.0		mA

5.6 Switching Characteristics

1) Symbol definitions: I_D = D to S current; I_S = S to D current; $I_{CS(src)}$ = current out of CS; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; V_{DS} = 520V; 10V ≤ V_{AUX} ≤ 26V; V_{EN} = 5V; V_{IN} = 0V; R_{RDRV} = 0Ω; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$t_{d(on)}$ (Idrain)	Drain current turn-on delay time	LMG3624, From V_{IN} > $V_{IN,IT+}$ to I_D > 37.5mA, V_{BUS} = 400V, L_{HB} current = 1.5A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		64		ns
		slew rate setting 1		31		
		slew rate setting 2		26		
		slew rate setting 3 (fastest)		23		
$t_{d(on)}$ (Idrain)	Drain current turn-on delay time	LMG3624Y, From V_{IN} > $V_{IN,IT+}$ to I_D > 37.5mA, V_{BUS} = 400V, L_{HB} current = 1.5A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		128		ns
		slew rate setting 1		55		
		slew rate setting 2		41		
		slew rate setting 3 (fastest)		24		
$t_{d(on)}$	Turn-on delay time	LMG3624, From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 1.5A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		86		ns
		slew rate setting 1		40		
		slew rate setting 2		34		
		slew rate setting 3 (fastest)		27		
$t_{d(on)}$	Turn-on delay time	LMG3624Y, From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 1.5A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		178		ns
		slew rate setting 1		76		
		slew rate setting 2		56		
		slew rate setting 3 (fastest)		28		
$t_{d(off)}$	Turn-off delay time	From V_{IN} < $V_{IN,IT-}$ to V_{DS} > 80V, V_{BUS} = 400V, L_{HB} current = 1.5A, (independent of slew rate setting), see GaN Power FET Switching Parameters		32		ns
$t_{f(off)}$	Turn-off fall time	From V_{DS} > 80V to V_{DS} > 320V, V_{BUS} = 400V, L_{HB} current = 1.5A, (independent of slew rate setting), see GaN Power FET Switching Parameters		22		ns

1) Symbol definitions: I_D = D to S current; I_S = S to D current; $I_{CS(src)}$ = current out of CS; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; V_{DS} = 520V; 10V ≤ V_{AUX} ≤ 26V; V_{EN} = 5V; V_{IN} = 0V; R_{RDRV} = 0Ω; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Turn-on slew rate	LMG3624, From V_{DS} < 250V to V_{DS} < 150V, T_J = 25°C, V_{BUS} = 400V, L_{HB} current = 1.5A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		20		V/ns
		slew rate setting 1		50		
		slew rate setting 2		75		
		slew rate setting 3 (fastest)		150		
	Turn-on slew rate	LMG3624Y, From V_{DS} < 250V to V_{DS} < 150V, T_J = 25°C, V_{BUS} = 400V, L_{HB} current = 1.5A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		7		V/ns
		slew rate setting 1		15		
		slew rate setting 2		22		
		slew rate setting 3 (fastest)		89		
CS						
t_r	Rise time	From $I_{CS(src)}$ > 0.2 × $I_{CS(src)(final)}$ to $I_{CS(src)}$ > 0.9 × $I_{CS(src)(final)}$, 0V ≤ V_{CS} ≤ 2V, enabled into a 1.5A load			35	ns
EN						
	EN Wake-up time	From V_{EN} > V_{IT+} to $I_{D(ls)}$ > 10mA, V_{INL} = 5V		1.5		µs

5.7 Typical Characteristics

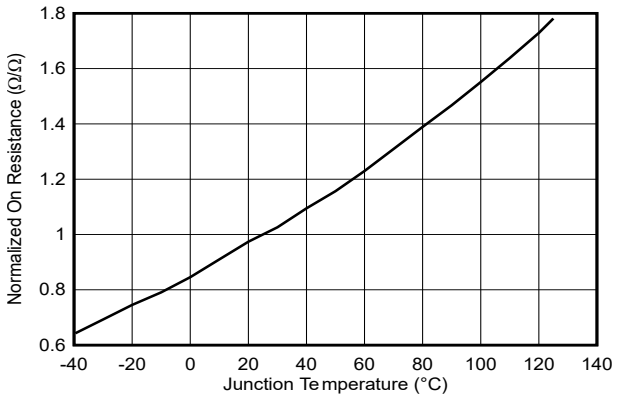


Figure 5-1. Normalized On-Resistance vs Junction Temperature

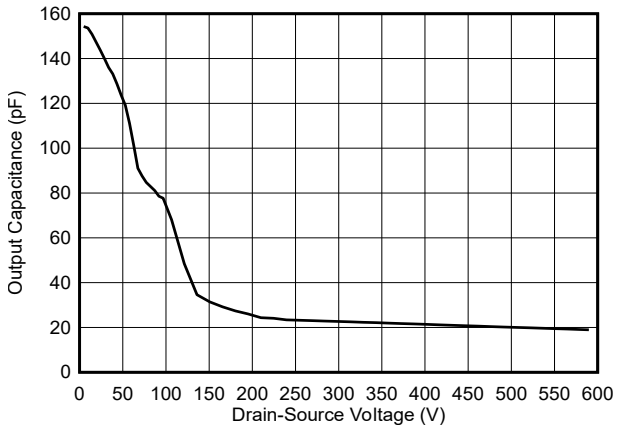


Figure 5-2. Output Capacitance vs Drain-Source Voltage

5.7 Typical Characteristics (continued)

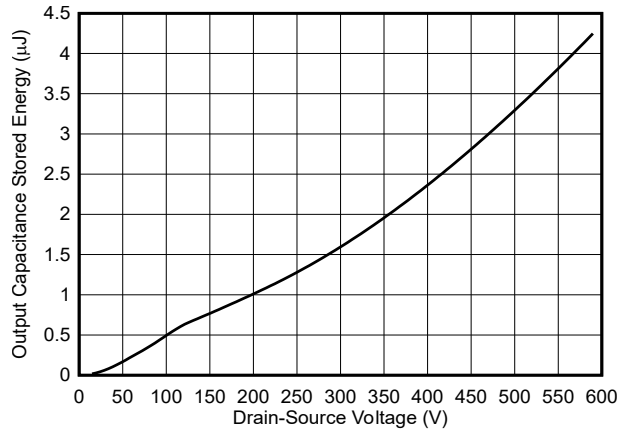


Figure 5-3. Output Capacitance Stored Energy vs Drain-Source Voltage

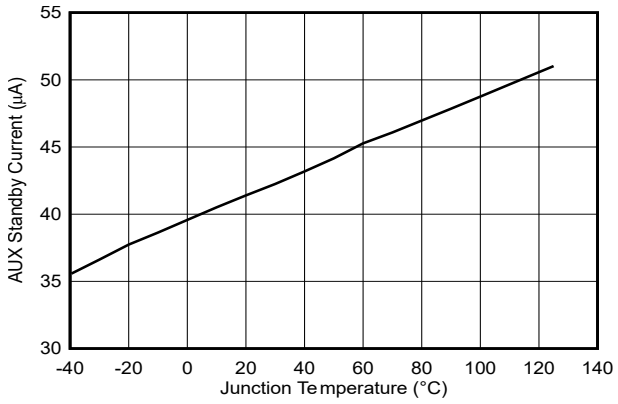


Figure 5-4. AUX Standby Current vs Junction Temperature

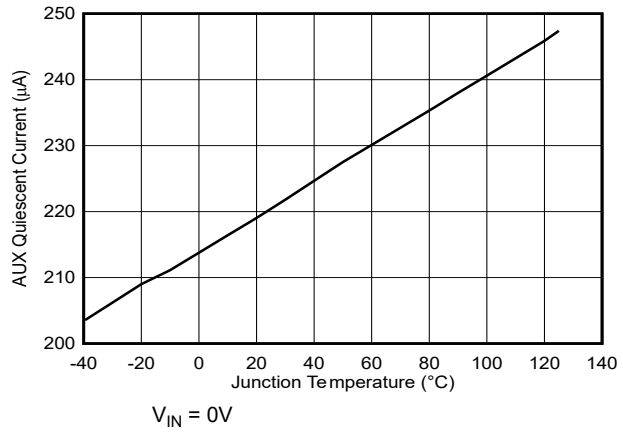


Figure 5-5. AUX Quiescent Current vs Junction Temperature

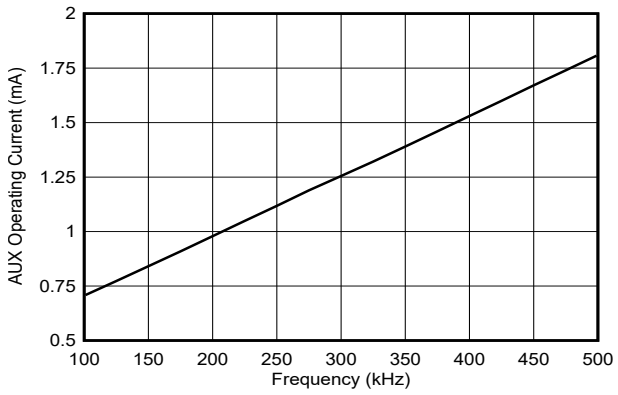


Figure 5-6. AUX Operating Current vs Frequency

6 Parameter Measurement Information

6.1 GaN Power FET Switching Parameters

Figure 6-1 shows the circuit used to measure the GaN power FET switching parameters. The circuit operates as a double-pulse tester. Consult external references for double-pulse tester details. The circuit operates in the boost configuration with the low-side LMG3624 as the device under test (DUT). The high-side LMG3624 acts as the double-pulse tester diode and circulates the inductor current in the off-state, third-quadrant conduction mode.

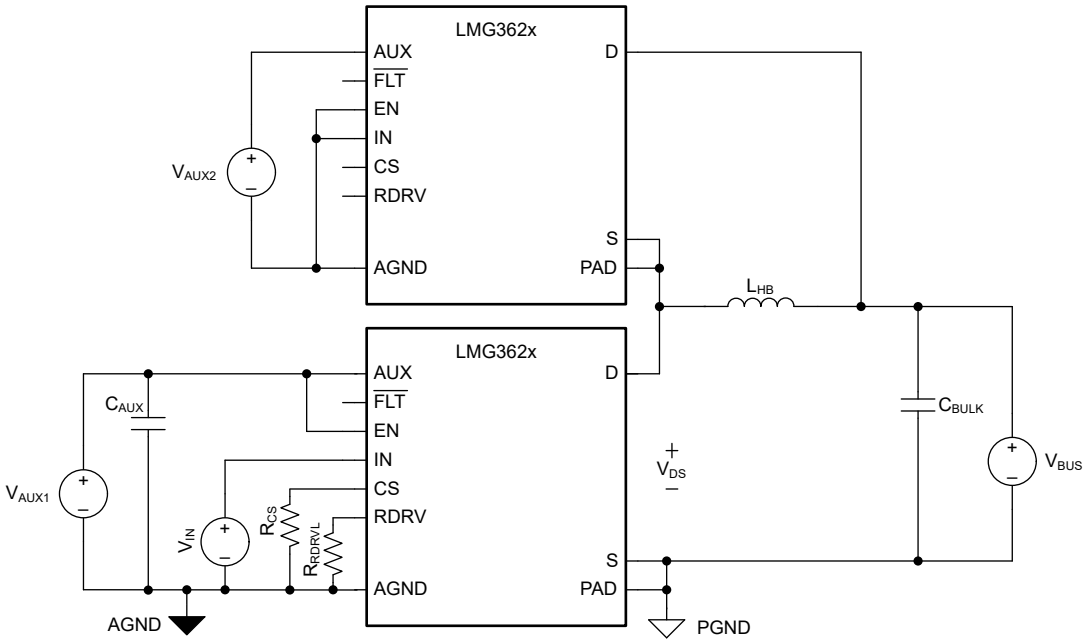


Figure 6-1. GaN Power FET Switching Parameters Test Circuit

Figure 6-1 shows the GaN power FET switching parameters.

The GaN power FET turn-on transition has three timing components: drain-current turn-on delay time, turn-on delay time, and turn-on rise time. Note that the turn-on rise time is the same as the V_{DS} 80% to 20% fall time. All three turn-on timing components are a function of the RDRV pin setting.

The GaN power FET turn-off transition has two timing components: turn-off delay time and turn-off fall time. Note that the turn-off fall time is the same as the V_{DS} 20% to 80% rise time. The turn-off timing components are independent of the RDRV pin setting, but heavily dependent on the L_{HB} current.

The turn-on slew rate is measured over a smaller voltage delta (100V) compared to the turn-on rise time voltage delta (240V) to obtain a faster slew rate which is useful for EMI design. Use the RDRV pin to program the slew rate.

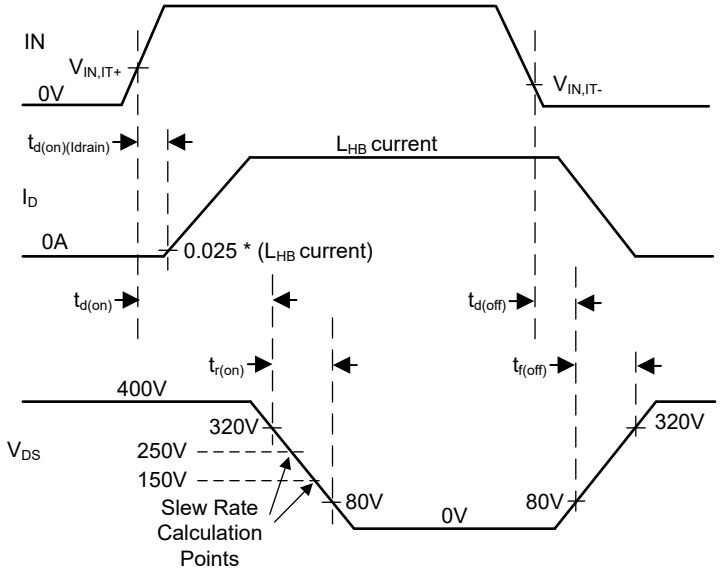


Figure 6-2. GaN Power FET Switching Parameters

7 Detailed Description

7.1 Overview

The LMG3624 is an integrated 700V 155mΩ GaN power FET intended for use in switching-power converters. The LMG3624 combines the GaN FET, gate driver, current-sense emulation function, and protection features in a 8mm × 5.3mm QFN package.

The 700V rated GaN FET supports the high voltages encountered in off-line power switching applications. The GaN FET low output-capacitive charge reduces both the time and energy needed for power converter switching and is the key characteristic needed to create small, efficient power converters.

The LMG3624 internal gate driver regulates the drive voltage for optimum GaN FET on-resistance. The internal driver reduces total gate inductance and GaN FET common-source inductance for improved switching performance, including common-mode transient immunity (CMTI). Individually program the GaN FET turn-on slew rate to one of four discrete settings for design flexibility regarding power loss, switching-induced ringing, and EMI.

Current-sense emulation places a scaled replica of the GaN FET drain current on the output of the CS pin. The CS pin terminates with a resistor to AGND to create the current-sense input signal to the external power supply controller. This CS pin resistor replaces the traditional current-sense resistor, placed in series with the GaN FET source, at significant power and space savings. Furthermore, with no current-sense resistor in series with the GaN FET source, connect the GaN FET thermal pad directly to the PCB power ground. This thermal pad connection both improves system thermal performance and provides additional device routing flexibility since full device current can conduct through the thermal pad.

The AUX input supply wide voltage range is compatible with the corresponding wide range supply rail created by power supply controllers. Low AUX quiescent currents support converter burst-mode operation critical for meeting government light-load efficiency mandates. Obtain further AUX quiescent current reduction by placing the device in standby mode with the EN pin.

The IN and EN control pins have high input impedance, low input threshold voltage, and maximum input voltage equal to the AUX voltage. This combination allows the pins to support both low voltage and high voltage input signals and be driven with low-power outputs.

The LMG3624 protection features are under-voltage lockout (UVLO), cycle-by-cycle current limit , and overtemperature protection. The overtemperature protection is reported on the open drain $\overline{\text{FLT}}$ output.

7.2 Functional Block Diagram

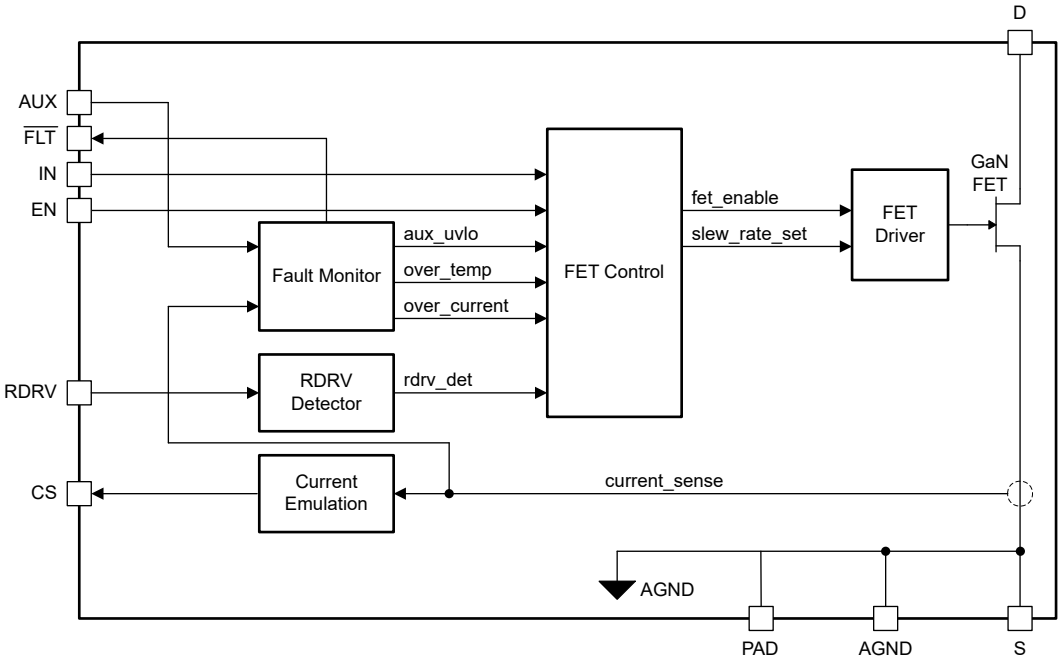


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 GaN Power FET Switching Capability

Due to the silicon FET's long reign as the dominant power-switch technology, many designers are unaware that the nameplate drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The nameplate drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The nameplate drain-source voltage of a GaN FET is set by the long term compliance to data sheet specifications.

Exceeding the nameplate drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the nameplate drain-source voltage. For example, the breakdown drain-source voltage of the LMG3624 GaN power FET is more than 800V which allows the LMG3624 to operate at conditions beyond an identically nameplate rated silicon FET.

The LMG3624 GaN power FET switching capability is explained with the assistance of Figure 7-2. The figure shows the drain-source voltage versus time for the LMG3624 GaN power FET for four distinct switch cycles in a switching application. No claim is made about the switching frequency or duty cycle. The first three cycles show normal operation and the last cycle shows operation during a rare input voltage surge. The LMG3624 GaN power FETs can be turned on in continuous-conduction mode (CCM) hard switching, zero-voltage switching (ZVS), and discontinuous-conduction mode (DCM) switching conditions.

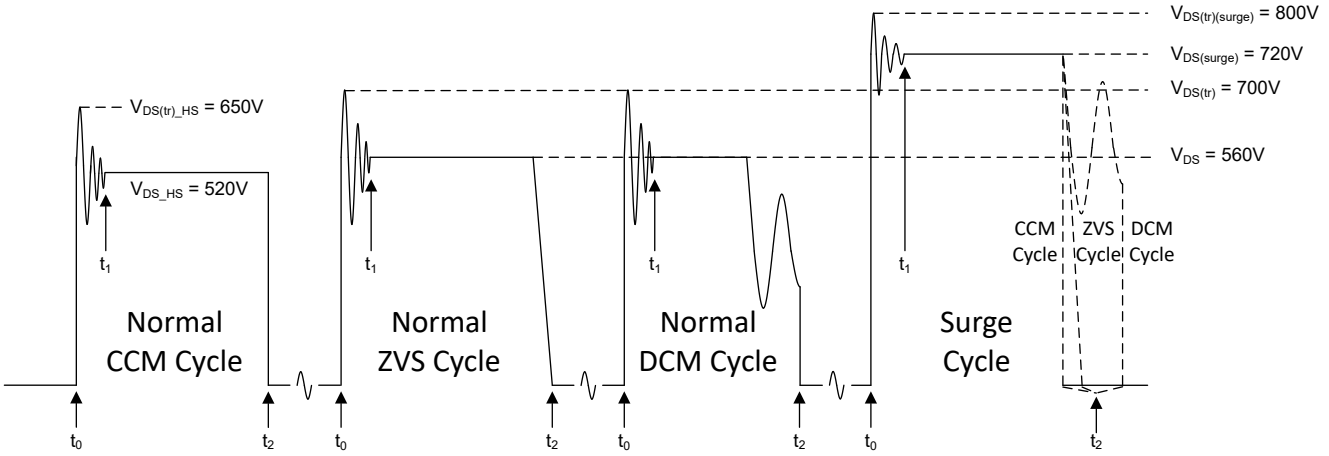


Figure 7-2. GaN Power FET Switching Capability

Each cycle starts before t_0 with the FET in the on state. At t_0, the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing dampens out by t_1. Between t_1 and t_2, the characteristic response of the switching application sets the FET drain-source voltage. The characteristic is shown as a flat line (plateau), but other responses are possible. At t_2, the GaN FET turns on. For normal CCM operation, the voltage limit of the transient ring is 650V and the voltage limit of the plateau is 520V. For normal ZVS/DCM operation, the voltage limit of the transient ring is 700V and the voltage limit of the plateau is 560V. For rare surge events, the voltage limit of the transient ring is 800V and the voltage limit of the plateau is 720V.

7.3.2 Turn-On Slew-Rate Control

The turn-on slew rate of the GaN power FET is programmed to one of four discrete settings by the resistance between the RDRV and AGND pins. The slew-rate setting is determined once during AUX power up when the AUX voltage goes above the AUX power-on reset voltage. The slew-rate setting determination time is not specified but is approximately 0.4µs.

Slew-Rate Setting shows the recommended typical resistance programming value for the four slew rate settings and the typical turn-on slew rate at each setting. As noted in the table, an open-circuit connection is acceptable for programming slew-rate setting 0 and a short-circuit connection (RDRV shorted to AGND) is acceptable for programming slew-rate setting 3.

Table 7-1. Slew-Rate Setting

TURN-ON SLEW RATE SETTING	RECOMMENDED TYPICAL PROGRAMMING RESISTANCE (kΩ)	TYPICAL TURN-ON SLEW RATE (V/ns)	COMMENT
0 (slowest)	120	LMG3624: 20	Open-circuit connection for programming resistance is acceptable.
		LMG3624Y: 7	
1	47	LMG3624: 50	
		LMG3624Y: 15	
2	22	LMG3624: 75	
		LMG3624Y: 22	
3 (fastest)	5.6	LMG3624: 150	Short-circuit connection for programming resistance (RDRV shorted to AGND) is acceptable.
		LMG3624Y: 89	

7.3.3 Current-Sense Emulation

The current-sense emulation function creates a scaled replica of the GaN power FET positive drain current at the output of the CS pin. The current-sense emulation gain, G_{CSE}, is a 0.965mA output from the CS pin, I_{CS}, for every 1A passing into the drain of the low-side GaN power FET, I_D.

$$G_{CSE} = I_{CS} \div I_D = 0.965mA \div 1A = 0.000965 \quad (1)$$

The CS pin terminates with a resistor to AGND, R_{CS}, creating the current-sense voltage input signal to the external power supply controller.

Determine R_{CS} by solving for the traditional current-sense design resistance, $R_{CS(trad)}$, and multiplying by the inverse of G_{CSE}. The traditional current-sense design creates the current-sense voltage, $V_{CS(trad)}$, by passing the GaN power FET drain current, I_D, through $R_{CS(trad)}$. The LMG3624 creates the current-sense voltage, V_{CS}, by passing the CS pin output current, I_{CS}, through R_{CS}. Verify that the current-sense voltage is the same in both designs.

$$V_{CS} = I_{CS} \times R_{CS} = V_{CS(trad)} = I_D \times R_{CS(trad)} \quad (2)$$

$$R_{CS} = I_D \div I_{CS} \times R_{CS(trad)} = 1 \div G_{CSE} \times R_{CS(trad)} \quad (3)$$

$$R_{CS} = 1036 \times R_{CS(trad)} \quad (4)$$

The CS pin internally clamps to a typical 2.55V. The clamp protects vulnerable current-sense input pins of the power-supply controller from overvoltage if, for example, the current sense resistor on the CS pin disconnect.

Figure 7-3 shows the current-sense emulation operation. In both cycles, the CS pin current emulates the GaN power FET drain current while the GaN FET is enabled. The first cycle shows normal operation where the controller turns off the GaN power FET when the controller current-sense input threshold is tripped. The second cycle shows a fault situation where the LMG3624 overcurrent protection turns off the GaN power FET before the controller current-sense input threshold is tripped. In this second cycle, the LMG3624 avoids a hung controller IN pulse by generating a fast-ramping artificial current-sense emulation signal to trip the controller current-sense input threshold. The artificial signal persists until the IN pin goes to logic-low which indicates the controller reestablishes control of switch operation.

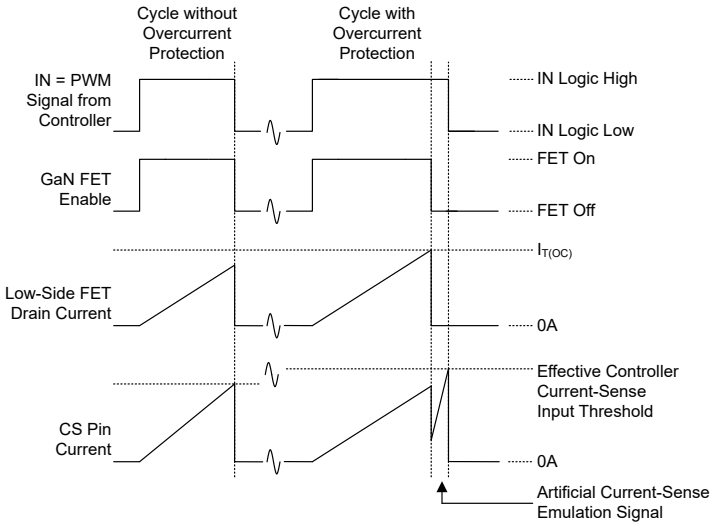


Figure 7-3. Current-Sense Emulation Operation

7.3.4 Input Control Pins (EN, IN)

The EN pin is used to toggle the device between the active and standby modes described in the *Device Functional Modes* section.

Use the IN pin to turn the GaN power FET on and off.

The input control pins have a typical 1V input-voltage threshold hysteresis for noise immunity. The pins also have a typical 400kΩ pull-down resistance to protect against floating inputs. The 400kΩ saturates for nominal input voltages above 4V to limit the maximum input pull-down current to a typical 10µA.

The following conditions block the IN turn-on action:

- Standby mode (as set by the EN pin above)
- AUX UVLO
- Overcurrent protection
- Overtemperature protection

The standby mode, AUX UVLO, and overtemperature protection are independent of the IN logic state. Figure 7-4 shows the IN independent blocking condition operation.

Meanwhile, overcurrent protection only acts after IN has turned on the GaN power FET. See Section 7.3.6 for more details.

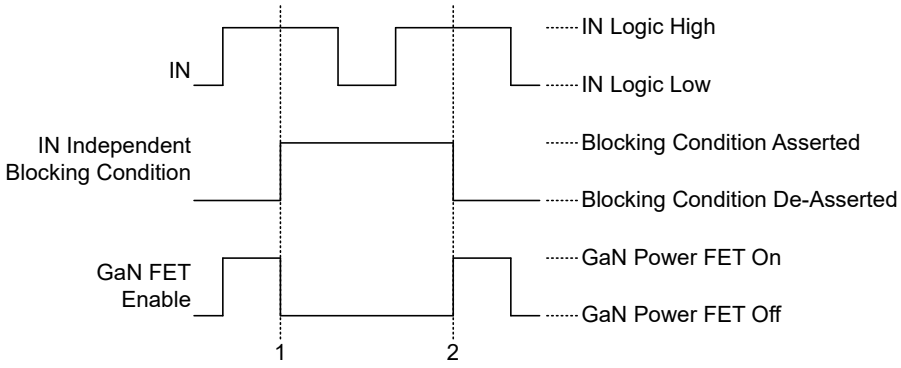


Figure 7-4. IN Independent Blocking Condition Operation

7.3.5 AUX Supply Pin

The AUX pin is the input supply for the internal circuits.

7.3.5.1 AUX Power-On Reset

If the AUX voltage is below the AUX power-on reset voltage, the AUX power-on reset disables all low-side functionality. The AUX power-on reset voltage is not specified but is approximately 5V. The AUX power-on reset initiates the one-time determination of the low-side slew-rate setting programmed on the RDRV pin when the AUX voltage goes above the AUX power-on reset voltage. The AUX power-on reset enables the overtemperature protection function if the AUX voltage is above the AUX power-on reset voltage.

7.3.5.2 AUX Under-Voltage Lockout (UVLO)

The AUX UVLO holds off the GaN power FET if the AUX voltage is below the AUX UVLO voltage. Figure 7-4 shows the AUX UVLO hold-off (blocking) operation. The AUX UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point.

7.3.6 Overcurrent Protection

The LMG3624 implements cycle-by-cycle overcurrent protection for the GaN power FETs. Figure 7-5 shows the cycle-by-cycle overcurrent operation. Every IN logic-high cycle turns on the GaN power FET. If the GaN power FET drain current exceeds the overcurrent threshold current, the overcurrent protection turns off the GaN power FET for the remainder of the IN logic-high duration.

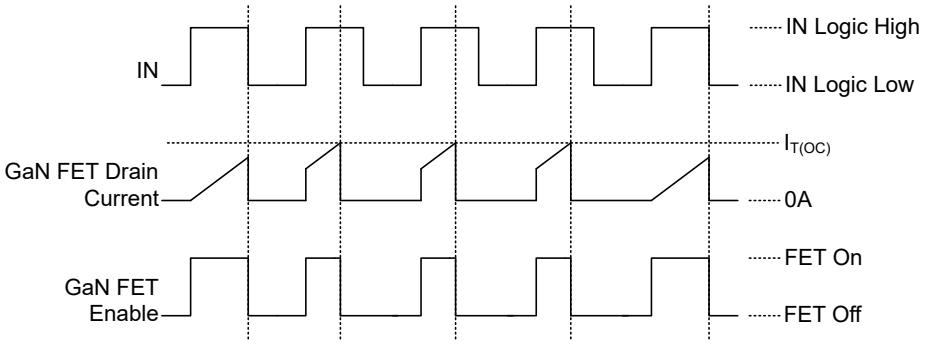


Figure 7-5. Cycle-by-Cycle Overcurrent Protection Operation

An overcurrent protection event is not reported on the $\overline{FLT}$ pin. Cycle-by-cycle overcurrent protection minimizes system disruption because the event is not reported and the protection allows the GaN power FET to turn on every IN cycle.

To prevent the controller from entering a hung state, the low-side overcurrent protection turns off the low-side GaN power FET, thereby generating an artificial CS pin current, as described in Section 7.3.3.

7.3.7 Overtemperature Protection

The overtemperature protection holds off the GaN power FET if the LMG3624 temperature is above the overtemperature protection temperature. Figure 7-4 shows the overtemperature protection hold-off (blocking) operation. The overtemperature protection hysteresis avoids erratic thermal cycling.

An overtemperature fault is reported on the $\overline{FLT}$ pin when the overtemperature protection is asserted. The overtemperature fault is the only fault event reported on the $\overline{FLT}$ pin. The overtemperature protection enables when the AUX voltage is above the AUX power-on reset voltage. The low AUX power-on reset voltage helps the overtemperature protection remain operational when the AUX rail droops during the application cool-down phase.

7.3.8 Fault Reporting

The LMG3624 only reports an overtemperature fault. An overtemperature fault is reported on the $\overline{FLT}$ pin when the Overtemperature Protection function is asserted. The $\overline{FLT}$ pin is an active low open-drain output so the pin pulls low when there is an overtemperature fault.

7.4 Device Functional Modes

LMG3624 has two modes of operation that are controlled by the EN pin. The device is in active mode when the EN is logic high and in standby mode when the EN pin is logic low. In active mode, the IN pin controls the power FET. In standby mode, the IN pin is ignored, the GaN power FET is held off, and the AUX quiescent current reduces to the AUX standby quiescent current.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMG3624 enables the simple adoption of GaN FET technology in switch-mode power-supply applications. The integrated gate driver, low IN input threshold voltage, and wide AUX input-supply voltage allows the LMG3624 to seamlessly pair with common industry power-supply controllers. The current-sense emulation feature saves power and improves thermal conduction.

Using the LMG3624 only requires setting the desired turn-on slew rate with a programming resistor and calculating the current sense resistor.

8.2 Typical Application

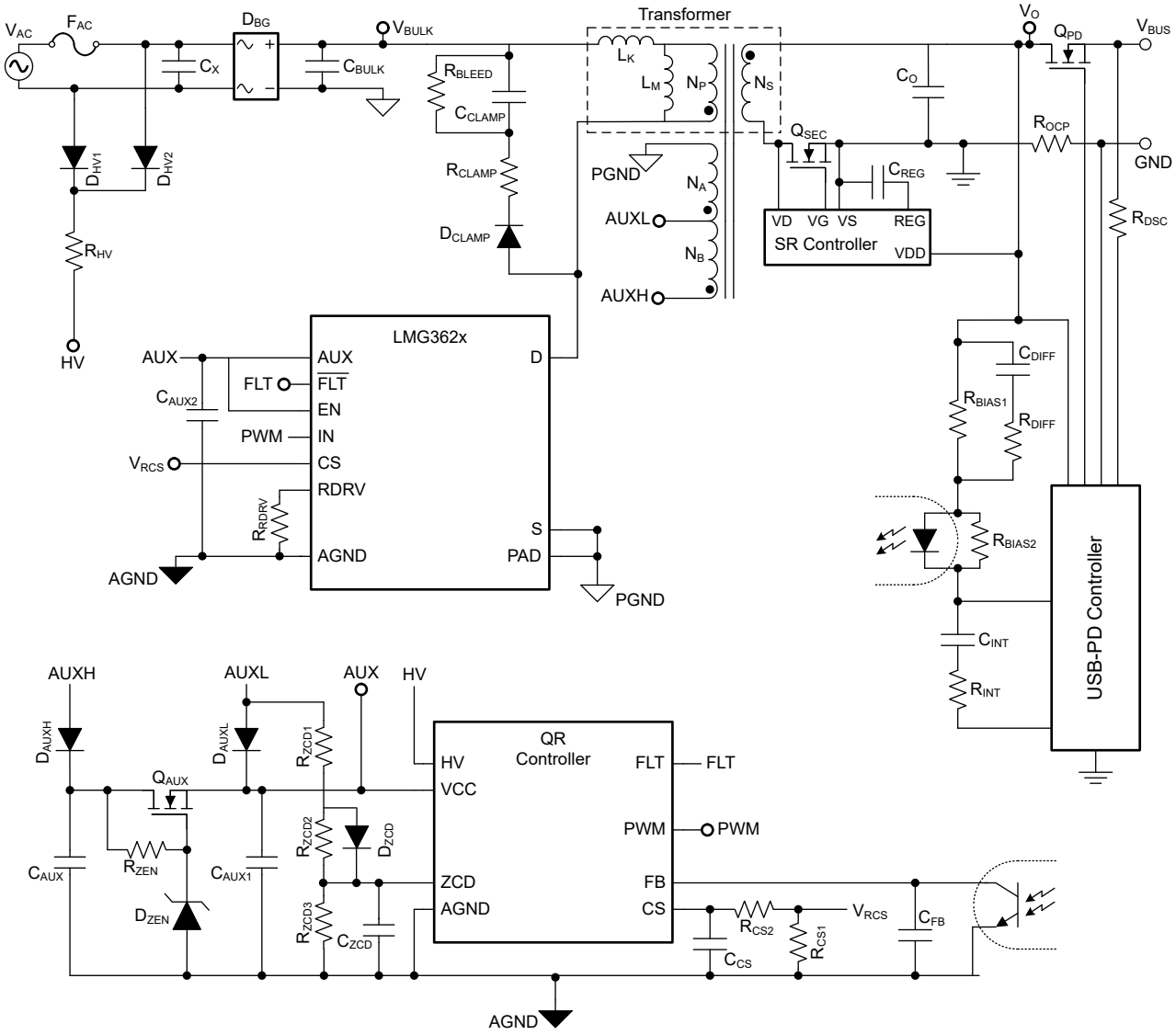


Figure 8-1. 65W USB PD Charger Quasi-Resonant Flyback Converter Application

8.2.1 Design Requirements

Table 8-1. Design Specification

SPECIFICATION	VALUE
Input AC voltage range	90VAC to 264VAC
Input line frequency range	47Hz to 63Hz
Output DC voltage settings	5V, 9V, 15V, 20V
20V-output rated current	3.25A
5V-, 9V-, and 15V-rated output current	3A
Maximum AC input power at no output load	70mW
Minimum efficiency over input AC voltage range at 20V output and full load	93%

8.2.2 Detailed Design Procedure

The 65W USB-PD charger application is taken from the EVM design found in the *Using the LMG3624EVM-081 65W USB-C PD High-Density Quasi-Resonant Flyback Converter* EVM user's guide. The entire quasi-resonant flyback converter design is not given here. Use the *LMG362XX Quasi-Resonant Power-Stage Design Calculator* to create a desired application specific converter design. This detailed design procedure focuses on the specifics of using the LMG3624 in the application.

8.2.2.1 Turn-On Slew-Rate Design

The LMG3624 turn-on slew rates are programmed as discussed in Section 7.3.2. One design consideration is the trade-off between power supply efficiency and EMI or transient ringing. Slower turn-on slew rates lessen EMI and ringing problems but can increase switching losses and vice versa.

In normal quasi-resonant flyback-converter operation, the power switch operates at both ZVS and also non-ZVS valley switching depending on operating conditions. The valley switching occurs at zero transformer current. Therefore, there are no switching cross-over losses in quasi-resonant converters. The only switching loss is the switch-node capacitive loss during valley switching. So the turn-on slew rate has no impact on the converter loss. This seems to indicate to use the slowest turn-on slew rate setting. The turn-on slew rate setting, however, can have a secondary impact on converter loss from the switch turn-on delay.

Depending on how the quasi-resonant controller implements valley switching, the switch turn-on delay can cause the power-converter to switch after the valley and increase capacitive switching losses. Since the switch turn-on delay increases as the turn-on slew rate is decreased, using slower turn-on slew rates can increase power supply losses. If the quasi-resonant controller compensates for switch turn-on delay, then there is no loss penalty for using the slowest turn-on slew rate setting. Otherwise, design optimization between switching noise problems and switching losses must be performed.

The turn-on slew rate is programmed by setting R_{DRV} to the recommended typical programming resistance shown in the *Turn-On Slew-Rate Control* section.

8.2.2.2 Current-Sense Design

The current-sense resistor R_{CS1} is calculated as described in Section 7.3.3 where a traditional current-sense resistor design calculation is first performed and then multiplied by the current-sense emulation inverse gain. The traditional current-sense resistor design calculation, denoted $R_{CS(trad)}$, is for when the current-sense resistor is in series with the power switch and is sensing the full power-switch current.

$$R_{CS1} = 1036 \times R_{CS(trad)} \quad (5)$$

The existence of R_{CS2} is dependent on the quasi-resonant controller. If R_{CS2} is used, the R_{CS2} design calculation can assume a traditional current-sense resistor with a very small value that has no impact on the R_{CS2} calculation. Verify that the R_{CS2} calculation accounts for the significant R_{CS1} value.

8.2.3 Application Curves

The following waveforms show typical switching waveforms. The blue trace is the LMG3624 drain voltage (switch node voltage) and the red trace is the CS pin current-sense emulation voltage.

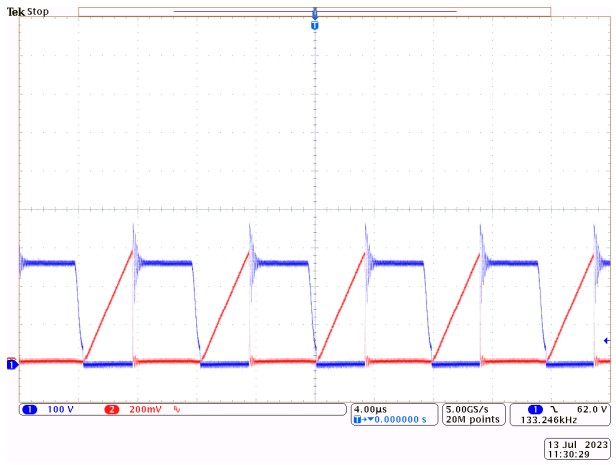


Figure 8-2. V_{IN} = 115VAC V_{OUT} = 20V I_{OUT} = 3.25A

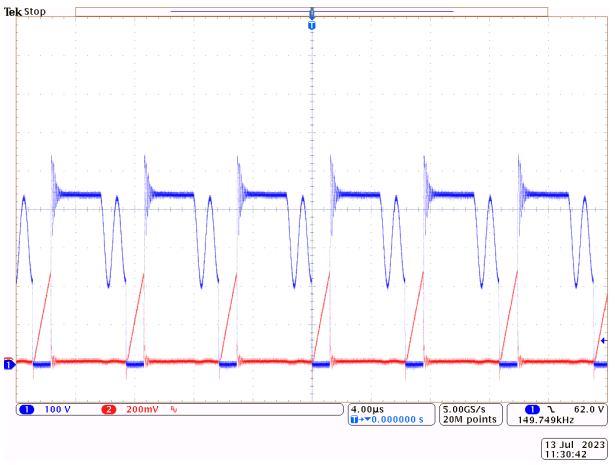


Figure 8-3. V_{IN} = 230VAC V_{OUT} = 20V I_{OUT} = 3.25A

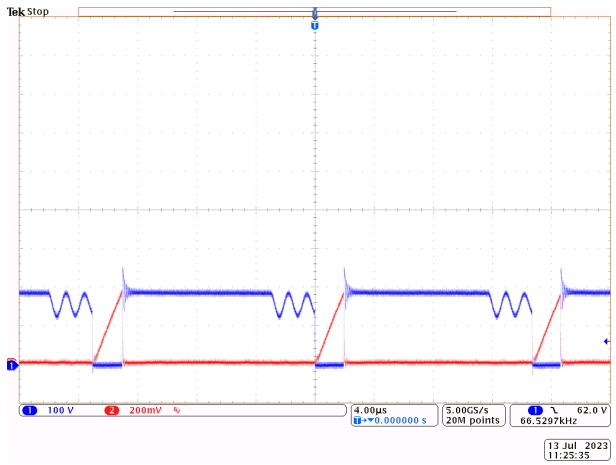


Figure 8-4. V_{IN} = 115VAC V_{OUT} = 5V I_{OUT} = 3A

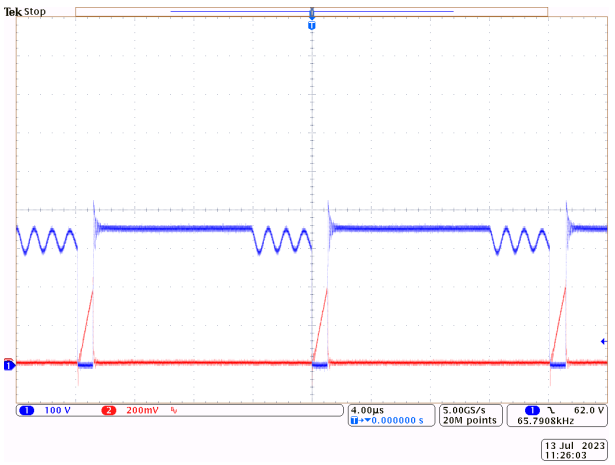


Figure 8-5. V_{IN} = 230VAC V_{OUT} = 5V I_{OUT} = 3A

8.3 Power Supply Recommendations

The LMG3624 operates from a single input supply connected to the AUX pin. The LMG3624 supports being operated from the same supply managed and used by the power supply controller. The wide recommended AUX voltage range of 10V to 26V overlaps common-controller supply-pin turn-on and UVLO voltage limits.

The AUX external capacitance is recommended to be a ceramic capacitor that is at least 0.03µF over operating conditions.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Solder-Joint Stress Relief

Large QFN packages can experience high solder-joint stress. Several best practices are recommended to provide solder-joint stress relief. First, the instructions for the NC1, NC2, and NC3 anchor pins found in Pin Functions must be followed. Second, all the board solder pads must be non-solder-mask defined (NSMD) as shown in the land pattern example in the *Mechanical, Packaging, and Orderable Information* section. Finally, any board trace connected to an NSMD pad must be less than two thirds the width of the pad on the pad side where it is connected. The trace must maintain this two-thirds width limit for as long as it is not covered by solder mask. After the trace is under solder mask, there are no limits on the trace dimensions. All these recommendations are followed in the *Layout Example* section.

8.4.1.2 Signal-Ground Connection

Design the power supply with separate signal and power grounds that only connect in one location. Connect the LMG3624 AGND pin to signal ground. Connect the LMG3624 SL pin and PAD thermal pad to power ground. The power-ground connection serves as the single connection point between the signal and power grounds since the AGND pin, S pin, and PAD thermal pad connect internally. Do not connect the signal and power grounds anywhere else on the board, except as recommended in the next sentence. To facilitate board debugging when the LMG3624 not installed, connect the AGND pad to the PAD thermal pad as Section 8.4.2 shows.

8.4.1.3 CS Pin Signal

As seen with Equation 4, the current-sense signal impedance is three orders of magnitude higher than a traditional current-sense signal. This higher impedance has implications for current-sense signal noise susceptibility. Minimize routing the current-sense signal near any noisy traces. Place the current-sense resistor and any filtering capacitors at the far end of the trace next to the controller current-sense input pin.

8.4.2 Layout Example

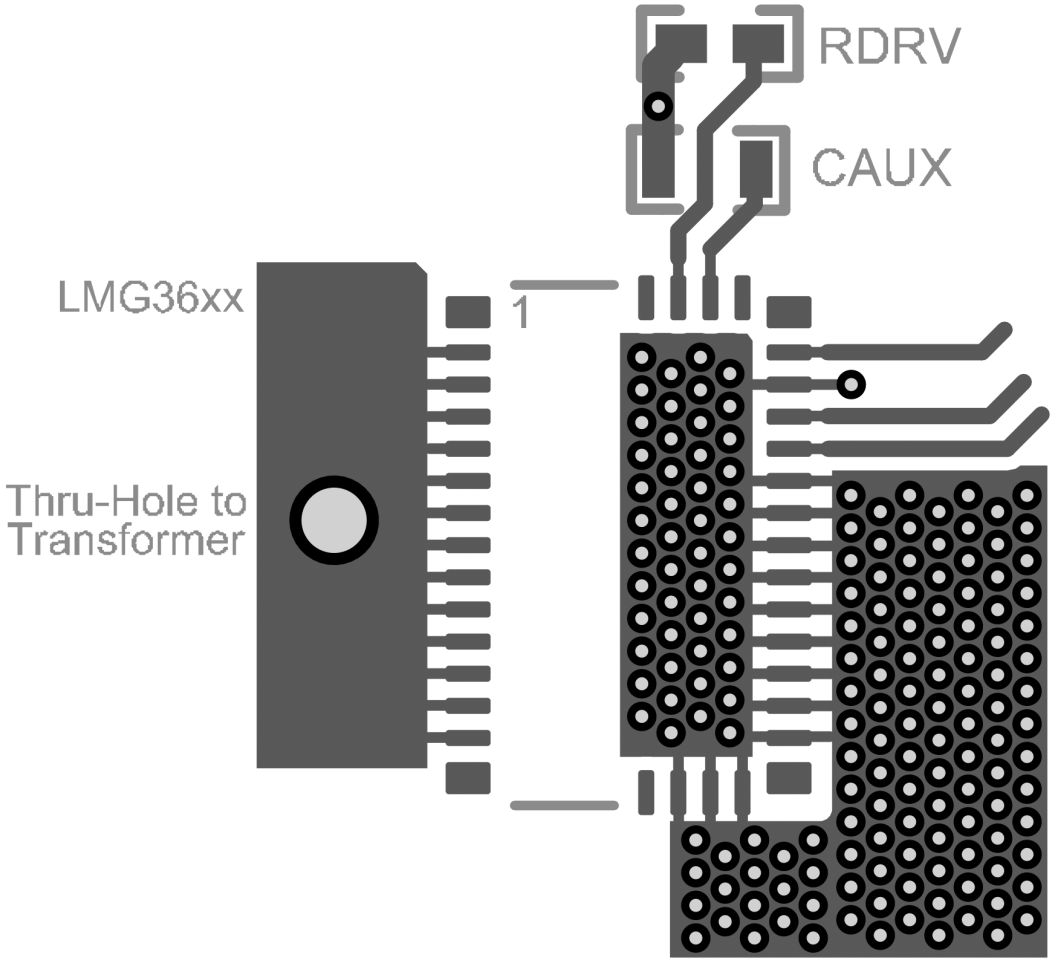


Figure 8-6. PCB Top Layer (First Layer)

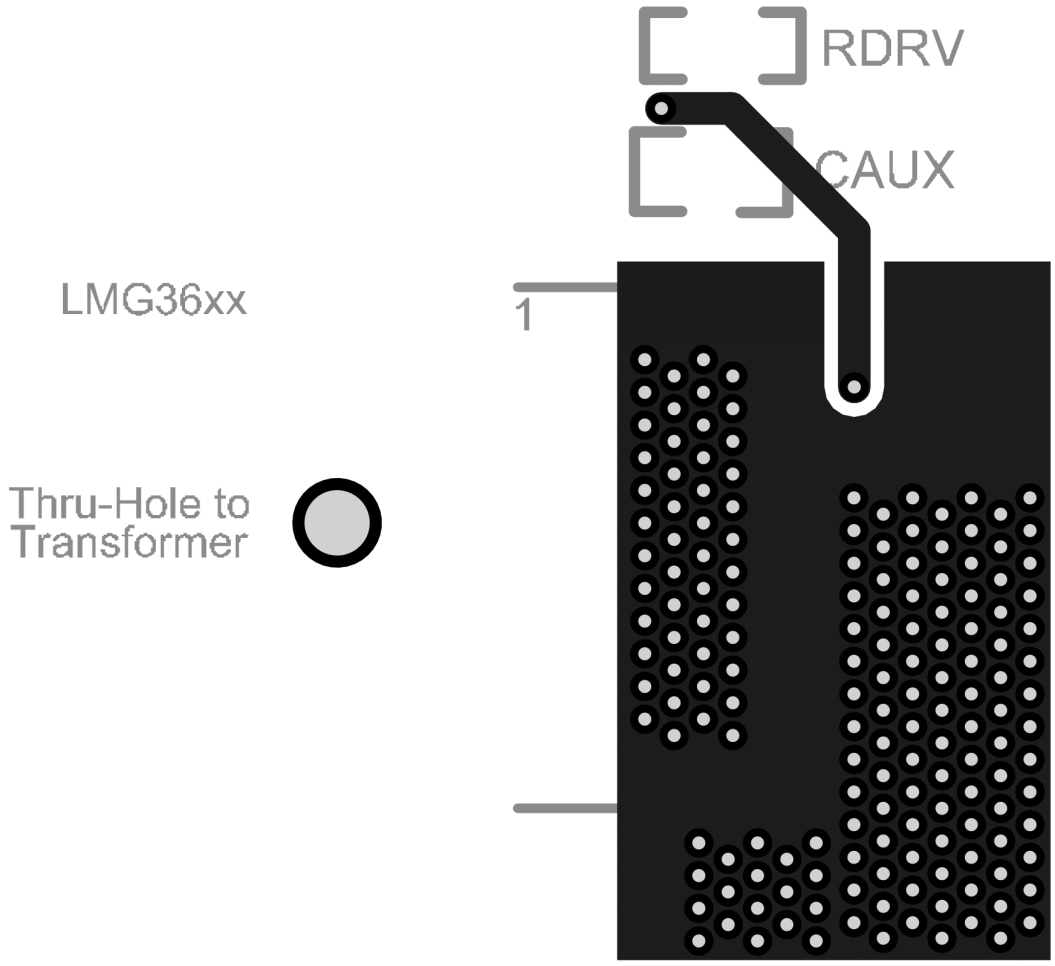


Figure 8-7. PCB Bottom Layer (Second Layer)

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *LMG362XX Quasi-Resonant Power-Stage Design Calculator*
- Texas Instruments, *Using the LMG3624EVM-081 65W USB-C PD High-Density Quasi-Resonant Flyback Converter* EVM user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2025) to Revision C (September 2025)	Page
• Added LMG3624Y information throughout	1
• Updated with LMG3624Y data and separated LMG3624 data	9
• Added LMG3624Y to Slew-Rate Settings	16

Changes from Revision A (June 2024) to Revision B (April 2025)	Page
• Updated voltage rating from 650V to 700V and drain-source on resistance from 170mΩ to 155mΩ	1
• Updated text in the *Applications* section	1
• Updated voltage rating with Footnote (2), and added Footnote (3) in *Absolute Maximum Ratings* section	5
• Added max value of drain-source on resistance at 25℃ and Updated typical value of drain-source on resistance at both 25℃ and 125℃ in the *GAN POWER FET* sub-section of *Electrical Characteristics* section	5
• Added min value of temperature fault – postive-going threshold temperature in the *OVERTEMPERATURE PROTECTION* sub-section of *Electrical Characteristics* section	5

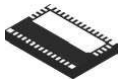
- Added Output Capacitance vs Drain-Source Voltage graph and Output Capacitance Stored Energy vs Drain-Source Voltage graphs in *Typical Characteristics* section..... 10
- Updated figure and added sentence clarifying application usage in *GaN Power FET Switching Capability* section..... 15
- Updated figure in *Layout Example* the section..... 24

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Mechanical Data

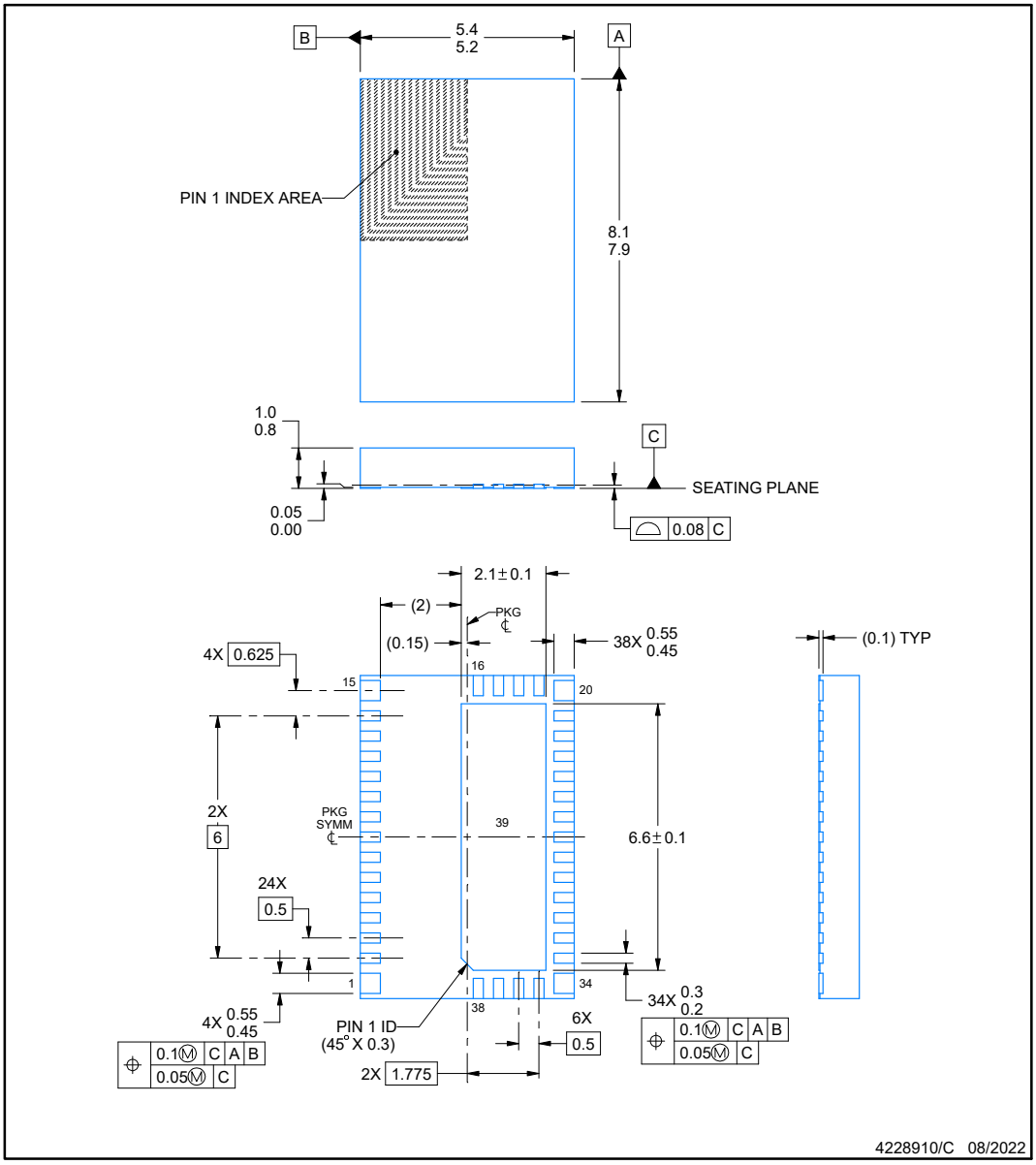
REQ0038A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



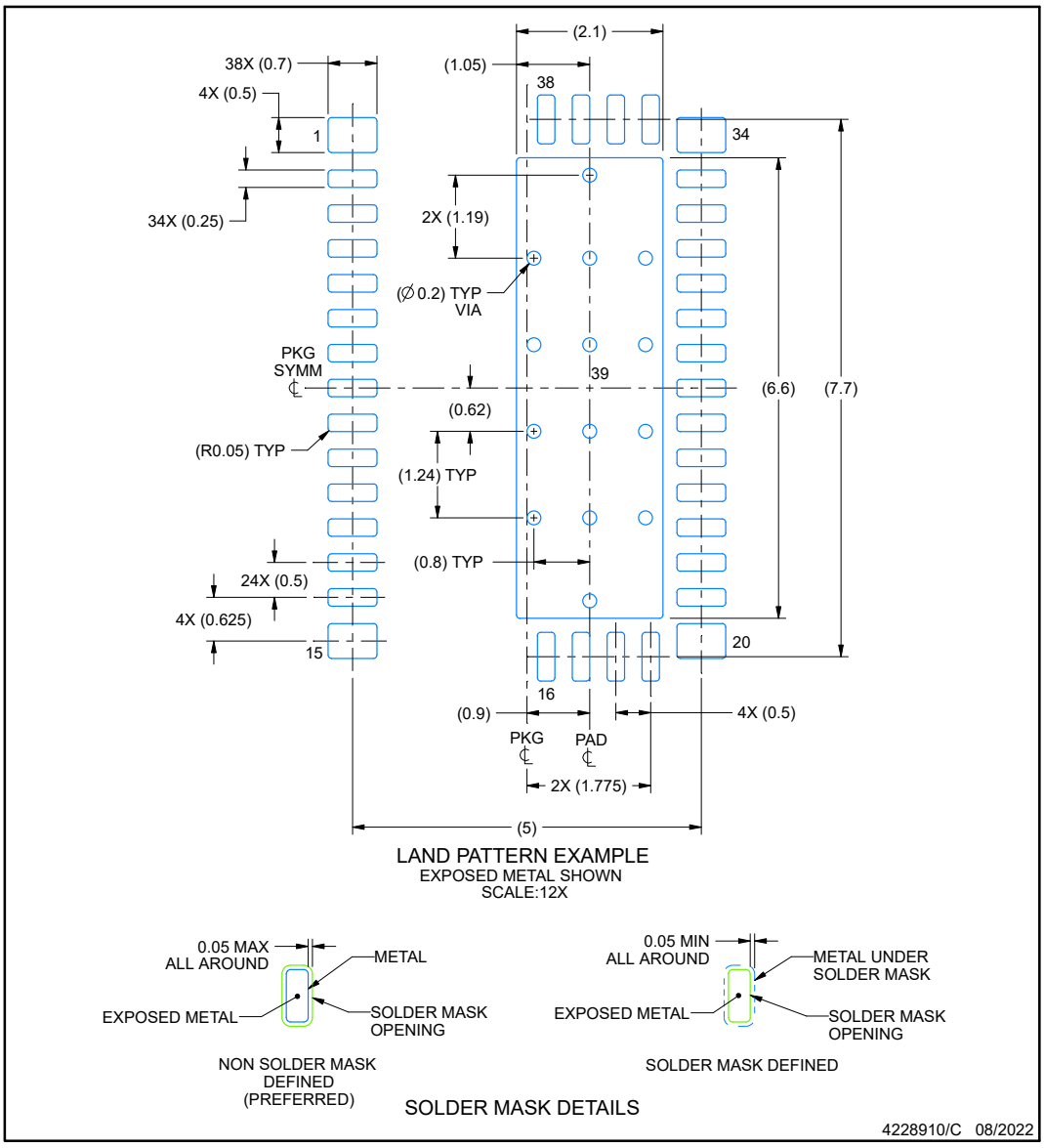
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REQ0038A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



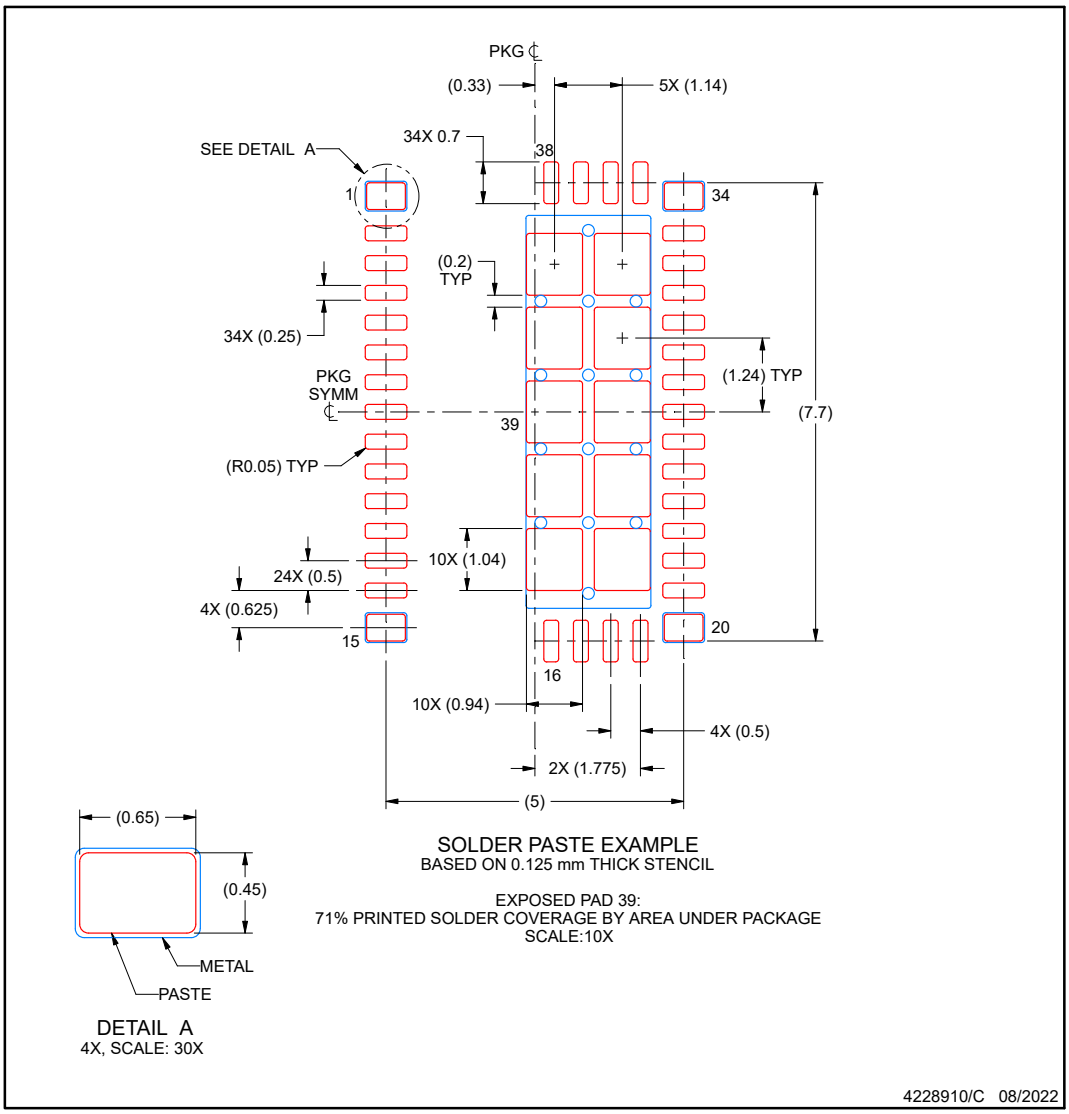
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

REQ0038A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4228910/C 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG3624REQR	Active	Production	VQFN (REQ) | 38	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	LMG3624 NNNNC
LMG3624REQR.A	Active	Production	VQFN (REQ) | 38	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	LMG3624 NNNNC
LMG3624REQR.B	Active	Production	VQFN (REQ) | 38	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMG3624YREQR	Active	Production	VQFN (REQ) | 38	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	LMG3624Y NNNNC
LMG3624ZREQR	Active	Production	VQFN (REQ) | 38	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168HRS	-40 to 125	LMG3624 NNNNC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

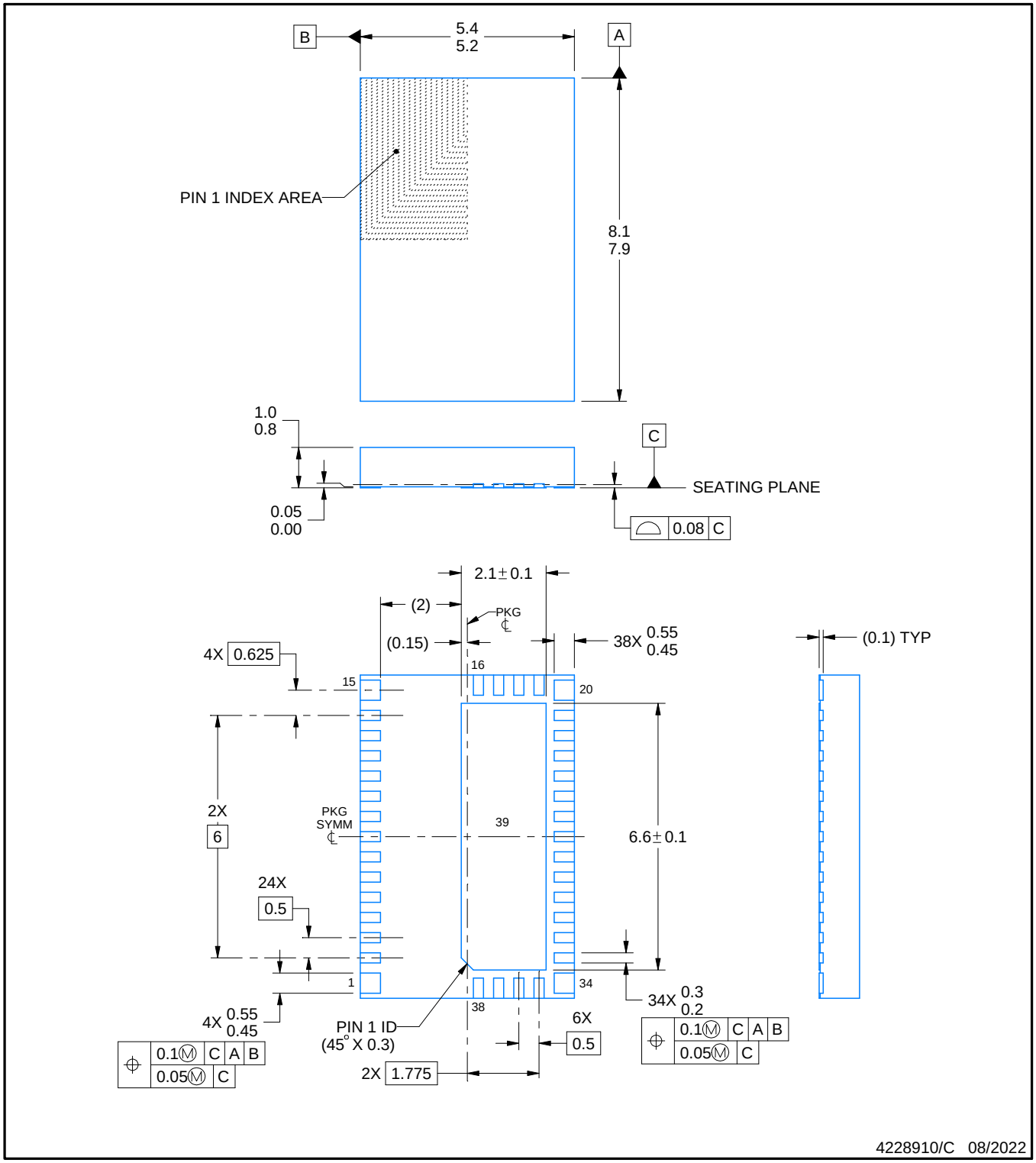
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

REQ0038A

PACKAGE OUTLINE

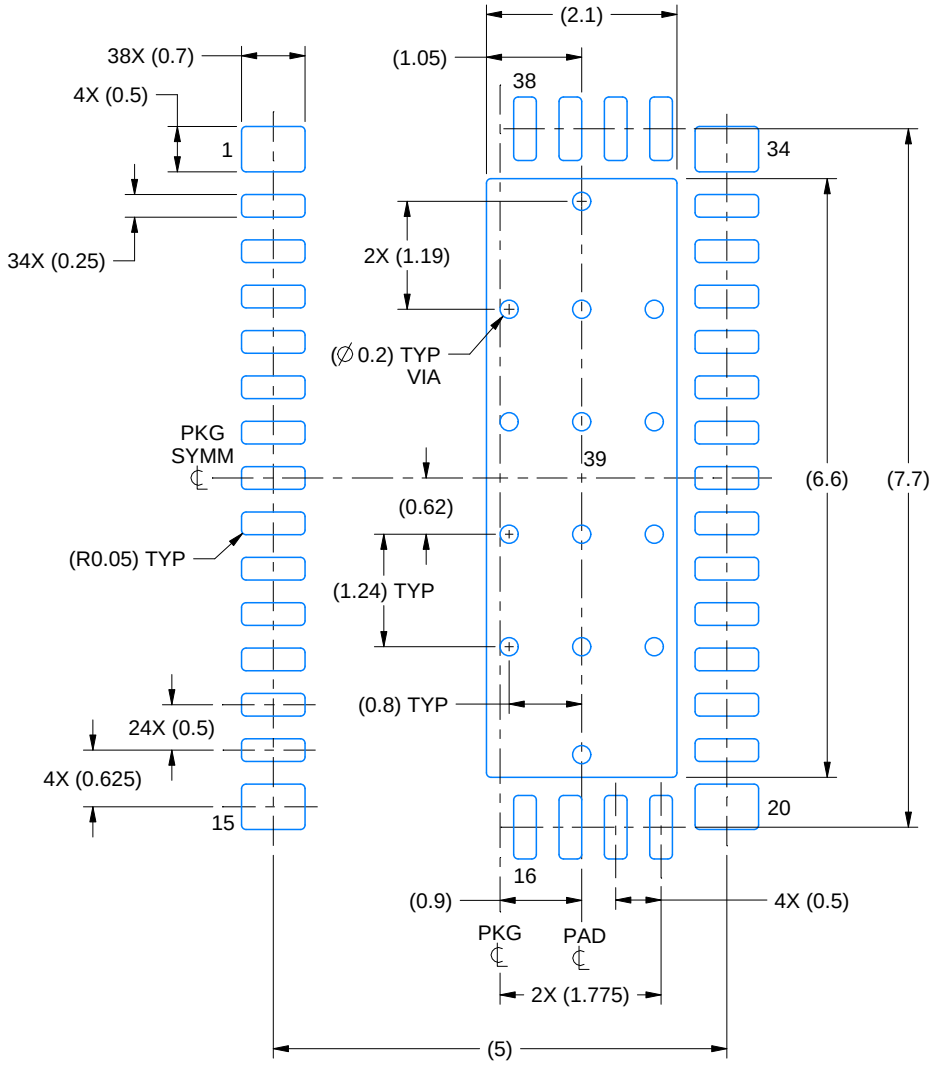
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

SOLDER MASK DETAILS

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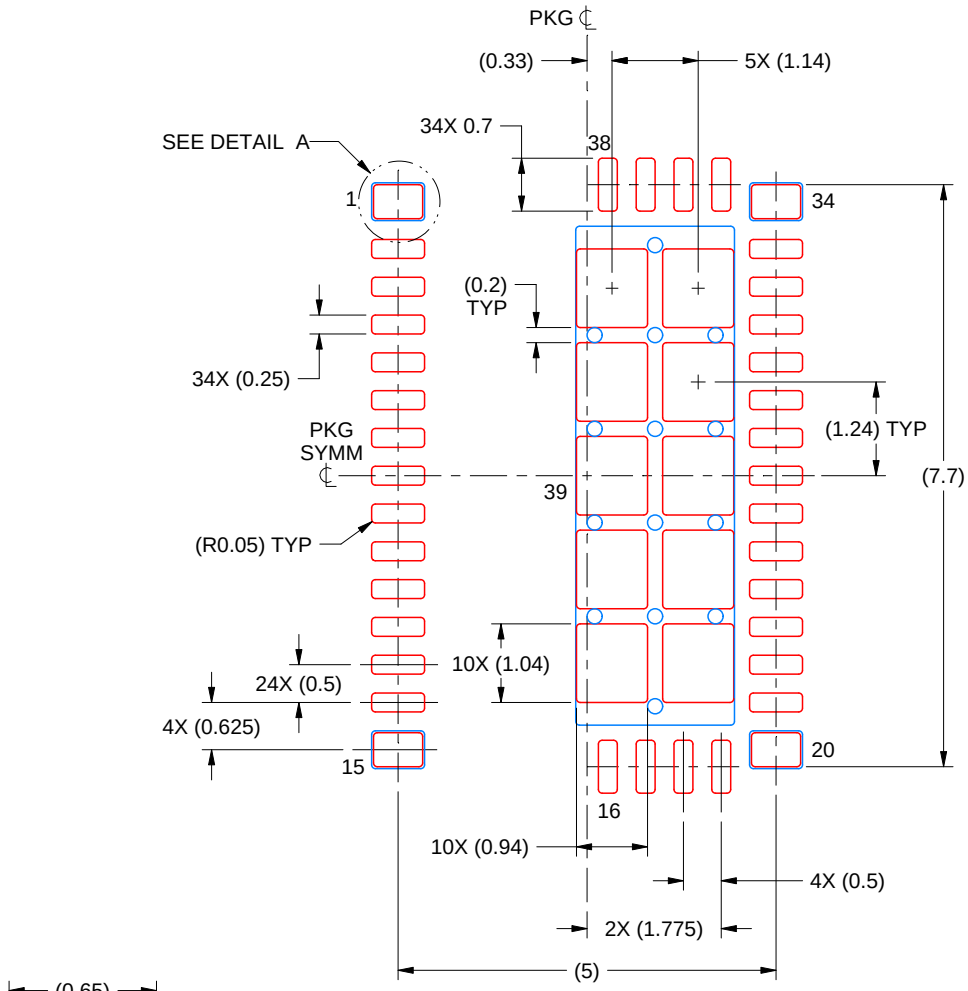
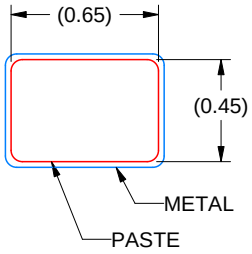
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 39:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:10X



DETAIL A
4X, SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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