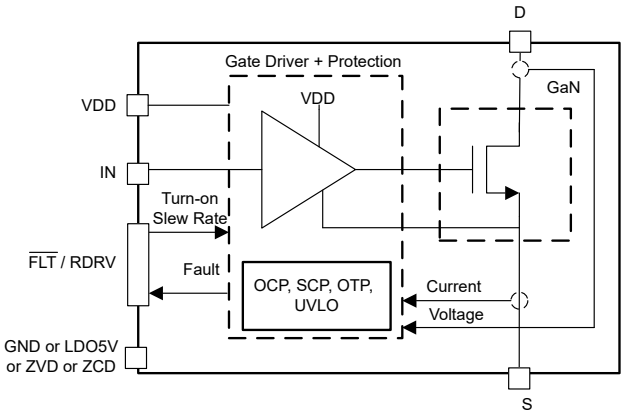
LMG366xR025 650V 25mΩ GaN FET With Integrated Driver and Protection

1 Features

- 650V 25mΩ GaN power FET with integrated gate driver
  - >200V/ns FET hold-off
  - 10V/ns to 80V/ns slew rate for optimization of switching performance and EMI mitigation
  - Operates with supply pin and input logic pin voltage range from 9V to 26V
- Robust protection
  - Cycle-by-cycle overcurrent and latched short-circuit protection with <300ns response
  - Withstands 720V surge while hard-switching
  - Self-protection from internal overtemperature and UVLO monitoring
- Advanced power management
  - LMG3666R025 includes zero-voltage detection (ZVD) feature that facilitates soft-switching converters and an adjustable turn-off slew rate from 10V/ns to full speed.
  - LMG3667R025 includes zero-current detection (ZCD) feature that facilitates soft-switching converters and an adjustable turn-off slew rate from 10V/ns to full speed.
- Top-side cooled 10.1mm × 15.2mm TOLT package separates electrical and thermal paths for lowest power loop inductance

2 Applications

- Open rack server PSU
- Merchant telecom rectifiers
- Common redundant power supply
- Uninterruptible power supplies
- Solar inverters and industrial motor drives



Simplified Block Diagram

3 Description

The LMG366xR025 GaN FET with integrated driver and protection is targeted at switch-mode power converters and enables designers to achieve new levels of power density and efficiency.

Adjustable gate driver strength allows the control of turn-on and maximum turn-off slew rates independently, which can be used to actively control EMI and optimize switching performance. Turn on slew rate varies from 10V/ns to 80V/ns, while the turn off slew rate control is available only in LMG3666R025 and LMG3667R025. The turn off slew rate can be limited from 10V/ns to a maximum based on the magnitude of load current. Protection features include under-voltage lockout (UVLO), cycle-by-cycle overcurrent limit, and short-circuit and overtemperature protection. The LMG3661R025 provides a 5V LDO output on LDO5V pin that powers external digital isolators. The LMG3666R025 includes the zero-voltage detection (ZVD) feature which provides a pulse output from the ZVD pin when zero-voltage switching is realized. The LMG3667R025 includes the zero-current detection (ZCD) feature that sets the ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG366xR025	KLG (TOLT,16)	10.1mm × 15.2mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	LDO 5V OUTPUT	ZERO-VOLTAGE DETECTION FEATURE	ZERO-CURRENT DETECTION FEATURE
LMG3660R025	—	—	—
LMG3661R025 (1)	Yes	—	—
LMG3666R025 (1)	—	Yes	—
LMG3667R025 (1)	—	—	Yes

(1) Product Preview

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4 Pin Configuration and Functions

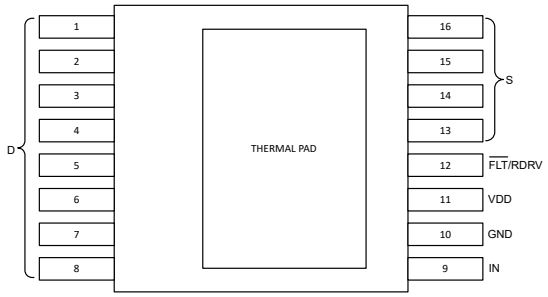

Figure 4-1. LMG3660R025, TOLT Package (Top View)

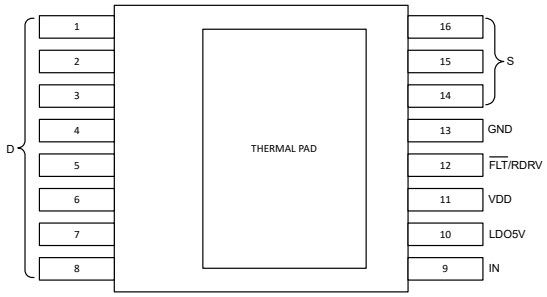

Figure 4-2. LMG3661R025, TOLT Package (Top View)

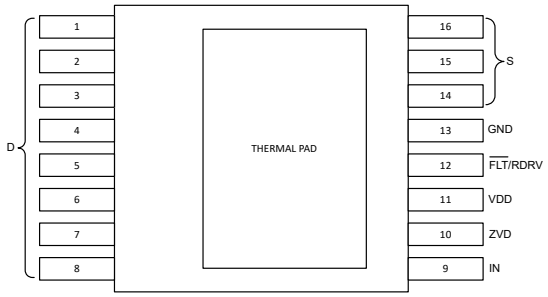

Figure 4-3. LMG3666R025, TOLT Package (Top View)

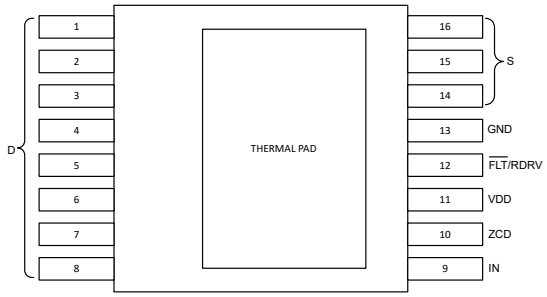

Figure 4-4. LMG3667R025, TOLT Package (Top View)

Table 4-1. Pin Functions

PIN					TYPE (1)	DESCRIPTION
NAME	LMG3660 R025	LMG3661 R025	LMG3666 R025	LMG3667 R025		
D	1 - 8	1 - 8	1 - 8	1 - 8	P	GaN FET drain.
$\overline{\text{FLT}}$/RDRV	12	12	12	12	O, I	Fault monitoring and turn-on drive strength selection pin. Connect a resistor from this pin to GND to set the turn-on drive strength. Slew rates are set one time at the time of power up, then the pin is used for fault monitoring.
GND	10	13	13	13	G	Signal ground. Internally connected to S, and THERMAL PAD.
IN	9	9	9	9	I	CMOS compatible non inverting input used to turn the FET on and off
LDO5V	—	10	—	—	P	5V LDO output for external digital isolator.
S	13 - 16	14 - 16	14 - 16	14 - 16	P	GaN FET source
THERMAL PAD	—	—	—	—	—	Thermal pad. Internally connected to S
VDD	11	11	11	11	P	Device input supply
ZCD	—	—	—	10	O, I	Zero-current detection and turn-off drive strength selection pin. Connect a resistor from this pin to GND to set the turn-off drive strength. Slew rates are set one time at the time of power up, then the pin is used as a push-pull digital output that sets ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.

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Table 4-1. Pin Functions (continued)

PIN					TYPE (1)	DESCRIPTION
NAME	LMG3660 R025	LMG3661 R025	LMG3666 R025	LMG3667 R025		
ZVD	—	—	10	—	O, I	Zero-voltage detection and turn-off drive strength selection pin. Connect a resistor from this pin to GND to set the turn-off drive strength. Slew rates are set one time at the time of power up, then the pin is used as a push-pull digital output that provides zero-voltage detection signal to indicate if device achieves zero-voltage switching in current switching cycle.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to GND/S(1)

			MIN	MAX	UNIT
V_{DS}	Drain-source voltage, FET off			650	V
$V_{DS(surge)}$	Drain-source voltage, surge condition, FET off			720	V
$V_{DS(tr)(surge)}$	Drain-source transient ringing peak voltage, surge condition, FET off			800	V
	Pin voltage	VDD	-0.5	26	V
		IN	-5(2)	28	V
		$\overline{FLT}$/RDRV, ZVD (LMG3666 only), ZCD (LMG3667 only)	-0.5	5.5	V
		LDO5V (LMG3661 only)		5.5	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on. Tj = 25℃(3)		-62	62	A
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on. Tj = 150℃(3)		-51.5	51.5	A
$I_{D(pulse)}$	Pulse drain current, FET on, t_p < 10µs. Tj = 25℃(3)		-85	85	A
$I_{S(cnts)}$	Source (S to D) continuous current, FET off. Tj = 25℃			62	A
$I_{S(cnts)}$	Source (S to D) continuous current, FET off. Tj = 150℃			51.5	A
T_J	Operating junction temperature(4)		–40	175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The IN pin voltage is limited to a minimum of -0.5V in steady state, with a transient tolerance of -5V for duration <1µs.
(3) Absolute maximum ratings are limited by device internal overcurrent protection feature. However, the FET drain intrinsic positive pulsed current rating for t_p < 10µs varies with junction temperature; 81A typ. at 150℃. The positive pulsed current must remain below the overcurrent threshold to avoid the FET being automatically shut off.
(4) Refer to the Electrical and Switching Characteristics Tables for junction temperature test conditions.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to GND/S

			MIN	NOM	MAX	UNIT
	Supply voltage	VDD	9		24	V
	Input voltage	IN	0		26	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on. Tj = 25℃		-50		50	A
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on. Tj = 150℃		-38		38	A
	Positive source current	LDO5V (LMG3661 only)			25	mA
$RDRV_{on}$	Resistance from external turn-on slew rate control resistor between $\overline{FLT}$/RDRV to GND		29.4		open	kΩ

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Unless otherwise noted: voltages are respect to GND/S

		MIN	NOM	MAX	UNIT
$RDRV_{off}$	Resistance from external turn-off slew rate control resistor between ZVD to GND (LMG3666) or ZCD to GND (LMG3667)	32.4		open	kΩ

5.4 Thermal Information

THERMAL METRIC[1]		KLG(TOLT) 16 PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.29	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/S; –40℃ ≤ T_J ≤ 150℃; VDD = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ & $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$R_{DS(on)}$	Drain-source on resistance	T_J = 25°C, I_L = 25A		23	32	mΩ
$R_{DS(on)}$	Drain-source on resistance	T_J = 150°C, I_L = 25A		46		mΩ
V_{SD}	Source-drain third-quadrant voltage	T_J = 25°C, I_{SD} = 0.1A		1.8		V
V_{SD}	Source-drain third-quadrant voltage	T_J = 150°C, I_{SD} = 0.1A		1.6		V
V_{SD}	Source-drain third-quadrant voltage	T_J = 25°C, I_{SD} = 35A		3.4		V
V_{SD}	Source-drain third-quadrant voltage	T_J = 150°C, I_{SD} = 35A		4.8		V
I_{DSS}	Drain leakage current	T_J = 25°C, V_{DS} = 650V		7		μA
I_{DSS}	Drain leakage current	T_J = 150°C, V_{DS} = 650V		10		μA
C_{OSS}	Output capacitance	V_{DS} = 400V		230		pF
Q_{OSS}	Output charge	V_{DS} = 0V to 400V		150		nC
E_{OSS}	Output capacitance stored energy	V_{DS} = 0V to 400V		23		μJ
$C_{OSS(tr)}$	Time related effective output capacitance	V_{DS} = 0V to 400V		400		pF
$C_{OSS(er)}$	Energy related effective output capacitance	V_{DS} = 0V to 400V		270		pF
Q_{RR}	Reverse recovery charge			0		nC
OVERCURRENT AND SHORT-CIRCUIT PROTECTIONS						
$I_{T(OC)}$	Overcurrent fault - threshold current	T_J = -40℃	57	67	70.5	A
$I_{T(OC)}$	Overcurrent fault - threshold current	T_J = 25℃	50	59	62	A
$I_{T(OC)}$	Overcurrent fault - threshold current	T_J = 150℃	38	46	51.5	A
$V_{T(Idsat)}$	Saturation current detection - threshold voltage		8.5	9	9.6	V
OVERTEMPERATURE PROTECTION						
T_{T+}	Temperature fault - positive-going threshold temperature			190		°C
$T_{T(hyst)}$	Temperature fault - threshold temperature hysterisis			20		°C
IN						
$V_{IN,IT+}$	Positive-going input threshold voltage		1.6	2	2.45	V
$V_{IN,IT-}$	Negative-going input threshold voltage		0.6	0.9	1.3	V
$V_{IN,IT(hyst)}$	Input threshold voltage hysteresis			1		V
R_{PDN}	Pull-down input resistance		115	150	185	kΩ

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Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/S; –40°C ≤ T_J ≤ 150°C; VDD = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ & $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{FLT}$/RDRV						
V_{OL}	Low-level output voltage	Output sink 8mA		0.2	0.4	V
V_{OH}	High-level output voltage	Output source 8mA	4.5	4.8		V
VDD						
$I_{VDD(ON)}$	Quiescent current when FET is ON	IN=1		1.2	16	mA
$I_{VDD(OFF)}$	Quiescent current when FET is OFF	IN=0		0.8	1.1	mA
$I_{VDD(op)}$	Operating current at 140 kHz	f_{sw} = 140kHz, V_{bus} = 400V, Hard-switched, 50% duty cycle.		6	10	mA
$V_{VDD, T+ (UVLO)}$	UVLO- positive-going threshold voltage		8.1	8.5	8.9	V
$V_{VDD, T- (UVLO)}$	UVLO- negative-going threshold voltage		7.6	8	8.4	V
$V_{VDD, T (hyst)}$	UVLO- threshold voltage hystresis			0.5		V
V_{LDO5V_25mA}	Output Voltage	LDO5V sourcing 25mA	4.75	5	5.25	V
I_{SC_LDO5V}	Short-circuit current		25	50	100	mA

5.6 Switching Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/S; –40°C ≤ T_J ≤ 150°C; V_{DD} = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ and $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIMES						
$t_{d(on)}$	Turn-on delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 0A, 80V/ns		45		ns
$t_{ir(on)}$	Turn-on current rise time + delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 15A, 80V/ns		45		ns
$t_{vf(on)}$	Turn-on voltage falling time	From V_{DS} < 320V to V_{DS} < 80V, V_{BUS} = 400V, L_{HB} current = 15A, 80V/ns		3.5		ns
	Turn-on slew rate	dv/dt when V_{DS} = 200V, V_{BUS} = 400V, L_{HB} current = 15A, 80V/ns		80		V/ns
	Pulse width distortion	slew-rate setting at 80V/ns, IDS = 26A, Measure difference between IN pulse width & VSW pulse width		9	20	ns
	Minimum input pulse changing the output L-H-L	slew-rate setting at 80V/ns such that SW crosses 200V			50	ns
$t_{d(off)}$	Turn-off delay time at full speed	From V_{IN} < $V_{IN,IT-}$ to V_{DS} ≥ 80V. V_{BUS} = 400V, I_L = 30A, fastest or full turn-off speed.		30		ns
$t_{vr(off)}$	Turn-off voltage rise time at full speed	From V_{DS} ≥ 80V to V_{DS} ≥ 320V. V_{BUS} = 400V, I_L = 30A, fastest or full turn-off speed.		5.5		ns
STARTUP TIMES						
T_{DRV_START}	Driver startup delay (LMG3660, LMG3661)	From Driver supply crossing UVLO to switch turning on if IN is high.	80	100	150	µs
	Driver startup delay (LMG3666, LMG3667)	From Driver supply crossing UVLO to switch turning on if IN is high.	160	190	280	µs

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Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/S; –40°C ≤ T_J ≤ 150°C; V_{DD} = 12V; $\overline{FLT}$/RDRV resistances $RDRV_{on}$ and $RDRV_{off}$ are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAULT TIMES						
$t_{off(OC)}$	Overcurrent fault FET turn-off time, FET on before overcurrent	From $I_D \geq I_{T(OC)}$ to V_{ds}> 10V, di/dt = 100A/µs, in the fastest turn-off speed		340	480	ns
$t_{off(OC\_ON)}$	Overcurrent total on time, turn-on into overcurrent.	From V_{ds} <= 10V to $V_{ds} \geq$ 10V, turning on at 110% of OC level, at 80 V/ns turn-on slew rate and fastest turn-off speed.		420	580	ns
$t_{off\_cur(SC\_ON)}$	SC on time measured through drain current	LS V_{ds} > 10V, measured from LS I_{ds} > 50A to I_{ds} < 50A, at 80 V/ns turn-on slew rate in a half-bridge configuration.	100	215	500	ns
$t_{off\_cur(SC)}$	SC response time with source current measurement	From LS Vds>9V to LS Ids<50A, at 80 V/ns turn-on slew rate in a half-bridge configuration. .		155	350	ns
	Latched-Fault reset time	Time required to hold gate driver input low to clear latched-fault	300	380	450	µs
ZERO-VOLTAGE DETECTION AND ZERO-CURRENT DETECTION TIMES						
	ZCD delay	Current crossing zero (low to high) to ZCD output pulse di/dt = 0.03A/ns	16	18	68	ns
t_{DL_ZVD}	ZVD delay	In rising to ZVD output pulse. 100V/ns turn-on speed.	13	20	50	ns
t_{WD_ZVD}	ZVD pulse width	V_{bus} = 10V, I_L = 5A, measure ZVD pulse width	90	120	170	ns
	ZVD sensing time	Sensing time to fet turn on (100V/ns). IL=2A		11	25	ns

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6 Parameter Measurement Information

6.1 Switching Parameters

Circuit Used to Determine Switching Parameters shows the circuit used to measure most switching parameters. The top device in this circuit re-circulates the inductor current and functions in third-quadrant mode only. The bottom device is the active device that turns on to increase the inductor current to the desired test current. The bottom device turns off and on to create switching waveforms at a specific inductor current. Both the drain current (at the source) and the drain-source voltage are measured. Measurement to Determine Propagation Delays and Slew Rates shows the specific timing measurement. TI recommends using the half-bridge as a double pulse tester. Excessive third-quadrant operation can overheat the top device.

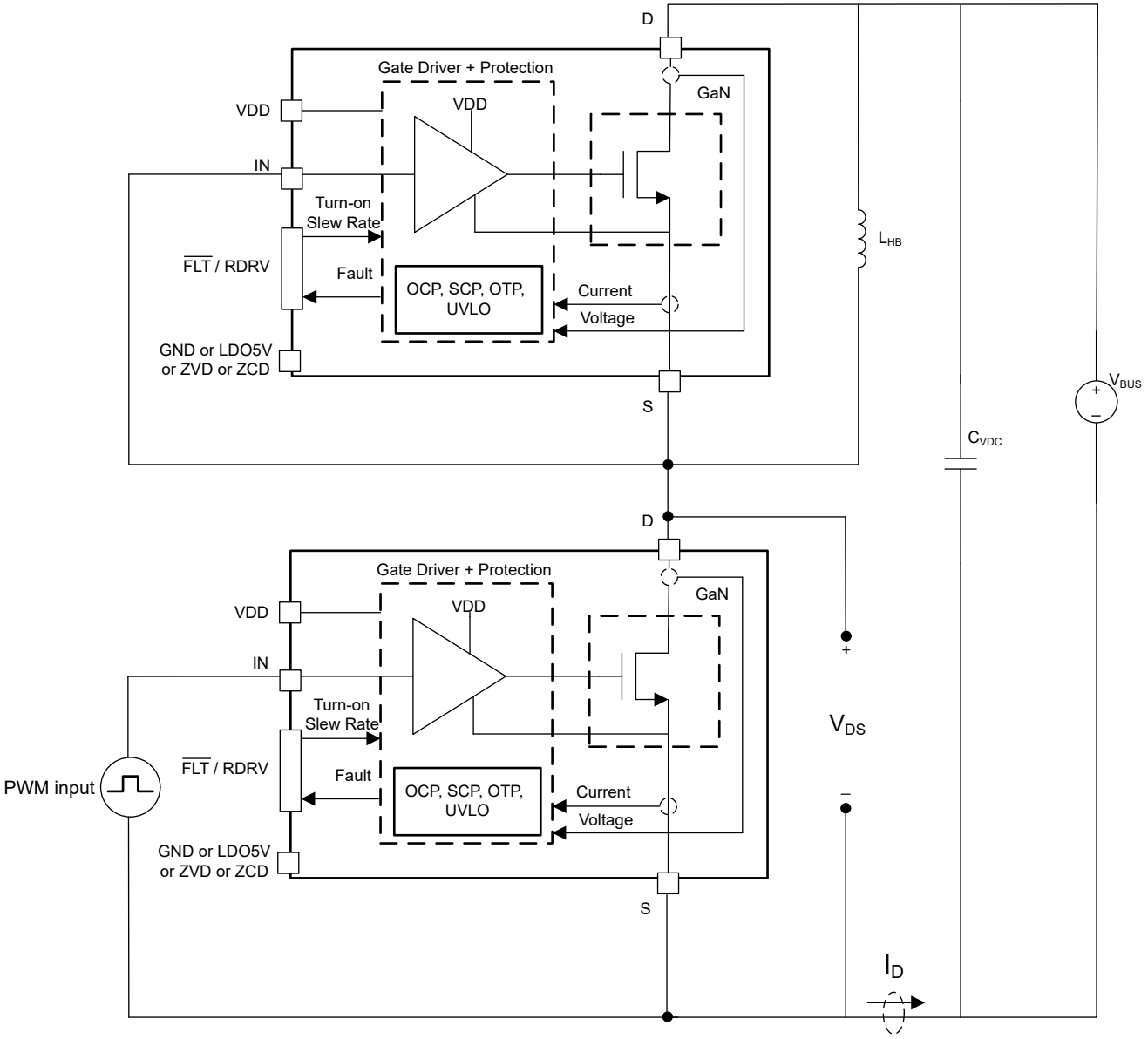

Figure 6-1. Circuit Used to Determine Switching Parameters

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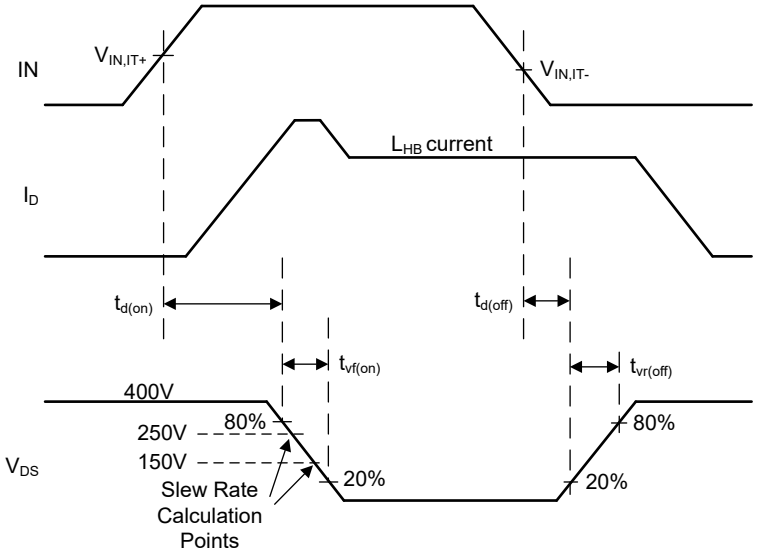


Figure 6-2. Measurement to Determine Propagation Delays and Slew Rates

6.1.1 Turn-On Times

The turn-on transition has two timing components: turn-on delay time and turn-on voltage fall time. The turn-on delay time is from when IN goes high to when the drain-source voltage falls 20% below the bus voltage. The turn-on voltage fall time is from when drain-source voltage falls 20% below the bus voltage to when the drain-source voltage falls 80% below the bus voltage. The turn-on timing components are a function of the turn-on drive strength resistance $RDRV_{on}$ connected to the $\overline{FLT}$/RDRV pin.

6.1.2 Turn-Off Times

The turn-off transition has two timing components: turn-off delay time and turn-off voltage rise time. The turn-off delay time is from when IN goes low to when the drain-source voltage rises to 20% of the bus voltage. The turn-off voltage rise time is from when the drain-source voltage rises from 20% of the bus voltage to when the drain-source voltage to 80% of the bus voltage. The turn-off timing components are dependent on the L_{HB} load current, however LMG3666R025 and LMG3667R025 also includes the ability to limit turn-off drive strength. When the drain-to-source current is sufficiently high and the turn-off drive strength is limited, the timing components are dependent on the programming resistor $RDRV_{off}$ connected to the ZVD pin or ZCD pin.

6.1.3 Drain-Source Turn-On and Turn-off Slew Rate

The drain-source turn-on and turn-off slew rate is measured on V_{DS} at approximately the midpoint of the bus voltage; the units are in volts per nanosecond. The resistor $RDRV_{on}$ connect to the $\overline{FLT}$/RDRV pin and program the turn-on slew rate. The resistor $RDRV_{off}$ connect to the ZVD pin in LMG3666R025 or ZCD pin in LMG3667R025 limits the turn-off slew rate.

6.1.4 Zero-Voltage Detection Times (LMG3666R025 only)

Figure 6-3 defines the switching timings related to the zero-voltage detection (ZVD) block, and shows the drain-to-source voltage, IN pin signal, and ZVD output signals of the device. When the device achieves zero-voltage switching (ZVS), the ZVD pin outputs a pulse-signal with width T_{WD_ZVD}, and the delay time in between IN pins rising edge and ZVD pulses rising edge is defined as T_{DL_ZVD}. A certain third quadrant conduction time is required to allow the device detecting a zero-voltage switching, and T_{3rd_ZVD} indicates this timing. See the Zero-Voltage Detection (ZVD) (LMG3656R070 Only) section for more information about the ZVD timing parameters.

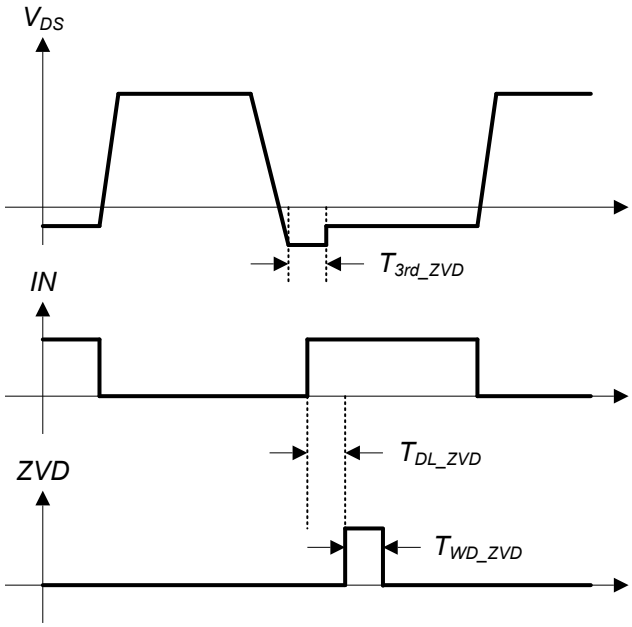


Figure 6-3. ZVD Timing Specifications

7 Detailed Description

7.1 Overview

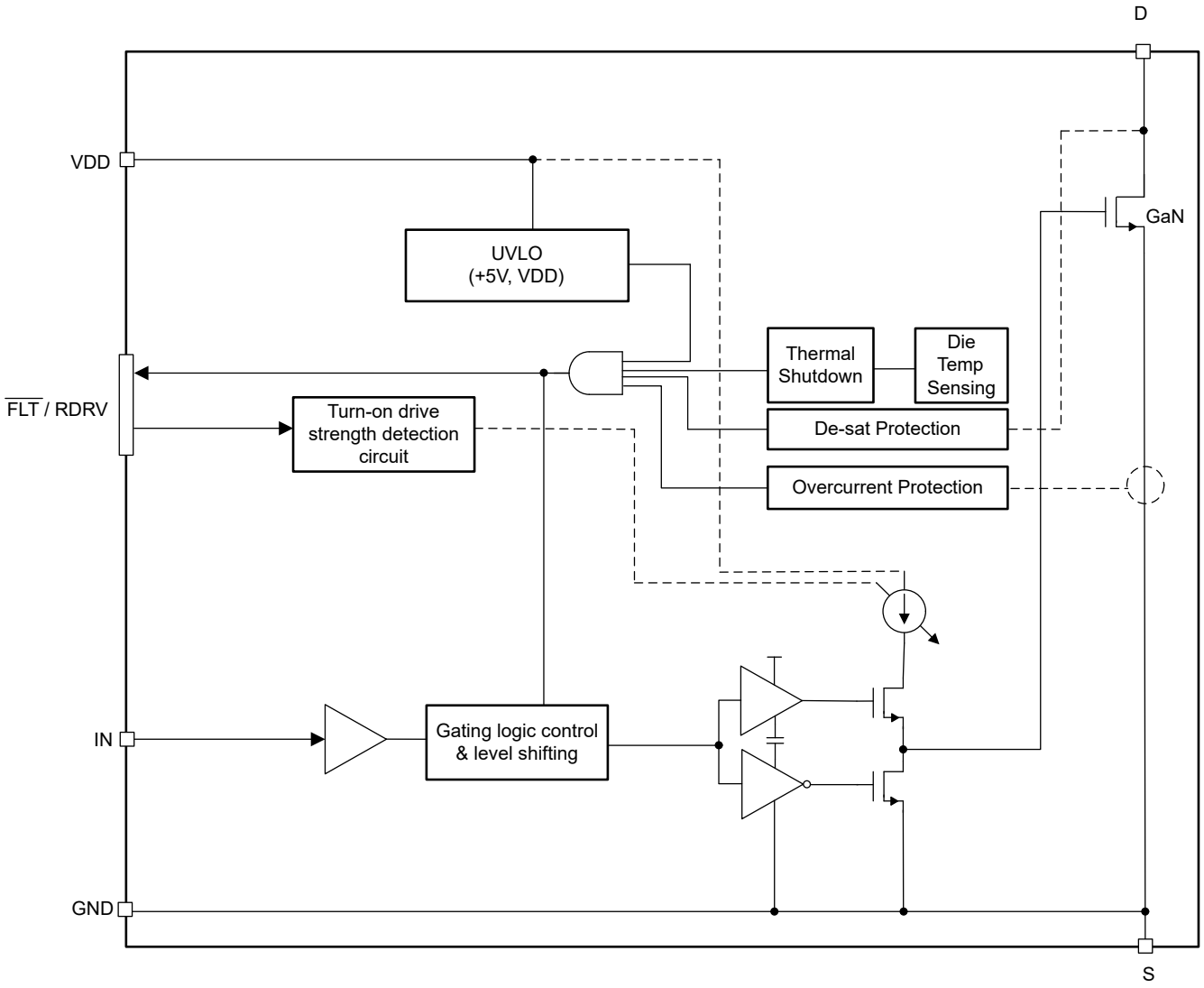
The LMG366xR025 is a high-performance power GaN device with an integrated gate driver. The GaN device offers zero reverse recovery and ultra-low output capacitance to enables high efficiency in bridge-based topologies.

The integrated driver establishes that the device remains off for high drain slew rates. The integrated driver protects the GaN device from overcurrent, short-circuit, overtemperature, and VDD undervoltage. The LMG3666R025 has a zero-voltage detection (ZVD) feature that outputs a pulse signal on the ZVD pin when zero-voltage switching (ZVS) is detected. The LMG3667R025 includes the zero-current detection (ZCD) feature which sets the ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.

Unlike Si MOSFETs, GaN devices do not have a p-n junction from source to drain and thus have no reverse recovery charge. However, GaN devices still conduct from source to drain similar to a p-n junction body diode, but with higher voltage drop and higher conduction loss. Therefore, minimize source-to-drain conduction time while the LMG366xR025 GaN FET is turned off.

7.2 Functional Block Diagram

7.2.1 LMG3660R025 Functional Block Diagram



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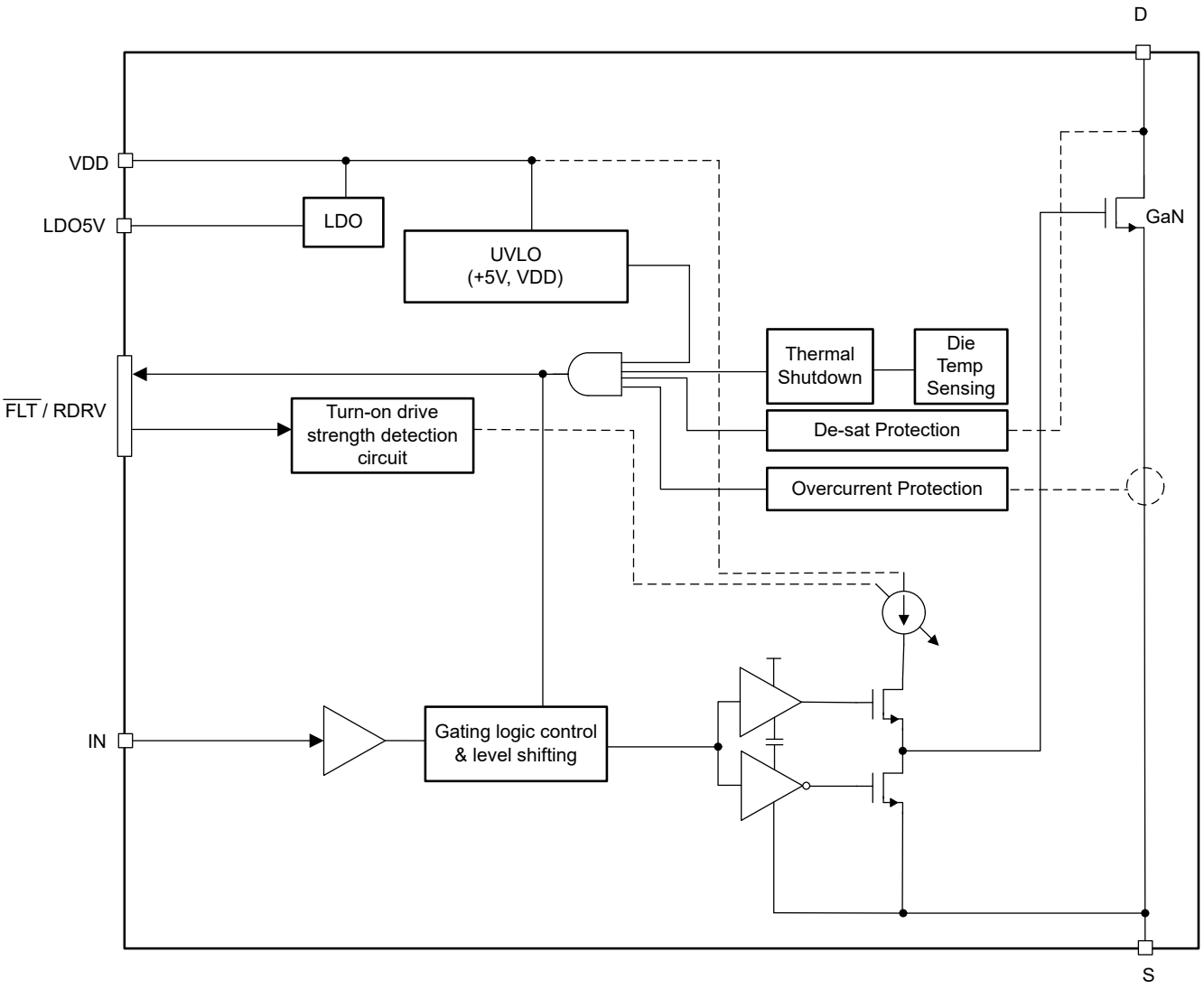
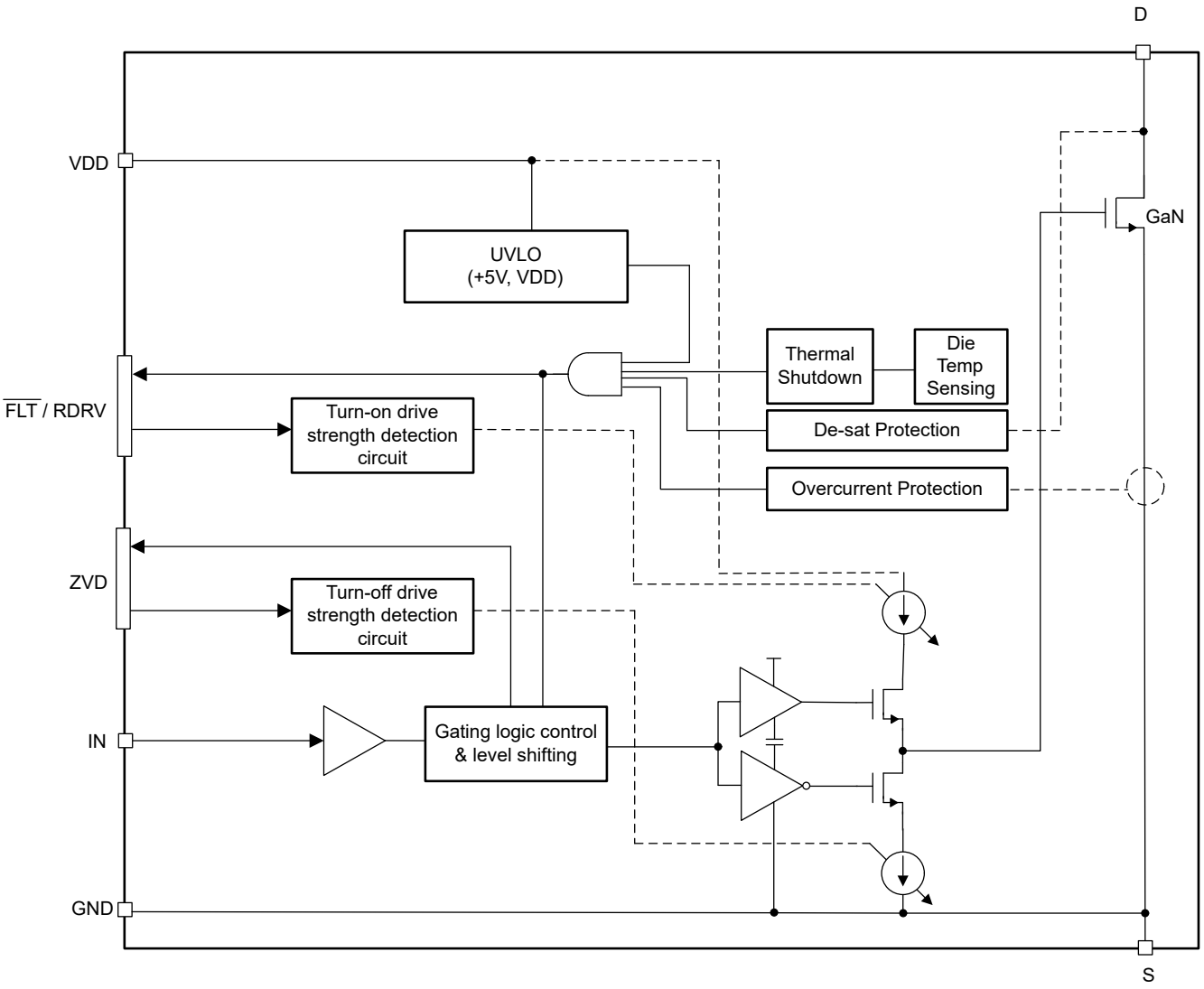
7.2.2 LMG3661R025 Functional Block Diagram



7.2.3 LMG3666R025 Functional Block Diagram



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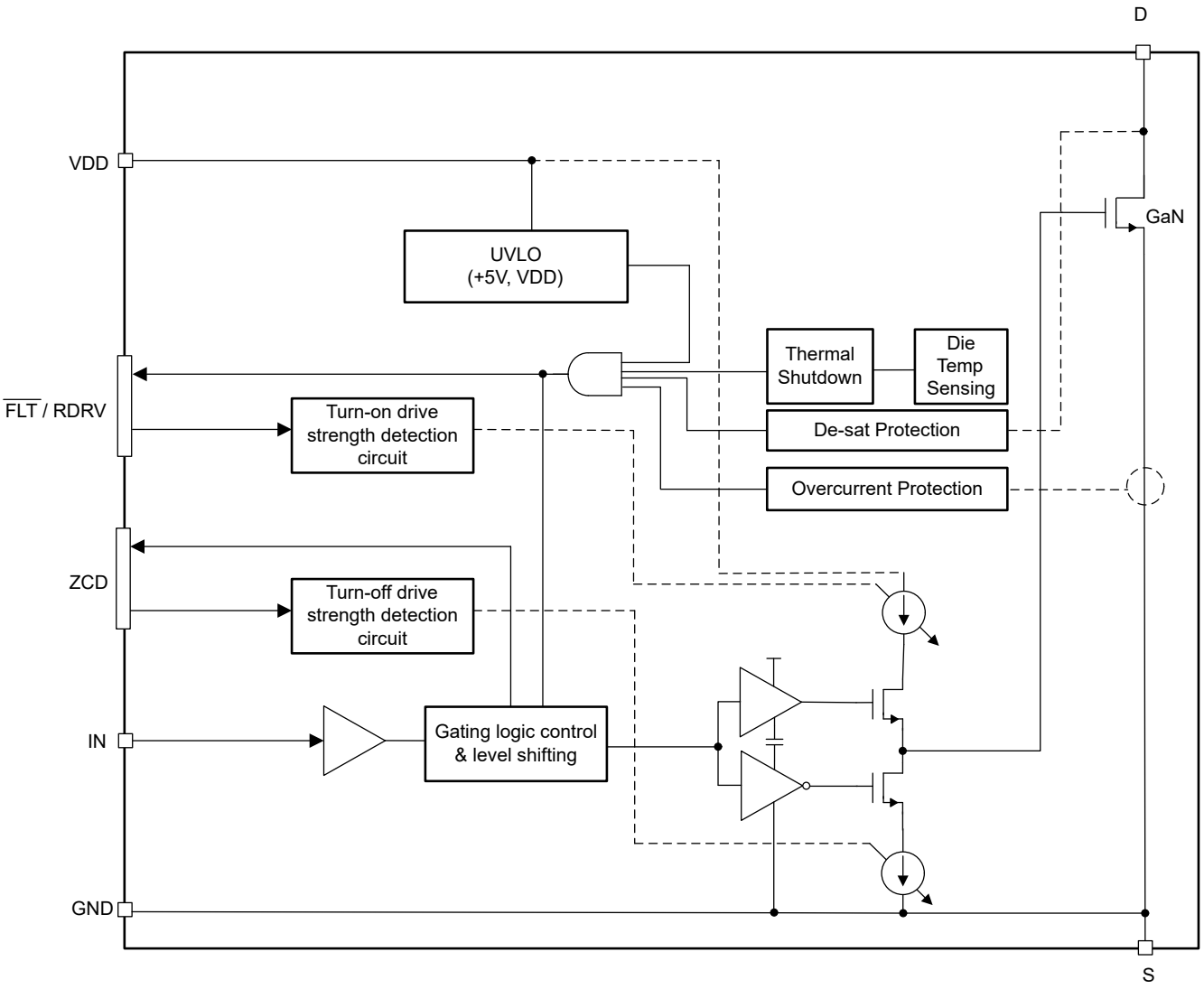
7.2.4 LMG3667R025 Functional Block Diagram



7.3 Feature Description

7.3.1 Drive Strength Adjustment

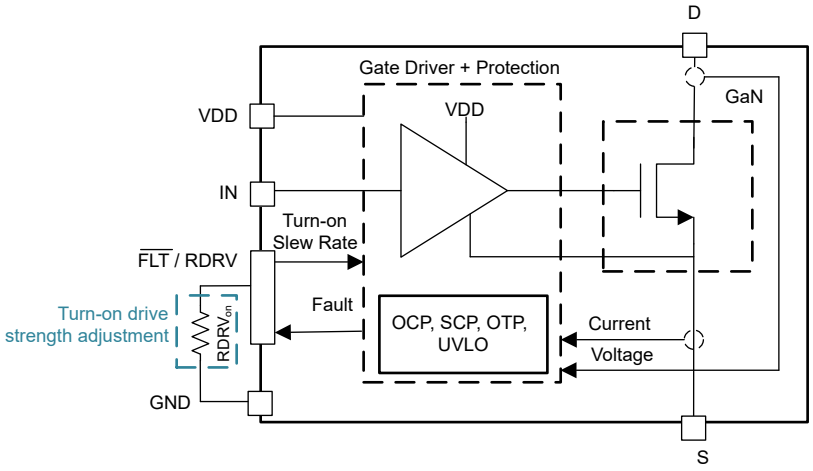


Figure 7-1. LMG3660R025 Drive Strength Adjustment Circuit

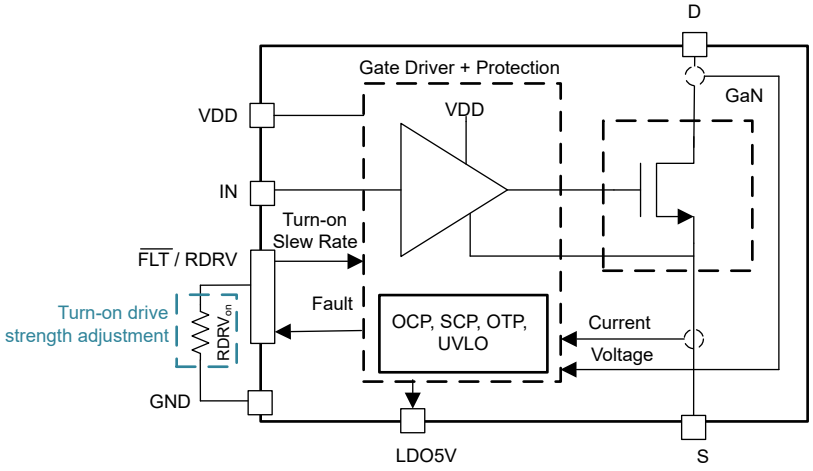


Figure 7-2. LMG3661R025 Drive Strength Adjustment Circuit

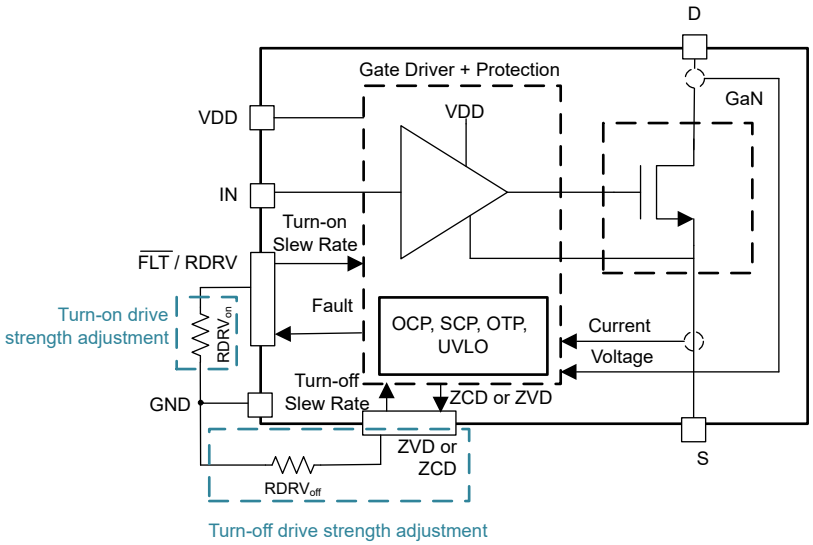


Figure 7-3. LMG3666R025 or LMG3667R025 Drive Strength Adjustment Circuit

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The LMG366xR025 allows users to adjust the drive strength of the device and obtain a desired slew rate, which provides flexibility when optimizing switching losses and minimizing EMI. The turn-on slew rate is programmed by the resistance between the $\overline{FLT}$/RDRV and GND pins. The turn-on slew rate setting is determined one time at power up, then the $\overline{FLT}$/RDRV pin is used as a push-pull 5V digital output for fault monitoring, as described in *Fault Reporting*.

Table 7-1 shows the recommended typical resistance programming values for each turn-on slew rate setting.

Table 7-1. Turn-On Slew Rate Settings

RECOMMENDED TYPICAL PROGRAMMING RESISTANCE $RDRV_{on}$(kΩ)	TYPICAL TURN-ON SLEW RATE (V/ns)
29.4	10
35.7	20
43.2	40
53.6	60
69.8	70
400 (1)	80

(1) Open-circuit connection for programming resistances is acceptable

The turn-off slew rate control is available only in LMG3666R025 and LMG3667R025, allwoing independent control of the maximum value of turn-off slew rate and typical turn-on slew rate.

For LMG3666R025, the turn-off slew rate setting is determined one time at power up, which can be programmed by the resistance between the ZVD and GND pins, then the ZVD pin is used as a push-pull 5V digital output for zero-voltage detection as described in *Zero-Voltage Detection (ZVD) (LMG3666R025 Only)*

For LMG3667R025, the turn-off slew rate setting is determined one time at power up, which can be programmed by the resistance between the ZCD and GND pins, then the ZCD pin is used as a push-pull 5V digital output for zero-current detection.

Table 7-2 shows the recommended typical resistance programming values for each turn-off slew rate setting.

Table 7-2. Turn-Off Slew Rate Settings

RECOMMENDED TYPICAL PROGRAMMING RESISTANCE $RDRV_{off}$(kΩ)	MAXIMUM TURN-OFF SLEW RATE (V/ns)
32.4	10
48.7	20
80.6	40
287 (1)	full speed (2)

(1) Open-circuit connection for programming resistances is acceptable
(2) Fully dependent on the magnitude of the drain-to-source current charging the output capacitance

For example, setting $RDRV_{on}$ = 53.6kΩ, $RDRV_{off}$ = 48.7kΩ results in turn-on slew rate of 60V/ns and turn-off slew rate is limited to a maximum of 20V/ns.

7.3.2 GaN Power FET Switching Capability

Due to the long reign of the silicon FET as the dominant power-switch technology, many designers are unaware that the nameplate drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The nameplate drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The nameplate drain-source voltage of a GaN FET is set by the long term compliance to data sheet specifications.

Exceeding the nameplate drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the nameplate drain-source voltage. For

example, the breakdown drain-source voltage of the LMG366xR025 GaN power FET is more than 800V which allows the LMG366xR025 to operate at conditions beyond an identically nameplate rated silicon FET.

The LMG366xR025 GaN power FET switching capability is explained with the assistance of Figure 7-4. The figure shows the drain-source voltage versus time for the LMG366xR025 GaN power FET for a single switch cycle in a switching application. No claim is made about the switching frequency or duty cycle.

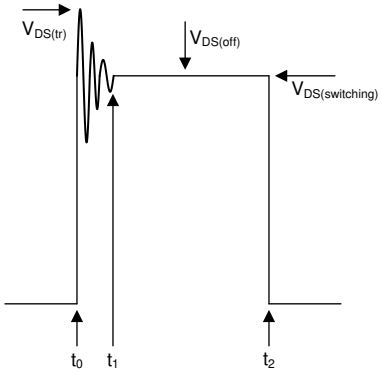

Figure 7-4. GaN Power FET Switching Capability

The waveform starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing damps out by t_1. Between t_1 and t_2 the FET drain-source voltage is set by the characteristic response of the switching application. The characteristic is shown as a flat line (plateau), but other responses are possible. At t_2 the GaN FET is turned on. For normal operation, the transient ring voltage is limited to 650V and the plateau voltage is limited to 520V. For rare surge events, the transient ring voltage limit is 800V and the plateau voltage limit is 720V.

7.3.3 VDD Supply

VDD is the input supply for the internal circuits. Wide voltage ranges from 9V to 24V are supported on VDD pin.

7.3.4 Overcurrent and Short-Circuit Protection

The driver detects two types of current faults: overcurrent and short-circuit.

The overcurrent protection (OCP) circuit monitors drain current and compares that current signal with an internally set limit $I_{T(OC)}$. Upon detection of the overcurrent, the LMG366xR025 performs cycle-by-cycle protection as shown in Cycle-by-Cycle Overcurrent Protection Operation. In this mode, the GaN device is shut off when the drain current crosses the $I_{T(OC)}$ plus a delay $t_{off(OC)}$, but the overcurrent signal clears after the IN pin signal goes low.

In the next cycle, the GaN device turns on as normal. Use the cycle-by-cycle function in cases where steady-state operation current is below the OCP level but transient response still reach current limit, while the circuit operation cannot pause. The cycle-by-cycle function also prevents the GaN device from overheating by overcurrent induced conduction losses. Additionally, the OCP level dynamically adjusts with junction temperature, with the internally set limit $I_{T(OC)}$ being higher at lower temperatures and decreasing as temperature increases, as defined in the Specifications, based on Equation 1. Dynamic adjustment allows customer to operate the device at lower temperatures with higher currents.

$$\frac{I_{T(OC)150°C}}{I_{T(OC)25°C}} = 77\% \quad (1)$$

The short-circuit protection is based on detection of saturation (de-sat), which monitors the drain-source voltage V_{DS} and compares the voltage with an internally set limit $V_{T(Idsat)}$. Saturation can damage the GaN, causing failures if continued to operate in that condition. If saturation is detected, the GaN device is latched off. Turning off the device at high current causes significant voltage overshoot. Therefore, when turning off from saturation, the device is turned off with an intentionally slowed driver to achieve a lower overshoot voltage and ringing

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during the turn-off event. This fast response circuit helps protect the GaN device even under a hard short-circuit condition. In this protection, the GaN device is shut off and held off until the fault is reset by either holding the IN pin low for a period of time defined in the Specifications or removing power from VDD.

For safety considerations, OCP allows cycle-by-cycle operation while de-sat latches the device until reset. Both faults are reported on the $\overline{FLT}$/RDRV pin.

Figure Figure 7-6 shows the behavior of the OC and de-sat protection. In the first two cycles OC limit is triggered without de-sat being triggered, so cycle-by-cycle protection takes place. In the third cycle OC limit is triggered, but within the $t_{off(OC)}$ the de-sat protection is triggers when V_{DS} rises above $V_{T(Idsat)}$. Since de-sat protection triggers, this results in a slowed turn-off and latched protection.

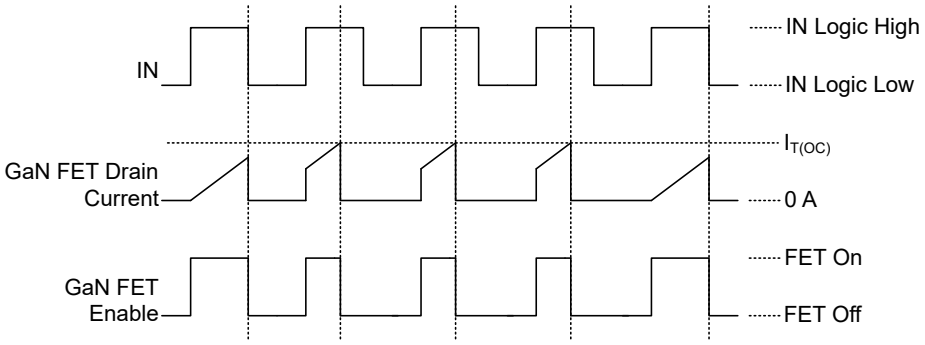

Figure 7-5. Cycle-by-Cycle Overcurrent Protection Operation

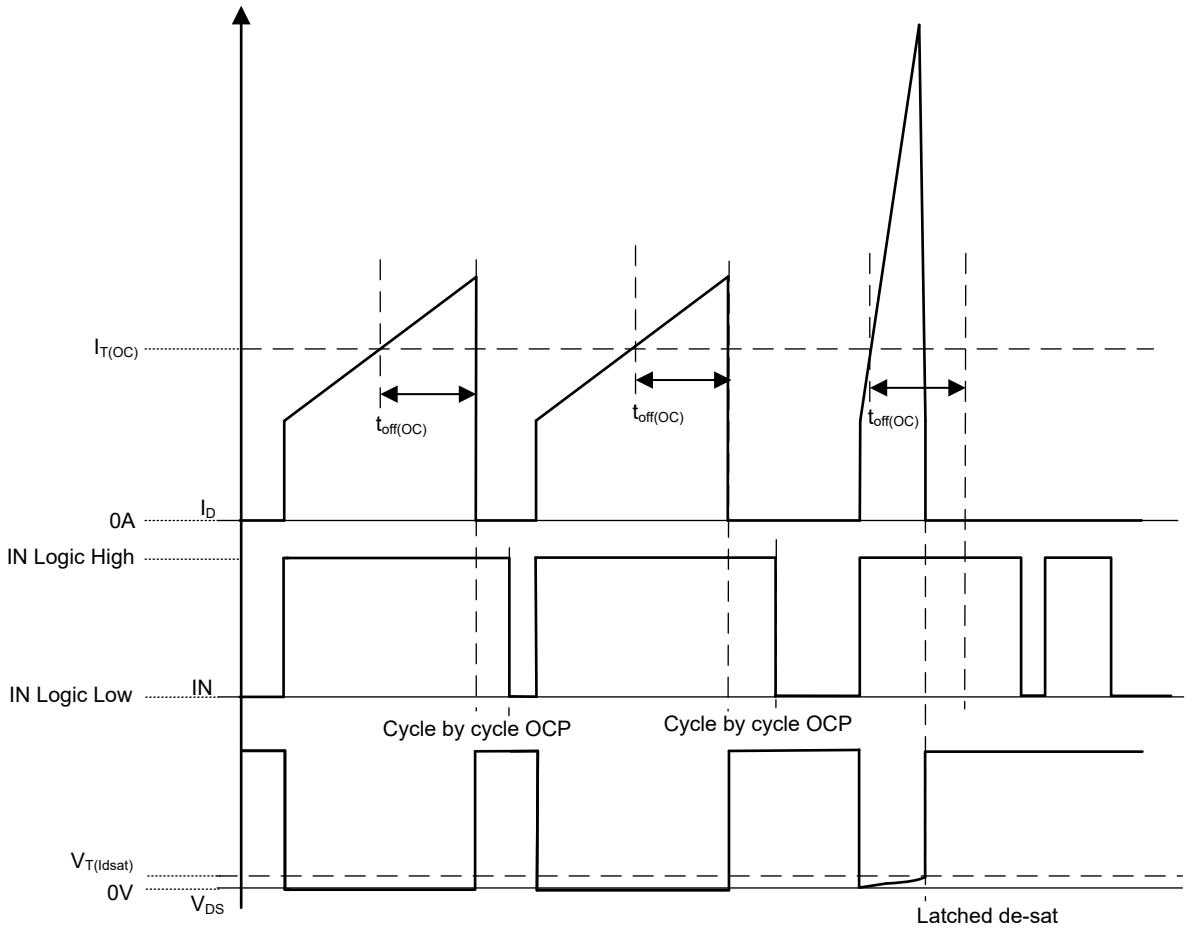

Figure 7-6. Overcurrent Detection vs Desaturation Detection

7.3.5 Overtemperature Protection

The overtemperature protection monitors the GaN FET temperature and holds off the GaN device when the temperature rises above the overtemperature protection threshold. The overtemperature protection hysteresis avoids erratic thermal cycling. An overtemperature fault is reported on the $\overline{FLT}$/RDRV pin when the overtemperature protection is asserted. $\overline{FLT}$/RDRV de-asserts and the device automatically returns to normal operation after the device temperature fall below the negative-going trip point.

7.3.6 UVLO Protection

The LMG366xR025 supports a wide range of V_{DD} voltages. However, when the V_{DD} voltage is below V_{DD} UVLO threshold, the GaN device stops switching and is held off. The V_{DD} UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point. The $\overline{FLT}$/RDRV pin is pulled low as an indication of UVLO.

7.3.7 Fault Reporting

All faults are reported on the $\overline{FLT}$/RDRV pin, which serves as both an input and output pin.

The $\overline{FLT}$/RDRV is configured as an input only at the time of power-up to adjust the drive-strength, as described in Drive Strength Adjustment.

The $\overline{FLT}$/RDRV is used as an active low digital output, indicating the fault status thereafter. The pin is a push-pull 5V digital output which goes high when all faults have cleared, which means that there is additional quiescent current through R1 when the pin is forced high.

Depending on the input threshold levels for the external digital receiver connected to the fault pin, the 1.2V step function which is forced on this pin at power-up can be interpreted as either high or low. For this reason, TI recommends that the receiver has higher thresholds such as those common for CMOS-compatible inputs and not use TTL compatible inputs. If the minimum input threshold of the external digital receiver connected to the fault pin is at or below 1.2V, the 1.2V step function at power-up can be interpreted as a *high*, before the LMG366xR025 is ready to begin switching.

7.3.8 Auxiliary LDO (LMG3661R025 Only)

A 5V voltage regulator inside LMG366xR025 is used to supply external loads, such as digital isolators for the high-side drive signal. The digital outputs of LMG366xR025 use this 5V rail as a voltage supply. A capacitor is not required for stability, but transient response is poor if no external capacitor is provided. If the application uses the LDO5V pin to supply external circuits, TI recommends using a capacitor of at least 0.1µF for improved transient response. Use a larger capacitor for further transient response improvement. Verify that the decoupling capacitor is a low-ESR ceramic type. Capacitances above 0.47µF slow down the start-up time of the LMG366xR025, due to the ramp-up time of the 5V rail.

7.3.9 Zero-Voltage Detection (ZVD) (LMG3666R025 Only)

The ZVD pin serves as both an input and output pin. The ZVD pin is configured as an input only at the time of powerup to adjust the turn-off drive-strength, as described in *Drive Strength Adjustment*. The ZVD pin then used as digital output, indicating the zero-voltage detection status thereafter as described below.

The zero-voltage switching (ZVS) converters are widely used to improve the power converter's efficiency. However, in those soft-switching topologies like LLC and triangular current mode (TCM) totem pole PFC, the device can lose ZVS depending on the load condition, inductor, magnetic parameters and control techniques, which affects the system efficiency. To insure ZVS, certain design margins or additional circuits are needed which sacrifices the converter performance and adds components.

To simplify the system design for soft-switching converters, the LMG3666R025 part integrates a zero-voltage detection (ZVD) circuit that provides a digital feedback signal to indicate if the device has achieved ZVS in the current switching cycle. The circuit diagram is shown in Circuit Diagram for Zero-Voltage Detection Circuit Block Diagram. When the IN pin signal goes high, the logic circuit checks if the device V_{DS} has reached below -1V to determine whether the device achieves zero voltage switching in the switching cycle. Once a ZVS is identified, a pulse-output with a width of T_{WD_ZVD} is sent out from the ZVD pin, after a delay time of T_{DL_ZVD} as indicated

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in ZVD Timing Specifications. Note that a certain third quadrant conduction time is required to allow the device detecting a zero-voltage switching, and T_{3rd_ZVD} is a function of the gate driver strength.

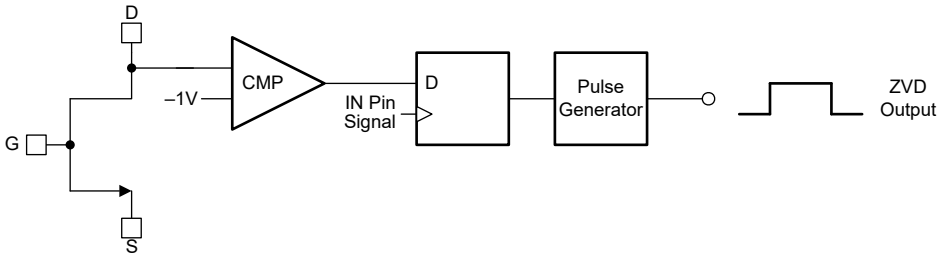

Figure 7-7. Circuit Diagram for Zero-Voltage Detection Circuit Block Diagram

ZVD Function in a CCM Buck Converter shows the waveforms of the ZVD pin corresponding to a continuous conduction mode buck converter. These waveforms demonstrate how ZVD function works in both hard-switching and soft-switching conditions. For I_L in the waveforms in ZVD Function in a CCM Buck Converter load current going out of the switch node is positive. In CCM buck operation, the high-side device is the hard-switching device while the low-side device can achieve zero-voltage switching with a proper dead-time settings. In the first switching cycle when low-side device IN pin rises, the switch-node voltage V_{DS} drops below zero and stays in third quadrant conduction for a period of T_1. Since this third quadrant conduction time T_1 is larger than the detection time T_{3rd_ZVD} specified in Section 5.5, a zero-voltage transition is identified and the ZVD pin outputs a pulse signal. The pulse width of the ZVD pulse is also defined in the electrical characteristic table as T_{WD}. In the second switching cycle, the device is turned on earlier, and the third quadrant conduction time T_2 is less than T_{3rd_ZVD}. Since T_2 is less than T_{3rd_ZVD}, the ZVD signal stays low, even though the device achieves ZVS. In the third switching cycle, the IN pin signal is advanced even earlier, and the device is in partial hard-switching. Accordingly, the ZVD output stays low when a ZVS transition is not achieved. Note the high side ZVD output stays low in this CCM buck operation as the high side device is always hard-switching turn-on.

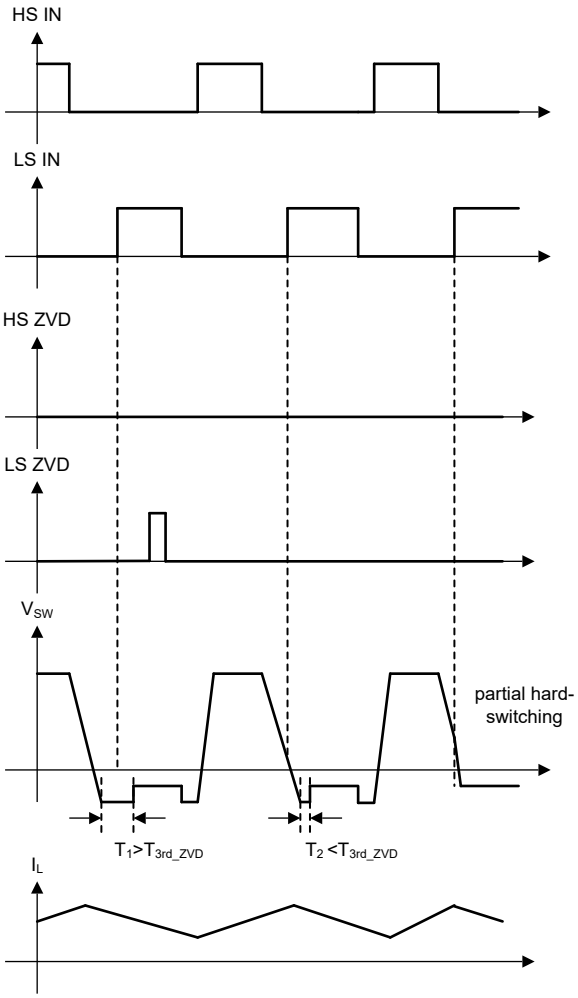

Figure 7-8. ZVD Function in a CCM Buck Converter

The ZVD function facilitates the control in soft-switching topology. ZVD Function in a TCM TP PFC Converter illustrate the facilitation with the ZVD waveforms in a TCM totem pole PFC. This diagram shows the positive half line-cycle with V_{IN} greater than half of V_{OUT}. For I_L in the waveforms in ZVD Function in a TCM TP PFC Converter load current going into the switch node is defined as positive. In the first switching cycle, the load current builds enough negative current, and the low-side device achieves ZVS with a clear third quadrant conduction time beyond T_{3rd_DET}. Therefore, the ZVD pin outputs a pulse signal. The ZVD pulses are missing in the next two switching cycles because the third quadrant conduction time shortens in second cycle and the device loses ZVS in the third cycle.

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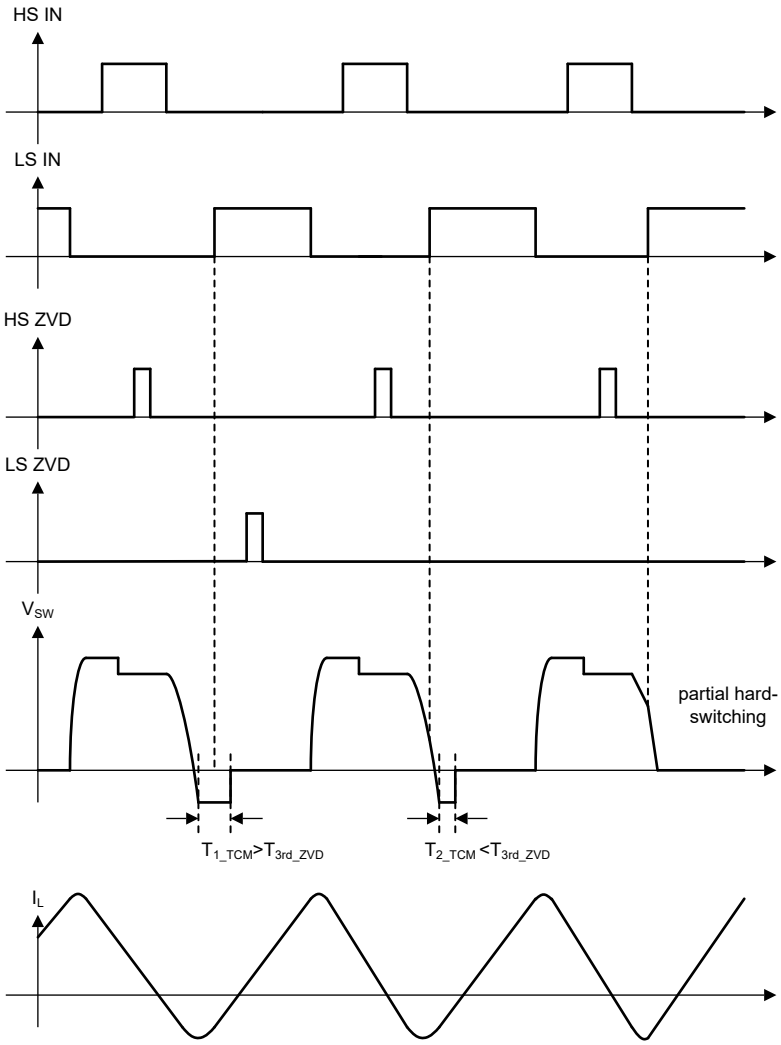

Figure 7-9. ZVD Function in a TCM TP PFC Converter

7.4 Device Functional Modes

The device has one applicable mode of operation when operating within the Recommended Operating Conditions.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMG366xR025 is a power IC targeting hard-switching and soft-switching applications operating up to 520V bus voltages. GaN devices offer zero reverse-recovery charge enabling high-frequency, hard-switching in applications, such as the totem-pole PFC. The low Q_{OSS} of GaN devices also benefits soft-switching converters, such as the LLC and phase-shifted full-bridge configurations. As half-bridge configurations are the foundation of the two mentioned applications and many others, this section describes how to use the LMG366xR025 in a half-bridge configuration.

8.2 Typical Application

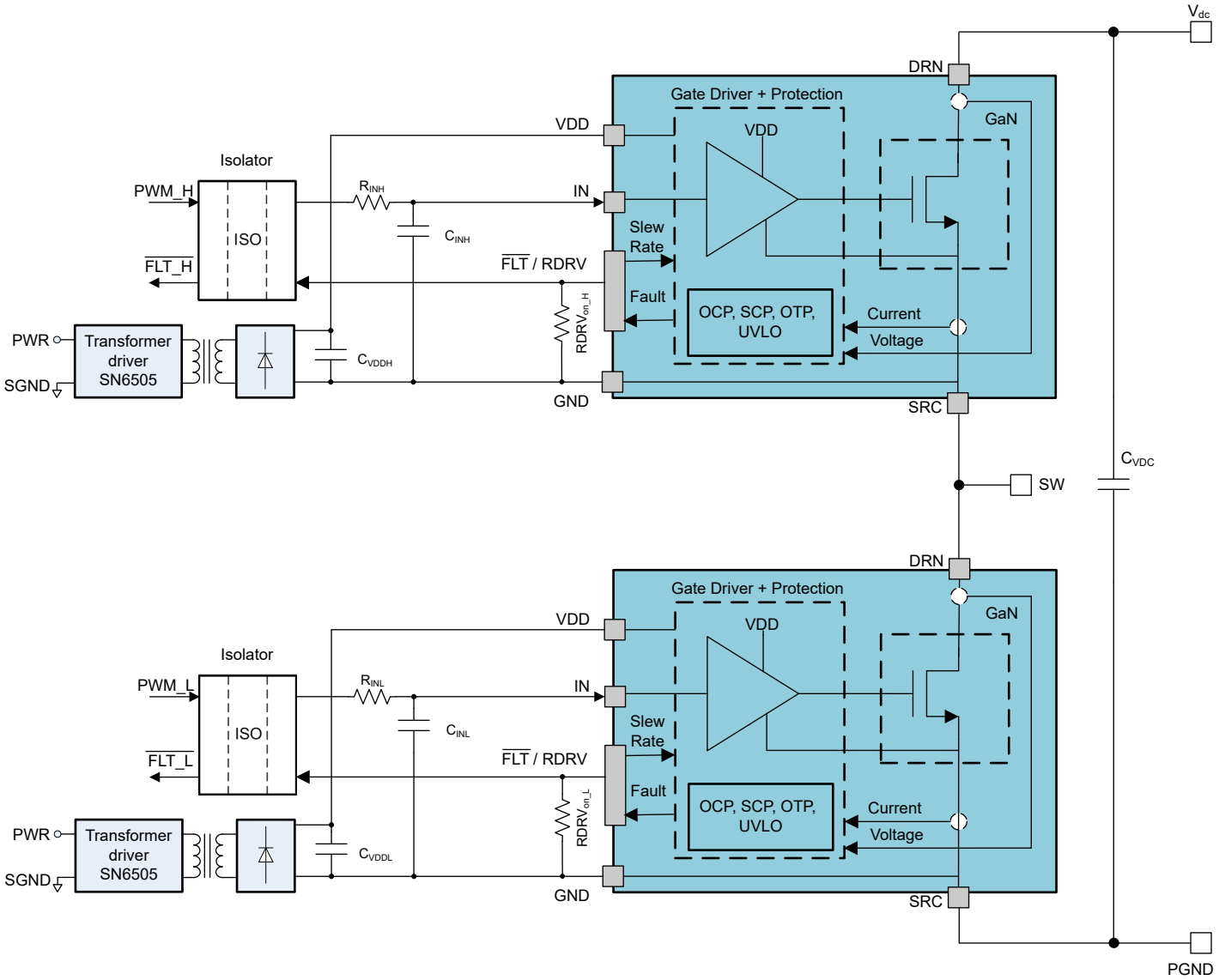

Figure 8-1. LMG3660R025 Typical Half-Bridge Application With Isolated Power Supply

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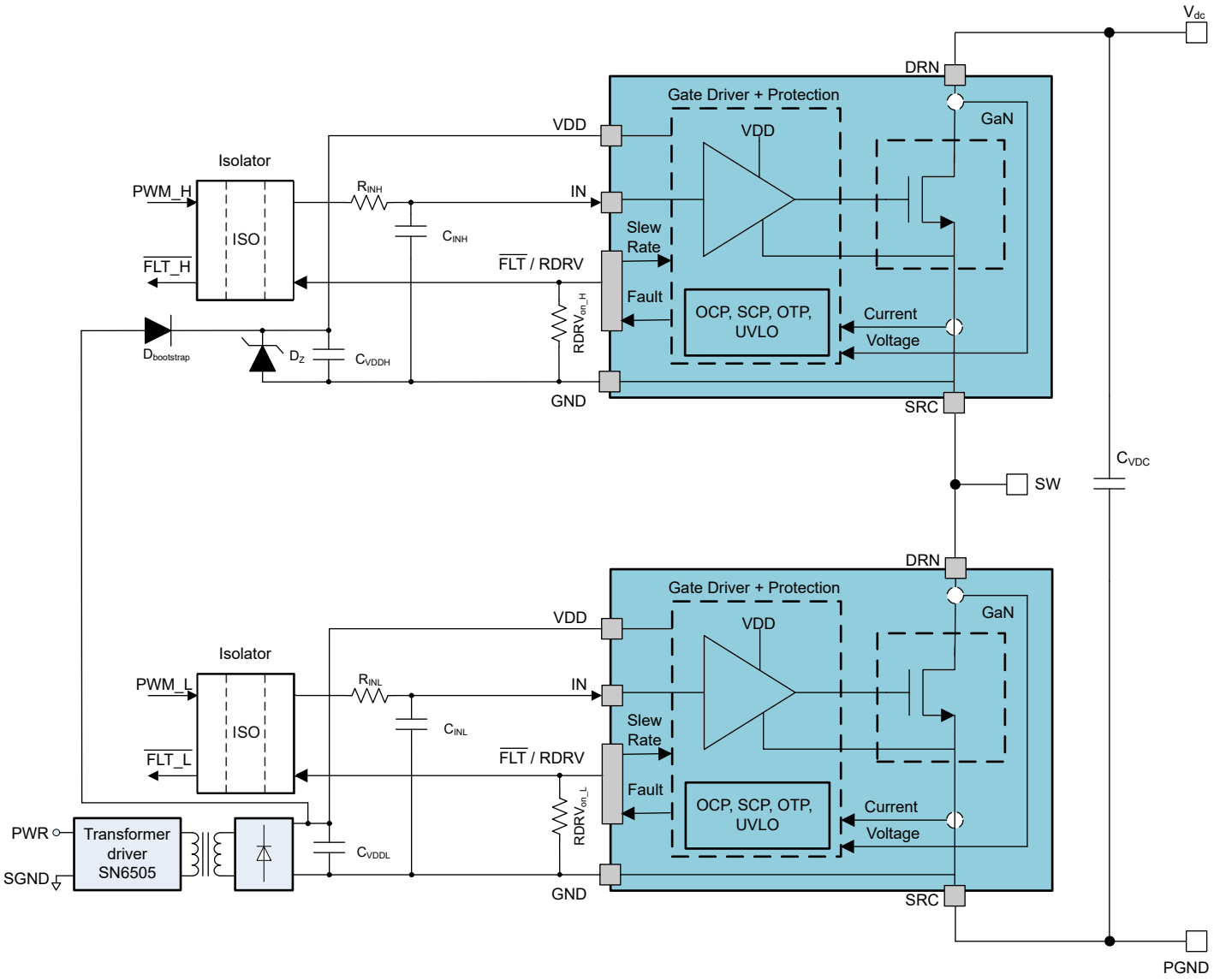

Figure 8-2. LMG3660R025 Typical Half-Bridge Application With Bootstrap

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8.2.1 Design Requirements

This design example is for a hard-switched boost converter which is representative of PFC applications. Design Parameters shows the system parameters for this design.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage	200VDC
Output voltage	400VDC
Input (inductor) current	20A
Switching frequency	100kHz

8.2.2 Detailed Design Procedure

In high-voltage power converters, circuit design and PCB layout are essential for high-performance power converters. This data sheet describes design considerations for half-bridges using the LMG366xR025.

8.2.2.1 Slew Rate Selection

Adjust the turn-on slew rate of LMG366xR025 from approximately 10V/ns to 80V/ns, and adjust the maximum turn-off slew rate limit from 10V/ns to unlimited (controlled only by I_{ds}). Refer to Section 7.3.1 for the details.

The slew rate affects GaN device performance in terms of:

- Switching loss
- Voltage overshoot
- Noise coupling
- EMI emission

Generally, high slew rates provide low switching loss, but high slew rates can also create higher voltage overshoot, noise coupling, and EMI emissions. Follow the design recommendations in this data sheet to mitigate the challenges caused by a high slew rate. The LMG366xR025 offers circuit designers the flexibility to select the proper slew rate for the best performance of applications.

8.2.2.2 Signal Level-Shifting

In half-bridges, use high-voltage level shifters or digital isolators to provide isolation for signal paths between the high-side device and control circuit. Using an isolator is optional for the low-side device. However, using and isolator equalizes the propagation delays between the high-side and low-side signal paths, and provides the ability to use different grounds for the GaN device and the controller. If an isolator is not used on the low-side device, connect the control ground and power ground at the device and nowhere else on the board. With fast-switching devices, common ground inductance can easily cause noise issues without the use of an isolator.

Selecting a digital isolator for level-shifting is important for the improvement of noise immunity. As GaN device can easily create high dv/dt, > 50V/ns, in hard-switching applications, TI highly recommends using isolators with high common-mode transient immunity (CMTI) and low barrier capacitance. Isolators with low CMTI can easily generate false signals, which can cause shoot-through. The barrier capacitance is part of the isolation capacitance between the signal ground and power ground, which is directionally proportional to the common mode current and EMI emission generated during the switching. Additionally, TI strongly encourages selecting non-edge-triggered isolators. In an edge-triggered isolator, a high dv/dt event can cause the isolator to flip states and cause circuit malfunction.

Generally, the preference is ON/OFF keyed isolators with a low default output. Default low state establishes that the system does not shoot-through when starting up or recovering from fault events. A high CMTI event causes a very short (a few nanoseconds) false pulse, TI recommends placing a low pass filter (such as 50Ω and 150pF R-C) at the driver input to filter out the false pulses.

8.3 Power Supply Recommendations

The LMG366xR025 only requires an unregulated VDD power supply from 9V to 24V. Obtain the low-side supply from the local controller supply. Verify that the supply of the high-side device comes from an isolated or bootstrap supply.

8.3.1 Using an Isolated Power Supply

The advantage of using an isolated power supply to power the high-side device is that it works regardless of continued power-stage switching or duty cycle. Using an isolated power supply can also power the high-side device before power-stage switching begins for a smooth start-up

Obtain the isolated supply with a push-pull converter, a flyback converter, a FlyBuck™ converter, or an isolated power module. When using an unregulated supply, verify that the input of LMG366xR025 do not exceed the maximum supply voltage. Use a 24V TVS diode to clamp the VDD voltage of LMG366xR025 for additional protection. Minimizing the inter-winding capacitance of the isolated power supply or transformer is necessary to reduce switching loss in hard-switched applications. Furthermore, capacitance across the isolated bias supply inject high currents into the signal-ground of the LMG366xR025 and can cause problematic ground-bounce transients. A common-mode choke can alleviate most of these issues.

8.3.2 Using a Bootstrap Diode

In half-bridge configuration, a floating supply is necessary for the high-side device. To obtain the best performance of LMG366xR025, TI recommends Using an isolated power supply. Use a bootstrap supply can be used with the recommendations of Using a Bootstrap Diode.

8.3.2.1 Diode Selection

The LMG366xR025 offers no reverse-recovery charge and very limited output charge. Hard-switching circuits using the LMG366xR025 also exhibit high voltage slew rates. A compatible bootstrap diode must not introduce high output charge and reverse-recovery charge.

A silicon carbide diode, like the GB01SLT06-214, can be used to avoid reverse-recovery effects. The SiC diode has an output charge of 3nC. Although there is additional loss from its output charge, it does not dominate the losses of the switching stage.

8.3.2.2 Managing the Bootstrap Voltage

In a synchronous buck or other converter where the low-side switch occasionally operates in third-quadrant, the bootstrap supply charges through a path that includes the third-quadrant voltage drop of the low-side LMG366xR025 during the dead time as shown in Charging Path for Bootstrap Diode. This third-quadrant drop can be large, which can overcharge the bootstrap supply in certain conditions. Verify that the V_{DD} supply of LMG366xR025 remains below 26V.

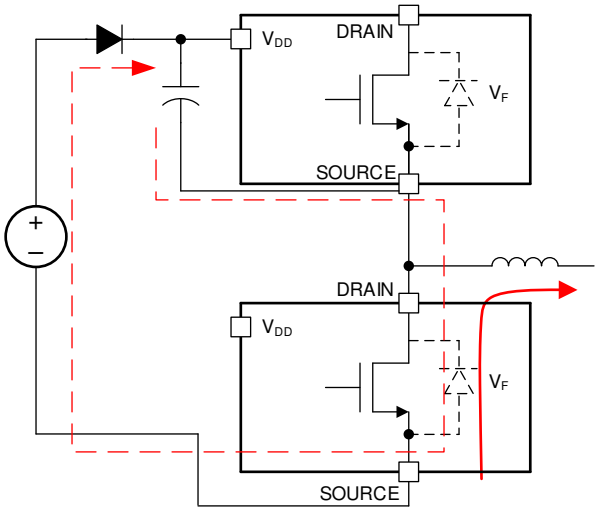

Figure 8-3. Charging Path for Bootstrap Diode

As Suggested Bootstrap Regulation Circuit shows, the recommended bootstrap supply includes a bootstrap diode, series resistor, and 24V TVS or Zener diode in parallel with the V_{DD} bypass capacitor. The parallel location prevents damage to the high-side LMG366xR025. The series resistor limits the charging current at start-up and when the low-side device operates in third-quadrant mode. Select the resistor to allow sufficient current to power the LMG366xR025 at the desired operating frequency. At 100kHz operation, TI recommends a value of approximately 2Ω. At higher frequencies, reduce or omit the resistor value to establish sufficient supply current.

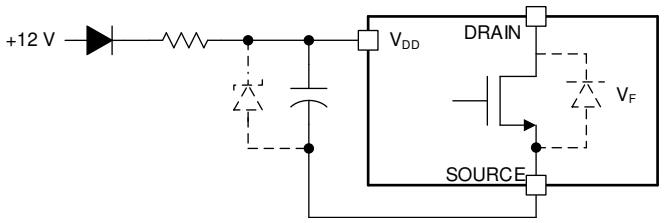

Figure 8-4. Suggested Bootstrap Regulation Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

FlyBuck™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

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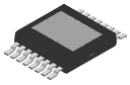
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

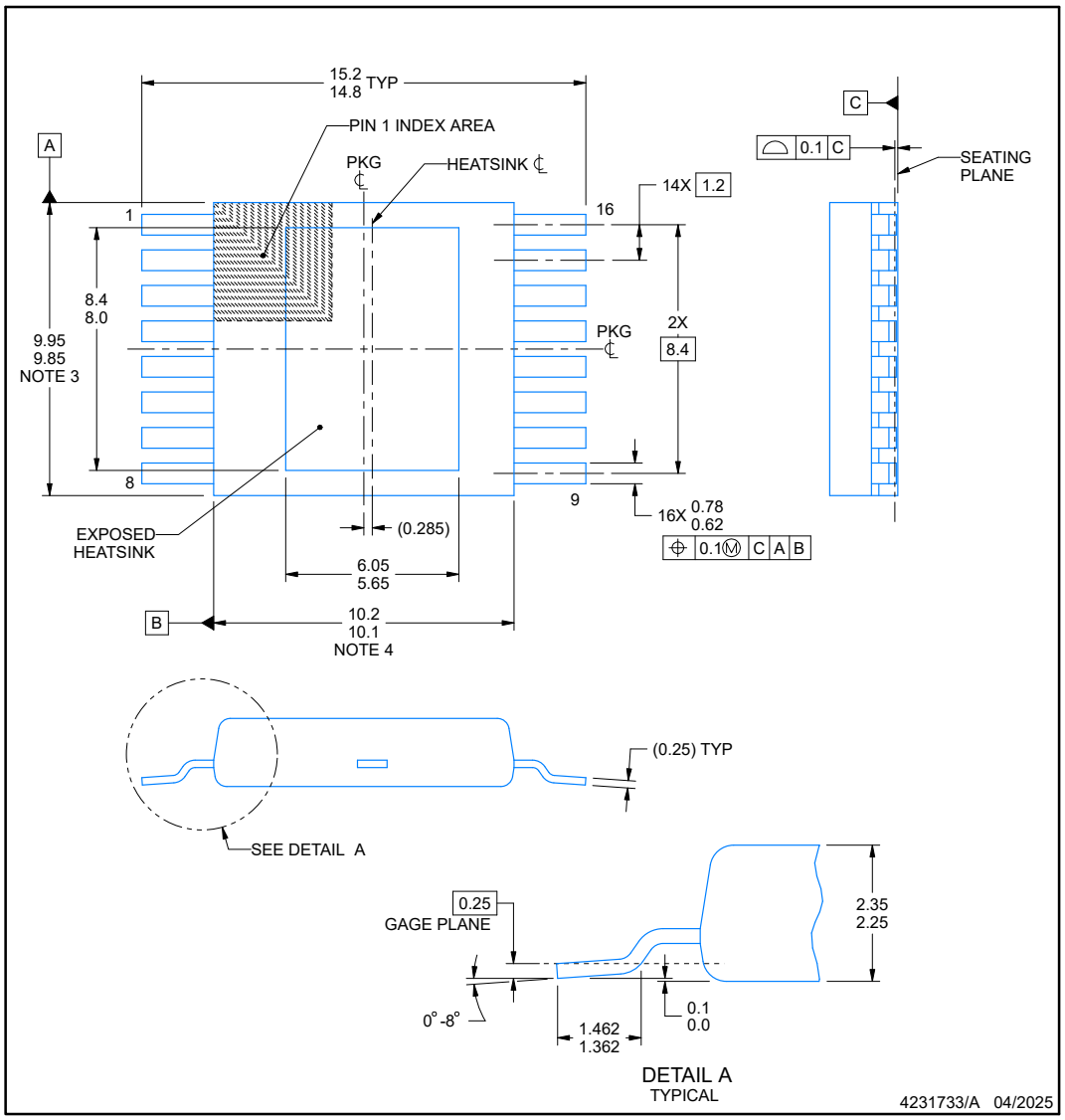


PACKAGE OUTLINE

KLG0016A

TO - 2.35 mm max height

TRANSISTOR OUTLINE



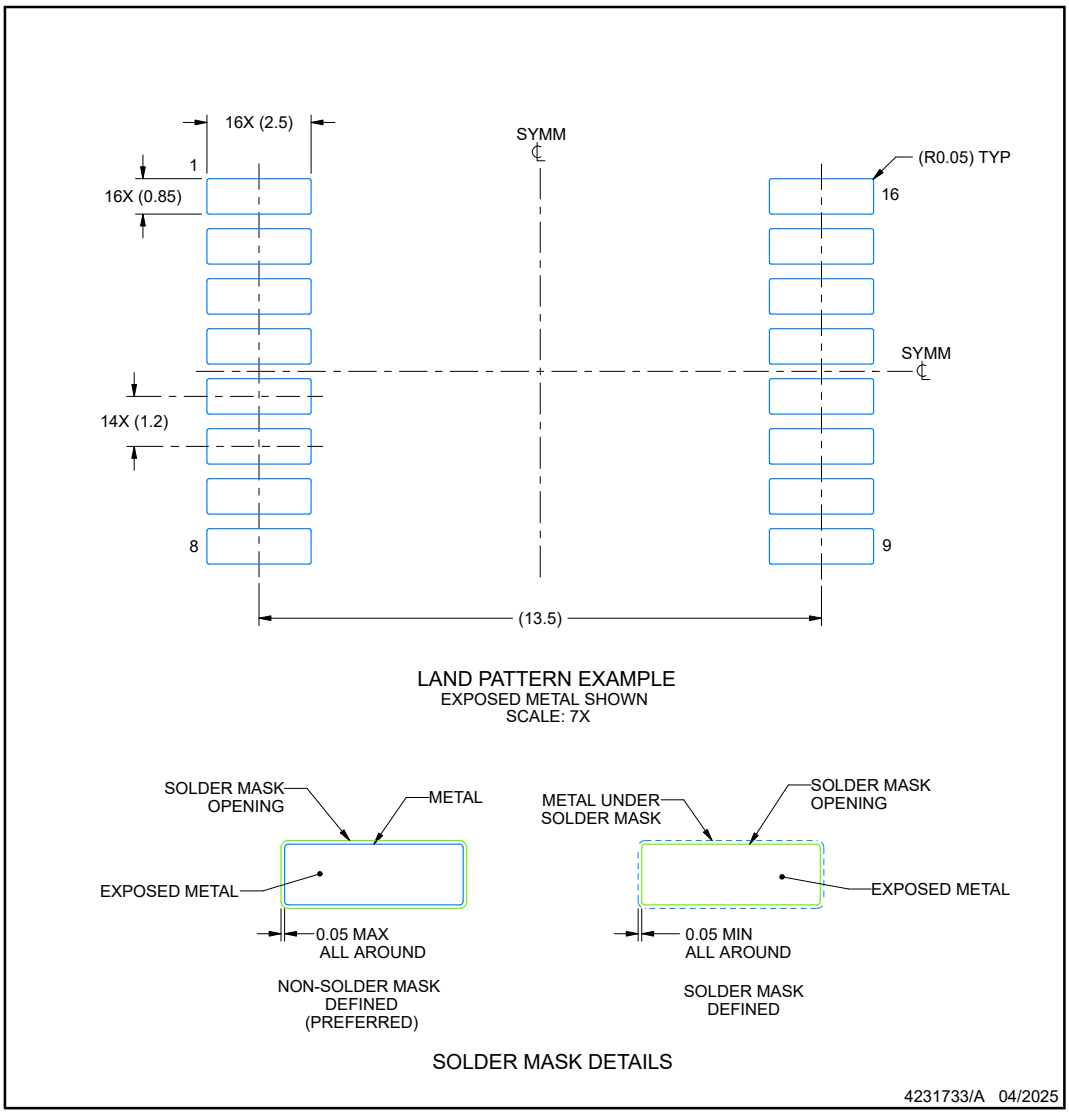
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

KLG0016A — **TO - 2.35 mm max height**

TRANSISTOR OUTLINE



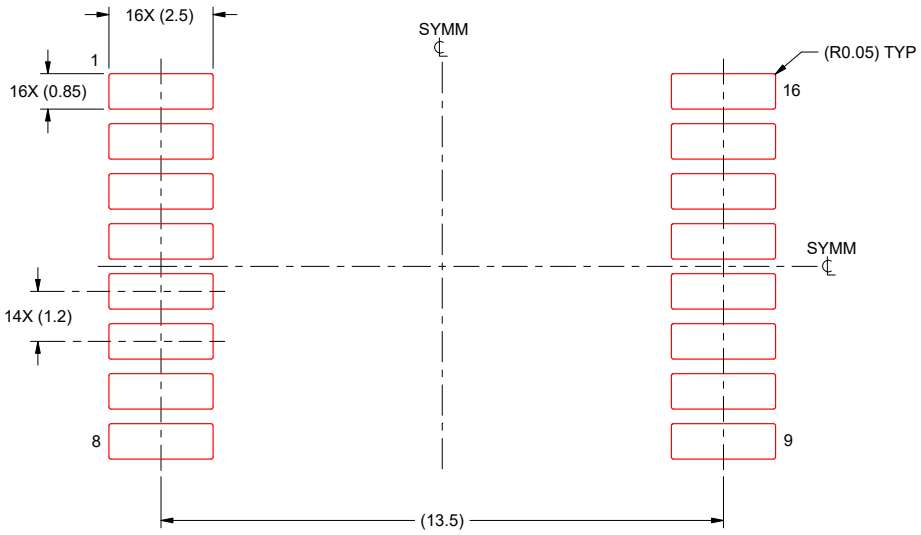
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

KLG0016A **TO - 2.35 mm max height**

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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