LMH0324 3G/HD/SD SDI Dual Output Adaptive Cable Equalizer

1 Features

- Supports ST 424(3G), ST 292(HD), and ST 259(SD)
- Compatible with DVB-ASI and AES10 (MADI)
- Adaptive Cable Equalizer
- Cable Reach (Belden 1694A):
  - 200 m at 2.97 Gbps
  - 280 m at 1.485 Gbps
  - 600 m at 270 Mbps
- Low Power: 78 mW (typical)
- Power Save Mode: 15 mW
- On-chip Input Termination (75 Ω single-ended)
- Integrated Input Return Loss Network
- Dual 100-Ω Output Drivers With De-Emphasis
- Independent Output Power-Down Control
- Supports Signal Splitter Mode (–6 dB Launch Amplitude)
- Cable Length Indicator
- Digital $MUTE_{REF}$ Threshold
- Powers from 2.5-V or 1.8-V Supply
- Configurable by Control Pins, SPI, or SMBus Interface
- 4-mm × 4-mm 24-pin QFN Package
- Operating Temperature Range: –40°C to +85°C

2 Applications

- SMPTE Compatible Serial Digital Interface (SDI)
- Broadcast Video Routers, Switchers, and Monitors
- DVB-ASI and Distribution Amplifiers
- Digital Video Processing and Editing

3 Description

The LMH0324 is a low-power, dual-output, extended reach adaptive cable equalizer. It is designed to equalize SDI data transmitted over 75-Ω coax cable. The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps. The equalizer includes an active sensing circuitry that ensures robust performance and enhanced immunity to variations in the input signal launch amplitude.

The LMH0324 provides extended cable reach with low power consumption. It offers power management to reduce power consumption further when no input signal is present.

The LMH0324 has two differential serial data outputs, which provide flexibility for fan-out buffering. The output drivers offer programmable de-emphasis to compensate for board trace losses at the LMH0324 outputs. The operating state of the LMH0324 can be set via pin control. Additional settings of the device can be programmed via SPI or SMBus interface.

The LMH0324 is pin-compatible to the LMH1219 (12-Gbps adaptive cable equalizer with integrated reclocker). The pin compatibility allows ease of upgrade from a 3-Gbps equalizer to a 12-Gbps equalizer with integrated reclocker.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH0324	QFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

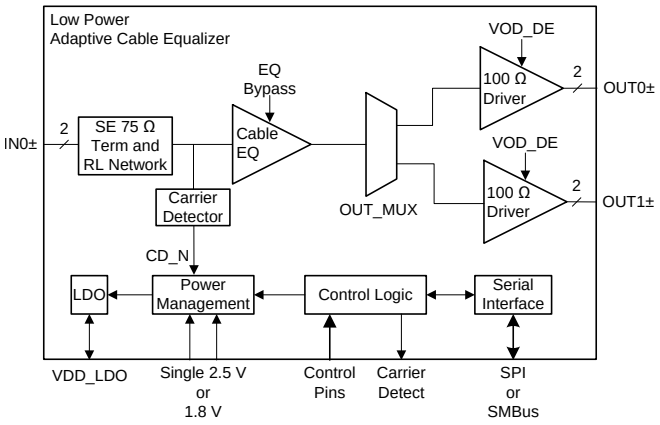


Table of Contents

4 Revision History

Changes from Revision A (May 2016) to Revision B **Page**

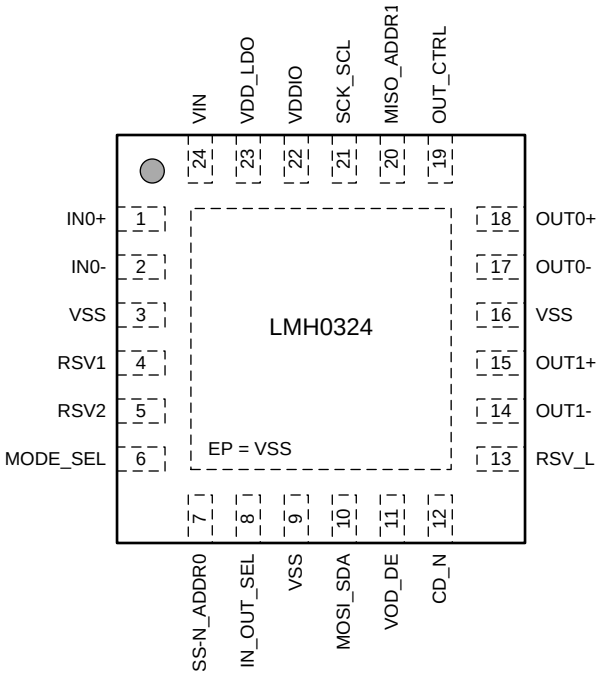
- Added top navigator link for reference design; first public release of data sheet ... 1

Changes from Original (April 2016) to Revision A **Page**

- Deleted min and max VOD_DE amplitude specification when VOD_DE = Level F ... 8
- Changed typical VOD_DE amplitude specifications for Levels F, R, and L ... 8
- Changed DEM value and DEM register settings in Table 4 to match correct VOD_DE pin logic levels ... 14
- Added new row for VOD = 5, DEM = 5 setting in Table 9 ... 28

5 Pin Configuration and Functions

RTW Package
24-Pin QFN
Top View



Pin Functions

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
High Speed Differential I/Os			
IN0+	1	I, Analog	Single-ended complementary inputs, 75-Ω internal termination from IN0+ or IN0- to internal common mode voltage and return loss compensation network. Requires external 4.7-µF AC coupling capacitors for SMPTE video applications.
IN0-	2	I Analog	
RSV1	4		Reserved pins. Do not connect.
RSV2	5		
OUT0+	18	O, Analog	Differential complementary outputs with 100-Ω internal termination. Requires external 4.7-µF AC coupling capacitors. Output driver OUT0± can be disabled under user control.
OUT0-	17	O, Analog	
OUT1+	15	O, Analog	Differential complementary outputs with 100-Ω internal termination. Requires external 4.7-µF AC coupling capacitors. Output driver OUT1± can be disabled under user control.
OUT1-	14	O, Analog	
Control Pins			
CD_N	12	O, LVCMOS, OD	CD_N is the carrier detect. CD_N is pulled LOW when signal is detected and adaptation is completed. CD_N is an open drain output. It requires an external resistor to logic supply. CD_N is tolerant to 3.3 V when VDDIO is powered from 2.5 V supply.
IN_OUT_SEL	8	I, 4-LEVEL	IN_OUT_SEL selects the signal flow at input port IN0 to output ports. See Table 2 for details. This pin setting can be overridden by register control.
OUT_CTRL	19	I, 4-LEVEL	OUT_CTRL selects the equalized or un-equalized signal from IN0 to OUT0± and OUT1±. See Table 3 for details. This pin setting can be overridden by register control.
VOD_DE	11	I, 4-LEVEL	VOD_DE selects the driver output amplitude and de-emphasis level for both OUT0± and OUT1±. See Table 4 for details. This pin setting can be overridden by register control.
MODE_SEL	6	I, 4-LEVEL	MODE_SEL enables SPI or SMBus serial control interface. See Table 5 for details.

(1) Note: I = Input, O=Output, IO=Input or Output, OD=Open Drain, LVCMOS=2-State Logic, 4-LEVEL=4-State Logic

Pin Functions (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
Serial Control Interface (SPI Mode), MODE_SEL = F (Float)			
SS_N	7	I, LVCMOS	SS_N is the Slave Select. When SS_N is at logic Low, it enables SPI access to the LMH0324 slave device. SS_N is a LVCMOS input referenced to VDDIO.
MISO	20	O, LVCMOS	MISO is the SPI serial data output from the LMH0324 slave device. MISO is a LVCMOS output referenced to VDDIO.
MOSI	10	I, LVCMOS	MOSI is used as the SPI serial data input to the LMH0324 slave device. MOSI is LVCMOS input referenced to VDDIO.
SCK	21	I, LVCMOS	SCK is the SPI serial input clock to the LMH0324 slave device. SCK is LVCMOS referenced to VDDIO.
Serial Control Interface (SMBus MODE) , MODE_SEL = L (1 kΩ to VSS)			
ADDR0	7	Strap, 4-LEVEL	ADDR[1:0] are SMBus address straps to select one of the 16 supported SMBus addresses. ADDR[1:0] are 4-level straps and are read into the device at power up.
ADDR1	20	Strap, 4-LEVEL	
SDA	10	IO, LVCMOS, OD	SMBus bi-directional open drain data line to or from the LMH0324 slave device. SDA is an open drain IO and requires an external 2 kΩ to 5 kΩ pull-up resistor to the SMBus termination voltage. SDA is 3.3 V tolerant when VDDIO is powered from 2.5 V.
SCL	21	I, LVCMOS, OD	SMBus input clock to the LMH0324 slave device. It is driven by a LVCMOS open drain driver from the SMBus master. SCL requires an external 2 kΩ to 5 kΩ pull-up resistor to the SMBus termination voltage. SCL is 3.3 V tolerant when VDDIO is powered from 2.5 V.
Power			
VSS	3, 9, 16	I, Ground	Ground reference.
VIN	24	I, Power	VIN is connected to an external power supply. It accepts either 2.5 V ± 5% or 1.8 V ± 5%. When VIN is powered from 2.5 V, VDD_LDO is the output of an on-chip LDO regulator and requires a bypass capacitor to VSS. When VIN is powered from 1.8 V, for lower power operation, both VIN and VDD_LDO should be connected to 1.8 V supply.
VDDIO	22	I, Power	VDDIO powers the LVCMOS IO and 4-level input logic. VDDIO should be connected to 2.5 V ± 5% or 1.8 V ± 5%. VDDIO must always be greater than or equal to VIN. For SMBus access, VDDIO must be 2.5 V ± 5%.
VDD_LDO	23	IO, Power	VDD_LDO is the output of the internal 1.8 V LDO regulator when VIN is connected to 2.5 V supply. VDD_LDO output requires external 1-µF and 0.1-µF bypass capacitors to VSS. The internal LDO is designed to power internal circuitry only. VDD_LDO is an input when VIN is powered from 1.8 V for lower power operation. When VIN is connected to a 1.8 V supply, both VIN and VDD_LDO should be connected to the 1.8 V supply.
RSV_L	13	I	For pin compatibility with the LMH1219 (11.88 Gbps Ultra-HD adaptive cable equalizer with integrated reclocker), connect RSV_L to a 2.5 V supply with a 0.1-µF bypass capacitor. For low power operation, tie RSV_L to VSS. See Power Supply Recommendations for details.
EP		I, Ground	EP is the exposed pad at the bottom of the QFN package. The exposed pad must be connected to the ground plane through a via array. See Figure 26 for details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage for 2.5-V Mode (VIN, VDDIO)	–0.5	2.75	V
Supply Voltage for 1.8-V Mode (VIN, VDD_LDO, VDDIO)	–0.5	2.0	V
4-Level Input/Output Voltage for 2.5 V Supply (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL, ADDR0, ADDR1)	–0.5	2.75	V
4-Level Input/Output Voltage for 1.8 V Supply (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL, ADDR0, ADDR1)	-0.5	2.0	V
SMBus Input/Output Voltage (SDA, SCL)(2)	–0.5	4.0	V
SPI Input/Output Voltage for 2.5 V Supply (SS_N, MISO, MOSI, and SCK)	–0.5	2.75	V
SPI Input/Output Voltage for 1.8 V Supply (SS_N, MISO, MOSI, and SCK)	-0.5	2.0	V
Input Voltage (IN0±)	–0.5	2.75	V
Input Current (IN0±)	–30	30	mA
Junction Temperature		125	°C
Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) SDA and SCL is 3.3 V tolerant when VDDIO is 2.5 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions. Pins listed as ±4500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions. Pins listed as ±1500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
2.5 V Supplies	VIN, VDDIO to VSS		2.375	2.5	2.625	V
1.8 V Supplies	VIN, VDDIO , VDD_LDO to VSS		1.71	1.8	1.89	V
VDD_{SMBUS}	SMBus: SDA, SCL Open Drain Termination Voltage, VDDIO = 2.5 V		2.375		3.6	V
V_{LAUNCH}	Source Launch Amplitude before Coax		0.72	0.8	0.88	Vp-p
	Splitter Mode		0.36	0.4	0.44	
$T_{JUNCTION}$	Operating Junction Temperature				100	°C
$T_{AMBIENT}$	Ambient Temperature		–40	25	85	°C
N_{PS}(1)	Supply Noise	50 Hz to 1 MHz, Sinusoidal		<20		mVp-p
		1.1 MHz to 6 GHz, Sinusoidal		<10		

(1) The sum of the DC supply voltage and AC supply noise should not exceed the recommended supply voltage range.

6.4 Thermal Information

THERMAL METRIC[1][2]		LMH0324 RTW (QFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) No heat sink is assumed for these estimations. Depending on the application, a heat sink, faster air flow, and/or reduced ambient temperature (<85°C) may be required in order to maintain the maximum junction temperature specified in *Electrical Characteristics*.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD_{1P8V}	Power Consumption[1]	Measured with PRBS-10, VOD = Default, only OUT0 enabled, 2.97 Gbps, VIN=VDD_LDO=VDDIO=1.8 V		78		mW
		Measured with PRBS-10, VOD = Default, OUT0 and OUT1 enabled, 2.97 Gbps, VIN=VDD_LDO=VDDIO=1.8 V		100		mW
PD_{Z1P8V}	Power Consumption[1]	Power Save Mode: No input signal, VIN=VDD_LDO=VDDIO=1.8 V		15		mW
PD_{2P5V}	Power Consumption[1]	Measured with PRBS-10, 2.97 Gbps, VOD = Default, only OUT0 enabled, VIN=VDDIO=2.5 V		128		mW
		Measured with PRBS-10, 2.97 Gbps, VOD = Default, OUT0 and OUT1 enabled, VIN=VDDIO=2.5 V		147		mW
PD_{Z2P5V}	Power Consumption[1]	Power Save Mode: No input signal, VIN=VDDIO=2.5 V		28		mW
IDD	Current Consumption[1]	Measured at 1.8 V supply with PRBS-10, 2.97 Gbps, VOD = Default, only OUT0 enabled		43	55	mA
		Measured at 2.5 V supply with PRBS-10, 2.97 Gbps, VOD = Default, only OUT0 enabled		51	71	
IDD_{Z_1P8V}	Current Consumption[1]	Forced Power Save Mode: MODE_SEL = LEVEL-H, Measured at 1.8 V supply, VIN=VDD_LDO=VDDIO=1.8 V		4	10	mA
V_{LDO}	LDO 1.8 V Output Voltage	VIN = VDDIO = 2.5 V	1.71	1.8	1.89	V

(1) Measured with RSV_L tied to VSS.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	2-Level Input (SS_N, SCK, MOSI), VDDIO = 2.5 V or 1.8 V	0.7 x VDDIO		VDDIO + 0.3	V
		2-Level Input (SCL, SDA), VDDIO = 2.5 V	0.7 x VDDIO		3.6	
V_{IL}	Low Level Input Voltage	2-Level Input (SS_N, SCK, MOSI) VDDIO = 2.5 V or 1.8 V	-0.3		0.3 x VDDIO	V
		2-Level Input (SCL, SDA), VDDIO = 2.5 V	0		0.3 x VDDIO	
V_{OH}	High Level Output Voltage	I_{OH} = -2 mA, (MISO), VDDIO = 2.5 V or 1.8 V	0.8 x VDDIO		VDDIO	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA, (MISO), VDDIO = 2.5 V or 1.8 V	0		0.2 x VDDIO	V
		I_{OL} = 3 mA, (CD_N, SCL, SDA), VDDIO = 2.5 V	0		0.4	
I_{IH}	Input High Leakage Current	SPI Mode: LVCMOS (SS_N, SCK, MOSI), Vinput = VDDIO			15	µA
		SMBus Mode: LVCMOS (CD_N, SCL, SDA), Vinput = VDDIO			10	
I_{IL}	Input Low Leakage Current	SPI Mode: LVCMOS (SS_N), Vinput = VSS	-40			µA
		SPI Mode: LVCMOS (SCK, MOSI), Vinput = VSS	-15			
		SMBus Mode: LVCMOS (CD_N, SCL, SDA), Vinput = VSS	-10			
4-LEVEL LOGIC DC SPECIFICATIONS (REFERENCE TO VDDIO, APPLY TO ALL 4-LEVEL INPUT CONTROL PINS)						
$V_{4\_LVL\_H}$	LEVEL-H Input Voltage	External pull-up 1 kΩ to VDDIO		VDDIO		V
$V_{4\_LVL\_F}$	LEVEL-F Default Voltage	Float, VDDIO = 2.5 V or 1.8 V		2/3 x VDDIO		V
$V_{4\_LVL\_R}$	LEVEL-R Input Voltage	External pull-down 20 kΩ to VSS, VDDIO = 2.5 V or 1.8 V		1/3 x VDDIO		V
$V_{4\_LVL\_L}$	LEVEL-L Input Voltage	External pull-down 1 kΩ to VSS		0		V
$I_{4\_LVL\_IH}$	Input High Leakage Current	4-Levels (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL), Vinput = VDDIO	20	45	80	µA
		SMBus Mode: 4-Levels (ADDR0, ADDR1), Vinput = VDDIO	20	45	80	
$I_{4\_LVL\_IL}$	Input Low Leakage Current	4-Levels (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL), Vinput = VSS	-160	–93	-40	µA
		SMBus Mode: 4-Levels (ADDR0, ADDR1), Vinput = VSS	-160	–93	-40	
RECEIVER SPECIFICATIONS (IN0+)						
R_{IN0_TERM}	DC Input Termination	IN0+ and IN0- to VSS	63	75	87	Ω
RL_{IN0}	Input Return Loss Reference to 75 Ω (2)	S11, 5 MHz to 1.485 GHz		–20		dB
		S11, 1.485 GHz to 3 GHz		–18		
V_{IN0_CM}	IN0 DC Common Mode Voltage	Input common mode voltage at IN0+ to VSS		1.4		V
V_{WANDER}	Input DC Wander	SD signal at IN0+, Input launch amplitude = 0.8 Vp-p		100		mVp-p
		HD, 3G signal at IN0+, Input launch amplitude = 0.8 Vp-p		50		mVp-p

(2) This parameter was measured with an LMH0324-18EVM.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS (OUT0± OR OUT1±)						
VOD	Output Differential Voltage(3)	8T pattern, see Figure 6, VOD_DE = LEVEL-H SD, HD, and 3G		410		mVp-p
		8T pattern, see Figure 6,VOD_DE = LEVEL-F SD, HD, and 3G	485	560	620	
		8T pattern, see Figure 6, VOD_DE = LEVEL-R SD, HD, and 3G		635		
		8T pattern, see Figure 6, VOD_DE = LEVEL-L SD, HD, and 3G		810		
VOD_{DE}	De-emphasized Output Differential Voltage(3)	8T pattern, see Figure 7, VOD_DE = LEVEL-H SD, HD, and 3G		410		
		8T pattern, see Figure 7, VOD_DE = LEVEL-F Default SD, HD, and 3G		500		
		8T pattern, see Figure 7, VOD_DE = LEVEL-R SD, HD, and 3G		480		
		8T pattern, see Figure 7, VOD_DE = LEVEL-L SD, HD, and 3G		480		
R_{OUT_TERM}	DC Output Differential Termination	Measured across OUTn+ and OUTn-	80	100	120	Ω
t_R/t_F	Output Rise or Fall Time (4)	20% - 80% using 8T Pattern 270 Mbps, 1.485 Gbps, 2.97 Gbps, measured after 1 inch trace		45		ps
D_R	Input Data Rate		125			Mbps
					2.97	Gbps
JIT_{RATE}	Jitter for Various Cable Length(4)	2.97 Gbps B1694A: 0 – 150 m		0.25		UI
		2.97 Gbps B1694A: 150 m		0.25	0.4	
		2.97 Gbps B1694A: 150 - 200 m		0.55		
		1.485 Gbps B1694A: 0 – 200 m		0.2		
		1.485 Gbps B1694A: 200 m		0.2	0.35	
		1.485 Gbps B1694A: 200 – 300 m		0.55		
		270 Mbps B1694A: 0 – 400 m		0.2		
		270 Mbps B1694A: 400 m		0.15	0.3	
		270 Mbps B1694A: 400 – 600 m		0.35		
T_{ADAPT}	Equalizer Adapt Time - Signal detect to Adaptation Completed	PRBS-10, Belden 1694A coax cable, nominal launch amplitude of 0.8 Vpp, 2.97 Gbps		5		ms

(3) ATE production tested with DC method.
(4) This parameter was measured with an LMH0324-18EVM.

6.6 Recommended SMBus Interface AC Timing Specifications

over recommended operating supply and temperature ranges (unless otherwise noted) (1)(2) (3)

			MIN	NOM	MAX	UNIT
F_{SCL}	SMBus SCL Frequency		10		400	kHz
T_{BUF}	Bus Free Time between Stop and Start Condition		1.3			µs
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.		0.6			µs
$T_{SU:STA}$	Repeated Start Condition Setup Time		0.6			µs
$T_{SU:STO}$	Stop Condition Setup Time		0.6			µs
$T_{HD:DAT}$	Data Hold Time		0			ns
$T_{SU:DAT}$	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period		0.6			µs
T_R	Clock/Data Rise Time				300	ns
T_F	Clock/Data Fall Time				300	ns

(1) These parameters support SMBus 2.0 specifications.
(2) These parameters are not production tested.
(3) See Figure 1 for timing diagrams.

6.7 Serial Parallel Interface (SPI) AC Timing Specifications

over recommended operating supply and temperature ranges (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
F_{SCK}	SPI SCK Frequency			10	20	MHz
T_{SCK}	SCK Period		50			ns
T_{PH}	SCK Pulse Width High		0.40 x T_{SCK}			ns
T_{PL}	SCK Pulse Width Low		0.40 x T_{SCK}			ns
T_{SU}	MOSI Setup Time		4			ns
T_H	MOSI Hold Time		4			ns
T_{SSSU}	SS_N Setup Time		14			ns
T_{SSH}	SS_N Hold Time		4			ns
T_{SSOF}	SS_N Off Time		1			µs
T_{ODZ}	MISO Driven-to-Tristate Time			20		ns
T_{OZD}	MISO Tristate-to-Driven Time			10		ns
T_{OD}	MISO Output Delay Time			15		ns

(1) See Figure 2 for timing diagrams.

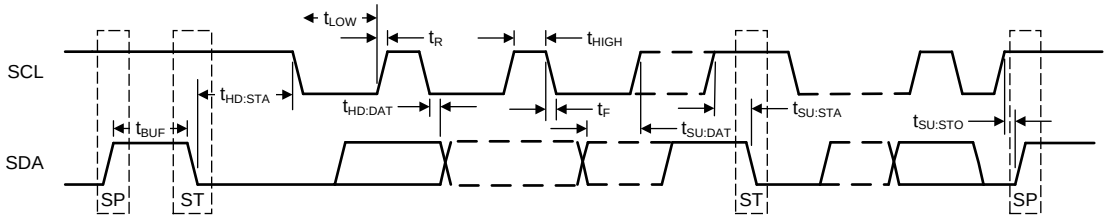


Figure 1. SMBus Timing Parameters

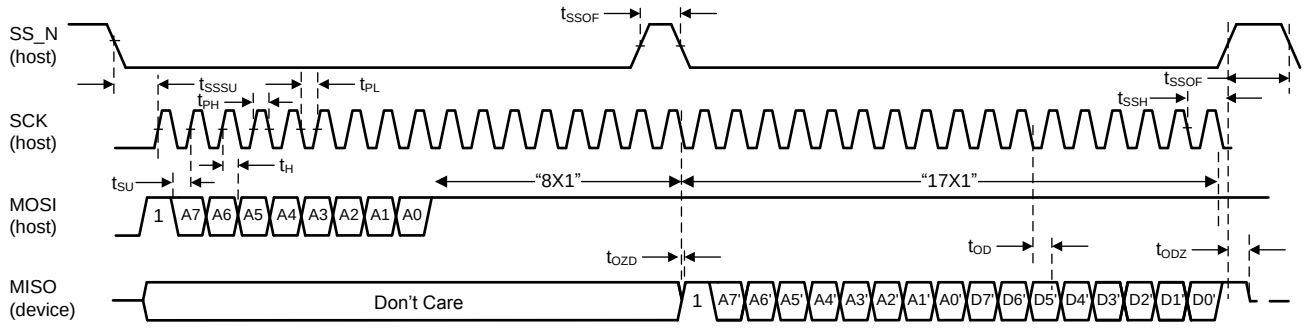


Figure 2. SPI Timing Parameters

6.8 Typical Characteristics

Typical device characteristics at T_A = 25°C and VIN = VDDIO = 2.5 V, unless otherwise noted.

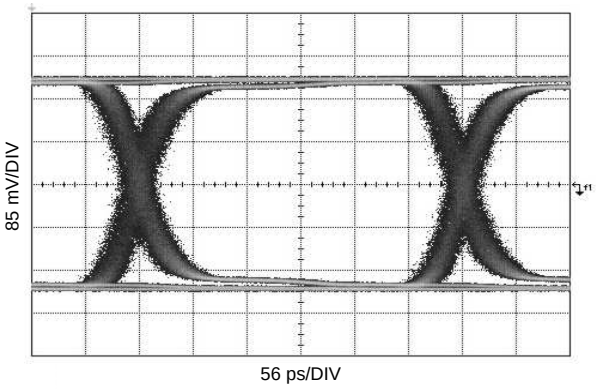


Figure 3. 2.97 Gbps, Input: 150 m Belden 1694A PRBS10

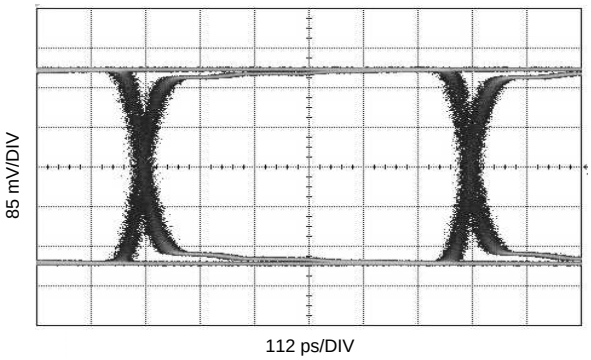


Figure 4. 1.485 Gbps, Input: 200 m Belden 1694A PRBS10

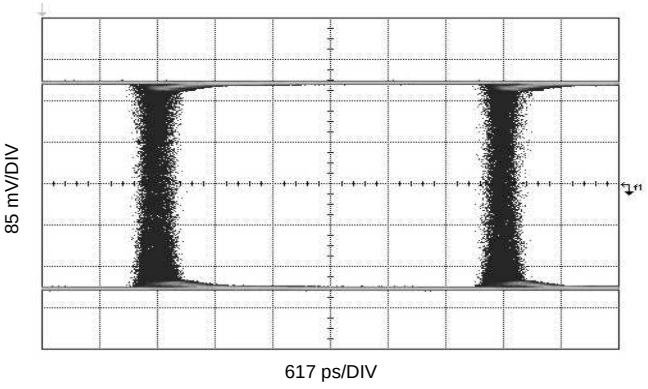


Figure 5. 270 Mbps, Input: 400 m Belden 1694A PRBS10

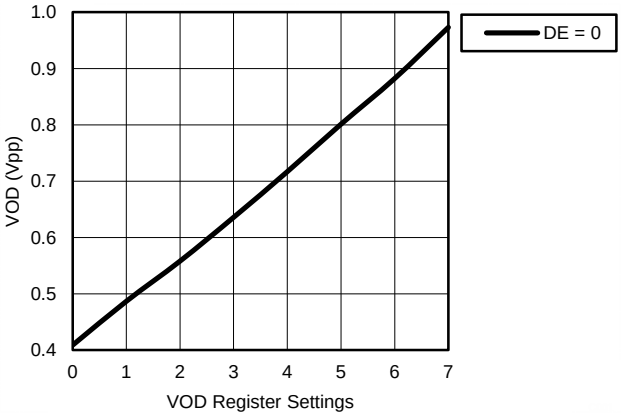


Figure 6. VOD vs. VOD and DEM Register Settings

Typical Characteristics (continued)

Typical device characteristics at T_A = 25°C and VIN = VDDIO = 2.5 V, unless otherwise noted.

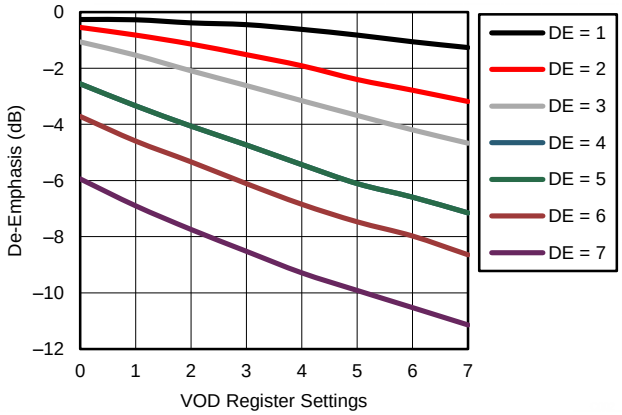


Figure 7. De-emphasis vs. VOD and DEM Register Settings

7 Detailed Description

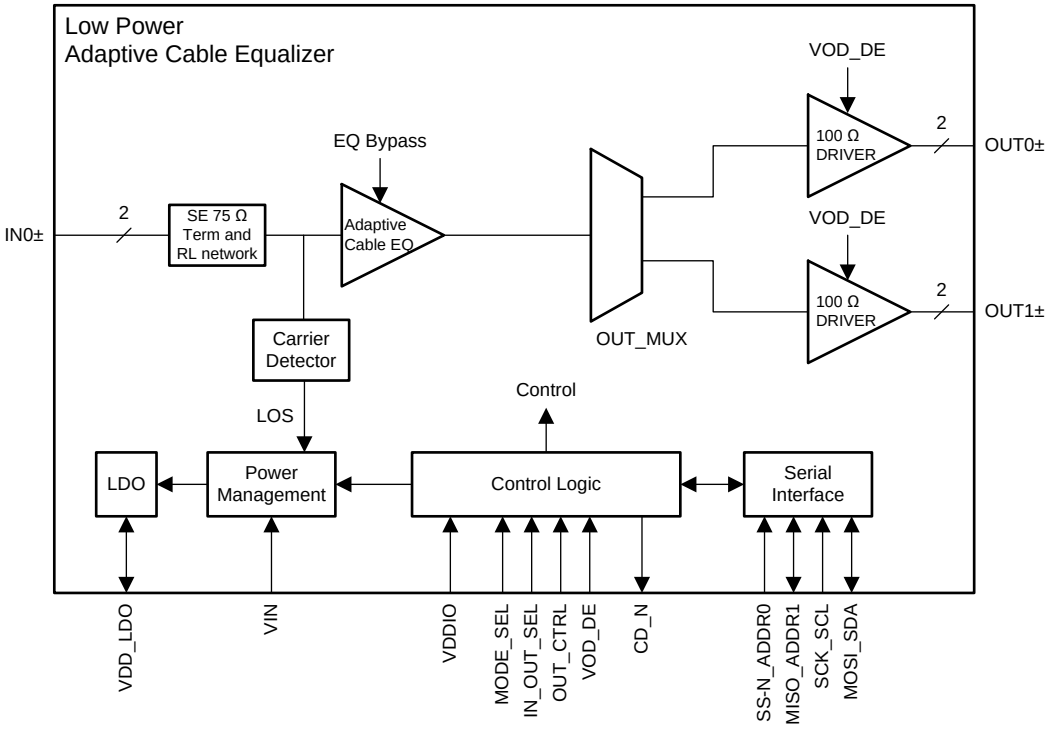
7.1 Overview

The LMH0324 is an adaptive cable equalizer designed to equalize serial digital video data transmitted over long distance of coaxial cable, such as Belden 1694A. It is designed with high gain equalization boost implemented with low power and low noise circuitry, supporting 3G/HD/SD SDI video transport over high loss coaxial cable.

It is designed to support common video data rates from 125 Mbps to 2.97 Gbps, compatible to SMPTE video standards ST-424, ST-344, ST-292, ST-259, and DVB-ASI.

The LMH0324 automatically selects the correct level of equalization boost based on the signal quality of the input signal. It offers two output drivers that support fan-out buffering. Programmable de-emphasis is available to reduce the inter-symbol interference jitter caused by the printed circuit board traces connecting the drivers to their downstream receivers.

7.2 Functional Block Diagram



7.3 Feature Description

The LMH0324 consists of several key blocks:

- *4-Level Input Configuration Pins*
- *Carrier Detect*
- *Adaptive Cable Equalizer*
- *Launch Amplitude*
- *Input-Output Mux Selection*
- *Output Function Control*
- *Output Driver Amplitude and De-Emphasis Control*

7.3.1 4-Level Input Configuration Pins

The 4-level input configuration pins use a resistor divider to provide four logic states for each control pin. There is an internal 30-kΩ pullup and a 60-kΩ pulldown connected to the control pin that sets the default voltage at 2/3 x VDDIO. These resistors, together with the external resistor, combine to achieve the desired voltage level. By using the 1-kΩ pull-down, 20-kΩ pulldown, no connect, and 1-kΩ pullup, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTING	RESULTING PIN VOLTAGE
H	Tie 1 kΩ to VDDIO	VDDIO
F	Float (leave pin open)	2/3 × VDDIO
R	Tie 20 kΩ to VSS	1/3 × VDDIO
L	Tie 1 kΩ to VSS	0

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VDDIO
- Internal Threshold between R and F = 0.5 × VDDIO
- Internal Threshold between F and H = 0.8 × VDDIO

7.3.2 Carrier Detect

An internal Carrier Detector circuit is used to monitor the presence or absence of the input signal. When the input signal amplitude exceeds the carrier detector's threshold, adaptation is activated, and CD_N is pulled low at the end of adaptation. When the input signal amplitude is below the carrier detector's threshold, input equalization circuitry is powered down and the CD_N is pulled high to indicate absence of input signal. The LMH0324 high gain adaptive cable equalizer supports long cable reach. As a result, the carrier detector threshold is sensitive, and system designers need to pay close attention to the PCB layout to avoid excessive crosstalk from interfering with the carrier detection.

In the absence of input signal, the LMH0324 automatically goes into Power Save Mode to conserve power consumption. When valid signal is detected, the LMH0324 automatically exits the Power Save Mode and returns to the normal operating mode. An LED can be connected to CD_N through a current limiting resistor to provide visual indication of the carrier detection.

7.3.3 Adaptive Cable Equalizer

IN0+ is the input to the adaptive cable equalizer. It has an on-chip 75-Ω termination to the input common mode voltage and includes a series return loss compensation network for meeting stringent SMPTE return loss requirements. It is designed for AC coupling, requiring a 4.7-µF AC coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern. The cable equalizer is designed with high gain and low noise circuitry to compensate for the insertion loss of a coaxial cable, such as Belden 1694A, which is widely used in broadcast video infrastructures.

Internal control loops are used to monitor the input signal quality and automatically select the optimum equalization boost and DC offset compensation. The LMH0324 is designed to handle the stringent pathological pattern defined in the SMPTE RP 198 and SMPTE RP 178 standards.

7.3.4 Launch Amplitude

The LMH0324 is designed to equalize data transmitted through a coaxial cable driven by a SMPTE compatible cable driver with launch amplitude of 800 mVp-p ± 10%. In applications where a 1:2 passive splitter is used, the signal amplitude is reduced by half due to the 6 dB insertion loss of the splitter. The LMH0324 is designed to support -6 dB splitter mode, enabled by SPI or SMBus serial interface.

7.3.5 Input-Output Mux Selection

By default, the LMH0324 input-to-output signal flow and data rate selection are configured by the IN_OUT_SEL pin logic settings shown in Table 2. These settings can be overridden via register control by applying the appropriate override bit values.

Table 2. IN_OUT_SEL Pin Settings

LEVEL	DEFINITION
H	IN0 to OUT0 and OUT1
F	IN0 to OUT0 (with OUT1 disabled)
R	Reserved
L	Reserved

7.3.6 Output Function Control

By default, the LMH0324 output function control for OUT0 and OUT1 is configured by the OUT_CTRL pin logic settings shown in Table 3. These settings can be overridden via register control by applying the appropriate override bit values.

Table 3. OUT_CTRL Pin Settings

LEVEL	DEFINITION
H	Equalizer Bypass Raw data at IN0+ is routed to the output drivers
F	Normal Data Equalized data is routed to the output drivers
R	Reserved
L	Reserved

7.3.7 Output Driver Amplitude and De-Emphasis Control

The VOD_DE control pin selects the output amplitude and de-emphasis settings for both OUT0± and OUT1±. It offers users the capability to select higher output amplitude and de-emphasis level for longer board trace that connects the drivers to their downstream receivers. Driver de-emphasis provides transmitter equalization to reduce the ISI caused by the board trace.

By default, the output driver VOD and de-emphasis settings are configured by the VOD_DE pin logic settings shown in Table 4. These settings can be overridden via register control. Through register programming, the output amplitude and de-emphasis level can be individually set for OUT0± and OUT1±. SPI and SMBus register programming provide a wider range of output amplitude and de-emphasis levels.

Table 4. Recommended VOD_DE Pin and Register Settings for Different FR4 Trace Lengths (1)

VOD_DE LEVEL	VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp) (2)	VOD_{DE} (mVpp) (2)	DEM (dB)	FR4 TRACE LENGTH (inches)
H	0	0	410	410	0	0 – 1
F	2	2	560	500	-0.9	2 – 4
R	3	3	635	480	-2.4	5 – 6
L	5	5	810	480	-6.1	7 – 8

(1) The output drivers are capable of providing higher VOD and DEM levels (max settings are 7). For more VOD and de-emphasis levels, refer to Table 9.
(2) See Figure 8.

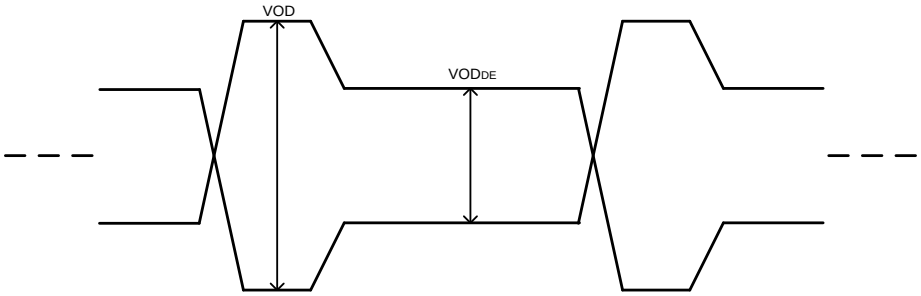


Figure 8. VOD and VOD_{DE} Levels

7.3.8 Additional Programmability

The LMH0324 supports extended programmability through the use of an SPI or SMBus serial control interface. Such added programmability includes:

- Cable Length Indicator (CLI).
- Digital $MUTE_{REF}$

7.3.8.1 Cable Length Indicator (CLI)

The Cable Length Indicator (CLI) indicates the length of the coaxial cable attached to IN0+. CLI is accessible through CableEQ/Driver Page Reg 0x25[5:0]. The 6-bit setting ranges in decimal value from 0 to 55 (000000'b to 110111'b binary), corresponding to approximately 0 to 600 m of Belden 1694A cable.

7.3.8.2 Digital $MUTE_{REF}$

Digital $MUTE_{REF}$ CableEQ/Driver Page Reg 0x03[5:0] sets the threshold for the maximum cable length to be equalized before muting the outputs. The $MUTE_{REF}$ register value is directly proportional to the cable length being equalized. $MUTE_{REF}$ is data rate dependent. Follow the steps below to set $MUTE_{REF}$ register setting for any desired SDI rate:

1. Connect the desired input cable length at which the driver output needs to be muted.
2. Send video pattern at IN0+ at the SD rate (270 Mbps). At SD, the Cable Length Indicator (CLI) has the largest dynamic range.
3. Read back Cable EQ/Driver Page Reg 0x25[5:0] to record the CLI value.
4. Copy the CLI value, and write this value to Digital $MUTE_{REF}$ Cable EQ/Driver Page Reg 0x03[5:0].

7.4 Device Functional Modes

The LMH0324 operates in one of two modes: System Management Bus (SMBus) or Serial Peripheral Interface (SPI) mode. In order to determine the mode of operation, the proper setting must be applied to the MODE_SEL pin at power-up, as detailed in Table 5.

Table 5. MODE_SEL Pin Settings

LEVEL	DEFINITION
H	Forced Power Save Mode, only SPI is enabled (all other circuitry powered down)
F	Select SPI Interface for register access
R	Reserved for factory testing – do not use
L	Select SMBus Interface for register access

NOTE

Changing logic states between LEVEL-L and LEVEL-H after power up is not allowed.

7.4.1 System Management Bus (SMBus) Mode

If MODE_SEL = L, the LMH0324 is in SMBus mode. In SMBus mode, Pins 10 and 21 are configured as SDA and SCL. Pins 7 and 20 act as 4-level address straps for ADDR0 and ADDR1 at power up to determine the 7-bit slave address of the LMH0324, as shown in Table 6.

Table 6. SMBus Device Slave Addresses(1)

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT SLAVE ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX]
L	L	1D	3A
L	R	1E	3C
L	F	1F	3E
L	H	20	40
R	L	21	42
R	R	22	44
R	F	23	46
R	H	24	48
F	L	25	4A
F	R	26	4C
F	F	27	4E
F	H	28	50
H	L	29	52
H	R	2A	54
H	F	2B	56
H	H	2C	58

(1) The 8-bit write command consists of the 7-bit slave address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit slave address is 0x1D (001 1101'b), the 8-bit write command is 0x3A (0011 1010'b).

7.4.1.1 SMBus Read and Write Transactions

SMBus is a two-wire serial interface through which various system component chips can communicate with the master. Slave devices are identified by having a unique device address. The two-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The LMH0324 SMBus SCL and SDA signals are open drain and require external pull-up resistors.

Start and Stop:

The master generates start and stop patterns at the beginning and end of each transaction.

- Start: High to low transition (falling edge) of SDA while SCL is high.
- Stop: Low to high transition (rising edge) of SDA while SCL is high.

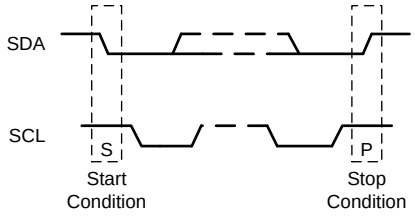


Figure 9. Start and Stop Conditions

The master generates nine clock pulses for each byte transfer. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is recorded when the device pulls SDA low, while a NACK is recorded if the line remains high.

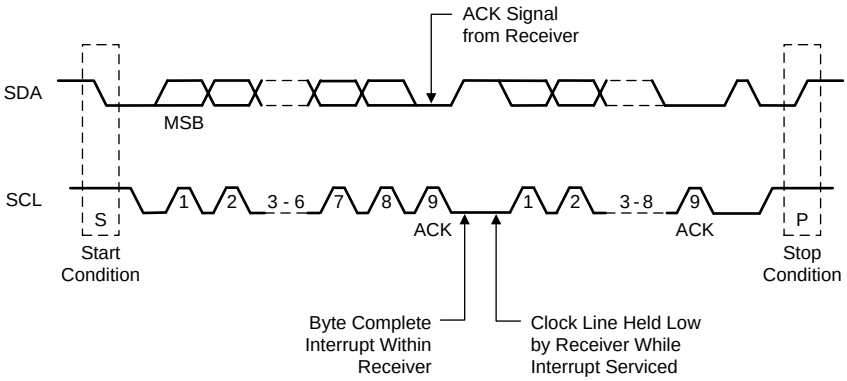


Figure 10. Acknowledge (ACK)

7.4.1.1.1 SMBus Write Operation Format

Writing data to a slave device consists of three parts, as illustrated in Figure 11:

1. The master begins with a start condition, followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the 8-bit data is written, followed by a stop condition.

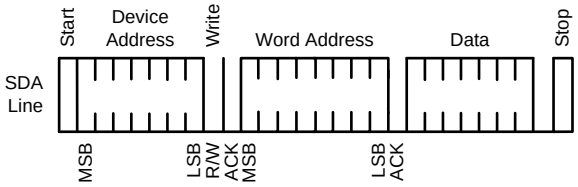


Figure 11. SMBus Write Operation

7.4.1.1.2 SMBus Read Operation Format

Reading data from a slave device consists of four parts, as illustrated in Figure 12:

1. The master begins with a start condition, followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the master initiates a re-start condition, followed by the slave address with the R/$\overline{W}$ bit set to 1'b.
4. After an ACK from the slave device, the 8-bit data is read back. The last ACK is high if there are no more bytes to read, and the last read is followed by a stop condition.

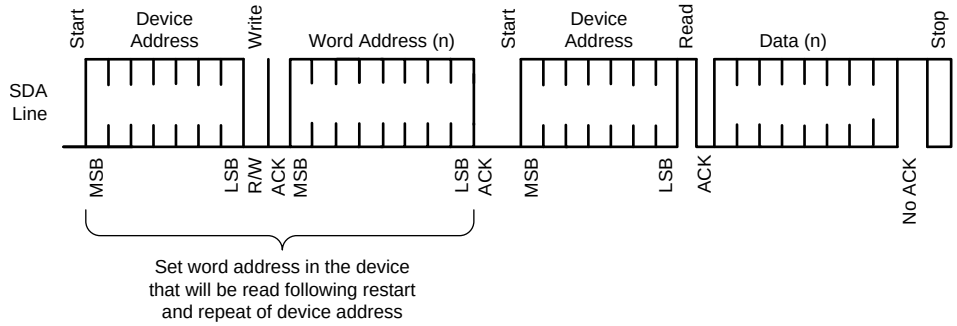


Figure 12. SMBus Read Operation

7.4.2 Serial Peripheral Interface (SPI) Mode

If MODE_SEL = F or H, the LMH0324 is in SPI mode. In SPI mode, the following pins are used for SPI bus communication:

- MOSI (pin 10): Master Output Slave Input
- MISO (pin 20): Master Input Slave Output
- SS_N (pin 7): Slave Select (active low)
- SCK (pin 21): Serial clock (input to the LMH0324 slave device)

7.4.2.1 SPI Read and Write Transactions

Each SPI transaction to a single device is 17 bits long and is framed by SS_N when asserted low. The MOSI input is ignored, and the MISO output is floated whenever SS_N is de-asserted (high).

The bits are shifted in left-to-right. The first bit is R/$\overline{W}$, which is 1'b for "read" and 0'b for "write." Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The previous SPI command, address, and data are shifted out on MISO as the current command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously when SS_N asserts low. The contents of a single MOSI or MISO transaction frame are shown in Table 7.

Table 7. 17-Bit Single SPI Transaction Frame

R/$\overline{W}$	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

7.4.2.1.1 SPI Write Transaction Format

For SPI writes, the R/$\overline{W}$ bit is 0'b. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of SS_N. The SPI transaction always starts on the rising edge of the clock.

The signal timing for a SPI Write transaction is shown in Figure 13. The "prime" values on MISO (for example, A7') reflect the contents of the shift register from the previous SPI transaction and are *don't-care* for the current transaction.

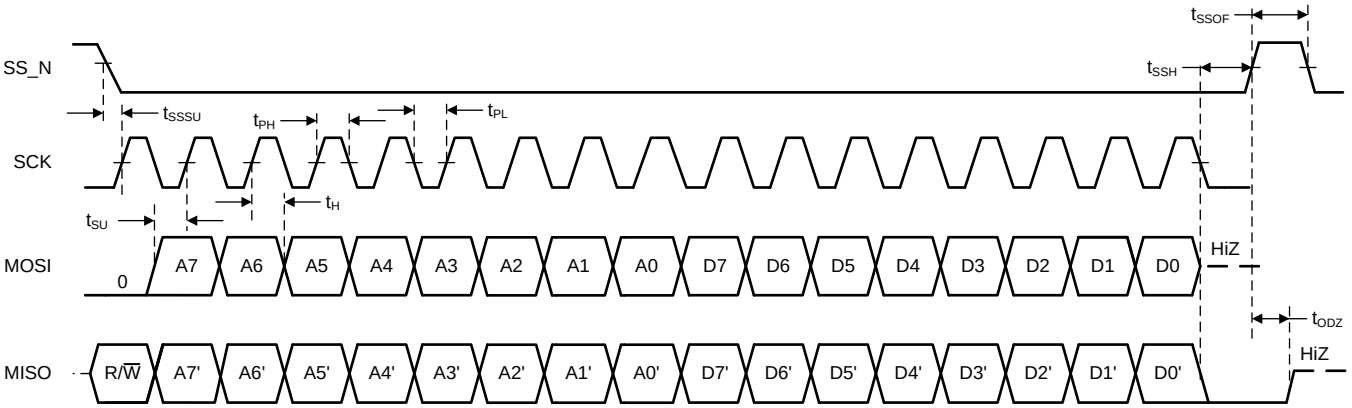


Figure 13. Signal Timing for a SPI Write Transaction

7.4.2.1.2 SPI Read Transaction Format

A SPI read transaction is 34 bits per device and consists of two 17-bit frames. The first 17-bit read transaction frame shifts in the address to be read, followed by a dummy transaction second frame to shift out 17-bit read data. The R/$\overline{W}$ bit is 1'b for the read transaction, as shown in Figure 14.

The first 17 bits from the read transaction specifies 1-bit of R/$\overline{W}$ and 8-bits of address A7-A0 in the first 8 bits. The eight 1's following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and needs to be ignored. However, the transaction is necessary in order to shift out the read data D7-D0 in the last 8 bits of the MISO output. As with the SPI Write, the "prime" values on MISO during the first 16 clocks are *don't-care* for this portion of the transaction. The values shifted out on MISO during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.

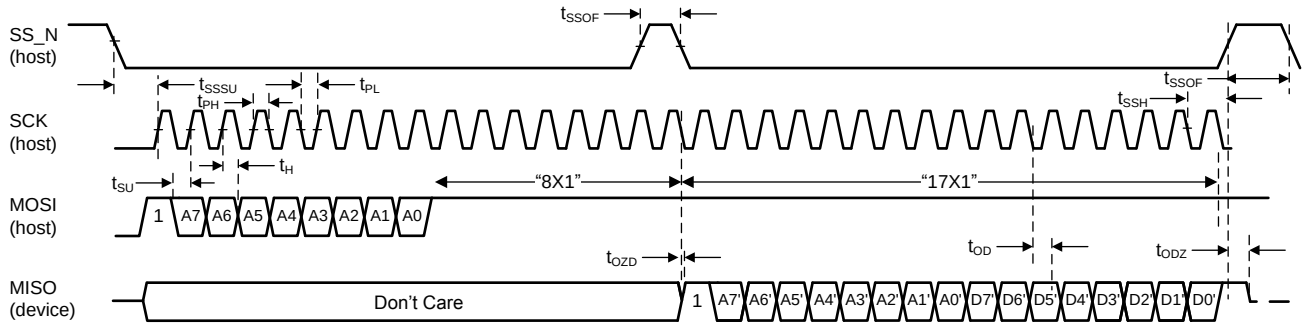


Figure 14. Signal Timing for a SPI Read Transaction

7.4.2.2 SPI Daisy Chain

The LMH0324 supports SPI daisy-chaining among multiple devices, as shown in Figure 15.

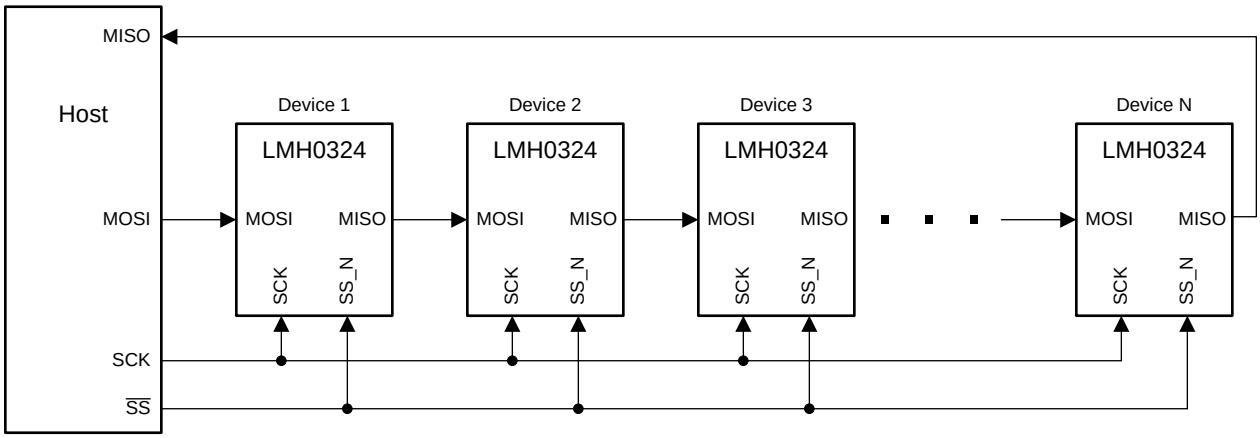


Figure 15. Daisy-Chain Configuration

Each LMH0324 device is directly connected to the SCK and SS_N pins of the host. The first LMH0324 device in the chain is connected to the host's MOSI pin, and the last device in the chain is connected to the host's MISO pin. The MOSI pin of each intermediate LMH0324 device in the chain is connected to the MISO pin of the previous LMH0324 device, thereby creating a serial shift register. In a daisy-chain configuration of N x LMH0324 devices, the host conceptually sees a shift register of length 17 x N for a basic SPI transaction, during which SS_N is asserted low for 17 x N clock cycles.

7.5 LMH0324 Register Map

The LMH0324 register set definition is divided into two register pages. These register pages are used to control different aspects of the LMH0324 functionality. A brief summary of the pages is shown below:

1. **Share Register Page**: This page corresponds to global parameters, such as LMH0324 device ID. This is the default page at start-up.
2. **CableEQ/Drivers Register Page**: This page corresponds to IN0 Cable EQ and both OUT0 and OUT1 driver output settings. Access this page by setting Reg 0xFF[2:0] = 101'b.

Please note the following about the LMH0324 default register values in the register map:

- Default register values were read after power-up with no active inputs applied to IN0.
- Default register values for Reserved "Read-Only" bits may vary dynamically from part to part.

7.5.1 Share Register Page

Address	Register Name	Bit	Field	Default	Type	Description
0x00	Reserved	7:0	Reserved	0x00	R	Reserved
0x01	Reserved	7:0	Reserved	0x40	R	Reserved
0x02	Reserved	7:0	Reserved	0x02	RW	Reserved
0x03	Reserved	7:0	Reserved	0x00	RW	Reserved
0x04	Reserved	7:0	Reserved	0x01	RW	Reserved
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved
0x06	Reserved	7:0	Reserved	0x00	RW	Reserved
0x07	Reserved	7:0	Reserved	0x04	RW	Reserved
0x08	Reserved	7:0	Reserved	0x11	RW	Reserved
0x09	Reserved	7:0	Reserved	0x00	R	Reserved
0xE2	Reset Share/Channel Regs	7:5	Reserved	0x10	R	Reserved
		4	reset_done		R	1 = Internal state machine register initialization done. 0 = Internal state machine register initialization not done.
		3:1	Reserved		RW	Reserved
		0	reset_init		RW	1 = Initialize internal state machine register settings.
0xF0	Device Revision	7:0	Version	0x02	R	Device Revision
0xF1	Device ID	7:0	Device_ID	0x81	R	For LMH0324, Device ID = 0x81
0xFF	Register Communication Control	7:6	Reserved	0x00	RW	Reserved
		5:4	Reserved		RW	Reserved
		3	Reserved		RW	Reserved
		2	page_select_enable		RW	0 = The shared registers are enabled. 1 = Enables communication access to the Register Page specified in Reg 0xFF[1:0].
		1:0	page_select		RW	Enable communication access to a specific Register Page 01 = CableEQ/Drivers Register Page Other values are invalid

7.5.2 CableEQ/Drivers Register Page

Address	Register Name	Bit	Field	Default	Type	Description
0x00	Reset CableEQ/Drivers Registers	7	adapt_cd	0x08	RW	CD_N pin status 0 = CD_N indicates when Coarse Adaptation is done 1 = CD_N indicates carrier detect
		6	Reserved		RW	Reserved
		5	reg_power_save_ov		RW	IN0 Power Save Override Control for Cable EQ 0 = Disable Power Save mode override. Automatic power save mode when no input signal detected. 1 = Enable Power Save mode override. Power Save mode control set by value in Reg 0x00[4:3].
		4:3	reg_power_save		RW	IN0 Auto Power Save mode control for Cable EQ if Reg 0x00[5] = 1 00 = Enable Power Save mode when no input signal is detected 01 = Disable auto Power Save mode 10 = Reserved 11 = Force Power Save mode
		2	rst_cableEQ/Drivers_regs		RW	Reset registers (self-clearing) 0 = Normal operation 1 = Reset CableEQ/Drivers Registers. Register re-initialization procedure required after resetting the CableEQ/Drivers Registers. Refer to the LMH0324 Programming Guide for details.
		1:0	Reserved		RW	Reserved
0x01	EQ Observation Status	7:1	Reserved	0x80	R	Reserved
		0	adaptation_status		R	0 = Adaptation not completed 1 = Adaptation completed
0x02	Rate and Driver Observation Status	7	Reserved	0x07	R	Reserved
		6	IN0 Carrier Detect		R	Carrier Detect Status of IN0 0 = No signal present at IN0 1 = Signal present at IN0
		5:3	freq_rate_det		R	Readback of rate detected 001 = 125M-270M 010 = 1.5G-3G
		2	power_save_status		R	Observation Bit 0 = Power Save Mode is Inactive 1 = Power Save Mode is Active
		1	mute_tx1		R	Observation Bit 0 = OUT1 Driver is Active 1 = OUT1 Driver is in Mute Note: When muted, driver output remains at common mode voltage.
		0	mute_tx0		R	Observation Bit 0 = OUT0 Driver is Active 1 = OUT0 Driver is in Mute Note: When muted, driver output remains at common mode voltage.
0x03	MUTERef Control	7:6	Reserved	0x3F	RW	Reserved
		5:0	MUTERef		RW	Digital MUTEref: Sets the threshold at which output will be muted. See Digital $MUTE_{REF}$.
0x04	Reserved	7:0	Reserved	0x00	RW	Reserved
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved
0x06	Reserved	7:0	Reserved	0xA0	RW	Reserved
0x07	Reserved	7:0	Reserved	0x24	RW	Reserved
0x08	Reserved	7:0	Reserved	0x27	RW	Reserved
0x09	Reserved	7:0	Reserved	0x01	RW	Reserved
0x0A	Reserved	7:0	Reserved	0x05	RW	Reserved
0x0B	Reserved	7:0	Reserved	0x37	RW	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x0C	Reserved	7:0	Reserved	0x01	RW	Reserved
0x0D	Reserved	7:0	Reserved	0x25	RW	Reserved
0x0E	Reserved	7:0	Reserved	0x37	RW	Reserved
0x0F	Reserved	7:0	Reserved	0x02	RW	Reserved
0x10	Reserved	7:0	Reserved	0x0A	RW	Reserved
0x11	Reserved	7:0	Reserved	0x02	RW	Reserved
0x12	Reserved	7:0	Reserved	0x08	RW	Reserved
0x13	Reserved	7:0	Reserved	0x04	RW	Reserved
0x14	Reserved	7:0	Reserved	0x3C	RW	Reserved
0x15	Reserved	7:0	Reserved	0x00	RW	Reserved
0x16	Reserved	7:0	Reserved	0x00	RW	Reserved
0x17	Reserved	7:0	Reserved	0x08	RW	Reserved
0x18	Reserved	7:0	Reserved	0x01	RW	Reserved
0x19	Reserved	7:0	Reserved	0x08	RW	Reserved
0x1A	Reserved	7:0	Reserved	0x01	RW	Reserved
0x1B	Reserved	7:0	Reserved	0xA7	RW	Reserved
0x1C	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x20	Reserved	7:0	Reserved	0x00	RW	Reserved
0x21	Reserved	7:0	Reserved	0xC0	RW	Reserved
0x22	Reserved	7:0	Reserved	0x00	RW	Reserved
0x23	Reserved	7:0	Reserved	0x00	RW	Reserved
0x24	Reserved	7:0	Reserved	0x00	RW	Reserved
0x25	Cable Length Indicator	7:6	Reserved	0x00	R	Reserved
		5:0	CLI		R	Readback of the Cable Length Indicator after adaptation is completed. See Cable Length Indicator (CLI).
0x26	Reserved	7:0	Reserved	0x05	R	Reserved
0x27	EQ Bypass Override	7:4	Reserved	0x00	RW	Reserved
		3	eq_bypass_ov		RW	Override eq_bypass value to analog core 0 = Disable EQ Bypass override 1 = Enable EQ Bypass override. Value of EQ Bypass Control determined by Reg 0x27[2].
		2	eq_bypass_val		RW	Override value of eq_bypass 0 = Do not Bypass Cable EQ. Use Adaptive EQ 1 = Bypass Cable EQ
		1:0	Reserved		RW	Reserved
0x28	Reserved	7:0	Reserved	0x00	RW	Reserved
0x29	Reserved	7:0	Reserved	0x20	R	Reserved
0x2A	Reserved	7:0	Reserved	0x40	RW	Reserved
0x2B	Reserved	7:0	Reserved	0x89	RW	Reserved
0x2C	Reserved	7:0	Reserved	0x0B	RW	Reserved
0x2D	Reserved	7:0	Reserved	0x20	RW	Reserved
0x2E	Reserved	7:0	Reserved	0x00	R	Reserved
0x2F	Reserved	7:0	Reserved	0x00	RW	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x30	OUT0 Output Control	7	tx0_mute_ov	0x0A	RW	OUT0 Mute Override Control 0 = Disable OUT0 Mute Override Control 1 = Enable OUT0 Mute Override Control by value in Reg 0x30[6].
		6	tx0_mute_val		RW	0 = Normal Operation 1 = Mute OUT0 if Reg 0x30[7] = 1
		5	tx0_vod_ov		RW	OUT0 VOD Override Control 0 = VOD settings for OUT0 determined by VOD_DE pin 1 = Override VOD pin settings for OUT0. VOD settings for OUT0 are controlled by Reg 0x30[2:0]
		4:3	Reserved		RW	Reserved
		2:0	tx0_vod		RW	VOD settings with DE = 0 for OUT0 if Reg 0x30[5] = 1. See Figure 6.
0x31	OUT0 De-Emphasis Control	7	Reserved	0x01	RW	Reserved
		6	tx0_dem_ov		RW	OUT0 De-Emphasis Override Control 0 = De-emphasis for OUT0 determined by VOD_DE pin 1 = Override De-emphasis settings for OUT0. De-emphasis settings for OUT0 are controlled by Reg 0x31[2:0]
		5	tx0_PD_ov		RW	OUT0 Power Down Override Control 0 = Disable OUT0 Power Down Override Control 1 = Enable OUT0 Power Down Override Control by value in Reg 0x31[4].
		4	tx0_PD		RW	0 = Normal Operation 1 = Power Down OUT0 if Reg 0x31[5] = 1
		3	Reserved		RW	Reserved
		2:0	tx0_dem		RW	De-emphasis settings for OUT0 if Reg 0x31[6] = 1. See Figure 7.
0x32	OUT1 Output Control	7	tx1_mute_ov	0x0A	RW	OUT1 Mute Override Control 0 = Disable OUT1 Mute Override Control 1 = Enable OUT1 Mute Override Control by value in Reg 0x32[6].
		6	tx1_mute_val		RW	0 = Normal Operation 1 = Mute OUT1 if Reg 0x32[7] = 1
		5	tx1_vod_ov		RW	OUT1 VOD Override Control 0 = VOD settings for OUT1 determined by VOD_DE pin 1 = Override VOD pin settings for OUT1. VOD settings for OUT1 are controlled by Reg 0x32[2:0]
		4:3	Reserved		RW	Reserved
		2:0	tx1_vod		RW	VOD settings with DE = 0 for OUT1 if Reg 0x32[5] = 1. See Figure 6.
0x33	OUT1 De-emphasis Control	7	Reserved	0x11	RW	Reserved
		6	tx1_dem_ov		RW	OUT1 De-Emphasis Override Control 0 = De-emphasis for OUT1 determined by VOD_DE pin 1 = Override De-emphasis settings for OUT1. De-emphasis settings for OUT1 are controlled by Reg 0x33[2:0]
		5	tx1_PD_ov		RW	OUT1 Power Down Override Control 0 = Disable OUT1 Power Down Override Control 1 = Enable OUT1 Power Down Override Control by value in Reg 0x33[4].
		4	tx1_PD		RW	0 = Normal Operation 1 = Power Down OUT1 if Reg 0x33[5] = 1
		3	Reserved		RW	Reserved
		2:0	tx1_dem		RW	De-emphasis settings for OUT1 if Reg 0x33[6] = 1. See Figure 7.
0x34	Splitter_Reg	7	hi_gain_mode	0x17	RW	-6 dB Launch Amplitude Adaptation Mode 0 = Enable EQ adaptation to operate with nominal 800 mV launch amplitude 1 = Enable EQ adaptation to operate with 400 mV launch amplitude
		6:0	Reserved			Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x35	Reserved	7:0	Reserved	0x61	RW	Reserved
0x36	Reserved	7:0	Reserved	0x02	RW	Reserved
0x37	Reserved	7:0	Reserved	0x00	RW	Reserved
0x38	Reserved	7:0	Reserved	0x00	RW	Reserved
0x39	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3A	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3B	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3C	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3D	Reserved	7:0	Reserved	0x7F	RW	Reserved
0x3E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x40	Reserved	7:0	Reserved	0x00	R	Reserved
0x41	Reserved	7:0	Reserved	0x00	R	Reserved
0x42	Reserved	7:0	Reserved	0x00	R	Reserved
0x43	Reserved	7:0	Reserved	0x00	R	Reserved
0x44	Reserved	7:0	Reserved	0x00	R	Reserved
0x45	Reserved	7:0	Reserved	0x00	R	Reserved
0x46	Reserved	7:0	Reserved	0x00	R	Reserved
0x47	Reserved	7:0	Reserved	0x00	R	Reserved
0x48	Reserved	7:0	Reserved	0x00	R	Reserved
0x49	Reserved	7:0	Reserved	0x01	R	Reserved
0x4A	Reserved	7:0	Reserved	0x00	R	Reserved
0x4B	Reserved	7:0	Reserved	0x00	R	Reserved
0x4C	Reserved	7:0	Reserved	0x00	R	Reserved
0x4D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x4E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x4F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x50	Reserved	7:0	Reserved	0x00	RW	Reserved
0x51	Reserved	7:0	Reserved	0x00	RW	Reserved
0x52	Reserved	7:0	Reserved	0x00	RW	Reserved
0x53	Reserved	7:0	Reserved	0x00	RW	Reserved
0x54	Reserved	7:0	Reserved	0x0F	R	Reserved

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 General Guidance for SMPTE Applications

SMPTE specifies the requirements for the Serial Digital Interface to transport digital video over coaxial cables. One of the requirements is meeting return loss, which specifies how closely the port resembles 75-Ω impedance across a specified frequency band. The SMPTE specifications also defines the use of AC coupling capacitors for transporting uncompressed serial data streams with heavy low frequency content. The use of 4.7-µF AC coupling capacitors is recommended to avoid low frequency DC wander. Refer to Table 8 for design requirements.

8.2 Typical Application

The LMH0324 is a low-power SDI equalizer that supports SDI data rates from 125 Mbps to 2.97 Gbps. Figure 16 shows a typical implementation of the LMH0324 as a SDI adaptive cable equalizer. Signal attenuated by a long coax cable is applied to the LMH0324 at the BNC port. Equalized data is output at OUT0± and OUT1± to a downstream video processor.

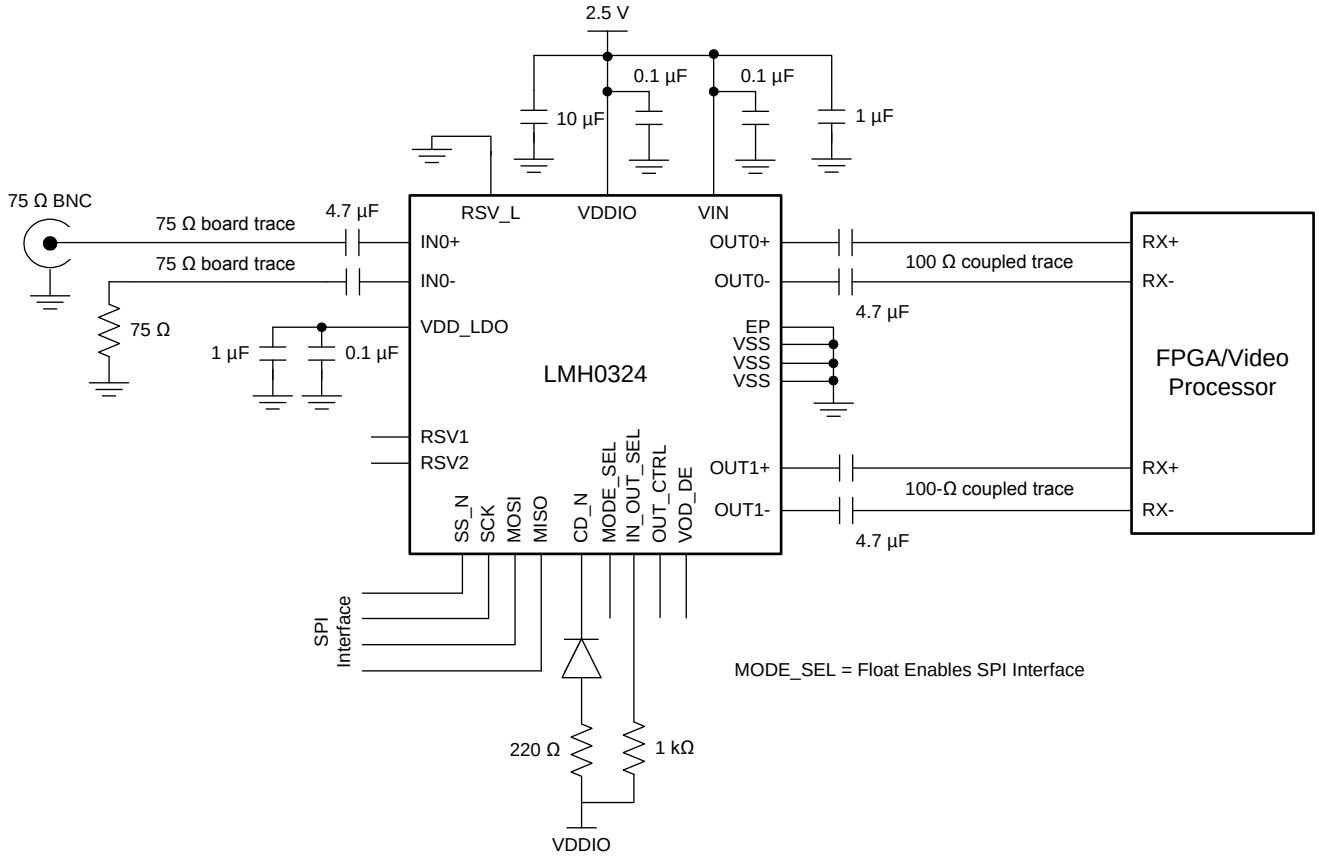


Figure 16. LMH0324 SPI Mode Connection Diagram

Typical Application (continued)

8.2.1 Design Requirements

Table 8. LMH0324 Design Requirements

DESIGN PARAMETER	REQUIREMENTS
Input AC coupling capacitors	AC coupling capacitor at IN0+ should be a 4.7-μF surface mount ceramic capacitor. IN0- should be AC terminated with 4.7 μF and 75 Ω to VSS.
High speed board trace for IN0	IN0+ and IN0- should be routed with uncoupled board traces with 75-Ω characteristic impedance.
BNC connector	High performance BNC capable to support 2.97 Gbps should be used. Footprint of the BNC should be designed to achieve 75-Ω characteristic impedance. For achieving best return loss performance, the BNC should be placed as close to the LMH0324 device as possible
Output AC coupling capacitors	Both OUT0± and OUT1± require AC coupling capacitors. 4.7-μF capacitors are recommended.
High speed board trace for OUT0± and OUT1±	OUT0± and OUT1± should be routed with coupled board traces with 100-Ω differential impedance.
Use of SPI or SMBus interface	Set MODE_SEL to Level-F (pin unconnected) for SPI. Set MODE_SEL to Level-L (connect 1 kΩ to VSS) for SMBus. SMBus is 3.3 V tolerant if VDDIO is powered from 2.5 V.

8.2.2 Detailed Design Procedure

The following general design procedure is recommended:

1. Select a suitable power supply voltage for the LMH0324. It can be powered from a single 2.5 V or 1.8 V supply. See *Power Supply Recommendations* for details.
2. Check that the power supply meets the DC and AC requirements in the *Recommended Operating Conditions*.
3. Select the proper pull-high or pull-low resistors for IN_OUT_SEL and OUT_CTRL for setting the signal path.
4. If -6 dB launch amplitude or other expanded programmable features are needed, select the use of SPI or SMBus by setting the proper pull-high or pull-low resistor for the MODE_SEL pin.
5. Choose a high quality 75-Ω BNC that is capable to support 2.97 Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended BNC footprint for meeting SMPTE return loss requirements.
6. Depending on the length and insertion loss of the output traces for OUT0± and OUT1±, select the proper pull-high or pull-low resistors for VOD_DE to set the output amplitude and de-emphasis settings. Refer to Table 4 for details.
7. Choose a small 0402 surface mount ceramic capacitors for the AC coupling and bypass capacitors.
8. Use proper footprint for BNC and AC coupling capacitors. Anti-pads are commonly used in power and VSS planes under these landing pads to achieve optimum return loss.

8.2.3 Recommended VOD and DE Register Settings

Table 9 shows recommended output amplitude and de-emphasis register settings for most applications.

Table 9. VOD and DE Register Settings

VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp)	DEM (dB)
0	0	410	0
1	1	486	-0.1
2	1	560	-0.1
2	2	560	-0.9
3	1	635	-0.3
3	2	635	-1.3
3	3	635	-2.4
4	1	716	-0.5

Table 9. VOD and DE Register Settings (continued)

VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp)	DEM (dB)
4	2	716	-1.8
4	3	716	-3.0
4	4	716	-4.0
5	1	810	-0.8
5	2	810	-2.4
5	3	810	-3.6
5	4	810	-4.6
5	5	810	-6.1
6	1	880	-1.0
6	2	880	-2.7
6	3	880	-4.0
6	4	880	-5.0
6	5	880	-6.5
7	1	973	-1.2
7	2	973	-3.1
7	3	973	-4.6
7	4	973	-5.7
7	5	973	-7.1

8.2.4 Application Performance Plots

The LMH0324 performance was measured with the test setups shown in Figure 17.

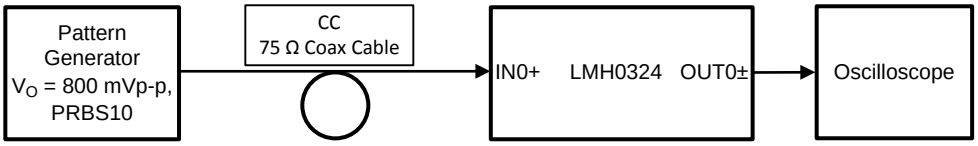


Figure 17. Test Setup for LMH0324 Cable Equalizer (IN0+)

The eye diagrams in this subsection show how the LMH0324 improves overall signal integrity in the data path when different cable lengths are used at IN0+.

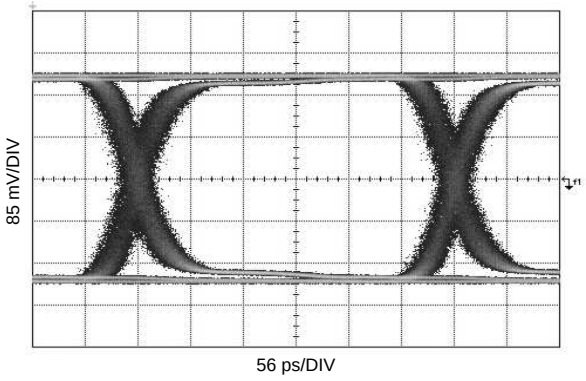


Figure 18. 2.97 Gbps, CC = 150 m Belden 1694A

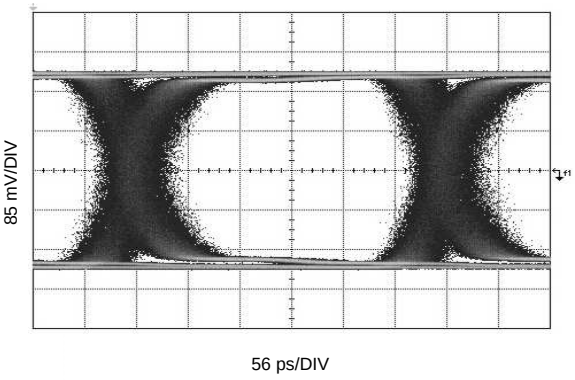


Figure 19. 2.97 Gbps, CC = 200 m Belden 1694A

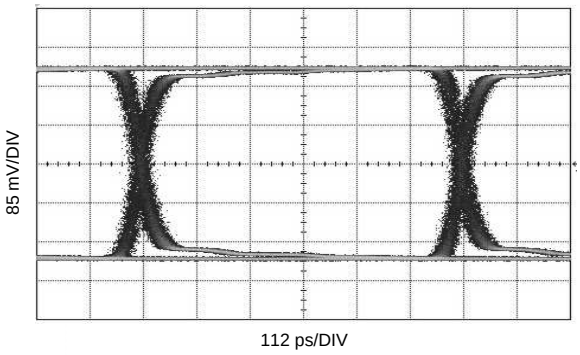


Figure 20. 1.485 Gbps, CC = 200 m Belden 1694A

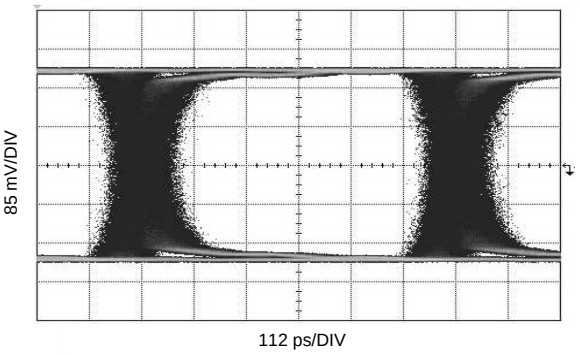


Figure 21. 1.485 Gbps, CC = 280 m Belden 1694A

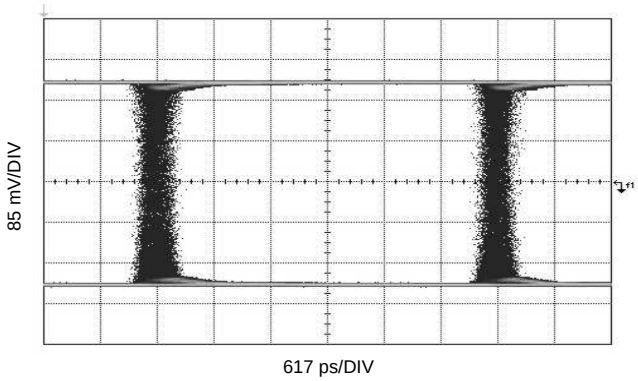


Figure 22. 270 Mbps, CC = 400 m Belden 1694A

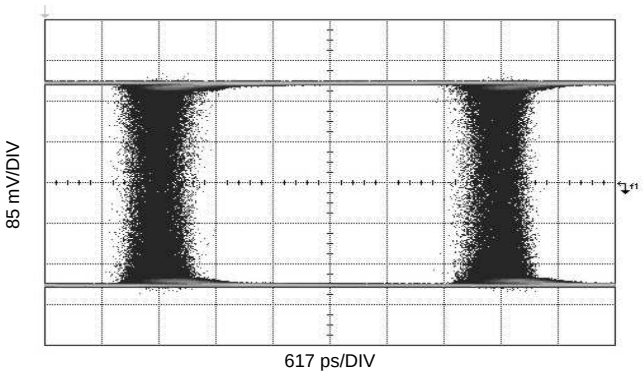


Figure 23. 270 Mbps, CC = 600 m Belden 1694A

9 Power Supply Recommendations

The LMH0324 is designed to provide flexibility in supply rails. There are two ways to power the LMH0324:

- **Single 2.5 V Supply Mode:** This mode offers ease of use and pin compatibility with the LMH1219 (11.88 Gbps Ultra-HD Adaptive Cable Equalizer with Integrated Reclocker). The internal circuitry receives power from the on-chip 1.8 V regulator. In this mode, 2.5 V is applied to VIN, VDDIO, and RSV_L. This mode supports SPI or SMBus serial interface. See Figure 24 for more details.
- **Single 1.8 V Supply Mode:** This mode provides the lowest power consumption. In this mode, 1.8 V is connected to VIN, VDD_LDO and VDDIO. RSV_L is tied to VSS. In this mode, SPI is supported, but SMBus serial interface is not. *In Single 1.8 V Supply Mode, the LMH0324 is not drop-in compatible with the LMH1219.* See Figure 25 for more details.

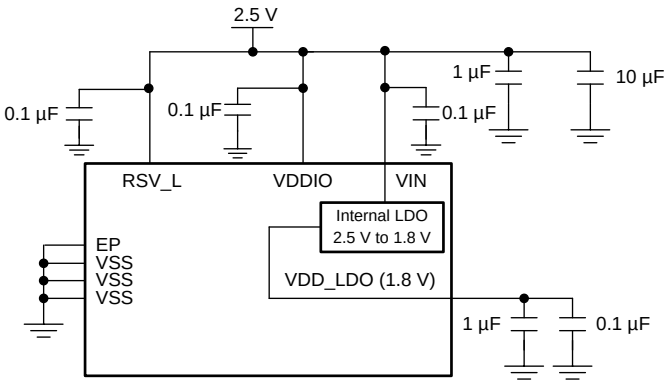


Figure 24. Single 2.5 V Supply Mode - Compatible with LMH1219

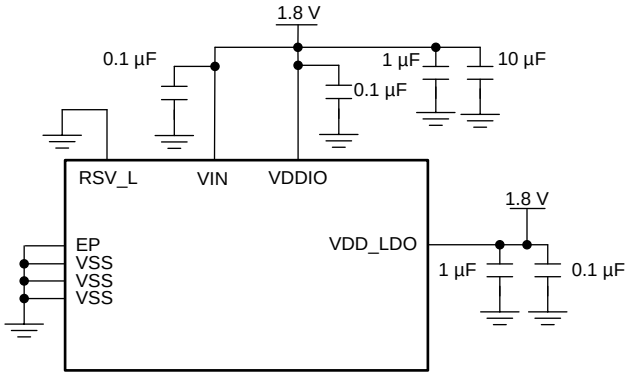


Figure 25. Single 1.8 V Supply Mode - Not Compatible with LMH1219

For power supply de-coupling, 0.1-µF surface-mount ceramic capacitors are recommended to be placed close to each supply pin to VSS. Larger bulk capacitors (for example, 10 µF and 1 µF) are recommended to be placed close to each LMH0324 device. Good supply bypassing requires low inductance capacitors. This can be achieved through an array of multiple small body size surface-mount bypass capacitors in order to keep low supply impedance. Better results can be achieved through the use of a buried capacitor formed by a VDD and VSS plane separated by 2-4 mil dielectric in a printed circuit board.

10 Layout

10.1 Layout Guidelines

The following layout guidelines are recommended for the LMH0324:

1. Choose a suitable board stack-up that supports 75-Ω single-ended trace and 100-Ω differential trace routing on the board's top layer. This is typically done with a Layer 2 ground plane reference for the 100-Ω differential traces and a second ground plane at Layer 3 reference for the 75-Ω single-ended traces.
2. Use single-ended uncoupled trace designed with 75-Ω impedance for signal routing to IN0+ and IN0-. The trace width is typically 8-10 mil reference to a ground plane at Layer 3.
3. Place anti-pad (ground relief) on the power and ground planes directly under the 4.7-µF AC coupling capacitor and IC landing pads to minimize parasitic capacitance. The size of the anti-pad depends on the board stack-up and can be determined by a 3-dimension electromagnetic simulation tool.
4. Use a well-designed BNC footprint to ensure the BNC's signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
5. Keep trace length short between the BNC and IN0+. The trace routing for IN0+ and IN0- should be symmetrical, approximately equal lengths and equal loading.
6. Use coupled differential traces with 100-Ω impedance for signal routing to OUT0± and OUT1±. They are usually 5-8 mil trace width reference to a ground plane at Layer 2.
7. The exposed pad EP of the package should be connected to the ground plane through an array of vias. These vias are solder-masked to avoid solder flow into the plated-through holes during the board manufacturing process.
8. Connect each supply pin (VIN, VDDIO, VDD_LDO, VSS) to the power or ground planes with a short via. The via is usually placed tangent to the supply pins' landing pads with the shortest trace possible.
9. Power supply bypass capacitors should be placed close to the supply pins. They are commonly placed at the bottom layer and share the ground of the EP.

10.2 Layout Example

The following example layout demonstrates the high speed signal trace routing to the LMH0324.

1. BNC footprint and anti-pad: Consult BNC manufacturer for proper size.
2. Anti-pad under passive components.
3. 75-Ω single-ended trace.
4. 100-Ω coupled trace.
5. Vias with solder mask.

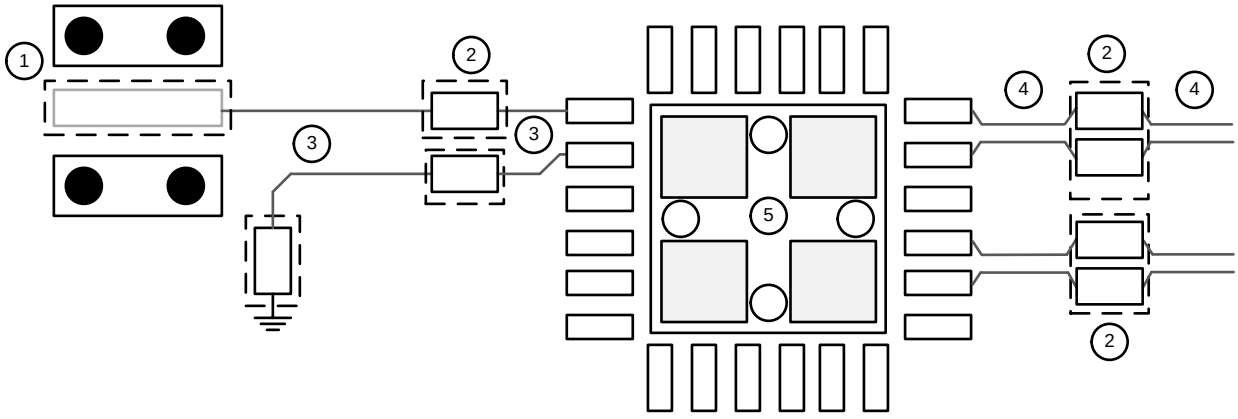


Figure 26. LMH0324 PCB Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH0324RTWR	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L0324A2
LMH0324RTWR.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L0324A2
LMH0324RTWR.B	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L0324A2
LMH0324RTWT	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L0324A2
LMH0324RTWT.A	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L0324A2
LMH0324RTWT.B	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L0324A2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

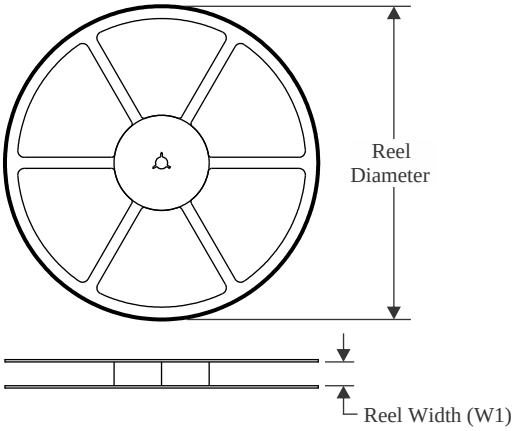
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

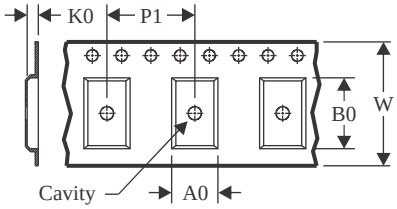
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

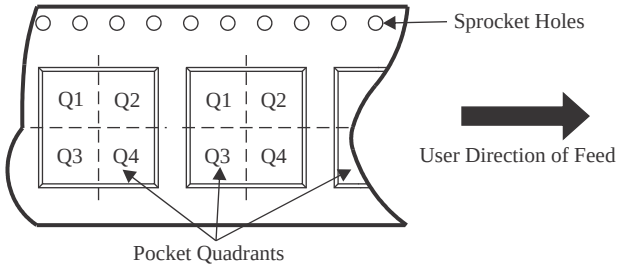


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

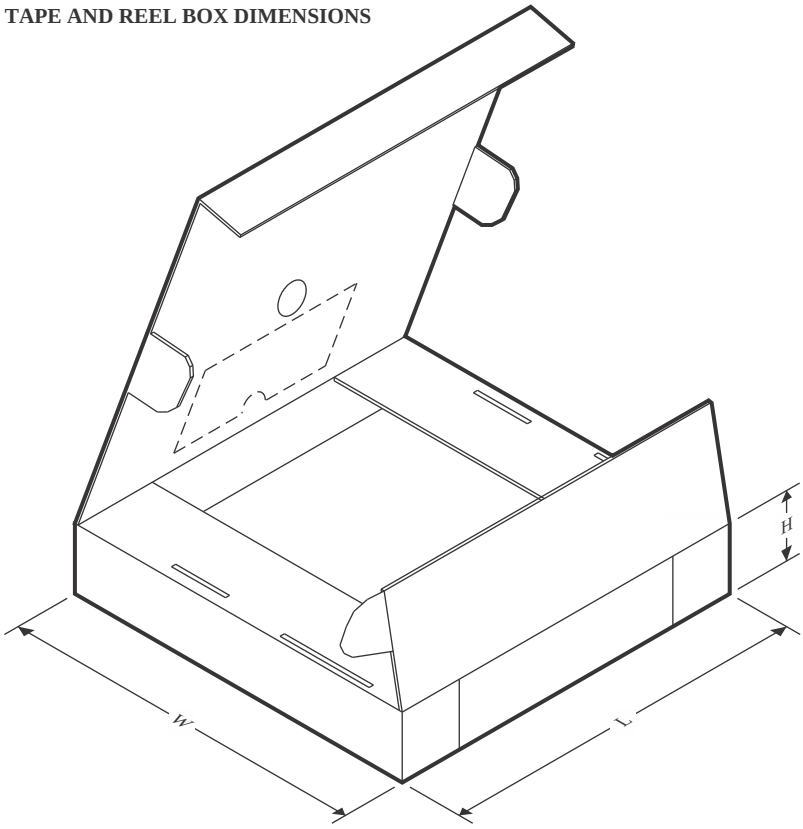
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0324RTWR	WQFN	RTW	24	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0324RTWT	WQFN	RTW	24	250	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

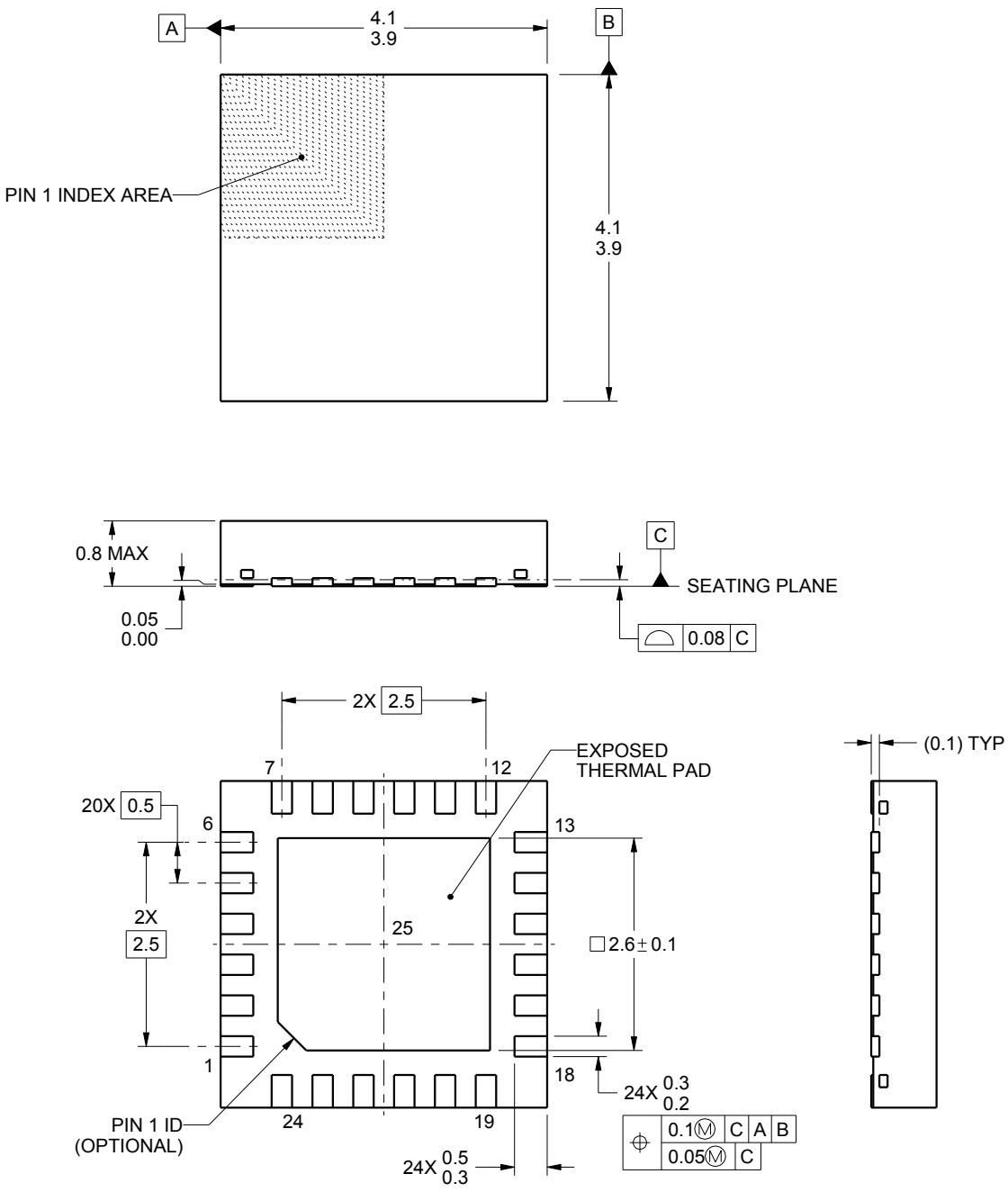
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0324RTWR	WQFN	RTW	24	3000	356.0	356.0	36.0
LMH0324RTWT	WQFN	RTW	24	250	208.0	191.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

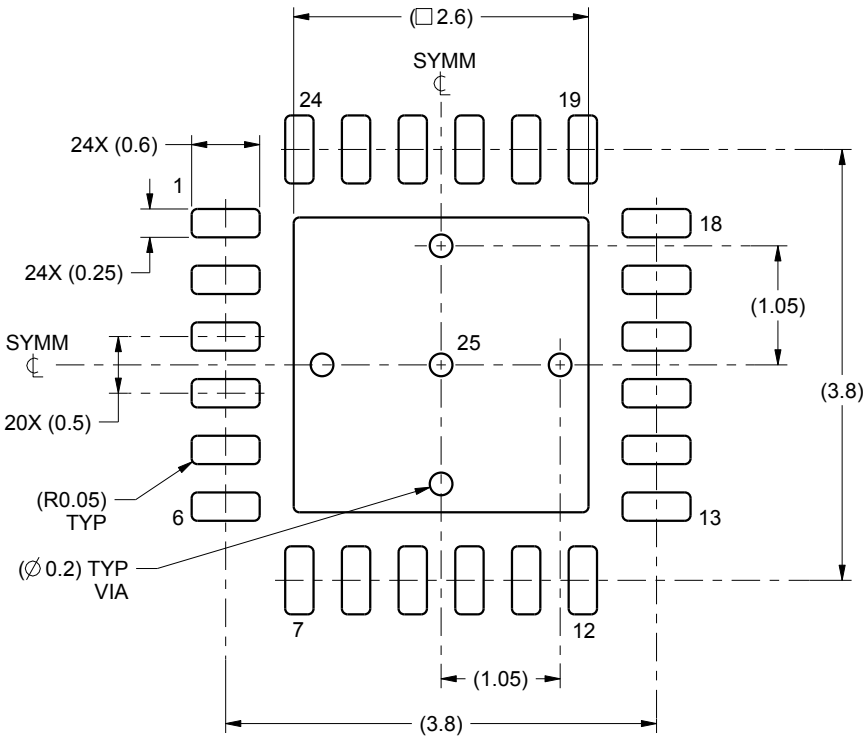
PLASTIC QUAD FLATPACK - NO LEAD



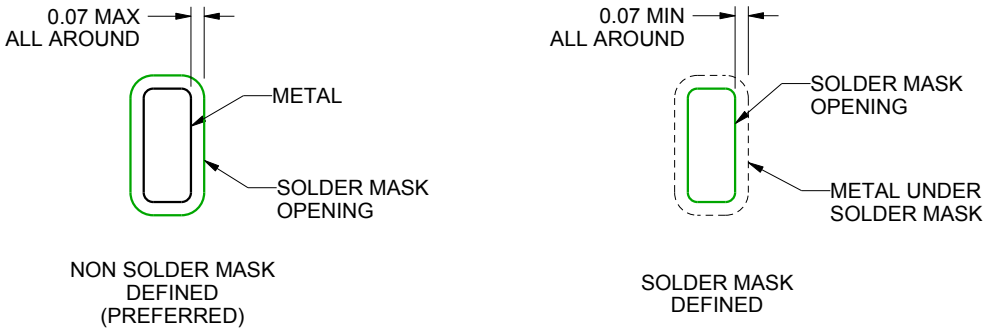
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

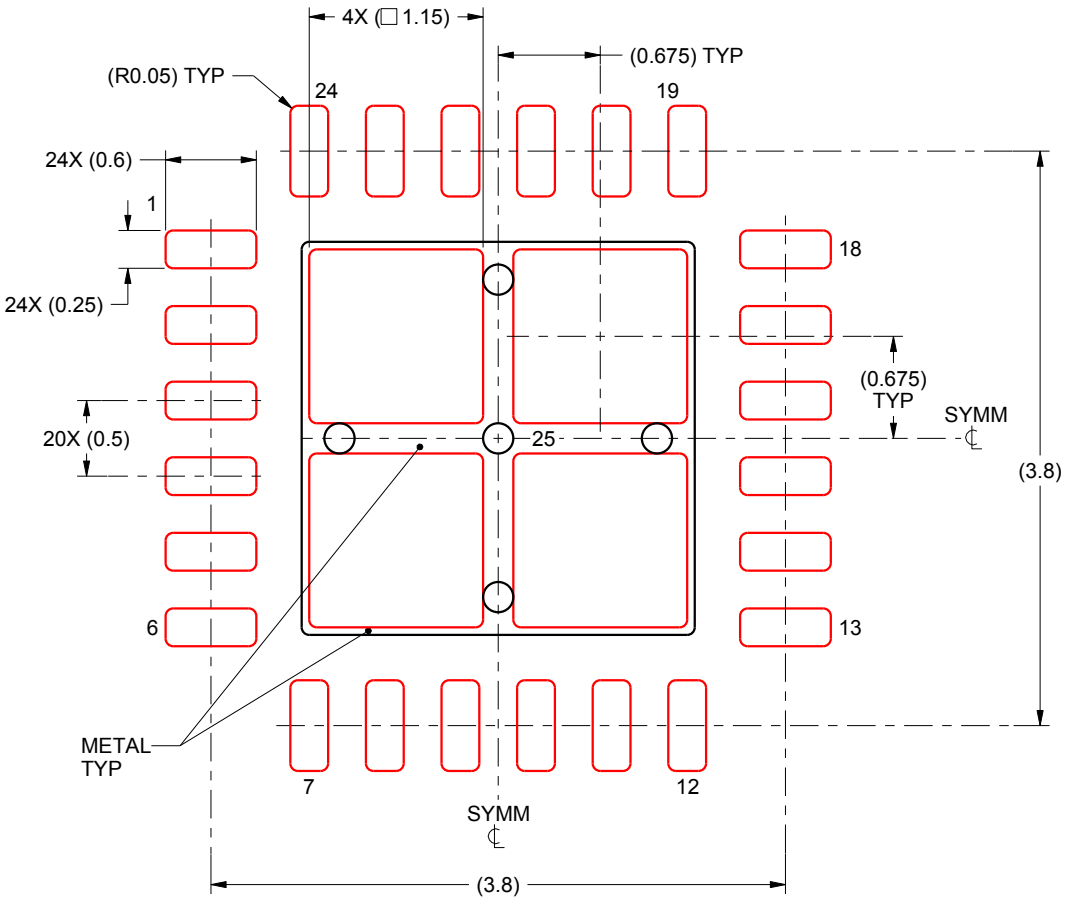


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025