

LMK1D210x Low Additive Jitter LVDS Buffer

1 Features

- High-performance LVDS clock buffer family: up to 2 GHz
 - Dual 1:2 differential buffer
 - Dual 1:4 differential buffer
- Supply voltage: 1.71 V to 3.465 V
- Fail-safe input operation
- Low additive jitter: < max 60 fs RMS in 12-kHz to 20-MHz @ 156.25 MHz
 - Very low phase noise floor: -164 dBc/Hz (typical)
- Very low propagation delay < 575 ps max
- Output skew of 20 ps max
- Universal inputs accept LVDS, LVPECL, LVCMOS, HCSL and CML signal levels.
- LVDS reference voltage, V_{AC_REF} , available for capacitive coupled inputs
- Industrial temperature range: -40°C to 105°C
- Packaged in
 - LMK1D2102: 3-mm x 3-mm, 16-Pin VQFN
 - LMK1D2104: 5-mm x 5-mm, 28-Pin VQFN

2 Applications

- Telecommunications and networking
- Medical imaging
- Test and measurement
- Wireless infrastructure
- Pro audio, video and signage

3 Description

The LMK1D210x clock buffer distributes two clock inputs (IN0 and IN1) to a total of up to 8 pairs of differential LVDS clock outputs (OUT0, OUT7) with minimum skew for clock distribution. Each buffer block consists of one input and up to 4 LVDS outputs. The inputs can either be LVDS, LVPECL, HCSL, CML or LVCMOS.

The LMK1D210x is specifically designed for driving 50-Ω transmission lines. In case of driving the inputs in single-ended mode, the appropriate bias voltage as shown in [Figure 9-6](#) must be applied to the unused negative input pin.

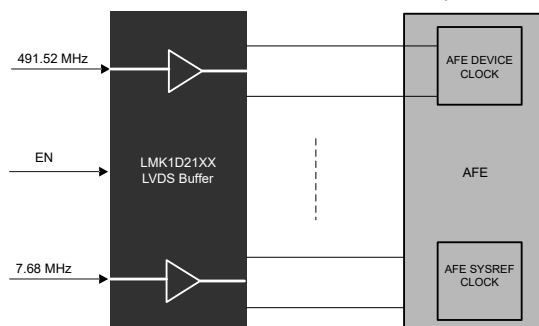
Using the control pin (EN), output banks can either be enabled or disabled. If this pin is left open, two buffers with all outputs are enabled, if switched to a logic "0", both banks with all outputs are disabled (static logic "0"), if switched to a logic "1", one bank and its outputs are disabled while another bank with its outputs are enabled. The part supports a fail-safe function. The device further incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

The device operates in 1.8-V or 2.5-V or 3.3-V supply environment and is characterized from -40°C to 105°C (ambient temperature). The LMK1D210x package variant is shown in the table below:

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE (NOM) ⁽²⁾ |
|-------------|------------------------|-----------------------------------|
| LMK1D2102 | VQFN (16) | 3.00 mm × 3.00 mm |
| LMK1D2104 | VQFN (28) | 5.00 mm × 5.00 mm |

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



Application Example



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (February 2022) to Revision B (June 2023) | Page |
|--|-------------|
| • Changed the <i>Device Information</i> table to <i>Package Information</i> | 1 |
| • Added the <i>Device Comparison</i> table for the LMK1Dxxxx buffer device family..... | 3 |
| • Moved the <i>Power Supply Recommendations</i> and <i>Layout</i> sections to the <i>Application and Implementation</i> section..... | 18 |

| Changes from Revision * (September 2021) to Revision A (February 2022) | Page |
|--|-------------|
| • Added bullet on fail-safe inputs to <i>Features</i> | 1 |
| • Removed the input specifiers on the output pins in the <i>Pin Functions</i> table..... | 4 |
| • Changed <i>Thermal Information</i> table..... | 6 |
| • Added the <i>Fail-Safe Inputs</i> section..... | 12 |

5 Device Comparison

Table 5-1. Device Comparison

| DEVICE | DEVICE TYPE | FEATURES | OUTPUT SWING | PACKAGE | BODY SIZE |
|------------|-------------|--|--------------|-----------|-------------------|
| LMK1D2108 | Dual 1:8 | Global output enable and swing control through pin control | 350 mV | VQFN (48) | 7.00 mm × 7.00 mm |
| | | | 500 mV | | |
| LMK1D2106 | Dual 1:6 | Global output enable and swing control through pin control | 350 mV | VQFN (40) | 6.00 mm × 6.00 mm |
| | | | 500 mV | | |
| LMK1D2104 | Dual 1:4 | Global output enable and swing control through pin control | 350 mV | VQFN (28) | 5.00 mm × 5.00 mm |
| | | | 500 mV | | |
| LMK1D2102 | Dual 1:2 | Global output enable and swing control through pin control | 350 mV | VQFN (16) | 3.00 mm × 3.00 mm |
| | | | 500 mV | | |
| LMK1D1216 | 2:16 | Global output enable control through pin control | 350 mV | VQFN (48) | 7.00 mm × 7.00 mm |
| | | | 500 mV | | |
| LMK1D1212 | 2:12 | Global output enable control through pin control | 350 mV | VQFN (40) | 6.00 mm × 6.00 mm |
| | | | 500 mV | | |
| LMK1D1208P | 2:8 | Individual output enable control through pin control | 350 mV | VQGN (40) | 6.00 mm × 6.00 mm |
| | | | 500 mV | | |
| LMK1D1208I | 2:8 | Individual output enable control through I ² C | 350 mV | VQFN (40) | 6.00 mm × 6.00 mm |
| | | | 500 mV | | |
| LMK1D1208 | 2:8 | Global output enable control through pin control | 350 mV | VQFN (28) | 5.00 mm × 5.00 mm |
| LMK1D1204P | 2:4 | Individual output enable control through pin control | 350 mV | VQGN (28) | 5.00 mm × 5.00 mm |
| LMK1D1204 | 2:4 | Global output enable control through pin control | 350 mV | VQFN (16) | 3.00 mm × 3.00 mm |

6 Pin Configuration and Functions

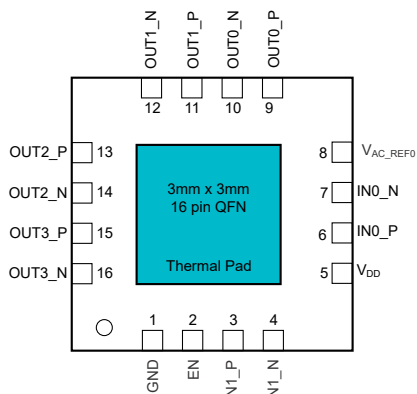


Figure 6-1. LMK1D2102: RGT Package 16-Pin VQFN Top View

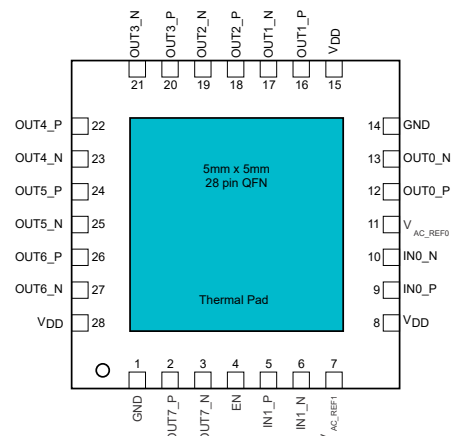


Figure 6-2. LMK1D2104: RHD Package 28-Pin VQFN Top View

Table 6-1. Pin Functions

| PIN | | | TYPE ⁽¹⁾ | DESCRIPTION |
|---|-----------|-----------|---------------------|---|
| NAME | LMK1D2102 | LMK1D2104 | | |
| DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT | | | | |
| IN0_P, IN0_N | 6, 7 | 9, 10 | I | Primary: Differential input pair or single-ended input |
| IN1_P, IN1_N | 3, 4 | 5, 6 | I | Secondary: Differential input pair or single-ended input. |
| | | | | Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N. |
| OUTPUT BANK CONTROL | | | | |
| EN | 2 | 4 | I | Output bank enable/disable with an internal 500-kΩ pullup and 320-kΩ pulldown, selects input port; (See Table 9-1) |
| BIAS VOLTAGE OUTPUT | | | | |
| V _{AC_REF0} , V _{AC_REF1} | 8 | 11, 7 | O | Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-μF capacitor to GND on this pin. |
| DIFFERENTIAL CLOCK OUTPUT | | | | |
| OUT0_P, OUT0_N | 9, 10 | 12, 13 | O | Differential LVDS output pair number 0 |
| OUT1_P, OUT1_N | 11, 12 | 16, 17 | O | Differential LVDS output pair number 1 |
| OUT2_P, OUT2_N | 13, 14 | 18, 19 | O | Differential LVDS output pair number 2 |
| OUT3_P, OUT3_N | 15, 16 | 20, 21 | O | Differential LVDS output pair number 3 |
| OUT4_P, OUT4_N | | 22, 23 | O | Differential LVDS output pair number 4 |
| OUT5_P, OUT5_N | | 24, 25 | O | Differential LVDS output pair number 5 |
| OUT6_P, OUT6_N | | 26, 27 | O | Differential LVDS output pair number 6 |
| OUT7_P, OUT7_N | | 2, 3 | O | Differential LVDS output pair number 7 |
| SUPPLY VOLTAGE | | | | |
| V _{DD} | 5 | 8, 15, 28 | P | Device Power Supply (1.8V or 2.5V or 3.3V) |
| GROUND | | | | |
| GND | 1 | 1, 14 | G | Ground |
| DAP | DAP | DAP | G | Die Attach Pad. Connect to the PCB ground plane for heat dissipation. |

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|------------------------------------|------|-----------------------|------|
| V _{DD} | Supply voltage | −0.3 | 3.6 | V |
| V _{IN} | Input voltage | −0.3 | 3.6 | V |
| V _O | Output voltage | −0.3 | V _{DD} + 0.3 | V |
| I _{IN} | Input current | −20 | 20 | mA |
| I _O | Continuous output current | −50 | 50 | mA |
| T _J | Junction temperature | | 135 | °C |
| T _{stg} | Storage temperature ⁽²⁾ | −65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Device unpowered

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾ | ±3000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾ | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|--|-------|-----|-------|------|
| V _{DD} | Core supply voltage | 3.3-V supply | 3.135 | 3.3 | 3.465 | V |
| | | 2.5-V supply | 2.375 | 2.5 | 2.625 | |
| | | 1.8-V supply | 1.71 | 1.8 | 1.89 | |
| Supply Ramp | Supply voltage ramp | Requires monotonic ramp (10-90% of V _{DD}) | 0.1 | | 20 | ms |
| T _A | Operating free-air temperature | | −40 | | 105 | °C |
| T _J | Operating junction temperature | | −40 | | 135 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LMK1D2102 | LMK1D2104 | UNIT |
|-------------------------------|--|-----------|-----------|------|
| | | VQFN | VQFN | |
| | | 16 PINS | 28 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 48.7 | 38.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.4 | 32.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 23.6 | 18.7 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 1.6 | 1 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 23.6 | 18.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 8.6 | 8.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

$V_{DD} = 1.8 \text{ V} \pm 5\%$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$. Typical values are at $V_{DD} = 1.8 \text{ V}$, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|---|---------------------|---------------------|---------------------|---------------|
| POWER SUPPLY CHARACTERISTICS | | | | | | |
| I_{DD_STAT} | LMK1D2102 | All-outputs enabled and unterminated, $f = 0 \text{ Hz}$ | | 50 | | mA |
| I_{DD_STAT} | LMK1D2104 | All-outputs enabled and unterminated, $f = 0 \text{ Hz}$ | | 55 | | mA |
| I_{DD_100M} | LMK1D2102 | All-outputs enabled, $R_L = 100 \Omega$, $f = 100 \text{ MHz}$ | | 70 | 80 | mA |
| I_{DD_100M} | LMK1D2104 | All-outputs enabled, $R_L = 100 \Omega$, $f = 100 \text{ MHz}$ | | 84 | 110 | mA |
| OUTPUT BANK CONTROL (EN) INPUT CHARACTERISTICS (Applies to $V_{DD} = 1.8 \text{ V} \pm 5\%$, $2.5 \text{ V} \pm 5\%$ and $3.3 \text{ V} \pm 5\%$) | | | | | | |
| V_{dI3} | 3-state input | Open | | $0.4 \times V_{CC}$ | | V |
| V_{IH} | Input high voltage | Minimum input voltage for a logical "1" state | $0.7 \times V_{CC}$ | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input low voltage | Maximum input voltage for a logical "0" state | -0.3 | | $0.3 \times V_{CC}$ | V |
| I_{IH} | Input high current | V_{DD} can be 1.8V/2.5V/3.3V with $V_{IH} = V_{DD}$ | | | 30 | μA |
| I_{IL} | Input low current | V_{DD} can be 1.8V/2.5V/3.3V with $V_{IH} = V_{DD}$ | -30 | | | μA |
| $R_{pull-up(EN)}$ | Input pullup resistor | | | 500 | | k Ω |
| $R_{pull-down(EN)}$ | Input pulldown resistor | | | 320 | | k Ω |
| SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to $V_{DD} = 1.8 \text{ V} \pm 5\%$, $2.5 \text{ V} \pm 5\%$ and $3.3 \text{ V} \pm 5\%$) | | | | | | |
| f_{IN} | Input frequency | Clock input | DC | | 250 | MHz |
| V_{IN_S-E} | Single-ended Input Voltage Swing | Assumes a square wave input with two levels | 0.4 | | 3.465 | V |
| dV_{IN}/dt | Input Slew Rate (20% to 80% of the amplitude) | | 0.05 | | | V/ns |
| I_{IH} | Input high current | $V_{DD} = 3.465 \text{ V}$, $V_{IH} = 3.465 \text{ V}$ | | | 50 | μA |
| I_{IL} | Input low current | $V_{DD} = 3.465 \text{ V}$, $V_{IL} = 0 \text{ V}$ | -30 | | | μA |
| C_{IN_SE} | Input capacitance | at 25°C | | 3.5 | | pF |
| DIFFERENTIAL CLOCK INPUT (Applies to $V_{DD} = 1.8 \text{ V} \pm 5\%$, $2.5 \text{ V} \pm 5\%$ and $3.3 \text{ V} \pm 5\%$) | | | | | | |
| f_{IN} | Input frequency | Clock input | | | 2 | GHz |
| $V_{IN_DIFF(p-p)}$ | Differential input voltage peak-to-peak $\{2 \times (V_{INP} - V_{INN})\}$ | $V_{ICM} = 1 \text{ V}$ ($V_{DD} = 1.8 \text{ V}$) | 0.3 | | 2.4 | V_{PP} |
| | | $V_{ICM} = 1.25 \text{ V}$ ($V_{DD} = 2.5 \text{ V}/3.3 \text{ V}$) | 0.3 | | 2.4 | |

$V_{DD} = 1.8 \text{ V} \pm 5\%$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$. Typical values are at $V_{DD} = 1.8 \text{ V}$, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|--|--|------|------|-------|------------------|
| V_{ICM} | Input common mode voltage | $V_{IN,DIFF(P-P)} > 0.4 \text{ V}$ ($V_{DD} = 1.8 \text{ V}/2.5/3.3 \text{ V}$) | 0.25 | | 2.3 | V |
| I_{IH} | Input high current | $V_{DD} = 3.465 \text{ V}$, $V_{INP} = 2.4 \text{ V}$, $V_{INN} = 1.2 \text{ V}$ | | | 30 | μA |
| I_{IL} | Input low current | $V_{DD} = 3.465 \text{ V}$, $V_{INP} = 0 \text{ V}$, $V_{INN} = 1.2 \text{ V}$ | –30 | | | μA |
| C_{IN_S-E} | Input capacitance (Single-ended) | at 25°C | | 3.5 | | pF |
| LVDS DC OUTPUT CHARACTERISTICS | | | | | | |
| $ V_{OD} $ | Differential output voltage magnitude $V_{OUTP} - V_{OUTN} $ | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$ | 250 | 350 | 450 | mV |
| ΔV_{OD} | Change in differential output voltage magnitude. Per output, defined as the difference between VOD in logic hi/lo states. | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$ | –15 | | 15 | mV |
| $V_{OC(SS)}$ | Steady-state common mode output voltage | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$ ($V_{DD} = 1.8 \text{ V}$) | 1 | | 1.2 | V |
| | | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$ ($V_{DD} = 2.5 \text{ V}/3.3 \text{ V}$) | 1.1 | | 1.375 | |
| $\Delta V_{OC(SS)}$ | Change in steady-state common mode output voltage. Per output, defined as the difference in VOC in logic hi/lo states. | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$ | –15 | | 15 | mV |
| LVDS AC OUTPUT CHARACTERISTICS | | | | | | |
| V_{ring} | Output overshoot and undershoot | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$, $f_{OUT} = 491.52 \text{ MHz}$ | –0.1 | | 0.1 | V_{OD} |
| V_{OS} | Output AC common mode | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$ | | 50 | 100 | mV _{pp} |
| I_{OS} | Short-circuit output current (differential) | $V_{OUTP} = V_{OUTN}$ | –12 | | 12 | mA |
| $I_{OS(cm)}$ | Short-circuit output current (common-mode) | $V_{OUTP} = V_{OUTN} = 0$ | –24 | | 24 | mA |
| t_{PD} | Propagation delay | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$, $R_{LOAD} = 100 \Omega$ ⁽²⁾ | 0.3 | | 0.575 | ns |
| $t_{SK, O}$ | Output skew | Skew between outputs with the same load conditions (4 and 8 channel) ⁽³⁾ | | | 20 | ps |
| $t_{SK, b}$ | Output bank skew | Skew between the outputs within the same bank (2102/2104) ⁽⁴⁾ | | | 15 | ps |
| $t_{SK, PP}$ | Part-to-part skew | Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading. | | | 250 | ps |
| $t_{SK, P}$ | Pulse skew | 50% duty cycle input, crossing point-to-crossing-point distortion ⁽⁴⁾ | –20 | | 20 | ps |
| $t_{RJIT(ADD)}$ | Random additive Jitter (rms) | $f_{IN} = 156.25 \text{ MHz}$ with 50% duty-cycle, Input slew rate = 1.5 V/ns , Integration range = $12 \text{ kHz} - 20 \text{ MHz}$, with output load $R_{LOAD} = 100 \Omega$ | | 50 | 60 | fs, RMS |
| Phase noise | Phase Noise for a carrier frequency of 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5 V/ns with output load $R_{LOAD} = 100 \Omega$ | $PN_{1\text{kHz}}$ | | –143 | | dBc/Hz |
| | | $PN_{10\text{kHz}}$ | | –152 | | |
| | | $PN_{100\text{kHz}}$ | | –157 | | |
| | | $PN_{1\text{MHz}}$ | | –160 | | |
| | | PN_{floor} | | –164 | | |

$V_{DD} = 1.8 \text{ V} \pm 5\%$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$. Typical values are at $V_{DD} = 1.8 \text{ V}$, 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-----|------|-------|------|
| MUX_{ISO} | Mux Isolation | $f_{\text{IN}} = 156.25 \text{ MHz}$. The difference in power level at f_{IN} when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active. | | 80 | | dB |
| SPUR | Spurious suppression between dual banks | Differential inputs with $F_{\text{IN}0} = 491.52 \text{ MHz}$, $F_{\text{IN}1} = 61.44 \text{ MHz}$; Measured between neighboring outputs | | –60 | | dB |
| | | Different inputs with $F_{\text{IN}0} = 491.52 \text{ MHz}$, $F_{\text{IN}1} = 15.36 \text{ MHz}$; Measured between neighboring outputs | | –70 | | |
| ODC | Output duty cycle | With 50% duty cycle input | 45 | | 55 | % |
| t_R/t_F | Output rise and fall time | 20% to 80% with $R_{\text{LOAD}} = 100 \Omega$ | | | 300 | ps |
| $V_{\text{AC_REF}}$ | Reference output voltage | $V_{DD} = 2.5 \text{ V}$, $I_{\text{LOAD}} = 100 \mu\text{A}$ | 0.9 | 1.25 | 1.375 | V |
| POWER SUPPLY NOISE REJECTION (PSNR) $V_{DD} = 2.5 \text{ V} / 3.3 \text{ V}$ | | | | | | |
| PSNR | Power Supply Noise Rejection ($f_{\text{carrier}} = 156.25 \text{ MHz}$) | 10 kHz, 100 mVpp ripple injected on V_{DD} | | –70 | | dBc |
| | | 1 MHz, 100 mVpp ripple injected on V_{DD} | | –50 | | |

- (1) Measured between single-ended/differential input crossing point to the differential output crossing point.
- (2) For the dual bank devices, the inputs are phase aligned and have 50% duty cycle.
- (3) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

7.6 Typical Characteristics

The [Figure 7-1](#) captures the variation of the LMK1D2104 current consumption with input frequency and supply voltage. The LMK1D2102 follows a similar trend. [Figure 7-2](#) shows the variation of the differential output voltage (VOD) swept across frequency. This result is applicable to LMK1D2102 as well.

It is important to note that [Figure 7-1](#) and [Figure 7-2](#) serve as a guidance to the users on what to expect for the range of operating frequency supported by LMK1D210x. It is crucial to note that these graphs were plotted for a limited number of frequencies and load conditions which may not represent the customer system.

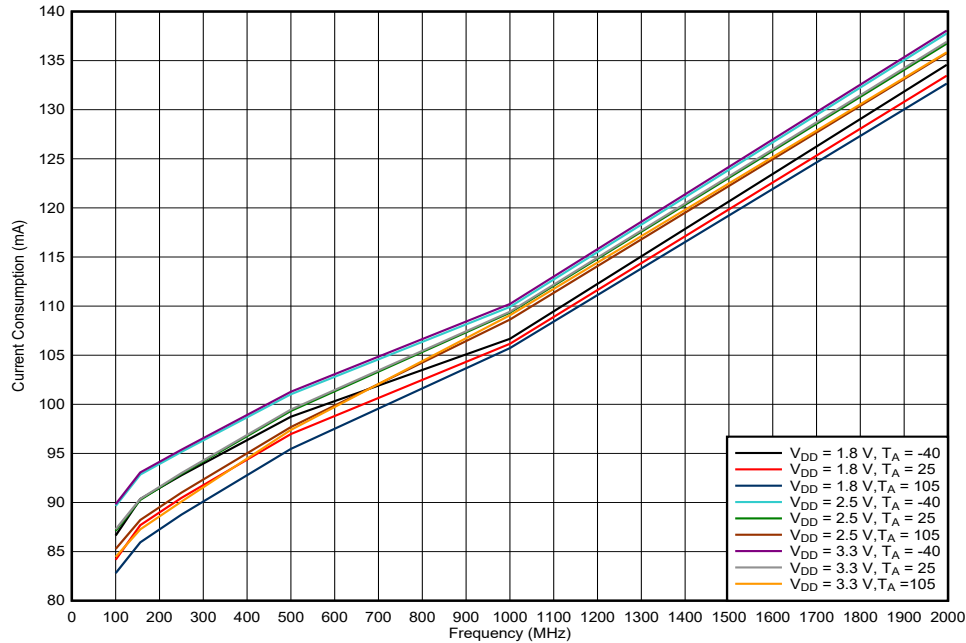


Figure 7-1. LMK1D2104 Current Consumption vs. Frequency

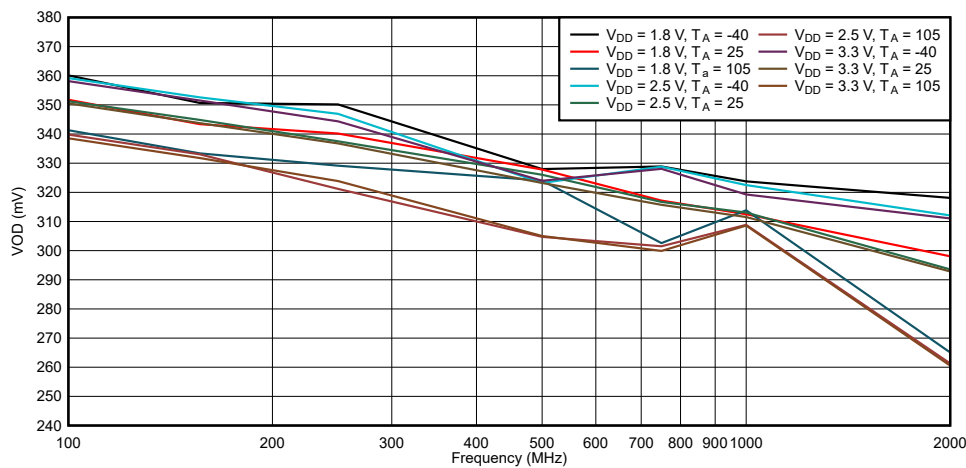


Figure 7-2. LMK1D2104 VOD vs. Frequency

8 Parameter Measurement Information

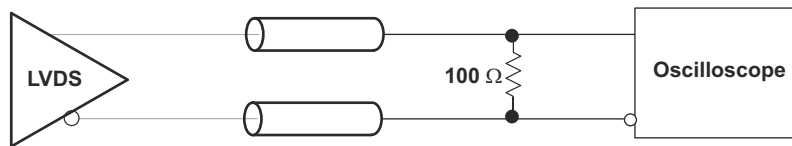


Figure 8-1. LVDS Output DC Configuration During Device Test

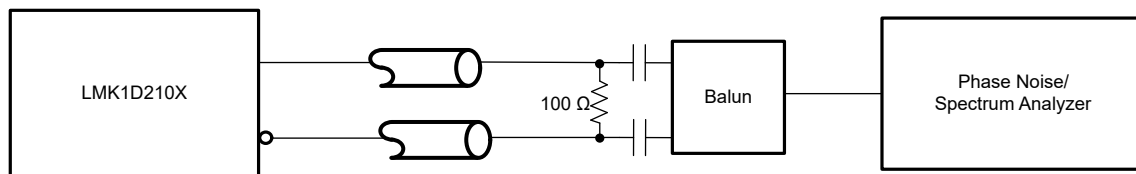


Figure 8-2. LVDS Output AC Configuration During Device Test

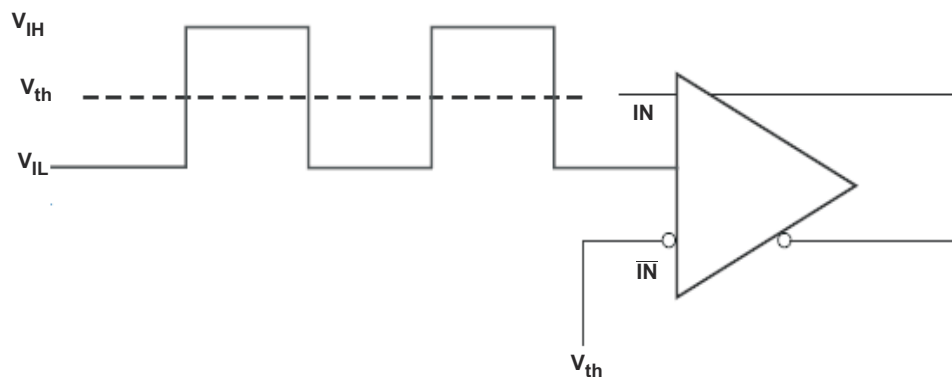


Figure 8-3. DC-Coupled LVCMOS Input During Device Test

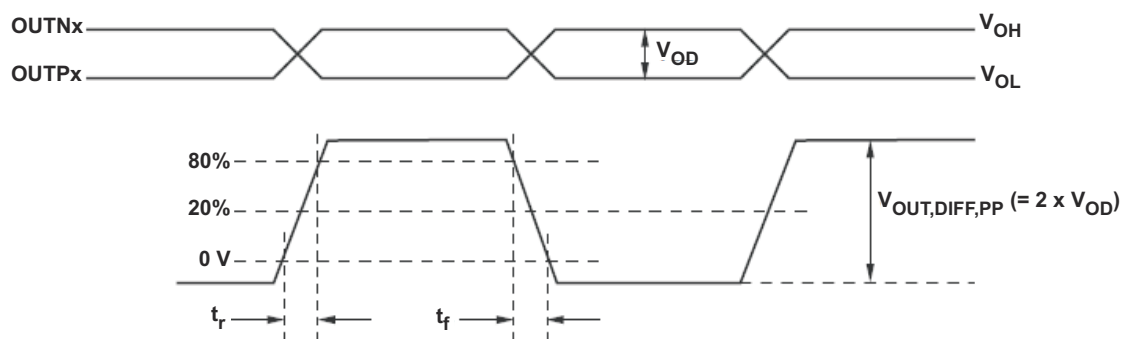
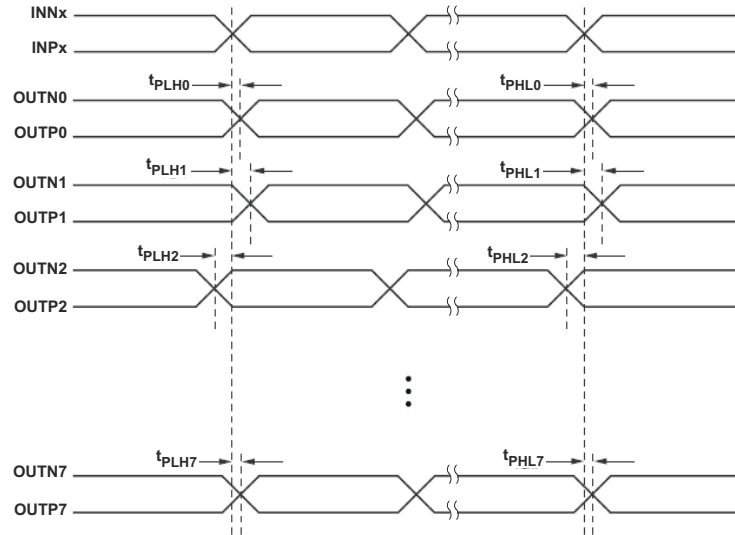


Figure 8-4. Output Voltage and Rise/Fall Time



- A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLH_n} or the difference between the fastest and the slowest t_{PHL_n} (n = 0, 1, 2, ..7)
- B. Part to part skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLH_n} or the difference between the fastest and the slowest t_{PHL_n} across multiple devices (n = 0, 1, 2, ..7)

Figure 8-5. Output Skew and Part-to-Part Skew

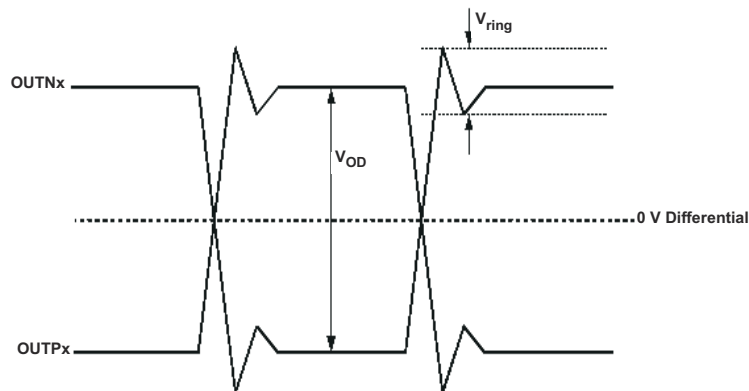


Figure 8-6. Output Overshoot and Undershoot

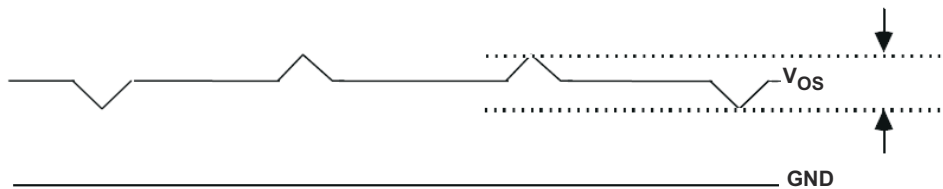


Figure 8-7. Output AC Common Mode

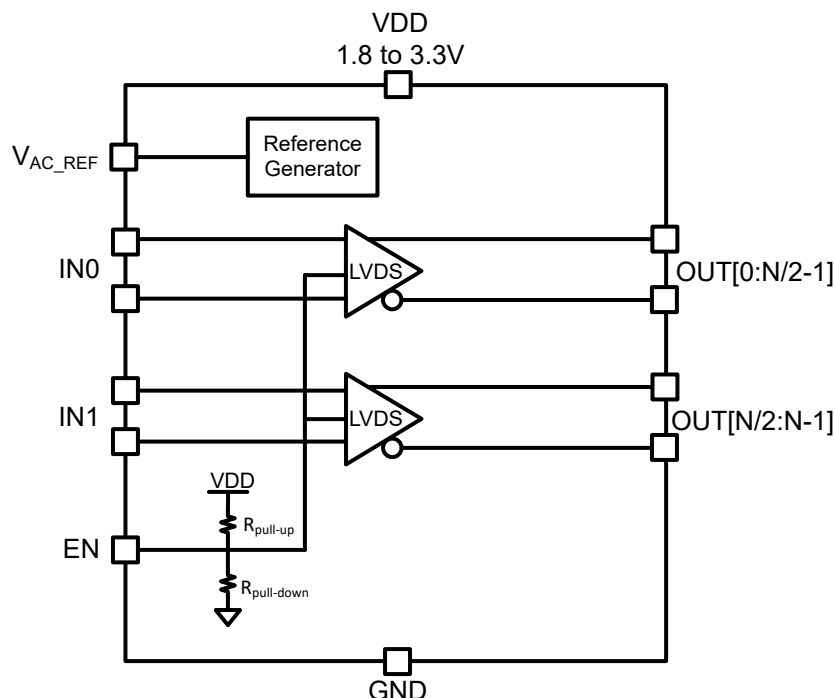
9 Detailed Description

9.1 Overview

The LMK1D210x LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D210x, AC-coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

9.2 Functional Block Diagram



9.3 Feature Description

The LMK1D210x is a low additive jitter LVDS fan-out buffer that can generate up to four copies of a single input which can be either LVPECL, LVDS, or LVCMOS on each of its banks. Since the device has two banks, this translates to a total of eight pairs of outputs (LMK1D2104). The reference clock frequencies can go up to 2 GHz.

Apart from providing a very low additive jitter and low output skew, the LMK1D210x has a control pin (EN), which controls the enabling/disabling of the output banks.

9.3.1 Fail-Safe Inputs

The LMK1D210x family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to [Section 7.1](#) for more information on the maximum input supported by the device. The device also incorporates an input hysteresis that prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

9.4 Device Functional Modes

The output banks of the LMK1D210x can be selected through the control pin (see [Table 9-1](#)). Unused inputs and outputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the LMK1D210x to provide greater system flexibility.

Table 9-1. Output Control Table

| EN | CLOCK OUTPUTS |
|------|--|
| 0 | All outputs disabled (static "0") |
| 1 | OUT0, OUT1... OUT[(N/2)-1] enabled and OUT[N/2]...OUT[-1] disabled. Example: LMK1D2102 (OUT0, OUT1 enabled, OUT2, OUT3 disabled) |
| Open | All outputs enabled |

9.4.1 LVDS Output Termination

TI recommends unused outputs to be terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

The LMK1D210x can be connected to LVDS receiver inputs with DC- and AC-coupling as shown in Figure 9-1 and Figure 9-2 (respectively).

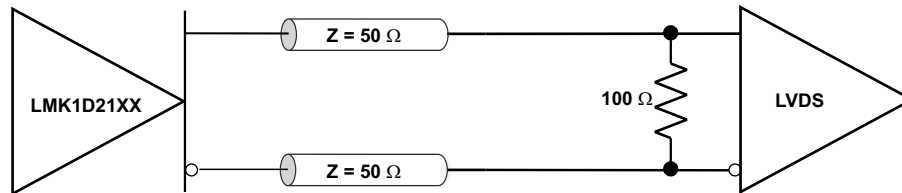


Figure 9-1. Output DC Termination

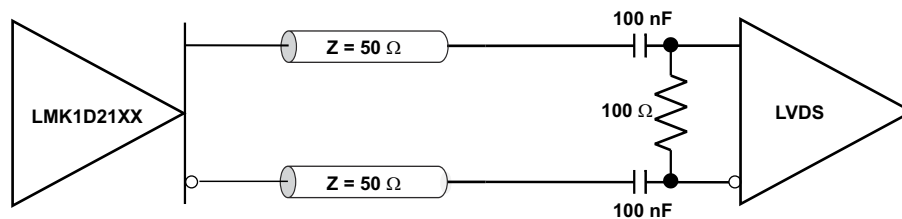


Figure 9-2. Output AC Termination (With the Receiver Internally Biased)

9.4.2 Input Termination

The LMK1D210x inputs can be interfaced with LVDS, LVPECL, HCSL or LVCMOS drivers.

LVDS drivers can be connected to LMK1D210x inputs with DC- and AC-coupling as shown Figure 9-3 and Figure 9-4 (respectively).

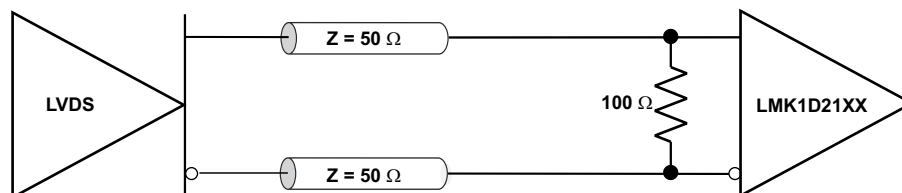


Figure 9-3. LVDS Clock Driver Connected to LMK1D210x Input (DC-Coupled)

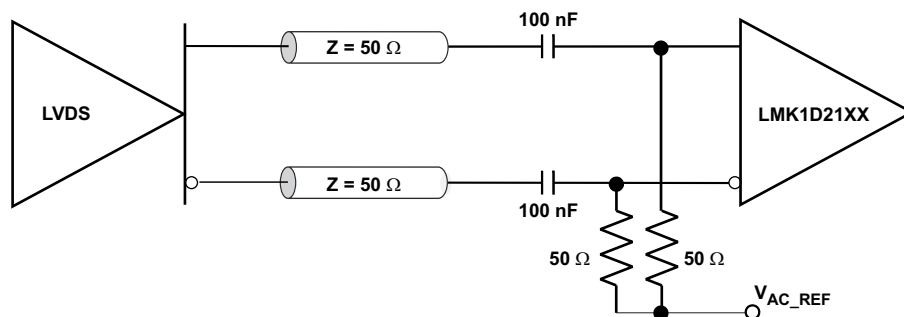


Figure 9-4. LVDS Clock Driver Connected to LMK1D210x Input (AC-Coupled)

Figure 9-5 shows how to connect LVPECL inputs to the LMK1D210x. The series resistors are required to reduce the LVPECL signal swing if the signal swing is $>1.6 V_{PP}$.

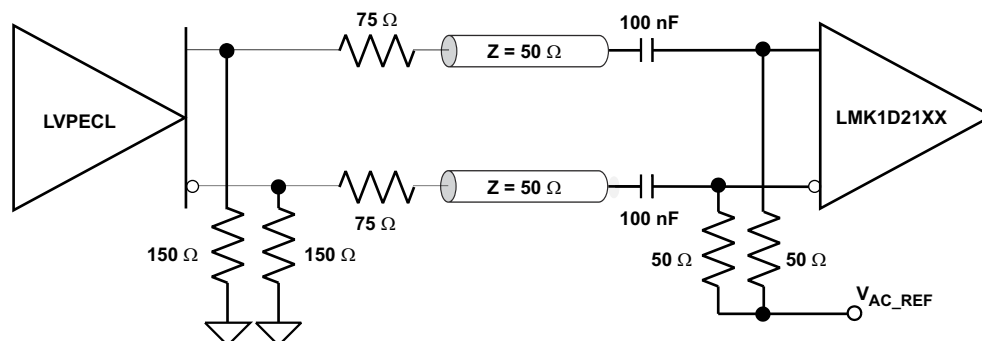


Figure 9-5. LVPECL Clock Driver Connected to LMK1D210x Input

Figure 9-6 illustrates how to couple a LVCMOS clock input to the LMK1D210x directly.

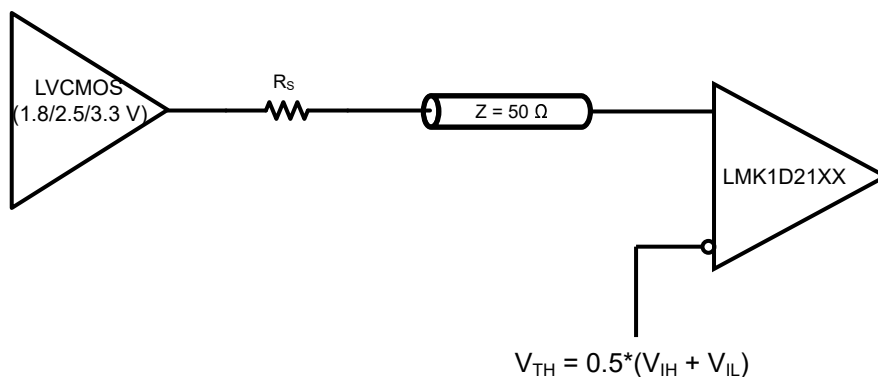


Figure 9-6. 1.8-V/2.5-V/3.3-V LVCMOS Clock Driver Connected to LMK1D210x Input

Unused inputs can be left floating thus reducing the need for additional components.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMK1D210x is a low additive jitter universal to LVDS fan-out buffer with dual inputs which fan-out to dual outputs banks. Each input can fan-out to a maximum of four outputs (LMK1D2104). The small package, 1.8 V power supply operation, low output skew, and low additive jitter makes this device suitable for applications that require high performance clock distribution as well as for low power and space constraint applications.

10.2 Typical Application

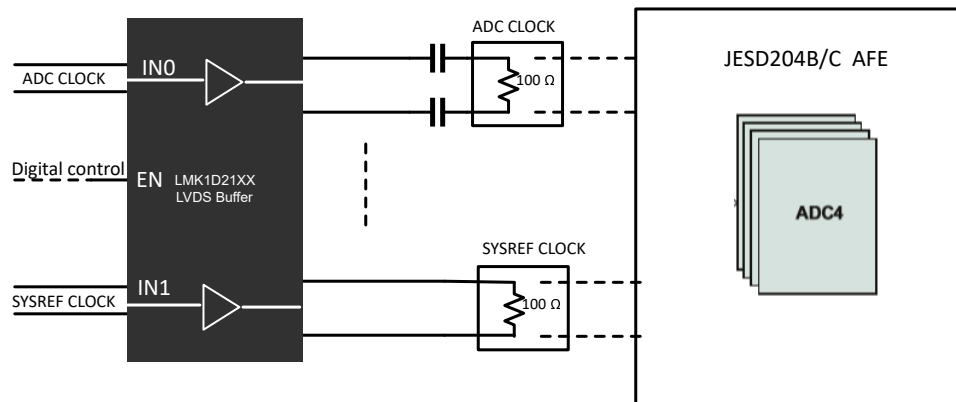


Figure 10-1. Fan-Out Buffer for ADC Device clock and SYSREF distribution

10.2.1 Design Requirements

The LMK1D210x shown in [Figure 10-1](#) is configured to fan-out an ADC clock on the first output bank and SYSREF clock on the second output bank for a system utilizing the JESD204B/C ADC. The low output to output skew, very low additive jitter and superior spurious suppression between dual banks makes the LMK1D210x a simple, robust and low-cost solution for distributing various clocks to JESD204B/C AFE systems. The configuration example can drive up to 4 ADC clocks and 4 SYSREF clocks for a JESD204B/C receiver with the following properties:

- The ADC clock receiver module is typically AC coupled with an LVDS driver such as the LMK1D210x due to differences in common-mode between the driver and receiver. Depending on the receiver, there may be an option for internal 100-Ω differential termination in which case an external termination would not be required for the LMK1D210x.
- The SYSREF clock receiver module is typically DC coupled provided the common-mode voltage of the LMK1D210x outputs match with the receiver. An external termination may not be needed in case of an internal termination in the receiver.
- Unused outputs of the LMK1D device are terminated differentially with a 100-Ω resistor for optimum performance.

10.2.2 Detailed Design Procedure

See [Section 9.4.2](#) for proper input terminations, dependent on single-ended or differential inputs.

See [Section 9.4.1](#) for output termination schemes depending on the receiver application.

TI recommends unused outputs to be terminated differentially with a 100- Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

In the application example described in the previous section [Figure 10-1](#), the ADC clock and SYSREF clocks require different output interfacing schemes. Power supply filtering and bypassing is critical for low-noise applications.

In case of common-mode mismatch between the output voltage of the LMK1D210x and the receiver, one can use AC coupling to get around this, however, in certain applications, it might not be possible to AC couple the LMK1D210x outputs to the receiver due to the settling time associated with this AC coupling network (High-pass filter) which can result in non-deterministic behavior during the initial transients. For such applications, it becomes necessary to DC couple the outputs and thus requires a scheme which can overcome the inherent mismatch between the common-mode of the driver and receiver.

The application report [Interfacing LVDS Driver With a Sub-LVDS Receiver](#) discusses how to interface between a LVDS driver and sub-LVDS receiver. Same concept can be applied to interface the LMK1D210x outputs to a receiver which has lower common-mode.

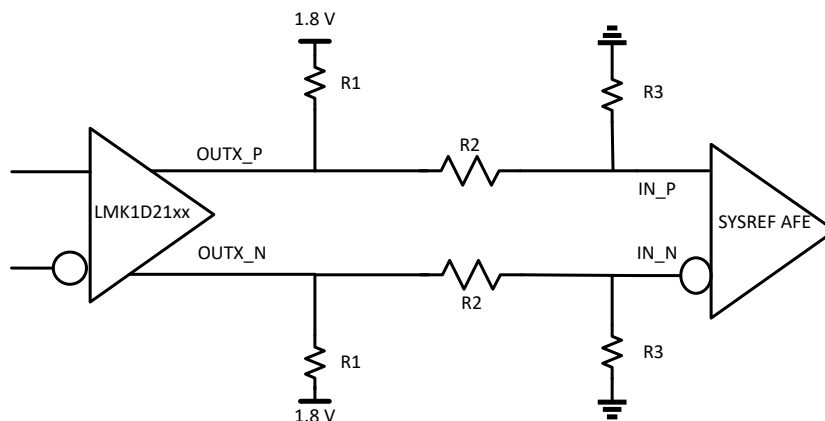
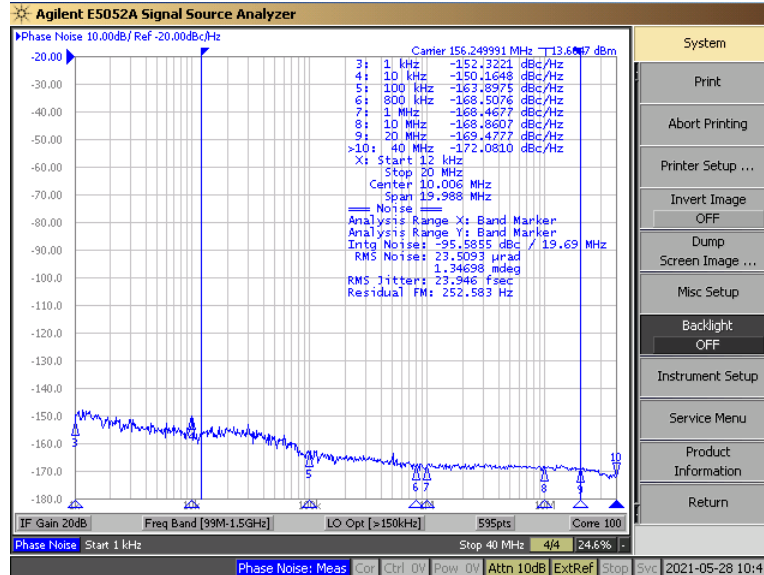


Figure 10-2. Schematic for DC coupling LMK1D21xx with lower common-mode receiver

The [Figure 10-2](#) illustrates the resistor divider network for stepping down the common mode as explained in the above application report. The resistors R1, R2 and R3 are chosen according to the input common mode requirements of the receiver. As highlighted before, user needs to make sure that the reduced swing is able to meet the requirements of the receiver.

10.2.3 Application Curves

The LMK1D2104's low additive noise is shown below. The low noise 156.25-MHz source with 24-fs RMS jitter shown in Figure 10-3 drives the LMK1D2104, resulting in 46.4-fs RMS when integrated from 12 kHz to 20 MHz (Figure 10-4). The resultant additive jitter is a low 39.7-fs RMS for this configuration. Note that this result applies to the LMK1D2102 device as well.



A. Reference signal is low-noise Rohde and Schwarz SMA100B

Figure 10-3. LMK1D2104 Reference Phase Noise, 156.25 MHz, 24-fs RMS (12 kHz to 20 MHz)

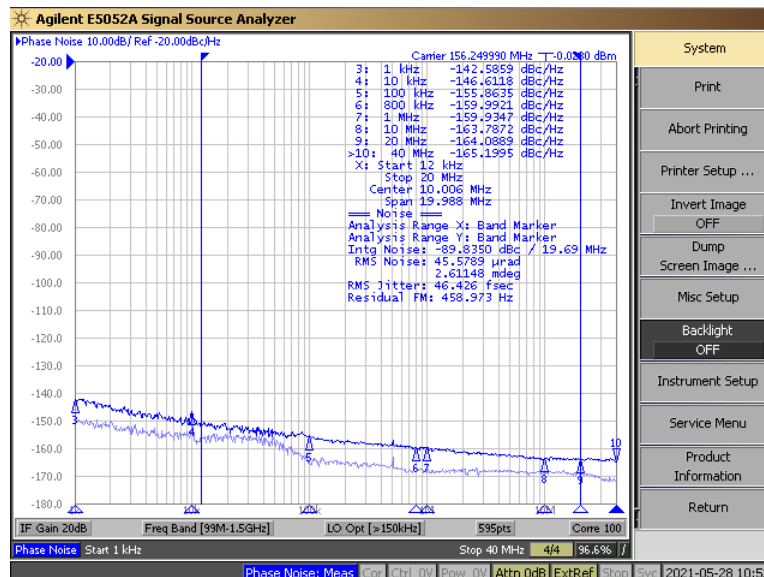


Figure 10-4. LMK1D2104 Output Phase Noise, 156.25 MHz, 46.4-fs RMS (12 kHz to 20 MHz)

The Figure 10-5 captures the low close-in phase noise of the LMK1D2104 device. The LMK1D2102 and LMK1D2104 have excellent flicker noise as a result of superior process technology and design. This enables their use for clock distribution in radar systems, medical imaging systems etc which require ultra-low close-in phase noise clocks.

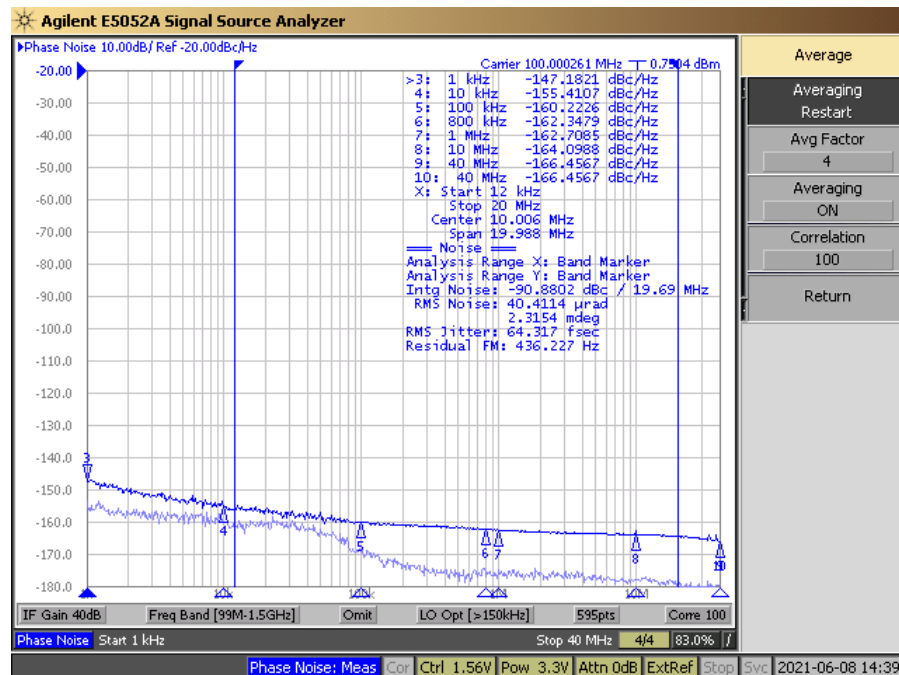


Figure 10-5. LMK1D2104 Output Phase Noise, 100 MHz, 1 kHz offset: -147 dBc/Hz

10.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC-resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 10-6 shows this recommended power-supply decoupling method.

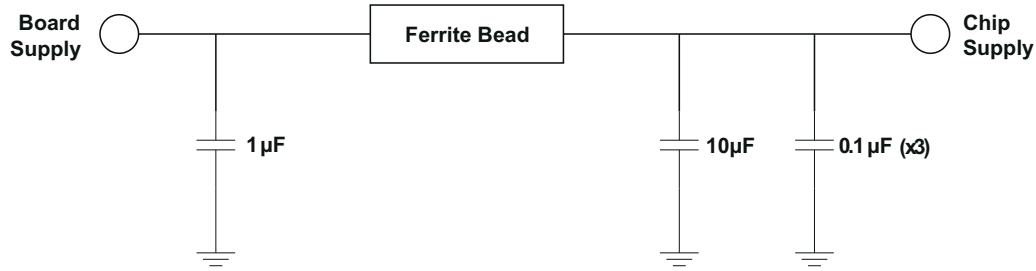


Figure 10-6. Power Supply Decoupling

10.4 Layout

10.4.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the printed-circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. [Figure 10-7](#) shows a recommended land and via pattern for the 16-pin package (LMK1D2102).

10.4.2 Layout Example

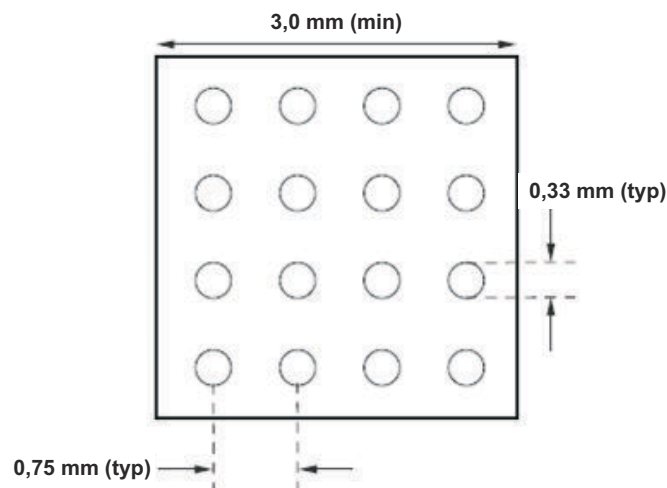


Figure 10-7. Recommended PCB Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- [Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board](#) (SCAU043)
- [Power Consumption of LVPECL and LVDS](#) (SLYT127)
- [Semiconductor and IC Package Thermal Metrics](#) (SPRA953)
- [Using Thermal Calculation Tools for Analog Components](#) (SLUA556)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

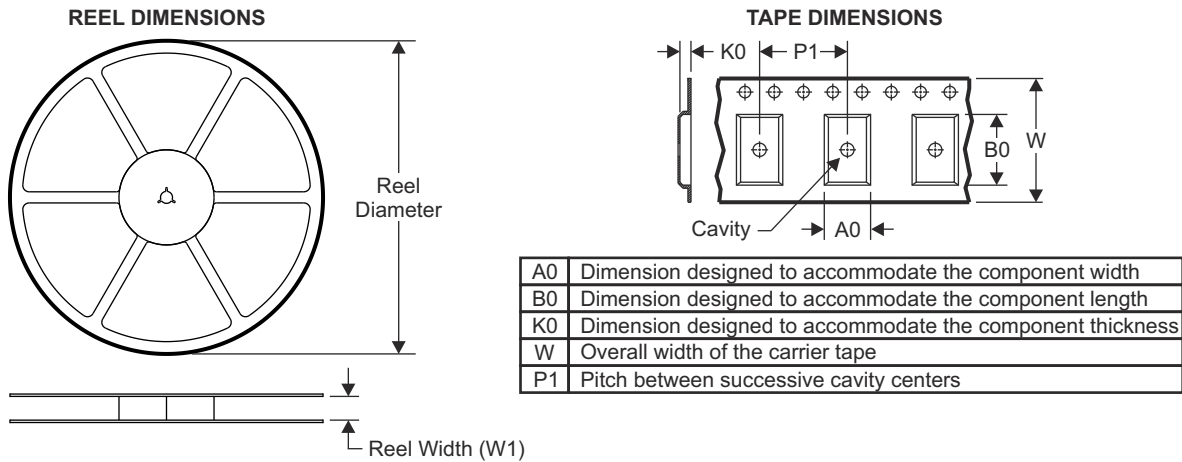
11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

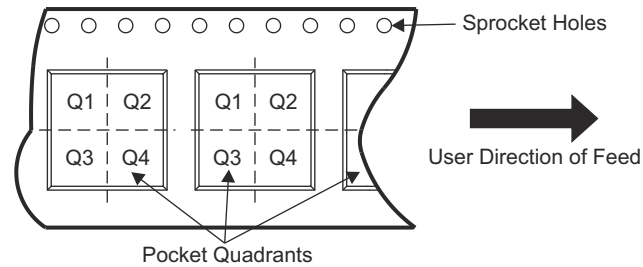
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

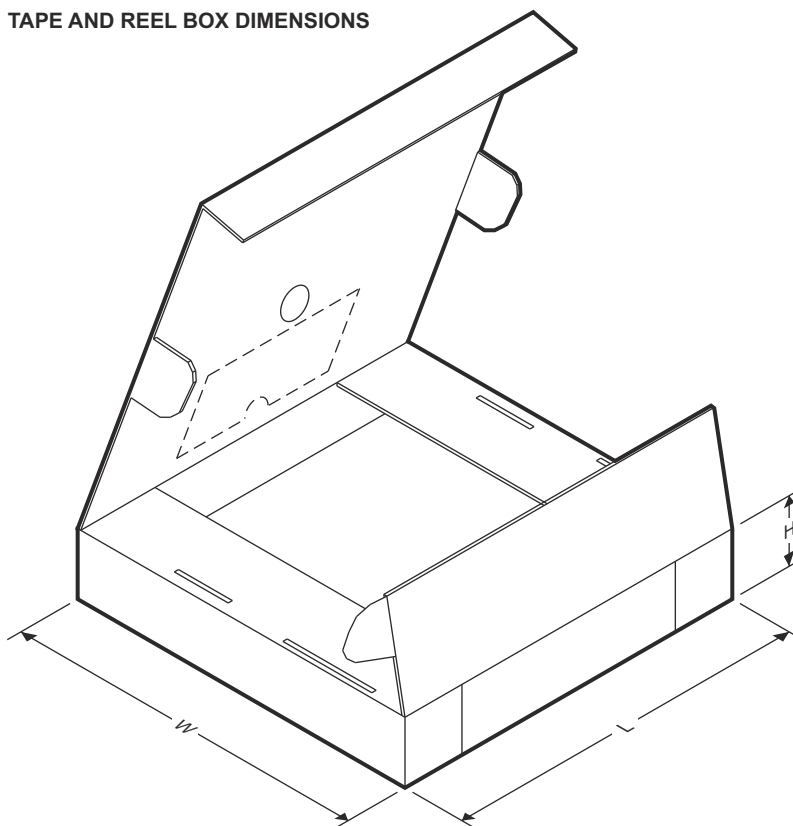


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMK1D2102RGTR | VQFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LMK1D2102RGTT | VQFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LMK1D2104RHDR | VQFN | RHD | 28 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LMK1D2104RHDT | VQFN | RHD | 28 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMK1D2102RGTR | VQFN | RGT | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| LMK1D2102RGTT | VQFN | RGT | 16 | 250 | 210.0 | 185.0 | 35.0 |
| LMK1D2104RHDR | VQFN | RHD | 28 | 3000 | 367.0 | 367.0 | 35.0 |
| LMK1D2104RHDT | VQFN | RHD | 28 | 250 | 210.0 | 185.0 | 35.0 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LMK1D2102RGTR | Active | Production | VQFN (RGT) 16 | 3000 LARGE T&R | Yes | FULL NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LD2102 |
| LMK1D2102RGTR.B | Active | Production | VQFN (RGT) 16 | 3000 LARGE T&R | Yes | FULL NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LD2102 |
| LMK1D2102RGTRG4 | Active | Production | VQFN (RGT) 16 | 3000 LARGE T&R | Yes | FULL NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LD2102 |
| LMK1D2102RGTRG4.B | Active | Production | VQFN (RGT) 16 | 3000 LARGE T&R | Yes | FULL NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LD2102 |
| LMK1D2102RGTT | Active | Production | VQFN (RGT) 16 | 250 SMALL T&R | Yes | FULL NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LD2102 |
| LMK1D2102RGTT.B | Active | Production | VQFN (RGT) 16 | 250 SMALL T&R | Yes | FULL NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LD2102 |
| LMK1D2104RHDR | Active | Production | VQFN (RHD) 28 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2104 |
| LMK1D2104RHDR.B | Active | Production | VQFN (RHD) 28 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2104 |
| LMK1D2104RHDRG4 | Active | Production | VQFN (RHD) 28 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2104 |
| LMK1D2104RHDRG4.B | Active | Production | VQFN (RHD) 28 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2104 |
| LMK1D2104RHDT | Active | Production | VQFN (RHD) 28 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2104 |
| LMK1D2104RHDT.B | Active | Production | VQFN (RHD) 28 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LMK1D 2104 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGT 16

GENERIC PACKAGE VIEW

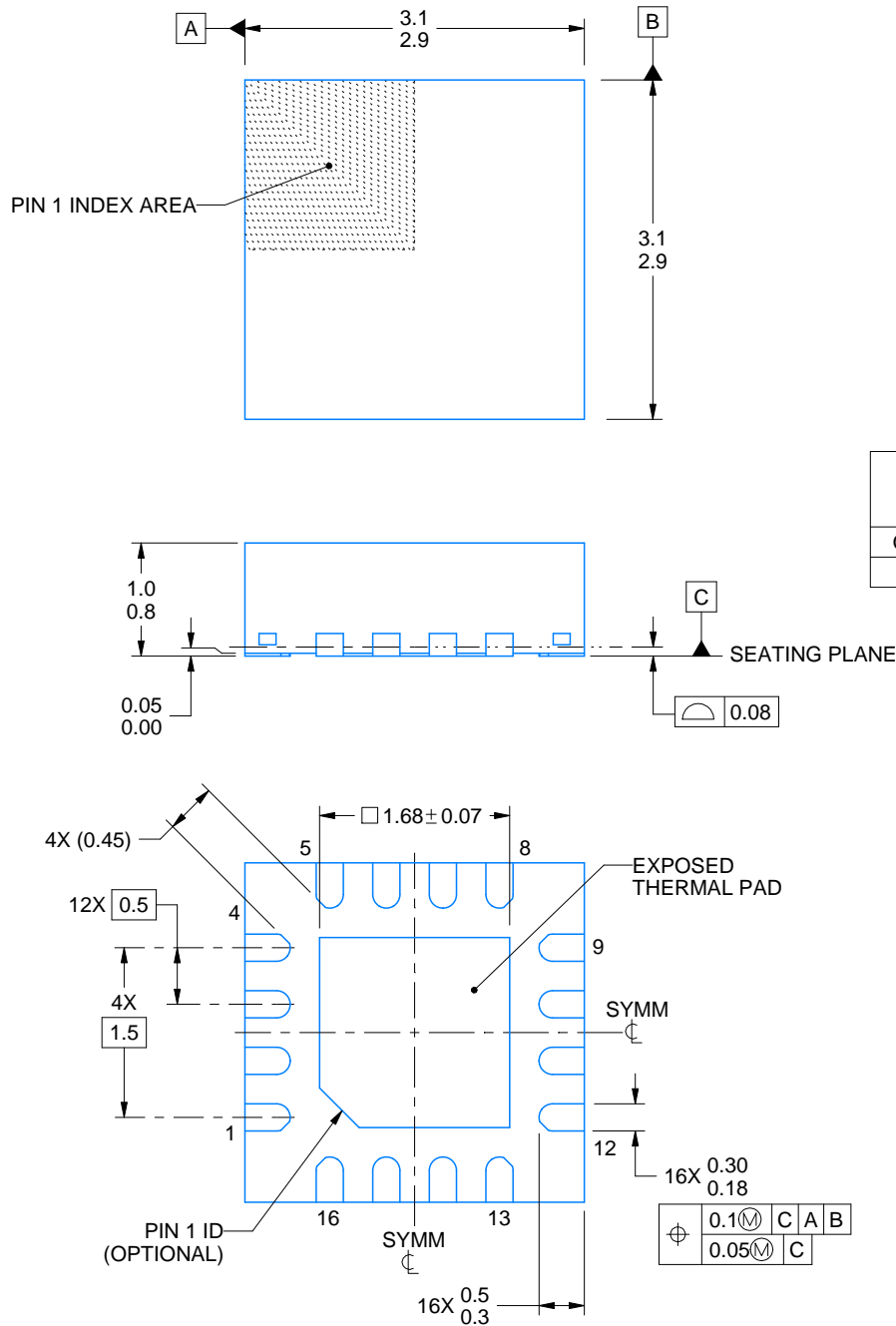
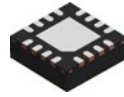
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



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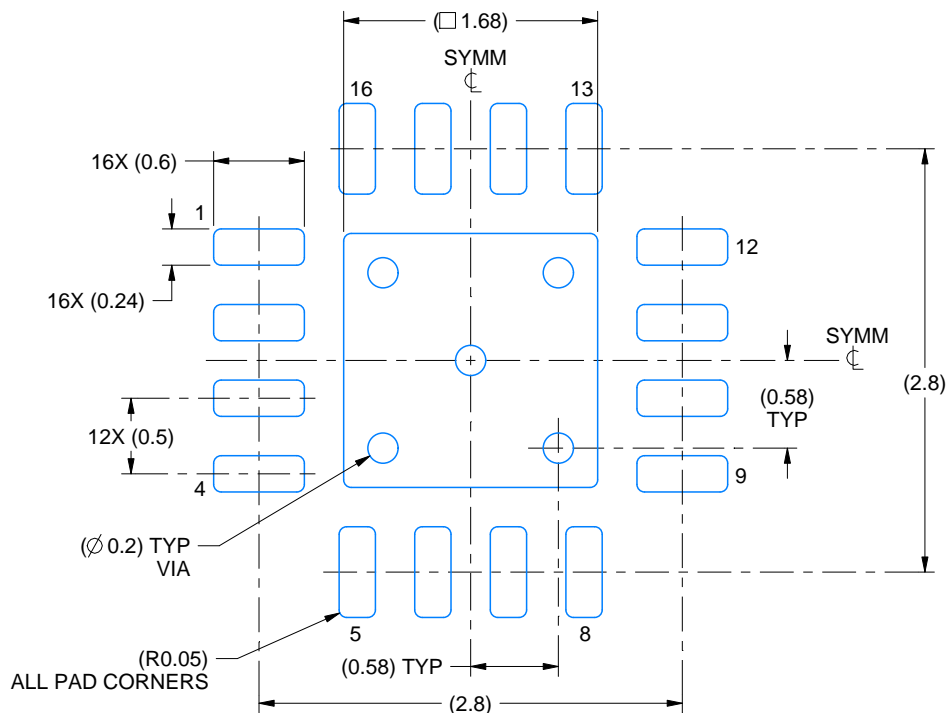
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

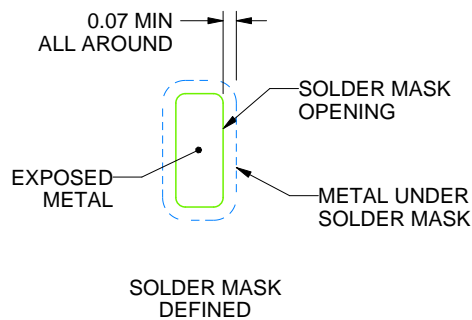
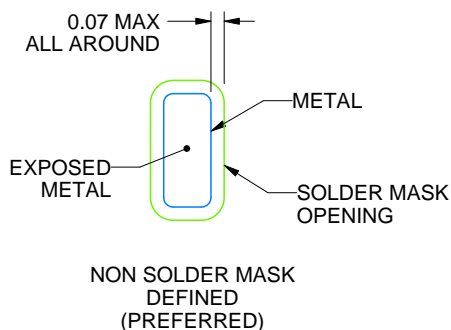
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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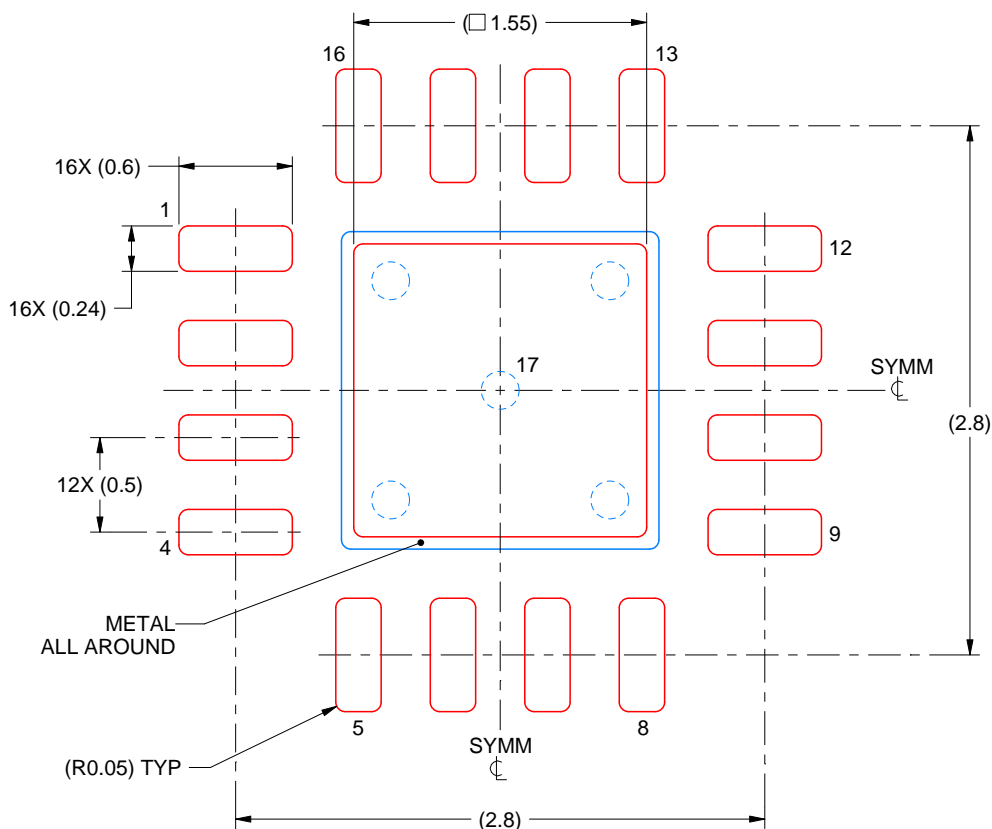
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

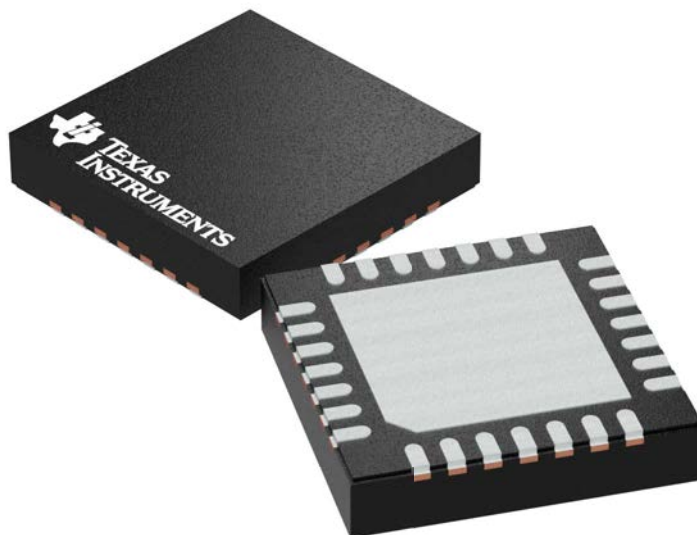
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

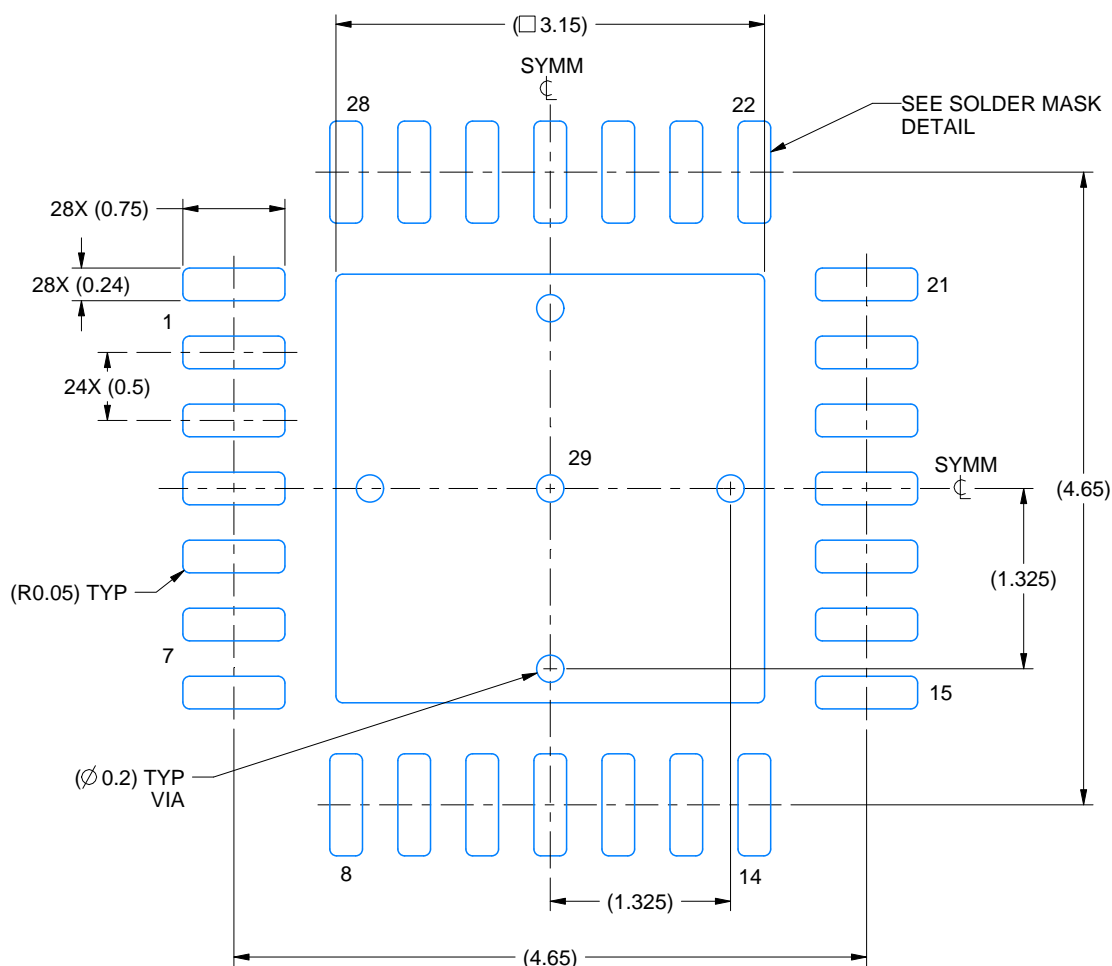
4204400/G

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

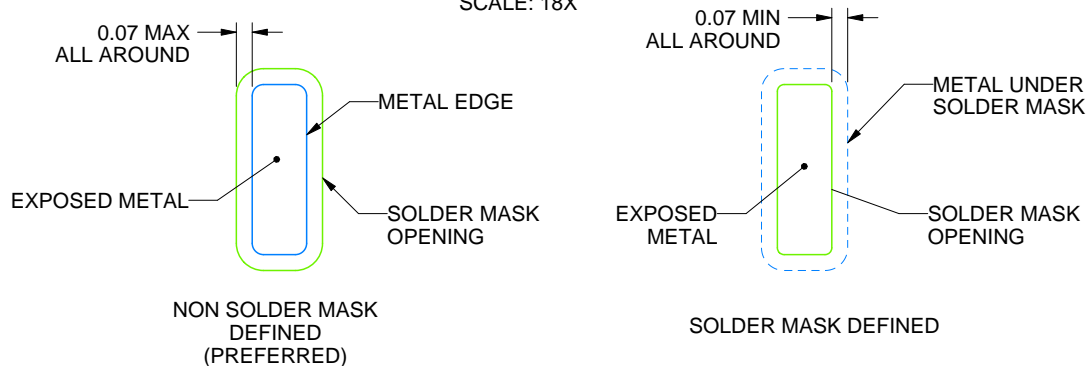
RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

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NOTES: (continued)

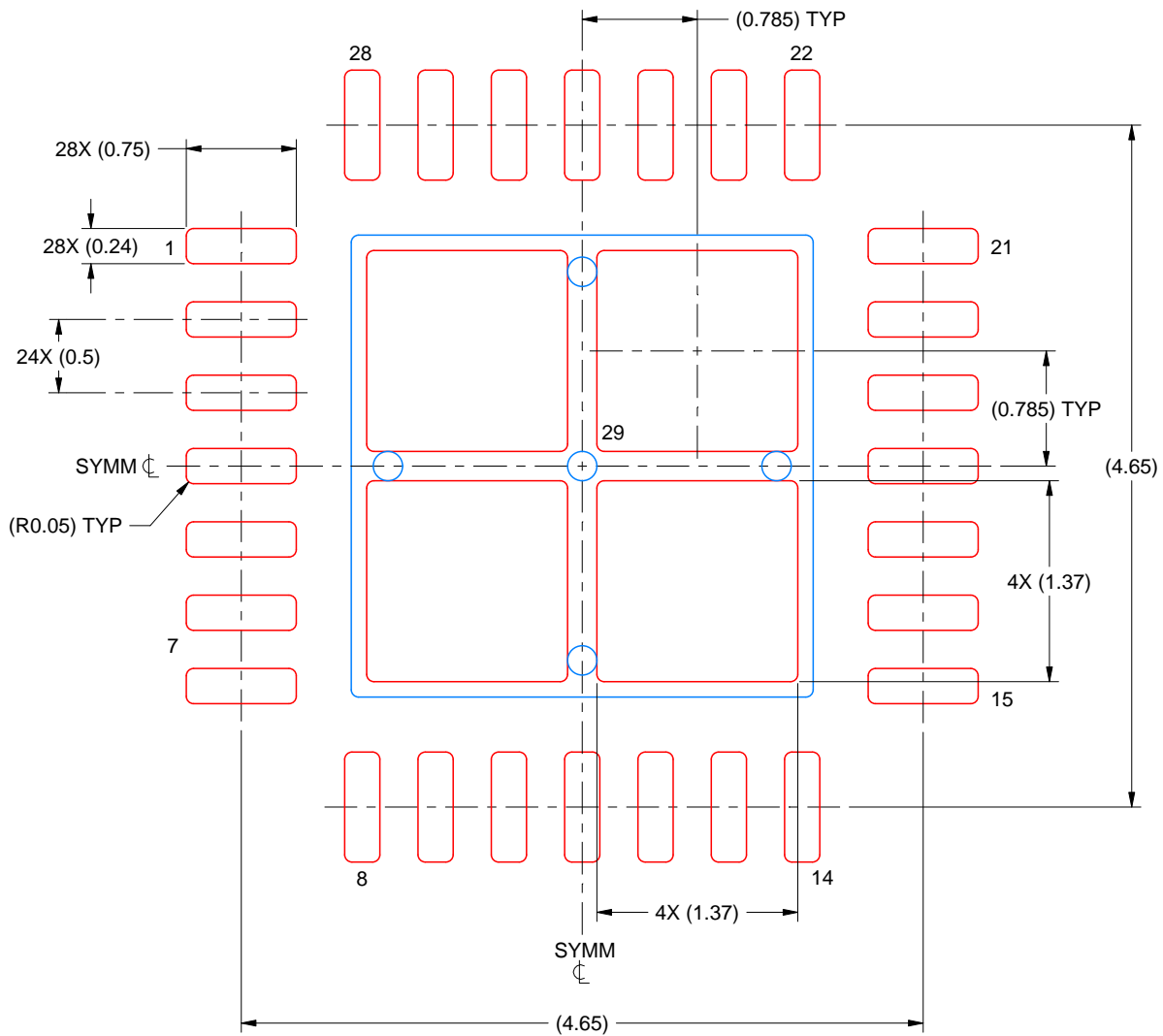
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 20X

EXPOSED PAD 29
 76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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