LMK6L-Q1 Ultra-Low Jitter, High-performance Differential Automotive BAW Oscillator

1 Features

- AEC Q-200 qualified:
  - Device temperature grade 2: –40°C to +105°C
- Output frequency:
  - Initial frequency offerings: 50, 100, 125, 156.25, 312.5, 625, 1250MHz
  - Other fixed frequencies on request
- Output formats:
  - LP-HCSL: 50MHz to 625MHz
    - V_{OH} options of 750mV or 850mV
  - LVDS, HS-LVDS, AC-LVPECL: 50MHz to 1250MHz
    - Output swing: 700mVppd to 2Vppd for 3.3V and 700mVppd to 1.6Vppd for 2.5V in 100mVppd step size
    - $V_{CM\ LVDS,\ HS\text{-}LVDS}$ = 1.2V and $V_{CM\ AC\text{-}LVPECL}$ = VDD/2
- Ultra-low jitter:
  - 53fs typical RMS jitter at 156.25MHz LP-HCSL output
  - 41fs typical RMS jitter at 312.5MHz LP-HCSL output
  - 45fs typical RMS jitter at 312.5MHz HS-LVDS (1.2Vppd) output
- Supports PCIe Gen 1 to Gen 7
- Less than –78dBc spurs for 156.25MHz LP-HCSL PSRR performance (ripple frequencies greater than 10kHz, 50mV supply ripple, 0.1µF decoupling capacitor)
- ±25ppm frequency accuracy (inclusive of all factors with 10-year aging at 25°C board temperature)
- 50mA typical current consumption at 3.3V and 156.25MHz LP-HCSL (V_{OH} = 750mV)
- 2.5V / 3.3V power supply (2.375V through 3.465V)
- Industry standard 6-pin wettable flank package:
  - 3.2mm × 2.5mm (DLE)
  - Preview, contact TI: 2.0mm × 1.6mm (DLR)

2 Applications

- SoC REFCLK
- High-performance compute
  - In-vehicle ethernet switch
- Bluetooth/Wi-Fi module

3 Description

Texas Instruments' high-precision bulk-acoustic wave (BAW) micro-resonator technology is integrated directly into a package allowing for low jitter clock circuitry. BAW is fully designed and manufactured at TI factories like other silicon-based fabrication processes.

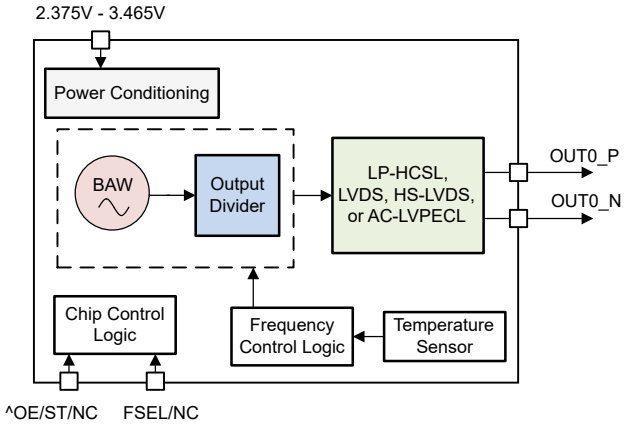
The LMK6L-Q1 device is an ultra-low jitter, fixed frequency oscillator. This device incorporates the BAW as the resonator source. The device is factory programmed per specific operation mode including frequency, output type, function pin, and frequency stability.

The high-performance clocking, mechanical stability, flexibility, ultra-low jitter, and small package options for this device are designed for reference and core clocks in highspeed SerDes or SoC automotive applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMK6L-Q1	DLE (VSON, 6, wettable flank)	3.2mm × 2.5mm
	DLR (VSON, 6, wettable flank)(3)	2mm × 1.6mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Preview information, contact TI.



LMK6L-Q1 Simplified Block Diagram

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4 Device Comparison

Use Figure 4-1 to understand the device nomenclature of the LMK6L-Q1 orderable options.

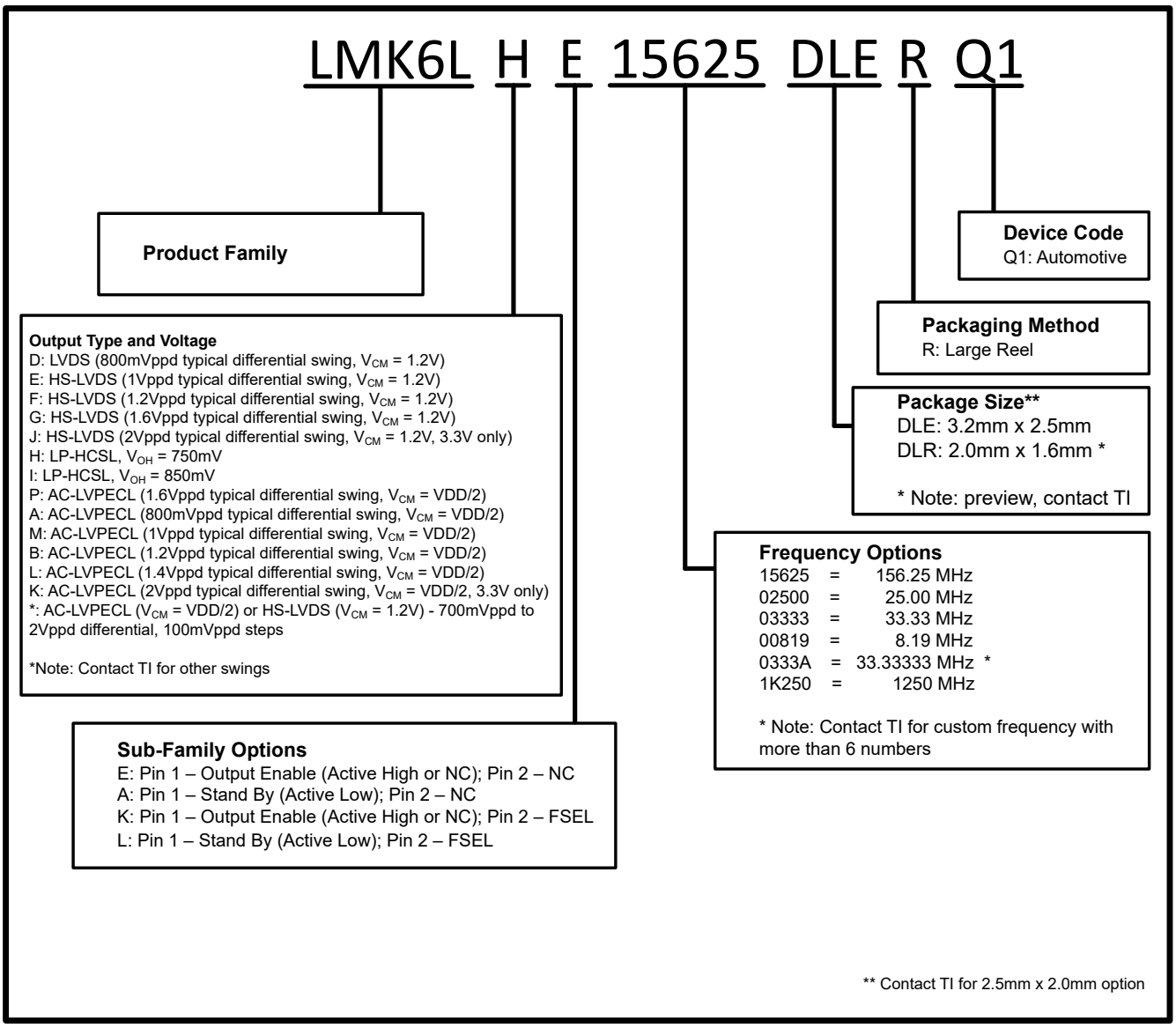

Figure 4-1. Part Number Guide: LMK6L-Q1

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5 Pin Configuration and Functions

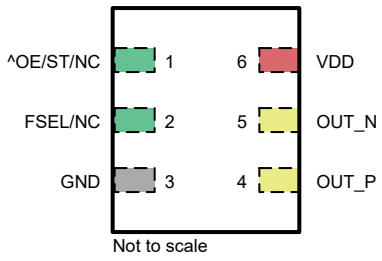

Figure 5-1. LMK6L-Q1 DLE and DLR 6-Pin (Top View)

Legend	
Input	Power
Ground	Output

Table 5-1. LMK6L-Q1 Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
^OE/ST/NC(2)	1	I / NC	Output Enable (OE), Stand By (ST), or No Connect (NC). For OE and ST: • Low: Output inactive • High/Floating: Output active Internal pull-up of 150kΩ. See Section 8.3.3 for more details.
^vFSEL/NC(2) (3)	2	I / NC	Output Frequency Select (FSEL) pin, or No Connect (NC). For FSEL, • Low: $F_{OUT}/4$ • Floating: F_{OUT} • High: $F_{OUT}/2$ F_{OUT} is the output frequency set by the OPN. See Section 4 for more details. Internal pullup resistor of 200kΩ and internal pulldown resistor of 200kΩ. See Section 8.3.3 for more details.
GND	3	G	Device ground.
OUT_P	4	O	Positive differential output clock.
OUT_N	5	O	Negative differential output clock.
VDD	6	P	Device power supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) Pins with a "^" prefix have an internal pullup resistor.
(3) Pins with a "v" prefix have an internal pulldown resistor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device Supply Voltage(2)	–0.3	3.7	V
EN	Logic Input Voltage	–0.3	VDD + 0.3	V
OUTP, OUTN	Clock Output Voltage(3)	–0.3	VDD + 0.3	V
T_J	Junction Temperature		140	℃
T_{STG}	Storage Temperature	–65	150	℃

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) For all devices with Recommended Operating Voltage of 2.5V±5% and 3.3V±5%
(3) For all differential output types.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q200, all pins(1)	±2000	V
		Human body model (HBM), per AEC Q200, all pins(1)	±2000	V

(1) AEC Q200-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Environmental Compliance

		VALUE	UNIT
Mechanical Shock Resistance	MIL-STD-883F, Method 2002, Condition A	1500	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2026, Condition C	10	g
	MIL-STD-883F, Method 2007, Condition A	20	g
Moisture Sensitivity Level (MSL)		MSL1	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Device Supply Voltage(1)	2.375	2.5, 3.3	3.465	V
T_A	Ambient temperature	–40		105	°C
T_{PCB}	PCB temperature (measured below package)	–40		105	°C
T_J	Junction temperature	–40		125	°C
t_{RAMP}	VDD power-up ramp time(1) (2)	0.1		100	ms

(1) For all devices with Recommended Operating Voltage of 2.5V ±5% and 3.3V + 5% to -10%
(2) VDD power-up ramp time is defined as minimum time taken for power supply to exceed 95% of nominal VDD. Monotonic power supply ramp is assumed. In case of erratic or non-monotonic power supply ramp, enable the output stage by controlling OE and EN pin.

6.5 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DLR (VSON)	6	TBD	TBD	TBD	TBD	TBD	TBD	°C/W

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PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DLE (VSON)	6	TBD	TBD	TBD	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Electrical Characteristics

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Tolerance						
F_T	Total frequency stability (OPN 14th character: option F)	Inclusive of: solder shift, initial tolerance, variation over -40°C to 105°C, variation over rated supply voltage range, and 10 year aging at 25°C.	–25		25	ppm
F_{AGE_1yr}	Frequency stability due to 1 year aging	1 year aging at 25°C (±25ppm)	TBD		TBD	ppm
F_{AGE_10yr}	Frequency stability change due to aging (included in total frequency stability)	10 year aging at 25°C (±25ppm)	TBD		TBD	ppm
F_{TEMP}	Frequency stability due to temperature (included in total frequency stability)	Over Recommended Operating Condition, dT/dt < 10°K/min	TBD		TBD	ppm
F_{HYS}	Frequency stability due to hysteresis (included in total frequency stability)		TBD		TBD	ppm
Current Consumption Characteristics						
I_{DD}	Device Power Consumption (LVDS, Excluding load current)	50MHz, 2.5V		49		mA
		50MHz, 3.3V		51		mA
		100MHz, 2.5V		52		mA
		100MHz, 3.3V		54		mA
		125MHz, 2.5V		49		mA
		125MHz, 3.3V		51		mA
		156.25MHz, 2.5V		50		mA
		156.25MHz, 3.3V		51		mA
		312.5MHz, 2.5V		51		mA
		312.5MHz, 3.3V		53		mA
		625MHz, 2.5V		49		mA
		625MHz, 3.3V		51		mA
		1250MHz, 2.5V		50		mA
		1250MHz, 3.3V		52		mA

ADVANCE INFORMATION

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device Power Consumption (HS-LVDS 1.2Vppd and AC-LVPECL 1.2Vppd, Excluding load current)	50MHz, 2.5V		49		mA
		50MHz, 3.3V		51		mA
		100MHz, 2.5V		53		mA
		100MHz, 3.3V		54		mA
		125MHz, 2.5V		50		mA
		125MHz, 3.3V		52		mA
		156.25MHz, 2.5V		50		mA
		156.25MHz, 3.3V		52		mA
		312.5MHz, 2.5V		52		mA
		312.5MHz, 3.3V		53		mA
		625MHz, 2.5V		50		mA
		625MHz, 3.3V		52		mA
		1250MHz, 2.5V		51		mA
		1250MHz, 3.3V		53		mA
I_{DD}	Device Power Consumption (LP-HCSL, V_{OH} = 750mV, Excluding load current)	50MHz, 2.5V		48		mA
		50MHz, 3.3V		49		mA
		100MHz, 2.5V		52		mA
		100MHz, 3.3V		53		mA
		125MHz, 2.5V		49		mA
		125MHz, 3.3V		50		mA
		156.25MHz, 2.5V		50		mA
		156.25MHz, 3.3V		51		mA
		312.5MHz, 2.5V		53		mA
		312.5MHz, 3.3V		54		mA
		625MHz, 2.5V		54		mA
		625MHz, 3.3V		56		mA
$I_{DD-STBY}$	Device Stand By current	ST (Stand By) = GND, 2.5V		2		mA
		ST (Stand By) = GND, 3.3V		2		mA
I_{DD-PD}	Device current with output disabled (156.25MHz)	OE = GND, LP-HCSL mode, V_{OH} = 750mV, VDD = 2.5V		44		mA
		OE = GND, LP-HCSL mode, V_{OH} = 750mV, VDD = 3.3 V		46		mA
LVDS Output Characteristics						
F_{out}	Output Frequency		50		1250	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC coupled, VDD = 3.3V, 156.25MHz	350	400		mV
		AC coupled, VDD = 2.5V, 156.25MHz	350	400		mV
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC coupled, VDD = 3.3V, 312.5MHz	350	400		mV
		AC coupled, VDD = 2.5V, 312.5MHz	350	400		mV
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC coupled, VDD = 3.3V, 625MHz	350	400		mV
		AC coupled, VDD = 2.5V, 625MHz	350	400		mV
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC coupled, VDD = 3.3V, 1250MHz	350	400		mV
		AC coupled, VDD = 2.5V, 1250MHz	350	400		mV
$V_{OD,DIFF}$	Differential Output peak-peak swing[2]			2×|V_{OD}|		mVppd
V_{OS}	Output Common-Mode Voltage	VDD = 3.3 V		1.2		V
		VDD = 2.5 V		1.2		V

ADVANCE INFORMATION

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, VDD = 2.5 V/ 3.3 V		226		ps
ODC	Output Duty Cycle	VDD = 2.5 V/ 3.3V, measured between 50% points on the waveform	45	50	55	%
V_{CM-IM}	Common Mode Imbalance	Measured at C_L = 100 pF on Common Mode Node	–150		150	mV
HS-LVDS Output Characteristics						
F_{out}	Output Frequency		50		1250	MHz
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 156.25MHz	350		1000	mV
		AC coupled, VDD = 2.5V, 156.25MHz	350		800	mV
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 312.5MHz	350		1000	mV
		AC coupled, VDD = 2.5V, 312.5MHz	350		800	mV
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 625MHz	350		1000	mV
		AC coupled, VDD = 2.5V, 625MHz	350		800	mV
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 1250MHz	350		750	mV
		AC coupled, VDD = 2.5V, 1250MHz	350		750	mV
$V_{OD,step}$	Output Voltage Swing (V_{OH} - V_{OL}) step size	AC coupled, 1250MHz		50		mV
$V_{OD,DIFF}$	Differential Output peak-peak swing[2]			2×|V_{OD}|		mVppd
V_{OS}	Output Common-Mode Voltage	VDD = 3.3 V		1.2		V
V_{OS}	Output Common-Mode Voltage	VDD = 2.5 V		1.2		V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, VDD = 2.5 V/ 3.3 V		230		ps
ODC	Output Duty Cycle	VDD = 2.5 V/ 3.3V, measured between 50% points on the waveform	45	50	55	%
V_{CM-IM}	Common Mode Imbalance	Measured at C_L = 100 pF on Common Mode Node	–150		150	mV
AC-LVPECL Output Characteristics						
F_{out}	Output Frequency		50		1250	MHz
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 156.25MHz	350		1000	mV
		AC coupled, VDD = 2.5V, 156.25MHz	350		750	mV
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 312.5MHz	350		1000	mV
		AC coupled, VDD = 2.5V, 312.5MHz	350		750	mV
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 625MHz	350		1000	mV
		AC coupled, VDD = 2.5V, 625MHz	350		750	mV
$V_{OD,range}$	Output Voltage Swing (V_{OH} - V_{OL}) range	AC coupled, VDD = 3.3V, 1250MHz	350		750	mV
		AC coupled, VDD = 2.5V, 1250MHz	350		750	mV
$V_{OD,step}$	Output Voltage Swing (V_{OH} - V_{OL}) step size	AC coupled, 1250MHz		50		mV
$V_{OD,DIFF}$	Differential Output peak-peak swing[2]			2×|V_{OD}|		mV_{ppd}
V_{OS}	Output Common-Mode Voltage	VDD = 3.3 V		VDD/2		V
		VDD = 2.5 V		VDD/2		V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, VDD = 2.5 V/ 3.3 V		222		ps
ODC	Output Duty Cycle	VDD = 2.5 V/ 3.3V, measured between 50% points on the waveform	45	50	55	%
V_{CM-IM}	Common Mode Imbalance	Measured at C_L = 100 pF on Common Mode Node	–150		150	mV
LP-HCSL Output characteristics						

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{out}	Output Frequency		50		625	MHz
V_{OH}	Output High Voltage (OPN 6th character: option H)	DC coupled, 2pF load, VDD = 2.5 V/3.3 V	650	750	850	mV
	Output High Voltage (OPN 6th character: option I)	DC coupled, 2pF load, VDD = 2.5 V/3.3 V	750	850	950	mV
V_{OL}	Output Low Voltage	DC coupled, 2pF load, VDD = 2.5 V/ 3.3 V	–150	0	150	mV
$V_{overshoot}$	Overshoot voltage	V_{max} - V_{OH}			150	mV
$V_{OD,DIFF}$	Differential Output peak-peak swing(2)			$2\times\lvert V_{OH} - V_{OL}\rvert$		mVppd
V_{cross}	Absolute Crossing Point Voltage(3)	VDD = 3.3 V / 2.5 V, f_{out} = 100 MHz, PCIe test load, 15 dB loss at 4 GHz, fout = 100 MHz, Zdiff = 100 Ω	0.28	0.35	0.48	V
$V_{cross\text{-}delta}$	Absolute Crossing Point Voltage variation	VDD = 3.3 V / 2.5 V, f_{out} = 100 MHz, PCIe test load, 15 dB loss at 4 GHz, fout = 100 MHz, Zdiff = 100 Ω			TBD	mV
dV/dt	Output Slew Rate	50 ohms to ground; DC coupled load; measured slew rate in ±150mV from Center, programmable.(1)	2		12	V/ns
ΔdV/dt	Output Slew Rate variation				20	%
ODC	Output Duty Cycle		45	50	55	%
$\lvert V_{RB}\rvert$	Absolute value of ring back voltage	PCIe test load, 15 dB loss at 4 GHz, fout = 100 MHz, Zdiff = 100 Ω	100			mV
t_{stable}	Time before V_{RB} is allowed	PCIe test load, 15 dB loss at 4 GHz, fout = 100 MHz, Zdiff = 100 Ω	500			ps
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$		250		ps
Z_{DIFF}	Differential output DC impedance	V_{DD} = 3.3V		100		Ω
Z_{SE}	Single-ended output DC impedance	V_{DD} = 3.3V		50		Ω
Pin 1 Input Characteristics (OE/ST)						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		1.3			V
I_{IL}	Input Low Current	OE = GND	–40			µA
I_{IH}	Input High Current	OE = VDD			40	µA
C_{IN}	Input Capacitance			2		pF
Pin 2 Input Characteristics (FSEL)						
V_{IL}	Input Low Voltage, FSEL				0.2×VDD	V
V_{MID}	Input Middle Voltage, FSEL			0.4×VDD – 0.6×VDD		V
V_{IH}	Input High Voltage, FSEL		0.8×VDD			V
I_{IL}	Input Low Current	OE = GND	–40			µA
I_{IH}	Input High Current	OE = VDD			40	µA
C_{IN}	Input Capacitance			2		pF
$FSEL_{VDD}$	Minimum F_{out} for pin frequency control	FSEL = VDD	100			MHz
$FSEL_{GND}$		FSEL = GND	200			MHz
PSRR Characteristics						

ADVANCE INFORMATION

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSRR_{50mV, 0.1\mu F}$	Spur induced by 50mV power supply ripple at 156.25MHz LP-HCSL output, 0.1µF decoupling capacitor	Sine wave at 10kHz		-78		dBc
		Sine wave at 100kHz		-89		dBc
		Sine wave at 200kHz		-93		dBc
		Sine wave at 500kHz		-94		dBc
		Sine wave at 1MHz		-93		dBc
		Sine wave at 2MHz		-93		dBc
		Sine wave at 5MHz		-94		dBc
		Sine wave at 10MHz		-96		dBc
$PSRR_{50mV}$	Spur induced by 50mV power supply ripple at 156.25MHz LP-HCSL output, no power supply decoupling capacitor	Sine wave at 10kHz		TBD		dBc
		Sine wave at 100kHz		-80		dBc
		Sine wave at 200kHz		-78		dBc
		Sine wave at 500kHz		-72		dBc
		Sine wave at 1MHz		-66		dBc
		Sine wave at 2MHz		-61		dBc
		Sine wave at 5MHz		-57		dBc
		Sine wave at 10MHz		-58		dBc
$PSRR_{50mV, 0.1\mu F}$	Spur induced by 50mV power supply ripple at 312.5MHz AC-LVPECL 1.2Vppd output, 0.1µF decoupling capacitor	Sine wave at 10kHz		-68		dBc
		Sine wave at 100kHz		-67		dBc
		Sine wave at 200kHz		-72		dBc
		Sine wave at 500kHz		-80		dBc
		Sine wave at 1MHz		-86		dBc
		Sine wave at 2MHz		-93		dBc
		Sine wave at 5MHz		-106		dBc
$PSRR_{50mV}$	Spur induced by 50mV power supply ripple at 312.5MHz AC-LVPECL 1.2Vppd output, no power supply decoupling capacitor	Sine wave at 10kHz		TBD		dBc
		Sine wave at 100kHz		-57		dBc
		Sine wave at 200kHz		-64		dBc
		Sine wave at 500kHz		-75		dBc
		Sine wave at 1MHz		-78		dBc
		Sine wave at 2MHz		-69		dBc
		Sine wave at 5MHz		-66		dBc
		Sine wave at 10MHz		-67		dBc
$PSRR_{JITTER}$	Jitter sensitivity to power supply ripple	100kHz sine wave ripple, 3.3 V Supply, LP-HCSL		TBD		fs/mV
Power-On Characteristics						
t_{START_UP}	Start-up Time	Time elapsed from 0.95 x VDD until output is enabled and output is within specification; Tested with a VDD supply ramp time of around 200 µs			2	ms
t_{ST-EN}	Chip enable time	Time elapsed from standby (ST = V_{IH}) until output is enabled and output is within specification			2	ms
t_{ST-DIS}	Chip disable time	Time elapsed from standby (ST = V_{IL}) until chip is in standby mode			270	ns
t_{OE-EN}	Output enable time	Time elapsed from OE = V_{IH} until output is enabled and output is within specification			25	µs
t_{OE-DIS}	Output disable Time	Time elapsed from OE = V_{IL} until output is disabled			1	µs
LVDS - Clock Output Jitter						

ADVANCE INFORMATION

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 156.25MHz, 800mVppd		61		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-109		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-133		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-155		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-161		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-162		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 312.5MHz, 800mVppd		47		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-103		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-127		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-147		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-155		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-160		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-164		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 625MHz, 800mVppd		32		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-97		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-121		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-143		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-155		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-160		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-161		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 1250MHz, 800mVppd		27		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-91		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-116		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-138		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-153		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-159		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-160		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 100MHz, 800mVppd		157		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 125MHz, 800mVppd		79		fs
HS-LVDS - Clock Output Jitter						

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Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 156.25MHz, 1.2Vppd		56		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-109		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-133		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-155		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-162		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-163		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 312.5MHz, 1.2Vppd		44		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-103		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-127		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-147		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-155		dBc/Hz
PN_{10M}	Phase Noise at 10MHz			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-164		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 625MHz, 1.2Vppd		32		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-97		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-121		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-143		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-155		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-162		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 1250MHz, 1.2Vppd		27		fs
PN_{100}	Phase Noise at 100 Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-91		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-116		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-138		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-154		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-159		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			TBD		dBc/Hz
AC-LVPECL - Clock Output Jitter						
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 156.25MHz, 1.2Vppd		57		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-110		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-133		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-155		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-162		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-163		dBc/Hz

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 312.5MHz, 1.2Vppd		45		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-104		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-128		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-147		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-155		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			TBD		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 625MHz, 1.2Vppd		33		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-97		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-121		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-143		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-155		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-160		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			TBD		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 1250MHz, 1.2Vppd		28		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-90		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-115		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-138		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-154		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-159		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			TBD		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 100MHz, 1.2Vppd		152		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 125MHz, 1.2Vppd		73		fs
LP-HCSL - Clock output jitter						

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Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe1-cc}$	PCIe Gen 1 Common Clock jitter (jitter limit = 86ps)	F_{out} = 100MHz, V_{OH} = 750mV		TBD		ps
$J_{PCIe1-SRNS}$	PCIe Gen 1 SRNS jitter			TBD		ps
$J_{PCIe2-cc}$	PCIe Gen 2 Common Clock jitter (jitter limit = 3ps)			TBD		ps
$J_{PCIe2-SRNS}$	PCIe Gen 2 SRNS jitter			TBD		ps
$J_{PCIe3-cc}$	PCIe Gen 3 Common Clock jitter (jitter limit = 1ps)			TBD		ps
$J_{PCIe3-SRNS}$	PCIe Gen 3 SRNS jitter			TBD		ps
$J_{PCIe4-cc}$	PCIe Gen 4 Common Clock jitter (jitter limit = 500fs)			TBD		ps
$J_{PCIe4-SRNS}$	PCIe Gen 4 SRNS jitter			TBD		ps
$J_{PCIe5-cc}$	PCIe Gen 5 Common Clock jitter (jitter limit = 150fs)			TBD		ps
$J_{PCIe5-SRNS}$	PCIe Gen 5 SRNS jitter			TBD		ps
$J_{PCIe6-cc}$	PCIe Gen 6 Common Clock jitter (jitter limit = 100fs)			TBD		ps
$J_{PCIe6-SRNS}$	PCIe Gen 6 SRNS jitter			TBD		ps
$J_{PCIe6-cc}$	PCIe Gen 7 Common Clock jitter (jitter limit = 69fs)			TBD		ps
$J_{PCIe6-SRNS}$	PCIe Gen 7 SRNS jitter			TBD		ps
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 100MHz, V_{OH} = 750mV		66		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-113		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-138		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-159		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-166		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-167		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 156.25MHz, V_{OH} = 750mV		53		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-109		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-134		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-155		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-163		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-165		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-166		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 312.5MHz, V_{OH} = 750mV		41		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-104		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-128		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-150		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-161		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-162		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-164		dBc/Hz

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	Fout = 625MHz, V_{OH} = 750mV		38		fs
PN_{100}	Phase Noise at 100Hz Offset			TBD		dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-97		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-122		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-144		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-156		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-158		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-160		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F_{out} = 125MHz, V_{OH} = 750mV		56		fs
$R_{JITT,RMS}$	RMS period jitter	F_{out} = 156.25MHz, V_{OH} = 750mV		TBD		fs
$R_{JITT,PK}$	Peak-to-peak period jitter	F_{out} = 156.25MHz, V_{OH} = 750mV		TBD		fs

(1) Parameter is specified by design, not characterized or tested in production.
(2) See *Differential Voltage Measurement Terminology* section for definition of $V_{OD,DIFF}$ voltages
(3) V_{CROSS} is single-ended voltage when CLKOUTx_P = CLKOUTx_N with respect to system ground. Only valid on rising edge of CLKOUTx_P, when CLKOUTx_N is rising.

6.7 Timing Diagrams

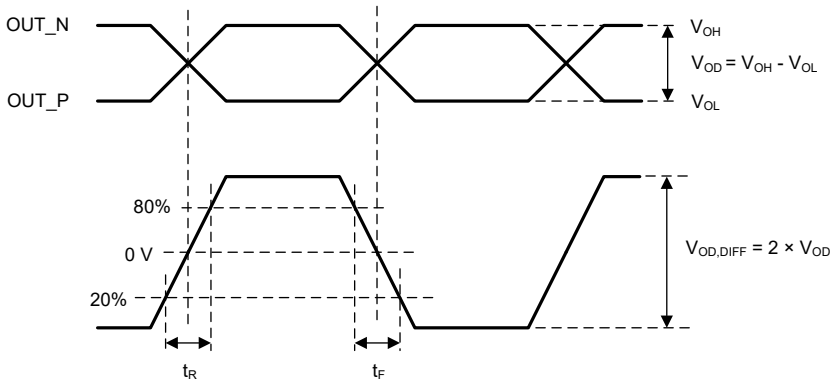

Figure 6-1. Differential Output Voltage Swing and Rise/Fall Time Definitions

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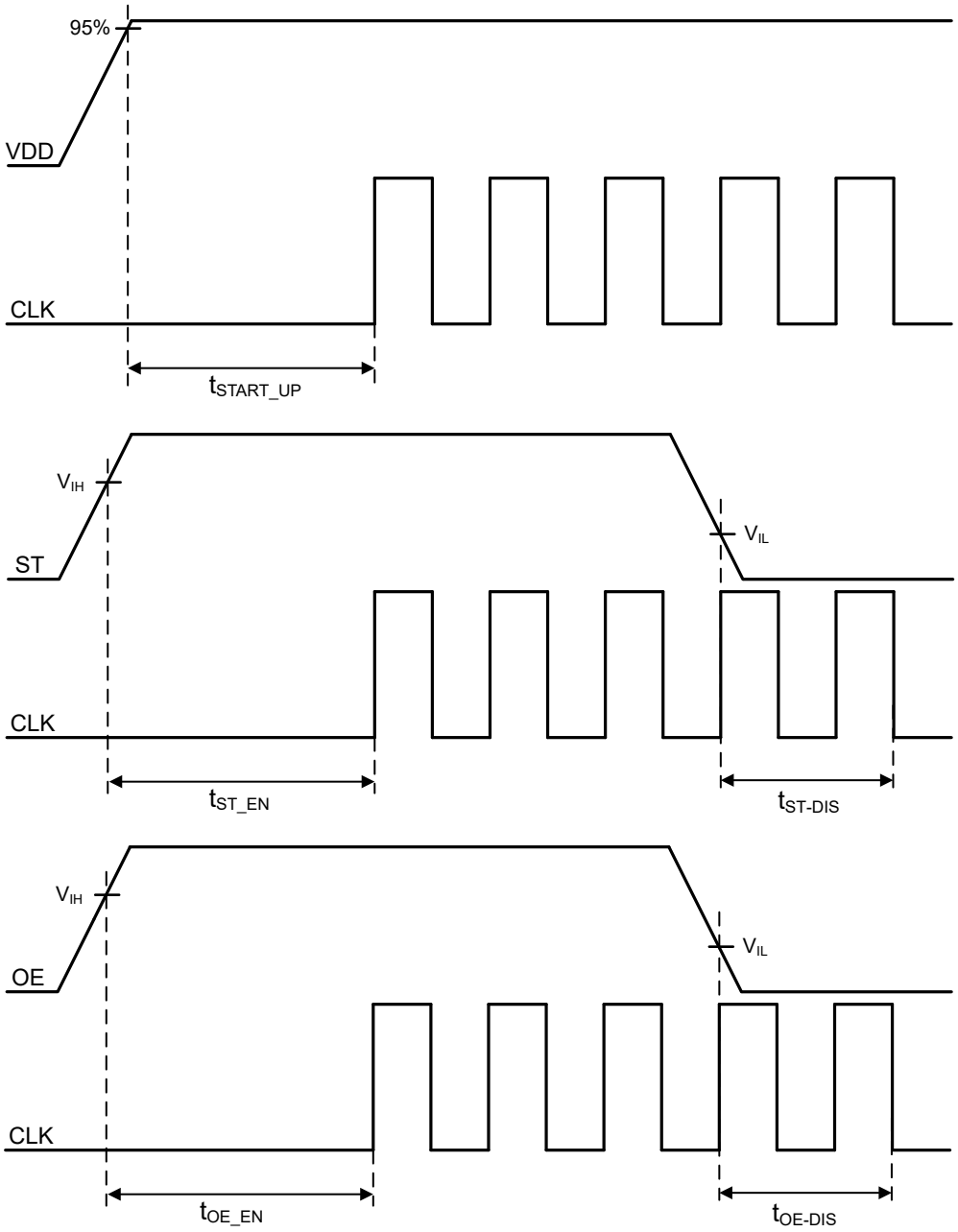

Figure 6-2. Power-On Characteristics

6.8 Typical Characteristics

Typical values at 25°C.

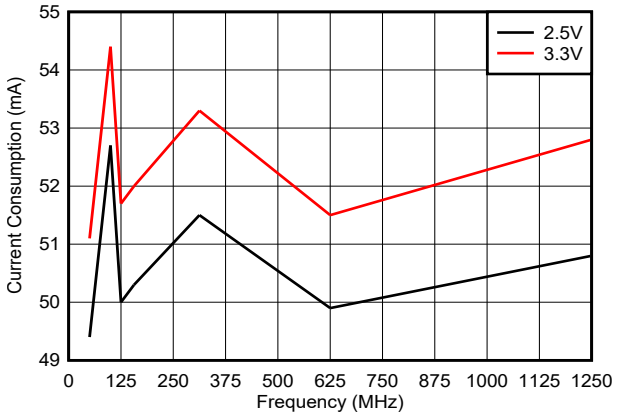

Figure 6-3. AC-LVPECL 1.2Vppd and HS-LVDS 1.2Vppd Current Consumption Across Frequency and Supply Voltage

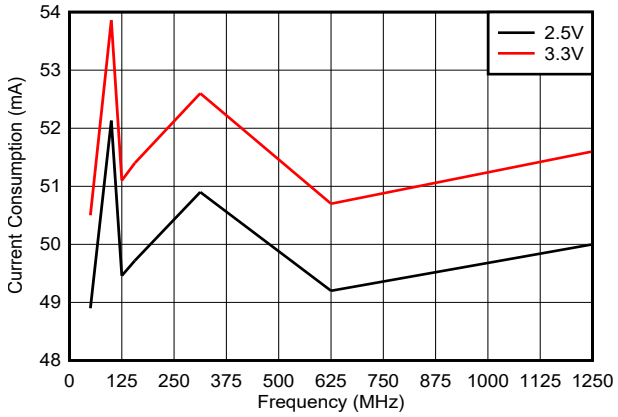

Figure 6-4. LVDS Current Consumption Across Frequency and Supply Voltage

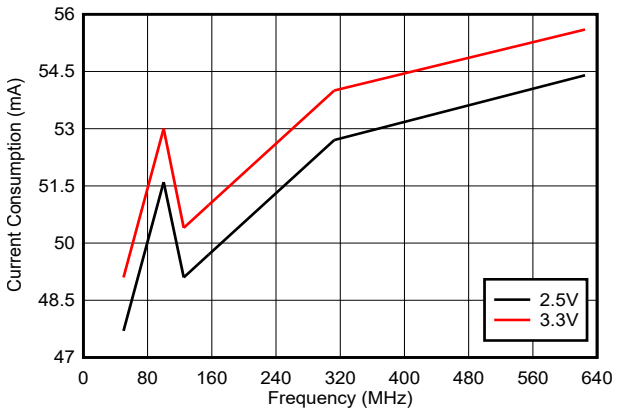

Figure 6-5. LP-HCSL (V_{OH} = 750mV) Current Consumption Across Frequency and Supply Voltage

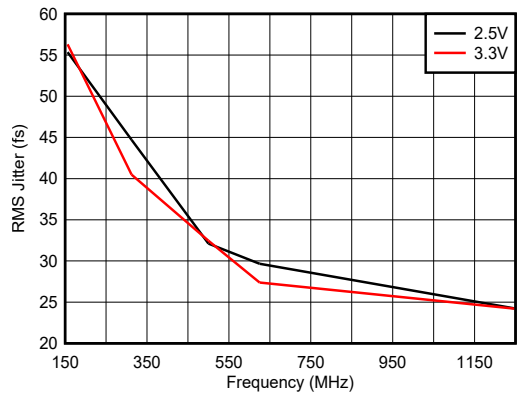

Figure 6-6. AC-LVPECL 1.2Vppd RMS Jitter (12kHz to 20MHz) Across Frequency and Supply Voltage

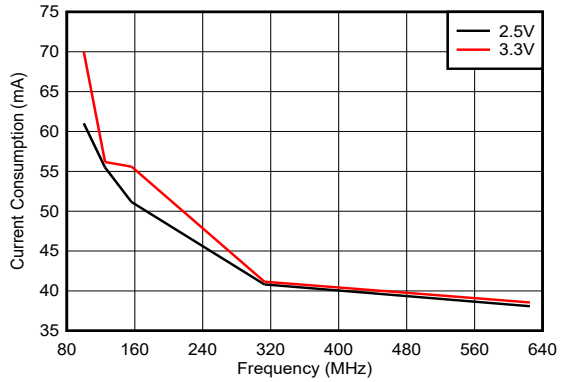

Figure 6-7. LP-HCSL (V_{OH} 750mV) RMS Jitter (12kHz to 20MHz) Across Frequency and Supply Voltage

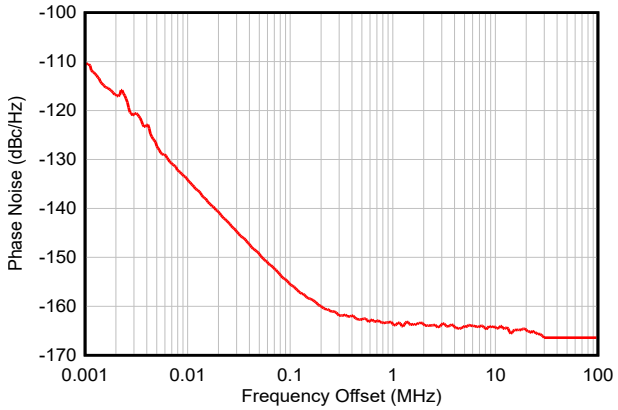

Figure 6-8. LP-HCSL (V_{OH} = 750mV) 156.25MHz Phase Noise Curve at 3.3V

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7 Parameter Measurement Information

7.1 Device Output Configurations

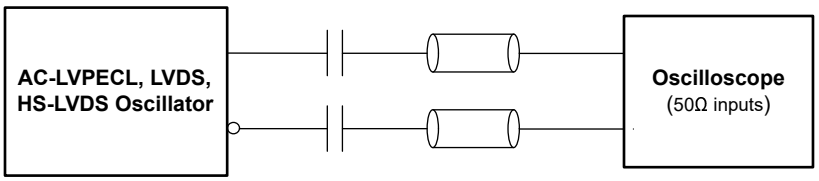


Figure 7-1. LMK6L-Q1 Output Test Configuration for AC-LVPECL, and LVDS Output Types

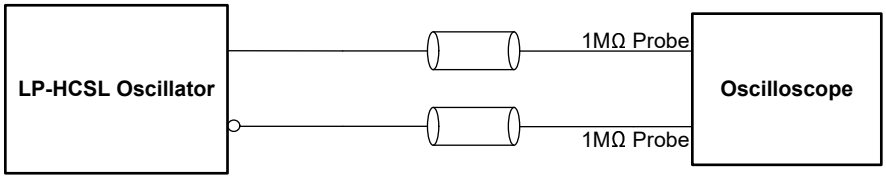


Figure 7-2. LMK6L-Q1 Output Test Configuration for LP-HCSL Output Type

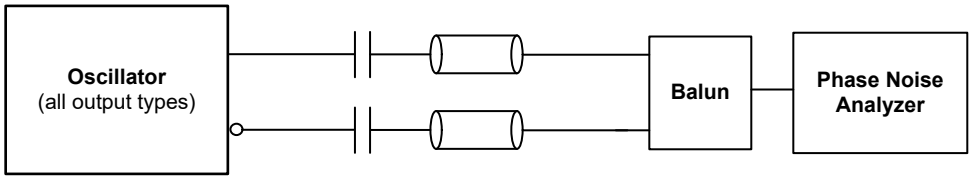


Figure 7-3. LMK6L-Q1 Output Phase Noise Configuration for All Output Types

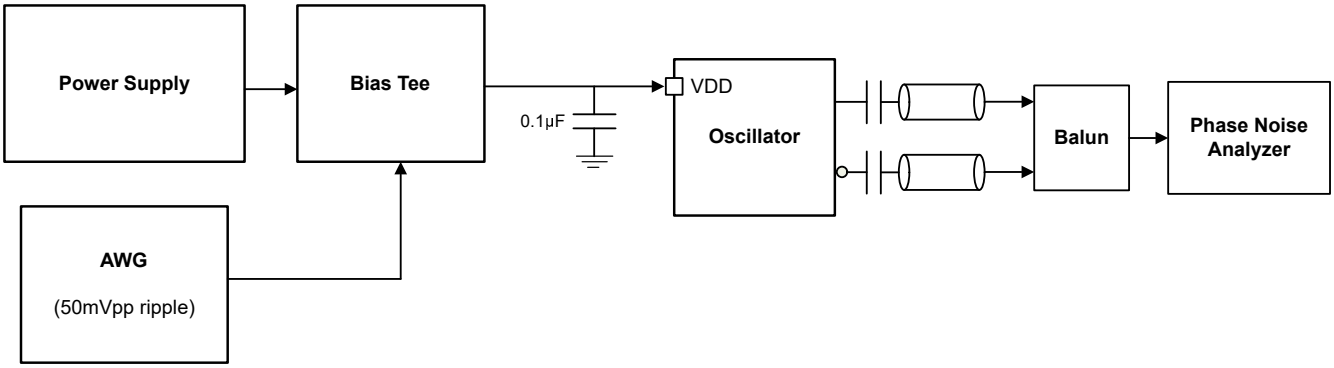


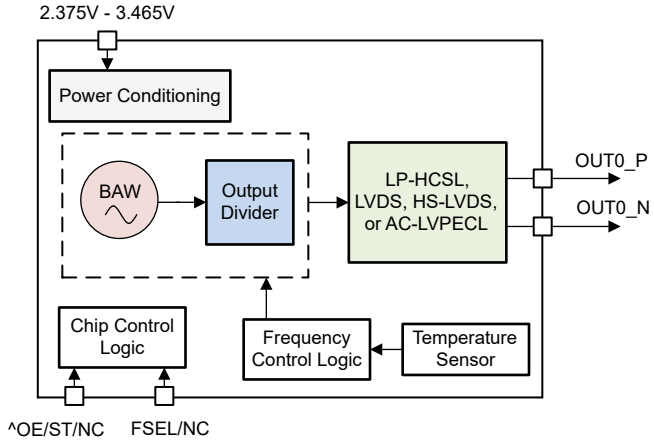
Figure 7-4. LMK6L-Q1 PSRR Configuration

8 Detailed Description

8.1 Overview

The LMK6L-Q1 is a fixed-frequency, factory-programmed BAW-based oscillator that can provide ultra-low jitter for differential outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bulk Acoustic Wave (BAW)

TI's BAW resonator technology uses piezoelectric transduction to generate high-Q resonance at 2.5GHz. The resonator is defined by the quadrilateral area overlaid by top and bottom electrodes. Alternating high- and low-acoustic impedance layers form acoustic mirrors beneath the resonant body to prevent acoustic energy leakage into the substrate. Furthermore, these acoustic mirrors are also placed on top of the resonator stack to protect the device from contamination and minimize energy leakage into the package materials. Figure 8-1 illustrates the BAW resonator's structure. This unique dual-Bragg acoustic resonator (DBAR) allows efficient excitation without the need of costly vacuum cavities around the resonator. As a result, TI's BAW resonator is immune to frequency drift caused by adsorption of surface contaminants and can be directly placed in the non-hermetic plastic package with a small standard oscillator footprint of the oscillator IC. Refer to the BAW webpage for more details on TI's BAW technology.

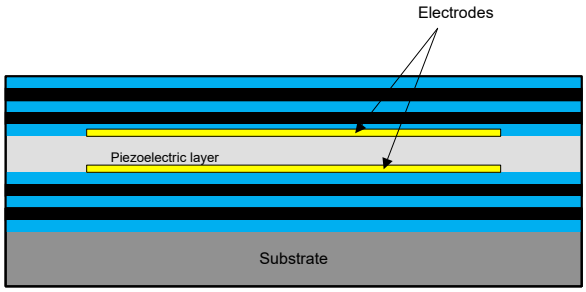


Figure 8-1. BAW Resonator Structure

8.3.2 Device Block-Level Description

The LMK6L-Q1 contains a BAW oscillator, an integer divider, and an output driver, which together generate a factory-programmed output frequency. Temperature variations of oscillation frequency are continuously monitored by an internal precision temperature sensor and provided as input to the frequency control logic block as seen on LMK6L-Q1 Functional Block Diagram. Using this frequency control logic block, frequency corrections are performed internally for maintaining the output frequency within ±25ppm across temperature range and aging for 10 years. The output driver is capable of providing differential AC-LVPECL, LVDS, HS-LVDS, or

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LP-HCSL output formats. The device contains internal LDOs which reduces the power supply noise, resulting in low noise clock output, and exceptional PSRR performance as seen on *Electrical Characteristics*.

8.3.3 Function Pins

Pins 1 and 2 on the LMK6L-Q1 serve multiple functions as defined by the OPN (refer to Section 4 for more information). Configurations include Output Enable (OE) and Stand By (ST) on pin 1, and Output Frequency Select (FSEL) on pin 2. FSEL divides the frequency defined in the OPN (or F_{OUT}) by 2 or 4, providing 3 different frequencies from one OPN. FSEL is further described in Table 8-1 and Section 8.3.3.1. OE is Active High and ST is Active Low by default, contact TI for other options.

Pin 1 is driven internally with a 150kΩ pullup resistor. Pin 2 is driven internally with a 200kΩ pullup and 200kΩ pulldown resistors. Both pin 1 and 2 can have a external pullup or pulldown resistor between 0Ω to 10kΩ each.

Table 8-1. Function Pin Descriptions for LMK6L-Q1

ORDERABLE OPTION (7TH CHARACTER)	PIN NO.	PIN DESCRIPTION	OUTPUT FUNCTION
E	Pin 1	Output Enable (Active High) or No Connect	**HIGH or No Connect**: Output active at specified frequency **LOW**: Output disabled, high impedance; current consumption is given by I_{DD-OD}
	Pin 2	No Connect	N/A
A	Pin 1	Standby (Active Low) or No Connect	**HIGH or No Connect**: Output active at specified frequency **LOW**: High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$
	Pin 2	No Connect	N/A
K	Pin 1	Output Enable (Active High) or No Connect	**HIGH or No Connect**: Output active at specified frequency **LOW**: Output disabled, high impedance; current consumption is given by I_{DD-OD}
	Pin 2	FSEL(1)	**HIGH**: Output active at $F_{OUT}/2$ **FLOATING**: Output active at F_{OUT} **LOW**: Output active at $F_{OUT}/4$
L	Pin 1	Standby (Active Low) or No Connect	**HIGH or No Connect**: Output active at specified frequency **LOW**: High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$
	Pin 2	FSEL(1)	**HIGH**: Output active at $F_{OUT}/2$ **FLOATING**: Output active at F_{OUT} **LOW**: Output active at $F_{OUT}/4$

(1) F_{OUT} is the output frequency defined in the OPN (refer to Section 4).

In standby mode, all blocks are powered down to provide a maximum current consumption savings equivalent to the standby current provided in the *Current Consumption Characteristics* portion of *Electrical Characteristics*. The return time to the active output clock, or t_{ST-EN}, corresponds to the same as the initial start-up time, or t_{START_UP}.

8.3.3.1 FSEL Implementation

FSEL automatically disables the /2 or /4 divider if the resulting output frequency violates the minimum output frequency of 50MHz. The output frequency does not change if:

- FSEL is tied to VDD and F_{OUT} < 100MHz.
- FSEL is tied to GND and F_{OUT} < 200MHz.
- FSEL state is changed after power-up (a power cycle is required to change the output frequency).
- FSEL is controlled by a digital signal. FSEL needs to be tied to GND, VDD, or left open at all times.

Table 8-2 demonstrates FSEL implementation examples. For 312.5MHz and 200MHz, FSEL divides the output frequency, for 156.25MHz and 100MHz, FSEL only divides down when set to VDD, and for 50MHz, FSEL does not change the output frequency.

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Table 8-2. FSEL Output Frequency Examples

F_{OUT}	FSEL	Output Frequency from FSEL (MHz)
312.5	VDD	156.25
	Hi-Z or NC	312.5
	GND	78.125
156.25	VDD	78.125
	Hi-Z or NC	156.25
	GND	156.25
100	VDD	50
	Hi-Z or NC	100
	GND	100
50	VDD	50
	Hi-Z or NC	50
	GND	50

8.3.4 Output Terminations

The LMK6L-Q1 has different output types: AC-LVPECL, LVDS, HS-LVDS, and LP-HCSL. HS-LVDS and AC-LVPECL are part of the multi-mode driver and have different swing options. LP-HCSL output type has different V_{OH} options. For more information refer to Section 4.

The multi-mode driver can create an output with a common mode of VDD/2 or 1.2V and a customizable swing from 700mVppd to 2Vppd in 100mVppd steps. For AC-LVPECL, the V_{CM} = VDD/2 and the swing can be set from 700mVppd to 2Vppd for 3.3V supply and 700mVppd to 1.5Vppd for 2.5V supply. The multi-mode driver can also generate an LVDS or HS-LVDS output, which has a 1.2V common mode and a customizable swing from 700mVppd to 2Vppd for a 3.3V supply and 700mVppd to 1.6Vppd for a 2.5V supply. At a 1250MHz output, the maximum swing possible is 1.5Vppd for both 2.5V and 3.3V supply. By default, the LVDS driver comes with a 800mVppd typical swing.

Termination schemes for AC-LVPECL, LVDS, and HS-LVDS are shown in Figure 8-2.

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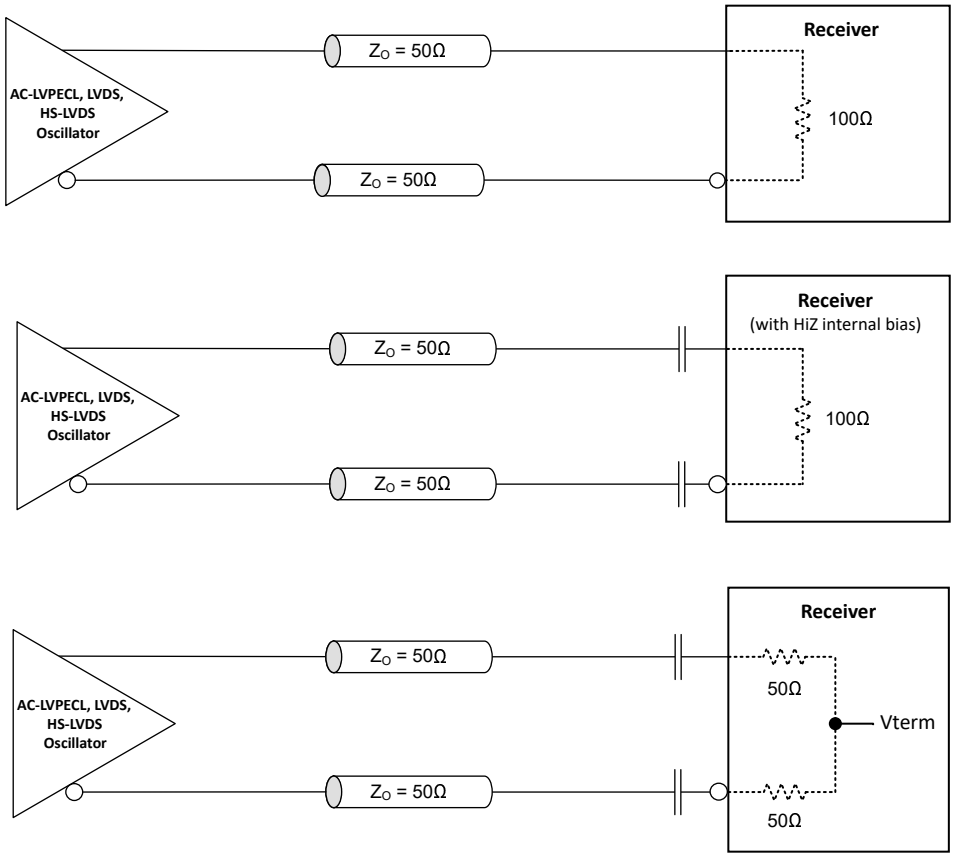

Figure 8-2. AC-LVPECL, LVDS, and HS-LVDS Output Terminations

No changes are required to replace an LVDS oscillator with the LMK6L-Q1. If replacing an LVDS oscillator for an AC-coupled applications and maximum performance is required, use the AC-LVPECL output type. Better performance is achieved with a higher swing, so order the highest swing the receiver can handle. No changes are required when replacing an LVDS oscillator with the AC-LVPECL driver for AC-coupled applications. To replace an LVPECL oscillator refer to Section 8.3.4.1.

The LP-HCSL output driver can have a V_{OH} of 850mV or 750mV typical. No external termination is required as shown in Figure 8-3.

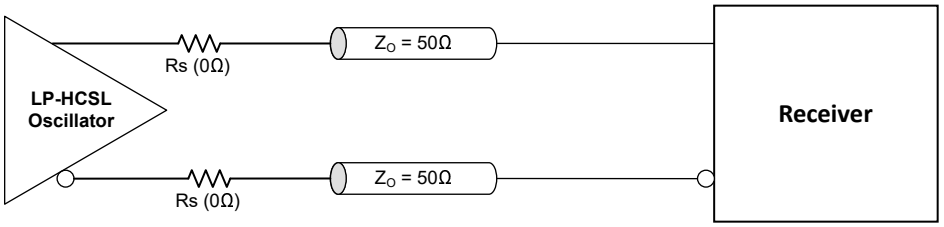

Figure 8-3. LP-HCSL Output Termination

No changes are required to replace a LP-HCSL oscillator with the LMK6L-Q1. To replace a HCSL oscillator with the LMK6L-Q1, refer to Section 8.3.4.2.

8.3.4.1 Replacing a LVPECL oscillator with the LMK6L-Q1

To replace a LVPECL oscillator with the LMK6L-Q1 for a AC-coupled applications,

1. The receiver must have a 100Ω internal termination (if not, one needs to be placed externally).
2. Use the LMK6L-Q1 AC-LVPECL output type.

3. Depopulate any emitter resistors as shown in Figure 8-4.

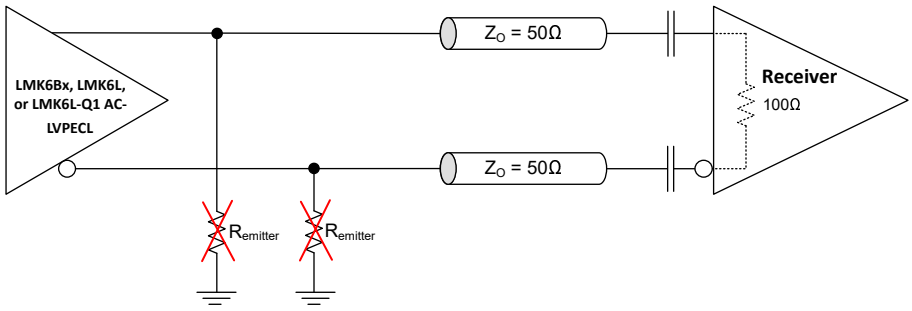

Figure 8-4. Replacing a LVPECL oscillator with the LMK6L-Q1

8.3.4.2 Replacing a HCSL OSC With the LMK6L-Q1

If using the LMK6L-Q1 to replace a HCSL oscillator, follow these steps:

1. Use the LMK6L-Q1 LP-HCSL output type.
2. Depopulate any 50Ω resistors to GND as shown in Figure 8-5.
3. Replace any series resistors with 0Ω as shown in Figure 8-5.

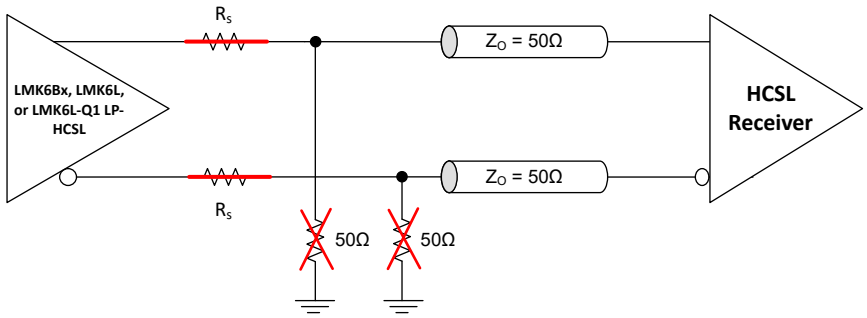

Figure 8-5. Replacing an HCSL Oscillator With the LMK6L-Q1

8.3.5 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the datasheet where packages include this feature.

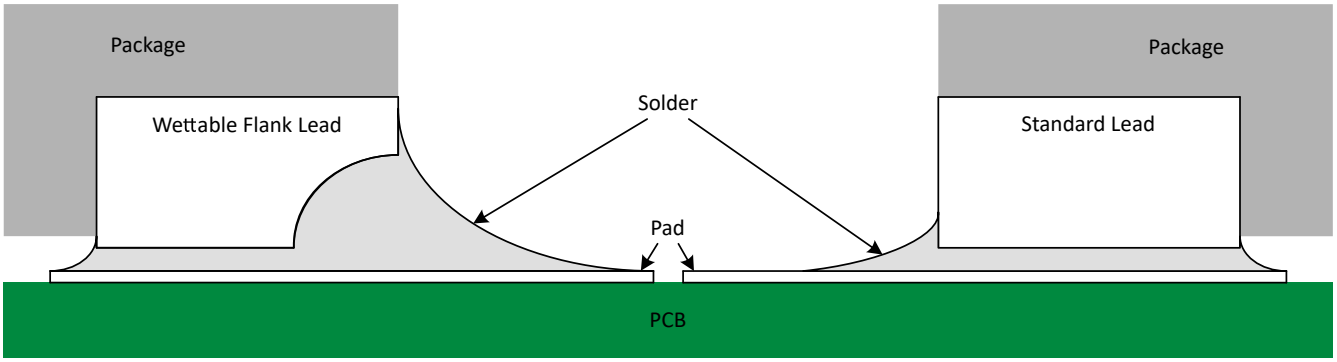

Figure 8-6. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 8-6, a wettable flank can be dimpled or step-cut to

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provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

8.4 Device Functional Modes

The fixed-frequency, factory-programmed LMK6L-Q1 can have different configurations based on the OPN as shown on Section 4. The function pins, pins 1 and 2, can be set to output enable, standby, frequency select, or no connect. Frequency select divides the frequency defined in the OPN by 2 or 4, providing 3 different frequencies from one OPN. For more details, refer to Section 8.3.3.

The LMK6L-Q1 can also come in different differential output types with different swings and common modes (AC-LVPECL, LVDS, HS-LVDS), and LP-HCSL with different V_{OH} options as shown on Section 4. For more details, refer to Section 8.3.4.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK6L-Q1 is an ultra-low jitter, fixed-frequency, factory-programmed, differential BAW oscillator that can be used as a reference clock for several applications. The device supports any output frequency between 50MHz to 1250MHz for the AC-LVPECL, LVDS, and HS-LVDS output types, and 50MHz to 625MHz for the LP-HCSL output type. The LMK6L-Q1 supports 2.375V to 3.465V supply rails (nominal 2.5V and 3.3V).

To drive TI clock buffers with the LMK6L-Q1, refer to Clocking TI Clock Buffers with the LMK6Bx application note.

9.2 Typical Application

The LMK6L-Q1 is an ultra low jitter differential oscillator, meeting the PCIE Gen 7 standard, targeting high-performance automotive systems including ADAS and IVI SoC, in-vehicle 10/40/100 Gbps Ethernet, Radar, and Lidar. Figure 9-1 shows an example of a typical application using the LMK6L-Q1 as the reference clock for an SoC.

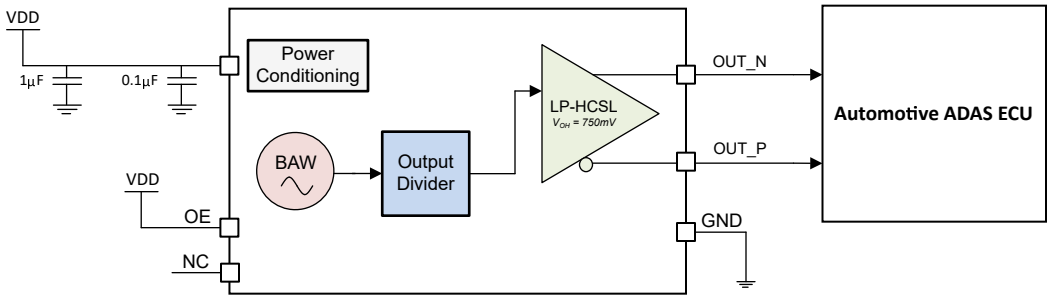

Figure 9-1. LMK6L-Q1 Used as a Reference Clock for an Automotive SoC

For a layout example of the LMK6L-Q1 and bypass capacitor and AC-coupling capacitor value recommendations, refer to Section 9.4.2. See Section 8.3.4 for output type termination and biasing.

9.2.1 Design Requirements

The LMK6L-Q1 is a fixed-frequency oscillator with no programming needed. Make sure to follow the recommended termination options as described in Section 8.3.4 and see Section 8.3.3 to understand pin 1 and 2 function. Order the part number based on Section 4 as per your requirements. Also, make sure to follow Section 9.3 and Section 9.4.1 to maximize the performance of the LMK6L-Q1.

9.2.2 Detailed Design Procedure

When designing with the LMK6L-Q1, the first step is to select the correct configuration based on your requirements. The OPN selected determines the output type, pins 1 and 2 functions, output frequency, and package type. Refer to Section 4 for more details.

The LMK6L-Q1 differential oscillator has AC-LVPECL, LVDS, HS-LVDS, and LP-HCSL output type options. Use the proper AC or DC termination based on the application requirement as shown in Section 8.3.4. The LMK6L-Q1 has output enable or standby options for pins 1 and frequency select (FSEL) option for pin 2. Refer to Section 8.3.3 for more information on each pin, function, and FSEL to determine the desired configuration. The LMK6L-Q1 has integrated LDOs and excellent PSRR performance as shown in *Electrical Characteristics*.

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Add a 0.1µF and 1µF to the VDD pin to achieve best performance. Follow Section 9.3 for more power supply pin recommendations and Section 9.4 for best board layout practices when designing with the LMK6L-Q1.

9.2.3 Application Curves

9.2.3.1 LVDS Phase Noise Curves

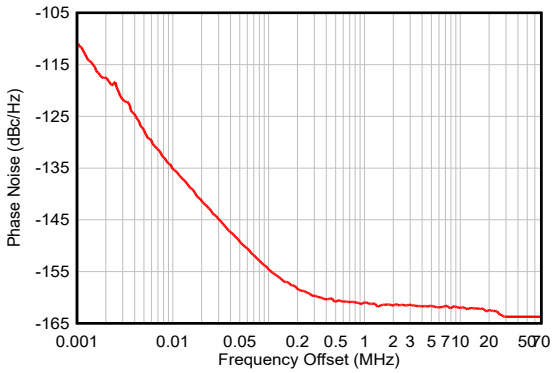


Figure 9-2. 156.25MHz LVDS, 25°C, 3.3V, 800mVppd, 60.5fs RMS jitter (12kHz to 20MHz)

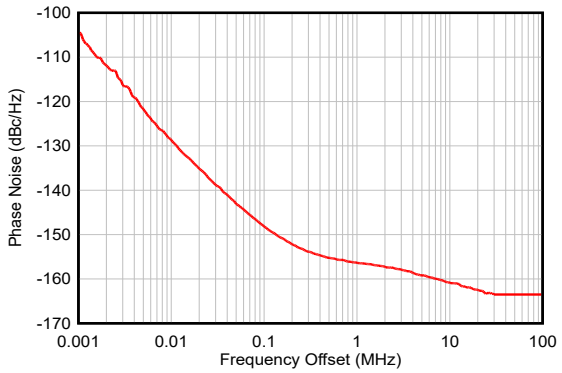


Figure 9-3. 312.5MHz LVDS, 25°C, 3.3V, 800mVppd, 46.6fs RMS jitter (12kHz to 20MHz)

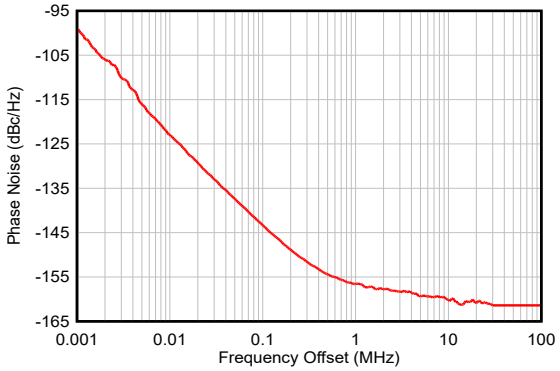
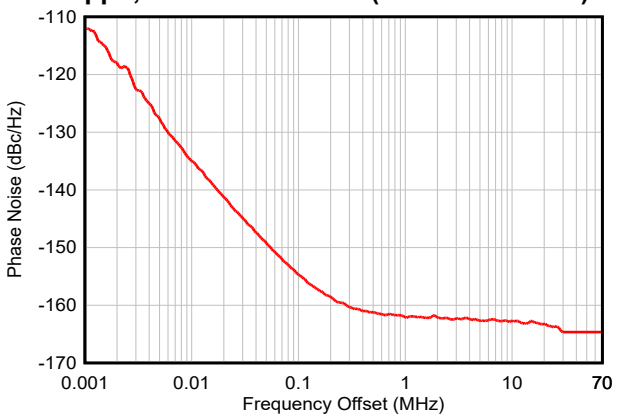


Figure 9-4. 625MHz LVDS, 25°C, 3.3V, 800mVppd, 32.3fs RMS jitter (12kHz to 20MHz)

9.2.3.2 HS-LVDS 1.2Vppd Phase Noise Curves

Figure 9-5. 156.25MHz, HS-LVDS, 25°C, 3.3V, 1.2Vppd, 56.3fs RMS Jitter (12kHz to 20MHz)



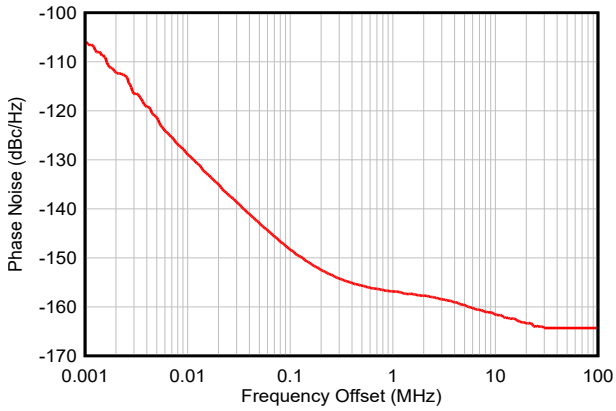


Figure 9-6. 312.5MHz, HS-LVDS, 25°C, 3.3V, 1.2Vppd, 44.4fs RMS Jitter (12kHz to 20MHz)

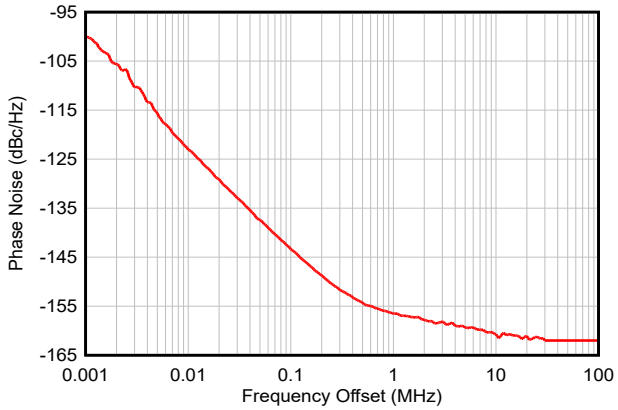


Figure 9-7. 625MHz, HS-LVDS, 25°C, 3.3V, 1.2Vppd, 31.8fs RMS Jitter (12kHz to 20MHz)

9.2.3.3 AC-LVPECL 1.2Vppd Phase Noise Curves

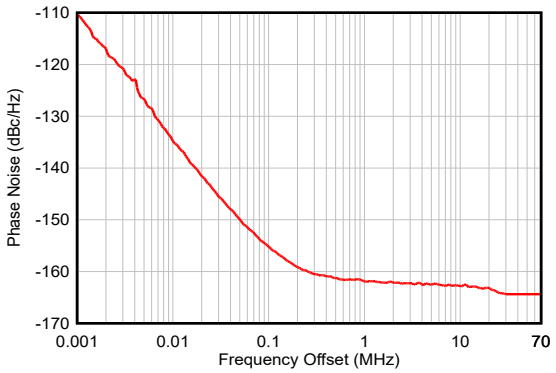


Figure 9-8. 156.25MHz, AC-LVPECL 1.2Vppd, 25°C, 3.3V, 57.0fs RMS Jitter (12kHz to 20MHz)

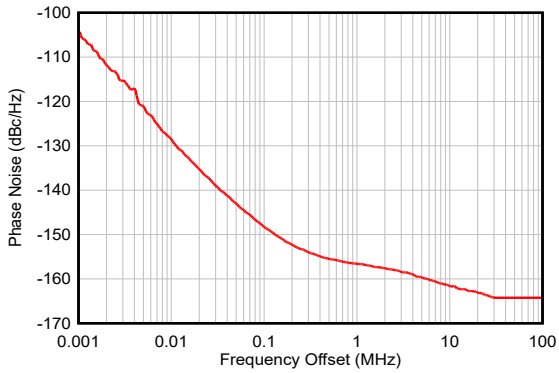


Figure 9-9. 312.5MHz AC-LVPECL 1.2Vppd, 25°C, 3.3V, 45.0fs RMS Jitter (12kHz to 20MHz)

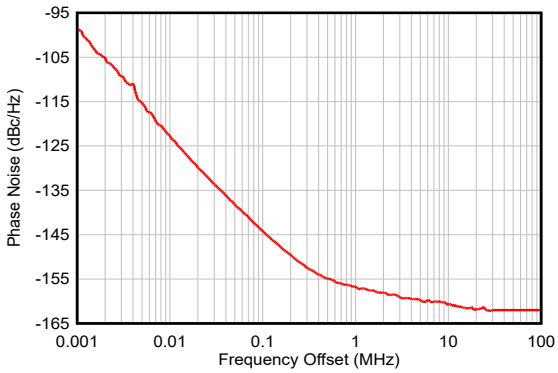


Figure 9-10. 625MHz AC-LVPECL 1.2Vppd, 25°C, 3.3V, 32.8fs RMS Jitter (12kHz to 20MHz)

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9.2.3.4 LP-HCSL Phase Noise Curves

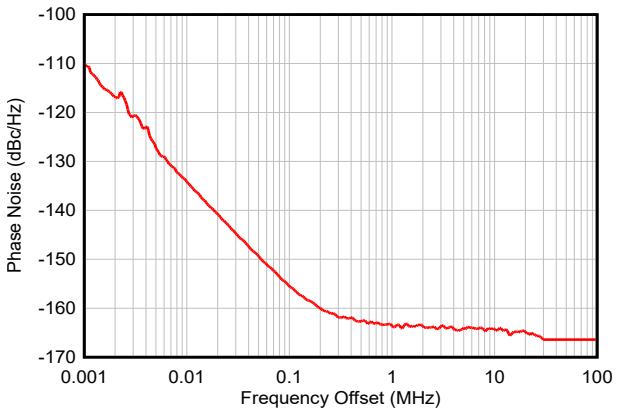


Figure 9-11. 156.25MHz LP-HCSL, 25°C, 3.3V, V_{OH} = 750mV, 53.3fs RMS Jitter (12kHz to 20MHz)

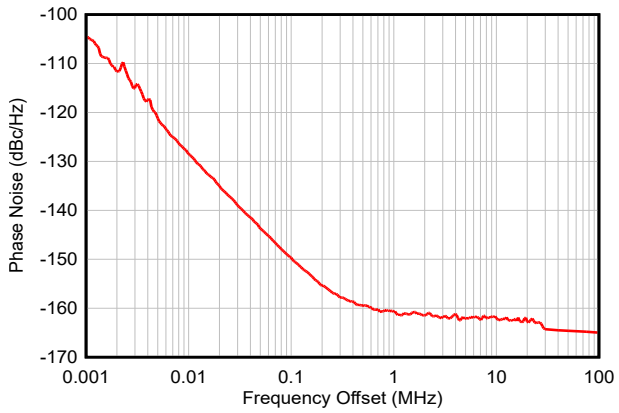


Figure 9-12. 312.5MHz LP-HCSL, 25°C, 3.3V, V_{OH} = 750mV, 41.0fs RMS Jitter (12kHz to 20MHz)

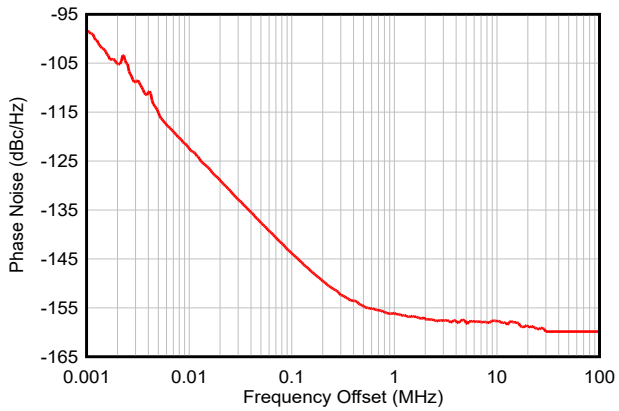


Figure 9-13. 625MHz LP-HCSL, 25°C, 3.3V, V_{OH} = 750mV, 38.3fs RMS Jitter (12kHz to 20MHz)

9.3 Power Supply Recommendations

For the best electrical performance of the LMK6L-Q1, TI recommends using 0.1µF and 1µF capacitor on the device power supply bypass network. Place these capacitors as close as possible to the supply pins. TI also recommends using component side mounting of the power supply bypass capacitors and use 0201 body size for the 0.1µF capacitor and 0603 body size for the 1µF capacitor to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

9.4 Layout

9.4.1 Layout Guidelines

The LMK6L-Q1 can operate up to 1250MHz. To optimize the oscillator's performance, make sure to follow industry-standard high-speed layout guidelines as explained in High-Speed Layout Guidelines. To summarize,

- Minimize long stubs that create antenna effects and deteriorate output performance.
- Impedance match the differential output traces to 50Ω single-ended or 100Ω differential to eliminate reflections.
- Make the output traces as short as possible and of equal length to achieve maximum performance.

Section 9.4.1.1 discusses on providing thermal reliability for good thermal and electrical performance. Section 9.4.1.2 discusses how to maintain signal integrity of the entire system by implementing a good solder reflow profile.

9.4.1.1 Providing Thermal Reliability

The LMK6L-Q1 is a high-performance device. Therefore, pay careful attention to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more to maximize thermal dissipation out of the package.

Equation 1 describes the relationship between the PCB temperature around the LMK6L-Q1 and the junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \quad (1)$$

where

- T_B: PCB temperature around the LMK6L-Q1
- T_J: Junction temperature of LMK6L-Q1
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK6L-Q1 (refer to the *Thermal Information* tables in the *Specifications* section for this information)
- P: On-chip power dissipation of LMK6L-Q1

9.4.1.2 Recommended Solder Reflow Profile

TI recommends following the recommendations provided by the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Processing the LMK6L-Q1 with the lowest peak temperature possible is preferable while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile depends on several factors including maximum peak temperature as rated on the MSL label, board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, solder manufacture recommended profile, and capability of the reflow equipment as confirmed by the SMT assembly operation.

ADVANCE INFORMATION

9.4.2 Layout Example

Figure 9-14 through Figure 9-18 show the printed circuit board (PCB) layout examples as done on the evaluation module (EVM) for the LMK6L-Q1.

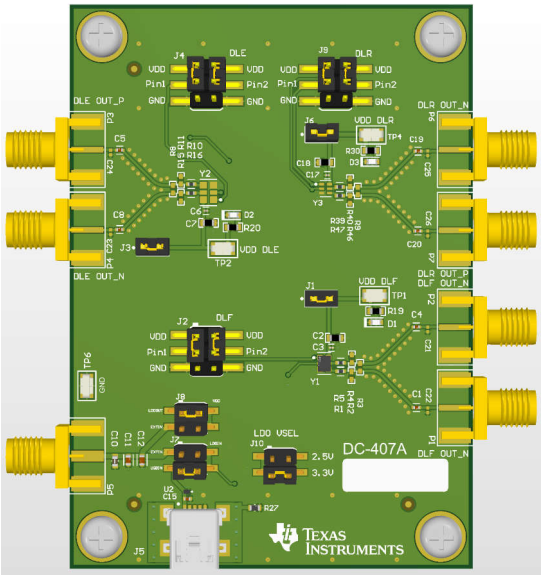


Figure 9-14. PCB Layout Example From LMK6LEVM

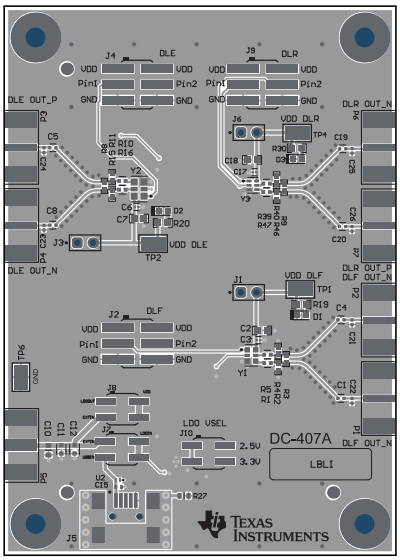


Figure 9-15. PCB Layout Example From LMK6LEVM - Top Layer

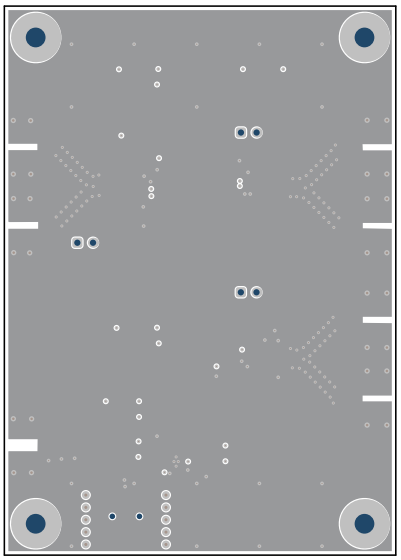


Figure 9-16. PCB Layout Example From LMK6LEVM - Ground Layer

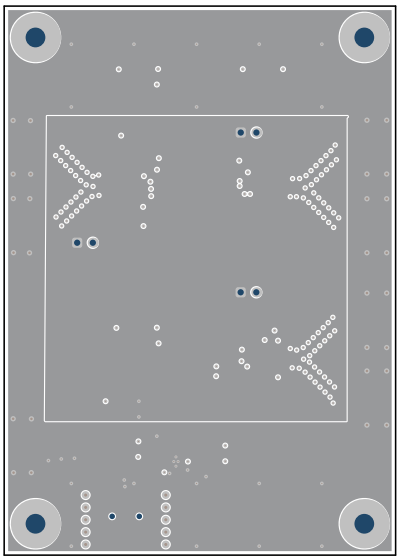


Figure 9-17. PCB Layout Example From LMK6LEVM - Power Layer

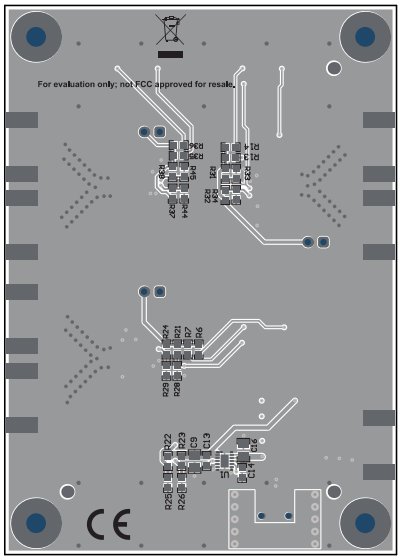


Figure 9-18. PCB Layout Example From LMK6LEVM - Bottom Layer

ADVANCE INFORMATION

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMK6LEVM User's Guide*
- Texas Instruments, *Standalone BAW Oscillators Advantages Over Quartz Oscillators*, application note
- Texas Instruments, *Vibration and Mechanical Shock Performance of TI's BAW Oscillators*, application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

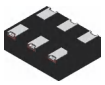
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

ADVANCE INFORMATION

12.1 Mechanical Data

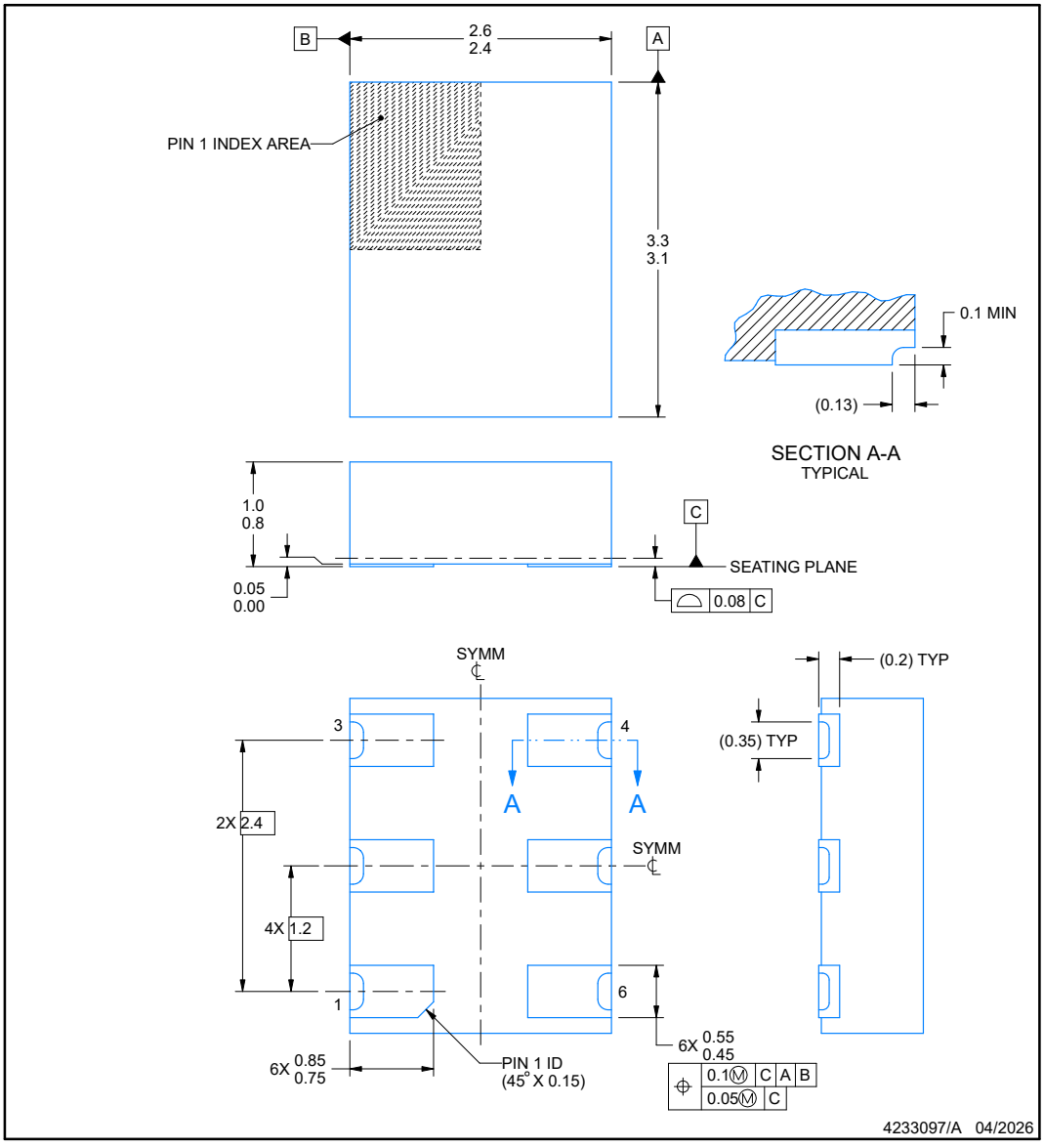
DLE0006C



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

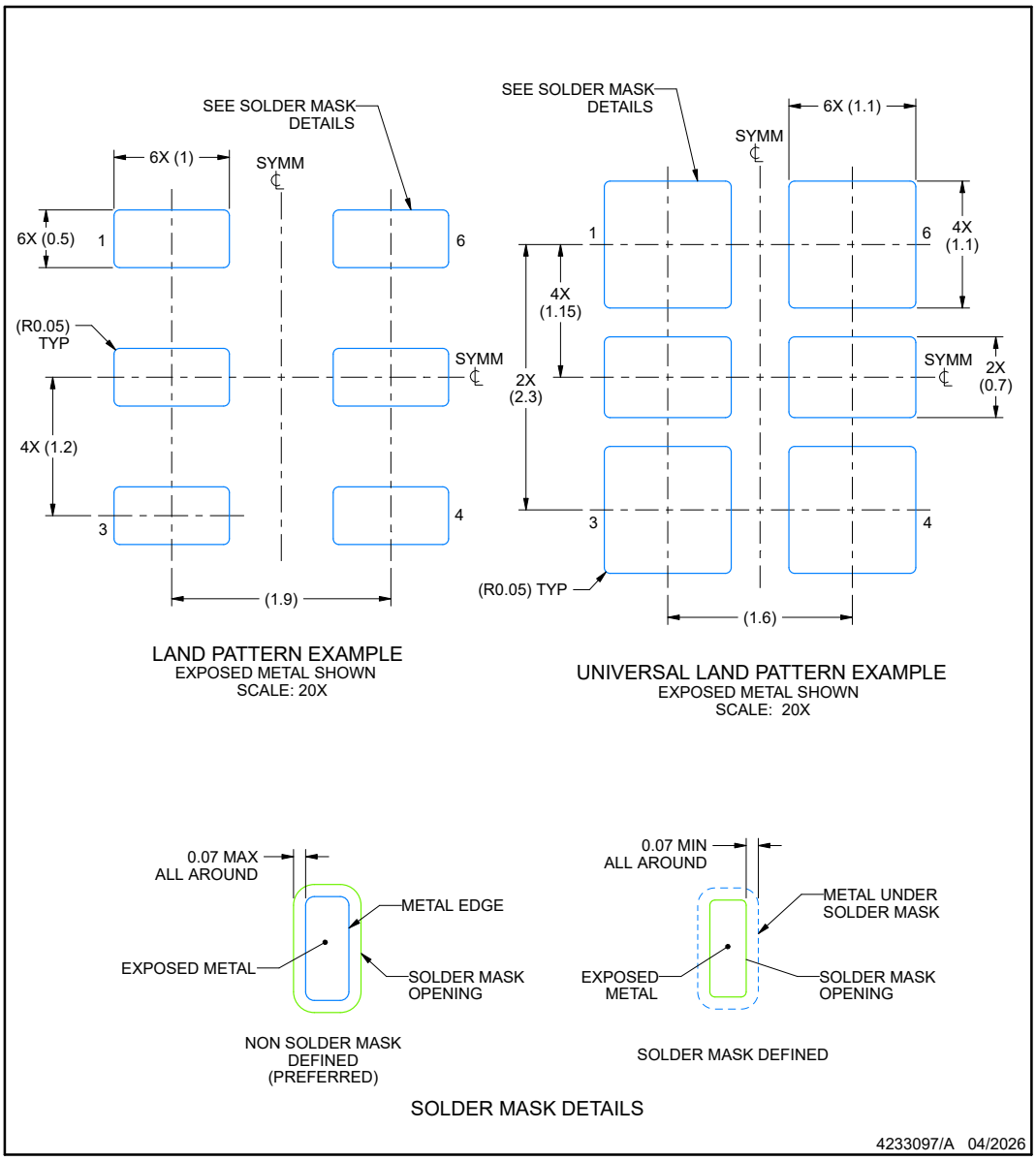
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DLE0006C

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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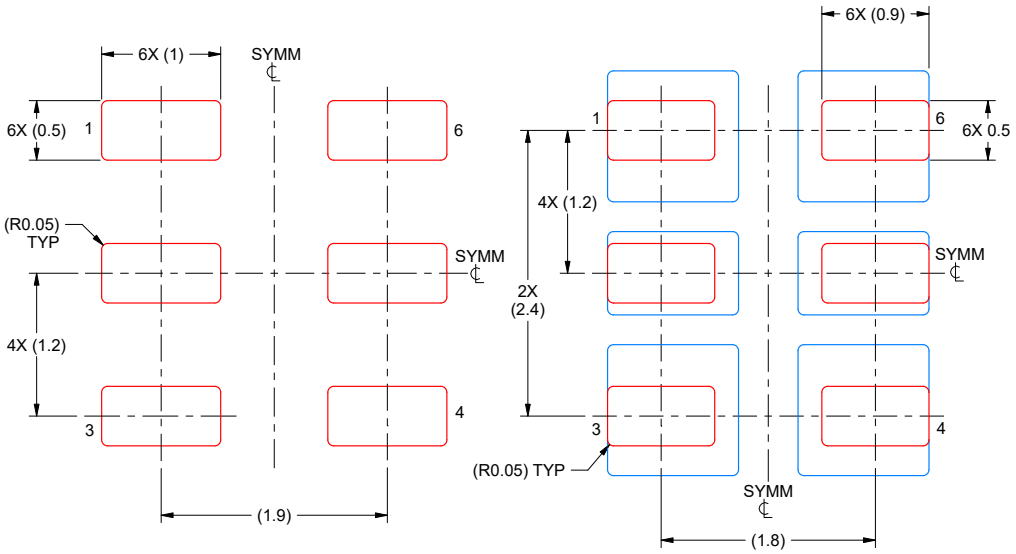
EXAMPLE STENCIL DESIGN

DLE0006C — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4233097/A 04/2026

NOTES: (continued)

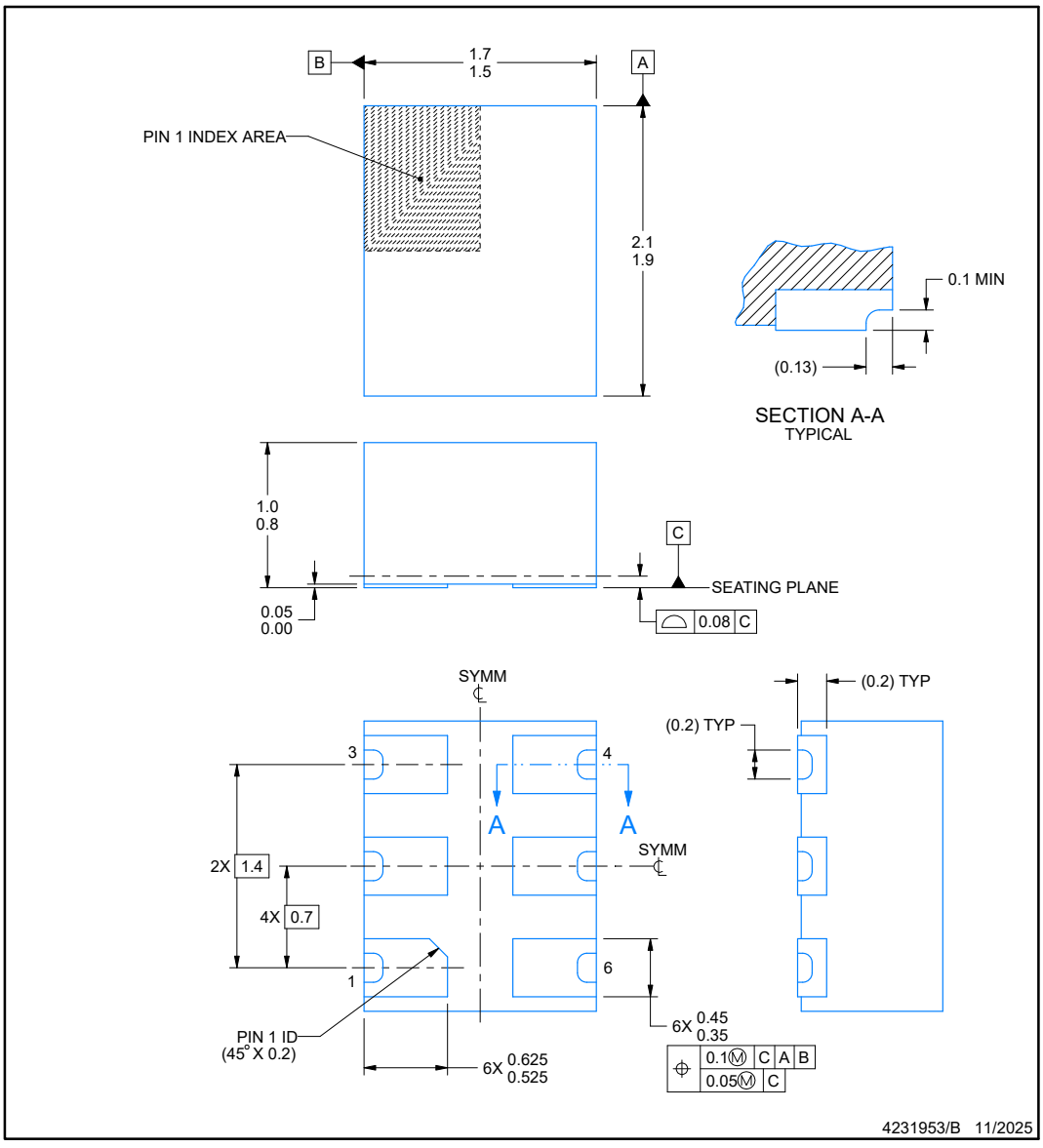
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLR0006B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

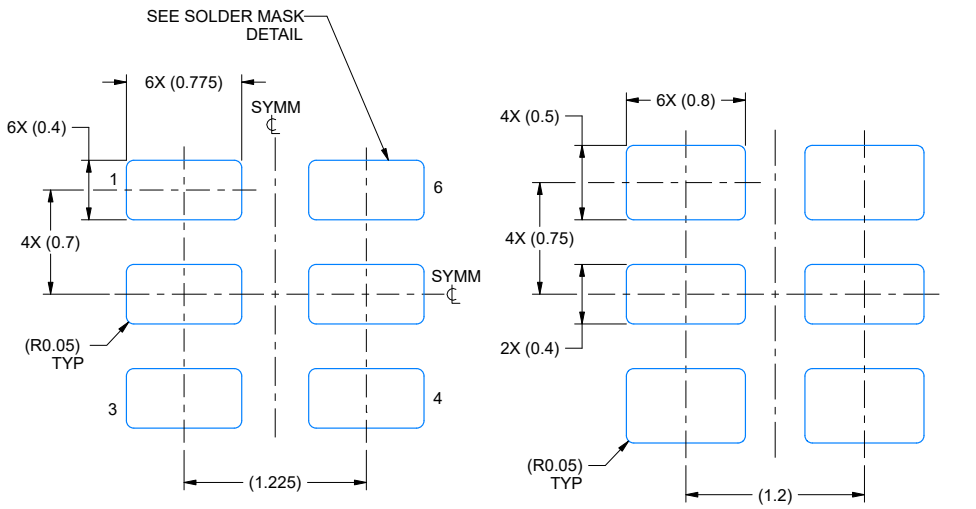
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

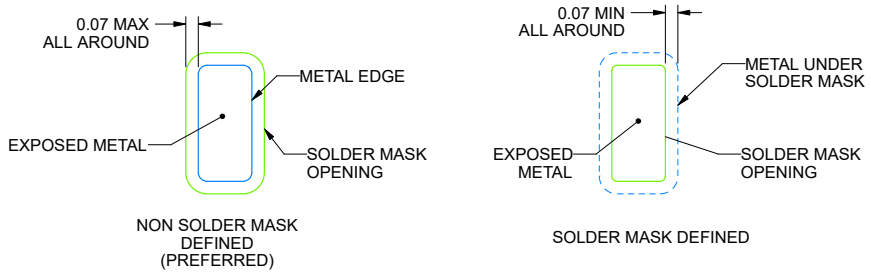
DLR0006B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

UNIVERSAL LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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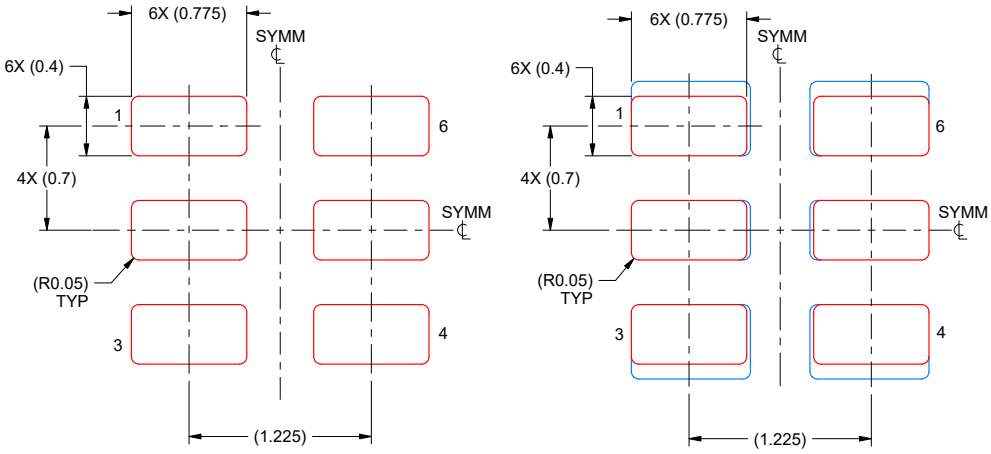
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DLR0006B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PMK6LHE15625DLERQ1	Active	Preproduction	null (null) |	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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