LMKDB12xx PCIe Gen 1 to Gen 7 Ultra Low Jitter 2 Input Clock MUX

1 Features

- LP-HCSL clock MUX that support:
  - PCIe Gen 1 to Gen 7
  - CC (Common Clock) and IR (Independent Reference) PCIe architectures
  - Input clock with or without SSC
- DB2000QL compliant:
  - All devices meet DB2000QL specifications
- Extremely low additive jitter:
  - 31fs maximum 12kHz to 20MHz RMS additive jitter at 156.25MHz
  - 13fs maximum additive jitter for PCIe Gen 4
  - 5fs maximum additive jitter for PCIe Gen 5
  - 3fs maximum additive jitter for PCIe Gen 6
  - 2.1fs maximum additive jitter for PCIe Gen 7
- Fail-safe input
- Flexible power-up sequence
- Automatic output disable
- Individual output enable
- SBI (Side Band Interface) for high-speed output enable or disable
- LOS (Loss of Signal) input detection
- 85Ω or 100Ω output impedance
- 1.8V / 3.3V ± 10% power supply
- –40°C to 105°C ambient temperature

2 Applications

- High Performance Computing
- Server Motherboard
- NIC/SmartNIC
- Hardware Accelerator

3 Description

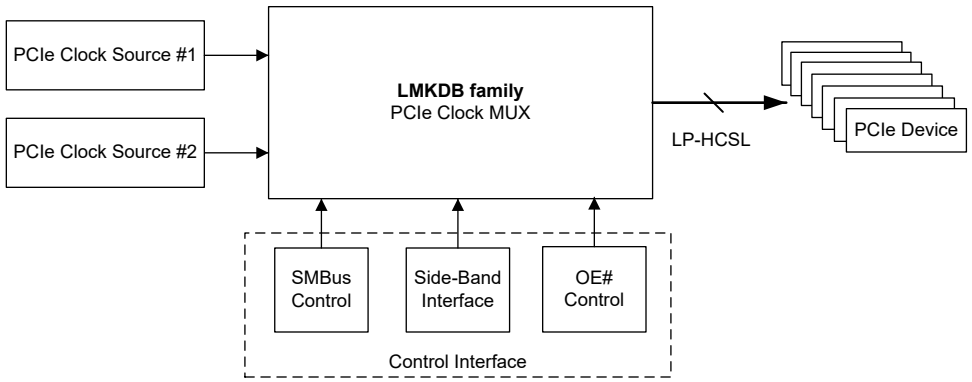
The LMKDB devices are a family of extremely-low-jitter LP-HCSL clock muxes that support PCIe Gen 1 to Gen 7 and are DB2000QL compliant. The devices provide flexible power-up sequence, fail-safe inputs, individual output enable and disable pins, loss of input signal (LOS) detection and automatic output disable features, as well as excellent power supply noise rejection performance.

Both 1.8V and 3.3V power supply voltages are supported.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMKDB1204	REX (VQFN, 28)	4mm × 4mm
LMKDB1202	REY (VQFN, 20)	3mm × 3mm

(1) For all available packages, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Device Comparison

Table 4-1. Device Comparison

PART NUMBER	Type	Input	Output	Output Impedance	Features
LMKDB1120Z85	Buffer	1	20	85Ω	All inputs fail-safe
LMKDB1120FS85	Buffer	1	20	85Ω	All inputs and outputs fail-safe
LMKDB1120Z100	Buffer	1	20	100Ω	All inputs fail-safe
LMKDB1116Z85 (1)	Buffer	1	16	85Ω	All inputs fail-safe
LMKDB1116Z100 (1)	Buffer	1	16	100Ω	All inputs fail-safe
LMKDB1113Z85 (1)	Buffer	1	13	85Ω	All inputs fail-safe
LMKDB1113Z100 (1)	Buffer	1	13	100Ω	All inputs fail-safe
LMKDB1112Z85 (1)	Buffer	1	12	85Ω	All inputs fail-safe
LMKDB1112Z100 (1)	Buffer	1	12	100Ω	All inputs fail-safe
LMKDB1108Z85	Buffer	1	8	85Ω	All inputs fail-safe
LMKDB1108FS85	Buffer	1	8	85Ω	All inputs and outputs fail-safe
LMKDB1108Z100	Buffer	1	8	100Ω	All inputs fail-safe
LMKDB1104Z85	Buffer	1	4	85Ω	All inputs fail-safe
LMKDB1104FS85	Buffer	1	4	85Ω	All inputs and outputs fail-safe
LMKDB1104Z100	Buffer	1	4	100Ω	All inputs fail-safe
LMKDB1102	Buffer	1	2	85Ω or 100Ω Selectable	All inputs fail-safe
LMKDB1216 (1)	Mux	2	16	85Ω or 100Ω Selectable	All inputs fail-safe
LMKDB1208 (1)	Mux	2	8	85Ω or 100Ω Selectable	All inputs fail-safe
LMKDB1204	Mux	2	4	85Ω or 100Ω Selectable	All inputs fail-safe
LMKDB1202	Mux	2	2	85Ω or 100Ω Selectable	All inputs fail-safe

(1) Preview only. Contact TI for more details.

5 Pin Configuration and Functions

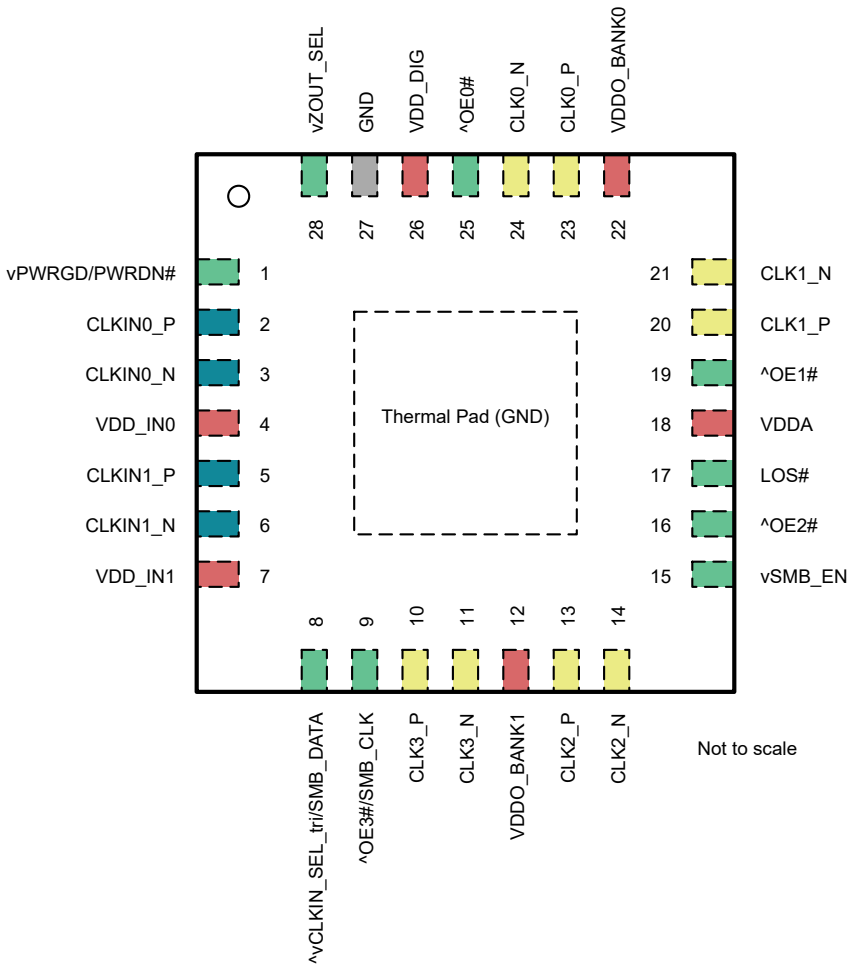


Figure 5-1. LMKDB1204 4mm × 4mm VQFN Package 28 Pin Top View

Legend		
CLOCK INPUTS	CLOCK OUTPUTS	POWER
GND	LOGIC CONTROLS / STATUS	NO CONNECT

Table 5-1. LMKDB1204 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME[2] [3]	NO.		
CLOCK INPUTS			
CLKIN0_P	2	I	Differential clock input 0.
CLKIN0_N	3	I	

Table 5-1. LMKDB1204 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME[2] [3]	NO.		
CLKIN1_P	5	I	Differential clock input 1.
CLKIN1_N	6	I	
CLOCK OUTPUTS			
CLK0_P	23	O	LP-HCSL differential clock output 0. No connect if unused.
CLK0_N	24	O	
CLK1_P	20	O	LP-HCSL differential clock output 1. No connect if unused.
CLK1_N	21	O	
CLK2_P	13	O	LP-HCSL differential clock output 2. No connect if unused.
CLK2_N	14	O	
CLK3_P	10	O	LP-HCSL differential clock output 0. No connect if unused.
CLK3_N	11	O	
POWER			
VDDA	18	P	Analog power supply. Additional power supply filtering is recommended. See Section 10.3 for details.
VDD_IN0	4	P	Power supply for CLKIN0
VDD_IN1	7	P	Power supply for CLKIN1
VDD_DIG	26	P	Power supply for digital
VDDO_BANK1	12	P	Power supply for output bank 1 (OUT4 to OUT7).
VDDO_BANK0	22	P	Power supply for output bank 0 (OUT0 to OUT3).
GND	27	G	Device Ground.
Thermal Pad (GND)	Pad	G	Device Ground, Thermal pad.
LOGIC CONTROLS / STATUS			
^OE0#	25	I	Active low input to control CLK0. Internal pullup resistor. 0 = Output Active, 1 = Output Inactive
^OE1#	19	I	Active low input to control CLK1. Internal pullup resistor. 0 = Output Active, 1 = Output Inactive
^OE2#	16	I	Active low input to control CLK2. Internal pullup resistor. 0 = Output Active, 1 = Output Inactive
^OE3#/SMB_CLK	9	I	Output Enable for CLK3 Active Low/SMBus Clock. Internal pullup resistor. Functionality is decided by the state of pin 15 (SMB_EN) at power-up. When used as SMBus Clock pin, external pullup resistor is required. No connect if unused.
^vCLKIN_SEL_tri/ SMB_DATA	8	I	3-Level Clock Input Select/SMBus Data. Internal pullup and pulldown resistor. Functionality is decided by the state of pin 15 (SMB_EN) at power-up. When used as CLKIN_SEL_tri pin: Low = CLKIN0 goes to all outputs Mid = CLKIN0 goes to Bank 0, CLKIN1 goes to Bank 1 High = CLKIN1 goes to all outputs When used as SMBus Data pin, external pullup resistor is required.
vPWRGD/PWRDN#	1	I	Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. On the first low-to-high transition, functions as Power Good pin which starts up the device On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. Low = power-down mode High = normal operation mode
vSMB_EN	15	I	SMBus Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. Low at power-up = SMBus disabled. Pin 8 is CLKIN_SEL_tri and Pin 9 is OE3#. High at power-up = SMBus enabled. Pin 8 is SMB_DATA and Pin 9 is SMB_CLK.

Table 5-1. LMKDB1204 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME[2] [3]	NO.		
vZOUT_SEL	28	I	LP-HCSL differential clock output impedance select. Internal pulldown resistor. Low = 85Ω. High = 100Ω.
LOS#	17	O	Loss of Input Clock Signal Active Low/No Connect. Open drain. Requires external pullup resistor. Low = Invalid input clock. High = Valid input clock.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect
(2) Pins with a "^" prefix have an internal pullup resistor. Pins with a "v" prefix have an internal pulldown resistor. Pins with a "^v" have an internal pullup resistor and an internal pulldown resistor so that mid level is selected when the pin is left floating. Pins with "^/v" have an internal pullup or pulldown based on selected function.
(3) The "#" symbol indicates active low.

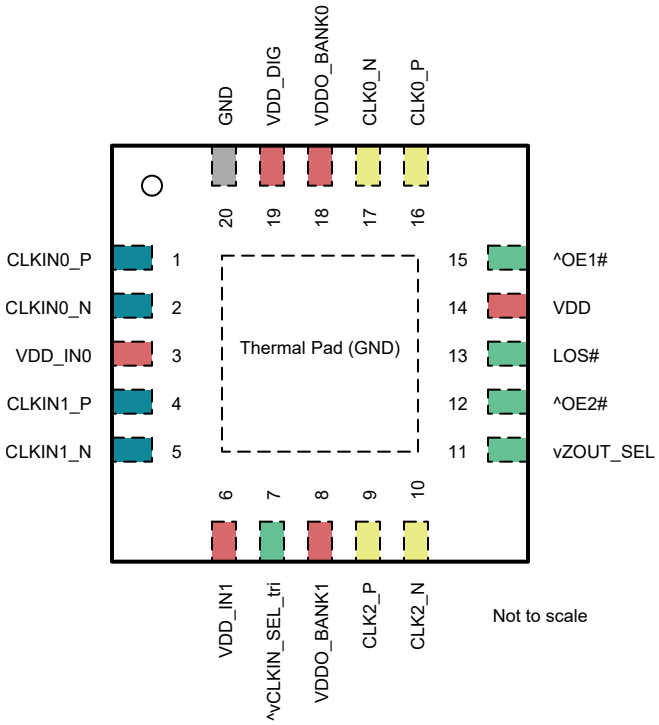


Figure 5-2. LMKDB1202 3mm × 3mm VQFN Package 20 Pin Top View

Legend		
CLOCK INPUTS	CLOCK OUTPUTS	POWER
GND	LOGIC CONTROLS / STATUS	NO CONNECT

Table 5-2. LMKDB1202 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME[2] [3]	NO.		
CLOCK INPUTS			
CLKIN0_P	1	I	Differential clock input 0.
CLKIN0_N	2	I	
CLKIN1_P	4	I	Differential clock input 1.
CLKIN1_N	5	I	
CLOCK OUTPUTS			
CLK1_P	16	O	LP-HCSL differential clock output 1. No connect if unused.
CLK1_N	17	O	
CLK2_P	9	O	LP-HCSL differential clock output 2. No connect if unused.
CLK2_N	10	O	
POWER			
VDD	14	P	Analog power supply. Additional power supply filtering is recommended. See Section 10.3 for details.
VDD_IN0	3	P	Power supply for CLKIN0
VDD_IN1	6	P	Power supply for CLKIN1
VDD_DIG	19	P	Power supply for digital

Table 5-2. LMKDB1202 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME[2] [3]	NO.		
VDDO_BANK1	8	P	Power supply for output bank 1.
VDDO_BANK0	18	P	Power supply for output bank 0.
GND	20	G	Device Ground.
Thermal Pad (GND)	Pad	G	Device Ground, Thermal pad.
LOGIC CONTROLS / STATUS			
^OE1#	15	I	Active low input to control CLK1. Internal pullup resistor. 0 = Output Active, 1 = Output Inactive
^OE2#	12	I	Active low input to control CLK2. Internal pullup resistor. 0 = Output Active, 1 = Output Inactive
^vCLKIN_SEL_tri	7	I	3-Level clock input select. Internal pullup and pulldown resistor. Low = CLKIN0 goes to all outputs Mid = CLKIN0 goes to Bank 0, CLKIN1 goes to Bank 1 High = CLKIN1 goes to all outputs
vZOUT_SEL	11	I	LP-HCSL differential clock output impedance select. Internal pulldown resistor. Low = 85Ω. High = 100Ω.
LOS#	13	O	Loss of Input Clock Signal Active Low/No Connect. Open drain. Requires external pullup resistor. Low = Invalid input clock. High = Valid input clock.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect
(2) Pins with a "^" prefix have an internal pullup resistor. Pins with a "v" prefix have an internal pulldown resistor. Pins with a "^v" have an internal pullup resistor and an internal pulldown resistor so that mid level is selected when the pin is left floating. Pins with "^/v" have an internal pullup or pulldown based on selected function.
(3) The "#" symbol indicates active low.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DDx}	Supply voltage on any VDD pin	–0.3	3.63	V
V_{IN}	Input voltage on CLKIN and digital input pins	–0.3	3.63	V
I_{OUT}	Output current - continuous (CLKOUT)		30	mA
	Output current - continuous (SMB_DATA, SBI_OUT)		25	mA
	Output current - surge (CLKOUT)		60	mA
	Output current - surge (SMB_DATA, SBI_OUT)		50	mA
T_S	Storage temperature	–65	150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature			125	°C
T_A	Ambient temperature	–40		105	°C
V_{DD}	Power supply voltage	2.97	3.3	3.6	V
		1.71	1.8	1.89	V
V_{IN}	Input voltage on CLKIN and digital input pins	–0.3		3.6	V
t_{ramp}	Power ramping time	0.05		5	ms

6.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
REX0028 (VQFN)	28	44.2	36.8	20.6	0.9	20.6	5.9	°C/W
REY0020 (VQFN)	20	46.4	50.4	20.3	1.1	20.3	6.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK INPUT REQUIREMENTS					

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN,\ cross}$	Clock input crossing point voltage		100		1400	mV
DC_{IN}	Clock input duty cycle		45		55	%
V_{IN}	Differential clock input amplitude (half of differential peak-peak voltage)	$f_0 \le 300$ MHz	200		2000	mV
		300 MHz < $f_0 \le 400$ MHz	250		2000	mV
dV_{IN}/dt	Clock input slew rate	Measured from –150 mV to +150 mV on the differential waveform	0.6			V/ns
CLOCK OUTPUT CHARACTERISTICS - 100 MHz 85 Ω PCIe						
$V_{OH,AC}$	Output voltage high	DB2000QL AC test load[6]	670		820	mV
$V_{OL,AC}$	Output voltage low		–100		100	mV
$V_{max,AC}$	Output max voltage (including overshoot)		670		920	mV
$V_{min,AC}$	Output min voltage (including undershoot)		–100		100	mV
$V_{OH,DC}$	Output voltage high with DC test load	DB2000QL DC test load[2]	225		270	mV
$V_{OL,DC}$	Output voltage low with DC test load		10		150	mV
$V_{ovs,DC}$	Output overshoot voltage with DC test load				75	mV
$V_{uds,DC}$	Output undershoot voltage with DC test load		–75			mV
Z_{diff}	Differential output impedance	Measured at V_{OL}/V_{OH}, V_{DD} = 3.3 V	80.75	85	89.25	Ω
		Measured at V_{OL}/V_{OH}, V_{DD} = 1.8 V	81	85	90	Ω
$Z_{diff-crossing}$	Differential output impedance - crossing	Measured during transition	68	85	102	Ω
dV/dt	Output slew rate	Measured from –150 mV to +150 mV on the differential waveform. Lowest slew rate[6] [7]	1.5		2.2	V/ns
		Measured from –150 mV to +150 mV on the differential waveform. Low slew rate[6] [7]	1.8		2.6	V/ns
		Measured from –150 mV to +150 mV on the differential waveform. High slew rate (default)[6] [7]	2		2.9	V/ns
		Measured from –150 mV to +150 mV on the differential waveform. Highest slew rate[6] [7]	2.4		4	V/ns
$\Delta dV/dt$	Rising edge rate to falling edge rate matching	DB2000QL AC test load[6]			10	%
DCD	Duty cycle distortion	Measured on the differential waveform. Input duty cycle = 50%[6]	–1		1	%
$V_{cross,AC}$	Absolute crossing point voltage	DB2000QL AC test load[6]	250		550	mV
$V_{cross,DC}$	Absolute crossing point voltage	DB2000QL DC test load[2]	130		200	mV
$\Delta V_{cross,AC}$	Variation of V_{cross} over all clock edges	DB2000QL AC test load[6]			140	mV
$\Delta V_{cross-DC}$	Variation of V_{cross} over all clock edges	DB2000QL DC test load[2]			35	mV
$\lvert V_{RB} \rvert$	Absolute value of ring back voltage as defined in PCIe	DB2000QL AC test load[6]	100			mV
t_{stable}	Time before V_{RB} is allowed	DB2000QL AC test load[6]	500			ps
CLOCK OUTPUT CHARACTERISTICS - 100 MHz 100 Ω PCIe						
V_{max}	Output voltage high including overshoot	PCIe AC test load[1]	670		920	mV
V_{min}	Output voltage low including undershoot	PCIe AC test load[1]	–100		100	mV

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage high	PCIe AC test load(1)	670		820	mV
V_{OL}	Output voltage low	PCIe AC test load(1)	–100		100	mV
Z_{diff}	Differential output DC impedance	V_{DD} = 3.3 V	95	100	105	Ω
		V_{DD} = 1.8 V	95	100	105	Ω
dV/dt	Output slew rate	Measured from –150 mV to +150 mV on the differential waveform. Lowest slew rate(1) (7)	1.5		2.2	V/ns
		Measured from –150 mV to +150 mV on the differential waveform. Low slew rate(1) (7)	1.8		2.6	V/ns
		Measured from –150 mV to +150 mV on the differential waveform. High slew rate(1) (7)	2		2.9	V/ns
		Measured from –150 mV to +150 mV on the differential waveform. Highest slew rate(1) (7)	2.4		4	V/ns
ΔdV/dt	Rising edge rate to falling edge rate matching	PCIe AC test load(1)			10	%
DCD	Duty cycle distortion	Measured on the differential waveform. Input duty cycle = 50%(1)	–1		1	%
V_{cross}	Absolute crossing point voltage	PCIe AC test load(1)	250		550	mV
ΔV_{cross}	Variation of V_{cross} over all clock edges	PCIe AC test load(1)			140	mV
$\lvert V_{RB} \rvert$	Absolute value of ring back voltage as defined in PCIe	PCIe AC test load(1)	100			mV
t_{stable}	Time before V_{RB} is allowed	PCIe AC test load(1)	500			ps
CLOCK OUTPUT CHARACTERISTICS - non-PCIe						
V_{OH}	Output voltage high	Output swing programmed to 800 mV. f_0 = 156.25 MHz or 312.5 MHz	720		880	mV
V_{OL}	Output voltage low		–120		120	mV
V_{OH}	Output voltage high	Output swing programmed to 900 mV. f_0 = 156.25 MHz or 312.5 MHz	780		980	mV
V_{OL}	Output voltage low		–120		120	mV
t_R, t_F	Rise/fall time on single-ended waveform, 20% to 80%	Output swing programmed to 800 mV. Fastest slew rate. f_0 = 156.25 MHz or 312.5 MHz			340	ps
		Output swing programmed to 900 mV. Fastest slew rate. f_0 = 156.25 MHz or 312.5 MHz			370	ps
DCD	Duty cycle distortion	Input duty cycle = 50%	–1		1	%
FREQUENCY AND TIMING CHARACTERISTICS						
f_0	Operating frequency	Automatic Output Disable functionality is disabled	1		400	MHz
		Automatic Output Disable functionality is enabled	25		400	MHz
$t_{startup}$	Startup time	Cold start. Measured from VDD valid (90% of final VDD) to output clock stable(3). Input clock is provided before VDD is valid. PWRGD_PWRDN# pin is tied to VDD. $f_0 \geq$ 100 MHz			0.4	ms
		Cold start. Measured from VDD valid (90% of final VDD) to output clock stable(3). Input clock is provided before VDD is valid. PWRGD_PWRDN# pin is tied to VDD. $f_0 <$ 100 MHz			0.8	ms

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{stable}	Clock stabilization time	VDD is stable. Measured from PWRGD assertion[4] to output clock stable. $f_0 \geq 100$ MHz[3]			0.4	ms
		VDD is stable. Measured from PWRGD assertion[4] to output clock stable. $f_0 <$ 100 MHz[3]			0.8	ms
$t_{PD\#}$	Powerdown deassertion time	Measured from PWRDN# deassertion[4] to output clock stable. $f_0 \geq 100$ MHz[3]			0.15	ms
		Measured from PWRDN# deassertion[4] to output clock stable. $f_0 <$ 100 MHz[3]			0.5	ms
t_{OE}	Output enable/disable time	Time elapsed from OE assertion/ deassertion[4] to output clock starts/stops	4		10	clk
$t_{LOS\text{-}assert}$	LOS# assertion time	Time elapsed from loss of input clock to LOS# assertion. $f_0 <$ 100 MHz			120	ns
		Time elapsed from loss of input clock to LOS# assertion. $f_0 \geq 100$ MHz			120	ns
$t_{LOS\text{-}deassert}$	LOS# deassertion time	Time elapsed from presence of input clock to LOS# deassertion. $f_0 <$ 100 MHz			340	ns
		Time elapsed from presence of input clock to LOS# deassertion. $f_0 \geq 100$ MHz			105	ns
t_{AOD}	Automatic output disable time	Time elapsed from LOS# assertion to output disable (both outputs are low/ low). $f_0 <$ 100 MHz			0.07	ns
		Time elapsed from LOS# assertion to output disable (both outputs are low/low), $f_0 \geq 100$ MHz			0.07	ns
t_{AOE}	Automatic output enable time	Time elapsed from LOS# deassertion to output clock stable. $f_0 <$ 100 MHz[3]			115	ns
		Time elapsed from LOS# deassertion to output clock stable, $f_0 \geq 100$ MHz[3]			22	ns
t_{switch}	Switch time	Switch between two 100MHz input clocks (MUX only)			70	ns
SKEW AND DELAY CHARACTERISTICS						
t_{skew}	Output-to-output skew	Same bank			50	ps
		Regardless of banks			50	ps
	Part-to-part skew				330	ps
t_{PD}	Input-to-output delay				1	ns
Δt_{PD}	Input-to-output delay variation	Single device over temperature and voltage			1.7	ps/°C
JITTER CHARACTERISTICS						

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe1-CC}$	PCIe Gen 1 CC jitter	Single clock input. Input slew rate ≥ 3.5 V/ns. Differential input swing ≥ 1600 mV			442.5	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC jitter				39	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC jitter				12.3	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC jitter				12.3	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC jitter				4.9	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC jitter				3	fs
$J_{PCIe7-CC}$	PCIe Gen 7 CC jitter				2.1	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR jitter				33.8	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR jitter				14.1	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR jitter				14.5	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR jitter				3.9	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR jitter				3	fs
$J_{PCIe7-IR}$	PCIe Gen 7 IR jitter				2.1	fs
$J_{PCIe1-CC}$	PCIe Gen 1 CC jitter	Single clock input. Input slew rate ≥ 1.5 V/ns. Differential input swing ≥ 800 mV			583.2	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC jitter				51.3	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC jitter				16	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC jitter				16	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC jitter				6.4	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC jitter				3.9	fs
$J_{PCIe7-CC}$	PCIe Gen 7 CC jitter				2.8	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR jitter				41.9	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR jitter				18.3	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR jitter				18.9	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR jitter				5.1	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR jitter				3.8	fs
$J_{PCIe7-IR}$	PCIe Gen 7 IR jitter				2.6	fs
$J_{PCIe1-CC}$	PCIe Gen 1 CC jitter	Both inputs (for MUX only) have running clocks. CLK_SEL pin = low (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz), mid (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz) or high (CLKIN0 = 99.7MHz, CLKIN1 = 100MHz). Input slew rate ≥ 3.5 V/ns. Differential input swing ≥ 1600 mV		255.3	517.5	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC jitter			30	45.3	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC jitter			8.3	13.7	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC jitter			8.3	13.7	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC jitter			2.9	5.5	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC jitter			2	3.5	fs
$J_{PCIe7-CC}$	PCIe Gen 7 CC jitter			1.4	2.5	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR jitter			31.9	48.5	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR jitter			8.8	21.7	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR jitter			8.8	21.7	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR jitter			3.4	6.7	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR jitter			2.8	4.7	fs
$J_{PCIe7-IR}$	PCIe Gen 7 IR jitter			1.4	2.5	fs

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe1-CC}$	PCIe Gen 1 CC jitter	Both inputs (for MUX only) have running clocks. CLK_SEL pin = low (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz), mid (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz) or high (CLKIN0 = 99.7MHz, CLKIN1 = 100MHz). Crosstalk included. Input slew rate ≥ 1.5 V/ns. Differential input swing ≥ 800 mV		388.6	669.5	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC jitter			35.4	57	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC jitter			10.1	17.1	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC jitter			10.1	17.1	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC jitter			3.7	7.4	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC jitter			2.4	4.4	fs
$J_{PCIe7-CC}$	PCIe Gen 7 CC jitter			1.7	3.1	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR jitter			35.4	57	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR jitter			9.8	24	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR jitter			9.9	24	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR jitter			4.3	8.6	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR jitter			3.3	6	fs
$J_{PCIe7-IR}$	PCIe Gen 7 IR jitter			2.3	4.2	
$J_{DB2000QL}$	DB2000QL filter	Input slew rate ≥ 1.5 V/ns. Differential input swing ≥ 800 mV[6]		8.7	11.5	fs
		Input slew rate ≥ 3.5 V/ns. Differential input swing ≥ 1600 mV[6]		6.5	9	fs
$J_{RMS-additive}$	Additive 12 kHz to 20 MHz RMS jitter	f = 100 MHz, slew rate ≥ 3.5 V/ns		27.3	37.5	fs
		f = 100 MHz, slew rate ≥ 1.5 V/ns		37.4	48.5	fs
	Additive 12 kHz to 20 MHz RMS jitter	f = 156.25 MHz, slew rate ≥ 3.5 V/ns		21.9	31	fs
		f = 156.25 MHz, slew rate ≥ 1.5 V/ns		29.4	38.5	fs
	Additive 12 kHz to 70 MHz RMS jitter	f = 156.25 MHz, slew rate ≥ 3.5 V/ns		35.1	48.5	fs
		f = 156.25 MHz, slew rate ≥ 1.5 V/ns		47.1	60.5	fs
	Additive 12 kHz to 20 MHz RMS jitter	f = 312.5 MHz, slew rate ≥ 3.5 V/ns		19.3	28	fs
		f = 312.5 MHz, slew rate ≥ 1.5 V/ns		27.4	39.5	fs
	Additive 12 kHz to 70 MHz RMS jitter	f = 312.5 MHz, slew rate ≥ 3.5 V/ns		29.5	41.5	fs
		f = 312.5 MHz, slew rate ≥ 1.5 V/ns		40.7	58	fs
SUPPLY CURRENT CHARACTERISTICS						
$I_{DD,total}$	LMKDB1202 total supply current	All outputs running, f_0 = 100 MHz			41	mA
$I_{DD,total}$	LMKDB1204 total supply current	All outputs running, f_0 = 100 MHz			54	mA
$I_{DD,core}$	LMKDB1202 core supply current	Pin PWRGD/PWRDN# = high, all outputs disabled			25.5	mA
$I_{DD,core}$	LMKDB1204 core supply current	Pin PWRGD/PWRDN# = high, all outputs disabled			25.5	mA
I_{DDO}	Output supply current per output	f_0 = 100 MHz			6.4	mA
		f_0 = 400 MHz			9.2	mA
I_{PD}	LMKDB1204, power down current	Pin PWRGD/PWRDN# = low			5.6	mA
PSNR CHARACTERISTICS						

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSNR	Power Supply Noise Rejection, V_{DD} = 3.3 V[5]	10 kHz noise ripple			–93	dBc
		50 kHz noise ripple			–91	dBc
		100 kHz noise ripple			–91	dBc
		500 kHz noise ripple			–95	dBc
		1 MHz noise ripple			–96	dBc
		5 MHz noise ripple			–111	dBc
		10 MHz noise ripple			–99	dBc
	Power Supply Noise Rejection, V_{DD} = 1.8 V[5]	10 kHz noise ripple			–85	dBc
		50 kHz noise ripple			–89	dBc
		100 kHz noise ripple			–91	dBc
		500 kHz noise ripple			–93	dBc
		1 MHz noise ripple			–94	dBc
		5 MHz noise ripple			–109	dBc
		10 MHz noise ripple			–97	dBc
I/O CHARACTERISTICS						
V_{IH}	Input voltage high	2-level logic input, V_{DD} = 3.3 V ± 10%	2		V_{DD} + 0.3	V
V_{IL}	Input voltage low		–0.3		0.8	V
V_{IH}	Input voltage high	3-level logic input, V_{DD} = 3.3 V ± 10%	2.4		V_{DD} + 0.3	V
V_{IM}	Input voltage mid		1.2		1.8	V
V_{IL}	Input voltage low		–0.3		0.8	V
V_{IH}	Input voltage high	2-level logic input, V_{DD} = 1.8 V ± 5%	1.3		V_{DD} + 0.3	V
V_{IL}	Input voltage low		–0.3		0.4	V
V_{IH}	Input voltage high	3-level logic input, V_{DD} = 1.8 V ± 5%	1.3		V_{DD} + 0.3	V
V_{IM}	Input voltage mid		0.65		0.95	V
V_{IL}	Input voltage low		–0.3		0.4	V
V_{OH}	Output high voltage	SBI_OUT, I_{OH} = -2 mA	2.4		V_{DD} + 0.3	V
V_{OL}	Output low voltage	SBI_OUT, I_{OL} = 2 mA			0.4	V
I_{IN}	Input leakage current	CLKINx_P	–40		40	µA
		CLKINx_N	–40		40	µA
		single-ended inputs with internal pulldown	–30		30	µA
		single-ended inputs without internal pulldown	–5		5	µA
		3-level logic input	–30		30	µA
$R_{PU,PD}$	Internal pullup/pulldown resistor for single-ended inputs			120		kΩ
SMBUS ELECTRICAL CHARACTERISTICS						
V_{IH}	SMB_CLK, SMB_DATA input high voltage		0.8 × V_{DD}			V
V_{IL}	SMB_CLK, SMB_DATA input low voltage				0.3 × V_{DD}	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05 × V_{DD}			V

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	SMB_DATA output low voltage	I_{OL} = 4 mA			0.4	V
I_{LEAK}	SMB_CLK, SMB_DATA input leakage		–10		10	µA
C_{PIN}	SMB_CLK, SMB_DATA pin capacitance				10	pF

(1) PCIe AC test load
(2) DB2000QL DC test load
(3) First clock edge is used for timing measurements. Clock outputs are muted until stabilized.
(4) For input pins, assertion or deassertion starts when the input voltage reaches the minimum voltage required for a "high" level, or the maximum voltage required for a "low" level
(5) All power supply pins are tied together. A 0.1µF capacitor is placed close to each power supply pin. 50 mVpp ripple is applied before the decoupling capacitors. Measure the spur level at the clock output
(6) DB2000QL AC test load
(7) Slew rate is highly dependent on PCB trace characteristics

6.6 SMBus Timing Requirements

		100-kHz CLASS		400-kHz CLASS		UNIT
		MIN	MAX	MIN	MAX	
f_{SMB}	SMBus Operating Frequency	10	100	10	400	kHz
f_{BUF}	Bus free time between STOP and START condition	4.7	–	1.3	–	µs
t_{HD_STA}	Hold time after (REPEATED) START condition	4.0	–	0.6	–	µs
t_{SU_STA}	REPEATED START condition setup time	4.7	–	0.6	–	µs
t_{SU_STO}	STOP condition setup time	4.0	–	0.6	–	µs
t_{HD_DAT}	Data hold time	0	–	0	–	ns
t_{SU_DAT}	Data setup time	250	–	100	–	ns
$t_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
t_{LOW}	Clock low period	4.7	–	1.3	–	µs
t_{HIGH}	Clock high period	4.0	50	0.6	50	µs
t_{LOW_SEXT}	Cumulative clock low extend time (secondary device)	–	25	–	25	ms
t_{LOW_PEXT}	Cumulative clock low extend time (primary device)	–	10	–	10	ms
t_F	Clock/Data Fall Time	–	300	–	300	ns
t_R	Clock/Data Rise Time	–	1000	–	300	ns
t_{SPIKE}	Noise spike suppression time	–	–	0	50	ns
t_{POR}	Time in which a device must be operational after power-on reset		500		500	ms

6.7 SBI Timing Requirements

		MIN	MAX	UNIT
t_{PERIOD}	Clock period	40	–	ns
t_{SETUP}	SHFT setup to SBI_CLK rising edge	10	–	ns
t_{DSU}	SBI_IN data setup to SBI_CLK rising edge	5	–	ns
t_{DHOLD}	SBI_IN data hold after SBI_CLK rising edge	2	–	ns
t_{DOUT}	SBI_CLK rising edge to SBI_OUT data valid	2	–	ns
t_{LD}	CLK rising edge to LD# falling edge	10	–	ns
t_{OE}	Delay from LD# falling edge to output enable/disable taking effect	4	10	clocks

		MIN	MAX	UNIT
t_{SLEW}	SBI_CLK 20% to 80% slew rate	0.7	4	V/ns

6.8 Timing Diagrams

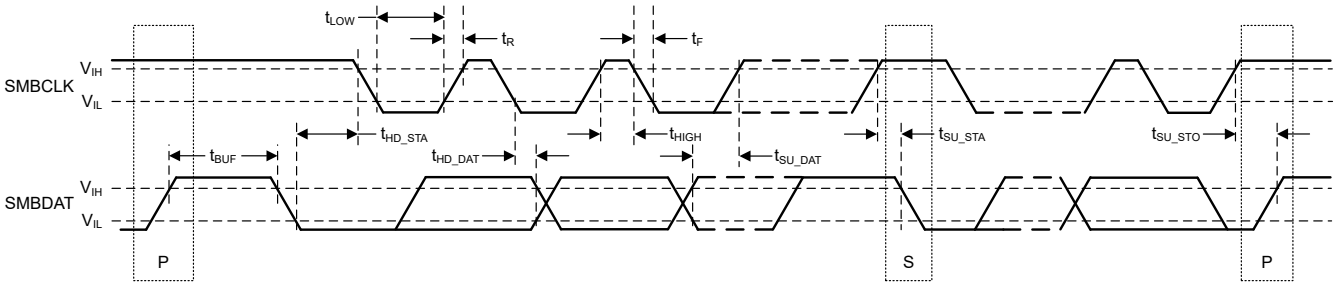


Figure 6-1. SMBus Timing Diagram

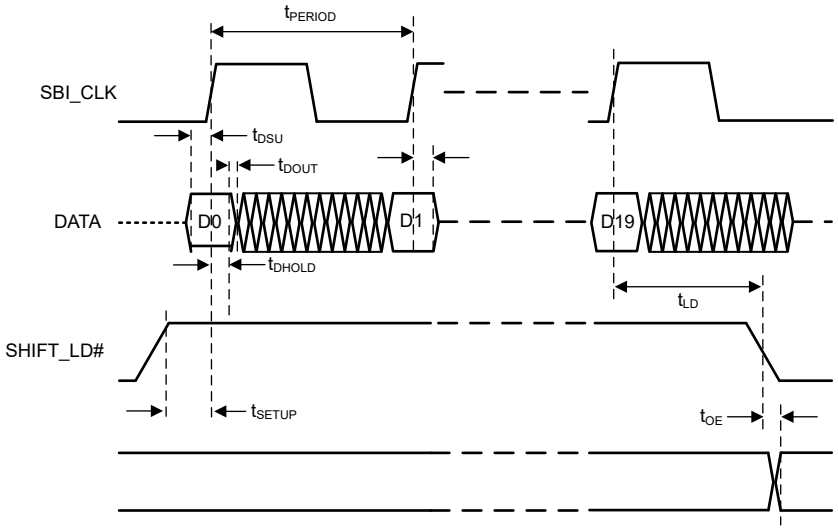


Figure 6-2. SBI Timing Diagram

6.9 Typical Characteristics

7 Parameter Measurement Information

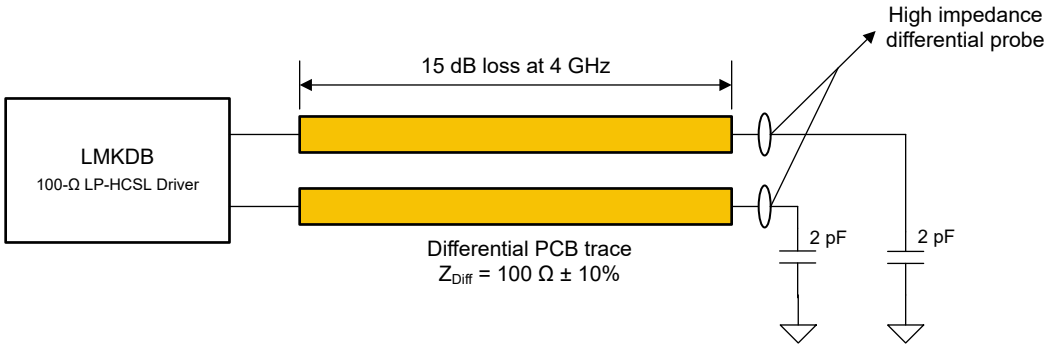


Figure 7-1. PCIe AC Test Load

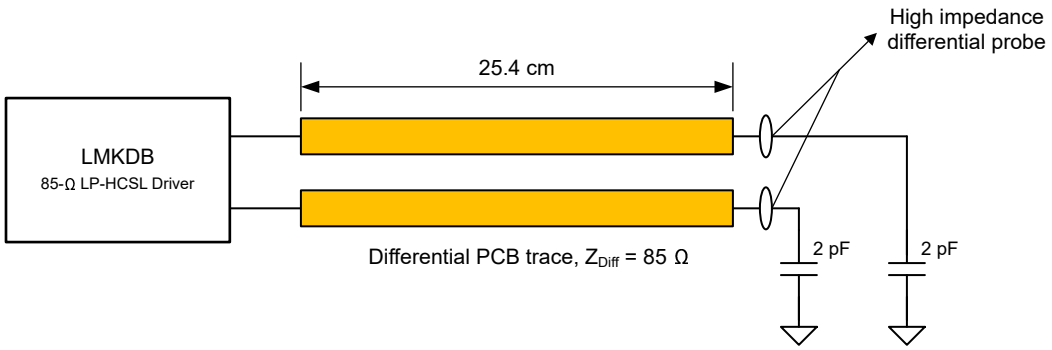


Figure 7-2. DB2000QL AC Test Load

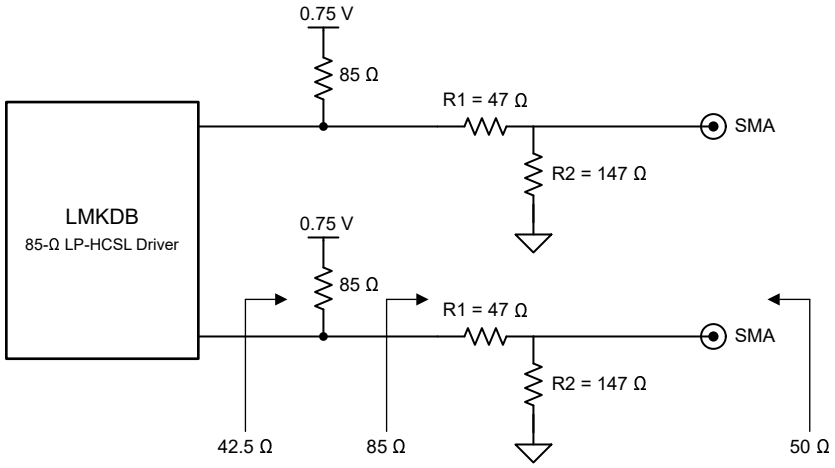


Figure 7-3. DB2000QL DC Test Load

8 Detailed Description

8.1 Overview

LMKDB12xx are PCIe Gen 1 to Gen7 and DB2000QL compliant two input clock muxes that distributes LP-HCSL clocks designed for PCIe Gen 1 through 7 applications.

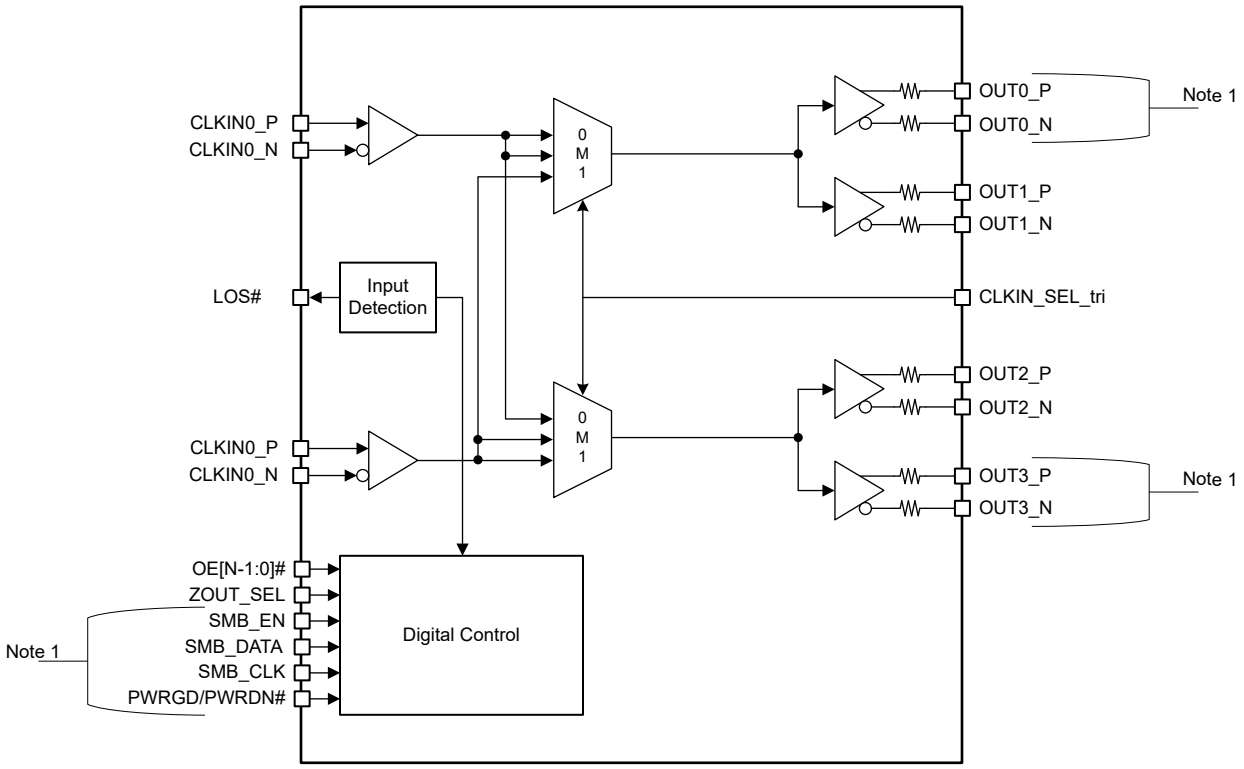
With ultra low additive jitter and ultra low propagation delay, LMKDB12xx devices allow for enough jitter margin for the entire clock path mainly required for PCIe Gen 6 and Gen 7 buffer cascading and Ethernet fan out applications. The LMKDB12xx also support both 1.8V and 3.3V supply voltages for better design flexibility.

LMKDB12xx have individual OE or group OE controls as mentioned in Section 4 for all outputs, which provides more design flexibility. Each output of each device also has programmable slew rate, programmable output amplitude swing, and automatic output disable. The devices support 100Ω or 85Ω LP-HCSL, denoted by the part number as shown in Section 4, with output frequencies of up to 400MHz. LMKDB12xx devices have ZOUT_SEL pin to select 100Ω or 85Ω LP-HCSL output impedance.

LMKDB12xx have pin mode, SMBus mode, and Side Band Interface (SBI) mode, which can all be used at the same time. The vSMB_EN pin on LMKDB1204 can be used to select pin mode or SMBus mode. SBI enables or disables output clocks at a much faster speeds (up to 25MHz) as compared to SMBus. Furthermore, because both SBI and SMBus can operate at the same time, SMBus can still be used to take over device control and readback status after power-up. For more details please refer to Section 8.4.

Refer to Section 8 for the detailed descriptions of the devices pins and the *Register Map* for more details on the device registers.

8.2 Functional Block Diagram



1. LMKDB1204 only.

Figure 8-1. LMKDB1204 LMKDB1202 Functional Block Diagram

8.3 Feature Description

8.3.1 Input Features

8.3.1.1 Running Input Clocks When Device is Powered Off

The device supports running input clocks when power is off. This is different than the fail-safe feature where the input can be pulled to static VDD when device power is off. This is useful if clock inputs are available before power is provided to the clock buffer.

8.3.1.2 Fail-Safe Inputs

All clock input pins and digital input pins support fail-safe. Fail-safe means a pin can be driven to VDD when device power is off, without causing any leakage or reliability problem. For example, an OE# pin can be driven to VDD before device power is up so that the output stays muted until the OE# pin goes low, sometime after power-up.

8.3.1.3 Input Configurations

LMKDB12xx devices input buffer stage supports four different configurations:

- DC coupled HCSL inputs.
- DC coupled LVDS input signal with external 100Ω termination resistor.
- AC coupled inputs with internal self-bias. See AC-Coupled or DC-Coupled Clock Inputs for more details.
- Internal 50Ω to ground terminations. See Internal Termination for Clock Inputs for more details.

All the devices with two inputs have individual AC coupling and input termination option. To configure each input, refer to register map for configuration bits.

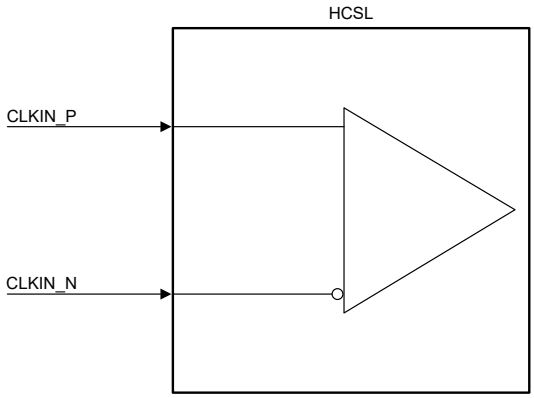


Figure 8-2. HCSL Input Interface (PCIe Standard)

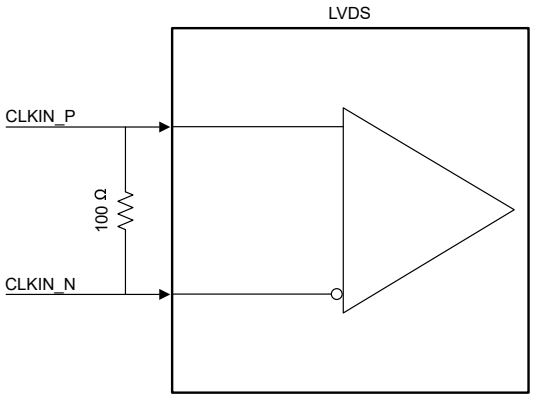


Figure 8-3. LVDS Input Interface

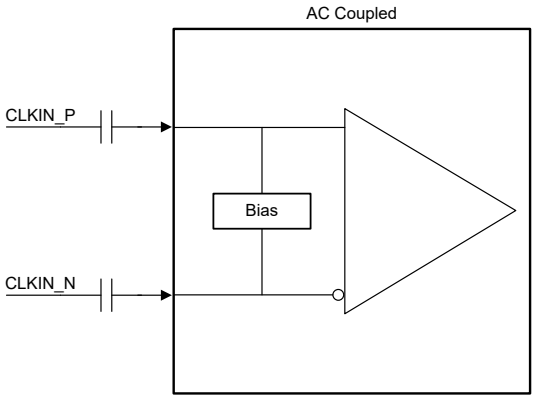


Figure 8-4. External AC-Coupled Input

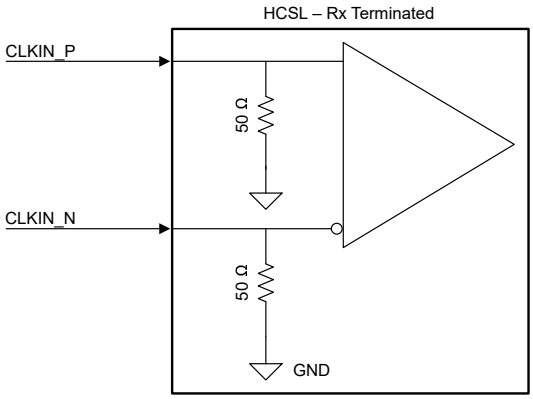


Figure 8-5. Receiver Internal Terminations

8.3.1.3.1 Internal Termination for Clock Inputs

There is an option to enable 50Ω internal termination for differential clock input. For LP-HCSL input, disable the internal termination. For HCSL input, enable internal termination if external termination is not provided. The internal termination is disabled by default.

8.3.1.3.2 AC-Coupled or DC-Coupled Clock Inputs

Input clocks can be either AC coupled or DC coupled. If the inputs are DC coupled, the input signal swing levels must match those in Specifications under the *CLOCK INPUT REQUIREMENTS*. Also, register RX_EN_AC_INPUT must be set to 0 for DC-coupled inputs or set to 1 for AC-coupled inputs. Refer to the *Register Map* for more information about RX_EN_AC_INPUT.

8.3.2 Flexible Power Sequence

8.3.2.1 PWRDN# Assertion and Deassertion

In the recommended power down sequence, PWRDN# is asserted while input clocks are valid. Make sure to hold the PWRDN# pin at low level for two consecutive rising edges of the input clock cycle. As a result, all clock outputs are muted to low/low (OUTx_P = Low, OUTx_N = Low) without a glitch. Following any other sequence brings the device to an undefined mode and can cause glitches or invalid outputs.

8.3.2.2 OE# Assertion and Deassertion

OE# pins can be asserted and deasserted at anytime, whether:

- Device power supply is on or off
- PWRGD/PWRDN# pin is pulled high or low
- Clock input is valid or invalid

The OE# pins only take effect if all below conditions are met:

1. The clock input is valid
2. The PWRGD/PWRDN# pin is high
3. The device power is up

Otherwise outputs are always muted and OE# assertion and deassertion has no impact.

If OE# pins become low in any of the below conditions:

1. Input clock is invalid
2. PWRGD/PWRDN# pin is low
3. Device power is off

Then when all below conditions are met:

1. The clock input is valid
2. The PWRGD/PWRDN# pin is high
3. The device power is up

Outputs are enabled without any glitch (assuming register OE and SBI OE are active).

8.3.2.3 Clock Input and PWRGD/PWRDN# Behaviors When Device Power is Off

Input clocks can be running, floating, low/low or pulled to VDD when device power is off, regardless of PWRGD/PWRDN# pin states (low, high, low-to-high transition and high-to-low transition). Table 8-1 shows all the supported sequences; where clock input can be applied before or after VDD is applied.

Table 8-1. Flexible Power-up Sequences

VDD	PWRGD/PWRDN#	CLKIN_P/CLKIN_N
Not Present	X	Running
		Floating
		Low / Low

Table 8-1. Flexible Power-up Sequences (continued)

VDD	PWRGD/PWRDN#	CLKIN_P/CLKIN_N
Present	0 or 1	Running
		Floating
		Low / Low

8.3.3 LOS and OE

8.3.3.1 Synchronous OE

Outputs are enabled and disabled synchronously. Synchronous OE means when an output is enabled or disabled, there is no glitch or runt pulse at the output.

8.3.3.2 OE Control

OE (Output Enable) can enable or disable a certain output. Three types of OE controls are supported: OE pin, OE register bit through SMBus, and OE control through SBI. The three controls follow the AND logic. An output is enabled only if all three controls enable that output. If any control disables that output, that output is disabled.

8.3.3.2.1 OE Mapping

The LMKDB12xx have maximum of 8 OE# pins. Below table provides mapping for LMKDB1216 and LMKDB1208. Alternate pin function in the table for LMKDB1216 can be selected through OE#_ASSIGNMENT registers.

Table 8-2. LMKDB1216 and LMKDB1208 OE# Mapping

Pin Name	SBI_EN Pin	LMKDB1216 Default Pin Function	LMKDB1216 Alternate Pin Function	LMKDB1208 Default Pin Function	LMKDB1208 Alternate Pin Function
OE0#	X	CLK0 OE#	CLK1 OE#	CLK0 OE#	N/A
OE1#	X	CLK2 OE#	CLK3 OE#	CLK1 OE#	
OE2#	X	CLK4 OE#	CLK5 OE#	CLK2 OE#	
OE3#/SBI_CLK	0 (Inactive)	CLK6 OE#	CLK7 OE#	CLK3 OE#	
	1 (Active)	SBI_CLK	N/A	SBI_CLK	
OE4#/SBI_IN	0 (Inactive)	CLK8 OE#	CLK9 OE#	CLK4 OE#	
	1 (Active)	SBI_IN	N/A	SBI_IN	
OE5#	X	CLK10 OE#	CLK11 OE#	CLK5 OE#	
OE6#/SHFT_LD#	0 (Inactive)	CLK12 OE#	CLK13 OE#	CLK6 OE#	
	1 (Active)	SHFT_LD#	N/A	SHFT_LD#	
OE7#/SBI_OUT	0 (Inactive)	CLK14 OE#	CLK15 OE#	CLK7 OE#	
	1 (Active)	SBI_OUT	N/A	SBI_OUT	

8.3.3.3 Automatic Output Disable

Automatic Output Disable (AOD) is enabled by default, and can be disabled through SMBus. When input clock becomes invalid and LOS# is active, output clocks are muted to low/low (OUTx_P = Low, OUTx_N = Low). Before LOS# is active and after input clock becomes invalid (because LOS detection takes time), output clocks stay at a steady state following the last input state. For example, if the input clock stopped at low/high, then output clocks first stay at low/high, then muted to low/low once LOS# is active.

8.3.3.4 LOS Detection

LOS (Loss Of input Signal) detects whether the clock input is valid or not. When input clock is valid, LOS# register bit = 1 and LOS# pin = high. When input clock is invalid, LOS register bit = 0 and LOS# pin = low.

At power-up, the LOS# pin is kept low until input is detected valid. Therefore, the LOS# pin can be used for the timing of OE# insertion and other operations.

The LOS# signal is only effective if PWRGD/PWRDN# pin is high. If this pin is low, then LOS# is low regardless of input validness

8.3.4 Output Features

8.3.4.1 Output Banks

LMKDB12xx muxes have two output banks that can be used as dual bank buffer mode. Each bank has a dedicated supply pin to avoid cross talk when operating at different frequencies. Refer to Figure 10-2 to minimize noise on the output banks. Below

Table 8-3. LMKDB12xx Output Banks

Output Bank	Outputs (P/N)
0	[0:N/2-1]
1	[N/2:N-1]

8.3.4.2 Double Termination

For regular PCIe applications, LP-HCSL outputs do not require external termination, but the LMKDB family does support double termination (this is uncommon). In that case, an external 50Ω termination is placed and the swing is halved. This results additional power consumption as well due to 50Ω termination to ground on the output.

8.3.4.3 Programmable Output Slew Rate

The LMKDB family offers slew rate control options through SMBus and pin modes. The pin mode option is global slew rate control for all the outputs. SMBus slew rate control supports programmable output slew rate for each individual output. The slew rate is heavily dependent on trace characteristics including trace width, copper thickness, substrate height, dielectric constant, and loss tangent.

LMKDB slew rate control settings are tested with PCIe test load shown in Figure 7-1.

8.3.4.3.1 Slew Rate Control Through SMBus

The LMKDB1120 has 16 different slew rates options that can be assigned to the outputs. 0x0 is the fastest slew rate setting and 0xF is the slowest slew rate setting. To set the slew rate of each output, follow these steps:

1. There are four different registers, SLEWRATE_OPT#, that can store up to four different slew rates. Select your desired slew rates by assigning a value from 0x0 (fastest) to 0xF (slowest) to each SLEWRATE_OPT# register. The default values set to each SLEWRATE_OPT# register can be found in Table 8-4.
   a. For example, if you wanted the fastest, second fastest, and the slowest slew rate, assign 0x0, 0x1, and 0xF to registers SLEWRATE_OPT#. SLEWRATE_OPT1 = 0x0 (fastest), SLEWRATE_OPT2 = 0x1 (second fastest), and SLEWRATE_OPT3 = 0xF (slowest). SLEWRATE_OPT4 does not have to be assigned, but if you want more than one register set to a slew rate, then SLEWRATE_OPT4 can be assigned to any of the three previous settings.
2. Set a slew rate option for each output by using the SLEWRATE_SEL_CLKX_LSB and SLEWRATE_SEL_CLKX_MSB as shown in Table 8-4 or drop-down menus under the Output Slew Rate Control Section in TICSPro. The default SLEWRATE_OPT# register assignment for all outputs is SLEWRATE_OPT2, which has a default slew rate of 0x6.

The corresponding ranges for the four default slew rates can be found in Section 6 under *CLOCK OUTPUT CHARACTERISTICS - 100MHz 85Ω PCIe* or *CLOCK OUTPUT CHARACTERISTICS - 100MHz 100Ω PCIe* for the specification *Output slew rate*.

Table 8-4. LMKDB Default SLEWRATE_OPT_# Values

Register Field Name	Default Value	Default Slew Rate
SLEWRATE_OPT_1	0x0	Highest
SLEWRATE_OPT_2	0x6	High (default for all outputs)

Table 8-4. LMKDB Default SLEWRATE_OPT_# Values (continued)

Register Field Name	Default Value	Default Slew Rate
SLEWRATE_OPT_3	0xA	Low
SLEWRATE_OPT_4	0xF	Lowest

Table 8-5. SLEWRATE_SEL_CLKX_LSB & SLEWRATE_SEL_CLKX_MSB Slew Rate Selection

SLEWRATE_SEL_CLKX_LSB	SLEWRATE_SEL_CLKX_MSB	Slew Rate Option Selection
0	0	SLEWRATE_OPT_4
1	0	SLEWRATE_OPT_3
0	1	SLEWRATE_OPT_2
1	1	SLEWRATE_OPT_1

To program the slew rate to the desired slew rate, the following sequence needs to be followed:

1. [Optional]: if the default assignments shown in Table 8-4 for each slew rate speed is not as desired, one of the slew rate options value can be changed to another slew rate.
2. [LMKDB1108 and 1104 only]: Program SLEWRATE_CTRL_MODE register to 1 to select SMBus programming mode for slew rate control. Refer to Section 9 section for LMKDB1108 and LMKDB1104 register bits information.
3. Program SLEWRATE_SEL_CLKX_MSB and SLEWRATE_SEL_CLKX_LSB to assign clock output X to desired slew rate speed option, as shown in Table 8-5. The default assignments for each option can be found in Table 8-4.

8.3.4.4 Programmable Output Swing

The LMKDB family supports programmable LP-HCSL swings between a range of 600mV to 975mV. All outputs are programmed to the same output swing via register AMP and AMP_BANKX for both buffer and mux respectively. To program the outputs to the desired swing refer to the Register Maps.

8.3.4.5 Accurate Output Impedance

The LMKDB family supports both 100Ω LP-HCSL and 85Ω LP-HCSL. The output impedance is accurately trimmed to ±5%. This helps improve impedance matching and clock signal integrity.

8.3.4.6 Programmable Output Impedance

The LMKDB12xx pin mode option to select 100Ω or 85Ω LP-HCSL output impedance provides flexibility in design. Output impedance can be selected using ZOUT_SEL pin on the device as shown in Table 8-6. If left floating, 85Ω output impedance is selected by default through an internal pulldown resistor.

Table 8-6. Programmable Output Impedance

ZOUT_SEL	Output Impedance
Low	85Ω
High	100Ω

8.4 Device Functional Modes

8.4.1 SMBus Mode

In SMBus mode, LMKDB11xx device SMBus registers can be written and read through SMBus pins. Pin SADR1 and SADR0 set the SMBus address.

SADR1	SADR0	8-Bit SMBus Address (R/W Bit = 0)
Low	Low	0xD8
Low	Float	0xDA
Low	High	0xDE

SADR1	SADR0	8-Bit SMBus Address (R/W Bit = 0)
Float	Low	0xC2
Float	Float	0xC4
Float	High	0xC6
High	Low	0xCA
High	Float	0xCC
High	High	0xCE

Table 8-7. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Register address for *Byte* operations, or starting register address for *Block*, operations

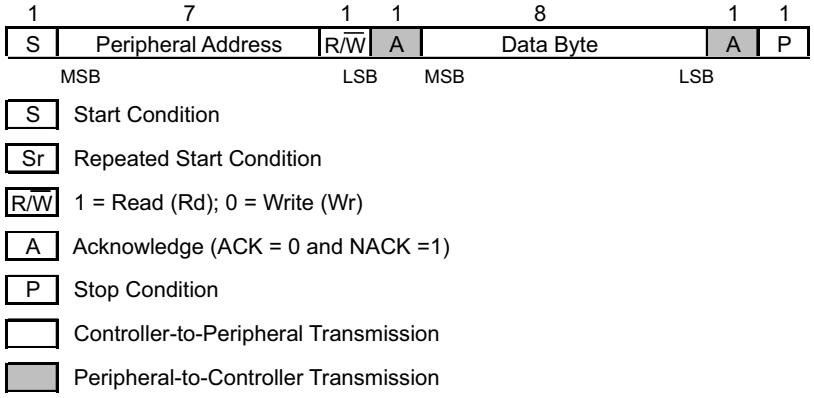


Figure 8-6. Generic Programming Sequence

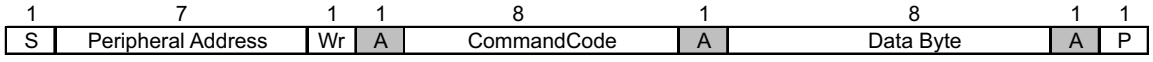


Figure 8-7. Byte Write Protocol

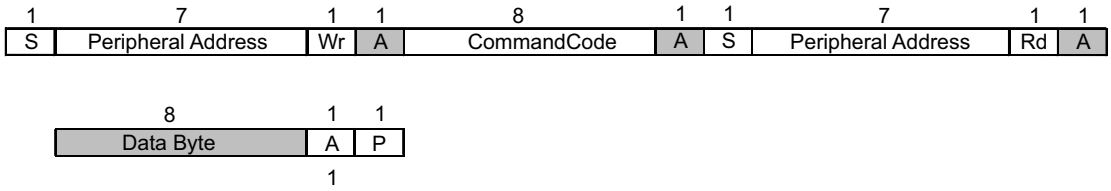


Figure 8-8. Byte Read Protocol

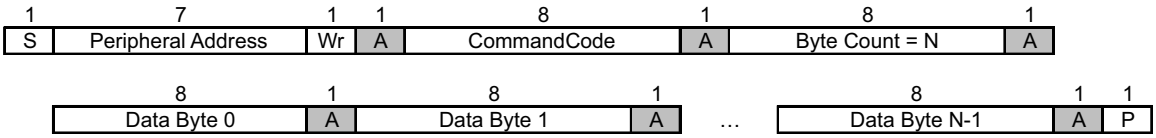


Figure 8-9. Block Write Protocol

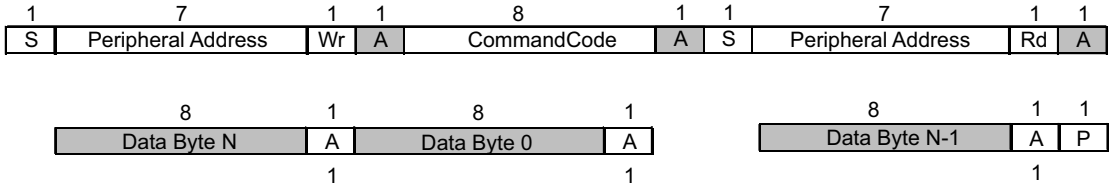


Figure 8-10. Block Read Protocol

8.4.2 SBI Mode

Side-Band Interface (SBI) is a simple 3-wire or 4-wire serial interface which consists of SHFT_LD#, SBI_IN, SBI_CLK and SBI_OUT (optional) pins. When the SHFT_LD# pin is high, the rising edge of SBI_CLK clocks SBI_IN into a shift register. After shifting data, the falling edge of SHFT_LD# loads the shift register contents into the output register. SBI registers can be shifted out through SBI_OUT pin to form daisy chain topology.

Enabling SBI mode does not disable SMBus. SBI registers can be accessed while PWRGD/PWRDN# pin is low.

LMKDB12xx only supports pin mode and SMBus mode.

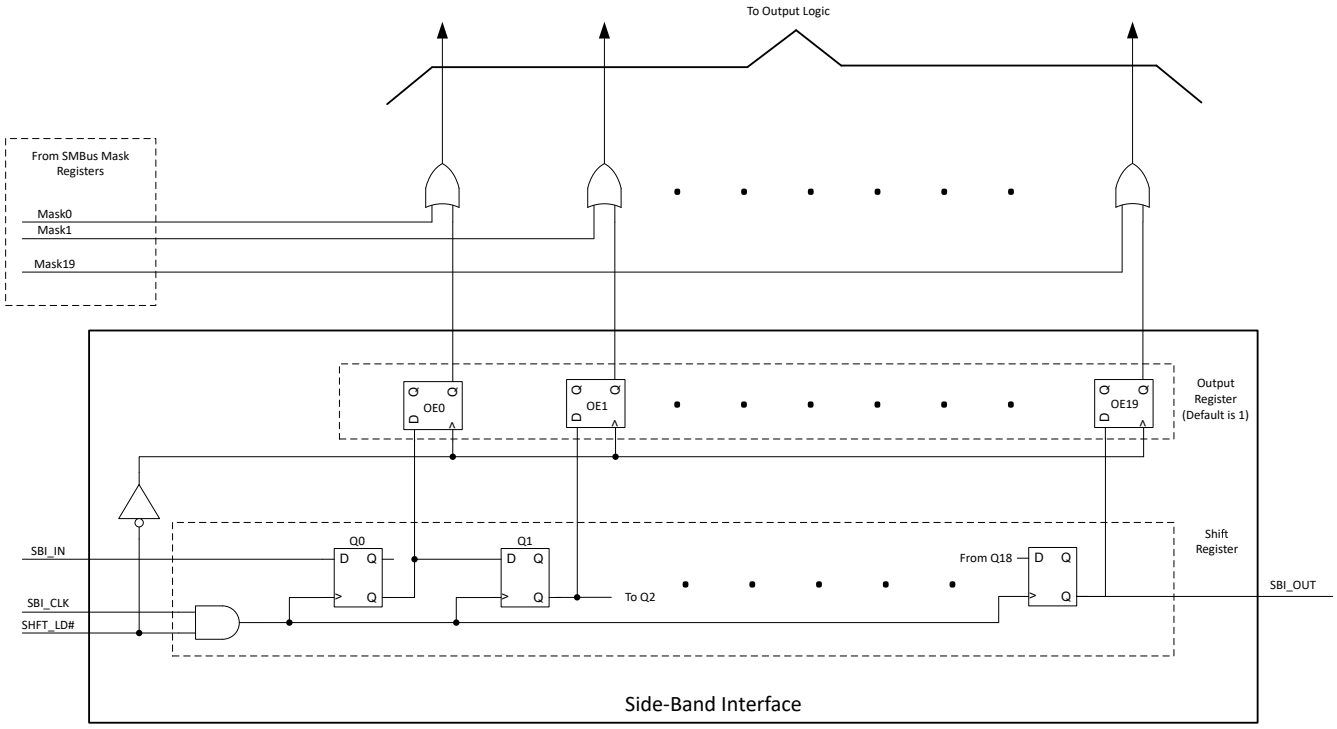


Figure 8-11. SBI Control Logic

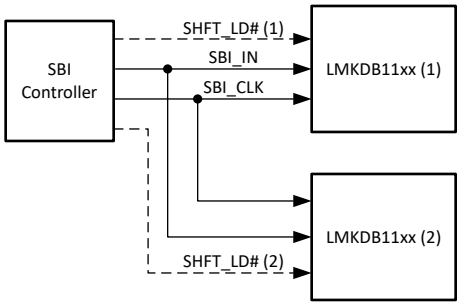


Figure 8-12. SBI Star Topology

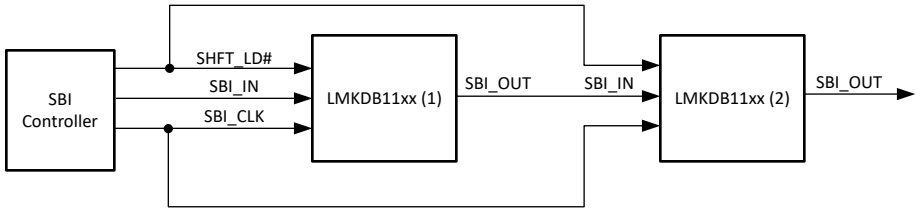


Figure 8-13. SBI Daisy Chain Topology

SBI register sequence:

8.4.3 Pin Mode

If the SMBus or SBI interface is not needed, the SMBus pins or SBI pins can be left floating. The device can operate in pin mode and the outputs can be enabled or disabled by OE# pins.

9 Register Maps

9.1 LMKDB12xx Registers

Table 9-1 lists the memory-mapped registers for the LMKDB1204 registers. All register offset addresses not listed in Table 9-1 must be considered as reserved locations and the register contents must not be modified.

Table 9-1. LMKDB12xx Registers

Offset	Acronym	Register Name	Section
0h	R0	Output Enable Control for CLK2 and CLK3	Section 9.1.1
1h	R1	Output Enable Control for CLK0 and CLK1	Section 9.1.2
2h	R2	OE Pin Readback for CLK2 and CLK3	Section 9.1.3
3h	R3	OE Pin Readback for CLK0 and CLK1	Section 9.1.4
4h	R4	CLKIN1 AOD Enable Control	Section 9.1.5
5h	R5	Device Info	Section 9.1.6
6h	R6	Device Info (cont.)	Section 9.1.7
7h	R7	SMBus Byte Counter	Section 9.1.8
11h	R17	Output Amplitude	Section 9.1.9
12h	R18	Input Configuration, Save Config in PD, SMB SDATA Monitoring, and LOS Readback	Section 9.1.10
14h	R20	Output Slew Rate Select MSB for CLK2 and CLK3	Section 9.1.11
15h	R21	Output Slew Rate Select MSB for CLK0 and CLK1	Section 9.1.12
24h	R36	CLKIN0 AOD Enable Control	Section 9.1.13
26h	R38	Non-clearable SMBUS Write Lock	Section 9.1.14
27h	R39	LOS Event Status and Clearable SMBus Write Lock	Section 9.1.15
2Bh	R43	CLKIN Source Select	Section 9.1.16
5Bh	R91	Slew Rate Speed Options 1 and 2 Assignments	Section 9.1.17
5Ch	R92	Slew Rate Speed Options 3 and 4 Assignments	Section 9.1.18
5Dh	R93	CLKIN0 AC/DC coupled Selection	Section 9.1.19
62h	R98	Output Slew Rate Select LSB for CLK0 and CLK1	Section 9.1.20
63h	R99	Output Slew Rate Select LSB for CLK2 and CLK3	Section 9.1.21

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. LMKDB12xx Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

9.1.1 R0 Register (Offset = 0h) [Reset = 28h]

R0 is shown in Table 9-3.

Return to the Summary Table.

Table 9-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	CLK_EN_1	R/W	1h	Output Enable for CLK1 0h = Output Disabled (low/low) 1h = Output Enabled
4	RESERVED	R	0h	Reserved
3	CLK_EN_0	R/W	1h	Output Enable for CLK0 0h = Output Disabled (low/low) 1h = Output Enabled
2:0	RESERVED	R	0h	Reserved

9.1.2 R1 Register (Offset = 1h) [Reset = 14h]

R1 is shown in Table 9-4.

Return to the Summary Table.

Table 9-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	CLK_EN_3	R/W	1h	Output Enable for CLK3 0h = Output Disabled (low/low) 1h = Output Enabled
3	RESERVED	R	0h	Reserved
2	CLK_EN_2	R/W	1h	Output Enable for CLK2 0h = Output Disabled (low/low) 1h = Output Enabled
1:0	RESERVED	R	0h	Reserved

9.1.3 R2 Register (Offset = 2h) [Reset = 00h]

R2 is shown in Table 9-5.

Return to the Summary Table.

Table 9-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RB_OEb_1	R	0h	Status of OEb1
4	RESERVED	R	0h	Reserved
3	RB_OEb_0	R	0h	Status of OEb0
2:0	RESERVED	R	0h	Reserved

9.1.4 R3 Register (Offset = 3h) [Reset = 00h]

R3 is shown in Table 9-6.

Return to the Summary Table.

Table 9-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved

Table 9-6. R3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RB_OEb_3	R	0h	Status of OEb3
3	RESERVED	R	0h	Reserved
2	RB_OEb_2	R	0h	Status of OEb2
1:0	RESERVED	R	0h	Reserved

9.1.5 R4 Register (Offset = 4h) [Reset = 10h]

R4 is shown in Table 9-7.

Return to the Summary Table.

Table 9-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	CLKIN1_AOD_ENABLE	R/W	1h	Enable automatic output disable (AOD) for CLKIN1 to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information. 0h = Inactive 1h = Active
3:0	RESERVED	R	0h	Reserved

9.1.6 R5 Register (Offset = 5h) [Reset = 0Ah]

R5 is shown in Table 9-8.

Return to the Summary Table.

Table 9-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	REV_ID	R	0h	Revision ID
3:0	VENDOR_ID	R	Ah	Vendor ID

9.1.7 R6 Register (Offset = 6h) [Reset = 24h]

R6 is shown in Table 9-9.

Return to the Summary Table.

Table 9-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID	R	24h	Device ID

9.1.8 R7 Register (Offset = 7h) [Reset = 07h]

R7 is shown in Table 9-10.

Return to the Summary Table.

Table 9-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4:0	SMBUS_BC	R/W	7h	SMBUS Block Read Byte Count

9.1.9 R17 Register (Offset = 11h) [Reset = 66h]

R17 is shown in Table 9-11.

Return to the Summary Table.

Table 9-11. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	AMP_BANK1	R/W	6h	Global Differential output Control,approximately 0.6V to 1V 25mV/ step (default = 0.75V) 0h = 600mV 1h = 625mV 2h = 650mV 3h = 675mV 4h = 700mV 5h = 725mV 6h = 750mV 7h = 775mV 8h = 800mV 9h = 825mV Ah = 850mV Bh = 875mV Ch = 900mV Dh = 925mV Eh = 950mV Fh = 975mV
3:0	AMP_BANK0	R/W	6h	Global Differential output Control,approximately 0.6V to 1V 25mV/ step (default = 0.75V) 0h = 600mV 1h = 625mV 2h = 650mV 3h = 675mV 4h = 700mV 5h = 725mV 6h = 750mV 7h = 775mV 8h = 800mV 9h = 825mV Ah = 850mV Bh = 875mV Ch = 900mV Dh = 925mV Eh = 950mV Fh = 975mV

9.1.10 R18 Register (Offset = 12h) [Reset = 0Ah]

R18 is shown in Table 9-12.

Return to the Summary Table.

Table 9-12. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RX_CLKIN1_EN_AC_INPUT	R/W	0h	Enable receiver bias when CLKIN1 is AC coupled 0h = DC Coupled Input 1h = AC Coupled Input
6	RX_CLKIN1_EN_RTERM	R/W	0h	Enable termination resistors on CLKIN1 0h = Input termination inactive 1h = Input termination active
5	RX_CLKIN0_EN_RTERM	R/W	0h	Enable termination resistors on CLKIN0 0h = Input termination inactive 1h = Input termination active
4	RESERVED	R	0h	Reserved

Table 9-12. R18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PD_RESTOREB	R	1h	Save configuration in powerdown 0h = Config Cleared 1h = Config Saved
2	RESERVED	R	0h	Reserved
1	SDATA_TIMEOUT_EN	R	1h	Enable SMBus SDATA time out monitoring 0h = Disable SDATA timeout 1h = Enable SDATA timeout
0	LOSb_RB	R	0h	Real time read back of loss detect block output 0h = LOS Event Detected 1h = LOS Event Not-Detected

9.1.11 R20 Register (Offset = 14h) [Reset = 28h]

R20 is shown in Table 9-13.

Return to the Summary Table.

Table 9-13. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	SLEWRATE_SEL_CLK1_MSB	R/W	1h	MSB CLK1 slew rate select
4	RESERVED	R	0h	Reserved
3	SLEWRATE_SEL_CLK0_MSB	R/W	1h	MSB CLK0 slew rate select
2:0	RESERVED	R	0h	Reserved

9.1.12 R21 Register (Offset = 15h) [Reset = 14h]

R21 is shown in Table 9-14.

Return to the Summary Table.

Table 9-14. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	SLEWRATE_SEL_CLK3_MSB	R/W	1h	MSB CLK3 slew rate select
3	RESERVED	R	0h	Reserved
2	SLEWRATE_SEL_CLK2_MSB	R/W	1h	MSB CLK2 slew rate select
1:0	RESERVED	R	0h	Reserved

9.1.13 R36 Register (Offset = 24h) [Reset = 09h]

R36 is shown in Table 9-15.

Return to the Summary Table.

Table 9-15. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved

Table 9-15. R36 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CLKIN0_AOD_ENABLE	R/W	1h	Enable automatic output disable (AOD) for CLKIN0 to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information. 0h = Inactive 1h = Active
2:0	RESERVED	R	0h	Reserved

9.1.14 R38 Register (Offset = 26h) [Reset = 00h]

R38 is shown in Table 9-16.

Return to the Summary Table.

Table 9-16. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	WRITE_LOCK	R	0h	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power. 0h = SMBus Not Locked for Writing 1h = SMBus Locked for Writing

9.1.15 R39 Register (Offset = 27h) [Reset = 00h]

R39 is shown in Table 9-17.

Return to the Summary Table.

Table 9-17. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0h	Reserved
1	LOS_EVT	R	0h	LOS Event Status. When high, indicates that a LOS event is detected. Can be cleared by writing a 1. 0h = Not LOS Event Detected 1h = LOS Event Detected
0	WRITE_LOCK_RW1C	R/W1C	0h	Clearable SMBus Write Lock bit. When written to one, the SMBus control registers can not be written to. This bit can be cleared by writing a 1. 0h = SMBus Not Locked for Writing 1h = SMBus Locked for Writing

9.1.16 R43 Register (Offset = 2Bh) [Reset = 00h]

R43 is shown in Table 9-18.

Return to the Summary Table.

Table 9-18. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:4	CLKIN_SEL	R/W	0h	CLKIN Source Select 0h = All outputs come from CLKIN0 1h = CLKIN0 inputs go to BANK0 and CLKIN1 inputs go to BANK1 2h = Invalid 3h = All outputs come from CLKIN1

Table 9-18. R43 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	R	0h	Reserved

9.1.17 R91 Register (Offset = 5Bh) [Reset = 60h]

R91 is shown in Table 9-19.

Return to the Summary Table.

Table 9-19. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SLEWRATE_OPT_2	R/W	6h	There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 2nd option. Go to Programmable Output Slew Rate section for more information. 0h = 0 (fastest) 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15 (slowest)
3:0	SLEWRATE_OPT_1	R/W	0h	There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 1st option. Go to Programmable Output Slew Rate section for more information. 0h = 0 (fastest) 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15 (slowest)

9.1.18 R92 Register (Offset = 5Ch) [Reset = FAh]

R92 is shown in Table 9-20.

Return to the Summary Table.

Table 9-20. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SLEWRATE_OPT_4	R/W	Fh	There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 4th option. Go to Programmable Output Slew Rate section for more information. 0h = 0 (fastest) 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15 (slowest)
3:0	SLEWRATE_OPT_3	R/W	Ah	There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 3rd option. Go to Programmable Output Slew Rate section for more information. 0h = 0 (fastest) 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15 (slowest)

9.1.19 R93 Register (Offset = 5Dh) [Reset = 00h]

R93 is shown in Table 9-21.

Return to the Summary Table.

Table 9-21. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	RX_CLKIN0_EN_AC_INPUT	R/W	0h	Enable receiver bias when CLKIN0 is AC coupled 0h = DC Coupled Input 1h = AC Coupled Input

9.1.20 R98 Register (Offset = 62h) [Reset = 00h]

R98 is shown in Table 9-22.

Return to the Summary Table.

Table 9-22. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	SLEWRATE_SEL_CLK2_LSB	R/W	0h	LSB CLK2 Slew Rate Control
4	SLEWRATE_SEL_CLK3_LSB	R/W	0h	LSB CLK3 Slew Rate Control
3:0	RESERVED	R	0h	Reserved

9.1.21 R99 Register (Offset = 63h) [Reset = 00h]

R99 is shown in Table 9-23.

Return to the Summary Table.

Table 9-23. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	SLEWRATE_SEL_CLK0_LSB	R/W	0h	LSB CLK0 Slew Rate Control
5:3	RESERVED	R	0h	Reserved
2	SLEWRATE_SEL_CLK1_LSB	R/W	0h	LSB CLK1 Slew Rate Control
1:0	RESERVED	R	0h	Reserved

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMKDB12xx devices are a family of ultra-low additive jitter LP-HCSL clock mux. The device can be controlled through SMBus registers, Side Band Interface, and OE# pins.

10.2 Typical Application

This example shows PCIe and Ethernet clock distribution. Provide multiple copies of PCIe clocks (100MHz) or Ethernet clocks (156.25MHz) based on the given source.

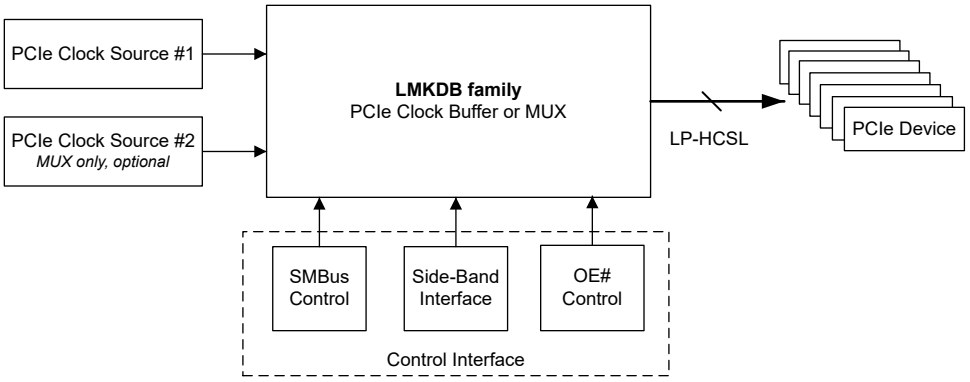


Figure 10-1. Typical Application

10.2.1 Design Requirements

Find two buffers for PCIe clock fan-out and Ethernet clock fan-out separately. Jitter requirements must be met and space must be minimized.

Table 10-1. Design Parameters

PARAMETER	VALUE
Number of PCIe clocks	15
Number of 156.25MHz Ethernet clocks	7
PCIe architecture	CC (Common Clock)
PCIe reference clock slew rate	≥3.5V/ns
PCIe Gen 5 reference clock jitter	45fs maximum
PCIe Gen 5 total jitter	50fs maximum
156.25MHz reference clock slew rate	≥3.5V/ns
156.25MHz reference clock jitter (12kHz to 20MHz)	90fs maximum
156.25MHz total jitter (12kHz to 20MHz)	100fs maximum

10.2.2 Detailed Design Procedure

First of all, calculate the jitter budget for the clock buffer using RMS addition. The maximum allowed additive jitter for the clock buffer is square root of the difference between square of reference clock jitter and square of total clock jitter.

The maximum PCIe Gen 5 additive jitter allowed for the buffer is sqrt(50^2 – 45^2) = 21fs. According to the Specifications under the *Electrical Characteristics* table, the additive PCIe Gen 5 jitter under Common Clock and ≥3.5V/ns input slew rate test condition is 13fs maximum, well below 21fs requirement.

Similarly, the maximum 12kHz to 20MHz additive jitter allowed at 156.25MHz is sqrt(100^2 – 90^2) = 43fs. According to the Specifications under the *Electrical Characteristics* table, the 12kHz to 20MHz additive jitter at 156.25MHz is 31fs maximum, well below the 43fs requirement.

10.2.3 Application Curves

The following plots are example phase noise plots before and after using the LMKDB12xx at 156.25MHz, respectively. The LMKDB clock mux adds a 22fs (typical) jitter from 12kHz to 20MHz. All LMKDB12xx devices have very similar performance.

To better understand jitter and how the additive jitter of the LMKDB12xx resulted in 22fs refer to *Timing is Everything: How to measure additive jitter* TI blog post.

10.3 Power Supply Recommendations

Place a 0.1µF capacitor close to every power supply pin. To minimize noise on VDDA, , place a 2.2Ω resistor next to the pins. All supply pins can be grouped onto one power rail. TI recommends a Ferrite Bead and a 10µF capacitor to GND for the entire chip. Figure 10-2 shows an example power schematic.

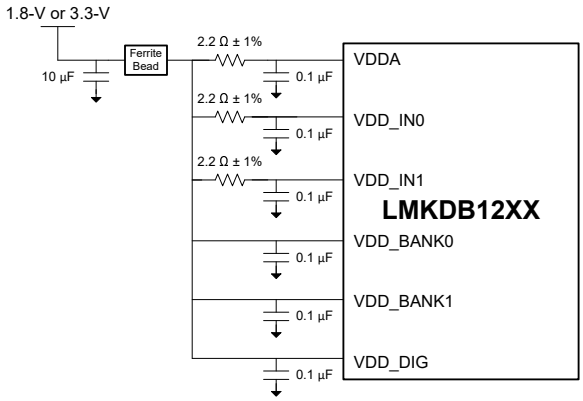


Figure 10-2. Power Supply Recommendation for LMKDB12XX MUX

10.4 Layout

10.4.1 Layout Guidelines

Use a low-inductance ground connection between the device DAP and the PCB.

Match PCB trace impedance with device output impedance (85Ω or 100Ω differential impedance). Eliminate stubs and reduce discontinuity on the transmission lines.

10.4.2 Layout Example

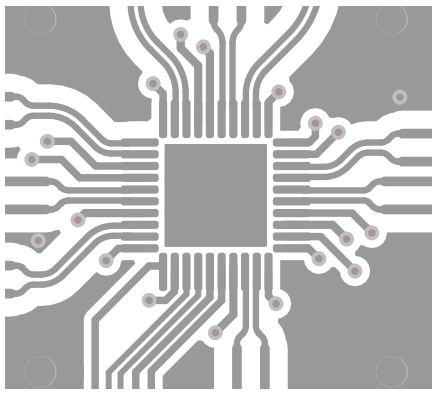


Figure 10-3. LMKDB1204 Layout Example - Bottom Layer

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMKDB1120 Evaluation Module*, user's guide
- Texas Instruments, *LMKDB1108 Evaluation Module*, user's guide
- Texas Instruments, *LMKDB1104 Evaluation Module*, user's guide
- Texas Instruments, *LMKDB1204 Evaluation Module*, user's guide
- Texas Instruments, *LMKDB1102/1202 Evaluation Module*, user's guide
- Texas Instruments, *Timing is Everything: How to measure additive jitter*, blog post

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	• Initial Release • Moved the LMKDB1204 and LMKDB1202 from old data sheet (SNAS855)

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMKDB1202REYR	Active	Production	VQFN (REY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	DB1202
LMKDB1202REYR.A	Active	Production	VQFN (REY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	DB1202
LMKDB1202REYT	Active	Production	VQFN (REY) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	DB1202
LMKDB1202REYT.A	Active	Production	VQFN (REY) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	DB1202
LMKDB1204REXR	Active	Production	VQFN (REX) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMKDB 1204
LMKDB1204REXR.A	Active	Production	VQFN (REX) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMKDB 1204
LMKDB1204REXT	Active	Production	VQFN (REX) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMKDB 1204
LMKDB1204REXT.A	Active	Production	VQFN (REX) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMKDB 1204

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

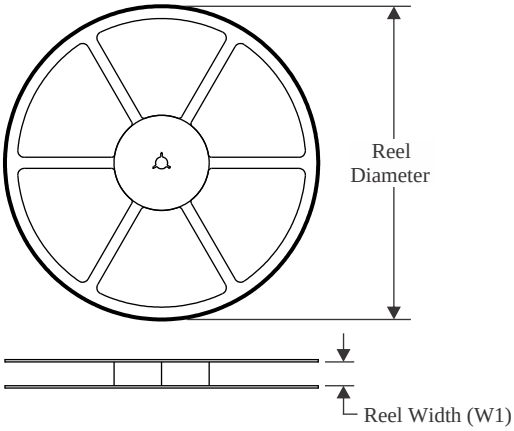
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

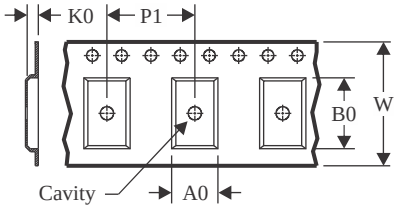
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

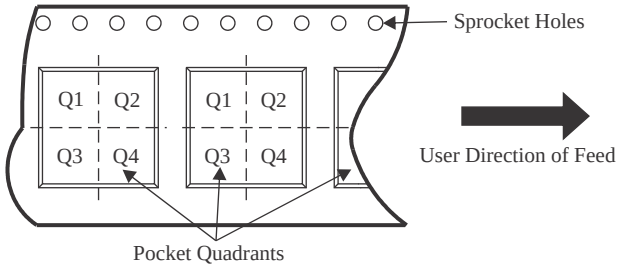


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

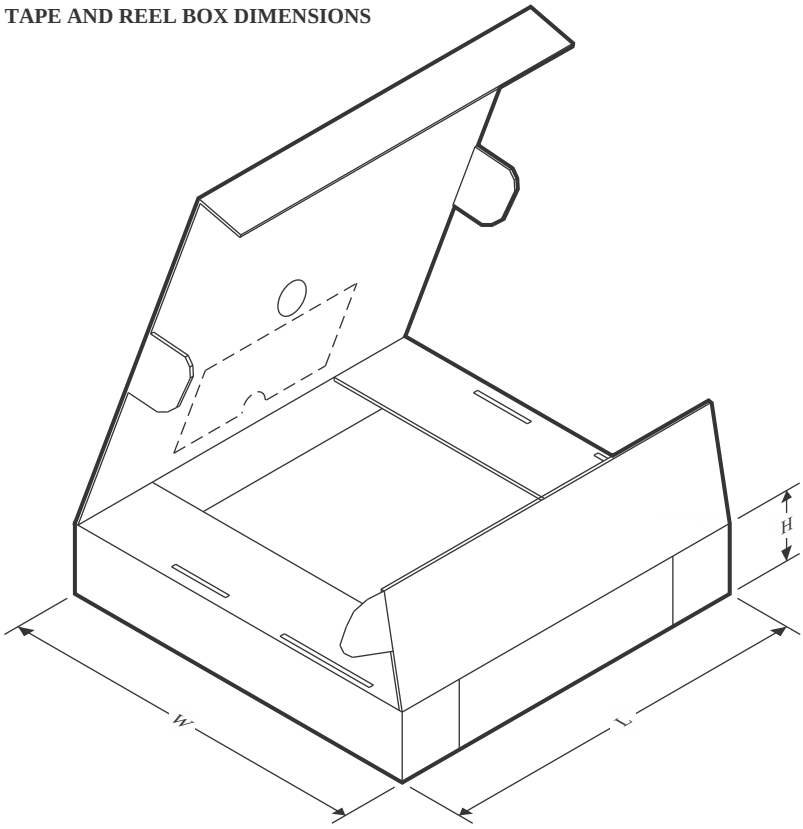
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMKDB1202REYR	VQFN	REY	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMKDB1204REXR	VQFN	REX	28	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

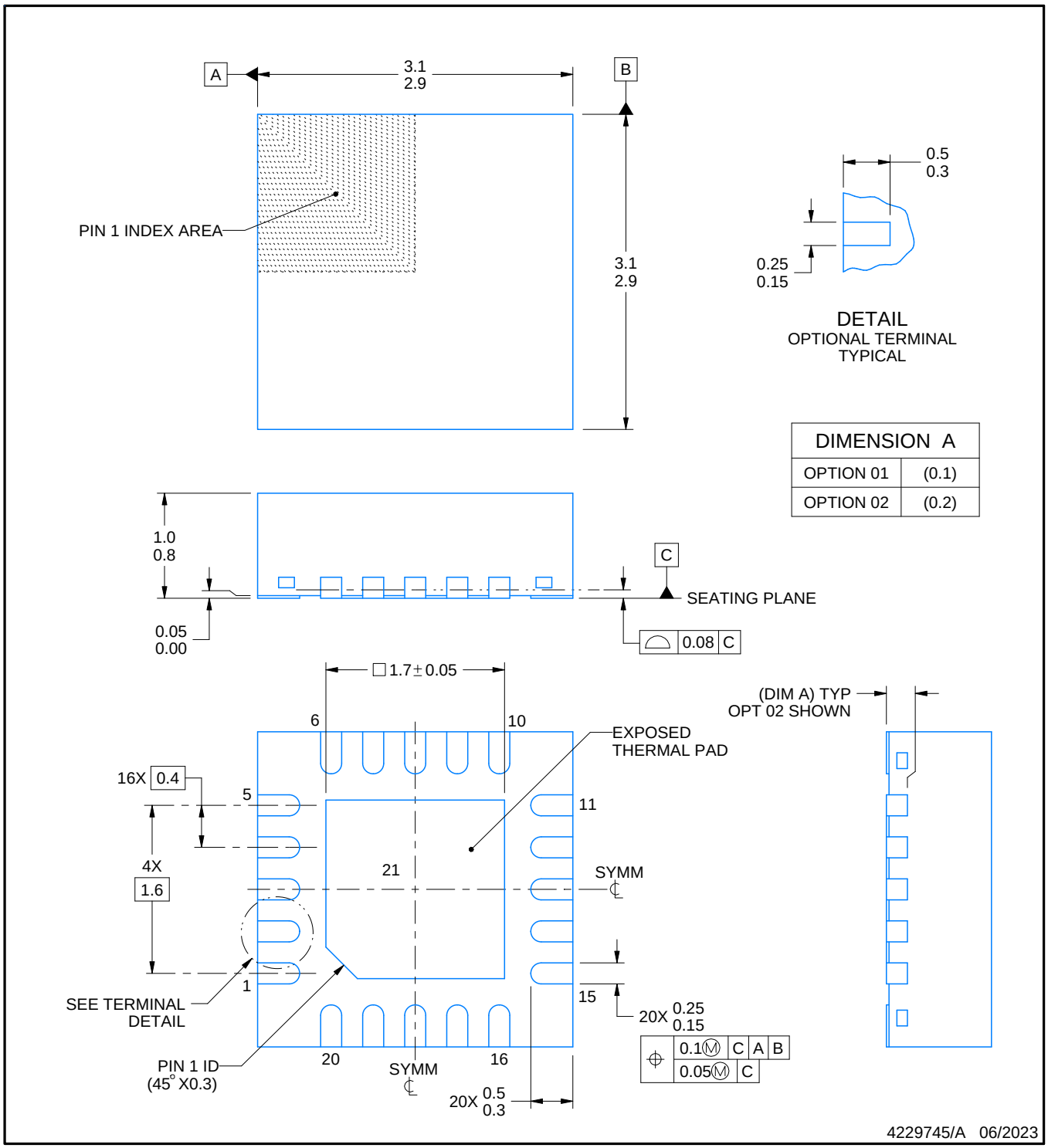
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMKDB1202REYR	VQFN	REY	20	3000	367.0	367.0	35.0
LMKDB1204REXR	VQFN	REX	28	3000	367.0	367.0	35.0

REY0020B

PACKAGE OUTLINE

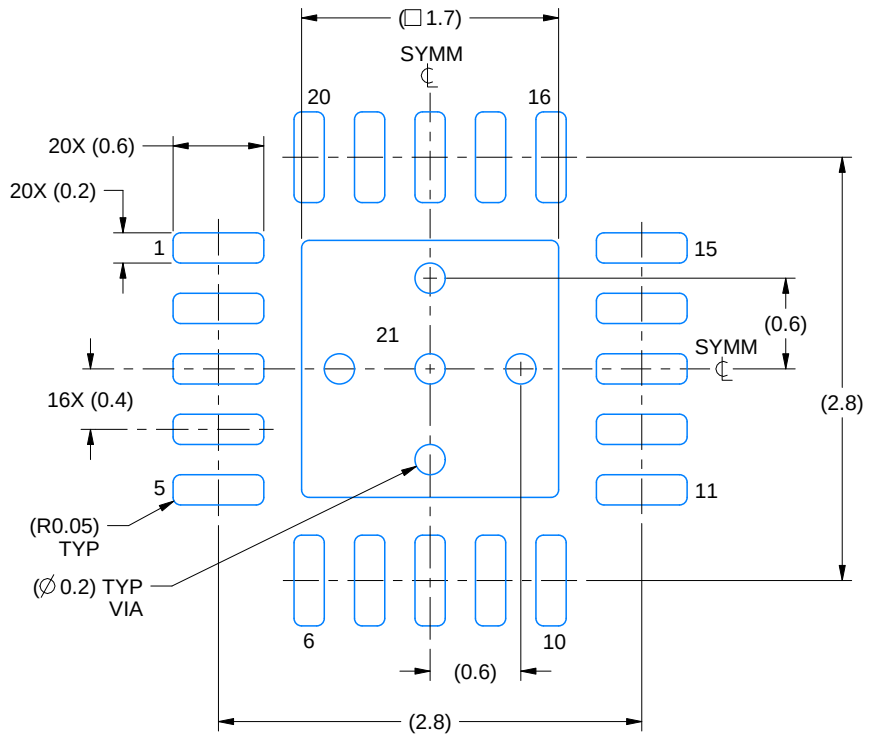
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

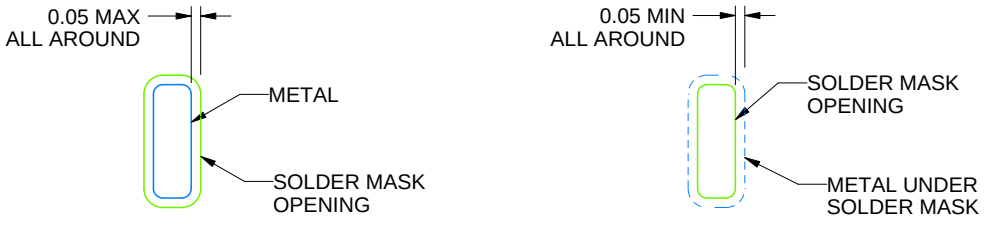


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

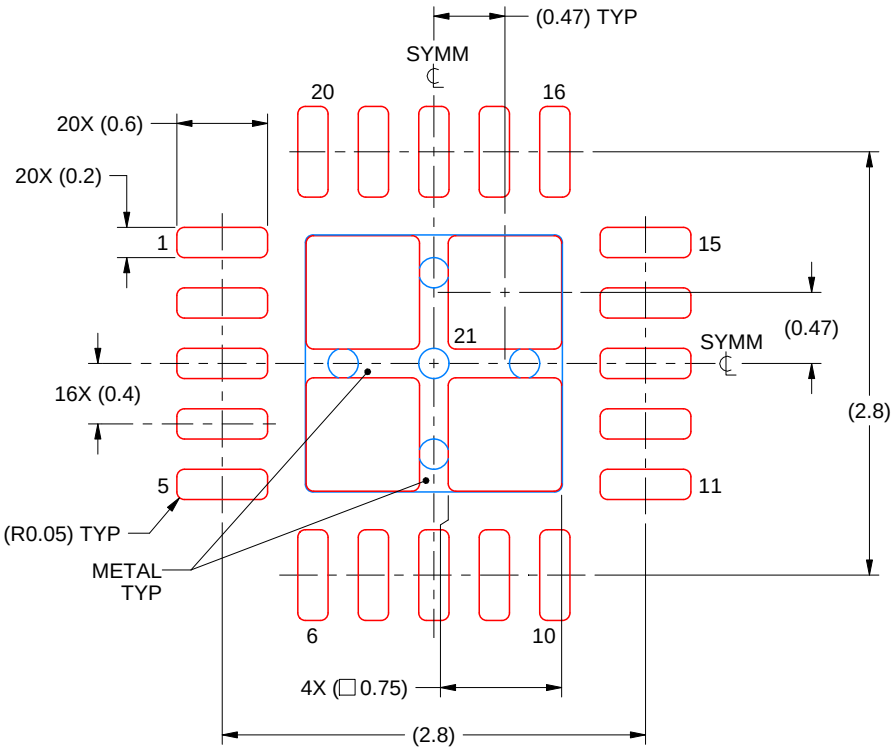
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4229745/A 06/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4229745/A 06/2023

NOTES: (continued)

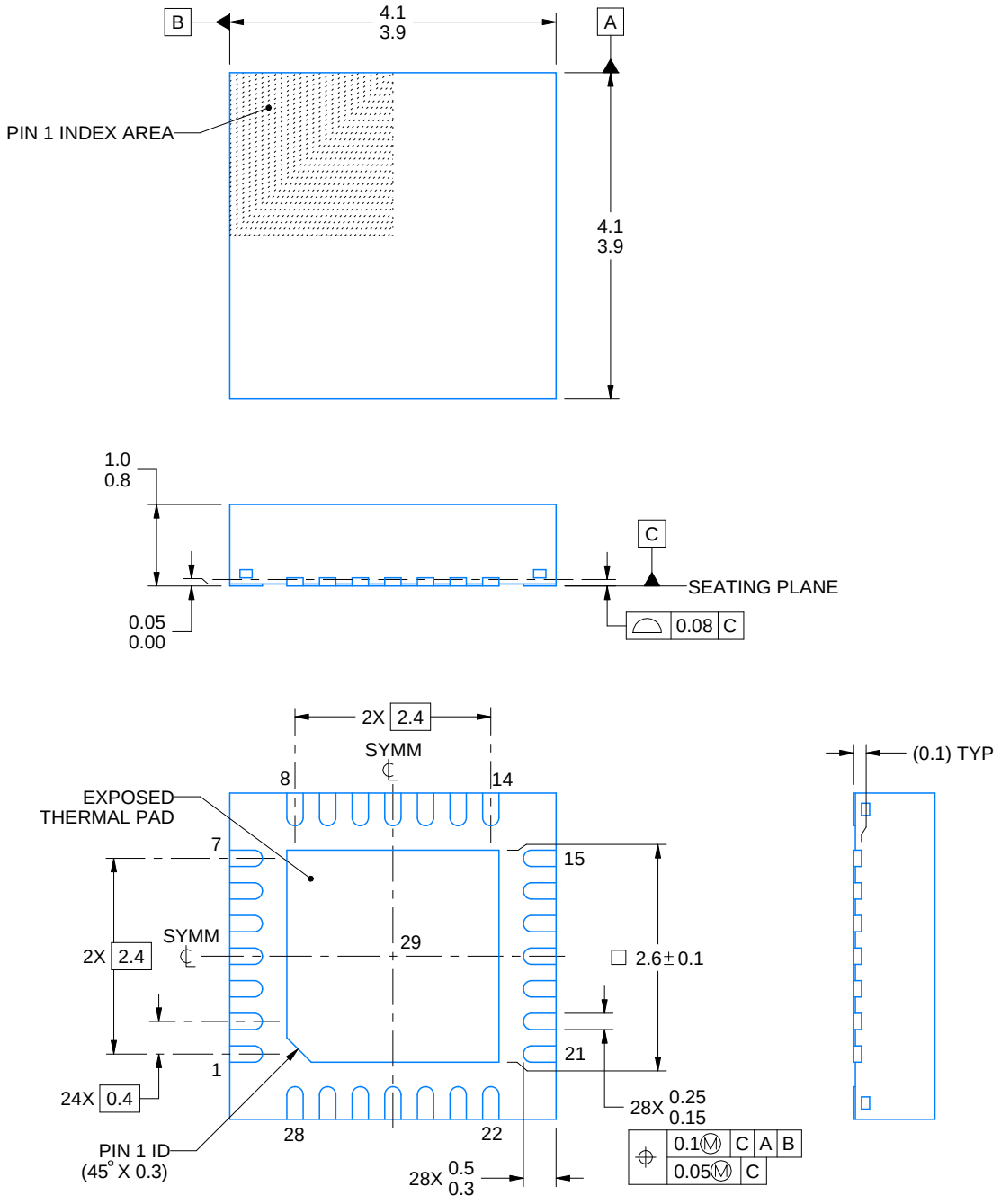
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REX0028A

PACKAGE OUTLINE

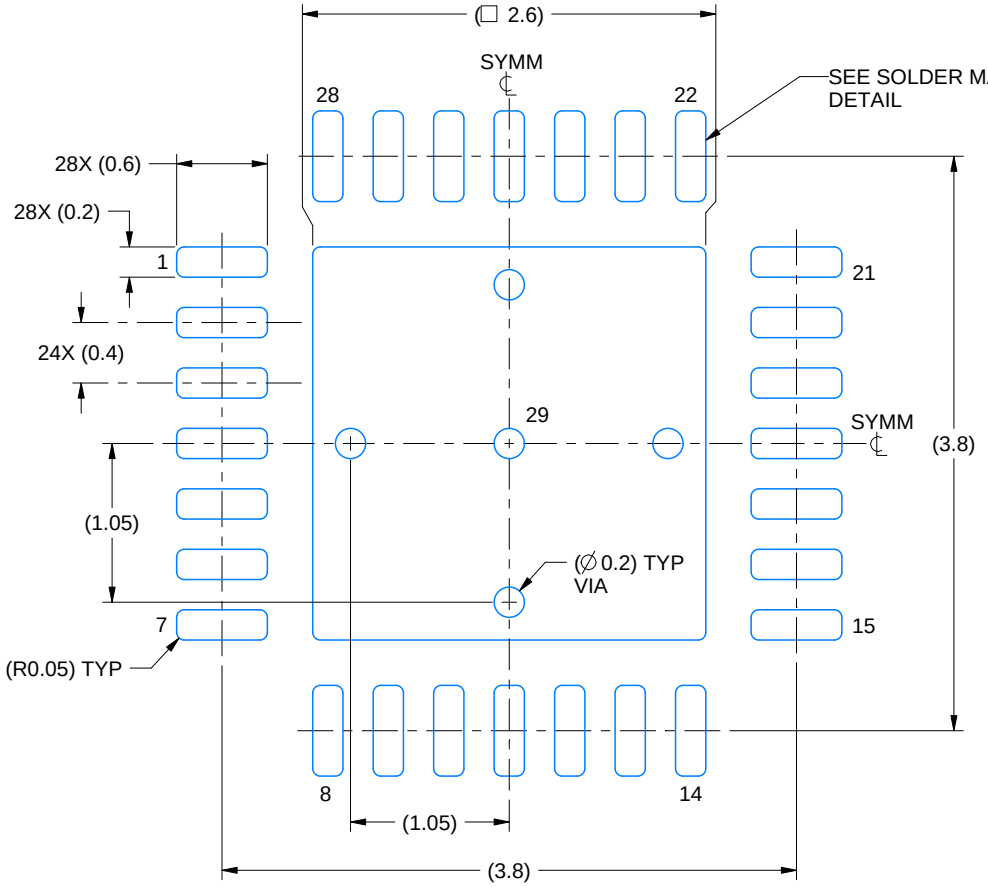
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

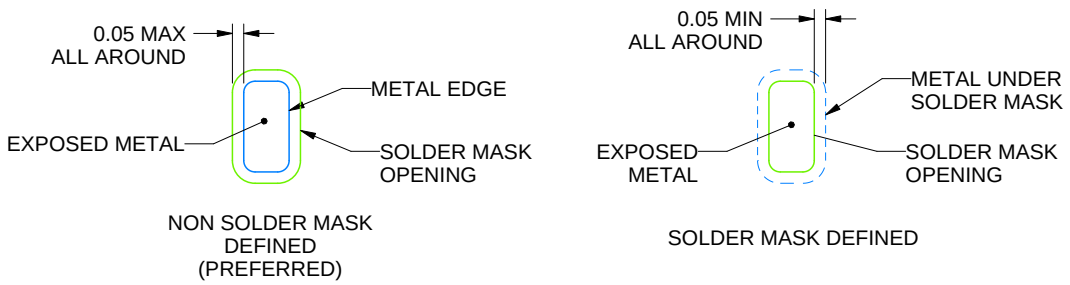


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

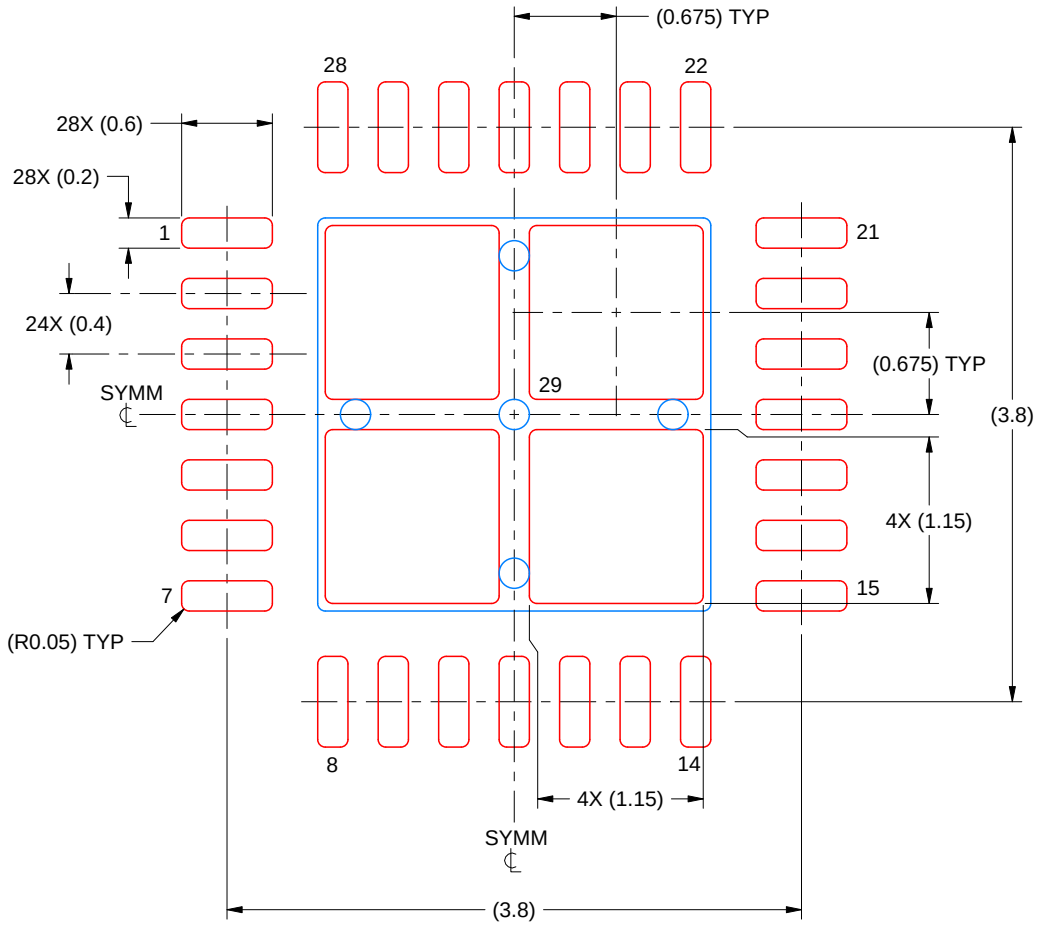


SOLDER MASK DETAILS

4229744/B 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229744/B 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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