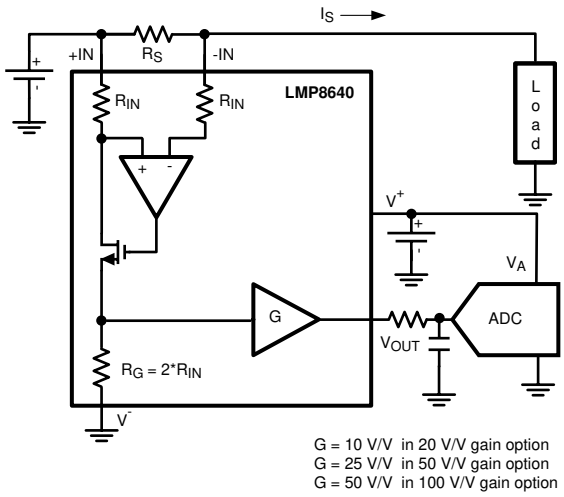
LMP8640/HV Precision High Voltage Current Sense Amplifiers

1 Features

- High Common-Mode Voltage Range
  - LMP8640: -2V to 42V
  - LMP8640HV: -2V to 76V
- Supply Voltage Range: 2.7V to 12V
- Gain Options: 20V/V; 50V/V; 100V/V
- Max Gain Error: 0.25%
- Low Offset Voltage: 900µV
- Input Bias Current: 13µA
- PSRR: 85dB
- CMRR (2.1V to 42V): 103dB
- Temperature Range: -40°C to 125°C
- 6-Pin Thin SOT-23 Package

2 Applications

- Medical CPAP & Ventilators
- Active Antenna (AAS)
- Remote Radio Unit (RRU)
- Server Motherboard Power



Typical Application

3 Description

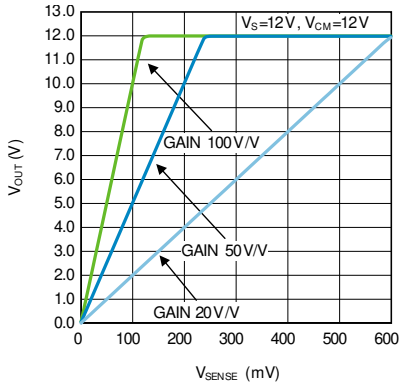
The LMP8640 and the LMP8640HV are precision current sense amplifiers that detect small differential voltages across a sense resistor in the presence of high input common mode voltages with a supply voltage range from 2.7V to 12V.

The LMP8640 accepts input signals with common mode voltage range from -2V to 42V, while the LMP8640HV accepts input signal with common mode voltage range from -2V to 76V. The LMP8640 and LMP8640HV have fixed gain for applications that demand accuracy over temperature. The LMP8640 and LMP8640HV come out with three different fixed gains 20V/V, 50V/V, 100V/V providing a gain error as low as 0.25%. The output is buffered to provide low output impedance. This high side current sense amplifier is ideal for sensing and monitoring currents in DC or battery powered systems, excellent AC and DC specifications over temperature, and keeps errors in the current sense loop to a minimum. The LMP8640 and LMP8640HV are designed for industrial and consumer applications. The LMP8640x is available in SOT-23-6 package.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)
LMP8640	DDC (SOT23, 6)	2.9mm x 2.8mm
LMP8640HV		

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Output Voltage vs. Input Voltage

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison

Table 4-1. Device Comparison

DEVICE NAME	GAIN	QUALIFICATIONS	MAX COMMON MODE VOLTAGE
LMP8640-T	x20		-2V to +42V
LMP8640-F	x50		-2V to +42V
LMP8640-H	x100		-2V to +42V
LMP8640HV-T	x20		-2V to +76V
LMP8640HV-F	x50		-2V to +76V
LMP8640HV-H	x100		-2V to +76V

5 Pin Configuration and Functions

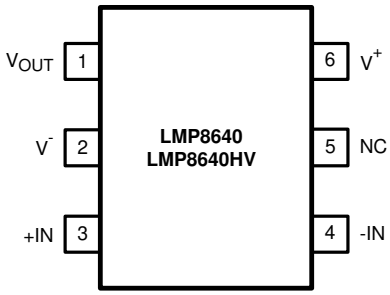


Figure 5-1. 6-Pin SOT-23DDC0006A Package(Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{OUT}	Output	Output
2	V^-	Power	Negative Supply Voltage
3	+IN	Input	Positive Input
4	–IN	Input	Negative Input
5	NC	-	Not Internally Connected
6	V^+	Power	Positive Supply Voltage

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6 Specifications

6.1 Absolute Maximum Ratings

(1)(2)			MIN	MAX	UNIT
Supply Voltage ($V_S = V^+ – V^–$)			-0.3	13.2	V
Differential Voltage +IN- (-IN)			-6	6	V
Voltage at pins +IN, -IN		LMP8640HV	-6	80	V
		LMP8640	-6	60	V
Voltage at V_{OUT} pin			V^-	V^+	V
T_J	Junction Temperature (3)		-40	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) For soldering specifications,see product folder at www.ti.com and http://www.ti.com/lit/SNOA549.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage ($V_S = V^+ - V^–$)	2.7	12	V
Operating Junction Temperature Range	-40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMP8640 LMP8640HV THIN SOT-23 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	
ψ_{JT}	Junction-to-top characterization parameter	41.1	
ψ_{JB}	Junction-to-board characterization parameter	55.8	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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6.5 Electrical Characteristics 2.7V

Unless otherwise specified, all limits verified at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 2.7V, V^- = 0 V, −2V < V_{CM} < 76V, R_L = 10MΩ.(1)

PARAMETER		TEST CONDITIONS	MIN(3)	TYP(2)	MAX(3)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1V	-900		900	µV
		V_{CM} = 2.1V, Over Temperature	-1160		1160	
TCV_{OS}	Input Offset Voltage Drift(4) (6)	V_{CM} = 2.1V			2.6	µV/°C
I_B	Input Bias Current (7)	V_{CM} = 2.1V, V_{SENSE} = 0V		12	20	µA
		V_{CM} = 2.1V, Over Temperature, V_{SENSE} = 0V			27	
e_{ni}	Input Voltage Noise (6)	f > 10kHz		117		nV/√Hz
Gain A_V	Gain LMP8640-T LMP8640HV-T			20		V/V
	Gain LMP8640-F LMP8640HV-F			50		
	Gain LMP8640-H LMP8640HV-H			100		
	Gain error	V_{CM} = 2.1V	-0.25%		0.25%	
		V_{CM} = 2.1V, Over Temperature	-0.51%		0.51%	
	Accuracy over temperature(6)	V_{CM} = 2.1V, Over Temperature			26.2	ppm/°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1V, 2.7V < V^+ < 12V,	85			dB
CMRR	Common Mode Rejection Ratio	LMP8640HV 2.1V < V_{CM} < 42V LMP8640 2.1V < V_{CM}< 42V	103			dB
		LMP8640HV 2.1V < V_{CM} < 76V	95			
		-2V <V_{CM} < 2V,	60			
BW	Fixed Gain LMP8640-T LMP8640HV-T (6)	DC V_{SENSE} = 67.5mV, C_L = 30pF,R_L= 1MΩ		950		kHz
	Fixed Gain LMP8640-F LMP8640HV-F (6)	DC V_{SENSE} =27mV, C_L = 30pF, R_L= 1MΩ		450		
	Fixed Gain LMP8640-H LMP8640HV-H (6)	DC V_{SENSE} = 13.5mV, C_L = 30pF, R_L= 1MΩ		230		
SR	Slew Rate (5)(6)	V_{CM} =5V, C_L = 30pF, R_L = 1MΩ, LMP8640-T LMP8640HV-T V_{SENSE} =100mVpp, LMP8640-F LMP8640HV-F V_{SENSE} =40mVpp, LMP8640-H LMP8640HV-H V_{SENSE} =20mVpp,		1.4		V/µs
R_{IN}	Differential Mode Input Impedance(6)			4		kΩ
I_S	Supply Current	V_{CM} = 2.1V		420	600	µA
		V_{CM} = 2.1V, Over Temperature			800	
		V_{CM} = −2V		2000	2500	
		V_{CM} = −2V, Over Temperature			2750	
V_{OUT}	Maximum Output Voltage	V_{CM} = 2.1V	2.65			V
	Minimum Output Voltage	LMP8640-T LMP8640HV-T V_{CM} = 2.1V			18.2	mV
		LMP8640-F LMP8640HV-F V_{CM} = 2.1V			40	
		LMP8640-H LMP8640HV-H V_{CM} = 2.1V			80	
C_{LOAD}	Max Output Capacitance Load(6)			30		pF

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device can be permanently degraded, either mechanically or electrically.

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(2) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlations using statistical quality control (SQC) method.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.
(6) This parameter is verified by design and/or characterization and is not tested in production.
(7) Positive Bias Current corresponds to current flowing into the device. Specification does not include input signal dependent currents on the positive input of approximately Vsense / 4KΩ due to topology feedback action.

6.6 Electrical Characteristics 5 V

Unless otherwise specified, all limits verified at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 5V, V^- = 0V, −2V < V_{CM} < 76V, R_L = 10MΩ. (1)

PARAMETER		TEST CONDITIONS	MIN(3)	TYP(2)	MAX(3)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1 V	-900		900	µV
		V_{CM} = 2.1 V, Over Temperature	-1160		1160	
TCV_{OS}	Input Offset Voltage Drift(4) (6)	V_{CM} = 2.1 V			2.6	µV/°C
I_B	Input Bias Current (7)	V_{CM} = 2.1 V, V_{SENSE} = 0 V		13	21	µA
		V_{CM} = 2.1 V, Over Temperature,V_{SENSE} = 0 V			28	
e_{ni}	Input Voltage Noise (6)	f > 10 kHz		117		nV/√Hz
Gain A_V	Gain LMP8640-T LMP8640HV-T			20		V/V
	Gain LMP8640-F LMP8640HV-F			50		
	Gain LMP8640-H LMP8640HV-H			100		
	Gain error	V_{CM} = 2.1 V	-0.25%		0.25%	
		V_{CM} = 2.1 V, Over Temperature	-0.51%		0.51%	
	Accuracy over temperature(6)	−40°C to 125°C, V_{CM}=2.1 V			26.2	ppm/°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1 V, 2.7V < V^+ < 12 V,	85			dB
CMRR	Common Mode Rejection Ratio	LMP8640HV 2.1V < V_{CM} < 42V LMP8640 2.1V < V_{CM}< 42V	103			dB
		LMP8640HV 2.1V < V_{CM} < 76V	95			
		-2 V <V_{CM} < 2 V,	60			
BW	Fixed Gain LMP8640-T LMP8640HV-T (6)	DC V_{SENSE} = 67.5 mV, C_L = 30 pF, R_L= 1 MΩ		950		kHz
	Fixed Gain LMP8640-F LMP8640HV-F (6)	DC V_{SENSE} =27 mV, C_L = 30 pF, R_L= 1 MΩ		450		
	Fixed Gain LMP8640-H LMP8640HV-H (6)	DC V_{SENSE} = 13.5 mV, C_L = 30 pF, R_L= 1MΩ		230		
SR	Slew Rate (5)(6)	V_{CM} =5 V, C_L = 30 pF, R_L = 1MΩ, LMP8640-T LMP8640HV-T V_{SENSE} = 200 mVpp, LMP8640-F LMP8640HV-F V_{SENSE} = 80 mVpp, LMP8640-H LMP8640HV-H V_{SENSE} = 40 mVpp,		1.6		V/µs
R_{IN}	Differential Mode Input Impedance(6)			4		kΩ
I_S	Supply Current	V_{CM} = 2.1 V		500	722	µA
		V_{CM} = 2.1 V, Over Temperature			922	
		V_{CM} = −2 V		2050	2500	
		V_{CM} = −2 V, Over Temperature			2750	

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Unless otherwise specified, all limits verified at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 5V, V^- = 0V, −2V < V_{CM} < 76V, R_L = 10MΩ. (1)

PARAMETER		TEST CONDITIONS	MIN(3)	TYP(2)	MAX(3)	UNIT
V_{OUT}	Maximum Output Voltage	V_{CM} = 2.1 V	4.95			V
	Minimum Output Voltage	LMP8640-T LMP8640HV-T V_{CM} = 2.1 V			18.2	mV
		LMP8640-F LMP8640HV-F V_{CM} = 2.1 V			40	
		LMP8640-H LMP8640HV-H V_{CM} = 2.1 V			80	
C_{LOAD}	Max Output Capacitance Load(6)			30		pF

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6.7 Electrical Characteristics 12V

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 12V, V^- = 0V, −2V < V_{CM} < 76V, R_L = 10MΩ. (1)

PARAMETER		TEST CONDITIONS	MIN(3)	TYP(2)	MAX(3)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1V	-900		900	µV
		V_{CM} = 2.1V, Over Temperature	-1160		1160	
TCV_{OS}	Input Offset Voltage Drift(4) (6)	V_{CM} = 2.1V			2.6	µV/°C
I_B	Input Bias Current (7)	V_{CM} = 2.1V, V_{SENSE} = 0V		13	22	µA
		V_{CM} = 2.1V, Over Temperature, V_{SENSE} = 0V			28	
e_{ni}	Input Voltage Noise (6)	f > 10kHz		117		nV/√Hz
Gain A_V	Gain LMP8640-T LMP8640HV-T			20		V/V
	Gain LMP8640-F LMP8640HV-F			50		
	Gain LMP8640-F LMP8640HV-F			100		
	Gain error	V_{CM} = 2.1V	-0.25%		0.25%	
		V_{CM} = 2.1V, Over Temperature	-0.51%		0.51%	
	Accuracy over temperature(6)	−40°C to 125°C, V_{CM}= 2.1V			26.2	ppm/°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1V, 2.7V < V^+ < 12V,	85			dB
CMRR	Common Mode Rejection Ratio	LMP8640HV 2.1V < V_{CM} < 42V LMP8640 2.1V < V_{CM}< 42V	103			dB
		LMP8640HV 2.1V < V_{CM} < 76V	95			
		-2V < V_{CM} < 2V,	60			
BW	Fixed Gain LMP8640-T LMP8640HV-T (6)	DC V_{SENSE} = 67.5mV, C_L = 30pF, R_L= 1MΩ		950		kHz
	Fixed Gain LMP8640-F LMP8640HV-F (6)	DC V_{SENSE} =27mV, C_L = 30pF, R_L= 1MΩ		450		
	Fixed Gain LMP8640-H LMP8640HV-H (6)	DC V_{SENSE} = 13.5mV, C_L = 30pF, R_L= 1MΩ		230		
SR	Slew Rate (5)(6)	V_{CM} =5V, C_L = 30pF, R_L = 1MΩ, LMP8640-T LMP8640HV-T V_{SENSE} =100mVpp, LMP8640-F LMP8640HV-F V_{SENSE} =40mVpp, LMP8640-H LMP8640HV-H V_{SENSE} =20mVpp,		1.8		V/µs
R_{IN}	Differential Mode Input Impedance(6)			4		kΩ
I_S	Supply Current	V_{CM} = 2.1V		720	1050	µA
		V_{CM} = 2.1V, Over Temperature			1250	
		V_{CM} = −2V		2300	2800	
		V_{CM} = −2V, Over Temperature			3000	
V_{OUT}	Maximum Output Voltage	V_{CM} = 2.1V	11.85			V
	Minimum Output Voltage	LMP8640-T LMP8640HV-T V_{CM} = 2.1V			18.2	mV
		LMP8640-F LMP8640HV-F V_{CM} = 2.1V			40	
		LMP8640-H LMP8640HV-H V_{CM} = 2.1V			80	
C_{LOAD}	Max Output Capacitance Load(6)			30		pF

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6.8 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

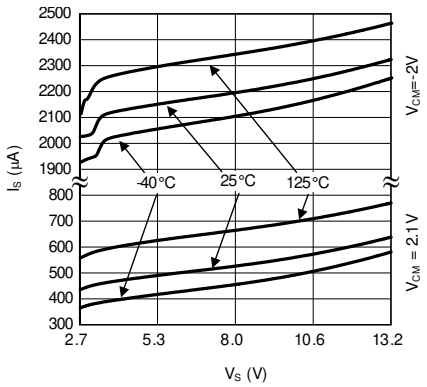


Figure 6-1. Supply Current vs. Supply Voltage

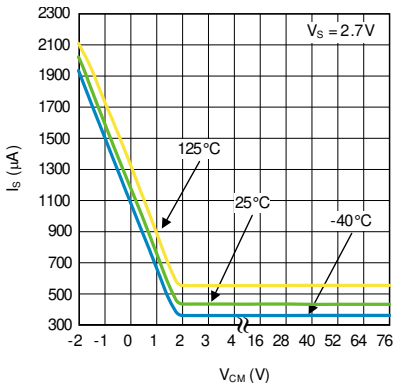


Figure 6-2. Supply Current vs. V_{CM}

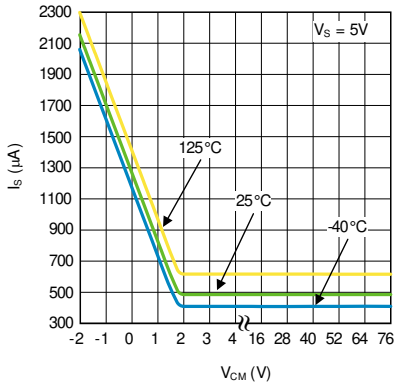


Figure 6-3. Supply Current vs. V_{CM}

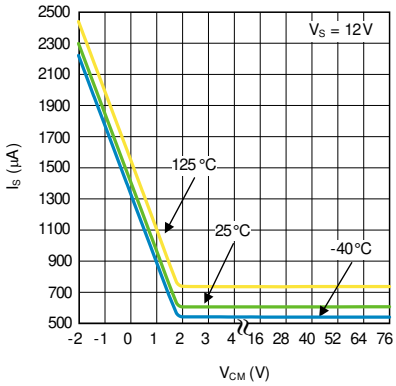


Figure 6-4. Supply Current vs. V_{CM}

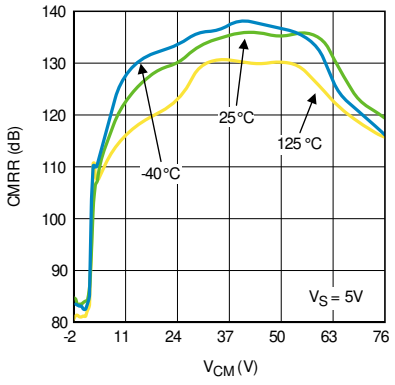


Figure 6-5. CMRR vs. V_{CM} (Gain 20 V/V)

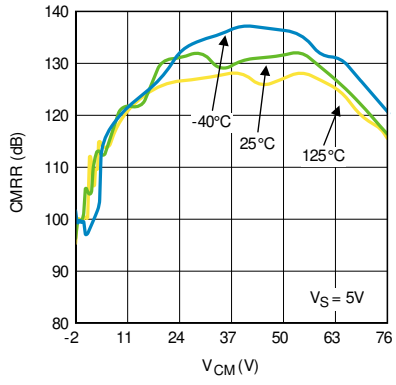


Figure 6-6. CMRR vs. V_{CM} (Gain 50 V/V)

6.8 Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

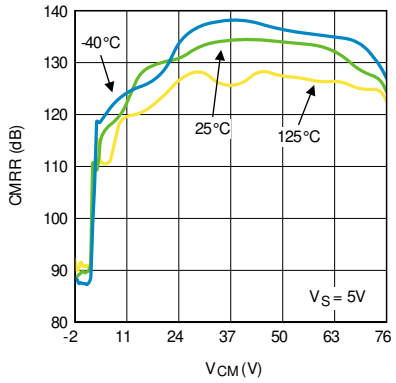


Figure 6-7. CMRR vs. V_{CM} (Gain 100 V/V)

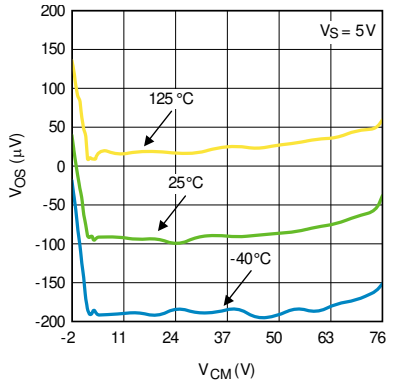


Figure 6-8. Input Voltage Offset vs. V_{CM}

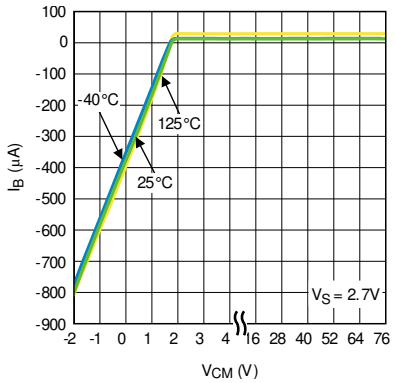


Figure 6-9. Ibias vs. V_{CM}

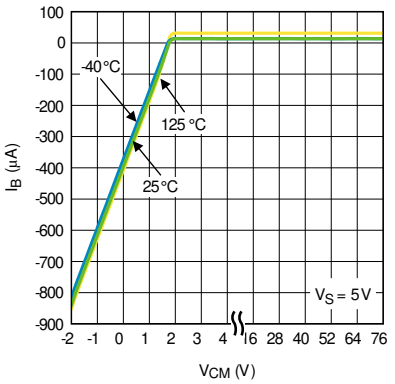


Figure 6-10. Ibias vs. V_{CM}

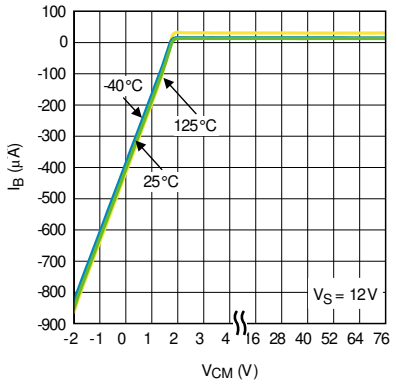


Figure 6-11. Ibias vs. V_{CM}

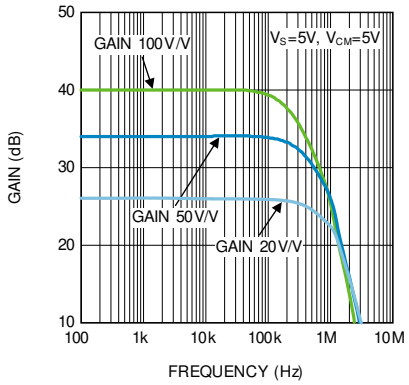


Figure 6-12. Gain vs. Frequency

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6.8 Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

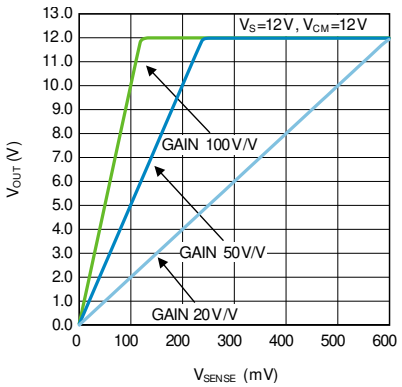


Figure 6-13. Output voltage vs. V_{SENSE}

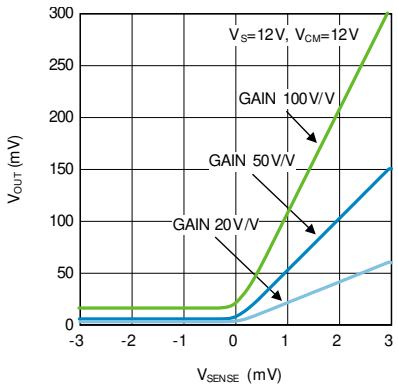


Figure 6-14. Output Voltage vs. V_{SENSE} (ZOOM Close to 0 V)

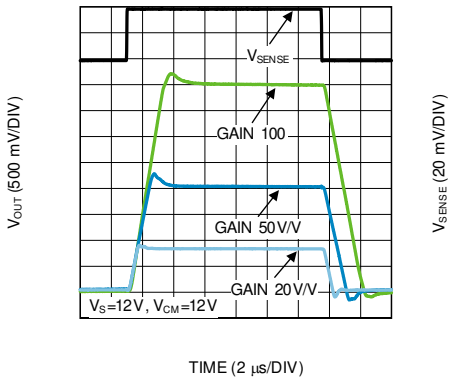


Figure 6-15. Large Step Response

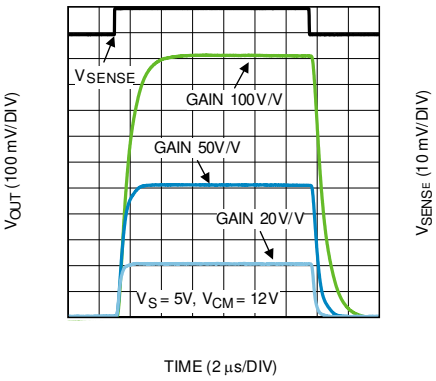


Figure 6-16. Small Step Response

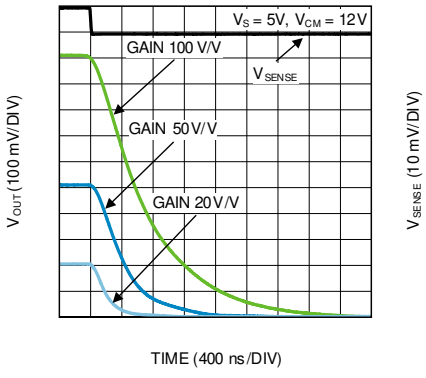


Figure 6-17. Settling Time (Fall)

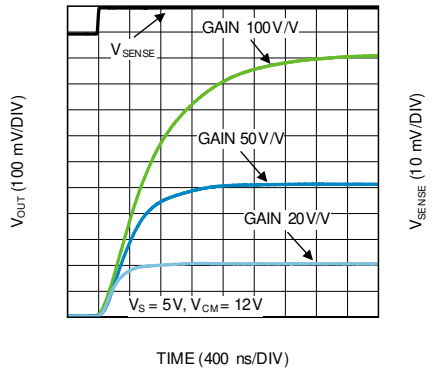


Figure 6-18. Settling Time (Rise)

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6.8 Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

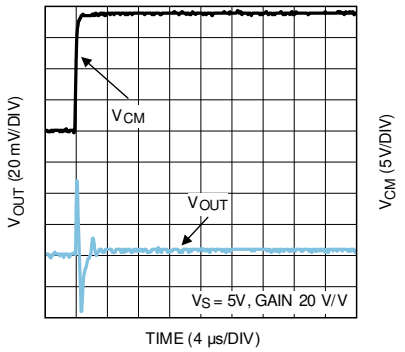


Figure 6-19. Common Mode Step Response (Rise)

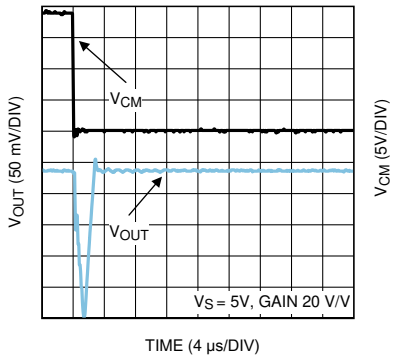


Figure 6-20. Common Mode Step Response (Fall)

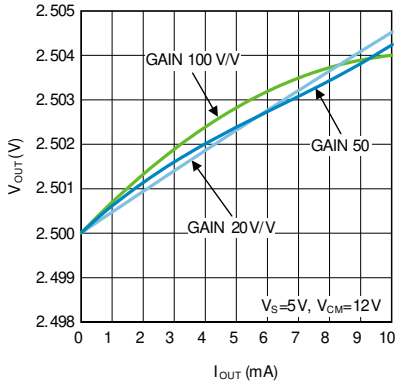


Figure 6-21. Load Regulation (Sinking)

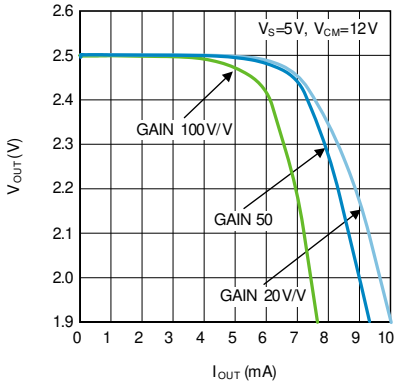


Figure 6-22. Load Regulation (Sourcing)

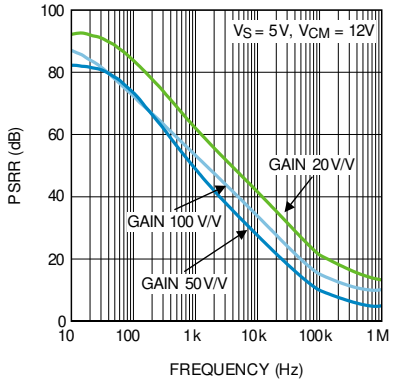


Figure 6-23. AC PSRR vs. Frequency

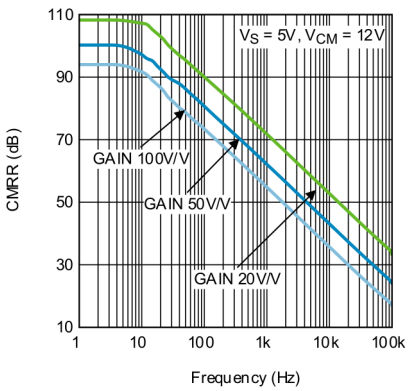


Figure 6-24. AC CMRR vs. Frequency

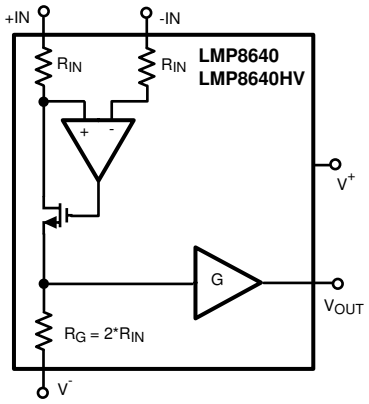
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7 Detailed Description

7.1 Overview

The LMP8640 and LMP8640HV are single supply high side current sense amplifiers with a fixed gain of 20V/V, 50V/V, 100V/V and a common mode voltage range of -2V to 42V (LMP8640) or -2V to 76V (LMP8640HV) with a buffered voltage output.

7.2 Functional Block Diagram



7.3 Feature Description

As seen in Figure 7-1, the current flowing through sense resistor R_S develops a voltage drop equal to V_{SENSE} across R_S. The voltage at the -IN pin is now less than +IN by an amount proportional to the V_{SENSE} voltage.

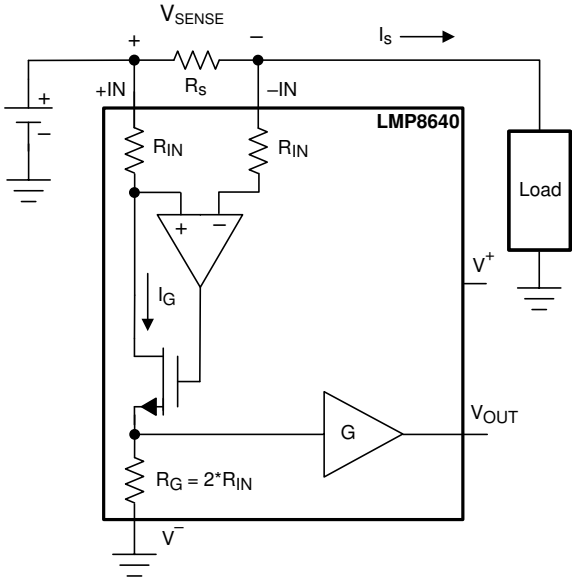


Figure 7-1. Simple Current Monitor

The low bias currents of the error amplifier cause little voltage drop through R_{IN-}, so the negative input of the internal error amplifier is at essentially the same potential as the -IN input. The R_{IN} resistors are 4kΩ each.

The error amplifier detects this voltage error between the inputs and drive the MOSFET gate to conduct more current, increasing the voltage drop across R_{IN+}, until the servo amplifiers positive input matches the negative input. At this point, the voltage drop across R_{IN+} now matches V_{SENSE}.

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I_G, a current proportional to I_S, flows according to the following relation:

$$I_G = V_{SENSE}/R_{IN} = R_S \times I_S/R_{IN} \quad (1)$$

I_G also flows through the internal gain resistor R_G developing a voltage drop equal to:

$$V_{RG} = I_G \times R_G = (V_{SENSE}/R_{IN}) \times R_G = ((R_S \times I_S)/ R_{IN}) \times R_G \quad (2)$$

$$V_{OUT} = 2 \times (R_S \times I_S) \times G, \quad (3)$$

where G = 10 V/V, 25 V/V or 50 V/V, according to the gain option selected.

The voltage on R_G is then amplified by a gain of the output gain stage to create the final overall gain of x20, x50 and x100. The output stage has a low impedance drive allowing LMP8640 and LMP8640HV to easily interface with other ICs (ADC, Mux, µC…). No external buffering is required.

7.3.1 Selection of Sense Resistor

The value selected for the shunt resistor, R_S, depends on the application. The shunt resistor plays a big role in a current sensing system and must be selected with care. The selection of the shunt resistor needs to take in account the tradeoffs in small-signal accuracy, the power dissipated and the voltage loss across the shunt.

In applications where a small current is sensed, a bigger value of R_S is selected to minimize the error in the proportional output voltage. Higher resistor value improves the signal-to-noise ratio (SNR) at the input of the current sense amplifier and hence gives a more accurate output.

Similarly when high current is sensed, the power losses in R_S can be significant so a smaller value of R_S is desired. Taking into account the power rating of the R_s resistor is required in this condition. The low input offset of LMP8640 and LMP8640HV allow the use of small sense resistors to reduce power dissipation still providing a good input dynamic range. The input dynamic range is the ratio between the maximum signal that can be measured and the minimum signal that can be detected, where typically the input offset is the principal limiting factor.

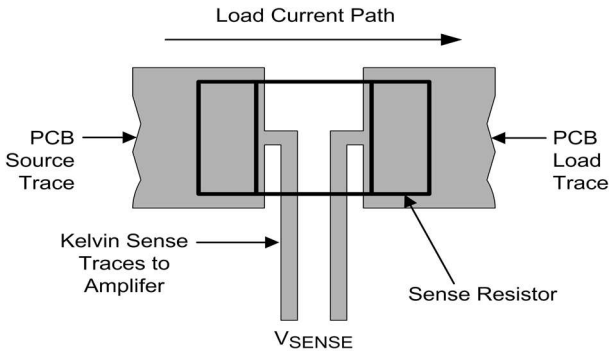


Figure 7-2. Example of a Kelvin (4-Wire) Connection to a Two-Terminal Resistor

The amplifier inputs must be directly connected to the sense resistor pads using “Kelvin” or “4-wire” connection techniques. The paths of the input traces must be identical, including connectors and vias, so that these errors are equal and cancel.

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7.3.1.1 Resistor Power Rating and Thermal Issues

The power dissipated by the sense resistor can be calculated from:

$$P_D = I_{MAX}^2 \times R_S \quad (4)$$

where

- P_D is the power dissipated by the resistor in Watts
- I_{MAX} is the maximum load current in Amps
- R_S is the sense resistor value in ohms.

The resistor must be rated for more than the expected maximum power (P_D), with margin for temperature derating. Be sure to observe any power derating curves provided by the resistor manufacturer.

Running the resistor at higher temperatures also affects the accuracy. As the resistor heats up, the resistance generally goes up, which causes a change in the measurement. The sense resistor must have as much heat-sinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting slightly after turn-on can typically be traced back to sense resistor heating.

7.3.1.2 Using PCB Trace as a Sense Resistor

While using a resistance of a known area of PCB trace or copper area as a sense resistor is a tempting strategy, for precision measurements this strategy is not recommended.

The temperature coefficient of copper is typically 3300-4000ppm/°K (0.33% to 0.4% per °C), which can vary with PCB processes.

A typical surface mount sense resistor temperature coefficient (tempco) is in the 50ppm to 500ppm per °C range offering more measurement consistency and accuracy over the copper trace. Special low tempco resistors are available in the 0.1 to 50ppm range, but at a much higher cost.

7.3.2 Sense Line Inputs

The sense lines must be connected to a point on the resistor that is not shared with the main current path, as shown in Figure 7-2 above. For lowest drift, the amplifier must be mounted away from any heat generating devices, which can include the sense resistor. The traces must be one continuous trace of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if the resistor is generating any significant heat gradients. Vias in the sense lines must be formed from continuous plated copper and routing through connectors must be avoided. Extending the sense lines is better than to place the amplifier in a hostile environment.

To minimize noise pickup and thermal errors, the input traces must be treated like a high-speed differential signal pair and routed tightly together with a direct path to the input pins on the same copper layer. The input traces do not need to be "impedance matched", but must follow the same matching rules about vias, spacing and equal lengths. The input traces must be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these input traces can contain high voltage, and must have the appropriate trace routing clearances to other traces and layers. Since the sense traces only carry the amplifier bias current (typically about 12µA per input at room temp), the connecting input traces can be thin traces running close together. This can help with routing or creating the required spacings.

Note that, due to the nature of the device topology, the positive input bias current varies with V_{SENSE} with an extra current approximately equivalent to V_{SENSE} / 4kΩ on top of the typical 12µA bias current. The negative input bias current is not in the feedback path and does not change over V_{SENSE}. High or miss-matched source impedances must be avoided as this imbalance creates an additional error over input voltage.

7.3.3 Effects of Series Resistance on Sense Lines

Because the input stage uses precision 4KΩ resistors internally to convert the voltage on the input pin to a current, any resistance added in series with the input pins changes this resistance, and thus alter the gain.

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If a resistance is added in series with an input, the gain of that input does not track that of the other input, causing a constant gain error.

Using external resistance to alter the gain is not recommended, as external resistors does not have the same thermal matching as the internal thin film resistors. Any added resistance severely degrades the offset and CMRR specifications. The total trace resistance is recommended to be less than 10Ω.

If resistors are purposely added for filtering, resistance must be added equally to both inputs and the user must be aware that the gain changes slightly.

7.4 Device Functional Modes

7.4.1 Bias Current at Low Common Mode Voltage

At common mode voltages below +2 V, the input bias current starts to reverse and crosses through zero at approximately +1.8 V. This can be seen in the Input Bias Current graphs in Figure 6-9 through Figure 6-11. Negative currents on the graph show current flow *out* of the input and *into* the load. The graphs show the current for each input, so the actual "bias" current is twice the graph value. This total current can be as high as 1mA, depending on the point of equilibrium.

While this does not affect the vast majority of applications, it can cause MOSFET switched designs with non-linear loads (like LEDs or diode-isolated loads) to "float" above ground where the load leakage and bias currents attain equilibrium. A small resistor to ground (on the load supply side) can bleed off this current.

7.4.2 Applying Input Voltage With No Supply Voltage

The full specified input common mode voltage range can be applied to the inputs while LMP8640 and LMP8640HV power is off (V+ = 0 V). When LMP8640 and LMP8640HV is powered off, the R_{IN} resistors are disconnected internally by MOSFETS and the leakage currents are very low (sub µA).

The 6 V input differential limit still applies, so keep the two inputs less than 6 V apart. There are also Zener clamps on the inputs to ground, so do not exceed the input limits specified in the Absolute Maximum Ratings.

7.4.3 Driving an ADC

The input stage of an Analog to Digital converter can be modeled with a resistor and a capacitance to ground. So if the voltage source does not have a low impedance, an error in amplitude measurement occurs. In this case, a buffer is needed to drive the ADC. LMP8640 and LMP8640HV have internal output buffer able to directly drive a capacitive load up to 30 pF, or, the input stage of an ADC. An external low pass RC filter is recommended to be added to the output of LMP8640 and LMP8640HV to reduce the noise and limit the bandwidth of the current sense measurement.

If the supply voltage of LMP8640 and LMP8640HV is higher than the ADC supply voltage, care must be taken to prevent LMP8640 and LMP8640HV output from over-driving the ADC input.

This can be accomplished with a series resistance (which must be present when driving a ADC) and a clamping diode to the ADCs power supply. The diode clamps the ADC input to a safe level. Do not completely rely on a calculated maximum output voltage. Transients or fault conditions outside the normal conditions area can cause the output to swing to a higher than expected voltage.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

LMP8640 or LMP8640HV amplifies the voltage developed across a current-sensing resistor.

8.2 Typical Application

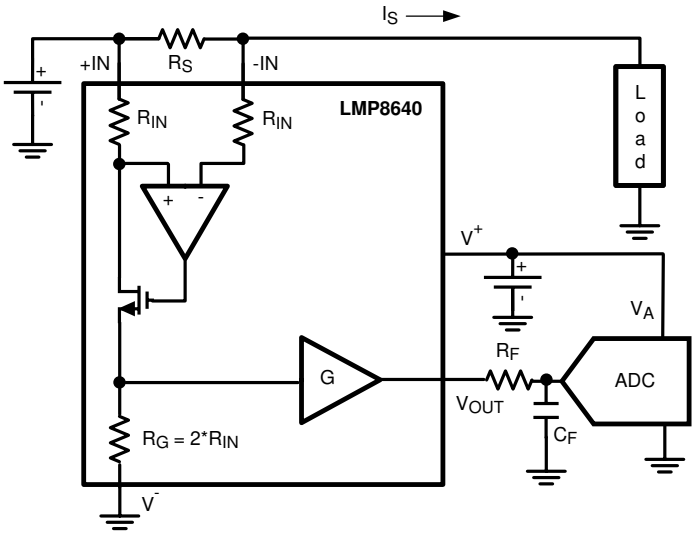


Figure 8-1. Typical Application Example

8.2.1 Design Requirements

In this example, a current monitor application is required to measure the current into a load (peak current 10 A) with a resolution of 10 mA and 0.5% of accuracy.

The 10bit analog to digital converter accepts a maximum input voltage of 4.1 V. To not burn too much power on the shunt resistor, the resistor needs to be less than 10 mΩ. Table 8-1 below summarizes the other design conditions.

Table 8-1. Example Design Requirements

WORKING CONDITION	VALUE	
	MIN	MAX
Supply Voltage	5 V	5.5 V
Common mode Voltage	48 V	70 V
Temperature	0°C	70°C
Signal BW	50 kHz	

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8.2.2 Design Procedure

8.2.2.1 First Step – LMP8640 or LMP8640HV Selection

The required common mode voltage of the application implies that the right choice is the LMP8640HV (High common mode voltage up tp 76 V).

8.2.2.2 Second Step – Gain Option Selection

We can choose between three gain option (20 V/V, 50 V/V, 100 V/V). Considering the maximum input voltage of the ADC (4.1 V), the maximum Sense voltage across the shunt resistor is evaluated according the following formula:

$$V_{SENSE} = (MAX\ Vin\ ADC) / Gain \quad (5)$$

hence the maximum V_{SENSE} is 205 mV, 82 mV, 41 mV respectively. The shunt resistor are then evaluated considering the maximum monitored current:

$$R_S = (max\ V_{SENSE}) / I_MAX \quad (6)$$

For each gain option the maximum shunt resistors are the following: 20.5 mΩ, 8.2 mΩ, 4.1 mΩ respectively.

One of the project constraints requires RS<10 mΩ, so the 20.5 mΩ is discarded and hence the 50 V/V and 100 V/V gain options are still in play.

8.2.2.3 Third Step – Shunt Resistor Selection

At this point an error budget calculation, considering the calibration of the Gain, Offset, CMRR, and PSRR, helps in the selection of the shunt resistor. In the table below the contribution of each error source is calculated considering the values of the Electrical Characteristics table at 5 V supply.

Table 8-2. Resolution Calculation

ERROR SOURCE	R_S = 4.1 mΩ	R_S = 8.1 mΩ
CMRR calibrated at mid VCM range	77.9 µV	77.9 µV
PSRR calibrated at 5 V	8.9 µV	8.9 µV
Total error (squared sum of contribution)	78 µV	78 µV
Resolution (Total error / R_S)	19.2 mA	9.6 mA

Table 8-3. Accuracy Calculation

ERROR SOURCE	R_S = 4.1 mΩ	R_S = 8.1 mΩ
Tc Vos	182 µV	182 µV
Noise	216 µV	216 µV
Gain drift	75.2 µV	151 µV
Total error (squared sum of contribution)	293 µV	320 µV
Accuracy 100×(Max_V_{SENSE} / Total Error)	0.7%	0.4%

From the tables above is clear that the 8.2 mΩ shunt resistor allows the respect of the project constraints. The power burned on the Shunt is 820 mW at 10 A.

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8.2.3 Application Curve

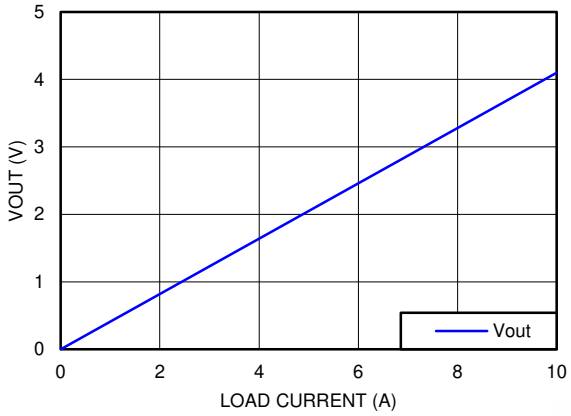


Figure 8-2. Application Example Results Using 8.2-mΩ Resistor

8.3 What to Do and What Not to Do

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, cables, long traces, muxes and ADC inputs.

Do not exceed the input common mode range.

8.4 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond the power supply voltage, V^+. For example, the voltage applied to the versus power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as +76 V. Power-supply bypass capacitors are required for stability and must be placed as closely as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF close to the V^+ pin. The capacitors must be rated for at least twice the maximum expected applied voltage. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

8.5 Layout

8.5.1 Layout Guidelines

- Use 4-wire (Kelvin) connections to the sense resistor. Connect to the resistor at a point that is not within a direct high-current path (See Figure 8-3).
- Do not "share" part of the sense trace path with the load current.
- Maintain proper clearance and spacings around the input traces, as the traces can be at a higher voltage (up to 76 V) than the surrounding traces and planes.
- Input traces from the sense resistor pads must follow the same path, be spaced tightly together, and ideally on the same copper layer.
- Vias used in the input traces must be of continuous plated copper to avoid creating thermocouples.
- Avoid routing inputs through jumpers and connectors. Even the best connectors introduce thermal errors ("thermocouples"). Each input trace must have the same number of "thermocouples" if the "thermocouples" can not be avoided.
- Keep the amplifier away from heat generating devices. The copper-solder-lead junction on the input pins form a thermocouple. The copper mass must be equal on both input pins.
- Avoid temperature gradients across the input pins. Input pins must be equal distance to the heat source.
- Place the LMP8640 in the most temperature-stable area possible and away from high-velocity air flows. Carefully extending the input traces is better than to place the amplifier in a less-than-ideal environment.
- Give the sense resistor as much copper trace area as possible to dissipate heat as the resistor value changes slightly with temperature. Also see the resistor manufacturers data sheet or application notes for further layout guidelines.

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- The power-supply bypass capacitor must be placed as closely as possible to the supply and ground terminals. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

8.5.2 Layout Example

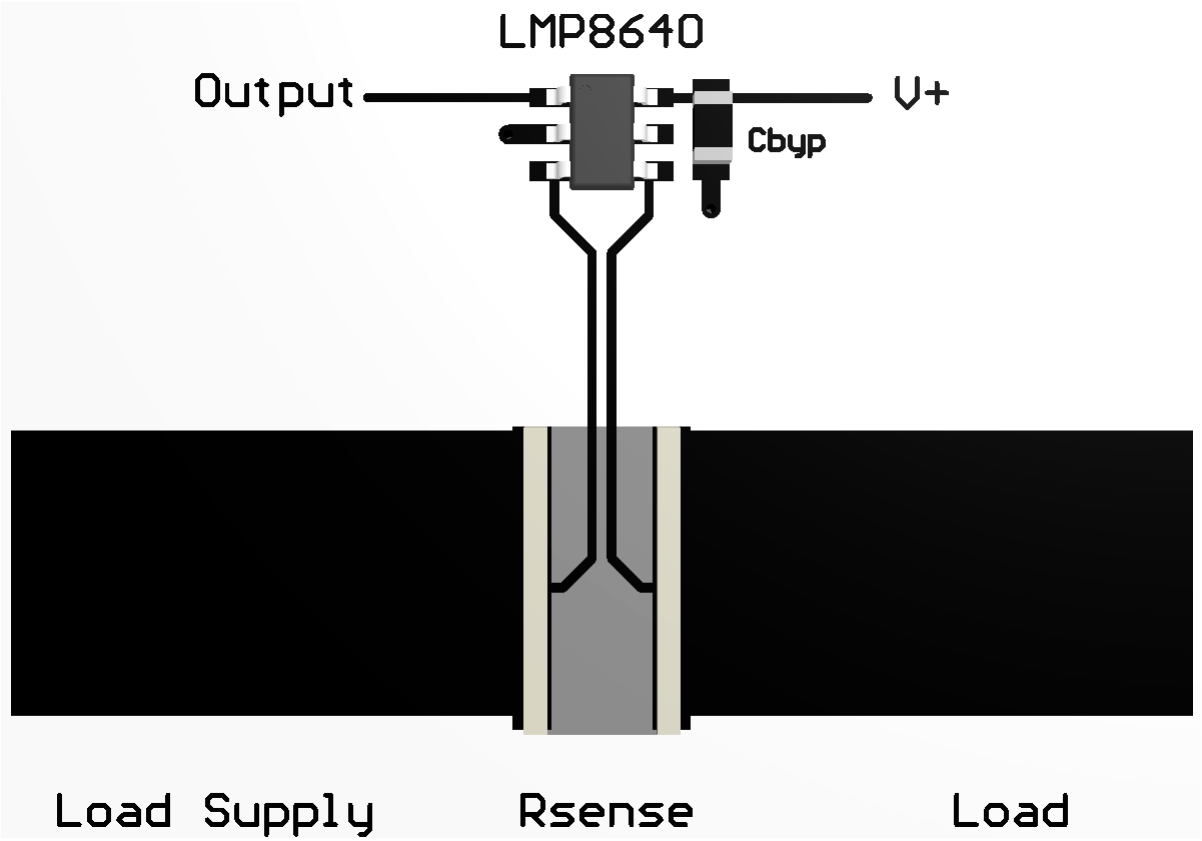


Figure 8-3. Layout Example - Kelvin Connection to a Two-Terminal Resistor

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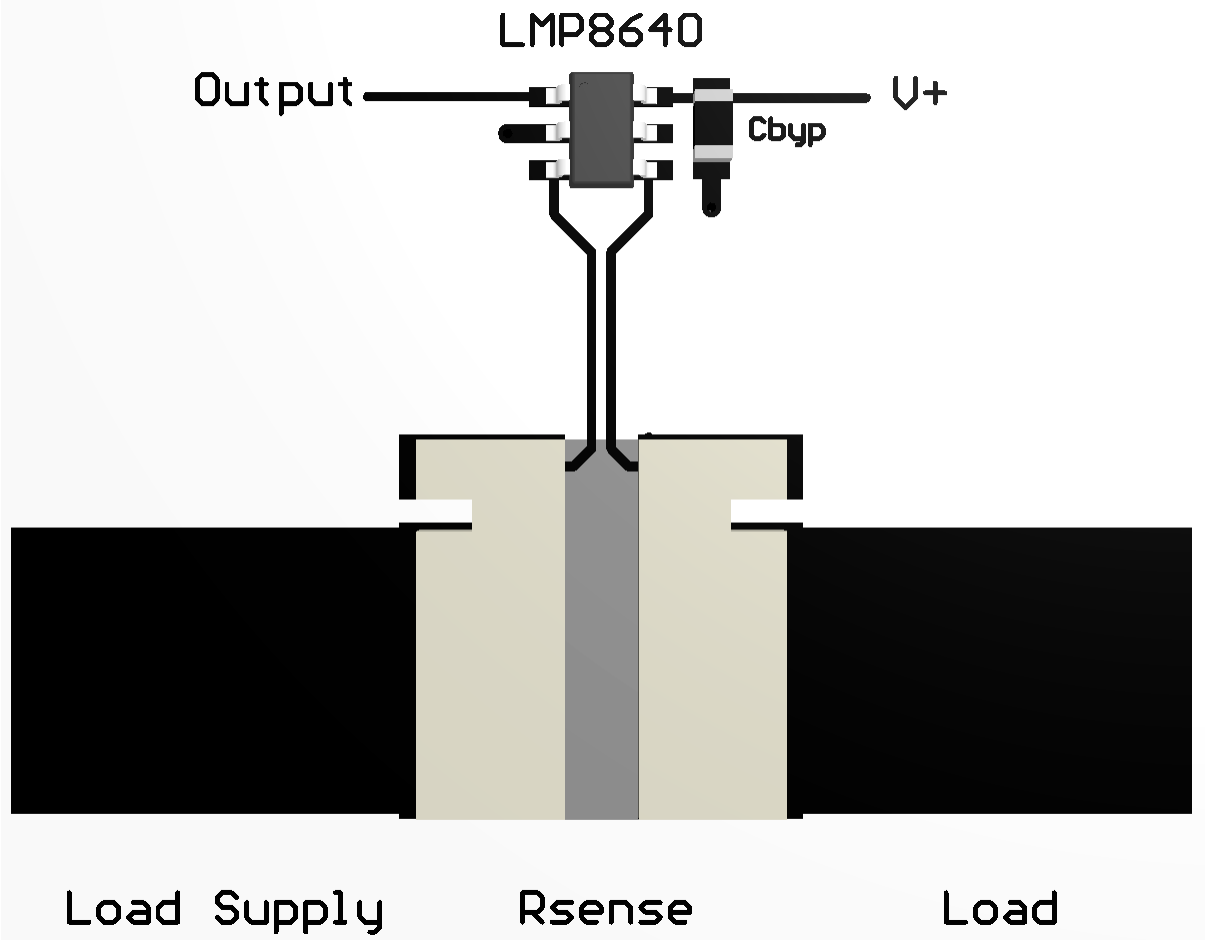


Figure 8-4. Layout Example - Four-Wire (Kelvin) Resistor Connection

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

- Evaluation Board for LMP8640HV-F, http://www.ti.com/tool/lmp8640hv-feval
- Evaluation Board for LMP8640HV-H, http://www.ti.com/tool/lmp8640hv-heval
- Evaluation Board for LMP8640HV-T, http://www.ti.com/tool/lmp8640hv-teval
- TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, AN-1975 LMP8640 / LMP8645 Evaluation Board User Guide
- Texas Instruments, Absolute Maximum Ratings for Soldering application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (November 2014) to Revision H (October 2026)	Page
• Moved the automotive device to a standalone data sheet (SNOSDI6)	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the ESD Ratings table and moved the storage temperature parameter to the *Absolute Maximum Ratings* table	1
• Machine Model ESD rating is removed	4
• Human-body model (HBM) for +IN and -IN pins are changed to ± 2000V to match with all other pins	4
• Thermal information is updated	4
• Differential Mode Input Impedance is changed to 4kΩ in *Electrical Characteristics 2.7V table*	5

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- Differential Mode Input Impedance is changed to 4kΩ *Electrical Characteristics 5V table* 6
- Differential Mode Input Impedance is changed to 4kΩ *Electrical Characteristics 12V table* 8
- Added section 19

Changes from Revision F (April 2013) to Revision G (November 2014) **Page**

- New Q Device added to data sheet 1
- Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP8640HVMK-F/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AD6A
LMP8640HVMK-H/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AF6A
LMP8640HVMKE-F/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AD6A
LMP8640HVMKE-H/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AF6A
LMP8640HVMKE-T/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AB6A
LMP8640HVMKX-F/G4	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A
LMP8640HVMKX-F/G4.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A
LMP8640HVMKX-F/G4.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A
LMP8640HVMKX-F/NO.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A
LMP8640HVMKX-F/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A
LMP8640HVMKX-H/NO.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF6A
LMP8640HVMKX-H/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF6A
LMP8640HVMKX-T/G4	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A
LMP8640HVMKX-T/G4.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A
LMP8640HVMKX-T/G4.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A
LMP8640HVMKX-T/NO.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP8640HVMKX-T/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A
LMP8640MK-F/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AC6A
LMP8640MK-H/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AE6A
LMP8640MK-T/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AA6A
LMP8640MKE-F/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AC6A
LMP8640MKE-H/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AE6A
LMP8640MKE-T/NOPB	Obsolete	Production	SOT-23-THIN (DDC) | 6	-	-	Call TI	Call TI	-40 to 125	AA6A
LMP8640MKX-F/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC6A
LMP8640MKX-F/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC6A
LMP8640MKX-F/NOPB.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC6A
LMP8640MKX-H/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE6A
LMP8640MKX-H/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE6A
LMP8640MKX-H/NOPB.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE6A
LMP8640MKX-T/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA6A
LMP8640MKX-T/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA6A
LMP8640MKX-T/NOPB.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA6A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LMP8640 :

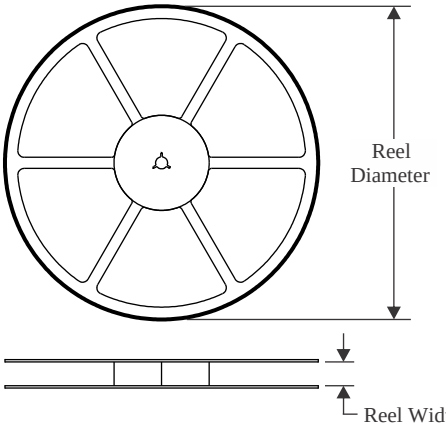
- Automotive : LMP8640-Q1

NOTE: Qualified Version Definitions:

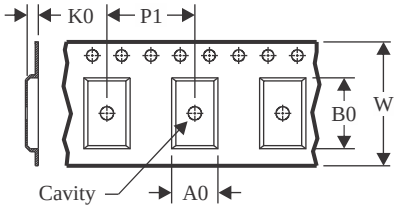
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

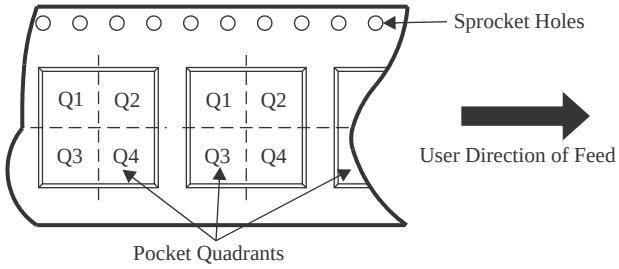


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

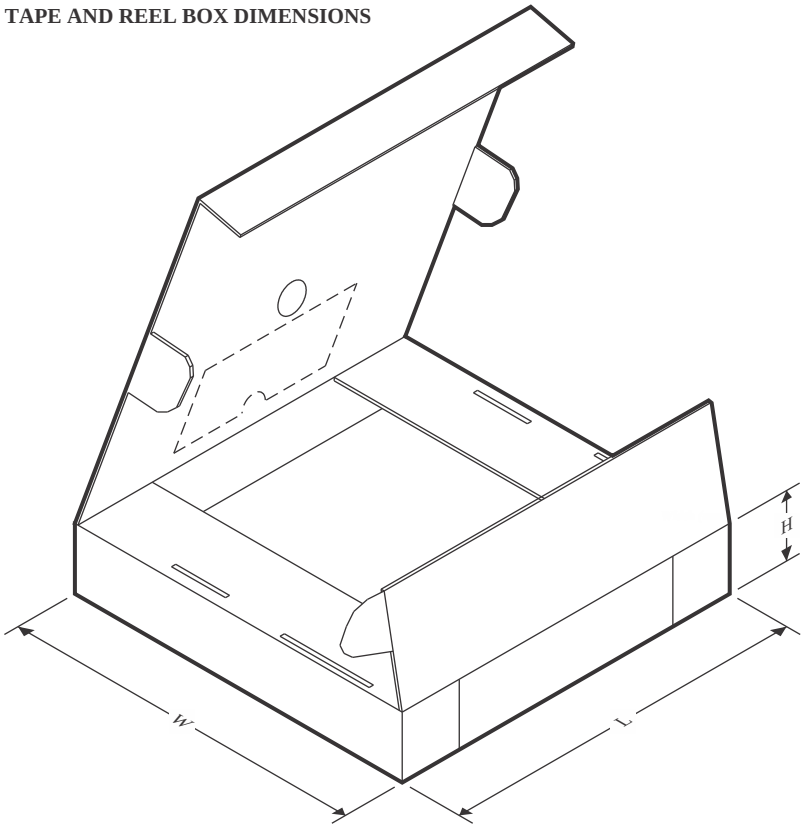


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8640HVMKX-F/G4	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKX-F/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKX-H/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKX-T/G4	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKX-T/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKX-F/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKX-F/NOPB	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
LMP8640MKX-H/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKX-H/NOPB	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8640MKX-T/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKX-T/NOPB	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

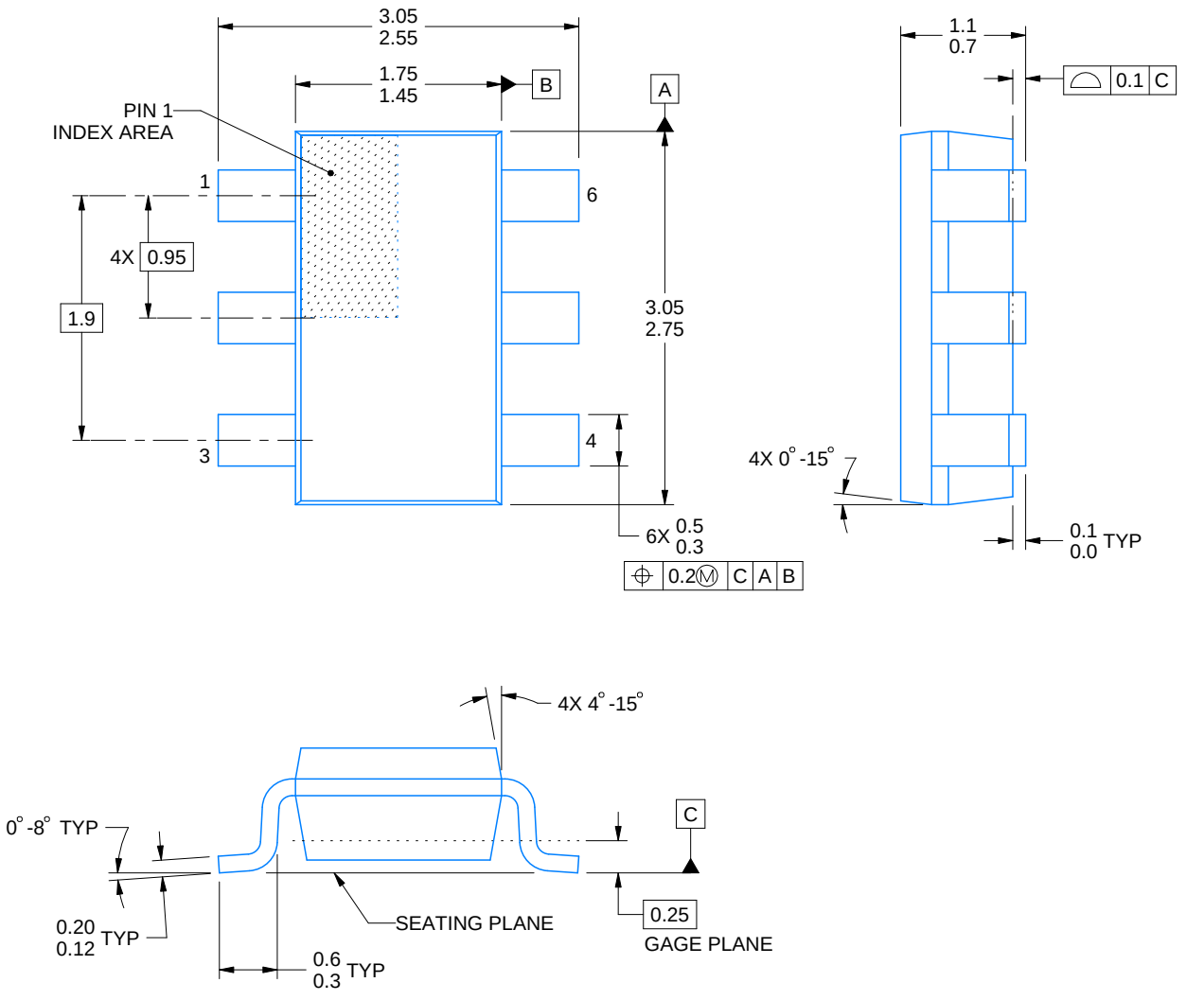
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8640HVMKX-F/G4	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640HVMKX-F/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640HVMKX-H/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640HVMKX-T/G4	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640HVMKX-T/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640MKX-F/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640MKX-F/NOPB	SOT-23-THIN	DDC	6	3000	183.0	183.0	20.0
LMP8640MKX-H/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640MKX-H/NOPB	SOT-23-THIN	DDC	6	3000	183.0	183.0	20.0
LMP8640MKX-T/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP8640MKX-T/NOPB	SOT-23-THIN	DDC	6	3000	183.0	183.0	20.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

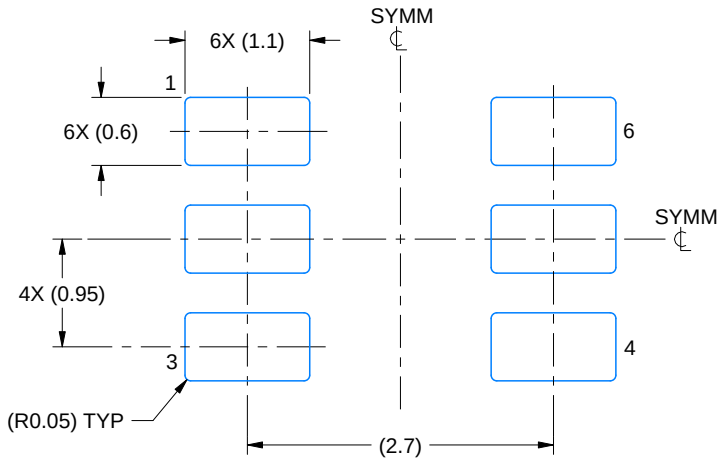
SMALL OUTLINE TRANSISTOR



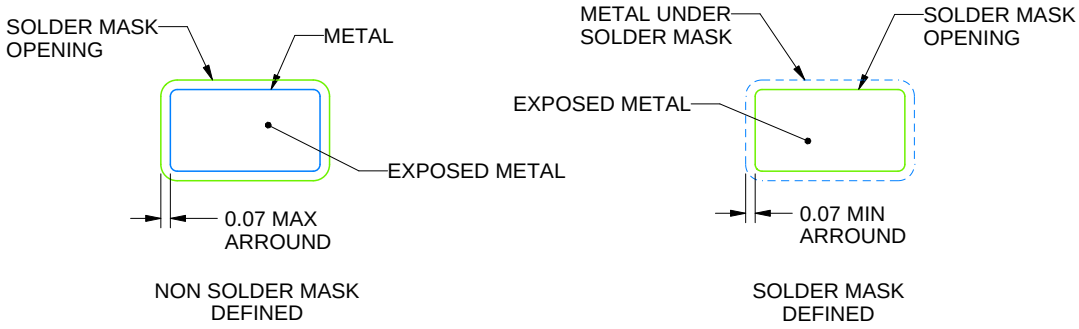
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

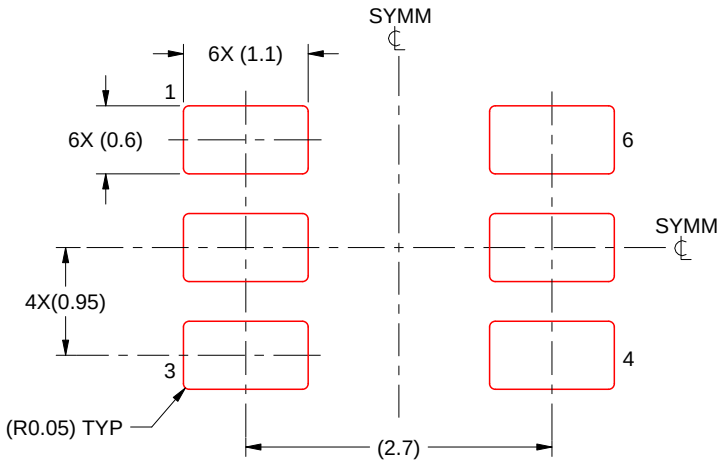


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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