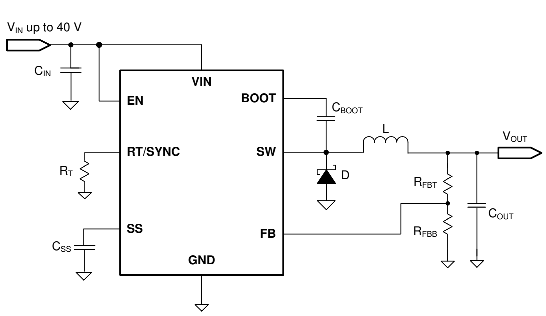
LMR14030-Q1 SIMPLE SWITCHER® Power Converter, 40V, 3.5A, Automotive, Step-Down Converter With 40µA I_Q

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level H1C
  - Device CDM ESD classification level C4A
- 4V to 40V input range
- 3.5A continuous output current
- Ultra-low 40µA operating quiescent current
- 90mΩ high-side MOSFET
- 75ns minimum switch-on time
- Current mode control
- Adjustable switching frequency from 200kHz to 2.5MHz
- Frequency synchronization to external clock
- Spread spectrum option for reduced EMI
- Internal compensation for ease of use
- High duty cycle operation supported
- Precision enable input
- 1µA shutdown current
- External soft start
- Thermal, overvoltage, and short protection
- 8-pin HSOIC with PowerPAD™ package

2 Applications

- Automotive battery regulation
- Industrial power supplies
- Telecom and datacom systems
- General purpose wide Vin regulation



Simplified Schematic

3 Description

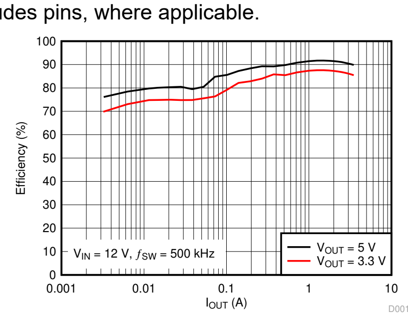
The LMR14030-Q1 is a 40V, 3.5A step down regulator with an integrated high-side MOSFET. With a wide input range from 4V to 40V, the device is designed for various applications from industrial to automotive for power conditioning from unregulated sources. An extended family is available in 2A and 5A options in pin-to-pin compatible packages, including LMR14020-Q1 and LMR14050-Q1. The regulator quiescent current is 40µA in sleep mode, which is designed for battery powered systems. An ultra-low 1µA current in shutdown mode can further prolong battery life. A wide adjustable switching frequency range allows either efficiency or external component size to be optimized. Internal loop compensation means that the user is free from the tedious task of loop compensation design. This feature also minimizes the external components of the device. A precision enable input allows simplification of regulator control and system power sequencing. The device also has built-in protection features such as cycle-by-cycle current limit, thermal sensing and shutdown due to excessive power dissipation, and output overvoltage protection.

The LMR14030-Q1 is available in an 8-pin HSOIC or 10-pin WSON package with exposed pad for low thermal resistance.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMR14030SQDDARQ1	DDA (HSOIC, 8)	4.9mm × 6mm
LMR14030SSQDDARQ1 (Spread Spectrum)		
LMR14030QDPRRQ1	DPR (WSON, 10)	4mm × 4mm
LMR14030SQDPRRQ1 (Spread Spectrum)		

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency vs Output Current

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4 Pin Configuration and Functions

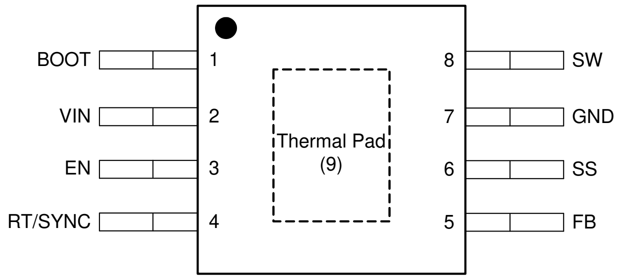


Figure 4-1. DDA Package 8-Pin (HSOIC) Top View

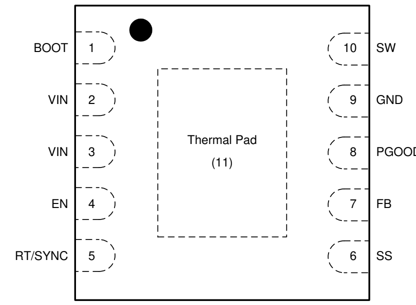


Figure 4-2. DPR Package 10-Pin (WSON) Top View

Table 4-1. Pin Functions

NAME	NO.		TYPE (1)	DESCRIPTION
	SO-8	WSON-10		
BOOT	1	1	P	Bootstrap capacitor connection for high-side MOSFET driver. Connect a high quality 0.1 µF capacitor from BOOT to SW.
VIN	2	2, 3	P	Connect to power supply and bypass capacitors C_{IN}. Path from VIN pin to high frequency bypass C_{IN} and GND must be as short as possible.
EN	3	4	A	Enable pin, with internal pull-up current source. Pull below 1.2V to disable. Float or connect to VIN to enable. Adjust the input under voltage lockout with two resistors. See the Enable and Adjusting Under voltage lockout section.
RT/SYNC	4	5	A	Resistor Timing or External Clock input. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to frequency programming by resistor.
FB	5	7	A	Feedback input pin, connect to the feedback divider to set V_{OUT}. Do not short this pin to ground during operation.
SS	6	6	A	Soft-start control pin. Connect to a capacitor to set soft-start time.
PGOOD	N/A	8	A	Open drain output for power-good flag. Use a 10kΩ to 100kΩ pull-up resistor to logic rail or other DC voltage no higher than 7V.
GND	7	9	G	System ground pin.
SW	8	10	P	Switching output of the regulator. Internally connected to high-side power MOSFET. Connect to power inductor.
Thermal Pad	9	11	G	Major heat dissipation path of the die. Must be connected to ground plane on PCB.

(1) A = Analog, P = Power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C to 125°C (unless otherwise noted) (1)

PARAMETER		MIN	MAX	UNIT
Input Voltages	VIN, EN to GND	–0.3	44	V
	BOOT to GND	–0.3	49	
	SS to GND	–0.3	5	
	FB to GND (DPR package)	–0.3	7	
	FB to GND (DDA package)	–0.3	5.5	
	RT/SYNC to GND	–0.3	3.6	
	PGOOD to GND	–0.3	7	
Output Voltages	BOOT to SW (DPR package)		6.5	V
	BOOT to SW (DDA package)		5.5	
	SW to GND	–3	44	
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 125°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Buck Regulator	VIN	4	40	V
	VOUT	0.8	28	
	BOOT		45	
	SW	–1	40	
	FB	0	5	
Control	EN	0	40	V
	RT/SYNC	0	3.3	
	SS	0	3	
	PGOOD to GND	0	5	
Frequency	Switching frequency range at RT mode	200	2500	kHz
	Switching frequency range at SYNC mode	250	2300	
Temperature	Operating junction temperature, T_J	–40	125	°C

(1) Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For specified specifications, see *Section 5.5*.

5.4 Thermal Information

THERMAL METRIC (1) (2)		LMR14030-Q1 DDA (HSOIC) 8 PINS	LMR14030-Q1 DPR (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.2	36.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	13.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	35.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	3.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	13.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Power rating at a specific ambient temperature T_A must be determined with a maximum junction temperature (T_J) of 125°C, which is illustrated in *Recommended Operating Conditions* section.

5.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = 4.0V to 40V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		4		40	V
UVLO	Undervoltage lockout thresholds	Rising threshold	3.5	3.7	3.9	V
		Hysteresis		285		mV
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, T_J = 25°C, 4.0 V ≤ V_{IN} ≤ 40 V		1.0	3.0	µA
I_Q	Operating quiescent current (non-switching)	V_{FB} = 1.0 V, T_J = 25°C		40		µA
ENABLE (EN PIN)						
V_{EN_TH}	EN threshold voltage		1.05	1.20	1.38	V
I_{EN_PIN}	EN PIN current	Enable threshold +50 mV		-4.6		µA
		Enable threshold –50 mV		-1.0		µA
I_{EN_HYS}	EN hysteresis current			-3.6		µA
EXTERNAL SOFT-START						
I_{SS}	SS pin current	T_J = 25°C		-3		µA
POWER GOOD (PGOOD PIN)						
V_{PG_UV}	Power-good flag under voltage tripping threshold	POWER GOOD (% of FB voltage)		94%		
		POWER BAD (% of FB voltage)		92%		
V_{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		109%		
		POWER GOOD (% of FB voltage)		107%		
V_{PG_HYS}	Power-good flag recovery hysteresis	% of FB voltage		2%		
I_{PG}	PGOOD leakage current at high level output	$V_{Pull\text{-}Up}$ = 5 V		10	200	nA
V_{PG_LOW}	PGOOD low level output voltage	$I_{Pull\text{-}Up}$ = 1 mA		0.1		V
$V_{IN\_PG\_MIN}$	Minimum VIN for valid PGOOD output	$V_{Pull\text{-}Up}$ < 5 V at $I_{Pull\text{-}Up}$ = 100 µA		1.6	1.95	V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	T_J = 25°C	0.744	0.750	0.756	V
		T_J = –40°C to 125 °C	0.735	0.750	0.765	V
HIGH-SIDE MOSFET						

5.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = 4.0V to 40V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DS_ON}	On-resistance	V_{IN} = 12 V		90	180	mΩ
HIGH-SIDE MOSFET CURRENT LIMIT						
I_{LIMT}	Current limit	V_{IN} = 12 V, T_J = –40°C to 125°C, Open Loop	4.1	5.5	7.7	A
THERMAL PERFORMANCE						
T_{SHDN}	Thermal shutdown threshold			170		°C
T_{HYS}	Hysteresis			12		°C

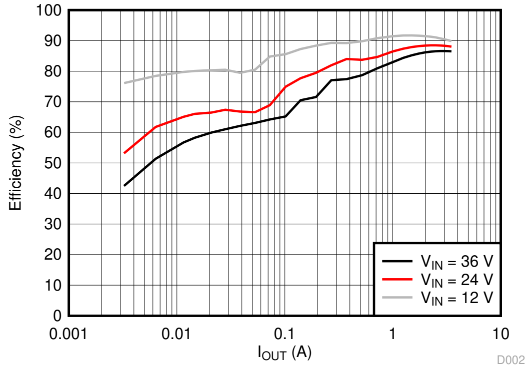
5.6 Switching Characteristics

Over the recommended operating junction temperature range of -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	R_T = 11.5kΩ	1758	1912	2066	kHz
	Switching frequency range at SYNC mode		250		2300	kHz
F_{DITHER}	Switching frequency dithering	Spread spectrum option, frequency dithering over center frequency		±6%		
V_{SYNC_HI}	SYNC clock high level threshold		1.7			V
V_{SYNC_LO}	SYNC clock low level threshold				0.5	V
T_{SYNC_MIN}	Minimum SYNC input pulse width	Measured at 500kHz, V_{SYNC_HI} > 3V, V_{SYNC_LO} < 0.3V		30		ns
T_{LOCK_IN}	PLL lock in time	Measured at 500kHz		100		µs
T_{ON_MIN}	Minimum controllable on time	V_{IN} = 12V, I_{Load} = 1A		75		ns
D_{MAX}	Maximum duty cycle	f_{SW} = 200kHz		97%		

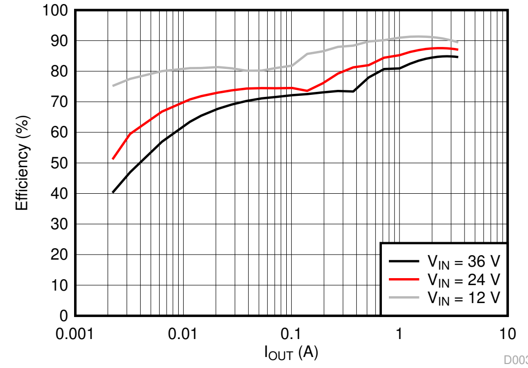
5.7 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12V, f_{SW} = 500kHz, L = 5.6µH, C_{OUT} = 47µF x 2, T_A = 25°C.



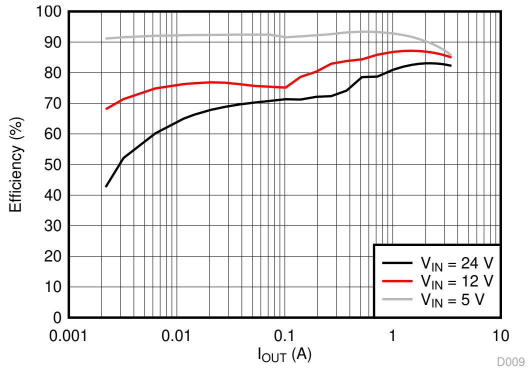
V_{OUT} = 5V f_{SW} = 500kHz

Figure 5-1. Efficiency vs. Load Current



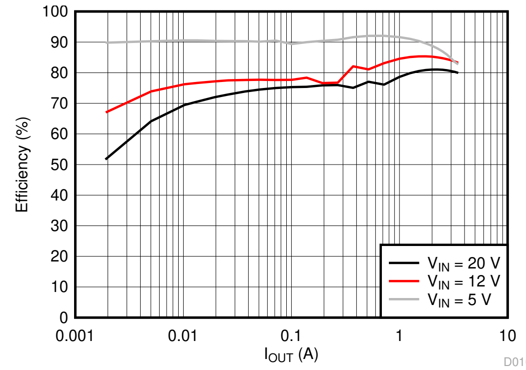
V_{OUT} = 5V f_{SW} = 1MHz

Figure 5-2. Efficiency vs. Load Current



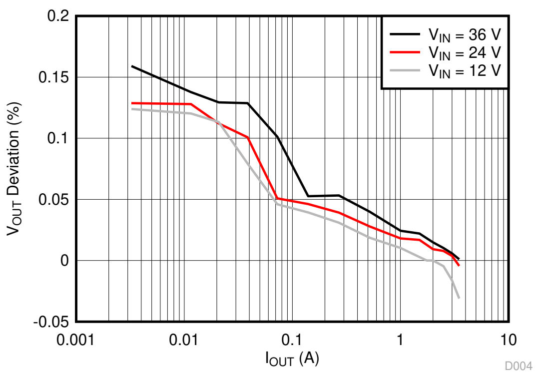
V_{OUT} = 3.3V f_{SW} = 1MHz

Figure 5-3. Efficiency vs. Load Current



V_{OUT} = 3.3V f_{SW} = 2.2MHz

Figure 5-4. Efficiency vs. Load Current



V_{OUT} = 5V f_{SW} = 500kHz

Figure 5-5. Load Regulation

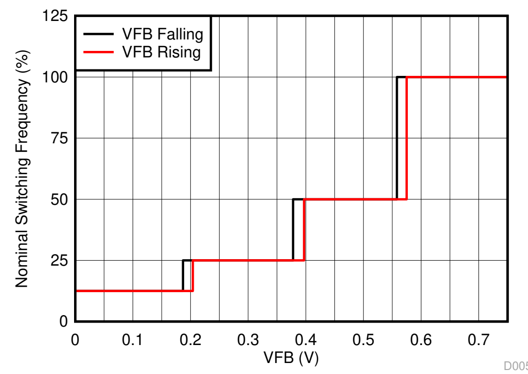
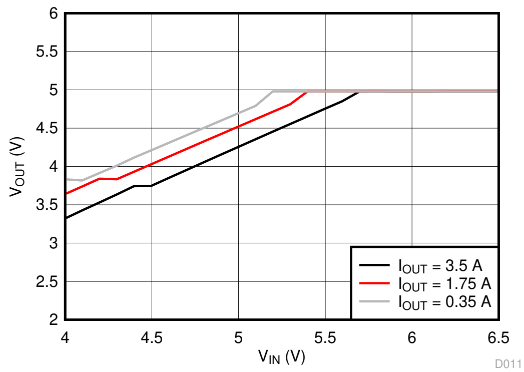


Figure 5-6. Frequency vs V_{FB}

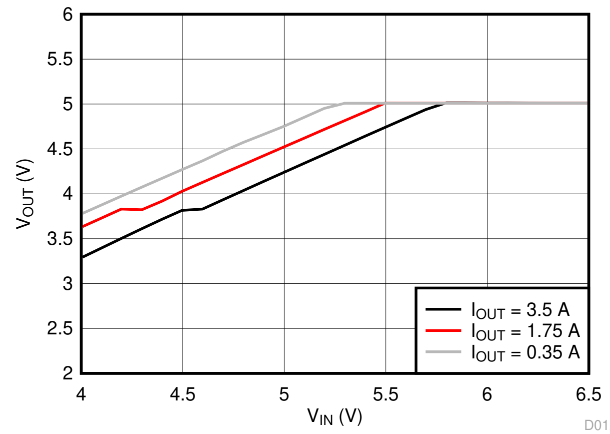
5.7 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12V, f_{SW} = 500kHz, L = 5.6µH, C_{OUT} = 47µF x 2, T_A = 25°C.



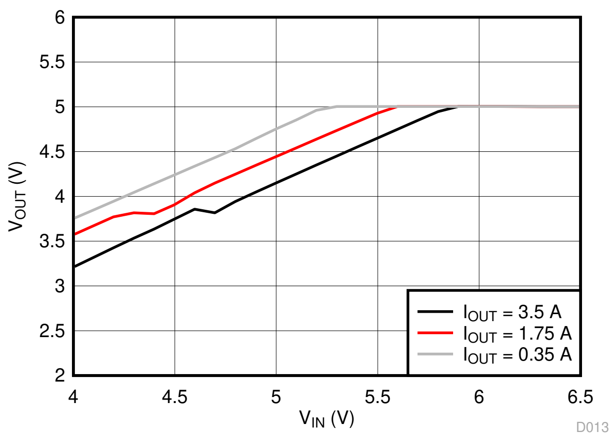
V_{OUT} = 5V f_{SW} = 500kHz

Figure 5-7. Dropout Curve



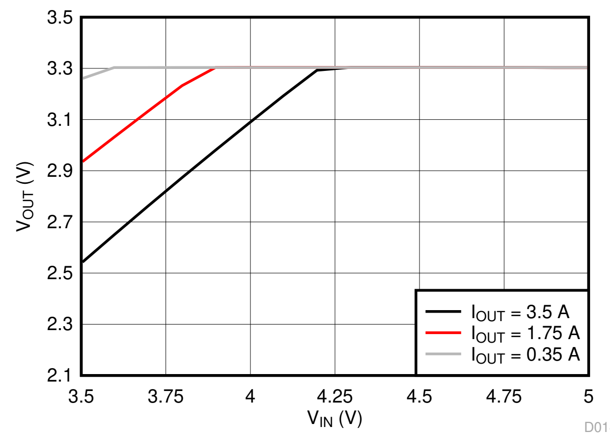
V_{OUT} = 5V f_{SW} = 1MHz

Figure 5-8. Dropout Curve



V_{OUT} = 5V f_{SW} = 2.2MHz

Figure 5-9. Dropout Curve



V_{OUT} = 3.3V f_{SW} = 2.2MHz

Figure 5-10. Dropout Curve

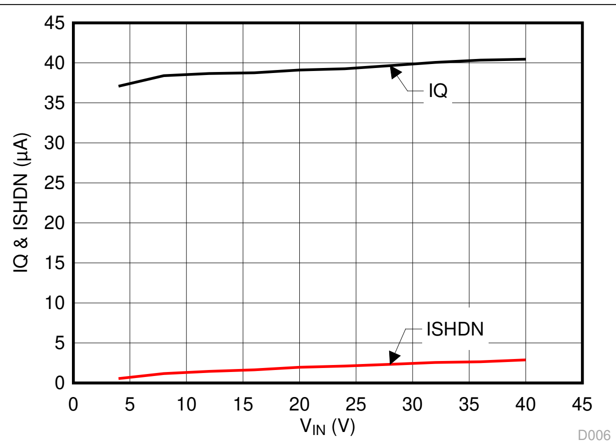
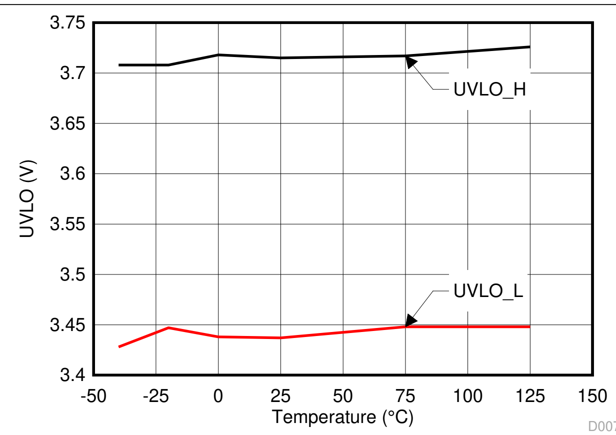


Figure 5-11. Shut-down Current and Quiescent Current



I_{OUT} = 0A

Figure 5-12. UVLO Threshold

6 Detailed Description

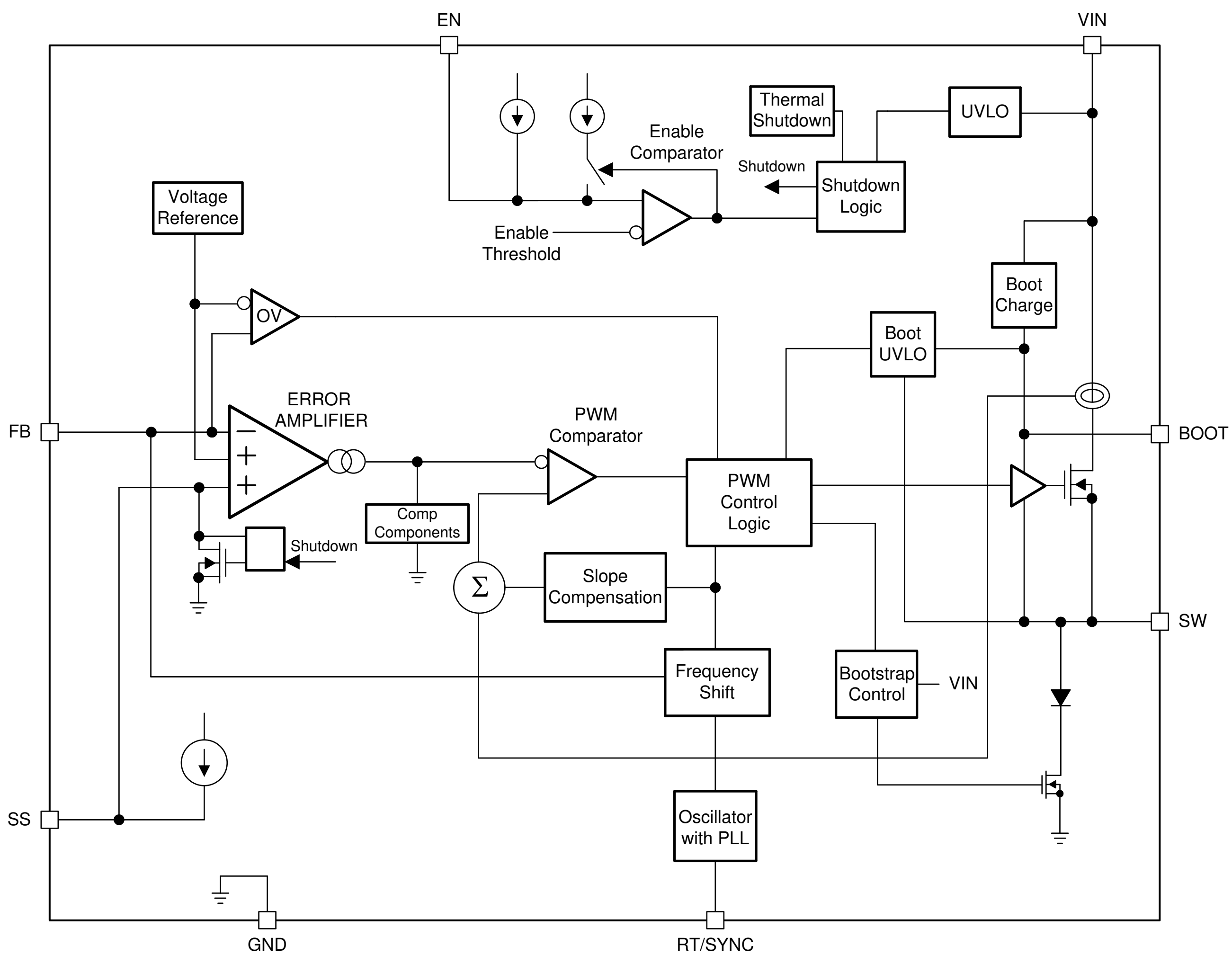
6.1 Overview

The LMR14030-Q1 SIMPLE SWITCHER® power converter regulator is an easy to use step-down DC-DC converter that operates from a 4.0 V to 40 V supply voltage. It integrates a 90 mΩ (typical) high-side MOSFET, and is capable of delivering up to 3.5 A DC load current with exceptional efficiency and thermal performance in a very small solution size. The operating current is typically 40 µA under no load condition (not switching). When the device is disabled, the supply current is typically 1 µA. An extended family is available in 2 A and 5 A load options in pin to pin compatible packages.

The LMR14030-Q1 implements constant frequency peak current mode control with Sleep-mode at light load to achieve high efficiency. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is programmable from 200 kHz to 2.5 MHz by an external resistor R_T. The LMR14030-Q1 is also capable of synchronization to an external clock within the 250 kHz to 2.3 MHz frequency range, which allows the device to be optimized to fit small board space at higher frequency, or high efficient power conversion at lower frequency.

Other features are included for more comprehensive system requirements, including precision enable, adjustable soft-start time, and approximate 97% duty cycle by BOOT capacitor recharge circuit. These features provide a flexible and easy to use platform for a wide range of applications. Protection features include over temperature shutdown, V_{OUT} over voltage protection (OVP), V_{IN} under-voltage lockout (UVLO), cycle-by-cycle current limit, and short-circuit protection with frequency fold-back.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LMR14030-Q1 refer to the *Section 6.2* and to the waveforms in Figure 6-1. LMR14030-Q1 output voltage is regulated by turning on the high-side N-MOSFET with controlled ON time. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increase with linear slope $(V_{IN} – V_{OUT}) / L$. When high-side switch is off, inductor current discharges through freewheel diode with a slope of $–V_{OUT} / L$. The control parameter of Buck converter is defined as Duty Cycle $D = t_{ON} / T_{SW}$, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal Buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

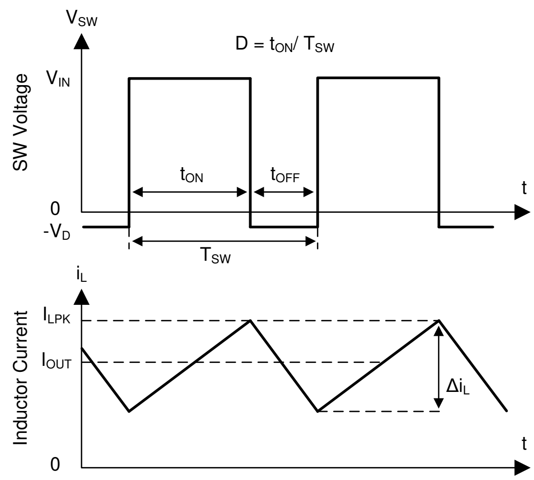


Figure 6-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR14030-Q1 employs fixed frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At very light load, the LMR14030-Q1 will operate in Sleep-mode to maintain high efficiency and the switching frequency will decrease with reduced load current.

6.3.2 Slope Compensation

The LMR14030-Q1 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

6.3.3 Sleep-mode

The LMR14030-Q1 operates in Sleep-mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the current threshold of 300 mA, the device enters Sleep-mode. The Sleep-mode current threshold is the peak switch current level corresponding to a nominal internal COMP voltage of 400 mV.

When in Sleep-mode, the internal COMP voltage is clamped at 400mV and the high-side MOSFET is inhibited, and the device draws only 40 μA (typical) input quiescent current. Because the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the internal COMP voltage. The high-side MOSFET is enabled and switching resumes when the error amplifier lifts internal COMP voltage above 400 mV. The output voltage recovers to the regulated value, and internal COMP voltage eventually falls below the Sleep-mode threshold at which time the device again enters Sleep-mode.

6.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The LMR14030-Q1 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or greater for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the LMR14030-Q1 operates at approximate 97% duty cycle. When the high-side MOSFET is continuously on for 5 or 6 switching cycles (5 or 6 switching cycles for frequency lower than 1 MHz, and 10 or 11 switching cycles for frequency higher than 1 MHz) and the voltage from BOOT to SW drops below 3.2 V, the high-side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor.

Because the gate drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 97%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

6.3.5 Adjustable Output Voltage

The internal voltage reference produces a precise 0.75 V (typical) voltage reference over the operating temperature range. The output voltage is set by a resistor divider from output voltage to the FB pin. It is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or less divider resistors. Select the low side resistor R_{FBB} for the desired divider current and use Equation 1 to calculate high-side R_{FBT}. Larger value divider resistors are good for efficiency at light load. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current can become noticeable. R_{FBB} in the range from 10 kΩ to 100 kΩ is recommended for most applications.

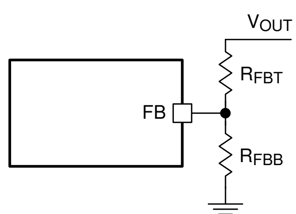


Figure 6-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} \times R_{FBB} \tag{1}$$

6.3.6 Enable and Adjustable Undervoltage Lockout

The LMR14030-Q1 is enabled when the VIN pin voltage rises above 3.7 V (typical) and the EN pin voltage exceeds the enable threshold of 1.2 V (typical) for at least 25μs. The LMR14030-Q1 is disabled when the VIN pin voltage falls below 3.42 V (typical) or when the EN pin voltage is below 1.2 V for at least 25μs. The EN pin has an internal pull-up current source (typically I_{EN} = 1 μA) that enables operation of the LMR14030-Q1 when the EN pin is floating.

Many applications benefit from the employment of an enable divider R_{ENT} and R_{ENB} in Figure 6-3 to establish a precision system UVLO level for the stage. System UVLO can be used for supplies operating from utility power as well as battery power. System UVLO can be used for sequencing, making sure of reliable operation, or supply protection, such as a battery. An external logic signal can also be used to drive EN input for system sequencing and protection.

When EN terminal voltage exceeds 1.2 V, an additional hysteresis current (typically I_{HYS} = 3.6 µA) is sourced out of EN terminal. When the EN terminal is pulled below 1.2 V, I_{HYS} current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use Equation 2 and Equation 3 to calculate R_{ENT} and R_{ENB} for desired UVLO hysteresis voltage.

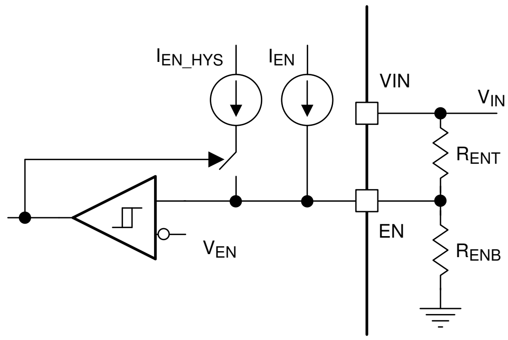


Figure 6-3. System UVLO By Enable Dividers

$$R_{ENT} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{2}$$

$$R_{ENB} = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{R_{ENT}} + I_{EN}} \tag{3}$$

where V_{START} is the desired voltage threshold to enable LMR14030-Q1, V_{STOP} is the desired voltage threshold to disable device.

6.3.7 External Soft-start

The LMR14030-Q1 has soft-start pin for programmable output ramp up time. The soft-start feature is used to prevent inrush current impacting the LMR14030-Q1 and the load when power is first applied. The soft-start time can be programed by connecting an external capacitor C_{SS} from SS pin to GND. An internal current source (typically I_{SS} = 3 µA) charges C_{SS} and generates a ramp from 0 V to V_{REF}. The soft-start time can be calculated by Equation 4:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \tag{4}$$

For LMR14030-Q1 in WSON package, the maximum value of C_{SS} is 4.7 nF.

The soft-start resets while device is disabled or in thermal shutdown.

6.3.8 Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the LMR14030-Q1 can be programmed by the resistor R_T from the RT/SYNC pin and GND pin. The RT/SYNC pin can't be left floating or shorted to ground. To determine the timing resistance for a given switching frequency, use Equation 5 or the curve in Figure 6-4. Table 6-1 gives typical R_T values for a given f_{SW}.

$$R_T(k\Omega) = 42904 \times f_{SW}(kHz)^{-1.088} \tag{5}$$

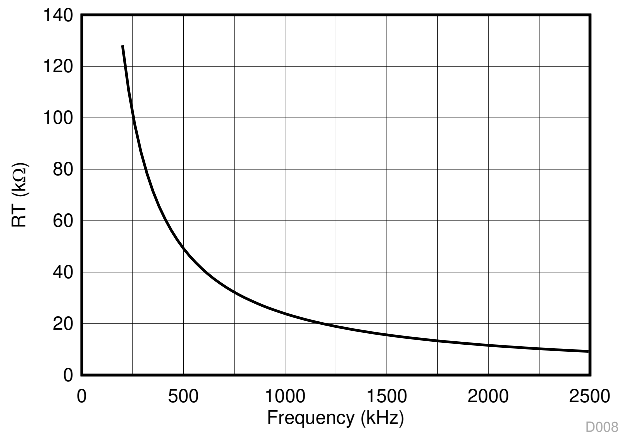


Figure 6-4. R_T vs Frequency Curve

Table 6-1. Typical Frequency Setting R_T Resistance

f_{SW} (kHz)	R_T (kΩ)
200	133
350	73.2
500	49.9
750	32.4
1000	23.2
1500	15.0
1912	11.5
2200	9.76

The LMR14030-Q1 switching action can also be synchronized to an external clock from 250 kHz to 2.3 MHz. Connect a square wave to the RT/SYNC pin through either circuit network shown in Figure 6-5. Internal oscillator is synchronized by the falling edge of external clock. The recommendations for the external clock include: high level no lower than 1.7 V, low level no higher than 0.5 V and have a pulse width greater than 30 ns. When using a low impedance signal source, the frequency setting resistor R_T is connected in parallel with an AC coupling capacitor C_{COUP} to a termination resistor R_{TERM} (that is, 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10 pF ceramic capacitor can be used for C_{COUP}. Figure 6-6, Figure 6-7 and Figure 6-8 show the device synchronized to an external system clock.

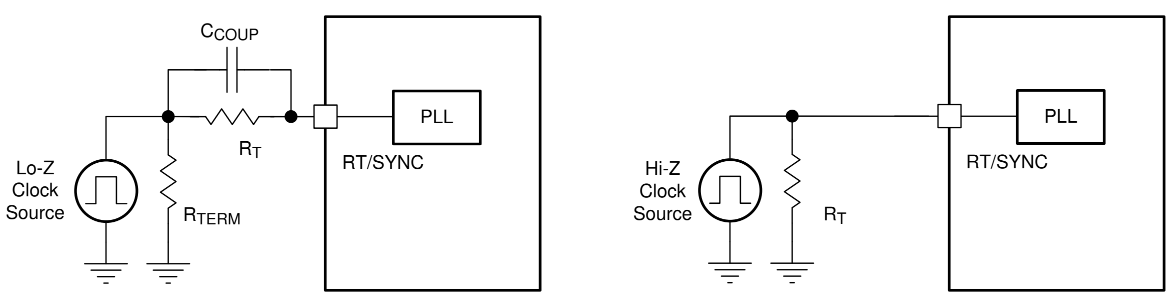


Figure 6-5. Synchronizing to an External Clock

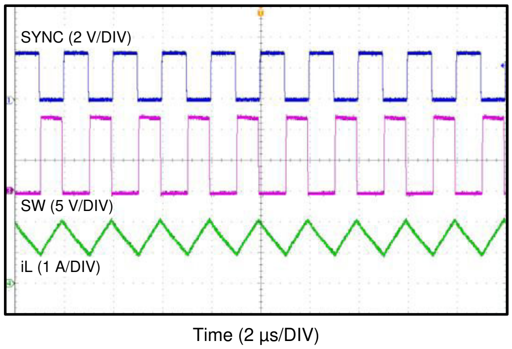


Figure 6-6. Synchronizing in CCM

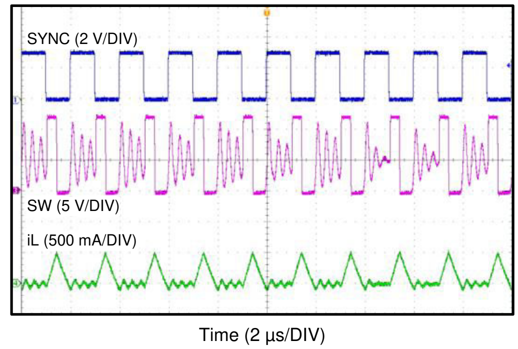


Figure 6-7. Synchronizing in DCM

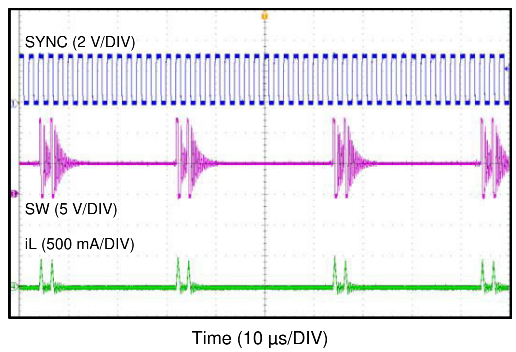


Figure 6-8. Synchronizing in Sleep-mode Mode

For spread spectrum option, the internal frequency dithering is diabled if the device is synchronized to an external clock.

Equation 6 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value causes the regulator to skip switching pulses to achieve the low duty cycle required at maximum input voltage.

$$f_{SW(max)} = \frac{1}{t_{ON}} \times \left(\frac{I_{OUT} \times R_{IND} + V_{OUT} + V_D}{V_{IN\_MAX} - I_{OUT} \times R_{DS\_ON} + V_D} \right) \tag{6}$$

where

- I_{OUT} = Output current
- R_{IND} = Inductor series resistance
- V_{IN_MAX} = Maximum input voltage
- V_{OUT} = Output voltage
- V_D = Diode voltage drop
- R_{DS_ON} = High-side MOSFET switch on resistance
- t_{ON} = Minimum on time

6.3.9 Power Good (PGOOD)

The LMR14020-Q1 in WSON-10 package has a built in power-good flag shown on PGOOD pin to indicate whether the output voltage is within the regulation level. The PGOOD signal can be used for start-up sequencing of multiple rails or fault protection. The PGOOD pin is an open-drain output that requires a pullup resistor to an appropriate DC voltage. Voltage seen by the PGOOD pin must never exceed 7 V. A resistor divider pair can be used to divide the voltage down from a higher potential. A typical range of pullup resistor value is 10 kΩ to 100 kΩ.

Refer to Figure 6-9. When the FB voltage is within the power-good band, +7% above and -6% below the internal reference V_{REF} typically, the PGOOD switch is turned off and the PGOOD voltage is pulled up to the voltage level defined by the pullup resistor or divider. When the FB voltage is outside of the tolerance band, +9% above or -8% below V_{REF} typically, the PGOOD switch is turned on and the PGOOD pin voltage is pulled low to indicate power bad.

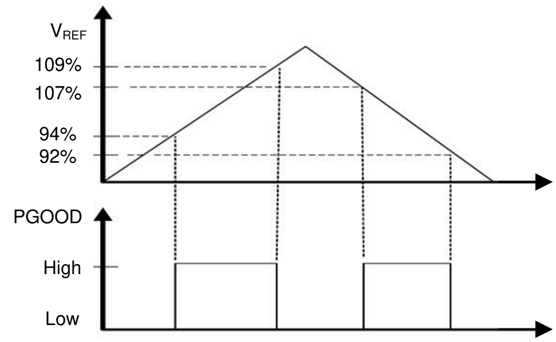


Figure 6-9. Power-Good Flag

6.3.10 Over Current and Short Circuit Protection

The LMR14030-Q1 is protected from over current condition by cycle-by-cycle current limiting on the peak current of the high-side MOSFET. High-side MOSFET over-current protection is implemented by the nature of the Peak Current Mode control. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. Please refer to Functional Block Diagram for more details. The peak current of high-side switch is limited by a clamped maximum peak current threshold which is constant. So the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The LMR14030-Q1 also implements a frequency fold-back to protect the converter in severe over-current or short conditions. The oscillator frequency is divided by 2, 4, and 8 as the FB pin voltage decrease to 75%, 50%, 25% of V_{REF}. The frequency fold-back increases the off time by increasing the period of the switching cycle, so that it provides more time for the inductor current to ramp down and leads to a lower average inductor current. Lower frequency also means lower switching loss. Frequency fold-back reduces power dissipation and prevents overheating and potential damage to the device.

6.3.11 Overvoltage Protection

The LMR14030-Q1 employs an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. The OVP feature minimizes output overshoot by turning off high-side switch immediately when FB voltage reaches to the rising OVP threshold which is nominally 109% of the internal voltage reference V_{REF}. When the FB voltage drops below the falling OVP threshold which is nominally 107% of V_{REF}, the high-side MOSFET resumes normal operation.

6.3.12 Thermal Shutdown

The LMR14030-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170 °C (typical). The high-side MOSFET stops switching when thermal shundown activates. After the die temperature falls below 158 °C (typical), the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

6.4 Device Functional Modes

6.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMR14030-Q1. When V_{EN} is below 1.0V, the device is in shutdown mode. The switching regulator is turned off and the quiescent current drops to 1.0µA typically. The LMR14030-Q1 also employs undervoltage lockout protection. If V_{IN} voltage is below the UVLO level, the regulator is turned off.

6.4.2 Active Mode

The LMR14030-Q1 is in active mode when V_{EN} is above the precision enable threshold and V_{IN} is above the UVLO level. The simplest way to enable the LMR14030-Q1 is to connect the EN pin to VIN pin. This action allows self startup when the input voltage is in the operation range: 4.0V to 40V. Please refer to *Section 6.3.6* for details on setting these operating levels.

In active mode, depending on the load current, the LMR14030 is in one of three modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple.
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation.
3. Sleep-mode when internal COMP voltage drop to 400mV at very light load.

6.4.3 CCM Mode

CCM operation is employed in the LMR14030-Q1 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 3.5A can be supplied by the LMR14030-Q1.

6.4.4 Light Load Operation

When the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR14030-Q1 operates in DCM. At even lighter current loads, Sleep-mode is activated to maintain high efficiency operation by reducing switching and gate drive losses.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LMR14030-Q1 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3.5 A. The following design procedure can be used to select components for the LMR14030-Q1. This section presents a simplified discussion of the design process.

7.2 Typical Application

The LMR14030-Q1 only requires a few external components to convert from wide voltage range supply to a fixed output voltage. A schematic of 5 V / 3.5 A application circuit based on LMR14030-Q1 in SO-8 package is shown in Figure 7-1. The external components have to fulfill the needs of the application, but also the stability criteria of the device's control loop.

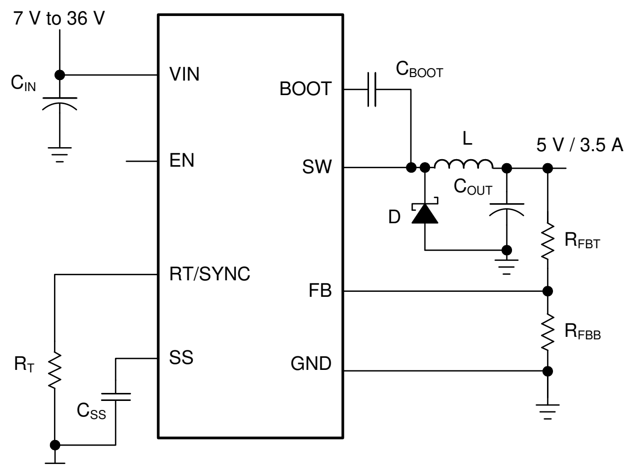


Figure 7-1. Application Circuit, 5V Output

7.2.1 Design Requirements

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level:

Table 7-1. Design Parameters

Input Voltage, V_{IN}	7 V to 36 V, Typical 12 V
Output Voltage, V_{OUT}	5.0 V
Maximum Output Current I_{O_MAX}	3.5 A
Transient Response 0.35 A to 3.5 A	5%
Output Voltage Ripple	50 mV
Input Voltage Ripple	400 mV
Switching Frequency f_{SW}	500 kHz
Soft-start time	5 ms

7.2.2 Detailed Design Procedure

7.2.2.1 Output Voltage Set-Point

The output voltage of LMR14030-Q1 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 7 is used to determine the output voltage:

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} \times R_{FBB} \tag{7}$$

Choose the value of R_{FBT} to be 100 kΩ. With the desired output voltage set to 5 V and the V_{FB} = 0.75 V, the R_{FBB} value can then be calculated using Equation 7. The formula yields to a value 17.65 kΩ. Choose the closest available value of 17.8 kΩ for R_{FBB}.

7.2.2.2 Switching Frequency

For desired frequency, use Equation 8 to calculate the required value for R_T.

$$R_T(\text{k}\Omega) = 42904 \times f_{SW}(\text{kHz})^{-1.088} \tag{8}$$

For 500 kHz, the calculated R_T is 49.66 kΩ and standard value 49.9 kΩ can be used to set the switching frequency at 500 kHz.

7.2.2.3 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 10 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value of K_{IND} must be 20%-40%. During an instantaneous short or over current operation event, the RMS and peak inductor current can be high. The inductor current rating must be higher than current limit.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \tag{9}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{10}$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load can be falsely triggered. It also generates more conduction loss because the RMS current is slightly higher. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 6.15 µH, and a nearest standard value is chosen: 6.5 µH. A standard 6.5 µH ferrite inductor with a capability of 4 A RMS current and 6.5 A saturation current can be used.

7.2.2.4 Output Capacitor Selection

The output capacitor(s), C_{OUT}, must be chosen with care because it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{11}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{12}$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator’s control loop usually needs three or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for three clock cycles to maintain the output voltage within the specified range. Equation 13

Equation 13 shows the minimum output capacitance needed for specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor. The catch diode can’t sink current so the energy stored in the inductor results in an output voltage overshoot. Equation 14 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > \frac{3 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \tag{13}$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L \tag{14}$$

where

- K_{IND} = Ripple ratio of the inductor ripple current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{US} = Target output voltage undershoot
- V_{OS} = Target output voltage overshoot

For this design example, the target output ripple is 50 mV. Presuppose ΔV_{OUT_ESR} = ΔV_{OUT_C} = 50 mV, and chose K_{IND} = 0.4. Equation 11 yields ESR no larger than 35.7 mΩ and Equation 12 yields C_{OUT} no smaller than 7 µF. For the target over/undershoot range of this design, V_{US} = V_{OS} = 5% × V_{OUT} = 250 mV. The C_{OUT} can be calculated to be no smaller than 75.6 µF and 30.8 µF by Equation 13 and Equation 14 respectively. In summary, the most stringent criteria for the output capacitor is 75.6 µF. Two 47 µF, 16 V, X7R ceramic capacitors with 5 mΩ ESR are used in parallel.

7.2.2.5 *Schottky Diode Selection*

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode must be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-D) × I_{OUT} however the peak current rating must be higher than the maximum load current. A 4 A to 5 A rated diode is a good starting point.

7.2.2.6 *Input Capacitor Selection*

The LMR14030-Q1 device requires high frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is 4.7 µF to 10 µF. A high-quality ceramic capacitor type X5R or X7R with sufficiency voltage rating is recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required, especially if the LMR14030-Q1 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 2.2 µF, X7R ceramic capacitors rated for 100 V are used. A 0.1 µF for high-frequency filtering and place it as close as possible to the device pins.

7.2.2.7 *Bootstrap Capacitor Selection*

Every LMR14030-Q1 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 0.1 µF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

7.2.2.8 *Soft-start Capacitor Selection*

Use Equation 15 to calculate the soft-start capacitor value:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \tag{15}$$

where

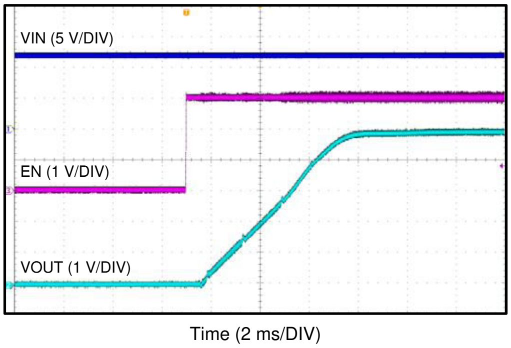
- C_{SS} = Soft-start capacitor value
- I_{SS} = Soft-start charging current (3 µA)
- t_{SS} = Desired soft-start time

For the desired soft-start time of 5 ms and soft-start charging current of 3.0 µA, Equation 15 yields a soft-start capacitor value of 20 nF, a standard 22 nF ceramic capacitor is used.

For design with LMR14030-Q1 in WSON package, the maximum value of C_{SS} is 4.7 nF.

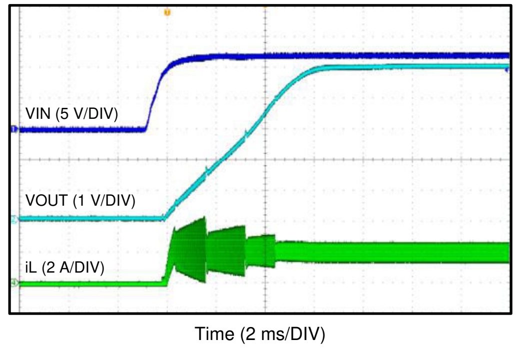
7.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 500 kHz, L = 5.6 µH, C_{OUT} = 47 µF × 2, T_A = 25 °C.



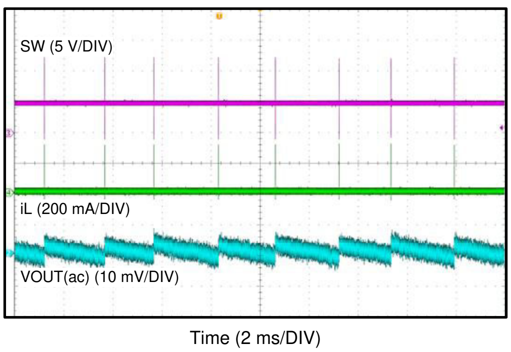
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 2 A

Figure 7-2. Start-up By EN



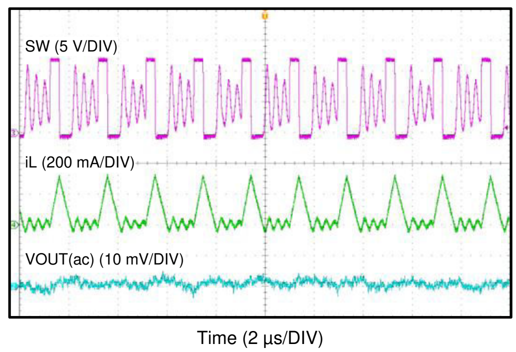
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 2 A

Figure 7-3. Start-up By V_{IN}



V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 0 A

Figure 7-4. Sleep-mode



V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 100 mA

Figure 7-5. DCM Mode

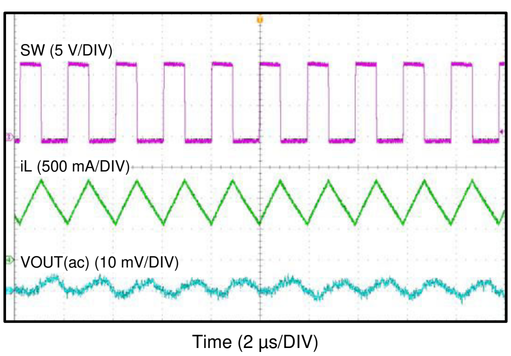
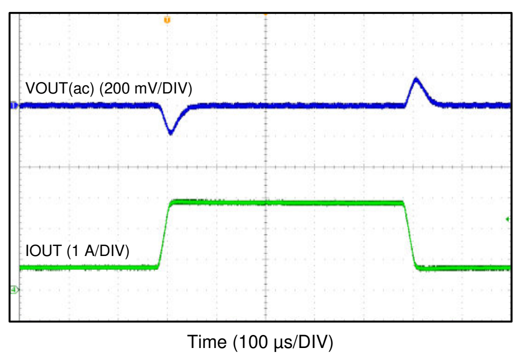
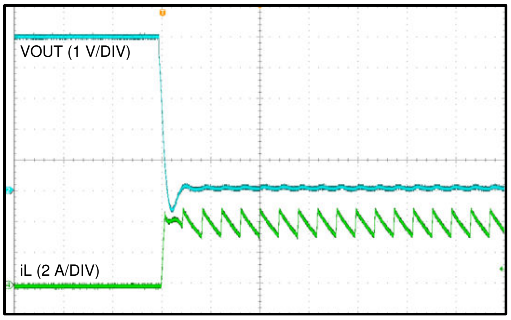


Figure 7-6. CCM Mode



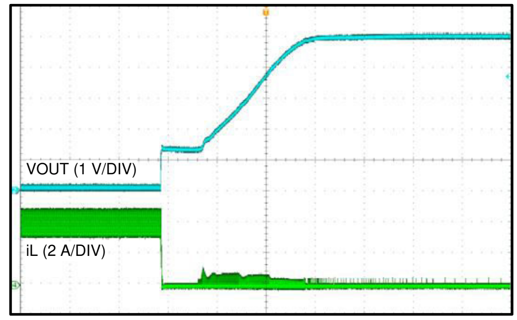
I_{OUT}: 20% → 80% of 3.5 A Slew rate = 100 mA/µs

Figure 7-7. Load Transient



V_{IN} = 12 V V_{OUT} = 5 V

Figure 7-8. Output Short



V_{IN} = 12 V V_{OUT} = 5 V

Figure 7-9. Output Short Recovery

7.3 Power Supply Recommendations

The LMR14030-Q1 is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR14030-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR14030-Q1, additional bulk capacitance can be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47 µF or 100 µF electrolytic capacitor is a typical choice.

7.4 Layout

7.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R_{FBT} and R_{FBB}, must be kept close to the FB pin. V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
2. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the GND pin and PAD.
3. The inductor L must be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} must be placed close to the junction of L and the diode D. The L, D, and C_{OUT} trace must be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for the diode, C_{IN}, and C_{OUT} must be as small as possible and tied to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane
6. For more detail on switching power supply layout considerations see SNVA021 Application Note AN-1149

7.4.2 Layout Example

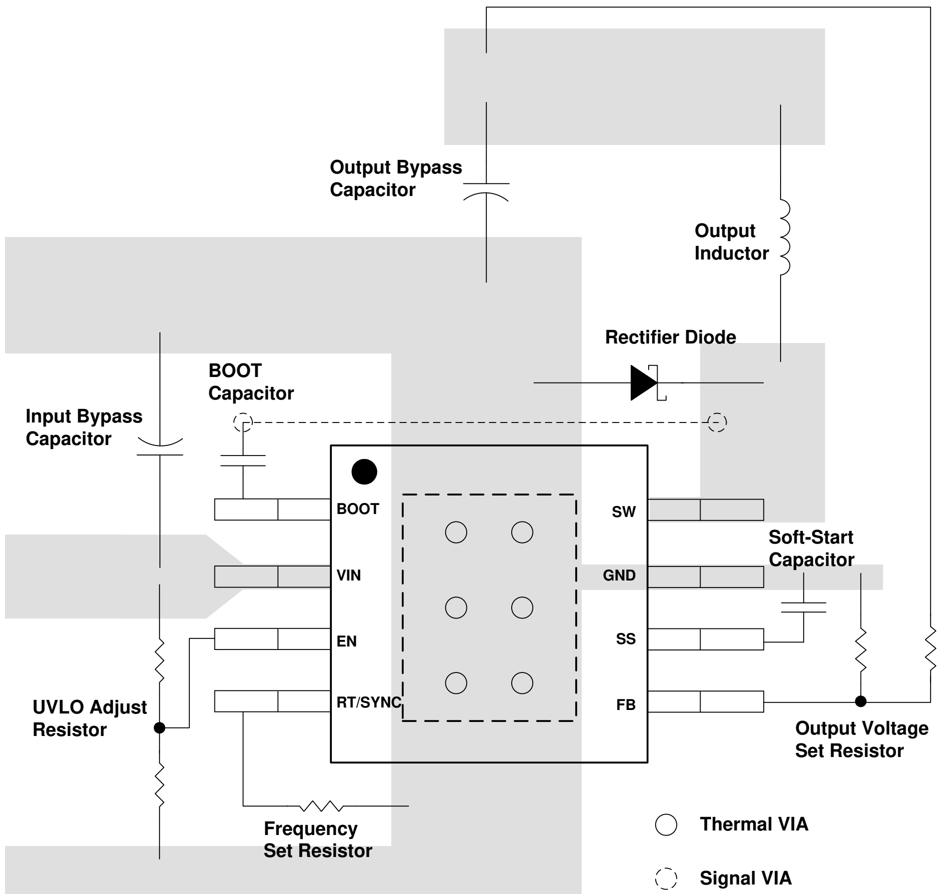


Figure 7-10. Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application note

8.2.2 Related Products

Part Number	V_{IN} (V)	I_{OUT} (A)	Comments
LMR14020-Q1	4.0 - 40	2	Non-synchronous step-down converter, I_Q = 40 µA, sleep mode, spread spectrum, SO-8 or WSON-10 package
LMR14050-Q1	4.0 - 40	5	Non-synchronous step-down converter, I_Q = 40 µA, sleep mode, spread spectrum, SO-8 or WSON-10 package

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
SIMPLE SWITCHER® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision A (June 2016) to Revision B (December 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the document title	1
• Added approved nouns after the SIMPLE SWITCHER trademark throughout the document	1
• Changed the MAX voltage rating of DDA package for BOOT to SW from 6.5V to 5.5V, and FB to GND from 7V to 5.5V	4
• Changed thermal metrics of DDA package: $R_{\theta JA}$ from 42.5 to 43.2, ψ_{JT} from 9.9 to 5.2, ψ_{JB} 25.4 to 16.4, $R_{\theta JC(top)}$ from 56.1 to 52.1, $R_{\theta JC(bot)}$ from 3.8 to 7.8, $R_{\theta JB}$ from 25.5 to 16.4	5
• Deleted the test condition of "BOOT to SW = 5.8 V" on parameter R_{DS_ON}	5
• Deleted the test condition of "BOOT to SW = 5.8 V" on parameter T_{ON_MIN}	6

Changes from Revision * (November 2015) to Revision A (June 2016)	Page
• Added DPR package information	1
• Added new column for WSON package	3
• Added new section for PGOOD	5
• Added PGOOD section	14

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR14030QDPRRQ1	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 14030Q
LMR14030QDPRRQ1.A	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 14030Q
LMR14030QDPRTQ1	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 14030Q
LMR14030QDPRTQ1.A	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 14030Q
LMR14030SQDDAQ1	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14030Q
LMR14030SQDDAQ1.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14030Q
LMR14030SQDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14030Q
LMR14030SQDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14030Q
LMR14030SQDPRRQ1	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 1403SQ
LMR14030SQDPRRQ1.A	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 1403SQ
LMR14030SQDPRTQ1	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 1403SQ
LMR14030SQDPRTQ1.A	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMR 1403SQ
LMR14030SSQDDAQ1	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1403SQ
LMR14030SSQDDAQ1.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1403SQ
LMR14030SSQDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1403SQ
LMR14030SSQDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1403SQ

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

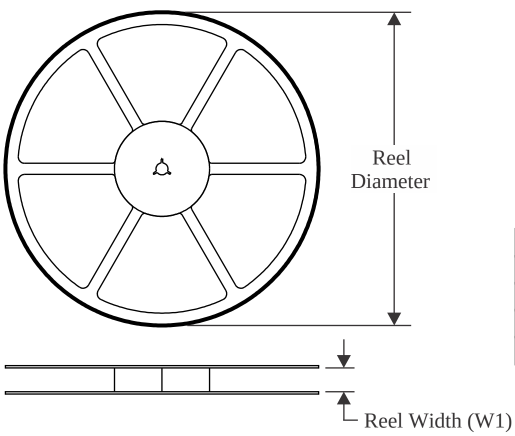
OTHER QUALIFIED VERSIONS OF LMR14030-Q1 :

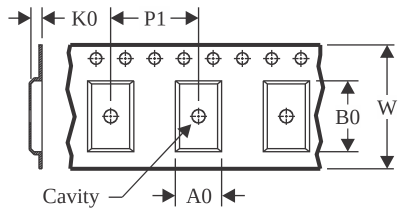
- Catalog : LMR14030

NOTE: Qualified Version Definitions:

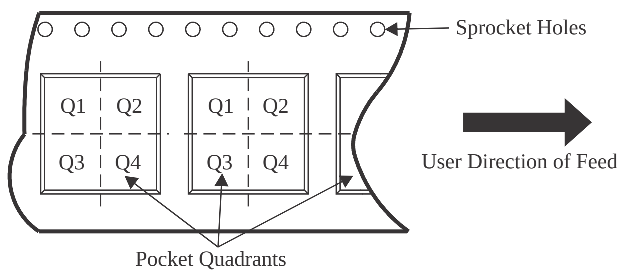
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





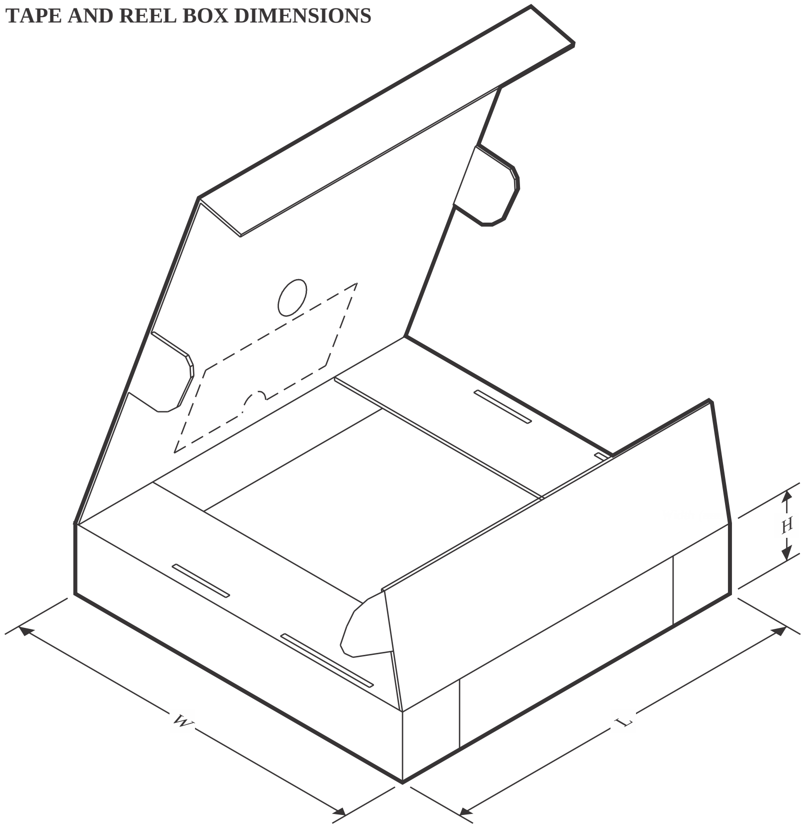
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR14030QDPRRQ1	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LMR14030QDPRTQ1	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LMR14030SQDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR14030SQDPRRQ1	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LMR14030SQDPRTQ1	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LMR14030SSQDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

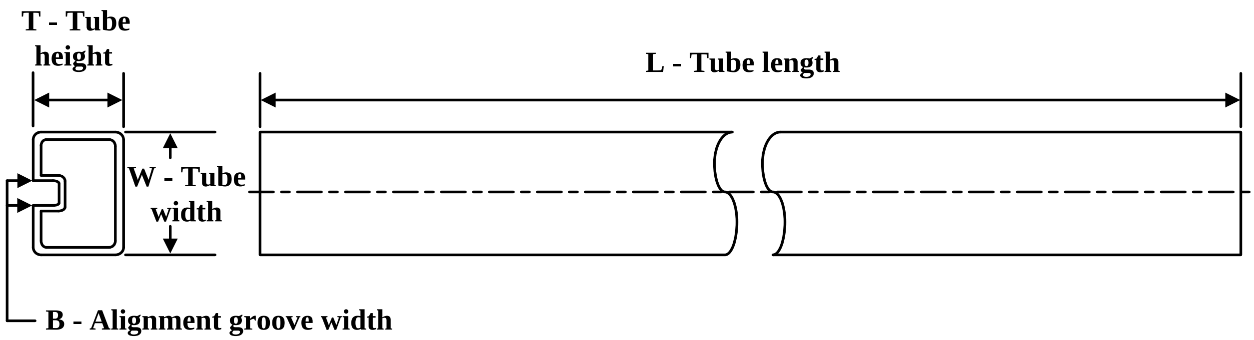
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

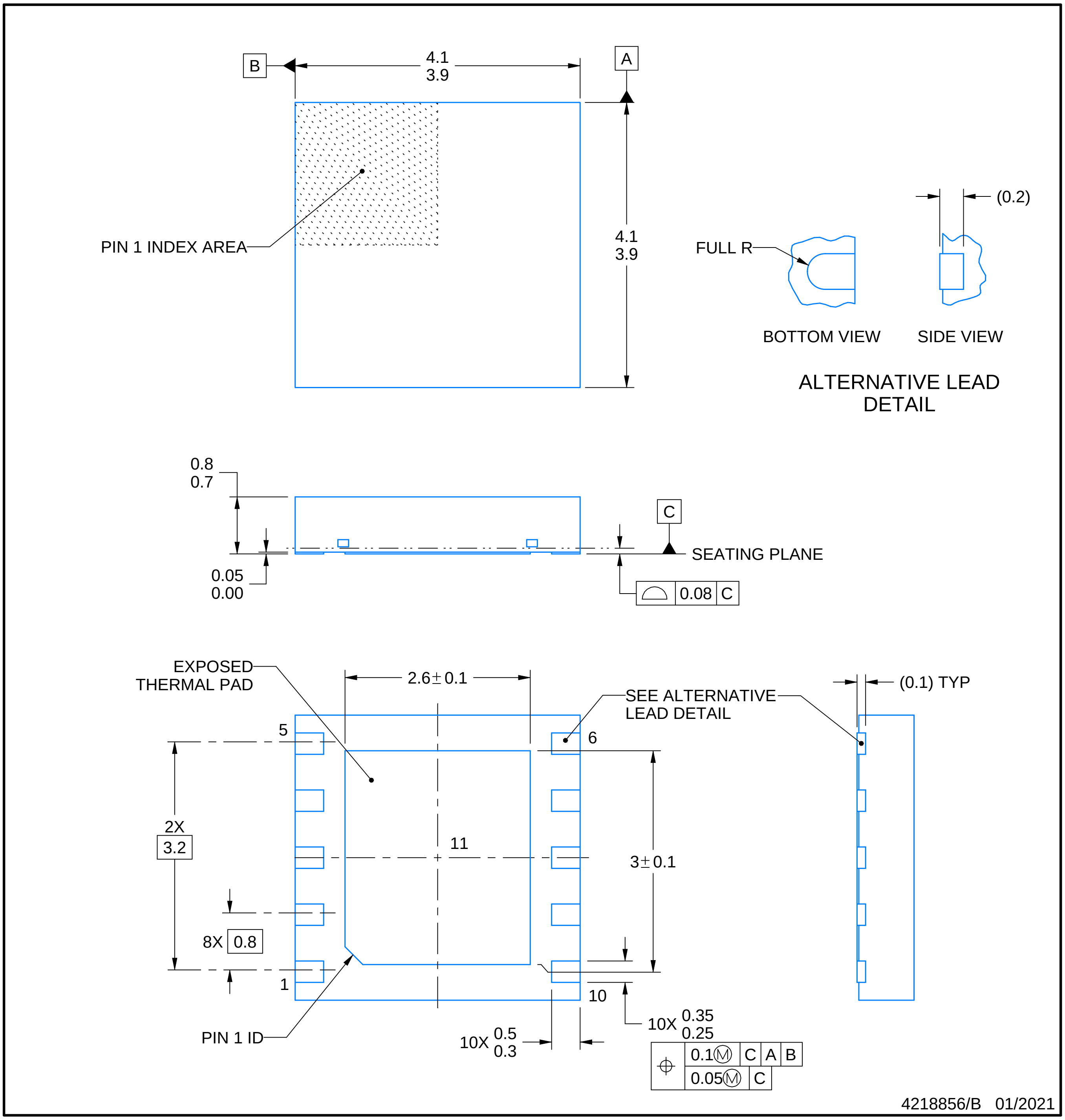
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR14030QDPRRQ1	WSON	DPR	10	3000	346.0	346.0	33.0
LMR14030QDPRTQ1	WSON	DPR	10	250	210.0	185.0	35.0
LMR14030SQDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR14030SQDPRRQ1	WSON	DPR	10	3000	346.0	346.0	33.0
LMR14030SQDPRTQ1	WSON	DPR	10	250	210.0	185.0	35.0
LMR14030SSQDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE



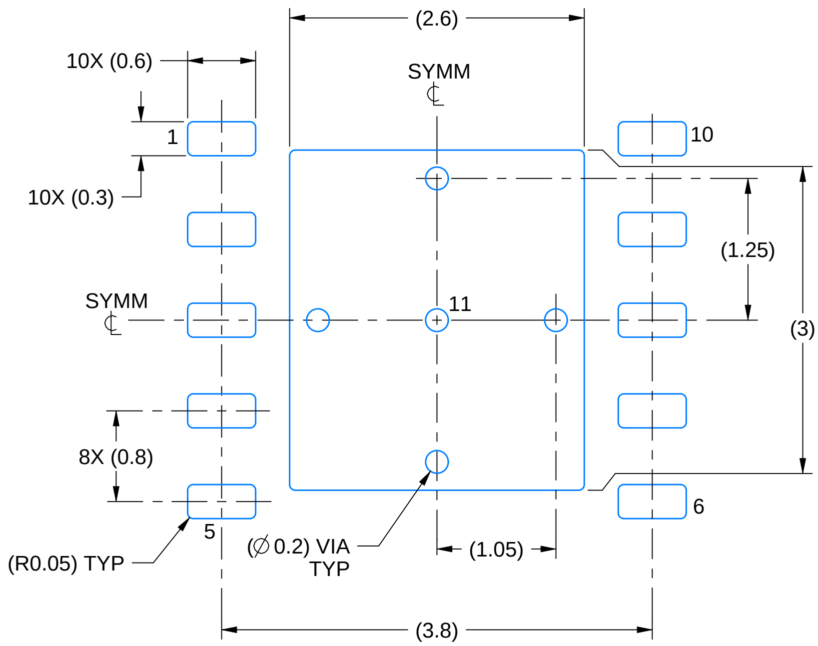
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMR14030SQDDAQ1	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR14030SQDDAQ1.A	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR14030SSQDDAQ1	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR14030SSQDDAQ1.A	DDA	HSOIC	8	75	517	7.87	635	4.25

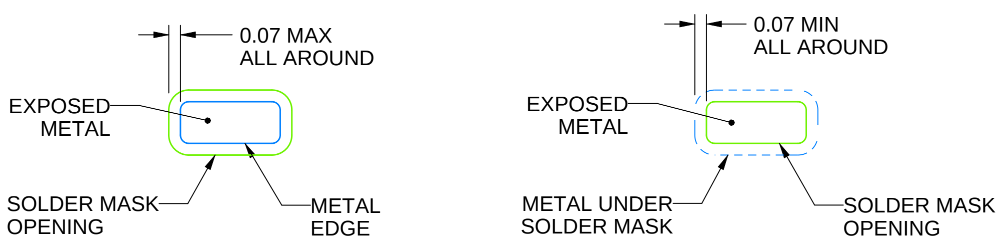


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

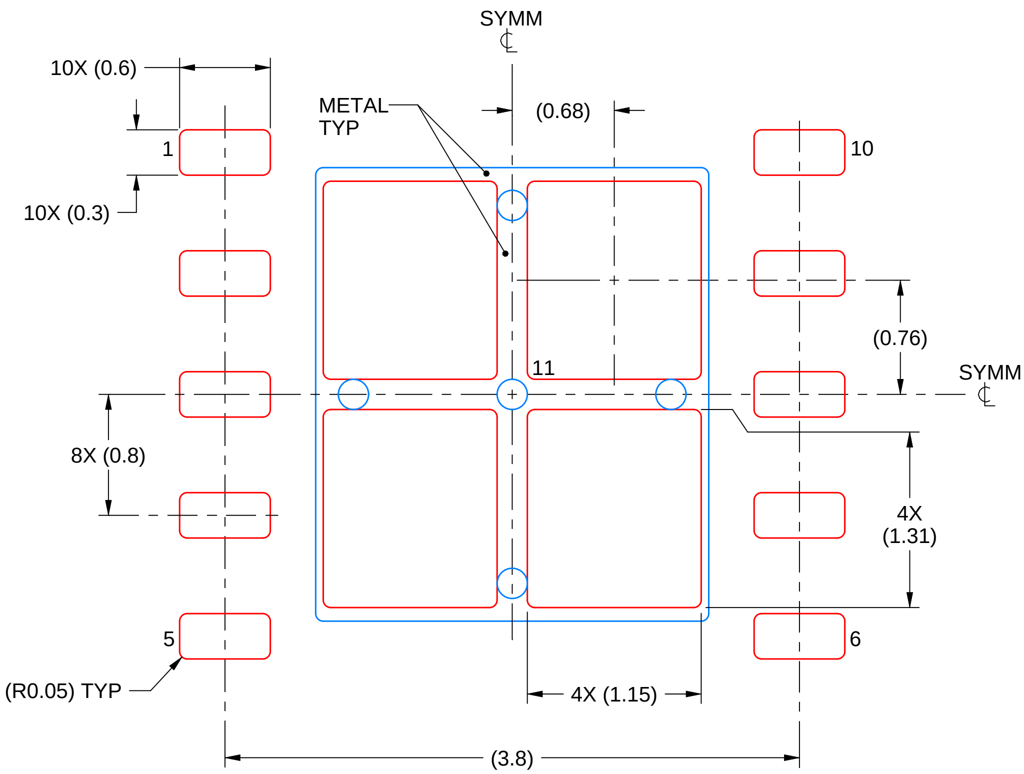
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

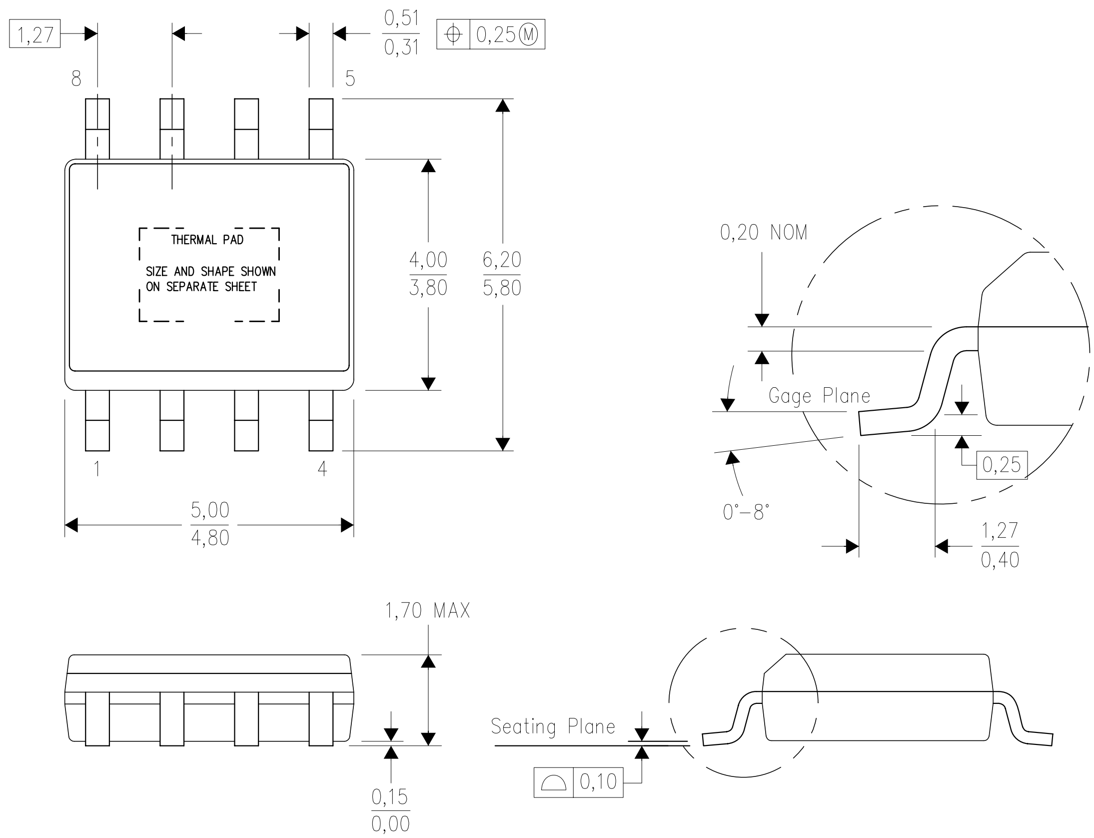
EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

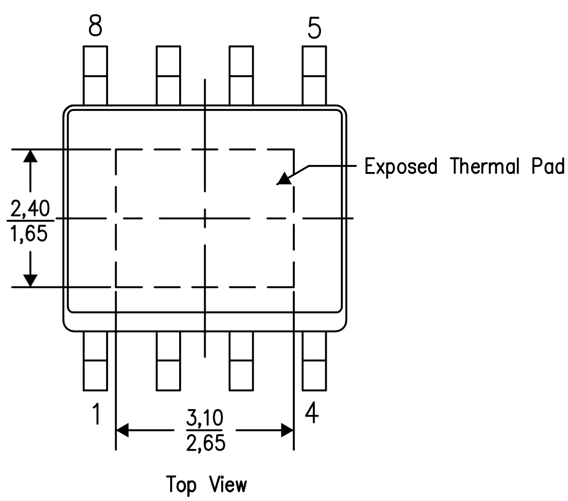
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

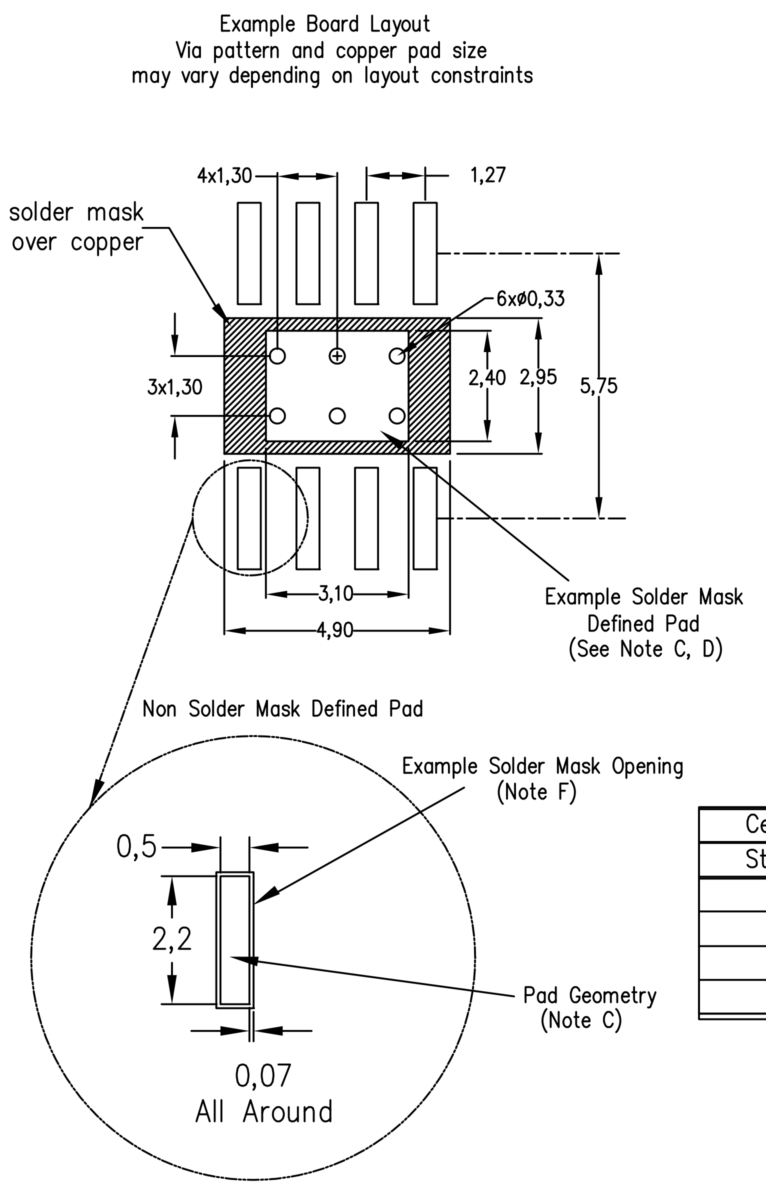


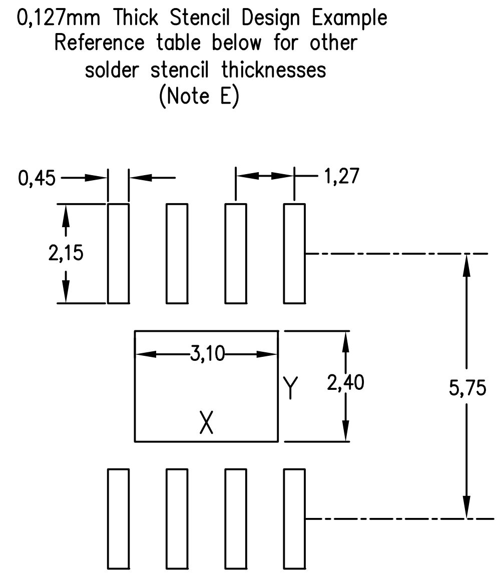
Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951-6/D 04/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.