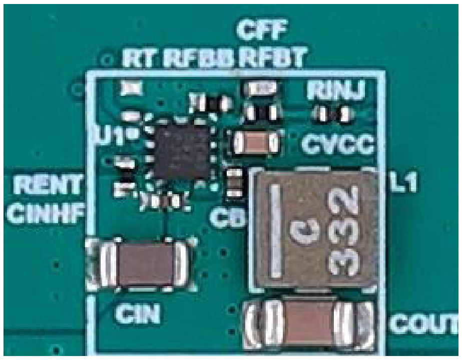
LMR436x0, 36-V, 1-A/2-A Buck Converter with < 2.5 µA I_Q at 150°C T_{JMAX} in 4-mm^2 HotRod™ QFN

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Miniature solution size and low component cost
  - 2-mm × 2-mm HotRod™ package with wettable flanks
  - Internal compensation
- Optimized for ultra-low EMI requirements
  - Pin selectable FPWM mode for constant frequency at light loads with MODE/SYNC pin
  - F_{SW} synchronization with MODE/SYNC pin
- Designed for industrial applications
  - –40°C to +150°C junction temperature range
  - Supports 42-V transients
  - Supports 3-V_{IN} minimum
  - Adjustable up to 95% of V_{IN}, 3.3-V and 5-V fixed V_{OUT} options available
- Greater than 85% efficiency at 1 mA
  - 1.3-µA I_Q at 24 V_{IN}, 5 V_{OUT} (fixed)
- Designed for scalable power supplies
  - 200 kHz to 2.2 MHz (RT pin) adjustable F_{SW}
  - Pin compatible with:
    - LMR36506 (65 V, 600 mA)
    - LMR36503 (65 V, 300 mA)

2 Applications

- Factory automation: Field transmitters and process sensors
- Building automation: HVAC and fire safety
- Appliances: Garden and power tools



Typical Solution Size (10 mm × 10 mm)

3 Description

The LMR436x0 is the industry smallest 36-V, 2-A, and 1-A synchronous step-down DC/DC converters in a 2-mm × 2-mm HotRod package. This easy-to-use converter supports a wide input voltage range of 3.0 V to 36 V with transients up to 42 V.

The control architecture and feature-set are optimized for an ultra-small solution size. The device uses peak current mode control to minimize output capacitance. The LMR436x0 minimizes input filter size by using dual random spread spectrum, a low-EMI HotRod package, and an optimized pinout. The MODE/SYNC and RT pin variants can be used to set or synchronize the frequency between 200 kHz and 2.2 MHz to avoid noise sensitive frequency bands.

The compact solution size and rich feature set of LMR436x0 simplifies implementation for a wide range of industrial applications.

Package Information

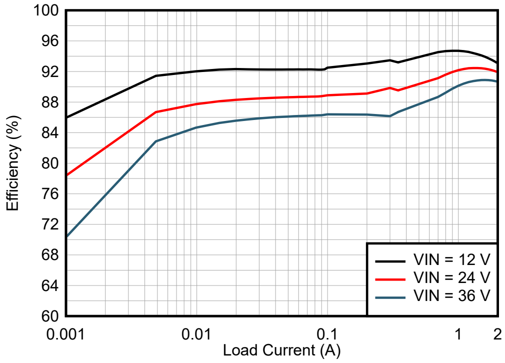
PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
LMR43620	RPE (VQFN-HR, 9)	2.00 mm × 2.00 mm
LMR43610		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Information

PART NUMBER	RATED OUTPUT CURRENT[1]
LMR43620	2 A
LMR43610	1 A

(1) See the *Device Comparison Table*.



Efficiency: V_{OUT} = 5 V (Fixed), 1 MHz

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

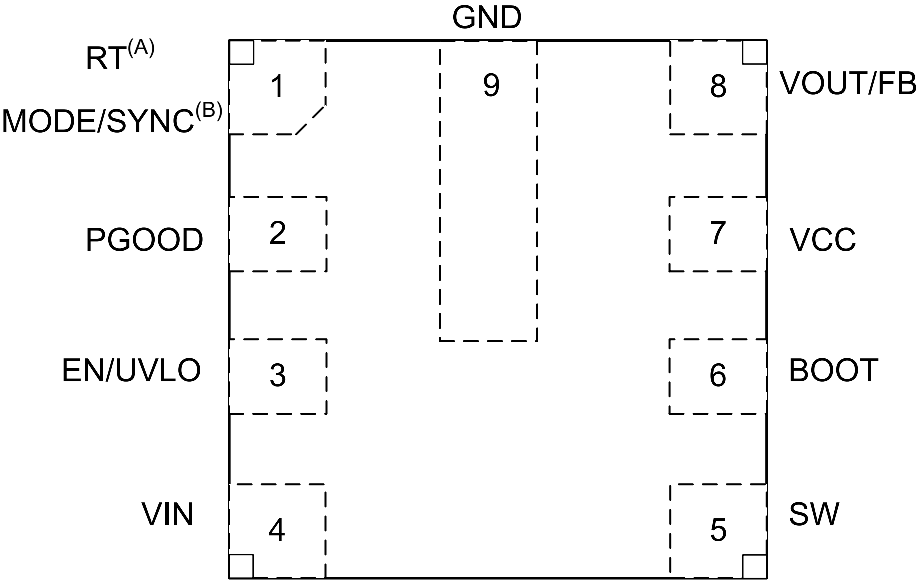
Changes from Revision A (October 2021) to Revision B (May 2023)	Page
• Changed document status from Advance Information to Production Data	1

5 Device Comparison Table

ORDERABLE PART NUMBER (1)	OUTPUT CURRENT	OUTPUT VOLTAGE	EXTERNAL SYNC	F_{SW}	SPREAD SPECTRUM
LMR43620MB5RPER	2 A	5-V fixed / adjustable	Yes (PFM/FPWM Selectable)	Fixed 1 MHz	No
LMR43620R5RPER	2 A	5-V fixed / adjustable	No (Default PFM at light load)	Adjustable with RT resistor	No
LMR43610MB3RPER	1 A	3.3-V fixed / adjustable	Yes (PFM/FPWM Selectable)	Fixed 1 MHz	No
LMR43610R3RPER	1 A	3.3-V fixed / adjustable	No (Default PFM at light load)	Adjustable with RT resistor	No

(1) For more information on device orderable part numbers, see *Device Nomenclature*.

6 Pin Configuration and Functions



A. See Device Comparison Table for more details. Pin 1 is factory-set for externally adjustable switching frequency RT variants only.

B. Pin 1 factory-set for fixed switching frequency MODE/SYNC variants only.

Figure 6-1. 9-Pin (2 mm × 2 mm) VQFN-HR RPE Package (Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RT or MODE/SYNC	A	For the RT variant, the switching frequency can be adjusted from 200 kHz to 2.2 MHz. For the MODE/SYNC variant, it can operate in user-selectable PFM/FPWM mode and can be synchronized to an external clock. *Do not float this pin.*
2	PGOOD	A	Open-drain power-good flag output. Connect to a suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. It goes low when EN = low. It can be open or grounded when not used.
3	EN/UVLO	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. *Do not float this pin.*
4	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND.
5	SW	P	Regulator switch node. Connect to power inductor.
6	BOOT	P	Bootstrap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin.
7	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
8	VOUT/FB	A	Fixed output options and adjustable output options are available with the VOUT/FB pin variant. Connect to the output voltage node for fixed VOUT. Connect to tap point of feedback voltage divider for adjustable VOUT. See Section 9.2.2.2.1 for how to select feedback resistor divider values. Check Section 5 for more details. *Do not float this pin.*
9	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
A = Analog, P = Power, G = Ground			

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to GND	–0.3	42	V
Voltages	SW to GND	–0.3	V_{IN} + 0.3	V
Voltages	BOOT to SW	–0.3	5.5	V
Voltages	VCC to GND	–0.3	5.5	V
Voltages	VOUT/FB to GND	–0.3	16	V
Voltages	SYNC/MODE or RT to GND	–0.3	5.5	V
Voltages	PGOOD to GND	–0.3	20	V
Voltages	EN to GND	–0.3	42	V
Temperature	T_J, Junction temperature	–40	150	°C
Temperature	T_{stg}, Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40 °C to 150 °C (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input Voltage Range for start-up	3.6	36	V
	Input Voltage Range after start-up	3.0	36	V
V_{OUT}	Output Voltage Range with Adjustable Output Voltage Setup	1	0.95 * VIN	V
I_{OUT}	LMR43620 Continuous DC Output Current Range	0	2	A
I_{OUT}	LMR43610 Continuous DC Output Current Range	0	1	A
T_J	Operating junction temperature	–40	150	°C

7.4 Thermal Information

The value of $R_{\theta JA}$ in this table is only valid for comparison with other packages. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, a 4-layer PCB can achieve a $R_{\theta JA}$= 50°C/W.

THERMAL METRIC (1)		LMR436x0	UNIT
		RPE (VQFN-HR)	
		9 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance for LMR43620MQ3EVM-2M	50	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{INMIN}	Input voltage rising threshold for start-up	Before start-up	3.2	3.35	3.5	V
	Input voltage falling threshold	After operating	2.45	2.7	3	V
$I_{SD(VIN)}$	Shutdown quiescent current at VIN pin	EN = 0 V		0.25	1	µA
I_{BIAS}	Non-switching input current at VOUT/FB	Fixed 5.0-V Vout, $V_{VOUT/FB}$ = 5.25 V		4.2	6.5	µA
I_{BIAS}	Non-switching input current at VOUT/FB	Fixed 3.3-Vout, $V_{VOUT/FB}$ = 3.47 V		4.2	6.5	µA
$I_{QVIN(nonsw)}$	Non-switching input current; measured at VIN pin (1)	Fixed 5.0-V V_{OUT}, $V_{VOUT/FB}$ = 5.25 V		1.6	3	µA
$I_{QVIN(nonsw)}$	Non-switching input current; measured at VIN pin (1)	Fixed 3.3-V V_{OUT}, $V_{VOUT/FB}$ = 3.47 V		1.2	2.2	µA
ENABLE (EN PIN)						
$V_{EN-WAKE}$	EN wakeup threshold		0.5	0.7	1	V
$V_{EN-VOUT}$	Precision enable rising threshold for V_{OUT}		1.16	1.23	1.3	V
$V_{EN-HYST}$	Enable hysteresis below $V_{EN-VOUT}$		0.3	0.35	0.4	V
I_{LKG-EN}	Enable pin input leakage current	V_{EN} = V_{IN} = 13.5 V		10		nA
INTERNAL LDO (VCC PIN)						
V_{CC}	VCC pin output voltage	V_{FB} = 0 V, I_{VCC} = 1 mA	3.1	3.3	3.45	V
VOLTAGE FEEDBACK (VOUT/FB PIN)						
V_{OUT}	Output voltage accuracy for fixed V_{OUT}	3.3-V V_{OUT}, V_{IN} = 3.6 V to 36 V, FPWM Mode	3.27	3.3	3.33	V
V_{OUT}	Output voltage accuracy for fixed V_{OUT}	5-V V_{OUT}, V_{IN} = 5.5 V to 36 V, FPWM Mode	4.94	5.00	5.06	V
V_{FB}	Internal reference voltage accuracy	V_{OUT} = 1 V, V_{IN} = 3.0 V to 36 V, FPWM Mode	0.99	1.00	1.01	V
$I_{FB(LKG)}$	FB input current	Adjustable configuration, FB = 1 V		10		nA
CURRENT LIMITS						
$I_{PEAKMAX}$	High-side peak current limit	LMR43610	1.4	1.8	2.1	A
I_{VALMAX}	Low-side valley current limit	LMR43610	0.85	1.1	1.4	A
$I_{PEAKMIN}$	Minimum peak current limit	LMR43610, Auto Mode	0.17	0.27	0.4	A
I_{NEGMIN}	Low-side valley current negative limit	LMR43610, FPWM Mode	-1	-0.8	-0.6	A
$I_{PEAKMAX}$	High-side peak current limit	LMR43620	2.8	3.4	3.9	A

7.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VALMAX}	Low-side valley current limit	LMR43620	1.9	2.2	2.53	A
$I_{PEAKMIN}$	Minimum peak current limit	LMR43620, Auto Mode	0.37	0.5	0.65	A
I_{NEGMIN}	Negative current limit	LMR43620, FPWM Mode	-1	-0.8	-0.6	A
I_{ZC}	Zero-cross current limit	Auto Mode	30	80	135	mA
POWER GOOD (PGOOD PIN)						
PGD_{OV}	PGOOD upper threshold - rising	% of VOUT/FB (Fixed or Adj. output)	104	108	111	%
PGD_{UV}	PGOOD upper threshold - falling	% of VOUT/FB (Fixed or Adj. output)	89	91	94.2	%
PGD_{HYST}	PGOOD recovery hysteresis for OV	% of VOUT/FB target regulation voltage	2	2.4	2.8	%
	PGOOD recovery hysteresis for UV	% of VOUT/FB target regulation voltage	1.1	3.3	5.9	%
$V_{PGD\text{-}VAL}$	Minimum V_{IN} for PGOOD function	V_{EN} = 0 V, R_{PGD_PU} = 10 kΩ			1.5	V
R_{PGD}	PGOOD ON resistance	V_{EN} = 3.3 V, 200 µA pull up current			100	Ω
R_{PGD}	PGOOD ON resistance	V_{EN} = 0 V, 200 µA pull up current			100	Ω
Soft Start						
POWER STAGE						
V_{BOOT_UVLO}	Voltage on BOOT pin compared to SW which will turnoff high-side switch			2.1		V
$R_{DSON\text{-}HS}$	High-side MOSFET on-resistance	Load = 1 A		132	260	mΩ
$R_{DSON\text{-}LS}$	Low-side MOSFET on-resistance	Load = 1 A		75	140	mΩ
SOFT START						
t_{SS}	Time from first SW pulse to VOUT/FB at 90% of set point.		2	3.5	4.6	ms
t_{HICCUP}	Time in hiccup before retry soft start		30	50	75	ms
POWER GOOD (PGOOD PIN)						
t_{RESET_FILTER}	PGOOD deglitch delay at falling edge		25	40	75	µs
t_{PGOOD_ACT}	Delay time to PGOOD high signal		1.35	2.5	4	ms
OSCILLATOR (SYNC/MODE PIN)						
t_{PULSE_H}	High duration needed to be recognized as a pulse		100			ns
t_{PULSE_L}	Low duration needed to be recognized as a pulse		100			ns
t_{SYNC}	High/Low level pulse maximum duration to be recognized as a valid clock signal				6	µs
t_{MODE}	Time at one level needed to indicate FPWM or Auto Mode		12.5			µs
OSCILLATOR (SYNC/MODE PIN)						
$F_{SW(1MHz)}$	Frequency of 1MHz variant in FPWM		0.9	1	1.1	MHz
f_{SYNC}	Frequency SYNC range		0.2		2.5	MHz
V_{MODE_L}	SYNC/MODE input voltage low level threshold		1			V
V_{MODE_H}	SYNC/MODE input voltage high level threshold				1.6	V
OSCILLATOR (RT PIN)						
$F_{SW(1MHz)}$	Switching frequency with Internal fixed 1 MHz setting	RT pin tie to V_{CC}	0.9	1	1.1	MHz
$F_{SW(2p2MHz)}$	Switching frequency with fixed 2.2 MHz	RT pin tied to GND	2.1	2.2	2.3	MHz
$F_{SW(Adj)}$	Accuracy of external frequency, 400 kHz	R_{RT} = 39.2 kΩ 0.1% resistor	0.34	0.4	0.46	MHz

7.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCH NODE						
t_{ON-MIN}	Minimum HS switch on-time	FPWM mode I_{OUT} = 1 A, 2.2 MHz fixed		65	75	ns
$t_{OFF-MIN}$	Minimum HS switch off-time			60	85	ns
t_{ON-MAX}	Maximum HS switch on-time	HS timeout in dropout	6	9	13	µs

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.

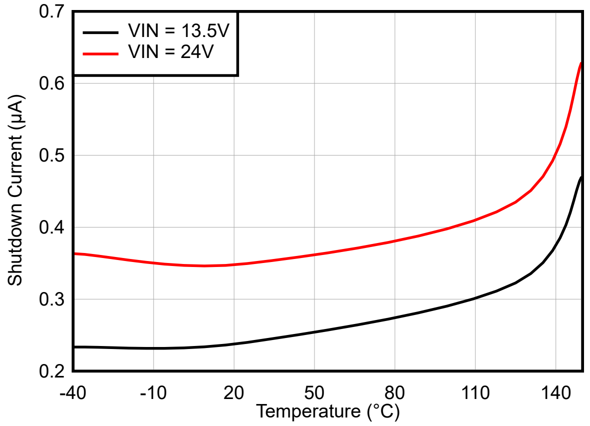
7.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{QVIN}	Input current to V_{IN}	V_{IN} = 13.5 V, Fixed 3.3-V V_{OUT}, I_{OUT} = 0 A, Auto mode		1.5		µA
		V_{IN} = 13.5 V, Fixed 5-V V_{OUT}, I_{OUT} = 0 A, Auto mode		2		µA
POWER STAGE						
V_{DROP1}	Input to output voltage differential to maintain V_{OUT} regulation ≥ 95%, with frequency foldback	V_{OUT} = 3.3-V, fixed 2.2 MHz, I_{OUT} = 1 A		0.2		V
		V_{OUT} = 5-V, fixed 2.2 MHz, I_{OUT} = 1 A		0.2		V
V_{DROP2}	Input to output voltage differential to maintain V_{OUT} regulation ≥ 95% and F_{SW} ≥ 1.85 MHz	V_{OUT} = 3.3-V, fixed 2.2 MHz, I_{OUT} = 1 A		0.7		V
	Input to output voltage differential to maintain V_{OUT} regulation ≥ 95% and F_{SW} ≥ 1.85 MHz	V_{OUT} = 5-V, fixed 2.2 MHz trim, I_{OUT} = 1 A		0.9		V
D_{MAX}	Maximum switch duty cycle	While in frequency fold-back		98		%
		F_{sw} = 1.85 MHz, V_{OUT} = 5.0-V, I_{OUT} = 1 A		87		%
$R_{FBPARA(min)}$	Minimum value of the parallel feedback resistors: R_{FBT}//R_{FBB}			5		kΩ
PROTECTION						
$T_{SD(trip)}$	Thermal shutdown temperature	Shutdown temperature	158	168	186	°C
$T_{SD(hyst)}$	Thermal shutdown temperature	Recovery temperature		15	20	°C

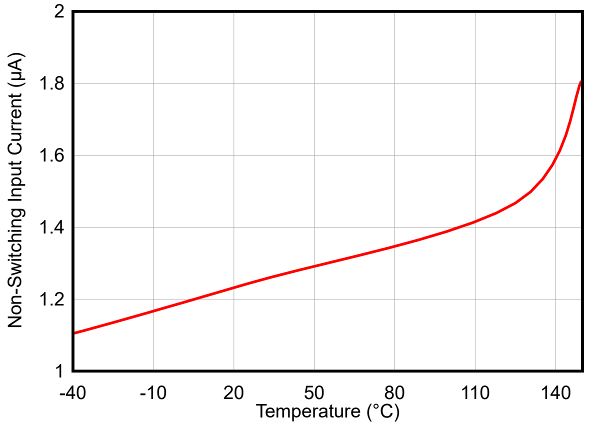
7.7 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C, V_{IN} = 13.5 V



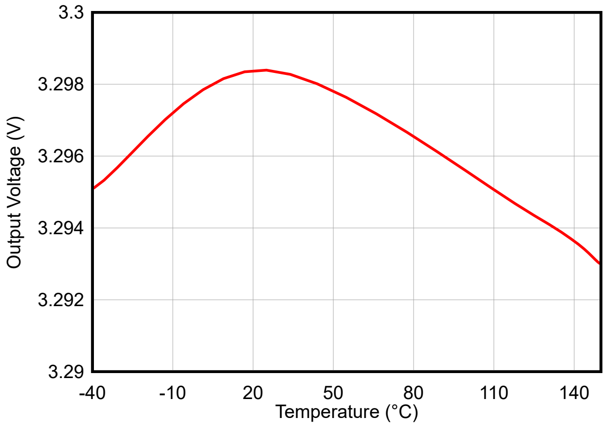
V_{OUT} = 3.3-V fixed

Figure 7-1. Shutdown Current Versus Temperature



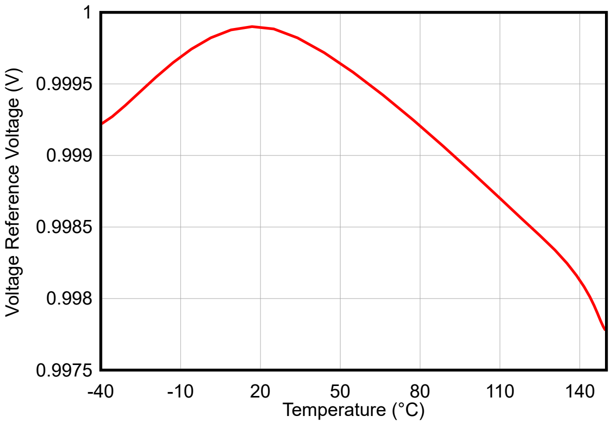
V_{OUT} = 3.3-V fixed

Figure 7-2. Nonswitching Input Current ($I_{QVIN(nonsw)}$) Versus Temperature



V_{OUT} = 3.3-V fixed

Figure 7-3. Output Voltage Accuracy Versus Temperature



V_{OUT} = adjustable

Figure 7-4. Feedback Voltage Accuracy Versus Temperature

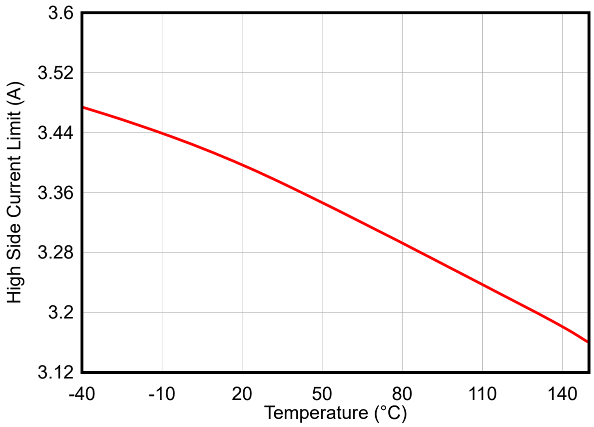


Figure 7-5. High Side MOSFET Current Limit Versus Temperature

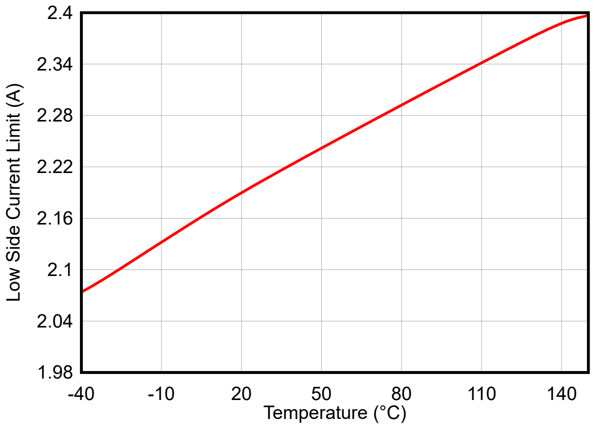


Figure 7-6. Low Side MOSFET Current Limit Versus Temperature

8 Detailed Description

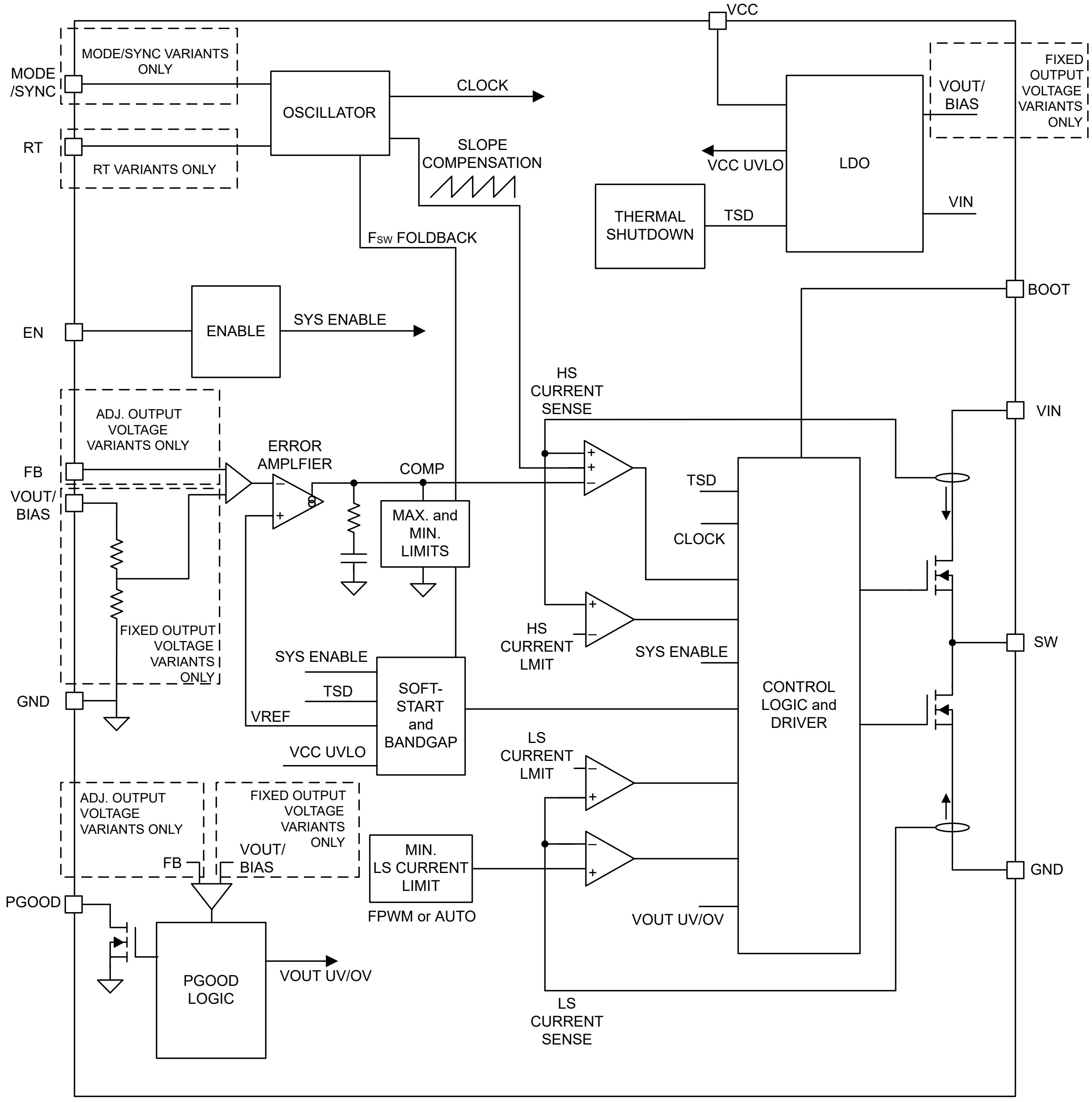
8.1 Overview

The LMR436x0 is a wide input, low-quiescent current, high-performance regulator that can operate over a wide range of duty ratio and switching frequencies, including sub-AM band at 400 kHz and above AM band at 2.2 MHz. During wide input transients, if the minimum on time or the minimum off time cannot support the desired duty ratio at the higher switching frequency settings, the switching frequency is reduced automatically, allowing the LMR436x0 to maintain the output voltage regulation. With an internally compensated design optimized for minimal output capacitors, the system design process with the LMR436x0 is simplified significantly compared to other buck regulators available in the market.

The LMR436x0 is designed to minimize external component cost and solution size while operating in all demanding industrial environments. The LMR436x0 family includes variants that can be set up to operate over a wide switching frequency range, from 200 kHz to 2.2 MHz, with the correct resistor selection from the RT pin to ground. To further reduce system cost, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

The LMR436x0 comes in an ultra-small 2-mm × 2-mm QFN package with wettable flanks, allowing for quick optical inspection along with specially designed corner anchor pins for reliable board level solder connections.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable, Start-Up, and Shutdown

Voltage at the EN pin controls the start-up or remote shutdown of the LMR436x0 family of devices. The part stays shut down as long as the EN pin voltage is less than $V_{EN\text{-}WAKE}$ = 0.5 V. During shutdown, the input current drawn by the device typically drops down to 0.25 µA (V_{IN} = 13.5 V). With the voltage at the EN pin greater than $V_{EN\text{-}WAKE}$, the device enters device standby mode and the internal LDO powers up to generate VCC. As the EN voltage increases further, approaching $V_{EN\text{-}VOUT}$, the device finally starts to switch, entering start-up mode with a soft start. During the device shutdown process, when the EN input voltage measures less than ($V_{EN\text{-}VOUT}$ – $V_{EN\text{-}HYST}$), the regulator stops switching and re-enters device standby mode. Any further decrease in the EN pin voltage, below $V_{EN\text{-}WAKE}$, and the device is then firmly shut down. The high-voltage compliant EN input pin can be connected directly to the V_{IN} input pin if remote precision control is not needed. The EN input pin must not be allowed to float. The various EN threshold parameters and their values are listed in *Electrical Characteristics*. Figure 8-2 shows the precision enable behavior and Figure 8-3 shows a typical remote EN start-up waveform in an application. After EN goes high, after a delay of about 2.5 ms, the output voltage begins to rise with a soft start and reaches close to the final value in about 3.5 ms (t_{ss}). After a delay of about 2.5 ms (t_{PGOOD_ACT}), the PGOOD flag goes high. During start-up, the device is not allowed to enter FPWM mode until the soft-start time has elapsed. This time is measured from the rising edge of EN. Check Section 9.2.2.8.1 for component selection.

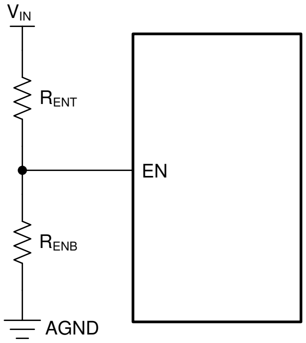


Figure 8-1. VIN UVLO Using the EN Pin

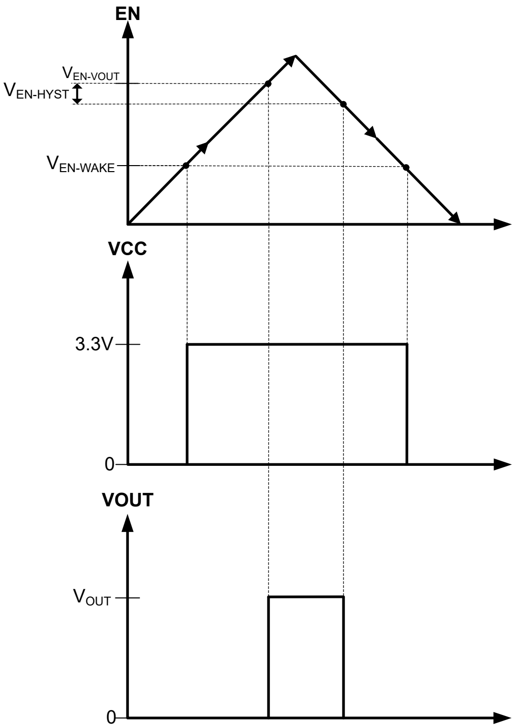


Figure 8-2. Precision Enable Behavior

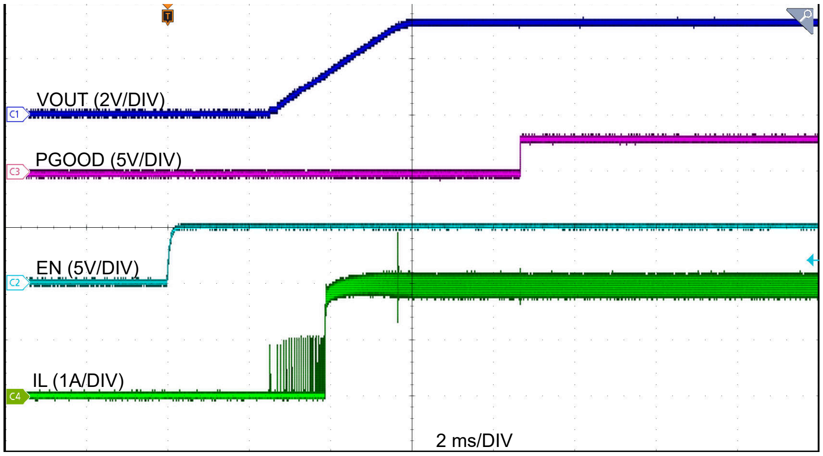


Figure 8-3. Enable Start-Up V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A

8.3.2 External CLK SYNC (with MODE/SYNC)

It is often desirable to synchronize the operation of multiple regulators in a single system, resulting in a well-defined system level performance. The select variants in the LMR436x0 with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. The LMR436x0 implements an in-phase locking scheme, where the rising edge of the clock signal, provided to the MODE/SYNC pin of the LMR436x0, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL), eliminating any large glitches. The external clock fed into the LMR436x0 replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well-regulated. The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

The MODE/SYNC input pin in the LMR436x0 can operate in one of three selectable modes:

- Auto mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor. See Section 8.4.3.2 for more details.
- FPWM mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current. See Section 8.4.3.3 for more details.
- SYNC mode: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off time or minimum on time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, it operates as though in FPWM mode: diode emulation is disabled, allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

8.3.2.1 Pulse-Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the LMR436x0 are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-dependent MODE/SYNC pin control is useful with these systems. To initiate pulse-dependent MODE/SYNC pin control, a valid sync signal must be applied. Table 8-1 shows a summary of the pulse dependent mode selection settings.

Table 8-1. Pulse-Dependent Mode Selection Settings

MODE/SYNC INPUT	MODE
> V_{MODE_H}	FPWM with spread spectrum factory setting
< V_{MODE_L}	Auto mode with spread spectrum factory setting
Synchronization Clock	SYNC mode

Figure 8-4 shows the transition between auto mode and FPWM mode while in pulse-dependent MODE/SYNC control. The LMR436x0 transitions to a new mode of operation after the time, t_{MODE}. Figure 8-4 and Figure 8-5 show the details.

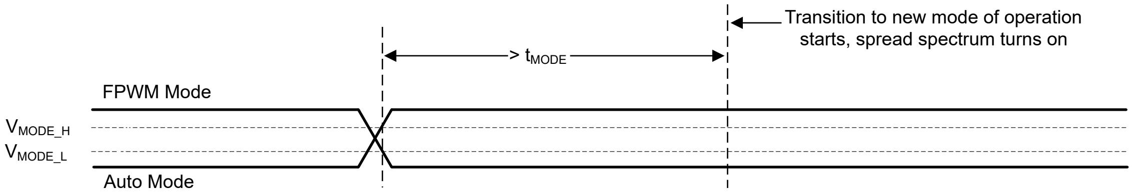


Figure 8-4. Transition from Auto Mode and FPWM Mode

If MODE/SYNC voltage remains constant longer than t_{MODE}, the LMR436x0 enters either auto mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in pulse-dependent scheme.

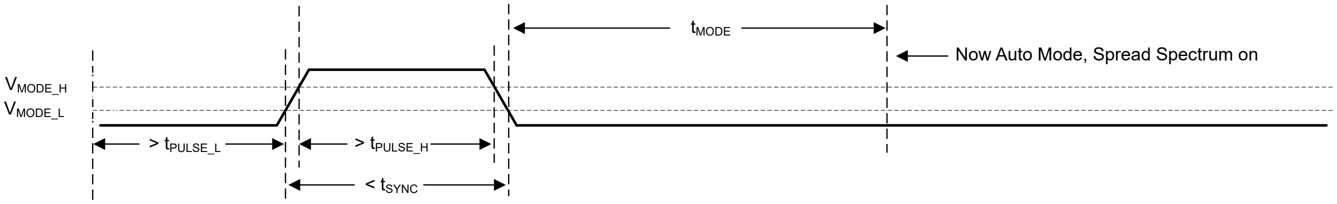


Figure 8-5. Transition from SYNC Mode to Auto Mode

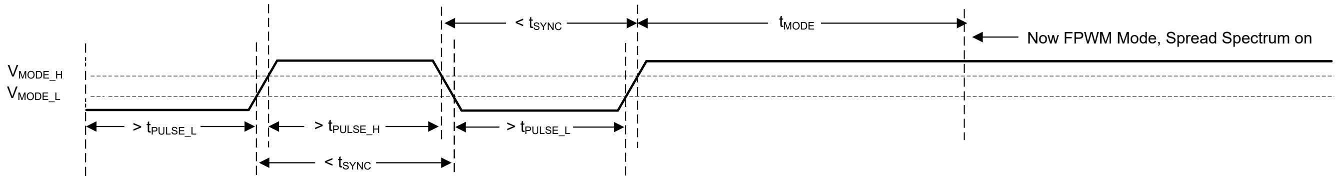


Figure 8-6. Transition from SYNC Mode to FPWM Mode

8.3.3 Adjustable Switching Frequency (with RT)

The select variants in the LMR436x0 family with the RT pin allow the power designers to set any desired operating frequency between 200 kHz and 2.2 MHz in their applications. See Figure 8-7 to determine the resistor value needed for the desired switching frequency. The RT pin and the MODE/SYNC pin variants share the same pin location. The power supply designer can either use the RT pin variant and adjust the switching frequency of operation as warranted by the application or use the MODE/SYNC variant and synchronize to an external clock signal. See Table 8-2 for selection on programming the RT pin.

Table 8-2. RT Pin Setting

RT INPUT	SWITCHING FREQUENCY
VCC	1 MHz
GND	2.2 MHz
RT resistor to GND	Adjustable according to Figure 8-7
Float (Not Recommended)	No switching

Equation 1 can be used to calculate the value of RT for a desired frequency.

$$RT = \frac{18286}{Fsw^{1.021}} \quad (1)$$

where

- RT is the frequency setting resistor value (kΩ).
- F_{SW} is the switching frequency.

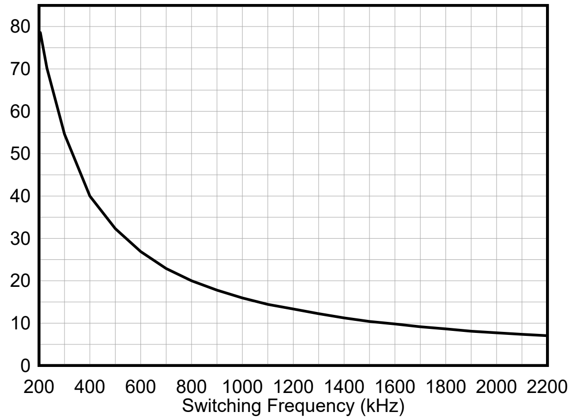


Figure 8-7. RT Values vs Frequency

8.3.4 Power-Good Output Operation

The power-good feature using the PGOOD pin of the LMR436x0 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to Figure 8-8. Table 8-3 gives a more detailed breakdown of the PGOOD operation. Here, $V_{PGD_{UV}}$ is defined as the PGD_{UV} scaled version of V_{OUT} (target regulated output voltage) and $V_{PGD_{HYST}}$ as the PGD_{HYST} scaled version of V_{OUT}, where both PGD_{UV} and PGD_{HYST} are listed in *Electrical Characteristics*. During the initial power up, a total delay of 6 ms (typical) is encountered from the time $V_{EN\text{-}VOUT}$ is triggered to the time that the power-good is flagged high. This delay only occurs during the device start-up and is not encountered during any other normal operation of the power-good function. When EN is pulled low, the power-good flag output is also forced low. With EN low, power-good remains valid as long as the input voltage ($V_{PGD\text{-}VAL}$ is ≥ 1.5 V (max)).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin can be open or grounded. Limit the current into this pin to ≤ 4 mA.

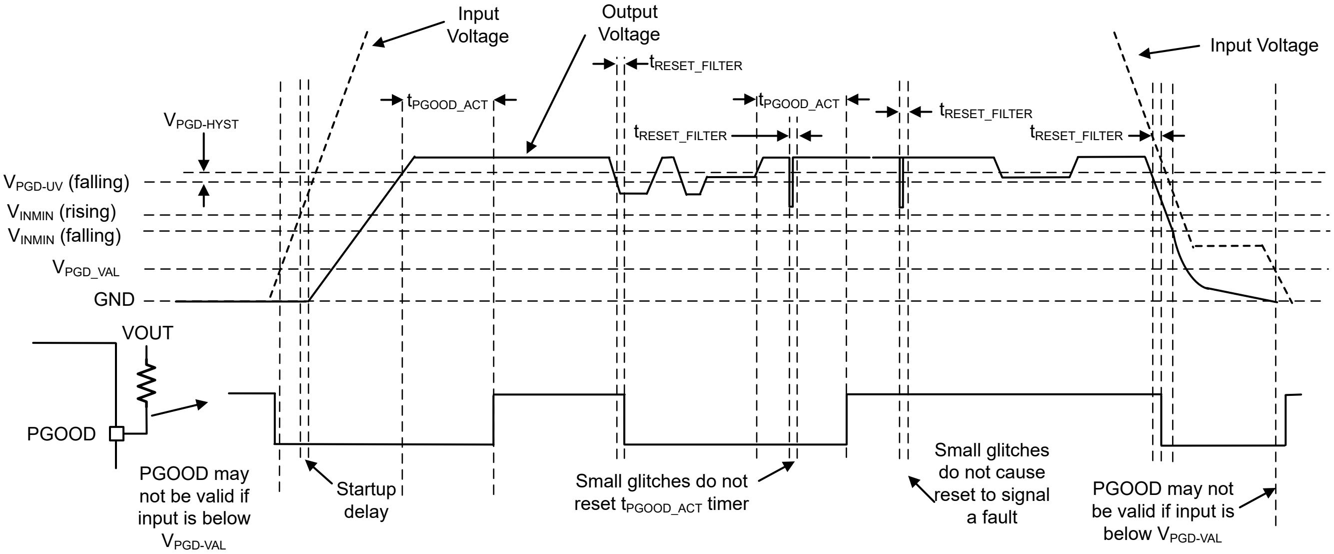


Figure 8-8. Power-Good Operation (OV Events Not Included)

Table 8-3. Fault Conditions for PGOOD (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{PGOOD_ACT} MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)
$V_{OUT} < V_{PGD_{UV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation: $V_{PGD_{UV}} + V_{PGD_{HYST}} < V_{OUT} < V_{PGD_{OV}} - V_{PGD_{HYST}}$
$V_{OUT} > V_{PGD_{OV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation
$T_J > T_{SD(trip)}$	$T_J < T_{SD(trip)} - T_{SD(hyst)}$ AND output voltage in regulation
EN < $V_{EN\text{-}VOUT} - V_{EN\text{-}HYST}$	EN > $V_{EN\text{-}VOUT}$ AND output voltage in regulation

8.3.5 Internal LDO, VCC, and VOUT/FB Input

The LMR436x0 uses the internal LDO output and the VCC pin for all internal power supply. The VCC pin draws power either from the V_{IN} (in adjustable output variants) or the VOUT/FB (in fixed-output variants). In the fixed output variants, after the LMR436x0 is active but has yet to regulate, the VCC rail continues to draw power from the input voltage, V_{IN}, until the VOUT/FB voltage reaches > 3.3 V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.3 V in both adjustable and fixed output variants. During start-up, VCC momentarily exceeds the normal operating voltage, then drops to the normal operating voltage.

8.3.6 Bootstrap Voltage and $V_{BOOT-UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to ensure the HS switch is turned ON. The capacitor connected between BOOT and SW works as a charge pump to boost voltage on the BOOT terminal to (SW+VCC). The boot diode is integrated on the LMR436x0 die to minimize physical solution size. TI recommends a 100-nF capacitor rated for 10 V or higher for CBOOT. The BOOT rail has a UVLO setting. This UVLO has a threshold of $V_{BOOT-UVLO}$ and is typically set at 2.1 V. If the CBOOT capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

8.3.7 Output Voltage Selection

In the LMR436x0 family, an adjustable output or fixed output voltage option is configurable for every device variant (see Section 5). For an adjustable output, the user needs an external resistor divider connection between the output voltage node, the device FB pin, and the system GND, as shown in Figure 8-9. The adjustable output voltage operation uses a 1-V internal reference voltage. Refer to section Section 9.2.2.2.1 for more details on how to adjust the output voltage.

When using the fixed-output configuration from the LMR436x0 family, simply connect the FB pin (identified as VOUT/FB pin for fixed-output variants in the rest of the data sheet) to the system output voltage node. See Section 5 for more details.

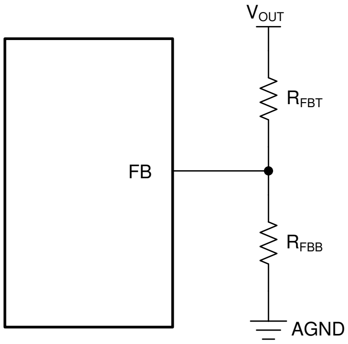


Figure 8-9. Setting Output Voltage for Adjustable Output Variant

In an adjustable output voltage configuration, an addition feedforward capacitor, C_{FF}, in parallel with the R_{FBT}, can be used to optimize the phase margin and transient response. See Section 9.2.2.8 for more details. No additional resistor divider or feedforward capacitor is needed in fixed-output variants.

8.3.8 Soft Start and Recovery from Dropout

When designing with the LMR436x0, slow rise in output voltage due to recovery from dropout and soft start must be considered as a two separate operating conditions, as shown in Figure 8-10 and Figure 8-11. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped up. The net result is that output voltage, if previously 0 V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a pre-bias start-up.

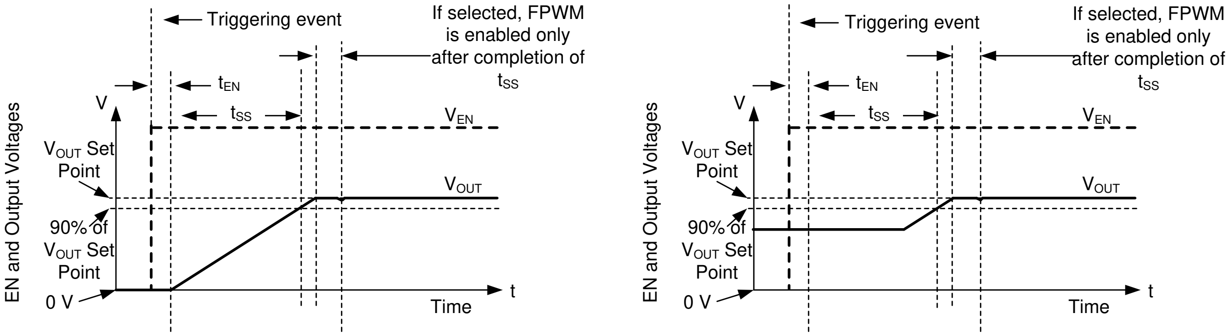


Figure 8-10. Soft Start With and Without Pre-bias Voltage

8.3.8.1 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device is set to FPWM, the device continues to operate in that mode during its recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LMR436x0 can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

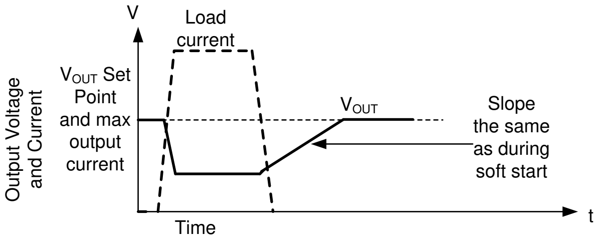


Figure 8-11. Recovery from Dropout

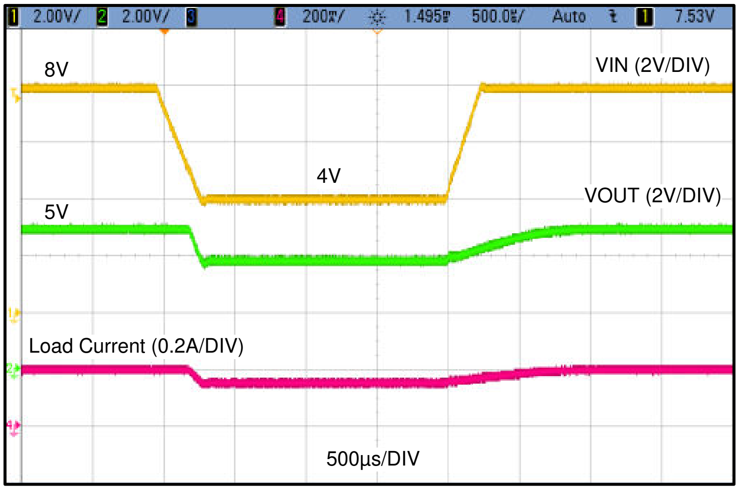


Figure 8-12. Typical Output Recovery from Dropout from 8 V to 4 V

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below its set point is removed, the output climbs at the same speed as during start-up. Figure 8-12 shows an example of this behavior.

8.3.9 Current Limit and Short Circuit

The LMR436x0 is protected from overcurrent conditions by cycle-by-cycle current limiting on both high-side (HS) and low-side (LS) MOSFETs.

High-side MOSFET overcurrent protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Because the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the LS switch is turned on, the current going through it is also sensed and monitored. Like the high-side device, the low-side device has a turn-off commanded by the internal error amplifier loop. In the case of the low-side device, turn-off is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This is called the low-side current limit, I_{VALMAX}. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off after the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

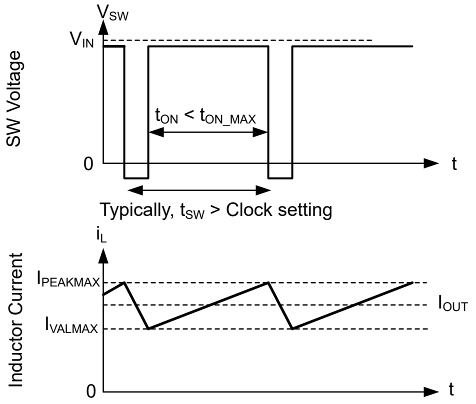


Figure 8-13. Current Limit Waveforms

Because the current waveform assumes values between $I_{PEAKMAX}$ and I_{VALMAX}, the maximum output current is very close to the average of these two values unless duty factor is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If duty factor is very high, current ripple must be very low to prevent instability. Because current ripple is low, the part is able to deliver full current. The current delivered is very close to I_{VALMAX}.

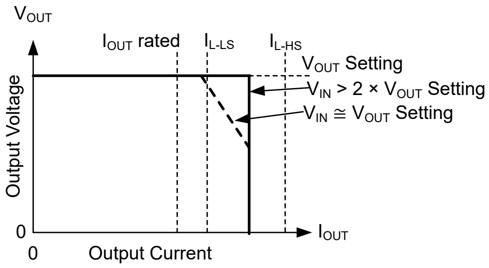


Figure 8-14. Output Voltage Versus Output Current

Under most conditions, current is limited to the average of $I_{PEAKMAX}$ and I_{VALMAX}. If input voltage is low, current can be limited to approximately I_{VALMAX}. Also note that the maximum output current does not exceed the average of $I_{PEAKMAX}$ and I_{VALMAX}. After the overload is removed, the part recovers as though in soft start.

8.3.10 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 153°C (typical). When the junction temperature falls below 153°C (typical), the LMR436x0 attempts another soft start.

While the LMR436x0 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

8.3.11 Input Supply Current

The LMR436x0 is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The VOUT/FB pin in the fixed-output voltage variants is the input to the LDO that powers the majority of the control circuits. By connecting the VOUT/FB input pin to the output node of the regulator, a small amount of current is drawn from the output. This current is reduced at the input by the ratio of V_{OUT} / V_{IN} as described in Equation 2.

$$I_{QVIN} = I_Q + I_{EN} + I_{BIAS} \times \frac{V_{OUT}}{\eta_{eff} \times V_{IN}} \tag{2}$$

where

- I_{QVIN} is the total standby (switching) current consumed by the operating (switching) buck converter when unloaded.
- I_Q is the current drawn from the V_{IN} terminal.
- I_{EN} is current drawn by the EN terminal. Include this current if EN is connected to VIN. Check $I_{LKG\text{-}EN}$ in *Electrical Characteristics* for I_{EN}.
- I_{BIAS} is bias current drawn by the BIAS LDO.
- η_{eff} is the light-load efficiency of the buck converter with I_{QVIN} removed from the input current of the buck converter. η_{eff} = 0.8 is a conservative value that can be used under normal operating conditions.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.7 V (typical), both the converter and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 250 nA.

8.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the converter. When the EN pin voltage is above 1 V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3 V typical. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above its precision enable threshold. The LMR436x0 also employs UVLO protection.

8.4.3 Active Mode

The LMR436x0 is in active mode whenever the EN pin is above $V_{EN\text{-}VOUT}$, V_{IN} is high enough to satisfy V_{INMIN}, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum V_{INMIN}.

In active mode, depending on the load current, input voltage, and output voltage, the LMR436x0 is in one of five modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the inductor current ripple
- Auto mode - Light Load Operation: PFM when switching frequency is decreased at very light load
- FPWM mode - Light Load Operation: Continuous conduction mode (CCM) when the load current is lower than half of the inductor current ripple
- Minimum on time: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation
- Dropout mode: When switching frequency is reduced to minimize voltage dropout

8.4.3.1 CCM Mode

The following operating description of the LMR436x0 refers to Section 8.2 and to the waveforms in Figure 8-15. In CCM, the LMR436x0 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \tag{3}$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \tag{4}$$

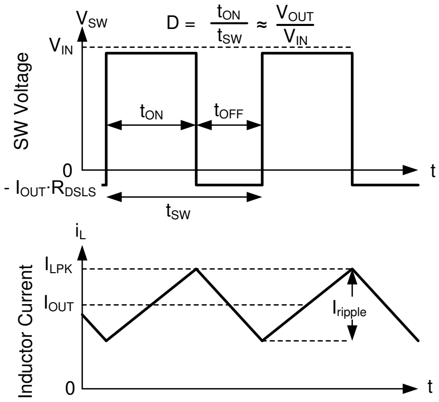


Figure 8-15. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

8.4.3.2 Auto Mode – Light-Load Operation

The LMR436x0 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LMR436x0 operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

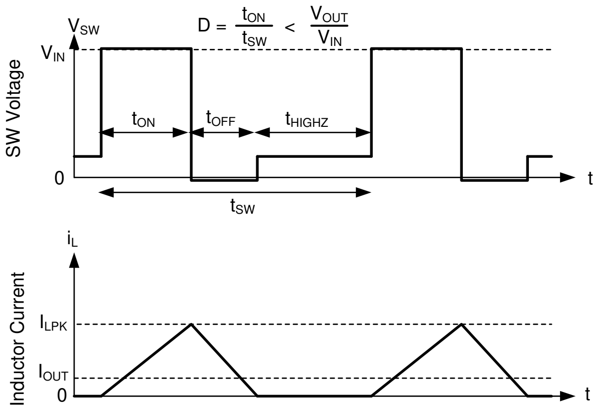
The light-load operation is employed in the LMR436x0 only in auto mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation. See Figure 8-16.
- Frequency reduction. See Figure 8-16.

Note that while these two features operate together to improve light load efficiency, they operate independently.

8.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



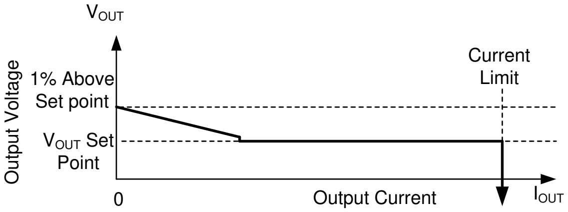
In auto mode, the low-side device is turned off after SW node current is near zero. As a result, after output current is less than half of what inductor ripple is in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

Figure 8-16. PFM Operation

The LMR436x0 has a minimum peak inductor current setting (see $I_{PEAKMIN}$ in *Electrical Characteristics*) while in auto mode. After current is reduced to a low value with fixed input voltage, on time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

8.4.3.2.2 Frequency Reduction

The LMR436x0 reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of VOUT/FB and the voltage applied to VOUT/FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



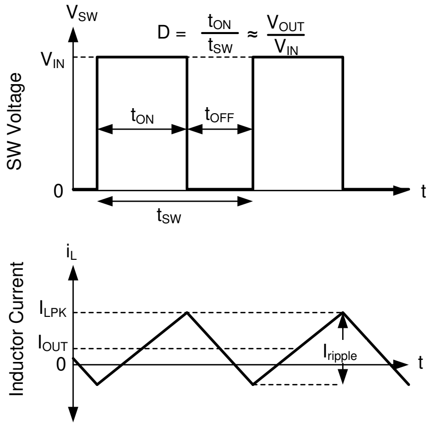
In auto mode, after output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

Figure 8-17. Steady State Output Voltage Versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM mode can be used to reduce or eliminate this offset.

8.4.3.3 FPWM Mode – Light-Load Operation

In FPWM mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see *Electrical Characteristics* for reverse current limit values.



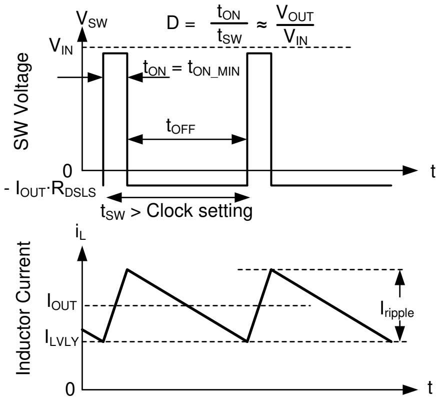
In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

Figure 8-18. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

8.4.3.4 Minimum On-Time (High Input Voltage) Operation

The LMR436x0 continues to regulate output voltage even if the input-to-output voltage ratio requires an on time less than the minimum on time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because on time is fixed at its minimum value, this type of operation resembles that of a device using a Constant On-Time (COT) control scheme; see Figure 8-19.

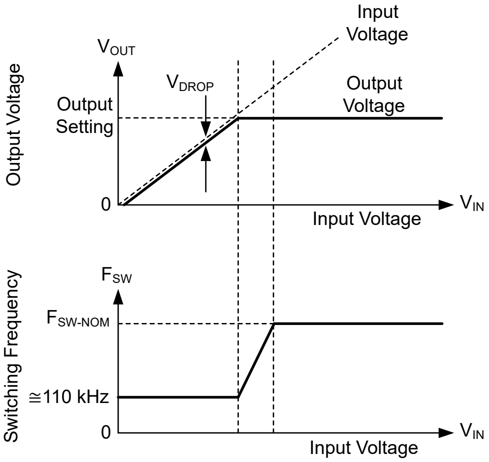


In valley control mode, minimum inductor current is regulated, not peak inductor current.

Figure 8-19. Valley Current Mode Operation

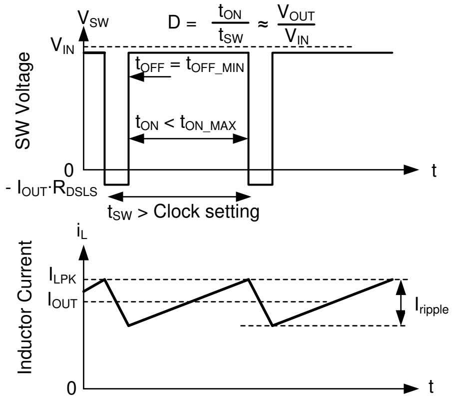
8.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off time. After this limit is reached as shown in Figure 8-21 if clock frequency was to be maintained, the output voltage falls. Instead of allowing the output voltage to drop, the LMR436x0 extends the high-side switch on time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a pre-determined maximum on time, $t_{ON\text{-}MAX}$, of approximately 9 µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off time, frequency drops to maintain regulation. As shown in Figure 8-20, if input voltage is low enough so that output voltage cannot be regulated even with an on time of $t_{ON\text{-}MAX}$, output voltage drops to slightly below the input voltage by V_{DROP}. For additional information on recovery from dropout, refer to Figure 8-11.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

Figure 8-20. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by $t_{ON\text{-}MAX}$.

Figure 8-21. Dropout Waveforms

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

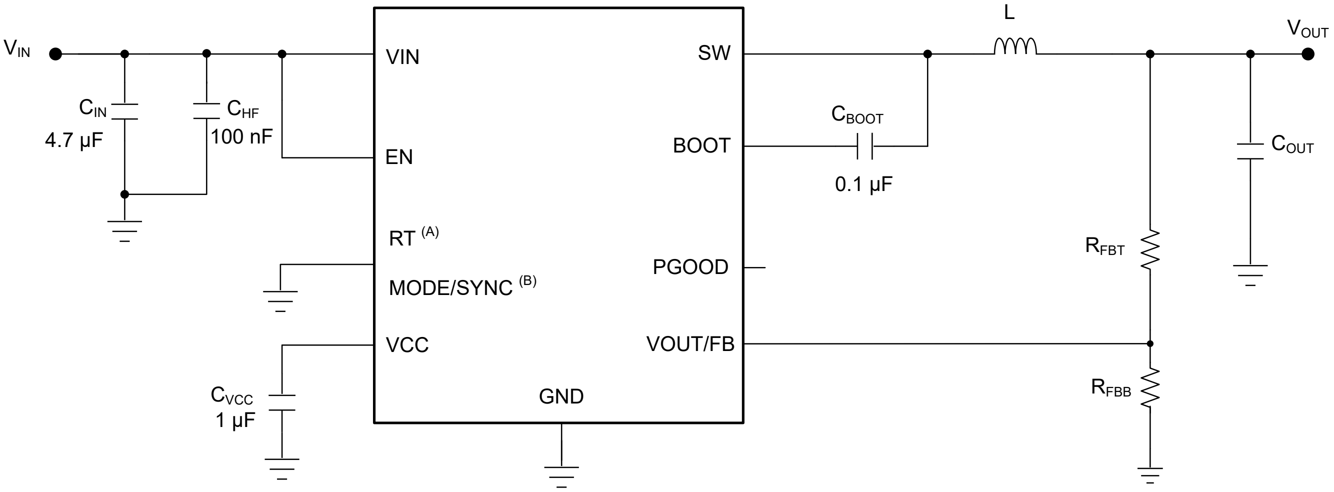
The LMR436x0 step-down DC-to-DC converters are typically used to convert a higher DC voltage to a lower DC voltage. LMR43620 supports a maximum output current of 2 A while the LMR43610 supports a maximum output current of 1 A. The following design procedure can be used to select components for the LMR43620. The design procedure can also be used to select components for the LMR43610 by limiting the maximum output current to 1 A.

Note

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

9.2 Typical Application

Figure 9-1 shows a typical application circuit for the LMR436x0. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick-start guide, Table 9-1 and Table 9-3 provide typical component values for a range of the most common output voltages.



A. The RT pin is factory-set for externally adjustable switching frequency RT variants only. Tying this pin to GND results in 2.2-MHz switching frequency. See Section 8.3.3 for details.

B. The MODE/SYNC pin is factory-set for fixed frequency frequency MODE/SYNC variants only. Tying this pin to GND results in AUTO mode. See Section 8.3.2 for details.

Figure 9-1. Example Application Circuit

Table 9-1. Typical External Component Values for Adjustable Output LMR43620

f_{SW} (kHz) (1)	V_{OUT} (V)	L (µH) (2)	NOMINAL C_{OUT} (RATED CAPACITANCE)	MINIMUM C_{OUT} (RATED CAPACITANCE)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{IN}	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3	10	3 × 22 µF	1 × 47 µF	33.2	14.3	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF
1000	3.3	4.7	2 × 22 µF	3 × 10 µF	33.2	14.3	2.2 µF + 1 × 100 nF	100 nF	1 µF	22 pF
2200	3.3	2.2	2 × 22 µF	1 × 22 µF	33.2	14.3	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF
400	5	10	3 × 22 µF	1 × 47 µF	49.9	12.4	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF
1000	5	4.7	2 × 22 µF	3 × 10 µF	49.9	12.4	2.2 µF + 1 × 100 nF	100 nF	1 µF	22 pF
2200	5	2.2	2 × 22 µF	1 × 22 µF	49.9	12.4	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF

(1) The switching frequencies listed here can be achieved in a number of ways depending on the device variant. For RT devices see Section 8.3.3. For MODE/SYNC devices see Section 8.3.2.

(2) Inductor values are calculated based on typical V_{IN} = 13.5 V.

Table 9-2. Typical External Component Values for Adjustable Output LMR43610

f_{SW} (kHz) (1)	V_{OUT} (V)	L (µH) (2)	NOMINAL C_{OUT} (RATED CAPACITANCE)	MINIMUM C_{OUT} (RATED CAPACITANCE)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{IN}	C_{BOOT}	C_{VCC}	C_{FF} (3)
400	3.3	22	2 × 22 µF	4 × 10 µF	33.2	14.3	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF
1000	3.3	8.2	1 × 22 µF	2 × 10 µF	33.2	14.3	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF

Table 9-2. Typical External Component Values for Adjustable Output LMR43610 (continued)

f_{SW} (kHz)[(1)]	V_{OUT} (V)	L (µH)[(2)]	NOMINAL C_{OUT} (RATED CAPACITANCE)	MINIMUM C_{OUT} (RATED CAPACITANCE)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{IN}	C_{BOOT}	C_{VCC}	C_{FF}[(3)]
2200	3.3	2.2	1 × 22 µF	2 × 10 µF	33.2	14.3	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF
400	5	22	2 × 22 µF	4 × 10 µF	49.9	12.4	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF
1000	5	4.7	1 × 22 µF	2 × 10 µF	49.9	12.4	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF
2200	5	2.2	1 × 22 µF	2 × 10 µF	49.9	12.4	4.7 µF + 1 × 100 nF	100 nF	1 µF	22 pF

(1) The switching frequencies listed here can be achieved in a number of ways depending on the device variant. For RT devices see Section 8.3.3. For MODE/SYNC devices see Section 8.3.2.
(2) Inductor values are calculated based on typical V_{IN} = 13.5 V.
(3) C_{FF} to be placed in parallel with R_{FBT}.

Table 9-3. Typical External Component Values for Fixed Output LMR43620

f_{SW} (kHz)[(1)]	V_{OUT} (V)	L (µH)[(2)]	NOMINAL C_{OUT} (RATED CAPACITANCE)	MINIMUM C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)[(3)]	C_{IN}	C_{BOOT}	C_{VCC}
400	3.3	10	3 × 22 µF	1 × 47 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF
1000	3.3	4.7	2 × 22 µF	3 × 10 µF	0	DNP	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	3.3	2.2	2 × 22 µF	1 × 22 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF
400	5	10	3 × 22 µF	1 × 47 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF
1000	5	4.7	2 × 22 µF	3 × 10 µF	0	DNP	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	5	2.2	2 × 22 µF	1 × 22 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF

(1) The switching frequencies listed here can be achieved in a number of ways depending on the device variant. For RT devices see Section 8.3.3. For MODE/SYNC devices see Section 8.3.2.
(2) Inductor values are calculated based on typical V_{IN} = 13.5 V.
(3) DNP = Do Not Populate.

Table 9-4. Typical External Component Values for Fixed Output LMR43610

f_{SW} (kHz)[(1)]	V_{OUT} (V)	L (µH)[(2)]	NOMINAL C_{OUT} (RATED CAPACITANCE)	MINIMUM C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)[(3)]	C_{IN}	C_{BOOT}	C_{VCC}
400	3.3	22	2 × 22 µF	4 × 10 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF
1000	3.3	4.7	1 × 22 µF	2 × 10 µF	0	DNP	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	3.3	2.2	1 × 22 µF	2 × 10 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF
400	5	22	2 × 22 µF	4 × 10 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF
1000	5	4.7	1 × 22 µF	2 × 10 µF	0	DNP	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	5	2.2	1 × 22 µF	2 × 10 µF	0	DNP	4.7 µF + 1 × 100 nF	100 nF	1 µF

(1) The switching frequencies listed here can be achieved in a number of ways depending on the device variant. For RT devices see Section 8.3.3. For MODE/SYNC devices see Section 8.3.2.
(2) Inductor values are calculated based on typical V_{IN} = 13.5 V.
(3) DNP = Do Not Populate.

9.2.1 Design Requirements

Section 9.2.2 provides a detailed design procedure based on Table 9-5.

Table 9-5. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 2 A
Switching frequency	1000 kHz

9.2.2 Detailed Design Procedure

The following design procedure applies to Figure 9-1 and Table 9-3.

9.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 1000 kHz is used.

9.2.2.2 Setting the Output Voltage

The VOUT/FB pin of the device can be either connected directly to the output capacitor or the mid point of a feedback resistor divider. When connected directly to the output capacitor, the device operates as a fixed output option. The 3.3-V or 5-V fixed output options are factory trimmed and are unique to a specific device. See Section 5 for the selection of fixed output voltage versions.

9.2.2.2.1 FB for Adjustable Output

If other voltages are desired, the VOUT/FB pin can be connected to a feedback resistor divider network to set the output voltage. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The converter determines whether fixed output voltage or adjustable output voltage is required by sensing the resistance of the feedback path during start-up. To ensure that the converter regulates to the desired output voltage, the typical minimum value for the parallel combination of R_{FBT} and R_{FBB} is 5 kΩ while the typical maximum value is 10 kΩ as shown in Equation 5. Equation 6 can be used as a starting point to determine the value of R_{FBT}. Reference Table 9-6 for a list of acceptable resistor values for various output voltages.

$$5\ k\Omega\ <\ R_{FBT}||R_{FBB}\ \leq 10\ k\Omega \tag{5}$$

$$R_{FBT} \leq 10\ k\Omega \times \frac{V_{OUT}}{1\ V} \tag{6}$$

Table 9-6. Recommended Feedback Resistor Values for Various Output Voltages

V_{OUT} (V)	R_{FBT} (1) (kΩ)	R_{FBB} (kΩ)
2.5	24.9	16.5
3.3	33.2	14.3
5	49.9	12.4
6	60.4	12.1
9	90.9	11.3

(1) R_{FBT} and R_{FBB} based on 1% standard resistor values.

For this 5-V example, the user can choose the *LMR43620MB5RPER* and connect the VOUT/FB pin directly to the output capacitor.

9.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. Equation 7 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, choose K = 0.4 and find an inductance of L = 3.64 µH. Select the standard value of 3.3 µH. It is important to note that the inductor values presented in Table 9-1 and Table 9-3 were calculated using K= 0.3.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} \tag{7}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, $I_{PEAKMAX}$ (see Section 7.5). This ensures that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{VALMAX}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

9.2.2.4 Output Capacitor Selection

The current mode control scheme of the LMR436x0 devices allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. Refer to Table 9-1 for typical output capacitor value for 3.3-V and 5-V output voltages. Based on Table 9-1, for a 3.3-V 5-V output design, you can choose the recommended 2 × 22-µF ceramic output capacitor for this example. For other designs with other output voltages, WEBENCH can be used as a starting point for selecting the value of output capacitor.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic capacitor placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 4.7 µF is required on the input of the LMR436x0. This must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100-nF ceramic capacitor must be used at the input, as close a possible to the regulator. In the case of the LMR43620R5EVM-1M this capacitor is placed approximately 0.38-mm away from the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example, a 4.7-µF, 50-V, X7R (or better) ceramic capacitor is chosen. The 100 nF must also be rated at 50 V with an X7R dielectric.

It is often desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from Equation 8 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{8}$$

9.2.2.6 C_{BOOT}

The LMR436x0 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

9.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see Section 8.3.4). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3 V; see *Electrical Characteristics* for limits.

9.2.2.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

Due to the nature of the feedback detect circuitry, the value of C_{FF} must be limited to ensure that the desired output voltage is established when configuring for adjustable output voltages. Equation 9 must be followed to ensure C_{FF} remians below the maximum value.

$$C_{FF} < C_{OUT} \times \frac{\sqrt{V_{OUT}}}{1.2\ M\Omega} \tag{9}$$

9.2.2.8.1 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in Figure 9-2. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then Equation 10 and Equation 11 are used to calculate R_{ENT} and V_{OFF} respectively.

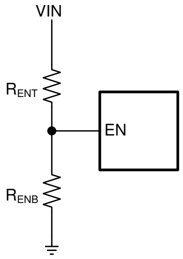


Figure 9-2. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-VOUT}} - 1 \right) \times R_{ENB} \quad (10)$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN-HYS}}{V_{EN-VOUT}} \right) \quad (11)$$

where

- V_{ON} is the V_{IN} turn-on voltage.
- V_{OFF} is the V_{IN} turn-off voltage.

9.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the LMR436x0 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{θJA}$, of the device, and PCB combination. The maximum junction temperature for the LMR436x0 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 12 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{θJA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{θJA}$ is more difficult to estimate. For more information reference *Semiconductor and IC Package Thermal Metrics Application Report*.

$$I_{OUT}\Big|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \quad (12)$$

where

- η is the efficiency.

The effective $R_{θJA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The IC junction temperature can be estimated for a given operating condition using Equation 13.

$$T_J \cong T_A + R_{\theta JA} \times IC\ Power\ Loss \quad (13)$$

where

- T_J is the IC junction temperature (ºC).
- T_A is the ambient temperature (ºC).
- $R_{θJA}$ is the thermal resistance (ºC/W).
- IC power loss is the power loss for the IC (W).

The IC Power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC resistance. The overall power loss can be approximated by using WEBENCH for a specific operating condition and temperature.

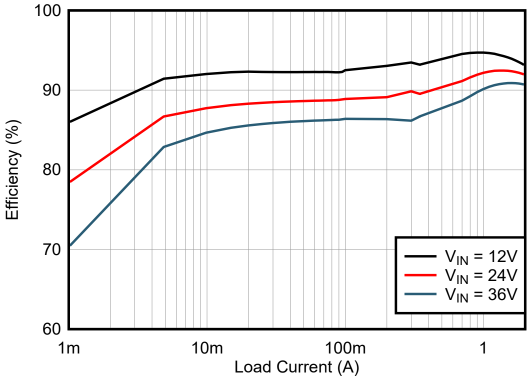
Use the following resources as guides to optimal thermal PCB design and estimating $R_{θJA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*

- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD™ Thermally Enhanced Package Application Report*
- *PowerPAD™ Made Easy Application Report*
- *Using New Thermal Metrics Application Report*
- *PCB Thermal Calculator*

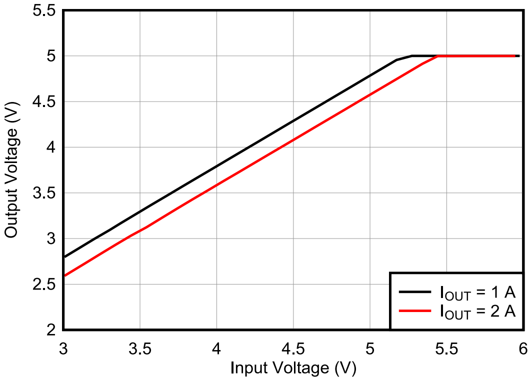
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, T_A = 25°C.



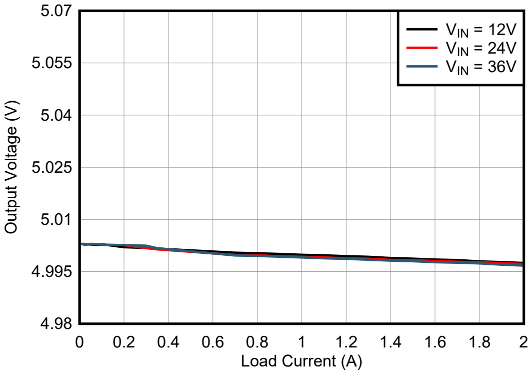
LMR43620MB5 Fixed V_{OUT} = 5 V f_{SW} = 1 MHz (auto)

Figure 9-3. Efficiency



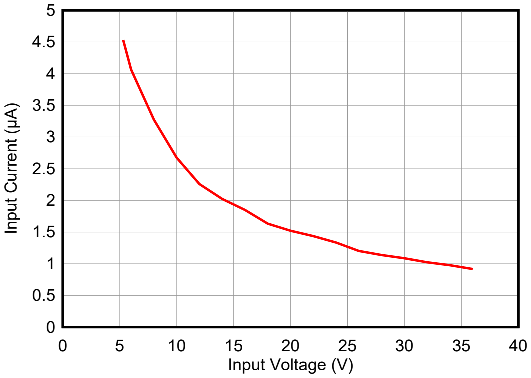
LMR43620MB5 Fixed V_{OUT} = 5 V f_{SW} = 1 MHz (auto)

Figure 9-4. Dropout



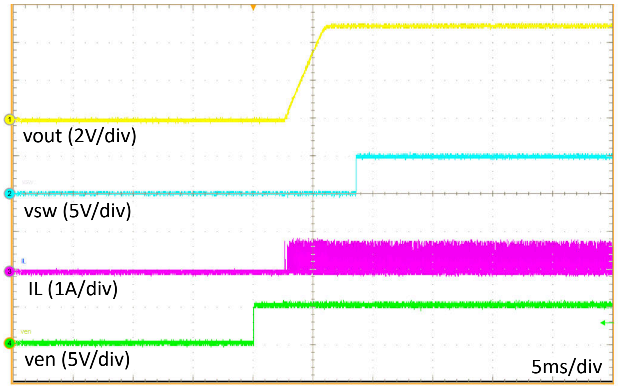
LMR43620MB5 Fixed V_{OUT} = 5 V f_{SW} = 1 MHz (auto)

Figure 9-5. Line and Load Regulation



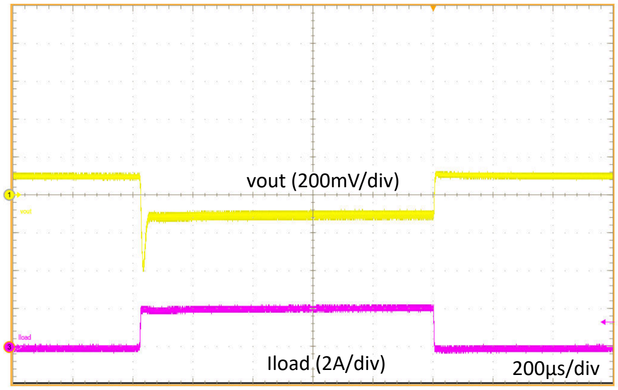
LMR43620MB5 Fixed V_{OUT} = 5 V f_{SW} = 1 MHz (auto)

Figure 9-6. Input Switching Current vs Input Voltage



LMR43620MB5 Fixed V_{OUT} = 5 V f_{SW} = 1 MHz (auto) I_{OUT} = 100 mA

Figure 9-7. Start-up

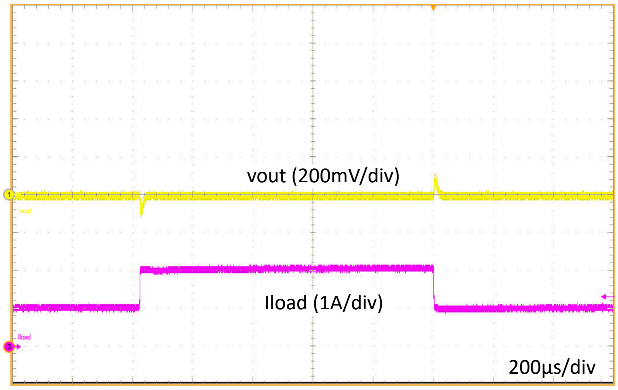


LMR43620MB5 Fixed V_{OUT} = 5 V f_{SW} = 1 MHz (auto) I_{OUT} = 0 A to 2 A,1 A/µs

Figure 9-8. Load Transient

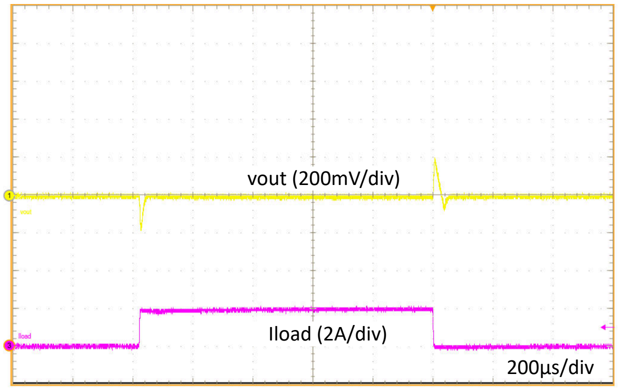
9.2.3 Application Curves (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, T_A = 25°C.



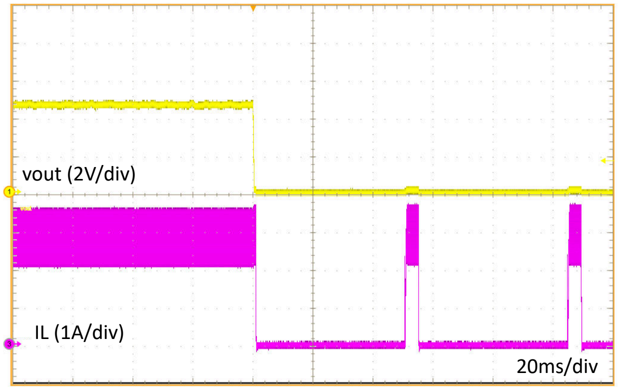
LMR43620MB5 Fixed
V_{OUT} = 5 V
f_{SW} = 1 MHz (auto)
I_{OUT} = 1 A to 2 A,1 A/µs

Figure 9-9. Load Transient



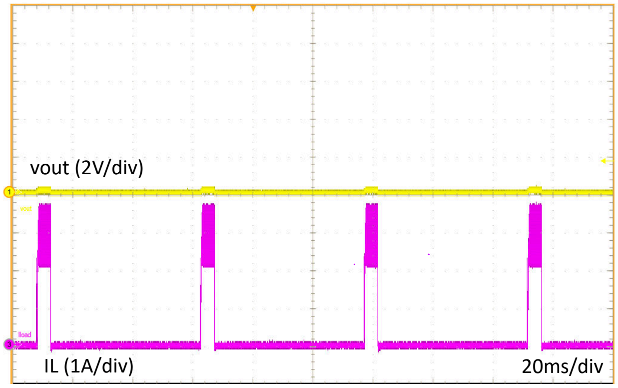
LMR43620MB5 Fixed
V_{OUT} = 5 V
f_{SW} = 1 MHz (FPWM)
I_{OUT} = 0 A to 2 A,1 A/µs

Figure 9-10. Load Transient



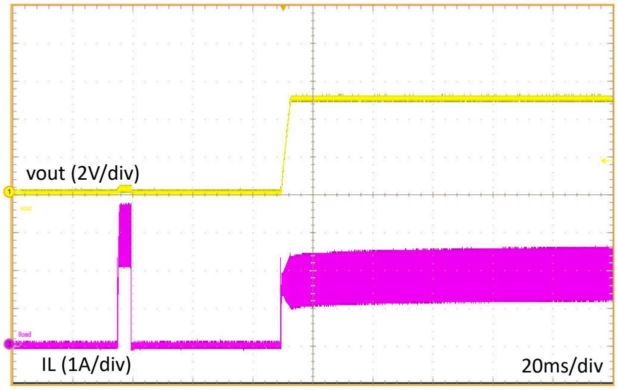
LMR43620MB5 Fixed
V_{OUT} = 5 V
V_{IN} = 24 V
auto mode
I_{OUT} = 2 A to Short Circuit

Figure 9-11. Short-Circuit Protection



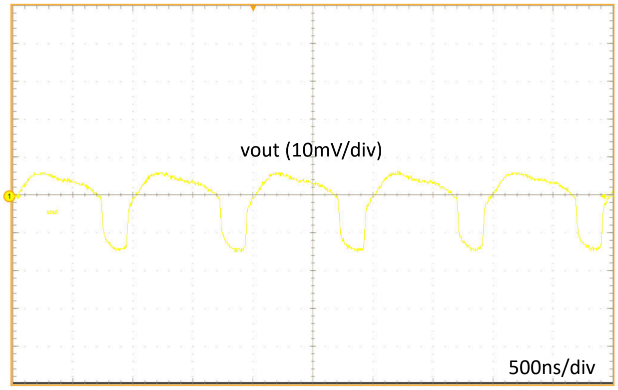
LMR43620MB5 Fixed
V_{OUT} = 5 V
V_{IN} = 24 V
auto mode
I_{OUT} = Short Circuit

Figure 9-12. Short-Circuit Performance



LMR43620MB5 Fixed
V_{OUT} = 5 V
V_{IN} = 24 V
auto mode
I_{OUT} = Short Circuit to 2 A

Figure 9-13. Short-Circuit Recovery

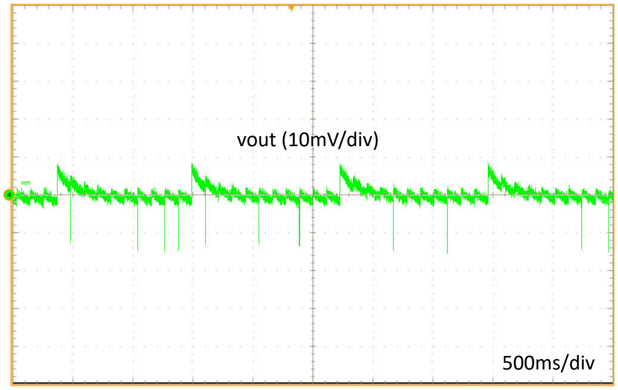


LMR43620MB5 Fixed
V_{OUT} = 5 V
V_{IN} = 24 V
f_{SW} = 1 MHz (auto)
I_{OUT} = 2 A

Figure 9-14. Output Voltage Ripple

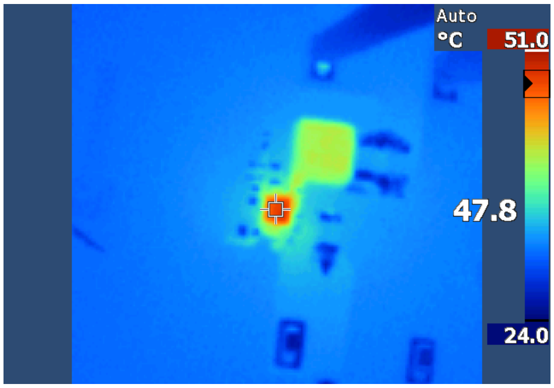
9.2.3 Application Curves (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, T_A = 25°C.



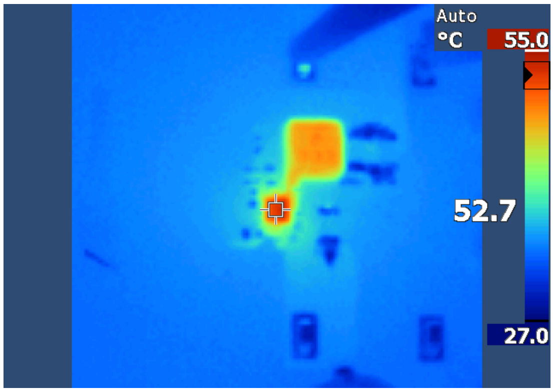
LMR43620MB5 V_{OUT} = 5 V f_{SW} = 1 MHz (auto)
Fixed V_{IN} = 24 V I_{OUT} = Open

Figure 9-15. Output Voltage Ripple



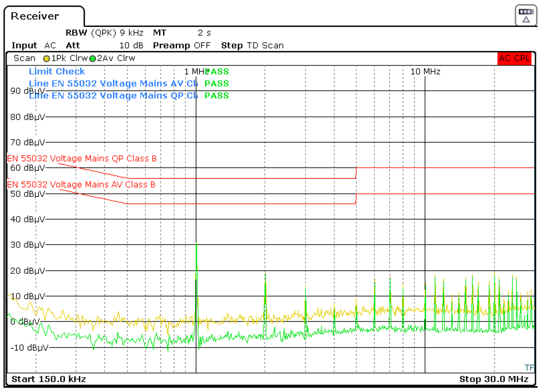
LMR43620MB5 V_{OUT} = 5 V f_{SW} = 1 MHz
Fixed V_{IN} = 12 V I_{OUT} = 2 A

Figure 9-16. EVM Thermal Performance



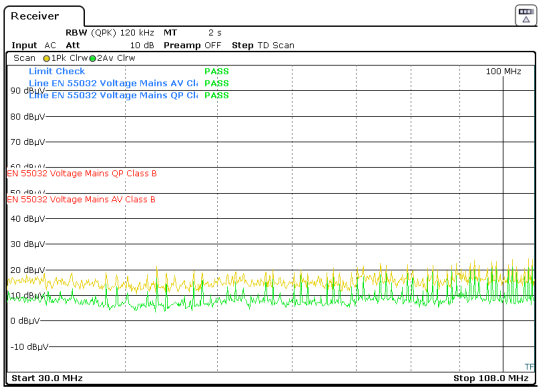
LMR43620MB5 V_{OUT} = 5 V f_{SW} = 1 MHz
Fixed V_{IN} = 24 V I_{OUT} = 2 A

Figure 9-17. EVM Thermal Performance



LMR43620MB5 V_{OUT} = 5 V f_{SW} = 1 MHz
Fixed V_{IN} = 24 V I_{OUT} = 2 A

Figure 9-18. Typical CISPR 32 Conducted EMI 150 kHz – 30 MHz Yellow: Peak Detect, Green = Average Detect



LMR43620MB5 V_{OUT} = 5 V f_{SW} = 1 MHz
Fixed V_{IN} = 24 V I_{OUT} = 2 A

Figure 9-19. Typical CISPR 32 Conducted EMI 30 MHz – 108 MHz Yellow: Peak Detect, Green = Average Detect

9.2.3 Application Curves (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, T_A = 25°C.

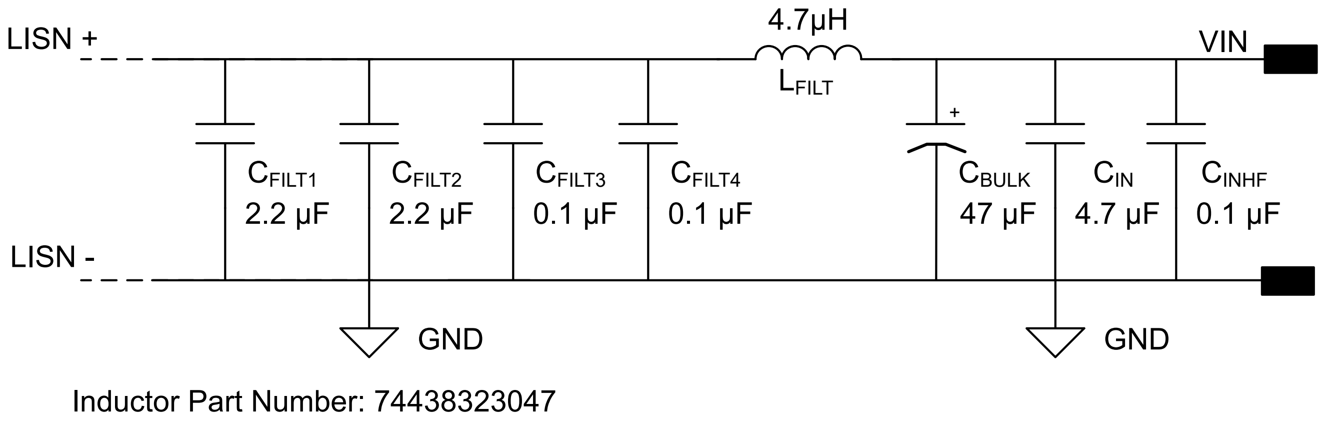
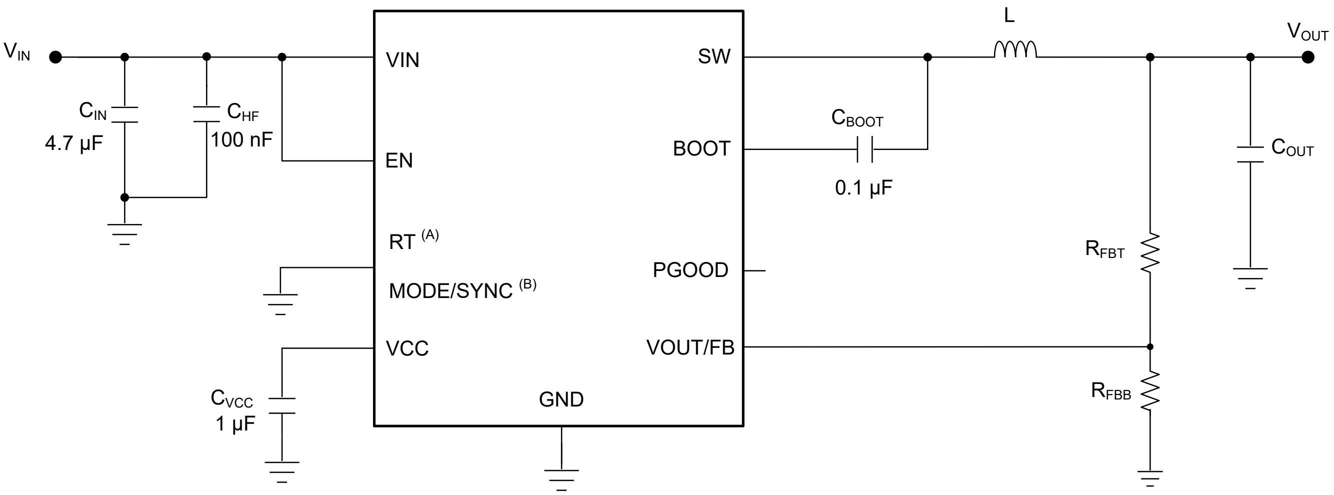


Figure 9-20. Typical Input EMI Filter



A. The RT pin is factory-set for externally adjustable switching frequency RT variants only. Tying this pin to VCC results in 1-MHz switching frequency. See Section 8.3.3 for details.

B. The MODE/SYNC pin is factory-set for fixed frequency MODE/SYNC variants only. Tying this pin to GND results in auto mode. See Section 8.3.2 for details.

Figure 9-21. Example Application Circuit

Table 9-7. BOM for Typical Application Curves

U1	f_{SW}	V_{OUT}	L	NOMINAL C_{OUT} (RATED CAPACITANCE)	RFBT	RFBB	CFF
LMR43620MB5RPER	1000 kHz	5 V Fixed	3.3 µH, 26 mΩ	2 × 22 µF	0 Ω	DNP	DNP

9.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.

9.4 Power Supply Recommendations

The characteristics of the input supply must be compatible with Section 7 found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 14.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{14}$$

where

- η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kind of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). TI does not recommend the use of a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

9.5 Layout

9.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in Figure 9-22. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 9-23 shows a recommended layout for the critical components of the LMR436x0.

- *Place the input capacitors as close as possible to the VIN and GND terminals.*
- *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
- *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins.
- *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
- *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- *Provide enough PCB area for proper heat-sinking.* As stated in Section 9.2.2.9, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
- *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

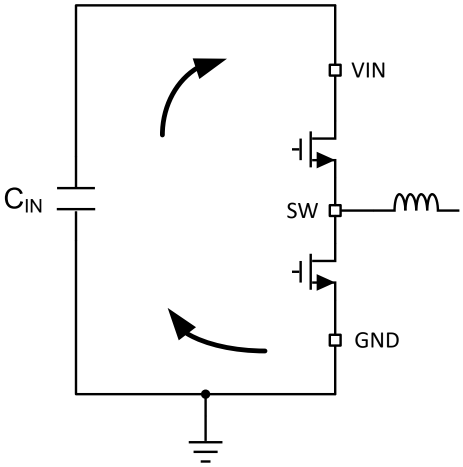


Figure 9-22. Current Loops with Fast Edges

9.5.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See Figure 9-23 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

9.5.2 Layout Example

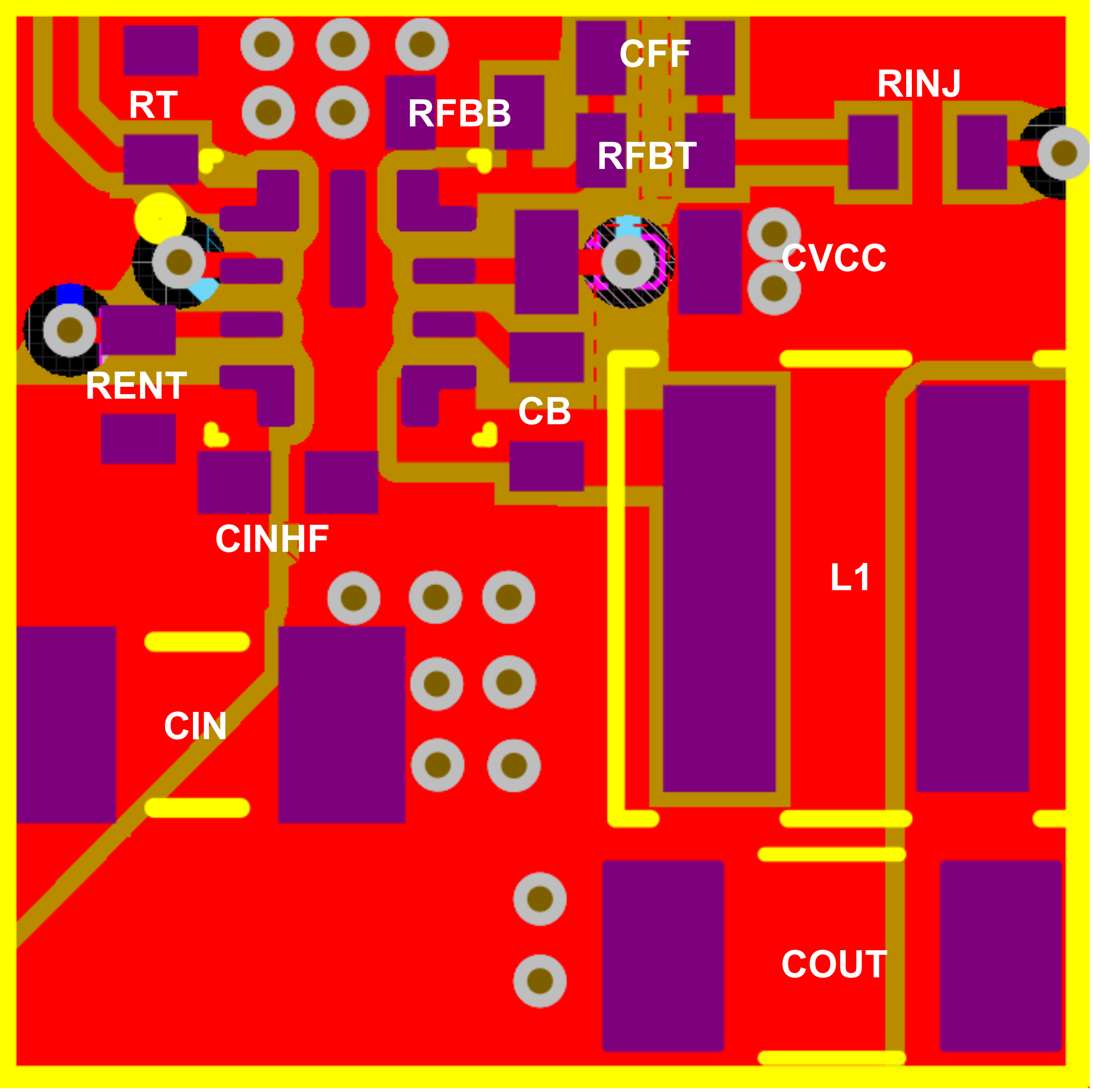


Figure 9-23. Example Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

10.1.2 Device Nomenclature

The following figure shows the device naming nomenclature of the LMR436x0-Q1. See Section 5 for the availability of each variant. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

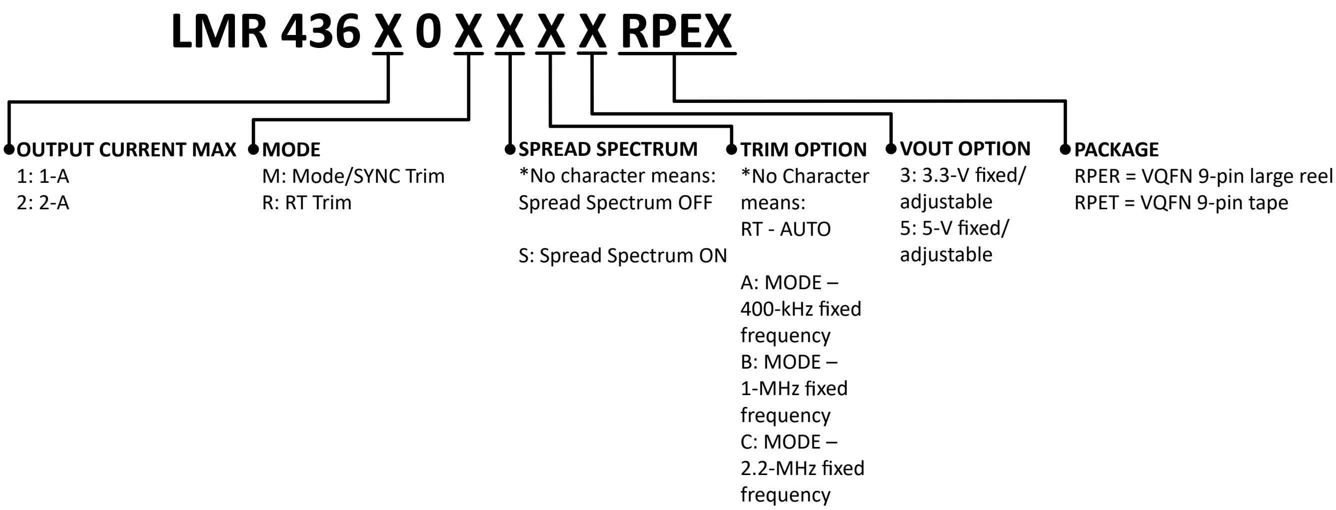


Figure 10-1. Device Naming Nomenclature

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight Application Report*
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package Application Report*
- Texas Instruments, *PowerPAD™ Made Easy Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies Application Report*
- Texas Instruments, *Simple Switcher PCB Layout Guidelines Application Report*
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR43610MB3RPER	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	1MB3
LMR43610MB3RPER.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	1MB3
LMR43610R3RPER	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	1R3
LMR43610R3RPER.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	1R3
LMR43620MB5RPER	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	2MB5
LMR43620MB5RPER.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	2MB5
LMR43620R5RPER	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	2R5
LMR43620R5RPER.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	2R5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

OTHER QUALIFIED VERSIONS OF LMR43610, LMR43620 :

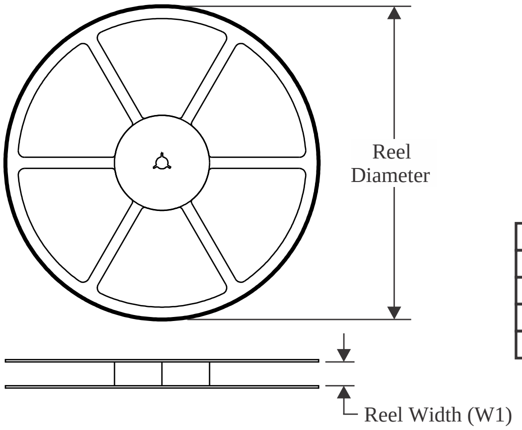
- Automotive : LMR43610-Q1, LMR43620-Q1

NOTE: Qualified Version Definitions:

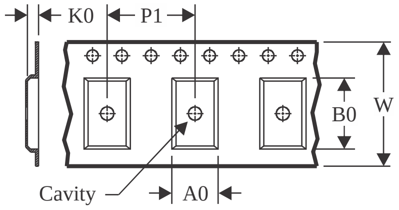
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

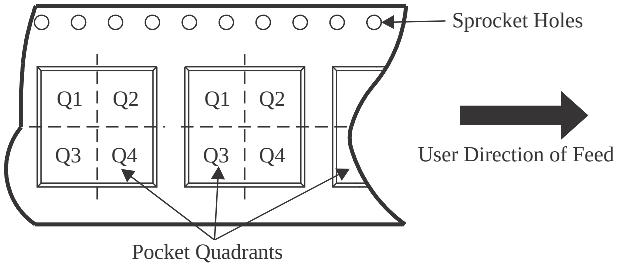


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

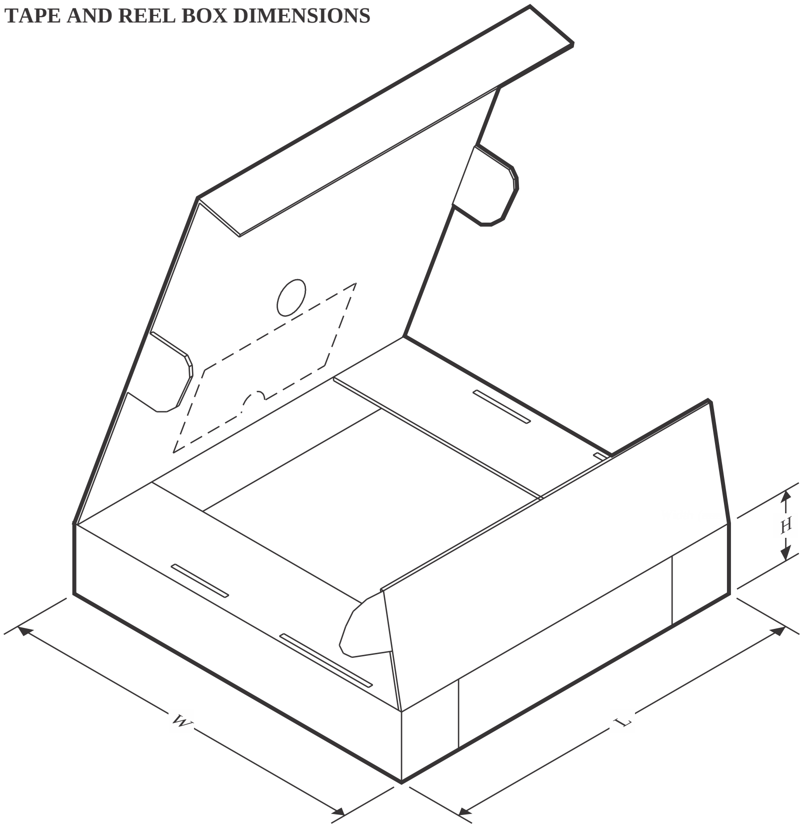
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR43610MB3RPER	VQFN-HR	RPE	9	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LMR43610R3RPER	VQFN-HR	RPE	9	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LMR43620MB5RPER	VQFN-HR	RPE	9	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LMR43620R5RPER	VQFN-HR	RPE	9	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR43610MB3RPER	VQFN-HR	RPE	9	3000	210.0	185.0	35.0
LMR43610R3RPER	VQFN-HR	RPE	9	3000	210.0	185.0	35.0
LMR43620MB5RPER	VQFN-HR	RPE	9	3000	210.0	185.0	35.0
LMR43620R5RPER	VQFN-HR	RPE	9	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

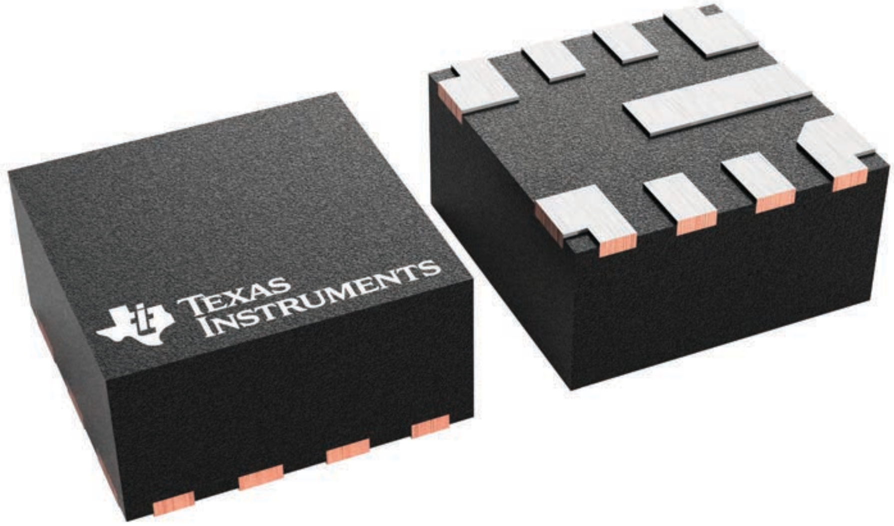
RPE 9

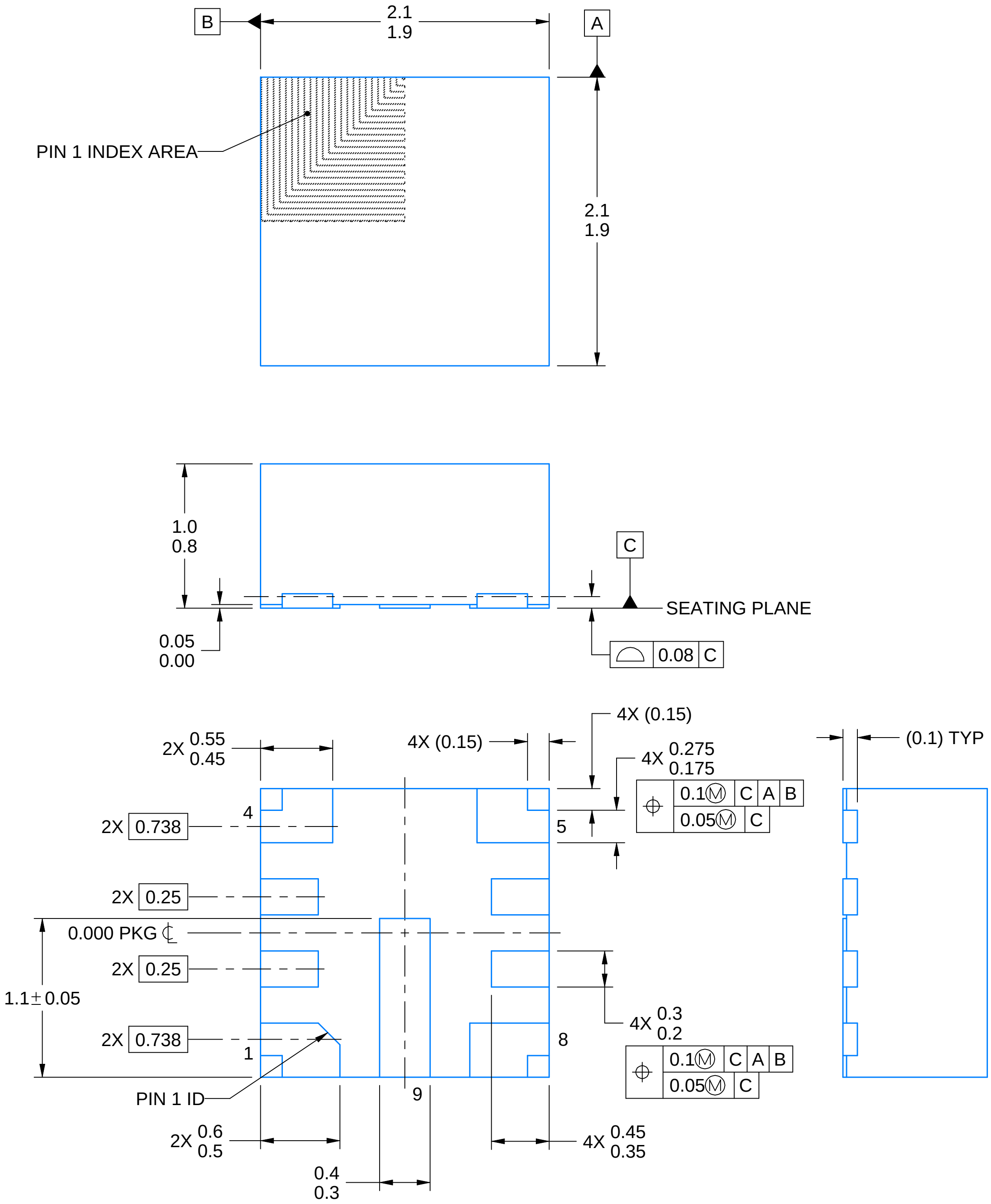
VQFN-HR - 1.0 mm max height

2 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

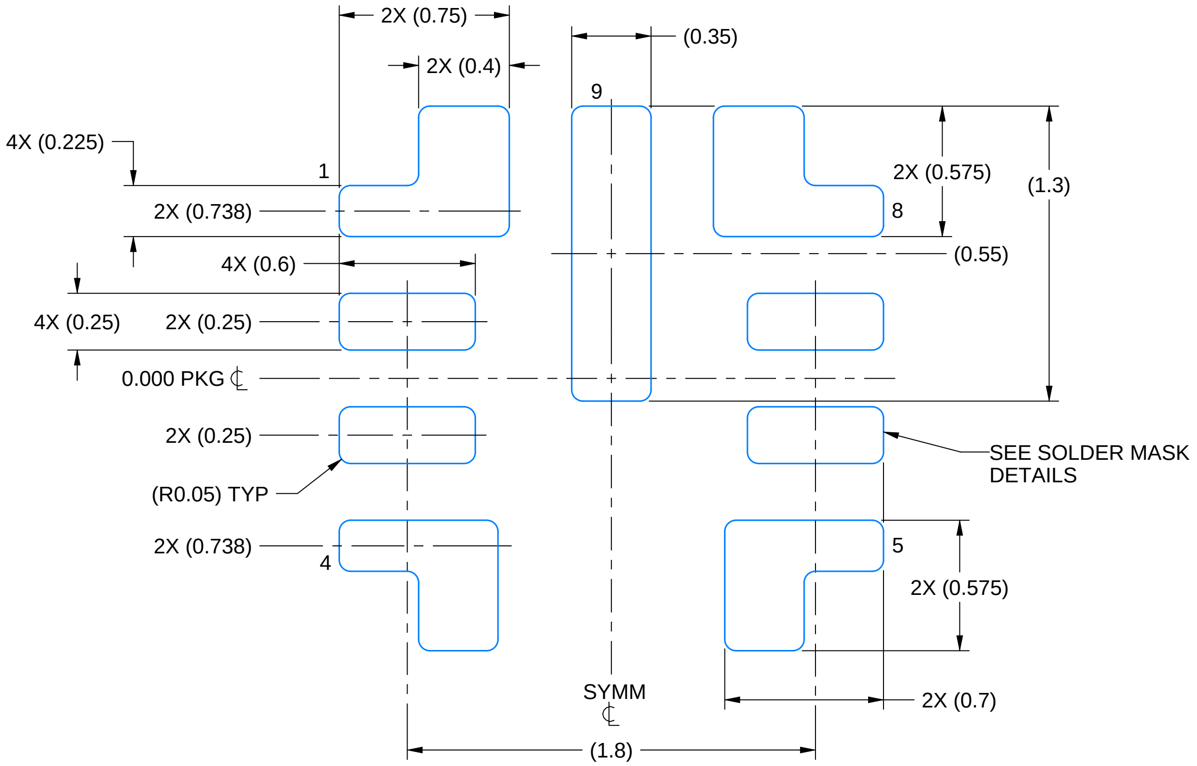




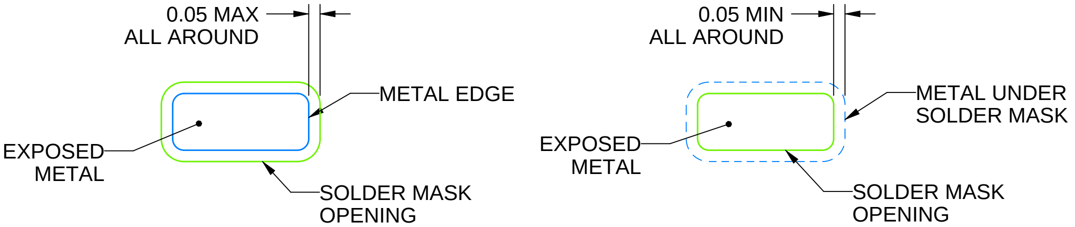
4227033/B 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



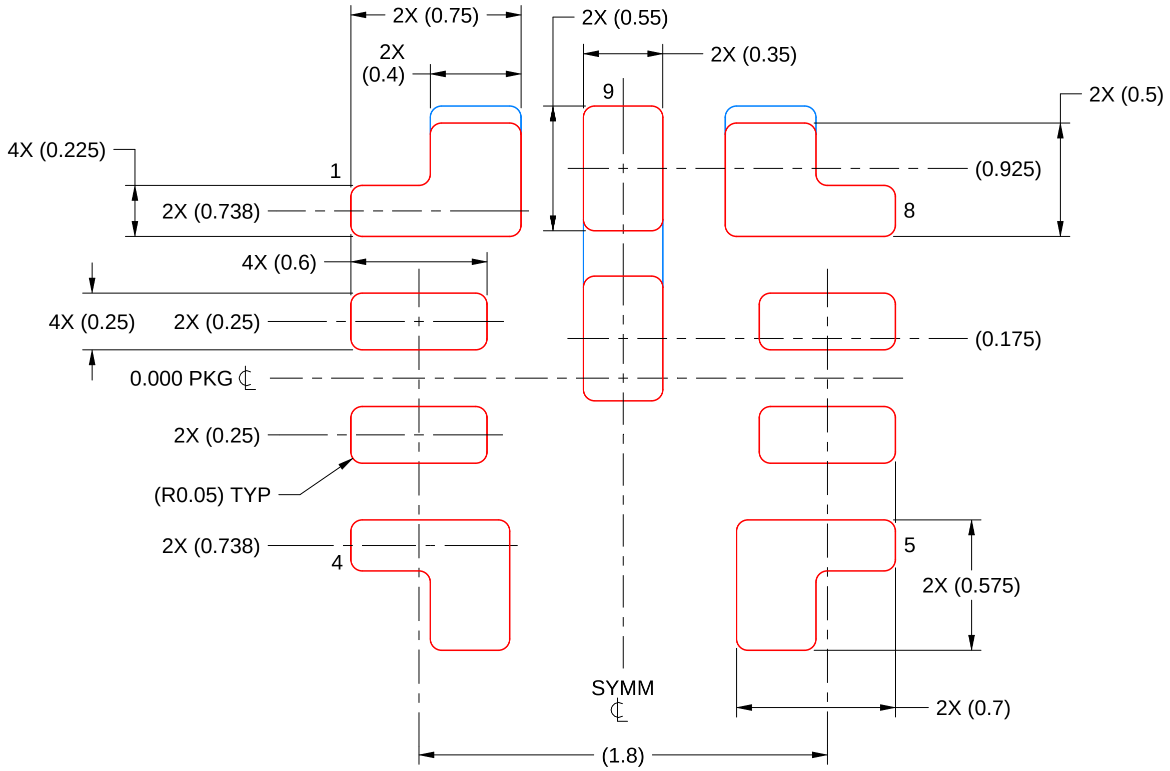
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PADS 1 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 9:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

DWG_NO:5/REV:5   MM_YYYY:5

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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