LMR719xx 1.5A, 0.75A, 115V, Step-Down Converter With Fly-Buck™ Converter Capability

ADVANCE INFORMATION

1 Features

- Designed for reliability in rugged applications
  - Wide input voltage range of 6V to 115V
  - Junction temperature range: –40°C to +150°C
  - Fixed 3ms internal soft-start timer
  - Peak and valley current-limit protection
  - Input UVLO and thermal shutdown protection
- Designed for scalable industrial power supplies and battery packs
  - Low minimum on time of 30ns and minimum off time of 50ns
  - Adjustable switching frequency up to 1MHz
  - Diode emulation for high light-load efficiency
  - Auto mode with low quiescent current (5µA typical)
  - FPWM for Fly-Buck converter capability
  - 1µA shutdown quiescent current
  - Pin-to-pin compatible with LM5169, LM5168, LM5164, LM5163, and LM5013
  - Similar pinout and functionality to LM5017 and LM34927
- Integration reduces design size and cost
  - COT mode control architecture
  - Integrated 0.7Ω NFET buck switch
  - Integrated 0.35Ω NFET synchronous rectifier
  - 1V internal voltage reference
  - No loop compensation components
  - Internal V_{CC} bias regulator and boot diode
  - Open-drain power-good indicator
  - SOIC PowerPAD™-8 integrated circuit package

2 Applications

- Communications – brick power module
- Motor drives, drones
- Industrial battery pack (≥ 10S)
- Battery pack – e-bike, e-scooter, LEV

3 Description

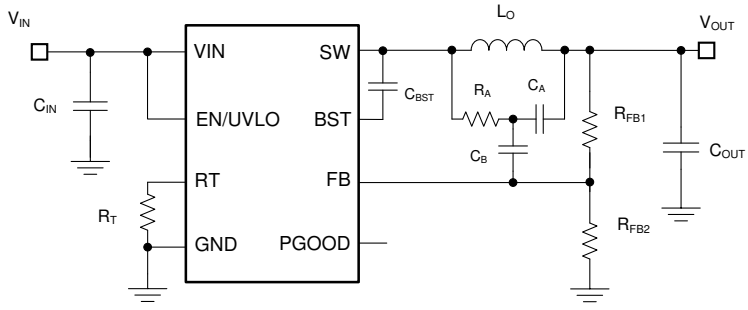
The LMR71915 and LMR71907 synchronous buck converters are designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on time of 30ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48V nominal input to low-voltage rails for reduced system complexity and design cost. The LMR719xx operates during input voltage dips as low as 6V, at nearly 100% duty cycle if needed, making the device an excellent choice for wide input supply range industrial and high cell count battery pack applications.

With integrated high-side and low-side power MOSFETs, the LMR71915 delivers up to 1.5A of output current and the LMR71907 delivers up to 0.75A of output current. A constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. The LMR719xx is available in FPWM or auto mode versions. FPWM mode provides forced CCM operation across the entire load range supporting isolated Fly-Buck converter applications. Auto mode enables ultra-low I_Q and diode emulation mode operation for high light-load efficiency.

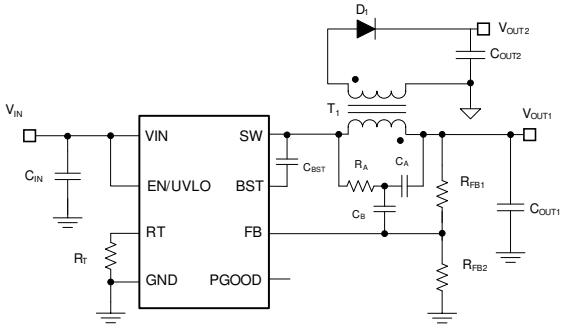
Device Information

PART NUMBER(2)	OUTPUT CURRENT	PACKAGE(1)
LMR71915	1.5A	DDA (HSOIC, 8)
LMR71907(3)	0.75A	

(1) For more information, see Section 11.
(2) See the *Device Comparison Table*.
(3) Product preview (not Advance Information).



Typical Buck Application Circuit



Typical Fly-Buck™ Converter Application Circuit

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4 Device Comparison Table

DEVICE NUMBER	PACKAGE	DESCRIPTION	OUTPUT CURRENT	LIGHT LOAD MODE	CURRENT LIMIT
LMR71907PDDAR(1)	DDA (HSOIC, 8)	0.75A, buck, AUTO, no hiccup	0.75A	PFM	1.1A, no hiccup
LMR71907FDDAR(1)		0.75A, buck/Fly-Buck, FPWM, hiccup		FPWM	1.1A, hiccup
LMR71915PDDAR(1)		1.5A, buck, AUTO, no hiccup	1.5A	PFM	2.2A, no hiccup
LMR71915FDDAR		1.5A, buck/Fly-Buck, FPWM, hiccup		FPWM	2.2A, hiccup

(1) Product preview (not Advance Information)

5 Pin Configuration and Functions

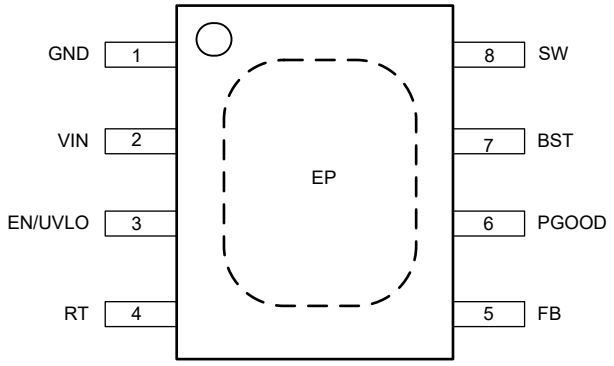

Figure 5-1. 8-Pin SO PowerPAD™ Integrated Circuit Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GND	G	Ground connection for internal circuits
2	VIN	P/I	Regulator supply input pin to the high-side power MOSFET and internal bias regulator. Connect directly to the input supply of the buck converter with short, low impedance paths.
3	EN/UVLO	I	Precision enable and undervoltage lockout (UVLO) programming pin. If the EN/UVLO rising voltage is below 1.1V, the converter is in shutdown mode with all functions disabled. If the UVLO voltage is greater than 1.1V and below 1.5V, the converter is in standby mode with the internal VCC regulator operational and no switching. If the EN/UVLO voltage is above 1.5V, the start-up sequence begins.
4	RT	I	On-time programming pin. A resistor between this pin and GND sets the buck switch on time.
5	FB	I	Feedback input of voltage regulation comparator
6	PGOOD	O	Power-good indicator. This pin is an open-drain output pin. Connect to a source voltage through an external pullup resistor between 10kΩ to 100kΩ. Connect to GND if the PGOOD feature is not needed.
7	BST	P/I	Bootstrap gate-drive supply. Required to connect a high-quality 2.2nF X7R ceramic capacitor between BST and SW to bias the internal high-side gate driver.
8	SW	P	Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching node of the power inductor.
—	EP	—	Exposed pad of the package. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	120	V
	SW, DC	–1.5	120	
	SW, transient <20ns	–3		
	BST	–0.3	125.5	
	BST – SW	–0.3	5.5	
	EN	–0.3	120	
	FB	–0.3	3	
	RT	–0.3	3	
	PGOOD	–0.3	14	
Operating junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Pin voltage	VIN	6		115	V
V_{EN}	Pin voltage	EN			115	V
I_{OUT}	Output current range	LMR71915		1.5		A
		LMR71907		0.75		A
C_{BST}	External BST to SW capacitance	FPWM Mode		2.2		nF
F_{SW}	Switching frequency		100		1000	kHz

6.4 Thermal Information

THERMAL METRIC(1)		LMR719xx DDA (SOIC) 8 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		LMR719xx DDA (SOIC) 8 PINs	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note

6.5 Electrical Characteristics

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	V_{EN} = 2.5V, PWM operation		360	600	µA
		V_{EN} = 2.5V, PFM operation		5	25	µA
$I_{Q(STANDBY)}$	VIN standby current - LDO only	V_{EN} = 1.25V		8	35	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0V, V_{IN} = 24V, Tj = 25°C		0.7	2	µA
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.45	1.5	1.55	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	1.35	1.4	1.44	V
$V_{SD(R)}$	EN standby rising threshold	EN rising, enable internal LDO, no switching.			1.1	V
$V_{SD(F)}$	EN standby falling threshold	EN falling, disable internal LDO.	0.45			V
REFERENCE VOLTAGE						
V_{FB}	FB voltage	V_{FB} falling	0.985	1	1.015	V
START-UP						
t_{SS}	Internal fixed soft-start time		1.75	3	4.75	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	I_{SW} = –100mA		0.7		Ω
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	I_{SW} = 100mA		0.35		Ω
$t_{ON(min)}$	Minimum ON pulse width	V_{VIN} = 115V, R_{RT} = 8.625kΩ		30		ns
$t_{ON(3)}$	On-time3	V_{VIN} = 12V, R_{RT} = 75kΩ		2550		ns
$t_{ON(4)}$	On-time4	V_{VIN} = 12V, R_{RT} = 25kΩ		830		ns
$t_{ON(4)}$	On-time48_1	V_{VIN} = 48V, R_{RT} = 75kΩ		625		ns
$t_{ON(4)}$	On-time48_2	V_{VIN} = 48V, R_{RT} = 25kΩ		208		ns
$t_{OFF(min)}$	Minimum OFF pulse width			50		ns
BOOT CIRCUIT						
$V_{BOOT-SW(UV\_R)}$	BOOT-SW UVLO rising threshold	$V_{BOOT-SW}$ rising		2.9	3.4	V
OVERCURRENT PROTECTION						
$I_{HS\_PK(OC)}$	High-side and low-side peak current limit	LMR71907	0.935	1.1	1.265	A
$I_{HS\_PK(OC)}$	High-side and low-side peak current limit	LMR71915	1.87	2.2	2.53	A
$I_{LS\_V(OC)}$	Low-side valley current limit	LMR71907	0.667	0.785	0.903	A
$I_{LS\_V(OC)}$	Low-side valley current limit	LMR71915	1.335	1.57	1.805	A
$I_{LS(NOC)}$	Low-side negative current limit	LMR71907	1.12	1.6	2.08	A
$I_{LS(NOC)}$	Low-side negative current limit	LMR71915	2.24	3.2	4.16	A
I_{ZC}	Zero-cross detection current threshold			0		A
T_W	Hiccup time before re-start			192		ms
POWER GOOD						
V_{PGTH}	Power-Good threshold	FB falling, PG high to low	0.882	0.9	0.918	V
		FB rising, PG low to high	0.921	0.95	0.979	V
R_{PG}	Power-Good threshold	VFB = 1V		10		Ω

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising		175		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			10		°C

(1) Specified by design, not product tested

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7 Detailed Description

7.1 Overview

LMR718xx are easy-to-use, ultra-low I_Q, constant on-time (COT), synchronous step-down buck regulators. With integrated high-side and low-side power MOSFETs, the LMR719xx is a low-cost, highly-efficient buck converter that operates from a wide input voltage of 6V to 115V, delivering up to 1.5A or 0.75A DC load current. The LMR719xx is available in an 8-pin, SO PowerPAD integrated circuit package with 1.27mm pin pitch for adequate spacing in high-voltage applications. This constant on-time (COT) converter is ideal for low-noise, high-current, and fast load transient requirements, operating with a predictive on-time switching pulse. Over the input voltage range, input voltage feed-forward is employed to achieve a quasi-fixed switching frequency. A controllable on time as low as 30ns permits high step-down ratios and a minimum forced off time of 50ns provides extremely high duty cycles. This action enables fixed frequency operation as VIN drops close to VOUT. After the forced off time of 50ns is reached, the device enters frequency fold-back operation to maintain a constant output voltage. The LMR719xx implements a smart peak and valley current limit detection circuit to ensure robust protection during output short circuit conditions. Control loop compensation is not required for this regulator, reducing design time and external component count.

LMR718xx are pre-programmed to operate in auto mode or FPWM mode. When configured to operate in auto mode, at light loads, the device transitions into an ultra-low I_Q mode to maintain high efficiency and prevent draining battery cells connected to the input when the system is in standby. When configured in FPWM mode, at light loads, the device maintains CCM operation, enabling Fly-Buck converter operation. The Fly-Buck converter configuration can be used to generate both a non-isolated primary output and an isolated secondary output.

The LMR719xx incorporates additional features for comprehensive system requirements, including an open-drain power-good circuit for the following:

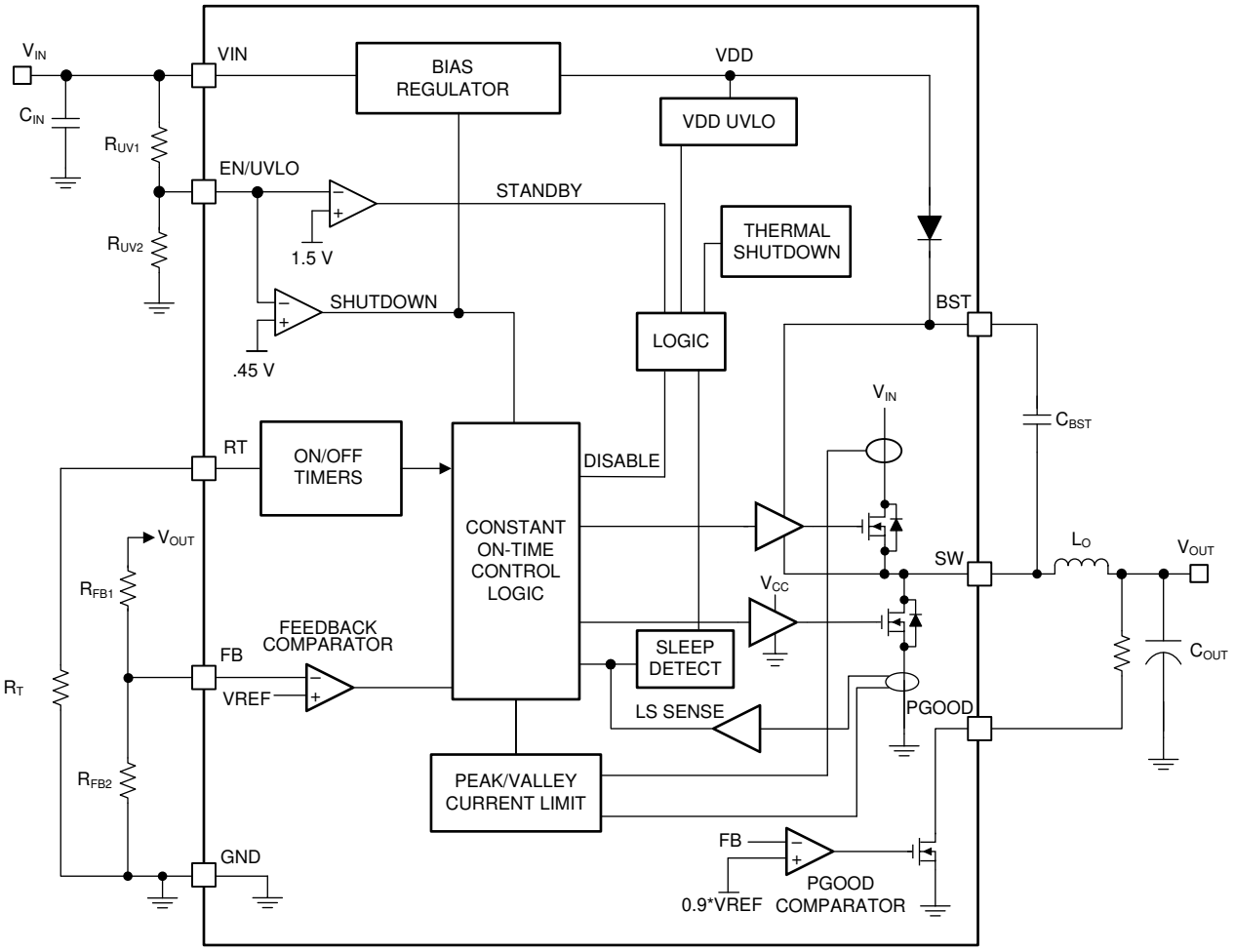
- Power-rail sequencing and fault reporting
- Internally fixed soft start
- Monotonic start-up into prebiased loads
- Precision enable for programmable line undervoltage lockout (UVLO)
- Smart cycle-by-cycle current limit for excellent inductor sizing
- Thermal shutdown with automatic recovery

The LMR719xx supports a wide range of end equipment requiring a regulated output from a high input supply where the transient voltage deviates from the DC level. Examples of such end equipment systems are the following:

- 48V automotive systems
- High cell-count battery-pack systems
- 24V industrial systems
- 48V telecom and PoE voltage ranges

The pin arrangement is designed for a simple layout that requires only a few external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Architecture

The LMR719xx step-down switching converter employs a constant on-time (COT) control scheme. The COT control scheme sets a fixed on time, t_{ON}, of the high-side FET using a timing resistor (R_T). t_{ON} is adjusted as V_{IN} changes and is inversely proportional to the input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After expiration of t_{ON}, the high-side FET remains off until the feedback pin is equal or below the reference voltage of 1V. To maintain stability, the feedback comparator requires a minimal ripple voltage that is in-phase with the inductor current during the off time. Furthermore, this change in feedback voltage during the off time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 20mV. In some cases, more ripple voltage can be needed for robust operation. This statement is especially true when there is excessive coupling from the SW pin or the BST pin to the FB pin. The Type 1 ripple generation method is more susceptible to noise injection than the other methods. See Table 7-1 for different types of ripple injection schemes that ensure stability over the full input voltage range.

During a rapid start-up or a positive load step, the regulator operates with minimum off times until regulation is achieved. This feature enables extremely fast load transient response with minimum output voltage undershoot. When regulating the output in steady-state operation, the off time automatically adjusts to produce the SW pin duty cycle required for output voltage regulation to maintain a fixed switching frequency. In CCM, the switching frequency F_{SW} is programmed by the R_T resistor.

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Table 7-1. Ripple Generation Methods

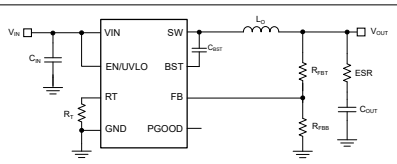
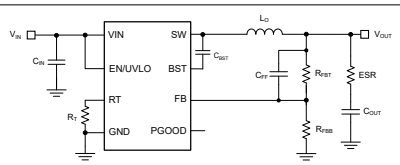
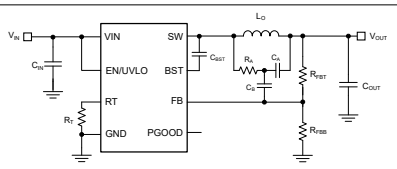
TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
		
$R_{ESR} \geq \frac{20\text{mV} \times V_{OUT}}{V_{FB} \times \Delta I_L}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \times V_{IN} \times F_{SW} \times C_{OUT}}$	$R_{ESR} \geq \frac{20\text{mV}}{\Delta I_L}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \times V_{IN} \times F_{SW} \times C_{OUT}}$ $C_{FF} \geq \frac{1}{2\pi \times F_{SW} \times (R_{FBB} \| R_{FBT})}$	$C_A \geq \frac{10}{F_{SW} \times (R_{FBB} \| R_{FBT})}$ $R_A \times C_A \leq \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{20\text{mV}}$ $C_B \geq \frac{T_{settle}}{3 \times R_{FBT}}$

Table 7-1 presents three different methods for generating appropriate voltage ripple at the feedback node. The Type-1 ripple generation method uses a single resistor, R_{ESR}, in series with the output capacitor. The generated voltage ripple has two components: capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor and resistive ripple caused by the inductor ripple current flowing into the output capacitor and through series resistance R_{ESR}. The capacitive ripple component is out-of-phase with the inductor current and does not decrease monotonically during the off time. The resistive ripple component is in-phase with the inductor current and decreases monotonically during the off time. The resistive ripple must exceed the capacitive ripple at V_{OUT} for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off time. The equations under Type 1 define the value of the series resistance R_{ESR} to make sure of sufficient in-phase ripple at the feedback node.

Type 2 ripple generation uses a C_{FF} capacitor in addition to the series resistor. As the output voltage ripple is directly AC-coupled by C_{FF} to the feedback node, the R_{ESR} and ultimately the output voltage ripple, are reduced by a factor of V_{OUT} / V_{FB}.

Type 3 ripple generation uses an RC network consisting of R_A and C_A, and the switch node voltage to generate a triangular ramp that is in-phase with the inductor current. This triangular wave is then AC-coupled into the feedback node with capacitor C_B. Because this circuit does not use output voltage ripple, this circuit is designed for applications where low output voltage ripple is critical. See the *Related Documentation* section for more details about COT control methods.

Light load mode operation can be set to PFM and DEM operation or FPWM operation as a factory option. Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains the highest efficiency at light load currents by decreasing the effective switching frequency. DEM operation occurs when the synchronous power MOSFET switches off as inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and prevents negative current conduction reduces conduction loss. Power conversion efficiency is higher in a DEM converter than an equivalent forced-PWM CCM converter. With DEM operation, the duration that both power MOSFETs remain off progressively increases as load current decreases. When this idle duration exceeds 15µs, the converter transitions into an ultra-low I_Q mode, consuming only 5µA quiescent current from the input. In FPWM operation, the DEM feature is turned off. This action means that the device remains in CCM under light loads, and the device is capable of operating in a Fly-Buck converter configuration.

7.3.2 Internal VCC Regulator and Bootstrap Capacitor

The LMR719xx contains an internal linear regulator that is powered from VIN with a nominal output of 5V, eliminating the need for an external capacitor to stabilize the linear regulator. The internal VCC regulator supplies current to internal circuit blocks, including the synchronous FET driver and logic circuits. The input pin (VIN) can be connected directly to line voltages up to 115V. Because the power MOSFET has a low total gate

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charge, use a low bootstrap capacitor value to reduce the stress on the internal regulator. Select a high-quality 2.2nF X7R ceramic bootstrap capacitor. An internal diode connects from the VCC regulator to the BST pin to replenish the charge in the high-side gate drive bootstrap capacitor when the SW voltage is low.

7.3.3 Internal Soft Start

The LMR719xx employs an internal soft-start control ramp that allows the output voltage to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. The soft-start feature produces a controlled, monotonic output voltage start-up. The soft-start time is internally set to 3ms.

7.3.4 On-Time Generator

The on time of the LMR719xx high-side FET is determined by the R_T resistor and is inversely proportional to the input voltage, V_{IN}. The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. Use Equation 1 to calculate the on time, where R_T is in kΩ.

$$T_{ON} = \frac{R_T}{2.5 \times V_{IN}} \ [\mu s] \quad (1)$$

Use Equation 2 to determine the R_T resistor to set a specific switching frequency in CCM, where F_{SW} is in kHz.

$$R_T = \frac{2500 \times V_{OUT}}{F_{SW}} \ [k\Omega] \quad (2)$$

Select R_T for a minimum on time (at maximum V_{IN}) greater than 30ns for proper buck operation and greater than 100ns for proper Fly-Buck converter operation. In addition to this minimum on time, the maximum frequency for this device is limited to 1MHz.

7.3.5 Current Limit

The LMR71907P manages overcurrent conditions with cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold (1.1A typical). To protect the converter from potential current runaway conditions, the LMR71907P includes a fold-back valley current limit feature, set at 0.75A, that is enabled if a peak current limit is detected. As shown in Figure 7-1, if the peak current in the high-side MOSFET exceeds 1.1A, the present cycle is immediately terminated regardless of the programmed on time (t_{ON}), the high-side MOSFET is turned off and the fold-back valley current limit is activated. The low-side MOSFET remains on until the inductor current drops below this fold-back valley current limit, after which the next on-pulse is initiated. This method folds back the switching frequency to prevent overheating and limits the average output current to less than 0.75A for LMR71907P to make sure of proper short-circuit and heavy-load protection.

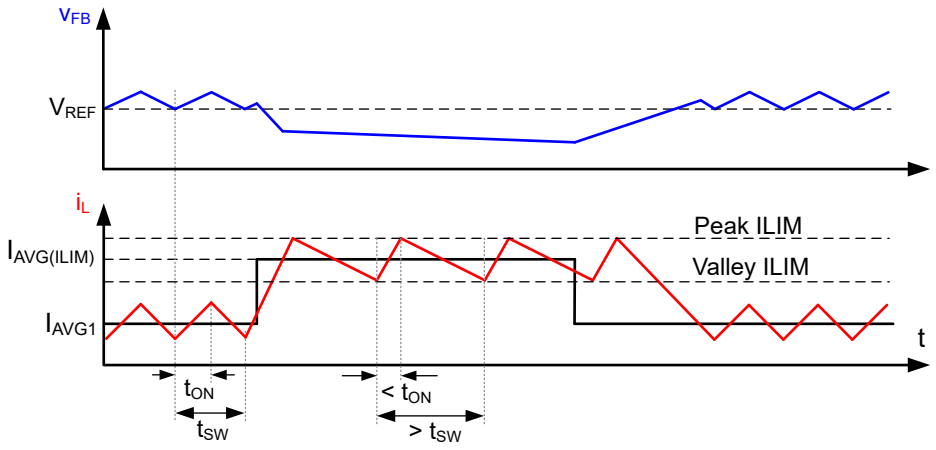

Figure 7-1. Current Limit Timing Diagram

Current is sensed after a leading-edge blanking time following the high-side MOSFET turn-on transition. The propagation delay of the current limit comparator is 100ns. During high step-down conditions when the on time is less than 100ns, a backup peak current limit comparator in the low-side FET also set at 2.2A or 1.1A, enables the foldback valley current limit set at 1.5A or 0.75A. This remarkable current limit scheme enables ultra-low duty-cycle operation, permitting large step-down voltage conversions while making sure of robust protection of the converter.

The LMR71907F, LMR71915F implement a current limit off-timer and hiccup protection. If the current in the high-side MOSFET exceeds $I_{HS\_PK(OC)}$, the high-side MOSFET is immediately turned off and a non-resettable off-timer is initiated. The length of the off time is controlled by the feedback voltage and the input voltage. The off-timer makes sure of safe short circuit operation in a Fly-Buck converter configuration. An overload current on the secondary output can result in the secondary voltage collapsing while the primary voltage remains in regulation. This action results in a possible condition where the secondary output voltage does not recover after the overload condition. Hiccup protection makes sure a soft-start counter enables both the secondary and primary output voltages to recover properly after an overcurrent event is detected for 16 consecutive current limit cycles. After eight consecutive cycles without current limit detection, restart the hiccup protection counter. These devices attempt soft start after a *hiccup period* of 192ms.

7.3.6 N-Channel Buck Switch and Driver

The LMR719xx integrates an N-channel buck switch and associated floating high-side gate driver. The gate-driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage bootstrap diode. A high-quality ceramic capacitor connected between the BST and SW pins provides the voltage to the high-side driver during the buck switch on time. See Section 7.3.2 for details. During the off time, the SW pin is pulled down to approximately 0V, and the bootstrap capacitor charges from the internal VCC through the internal bootstrap diode. The minimum off-timer, set to 50ns (typical), makes sure of a minimum time each cycle to recharge the bootstrap capacitor. When the on time is less than 150ns, the minimum off-timer is forced to 200ns to make sure that the BST capacitor is charged in a single cycle. This is vital during wake-up from sleep mode when the BST capacitor is most likely discharged.

7.3.7 Synchronous Rectifier

The LMR719xx provides an internal low-side synchronous rectifier N-channel MOSFET. This MOSFET provides a low-resistance path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier operates in a diode emulation mode. Diode emulation enables the regulator to operate in a pulse-skipping mode during light load conditions. This mode leads to a reduction in the average switching frequency at light loads. Switching losses and FET gate driver losses, both of which are proportional to switching frequency, are significantly reduced at very light loads and efficiency is improved. This pulse-skipping mode also reduces the circulating inductor current and losses associated with conventional CCM at light loads.

7.3.8 Enable, Undervoltage Lockout (EN/UVLO)

The LMR719xx contains a dual-level EN/UVLO circuit. When the EN/UVLO voltage is below 0.45V (typical), the converter is in a low-current shutdown mode and the input quiescent current (I_Q) is dropped down to 0.7µA (typical). When the voltage is greater than 1.1V but less than 1.5V (typical), the converter is in standby mode. In standby mode, the internal bias regulator is active while the control circuit is disabled. When the voltage exceeds the rising threshold of 1.5V (typical), normal operation begins. Install a resistor divider from VIN to GND to set the minimum operating voltage of the regulator. If the user wishes to implement an input voltage UVLO, refer to Figure 7-2, Equation 3, and Equation 4 for details. Typically, the user chooses a value for R_{UV1} and calculate the value of R_{UV2} using Equation 3 based on a desired V_{ON}. Reasonable values for R_{UV1} are in the 1MΩ range. Equation 4 is then used to calculate the resulting V_{OFF}. V_{ON} and V_{OFF} are the input voltages where the device turns on and off, respectively.

ADVANCE INFORMATION

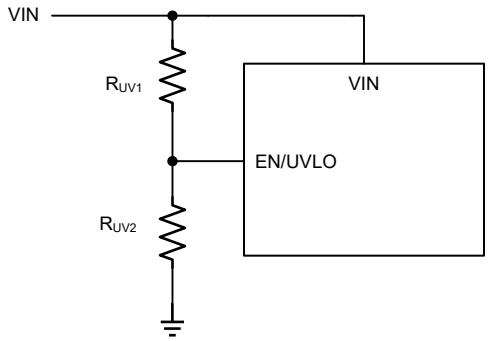

Figure 7-2. Input UVLO Connections

$$R_{UV2} = R_{UV1} \times \left(\frac{V_{EN(R)}}{V_{ON} - V_{EN(R)}} \right) \quad (3)$$

$$V_{OFF} = V_{EN(F)} \times \left(1 + \frac{R_{UV1}}{R_{UV2}} \right) \quad (4)$$

If input UVLO is not required, the user can either drive EN/UVLO as an enable input driven by a logic signal or connect directly to VIN. If EN/UVLO is directly connected to VIN, the regulator begins switching as soon as the internal bias rails are active; about 4.5V at VIN.

7.3.9 Power Good (PGOOD)

The LMR719xx provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start-up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 14V. The typical range of pullup resistance is 10kΩ to 100kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. When the FB voltage exceeds 95% of the internal reference V_{REF}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 90% of V_{REF}, an internal 7Ω PGOOD switch turns on and PGOOD pulls low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5µs.

7.3.10 Thermal Protection

The LMR719xx includes an internal junction temperature monitor to protect the device in the event of higher than normal junction temperature. If the junction temperature exceeds 175°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The LMR719xx initiates a restart sequence when the junction temperature falls to 165°C, based on a typical thermal shutdown hysteresis of 10°C. This protection is a non-latching protection, so the device cycles into and out of thermal shutdown if the fault persists.

ADVANCE INFORMATION

7.4 Device Functional Modes

7.4.1 Shutdown Mode

EN/UVLO provides ON and OFF control for the LMR719xx. When $V_{EN/UVLO}$ is below approximately 0.45V, the device is in shutdown mode. Both the internal linear regulator and the switching regulator are off. The quiescent current in shutdown mode drops to 0.7µA typical at V_{IN} = 24V. The LMR719xx also employs internal bias rail undervoltage protection. If the input voltage is below about 4.5V, the regulator remains off.

7.4.2 Active Mode

The LMR719xx is in active mode when $V_{EN/UVLO}$ is above the precision enable threshold and the internal bias rail is above the UV threshold. In COT active mode, the LMR719xx is in one of the following modes depending on the load current:

1. CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
2. Auto mode (P device designator) – light load operation: Pulse skipping and diode emulation mode (DEM) when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation.
3. FPWM mode (F device designator) – light load operation: continuous conduction mode (CCM) throughout the entire load current range, including when the load current is lower than half of the inductor current ripple
4. Current limit CCM with peak and valley current limit protection when an over-current condition is applied at the output

7.4.3 Sleep Mode

Control Architecture gives a brief introduction to the LMR719xx diode emulation (DEM) feature. The converter enters DEM during light-load conditions when the inductor current decays to zero and the synchronous MOSFET is turned off to prevent negative current in the system. In the DEM state, the load current is lower than half of the peak-to-peak inductor current ripple and the switching frequency decreases when the load is further decreased as the device operates in a pulse skipping mode. A switching pulse is set when V_{FB} drops below 1V.

As the frequency of operation decreases and V_{FB} remains above 1V (V_{REF}) with the output capacitor sourcing the load current for greater than 15µs, the converter enters an ultra-low I_Q sleep mode to prevent draining the input power supply. The input quiescent current (I_Q) required by the LMR719xx decreases to 5µA typical in sleep mode, improving the light-load efficiency of the regulator. In this mode, all internal controller circuits are turned off to make sure of very low current consumption by the device. Such low I_Q renders the LMR719xx as the best option to extend operating lifetime for off-battery applications. The FB comparator and internal bias rail are active to detect when the FB voltage drops below the internal reference V_{REF} and the converter transitions out of sleep mode into active mode. There is a 9µs wake-up delay from sleep to active states.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMR719xx requires only a few external components to create a buck converter to step down from a wide range of supply voltages to a fixed output voltage. Several features are integrated in the device to meet system design requirements, including the following:

- Precision enable
- Input voltage UVLO
- Internal soft start
- Programmable switching frequency
- A PGOOD indicator

8.2 Typical Fly-Buck™ Converter Application

The LMR719xxF is designed for Fly-Buck converter applications by operating in FPWM mode. Figure 8-1 shows the schematic for a 12V output Fly-Buck converter regulator with a 12V auxiliary output, capable of delivering 625mA from each output, used as an example application for the LMR719xxF. Note that the secondary output ground can be floating with respect to the input supply ground. See Table 8-1 for a description of Fly-Buck converter terminology used in this example.

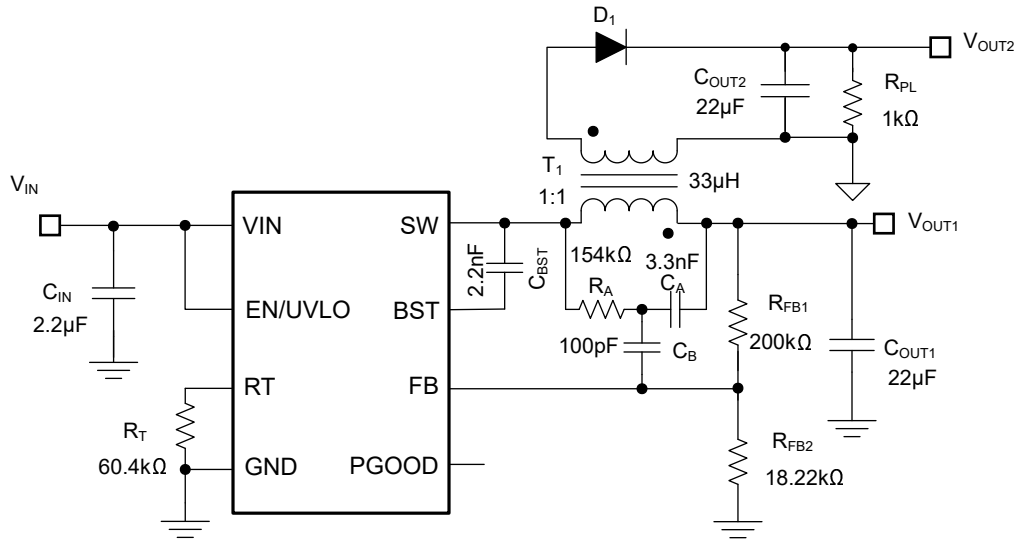

Figure 8-1. Example Fly-Buck™ Converter Application Circuit

Table 8-1. Fly-Buck™ Converter Terminology

TERM	DESCRIPTION
V_{OUT1}	Primary output voltage, as for a buck regulator. This output is tightly regulated by the LMR719xx.
V_{OUT2}	Secondary output voltage from couple inductor secondary winding. This voltage is not tightly regulated, but depends on parasitic voltage drops on the primary and secondary sides.
I_{OUT1}	Primary output current, as for a buck regulator
I_{OUT2}	Secondary output current from coupled inductor secondary winding

Note

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature, not the rated or nameplate values. Use high-quality, low ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This use can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

ADVANCE INFORMATION

8.2.1 Design Requirements

Table 8-2 lists the design requirements for a typical Fly-Buck converter application using the LMR719xx.

Table 8-2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Nominal input voltage	48V
Input voltage range	34V to 75V (operational to 115V)
Primary output voltage	12V
Secondary output voltage	12V
Primary output current	0.625A
Secondary output current	0.625A
Switching frequency	500kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency (R_T)

The switching frequency of the LMR719xx is set by the on-time programming resistor connected to the RT pin. Use Equation 2to calculate R_T based on the desired switching frequency. For this example of 500kHz, 60.4kΩ is used.

Note that at very low duty cycles, the 30ns minimum controllable on time of the high-side MOSFET, $t_{ON(min)}$, limits the maximum switching frequency. In CCM, $t_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency.

Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, design size, and efficiency.

8.2.2.2 Transformer Selection

For this Fly-Buck converter application, a coupled inductor (sometimes called a transformer) is required. The first step is to decide upon the turns ratio. In a Fly-Buck converter, the secondary output voltage is slightly less than the reflected primary output voltage scaled by the turns ratio. Equation 5 can be used to calculate the turns ratio for a given V_{OUT1} and V_{OUT2}. The nearest integer ratio must be selected. V_{OUT2} is slightly less than calculated due to the secondary diode drop and other parasitic voltage drops in the secondary. Also, keep in mind that the secondary voltage is not fed back to the controller, and is, therefore, not well regulated. For this example, V_{OUT2} is equal to V_{OUT1}, therefore, use a 1:1 turns ratio.

$$\frac{V_{OUT2}}{V_{OUT1}} \approx \frac{N_2}{N_1} \tag{5}$$

Next, the primary inductance must be calculated. This calculation is the same as calculating the inductance for an ordinary buck regulator, and is based on the desired primary ripple current. Typically, a ripple current of between 20% and 40% of the primary current is used. Equation 6 gives the primary current in a Fly-Buck converter and Equation 7 gives the required primary inductance. Using an input voltage of 48V and the other parameters in Table 8-2, the user arrives at a value of 36µH. A standard value of 33µH for this example is selected.

$$I_{PRI} = I_{OUT1} + I_{OUT2} \times \frac{N_2}{N_1} \tag{6}$$

$$L = \frac{V_{IN} - V_{OUT1}}{K \times I_{PRI} \times F_{SW}} \times \frac{V_{OUT1}}{V_{IN}} \tag{7}$$

where

- K = ripple current factor = 20% to 40%

Finally, the maximum currents in the transformer must be checked.

8.2.2.3 Secondary Output Diode

The secondary output diode must block the maximum input voltage reflected to the secondary by the transformer turns ratio. Use Equation 8 to determine the maximum reverse voltage on the diode. For this example, a value of 127V is calculated and a 200V diode is chosen. The diode current rating must be at least equal to the secondary output current with an appropriate factor of safety. Schottky diodes are the best choice for this application. Ultra-fast recovery diodes can also be used. In any case, choose a diode with the lowest turn-off time.

$$V_R > V_{IN}\frac{N_2}{N_1} + V_{OUT2} \quad (8)$$

8.2.2.4 C_{BST} Selection

The LMR719xx requires a bootstrap capacitor to be connected between the BST pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 2.2nF is required. Be sure to take into account the D.C. bias derating of the capacitor. The value of C_{BST} must not exceed 2.5nF.

8.2.2.5 Minimum Secondary Output Load

The secondary output must have a *dummy* load connected at all times to prevent the output voltage from rising too high under certain conditions. Because the secondary output is not tightly regulated by the control loop, and because of transformer and diode parasitics, C_{OUT2} can charge to high levels unless the energy is dissipated in the secondary output load. In this example, a 1kΩ resistor is used as a minimum load on the secondary output. A Zener diode can also be used to clamp the secondary output voltage, if desired.

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8.3 Power Supply Recommendations

The LMR719xx buck converter is designed to operate from a wide input voltage range between 6V and 115V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use Equation 9 to estimate the average input current.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (9)$$

where

η = efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, the parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the converter is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps to damp the input resonant circuit and reduce any voltage overshoots. A 10µF electrolytic capacitor with a typical ESR of 0.5Ω provides enough damping for most input circuit configurations.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters* application report provides helpful suggestions when designing an input filter for any switching regulator.

8.4 Layout

8.4.1 Layout Guidelines

PCB layout is a critical portion of good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply performance.

- Bypass the VIN pin to GND with a low-ESR ceramic bypass capacitor with a high-quality dielectric to help eliminate these problems,. Place C_{IN} as close as possible to the LMR719xx VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the GND pin and GND PAD.
- Minimize the loop area formed by the input capacitor connections to the VIN and GND pins.
- Locate the inductor close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling.
- Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
- Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
- Have a single-point ground connection to the plane. Route the ground connections for the feedback, and enable components to the ground plane. This action prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This action reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Minimize trace length to the FB pin. Place both feedback resistors, R_{FB1} and R_{FB2}, close to the FB pin. Place C_{FF} (if used) directly in parallel with R_{FB1}. If output set-point accuracy at the load is important, connect the V_{OUT} sense at the load. Route the V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a grounded shielding layer.
- The R_T pin is sensitive to noise. Thus, locate the R_T resistor as close as possible to the device and route with minimal lengths of trace. The parasitic capacitance from RT to GND must not exceed 20pF.

ADVANCE INFORMATION

- Provide adequate heat sinking for the LMR719xx to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad to the PCB ground plane. If the PCB has multiple copper layers, make sure these thermal vias also connect to inner layer heat-spreading ground planes.

8.4.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimizing radiated EMI is to identify the pulsing current path and minimize the area of that path. The topological architecture of a buck converter means that a particularly high di/dt current path exists in the loop comprising the input capacitor and the integrated MOSFETs of the LMR719xx, and reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory.

The input capacitor provides the primary path for the high di/dt components of the current of the high-side MOSFET. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the V_{OUT} side of the inductor, and connect the return terminal of the capacitor to the GND pin and exposed PAD of the LMR719xx.

8.4.1.2 Feedback Resistors

Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. The FB pin is the input to the feedback comparator, and as such, is a high impedance node sensitive to noise. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider, keeping away from the SW node, the inductor, and V_{IN} to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This action is most important when high feedback resistances greater than 100kΩ are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node, and V_{IN} so there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This action provides further shielding for the voltage feedback path from switching noise sources.

ADVANCE INFORMATION

8.4.2 Layout Example

Figure 8-2 shows an example layout for the PCB top layer with essential components placed on the top side.

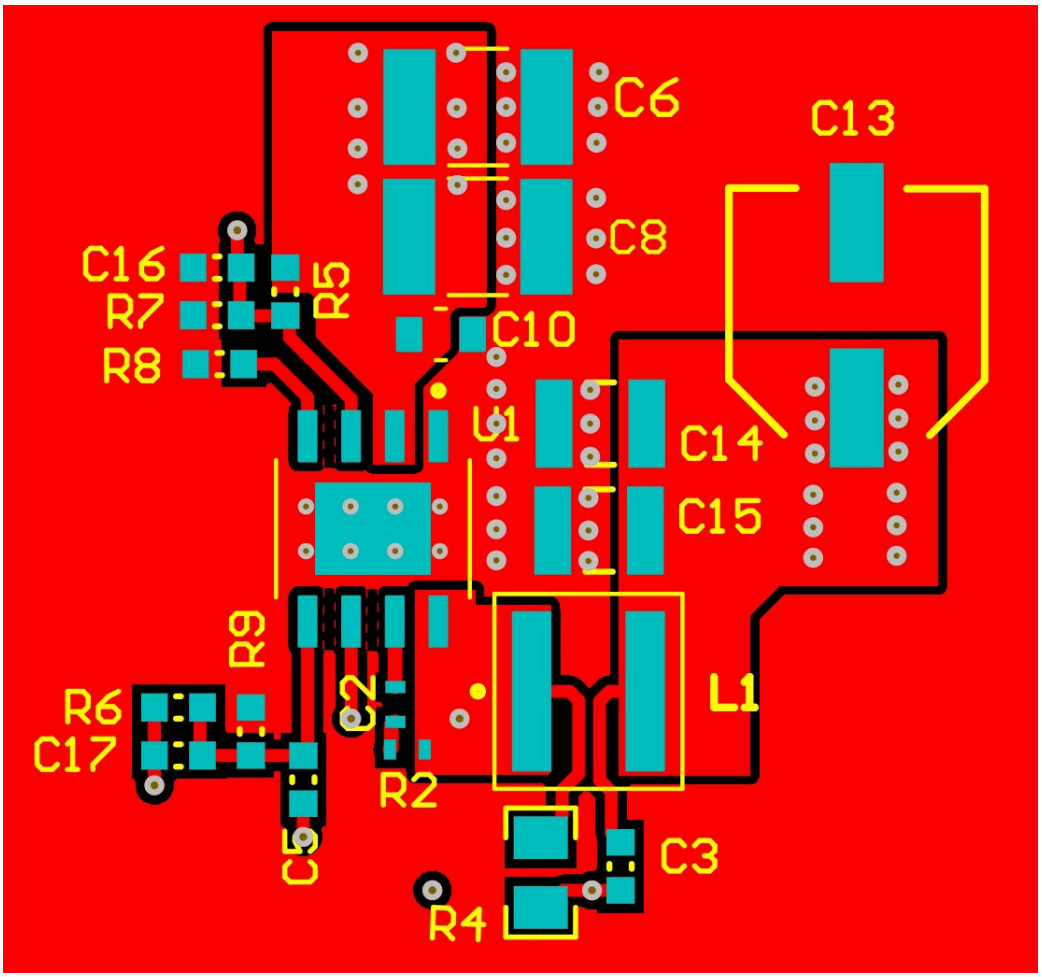

Figure 8-2. LMR719xx PCB Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Stability Analysis of COT Type-III Ripple Circuit* application note
- Texas Instruments, *Designing an Isolated Fly-Buck Converter Application Report* application note
- Texas Instruments, *Design a Fly-Buck Solution with Opto-coupler Application Report* application note
- Texas Instruments, *Designing an Isolated Fly-Buck Converter Using the LMR36520* application note
- Texas Instruments, *Selecting an Ideal Ripple Generation Network for Your COT Buck Converter* application note
- Texas Instruments, *Valuing Wide V_{IN}, Low-EMI Synchronous Buck Circuits for Cost-Effective, Demanding Applications* white paper
- Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies* white paper
- Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies* white paper
- Texas Instruments, *24V AC Power Stage with Wide V_{IN} Converter and Battery Gauge for Smart Thermostat* design guide
- Texas Instruments, *Accurate Gauging and 50µA Standby Current, 13S, 48V Li-ion Battery Pack Reference* design guide
- Texas Instruments, *AN-2162: Simple Success with Conducted EMI from DC/DC Converters* application note
- Texas Instruments, *Powering Drones with a Wide V_{IN} DC/DC Converter* application note
- Texas Instruments, *Using New Thermal Metrics* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ADVANCE INFORMATION

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
July 2025	*	Initial Release

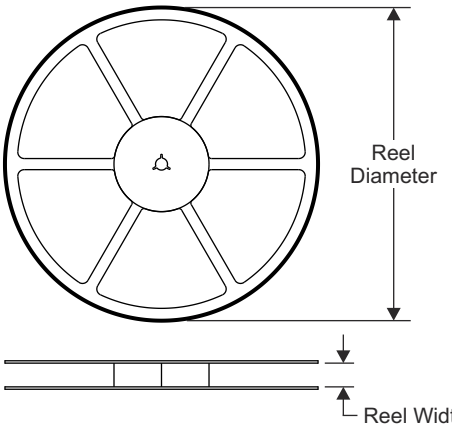
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

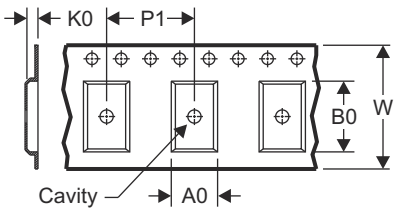
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

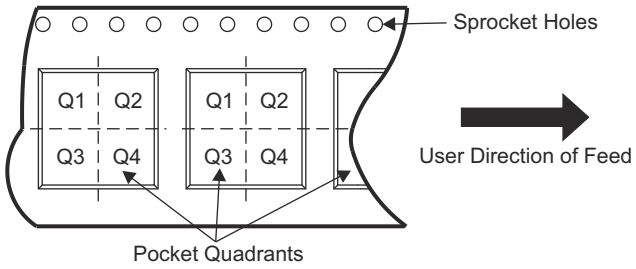


TAPE DIMENSIONS

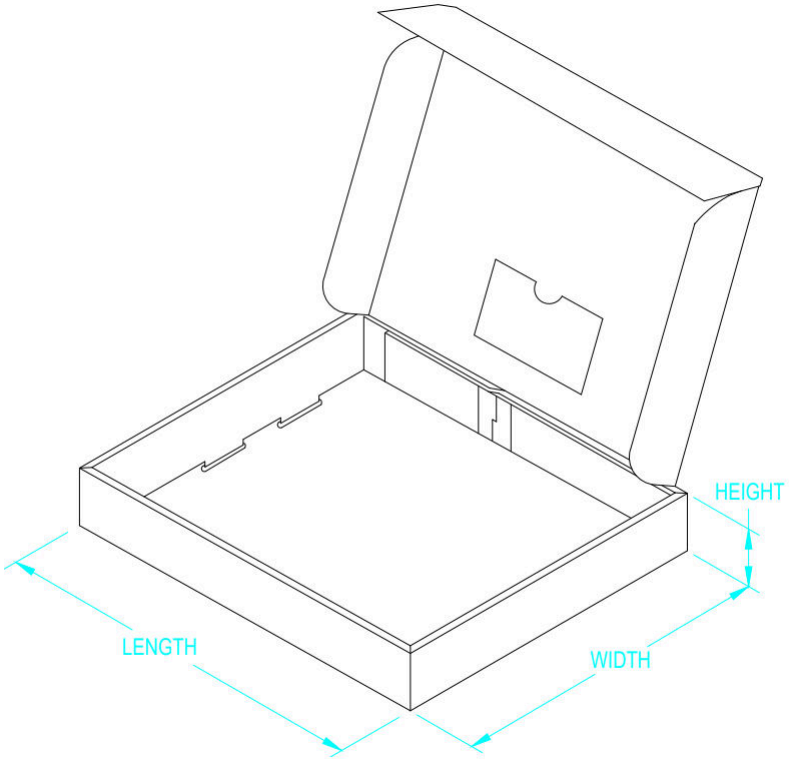


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR71915FDDARQ1	SOIC	DDA	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR71915FDDARQ1	SOIC	DDA	8	3000	353	353	35

ADVANCE INFORMATION

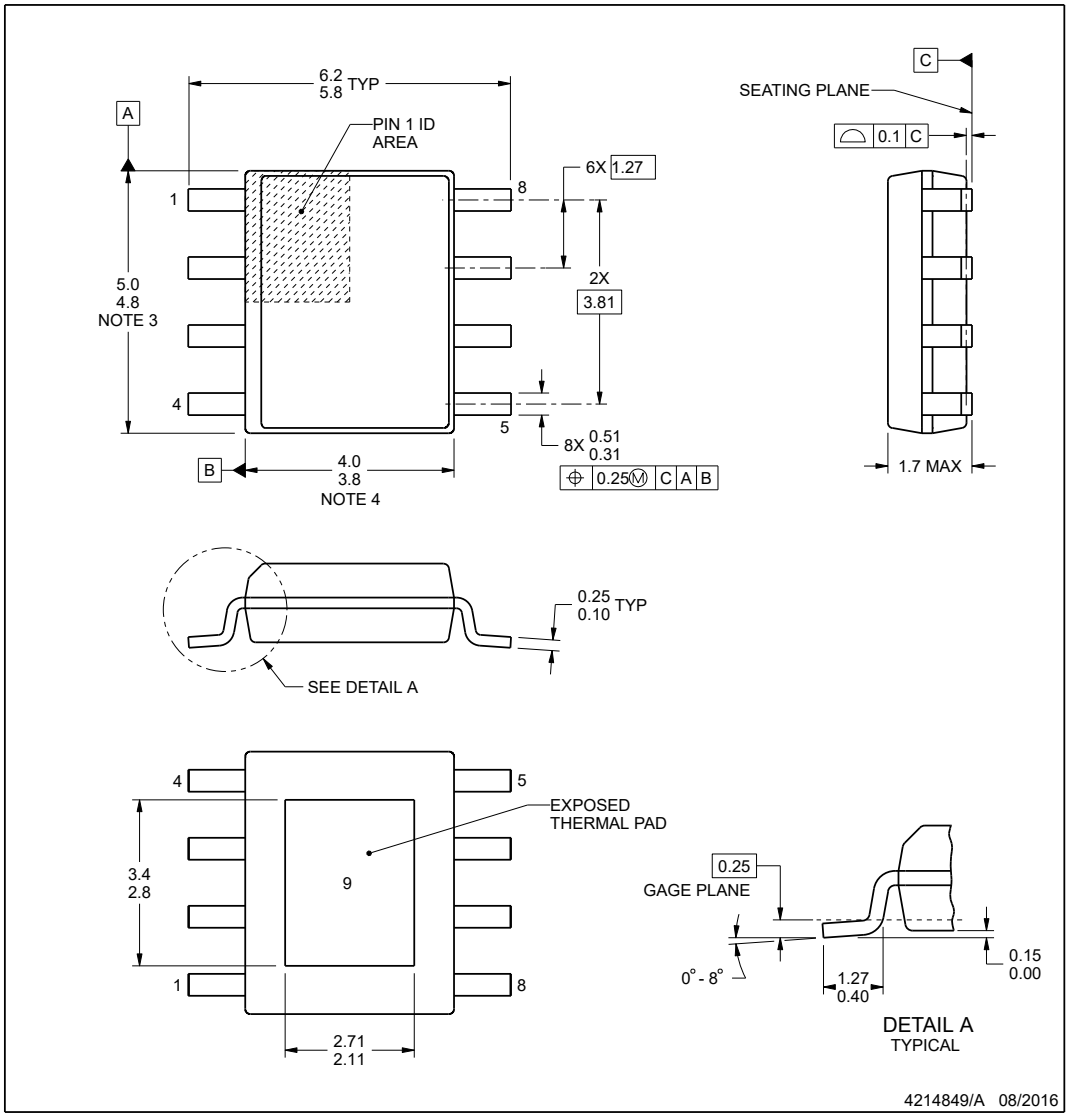
ADVANCE INFORMATION

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

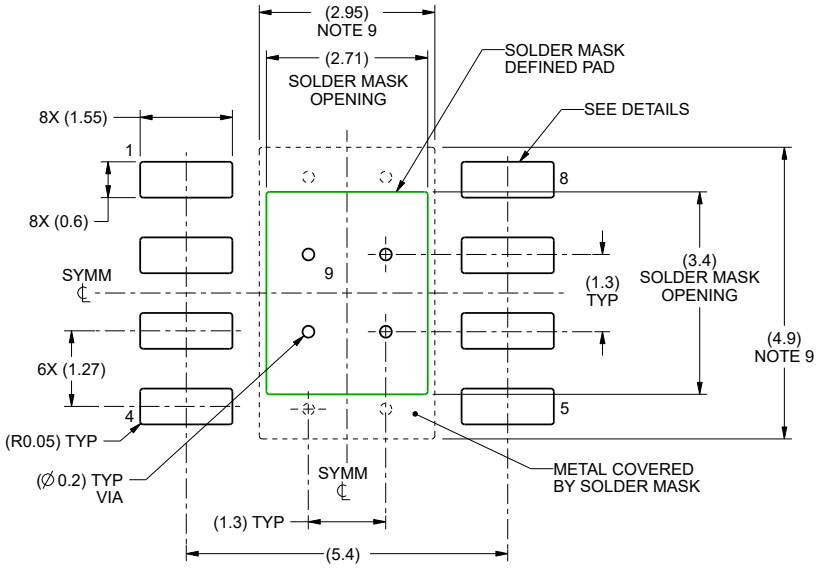
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

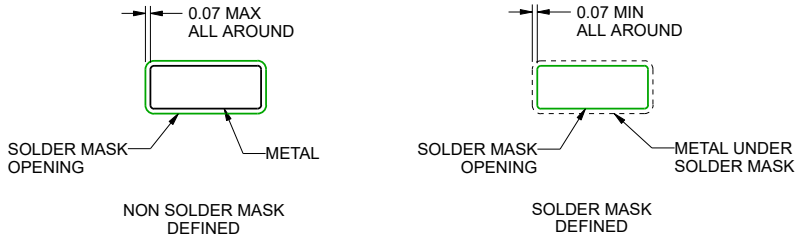
EXAMPLE BOARD LAYOUT

DDA0008B — **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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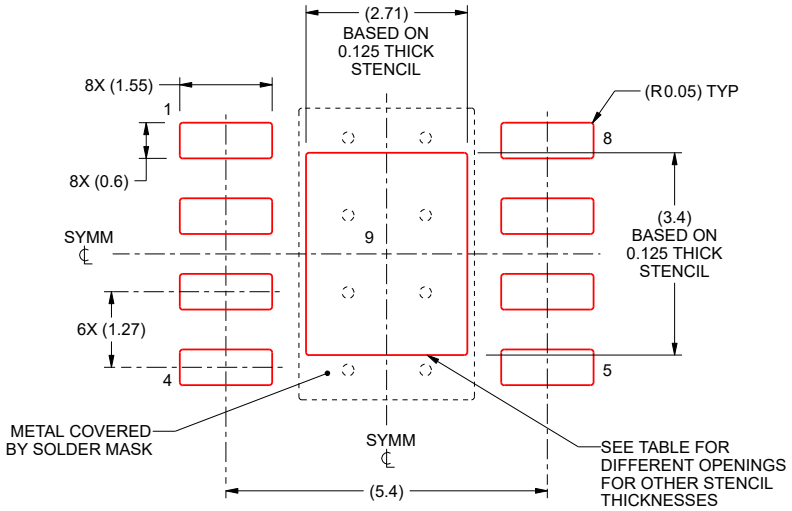
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DDA0008B — **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLMR71915FDDAR	Active	Preproduction	SO PowerPAD (DDA) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

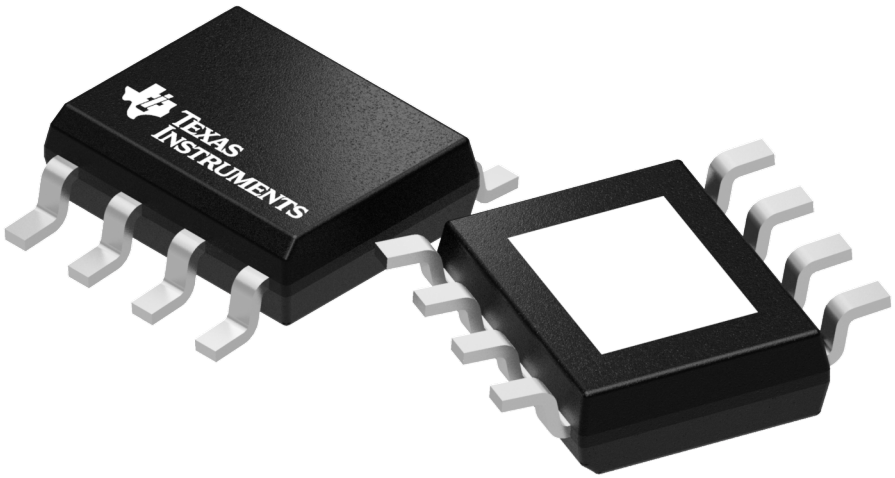
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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Last updated 10/2025