LMV7239-Q1 75-ns, Ultra Low Power, Low Voltage, Rail-to-Rail Input Comparator With Open-Drain and Push-Pull Output

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C5 for the DBV Package
- V_S = 5 V, T_A = 25°C (Typical Values Unless Otherwise Specified)
- Propagation Delay: 75 ns
- Low supply Current: 65 µA
- Rail-to-Rail Input
- Open Drain and Push-Pull Output
- Ideal for 2.7-V and 5-V, Single-Supply Applications
- Available in Space-Saving Packages:
  - 5-Pin SOT-23
  - 5-Pin SC70

2 Applications

- Portable and Battery-Powered Systems
- Set Top Boxes
- High-Speed Differential Line Receiver
- Window Comparators
- Zero-Crossing Detectors
- High-Speed Sampling Circuits

3 Description

The LMV7239-Q1 is a ultra low power, low voltage, 75-ns comparator. It is ensured to operate over the full supply voltage range of 2.7 V to 5.5 V. This device achieves a 75-ns propagation delay while consuming only 65 µA of supply current at 5 V.

The LMV7239-Q1 has a greater than rail-to-rail common-mode voltage range. The input common mode voltage range extends 200 mV below ground and 200 mV above supply, allowing both ground and supply sensing.

The LMV7239-Q1 features a push-pull output stage. This feature allows operation without the need of an external pullup resistor.

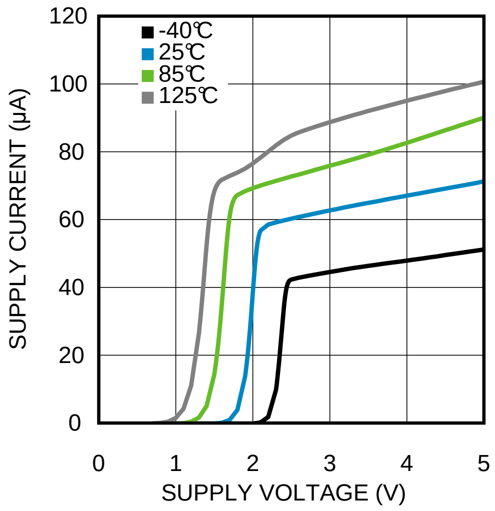
The LMV7239-Q1 is available in the 5-pin SC70 and 5-pin SOT-23 packages, which are ideal for systems where small size and low power is critical.

Device Information[1]

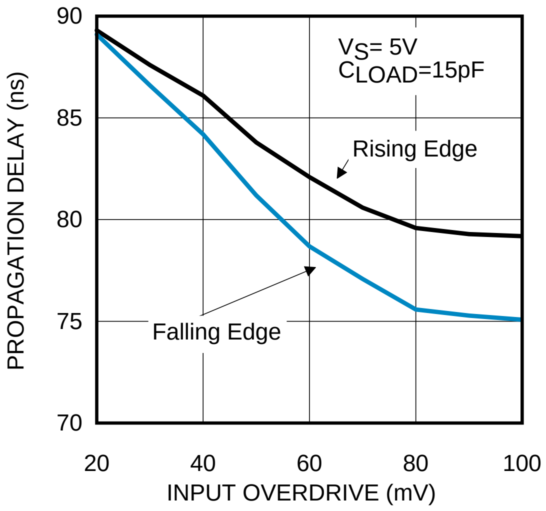
PART NUMBER	PACKAGES	BODY SIZE (NOM)
LMV7239-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Supply Current vs. Supply Voltage



Propagation Delay vs. Overdrive



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2018	*	Initial release. Moved the automotive device from the SNOS532 to a standalone data sheet and updated the input offset voltage parameter in the *Electrical Characteristics, 2.7 V* and *Electrical Characteristics, 5 V* tables

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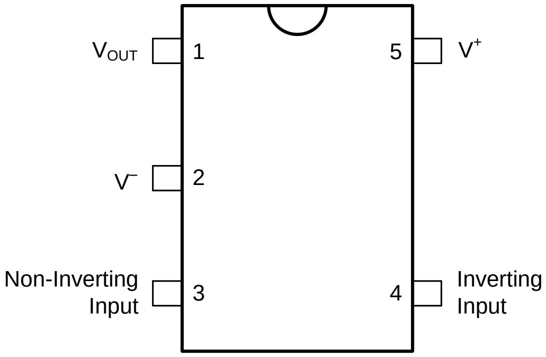
5 Pin Configuration and Functions

DBV and DGK Package
5-Pin SC70 and SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{OUT}	O	Output
2	V^{-}	P	Negative Supply
3	IN+	I	Noninverting Input
4	IN-	I	Inverting Input
5	V^{+}	P	Positive Supply

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Differential Input Voltage		± Supply Voltage	V
Output Short Circuit Duration		See (2)	
Supply Voltage (V^+ - V^-)		6	V
SOLDERING INFORMATION			
Infrared or Convection (20 sec)		235	°C
Wave Soldering (10 sec)		260 (lead temp)	°C
Voltage at Input/Output Pins		(V^+) +0.3, (V^-) −0.3	V
Current at Input Pin (3)		±10	mA
Storage Temperature, T_{stg}	–65	150	°C
Junction Temperature,T_J		150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.

(3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±1000	V
		Charged-device model (CDM), per AEC Q100-011(1)	DBV package only	±750	
		Machine model (MM)		±100	

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltages (V^+ - V^-)	2.7	5.5	V
Temperature Range(1)	–40	125	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC(1)		LMV7239-Q1		UNIT
		DGK (SC70)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	478	265	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics, 2.7 V

Unless otherwise specified, all limits ensured for T_A = 25°C, $V_{CM} = V^+/2$, V^+ = 2.7 V, V^- = 0 V^-.

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input Offset Voltage			–6	±0.8	+6	mV
		At temp extremes		–8		+8	
I_B	Input Bias Current				30	400	nA
		At temp extremes				600	
I_{OS}	Input Offset Current				5	200	nA
		At temp extremes				400	
CMRR	Common-Mode Rejection Ratio	0 V < V_{CM} < 2.7 V[3]		52	62		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7 V to 5 V		65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50 dB		V^- −0.1	−0.2 to 2.9	V^+ +0.1	V
			At temp extremes	V^-		V^+	
V_O	Output Swing Low	I_L = −4 mA, V_{ID} = −500 mV			230	350	mV
		At temp extremes				450	
		I_L = −0.4 mA, V_{ID} = −500 mV			15		
I_S	Supply Current	No load			52	85	μA
		At temp extremes				100	
t_{PD}	Propagation Delay	Overdrive = 20 mV C_{LOAD} = 15 pF			96		ns
		Overdrive = 50 mV C_{LOAD} = 15 pF			87		ns
		Overdrive = 100 mV C_{LOAD} = 15 pF			85		ns
t_r	Output Rise Time	LMV7239/LMV7239Q 10% to 90%			1.7		ns
t_f	Output Fall Time	90% to 10%			1.7		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) CMRR is not linear over the common mode range. Limits are guaranteed over the worst case from 0 to $V_{CC/2}$ or $V_{CC/2}$ to V_{CC}.

6.6 Electrical Characteristics, 5 V

Unless otherwise specified, all limits ensured for T_A = 25°C, $V_{CM} = V^+/2$, V^+ = 5 V, V^- = 0 V.

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input Offset Voltage			–6	±1	+6	mV
		At temp extremes		–8		+8	
I_B	Input Bias Current				30	400	nA
		At temp extremes				600	
I_{OS}	Input Offset Current				5	200	nA
		At temp extremes				400	
CMRR	Common-Mode Rejection Ratio	0 V < V_{CM} < 5 V		52	67		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7 V to 5 V		65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB		V^- −0.1	−0.2 to 5.2	V^+ +0.1	V
			At temp extremes	V^-		V^+	
V_O	Output Swing Low	I_L = −4 mA, V_{ID} = −500 mV			230	350	mV
			At temp extremes			450	
		I_L = −0.4 mA, V_{ID} = −500 mV			10		
I_S	Supply Current	No load			65	95	µA
			At temp extremes			110	
t_{PD}	Propagation Delay	Overdrive = 20 mV C_{LOAD} = 15 pF			89		ns
		Overdrive = 50 mV C_{LOAD} = 15 pF			82		ns
		Overdrive = 100 mV C_{LOAD} = 15 pF			75		ns
t_f	Output Fall Time	90% to 10%			1.2		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

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6.7 Typical Characteristics

(Unless otherwise specified, V_S = 5V, C_L = 10pF, T_A = 25°C).

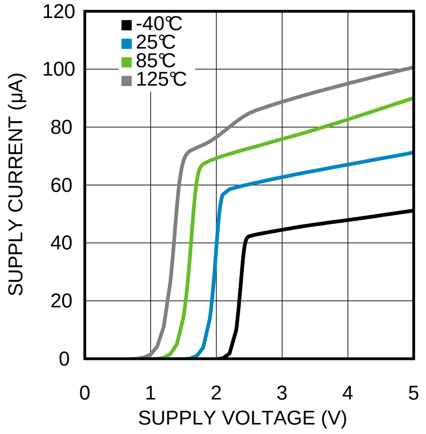

Figure 1. Supply Current vs. Supply Voltage

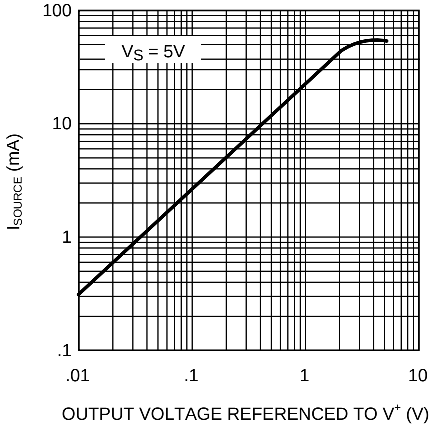

Figure 2. Sourcing Current vs. Output Voltage

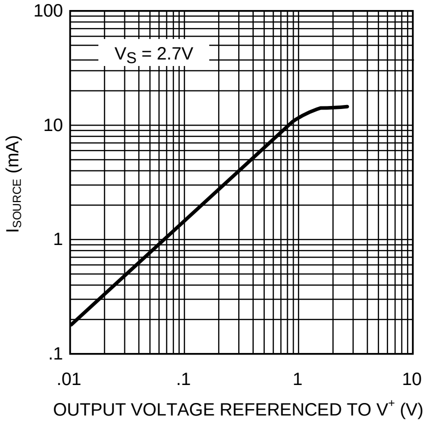

Figure 3. Sourcing Current vs. Output Voltage

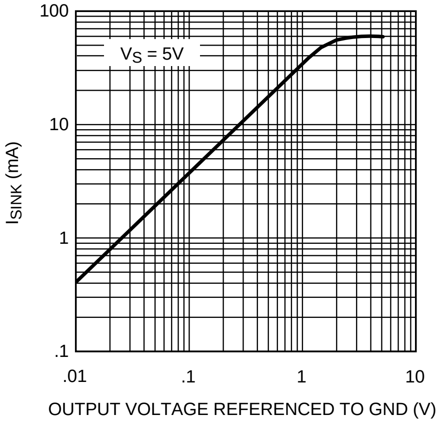

Figure 4. Sinking Current vs. Output Voltage

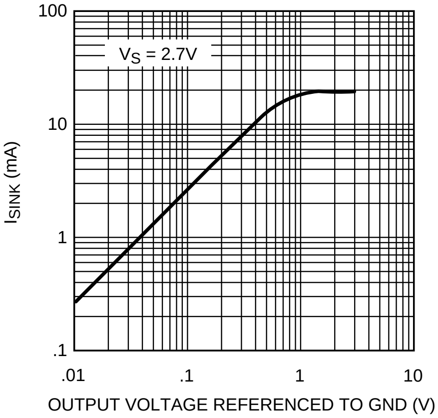

Figure 5. Sinking Current vs. Output Voltage

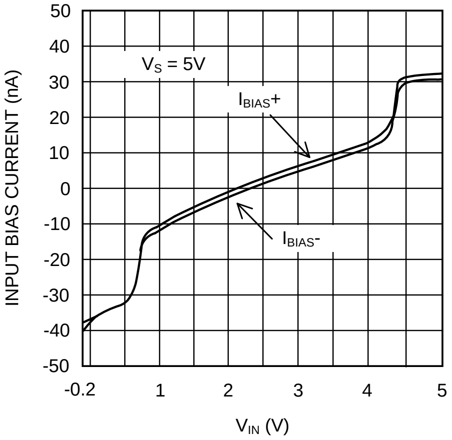

Figure 6. Input Bias Current vs. Input Voltage

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Typical Characteristics (continued)

(Unless otherwise specified, V_S = 5V, C_L = 10pF, T_A = 25°C).

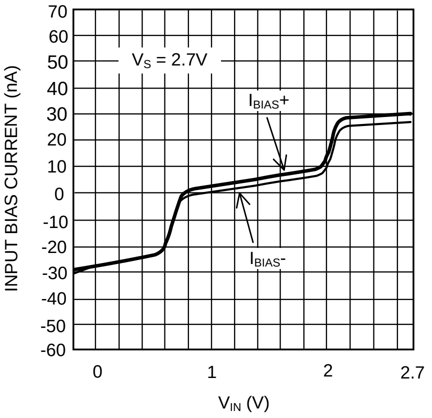

Figure 7. Input Bias Current vs. Input Voltage

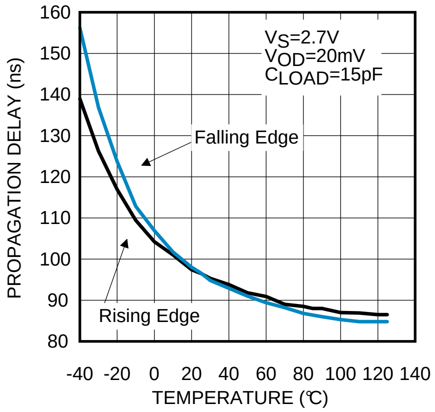

Figure 8. Propagation Delay vs. Temperature

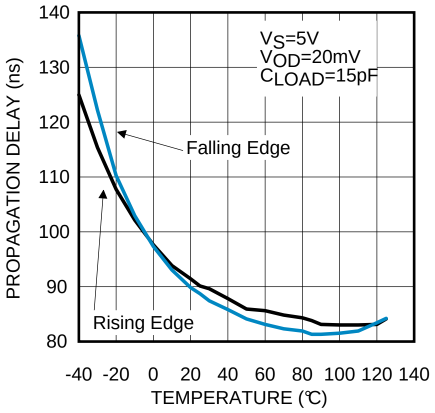

Figure 9. Propagation Delay vs. Temperature

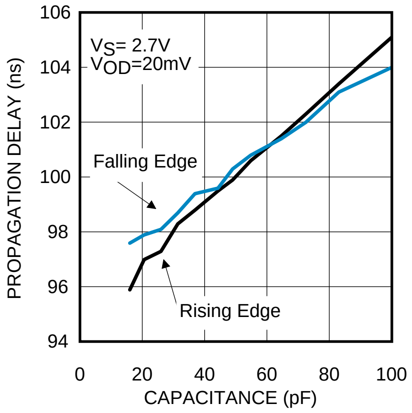

Figure 10. Propagation Delay vs. Capacitive Load

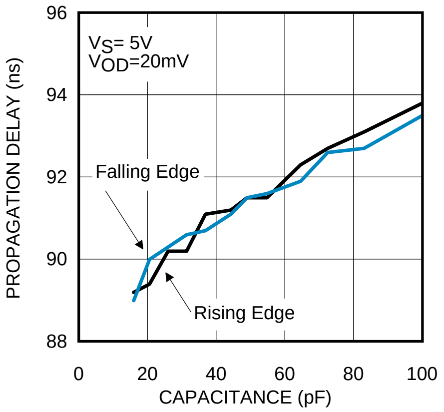

Figure 11. Propagation Delay vs. Capacitive Load

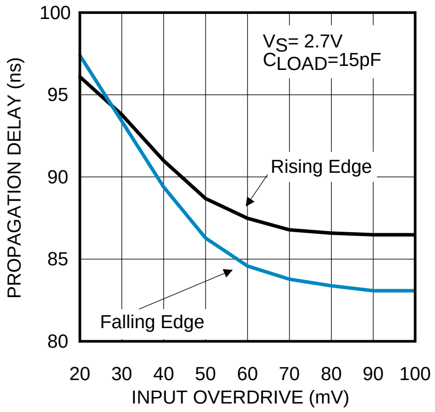

Figure 12. Propagation Delay vs. Input Overdrive

Typical Characteristics (continued)

(Unless otherwise specified, V_S = 5V, C_L = 10pF, T_A = 25°C).

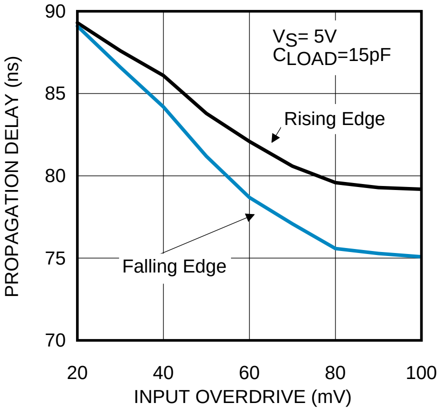

Figure 13. Propagation Delay vs. Input Overdrive

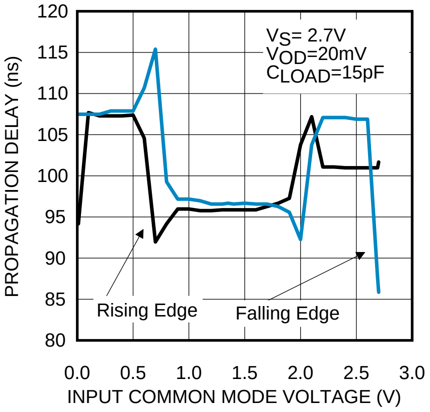

Figure 14. Propagation Delay vs. Common-Mode Voltage

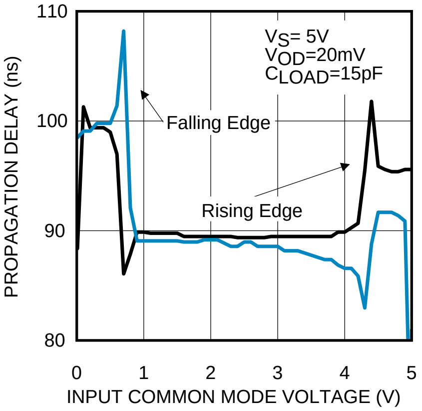

Figure 15. Propagation Delay vs. Common-Mode Voltage

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7 Detailed Description

7.1 Overview

The LMV7239-Q1 is an ultra low power, low voltage, 75-ns comparator. They are ensured to operate over the full supply voltage range of 2.7 V to 5.5 V. These devices achieve a 75-ns propagation delay while consuming only 65 µA of supply current at 5 V.

The LMV7239-Q1 has a greater than rail-to-rail common-mode voltage range. The input common-mode voltage range extends 200 mV below ground and 200 mV above supply, allowing both ground and supply sensing.

7.2 Functional Block Diagram

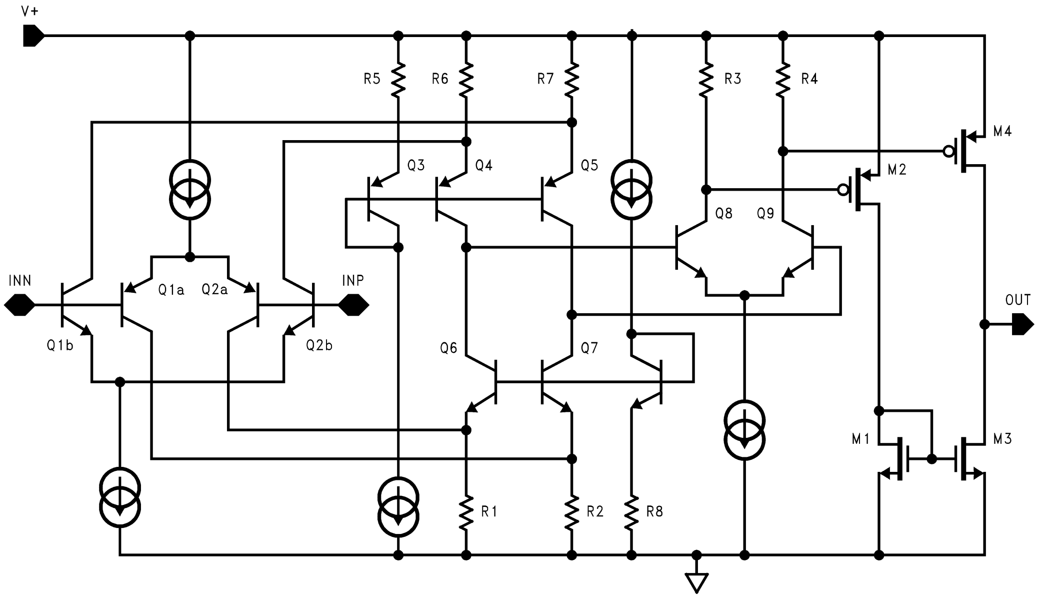

Figure 16. Simplified Schematic

7.3 Feature Description

7.3.1 Input Stage

The LMV7239-Q1 is a rail-to-rail input and output. The typical input common-mode voltage range of −0.2 V below the ground to 0.2 V above the supply. The LMV7239-Q1 uses a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^- and the NPN stage senses common-mode voltage near V^+. If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on resulting in an increase of input bias current.

If one of the inputs goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common-mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

7.3.2 Output Stage: LMV7239-Q1

The LMV7239-Q1 has a push-pull output. When the output switches, there is a low resistance path between V_{CC} and ground, causing high output sinking or sourcing current during the transition.

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Feature Description (continued)

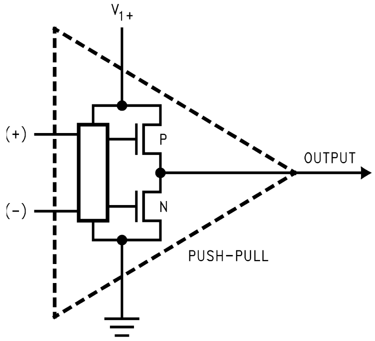

Figure 17. LMV7239-Q1 Push-Pull Output Stage

7.4 Device Functional Modes

7.4.1 Capacitive and Resistive Loads

The propagation delay is not affected by capacitive loads at the output of the LPV7239 or LMV7239-Q1. However, resistive loads slightly effect the propagation delay on the falling edge depending on the load resistance value.

7.4.2 Noise

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero. The high gain of this comparator eliminates this problem. Less than 1 μV of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See *Hysteresis*.)

7.4.3 Hysteresis

To improve propagation delay when low overdrive is needed hysteresis can be added.

7.4.3.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V^+ of the comparator as shown in Figure 18. When V_{IN} at the inverting input is less than V_A, the voltage at the noninverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V^+). The three network resistors can be represented as $R_1//R_3$ in series with R_2.

Device Functional Modes (continued)

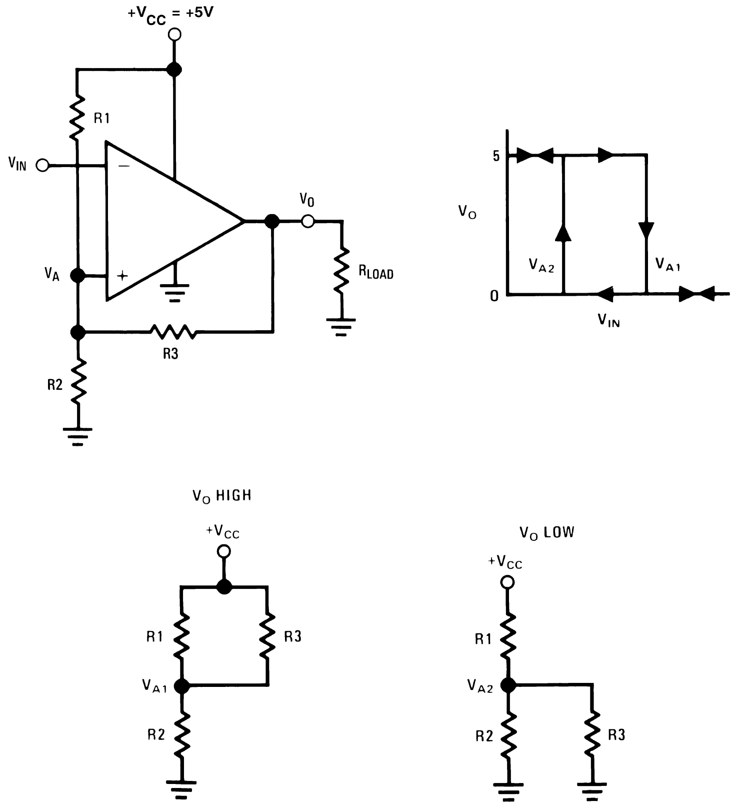

Figure 18. Inverting Comparator With Hysteresis

The lower input trip voltage V_{A1} is defined as:

$$V_{A1} = V_{CC}R_2 / [(R_1 // R_3) + R_2)] \quad (1)$$

When V_{IN} is greater than V_A, the output voltage is low or very close to ground. In this case the three network resistors can be presented as R_2 // R_3 in series with R_1.

The upper trip voltage V_{A2} is defined as:

$$V_{A2} = V_{CC} (R_2 // R_3) / [(R_1) + (R_2 // R_3)] \quad (2)$$

The total hysteresis provided by the network is defined as $\Delta V_A = V_{A1} - V_{A2}$.

$$\Delta V_A = \frac{+V_{CC}R_1R_2}{R_1R_2 + R_1R_3 + R_2R_3} \quad (3)$$

7.4.3.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by:

$$\Delta V_{IN1} = \frac{V_{REF}(R_1 + R_2)}{R_2} \quad (4)$$

As soon as V_O switches to V_{CC}, V_A steps to a value greater than V_{REF} which is given by:

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN1})R_1}{R_1 + R_2} \quad (5)$$

To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN2} can be calculated by:

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Device Functional Modes (continued)

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC} R_1}{R_2} \qquad (6)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC} R_1 / R_2 \qquad (7)$$

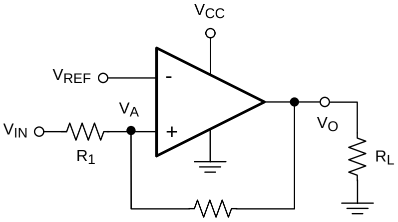

Figure 19. Noninverting Comparator With Hysteresis

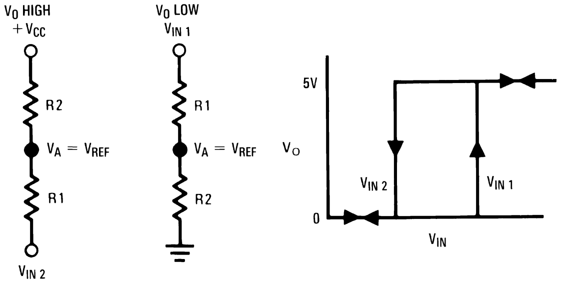

Figure 20. Noninverting Comparator Thresholds

7.4.4 Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the noninverting input is connected to a 100 mV_{PP} AC signal. As the signal at the noninverting input crosses 0V, the comparator's output changes state.

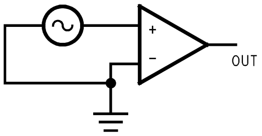

Figure 21. Simple Zero Crossing Detector

7.4.4.1 Zero Crossing Detector With Hysteresis

To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider R_4 and R_5 establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$.

The positive feedback resistor, R_6, is made very large with respect to $R_5 \parallel R_6 = 2000\ R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions.

Diode D_1 is used to ensure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

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Device Functional Modes (continued)

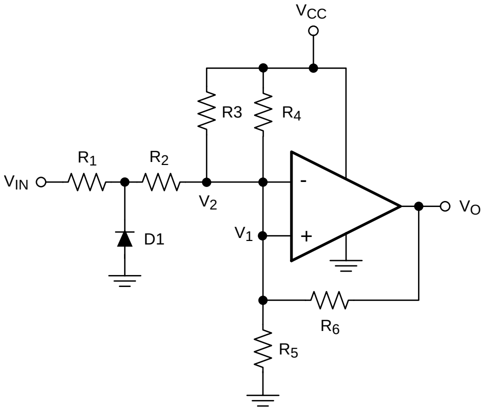

Figure 22. Zero Crossing Detector With Hysteresis

7.4.5 Threshold Detector

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. As the input on the noninverting input passes the V_{REF} threshold, the comparator's output changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

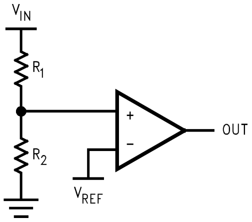

Figure 23. Threshold Detector

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV7239-Q1 is a single supply comparator with 75 ns of propagation delay and only 65 µA of supply current.

8.2 Typical Applications

8.2.1 Square Wave Oscillator

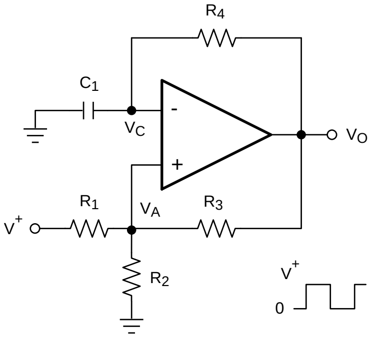

Figure 24. Square Wave Oscillator

8.2.1.1 Design Requirements

A typical application for a comparator is as a square wave oscillator. The circuit in Figure 24 generates a square wave whose period is set by the RC time constant of the capacitor C_1 and resistor R_4.

8.2.1.2 Detailed Design Procedure

The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.

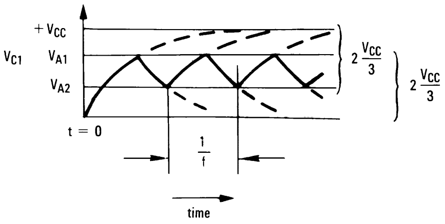

Figure 25. Square Wave Oscillator Timing Thresholds

Consider the output of Figure 24 to be high to analyze the circuit. That implies that the inverted input (V_C) is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at this point is:

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \parallel R_3} \tag{8}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{cc}/3$

Typical Applications (continued)

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is:

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)} \tag{9}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$.

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases until it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1 \cdot \ln 2$. Hence the formula for the frequency is:

$$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2) \tag{10}$$

The LMV7239 should be used for a symmetrical output. The LMV7235 will require a pullup resistor on the output to function, and will have a slightly asymmetrical output due to the reduced sourcing current.

8.2.1.3 *Application Curves*

Figure 26 shows the simulated results of an oscillator using the following values:

1. $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
2. $C_1 = 100$ pF, $C_L = 20$ pF
3. V+ = 5 V, V– = GND
4. C_{STRAY} (not shown) from Va to GND = 10 pF

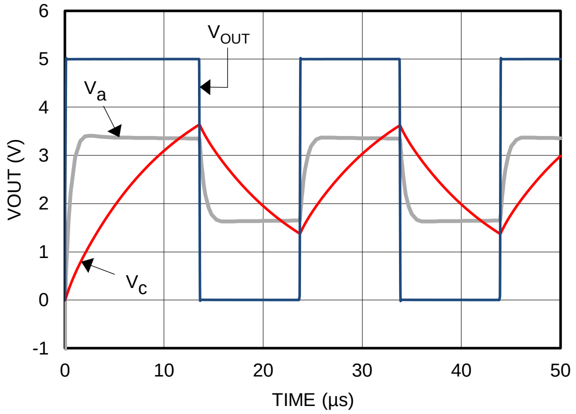

Figure 26. Square Wave Oscillator Output Waveform

8.2.2 Crystal Oscillator

A simple crystal oscillator using the LMV7239-Q1 is shown in Figure 27. Resistors R_1 and R_2 set the bias point at the comparator's noninverting input. Resistors, R_3 and R_4 and capacitor C_1 set the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator

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Typical Applications (continued)

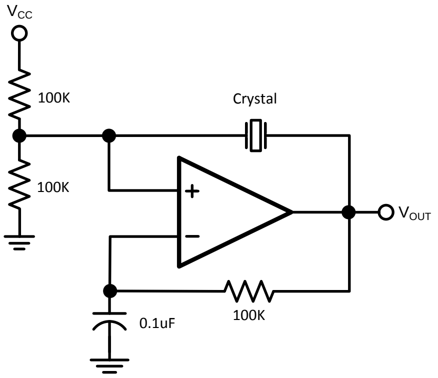

Figure 27. Crystal Oscillator

8.2.3 Infrared (IR) Receiver

The LMV7239-Q1 can also be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across RD. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions.

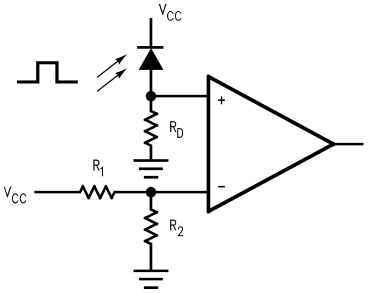

Figure 28. IR Receiver

8.2.4 Window Detector

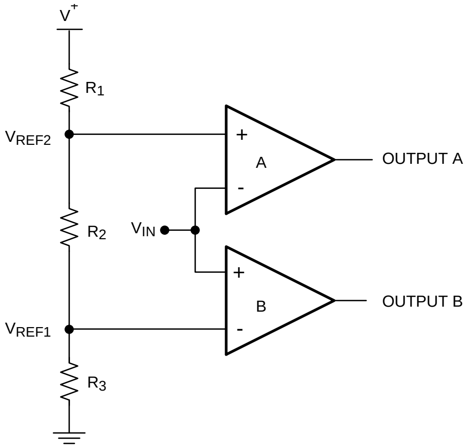

Figure 29. Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when $V_{REF1} < V_{IN} < V_{REF2}$

Typical Applications (continued)

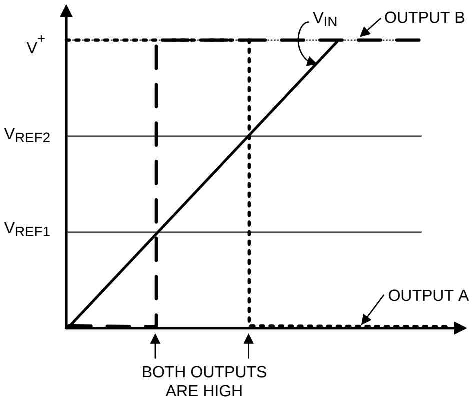

Figure 30. Window Detector Output Signal

The comparator outputs A and B are high only when $V_{REF1} < V_{IN} < V_{REF2}$, or "within the window", where these are defined as:

$$V_{REF1} = R_3/R_1+R_2+R_3) \times V+ \quad (11)$$

$$V_{REF2} = R_2+R_3)/R_1+R_2+R_3) \times V+ \quad (12)$$

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.

9 Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01-µF ceramic capacitor in parallel with a 10-µF capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to "ring" due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV7239-Q1 as a high-speed device. Keep the ground paths short and place small (low ESR ceramic) bypass capacitors directly between the V+ and V– pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

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10 Layout

10.1 Layout Guidelines

Proper grounding and the use of a ground plane will help to ensure the specified performance of the LMV7239-Q1. Minimizing trace lengths, reducing unwanted parasitic capacitance and using surface-mount components will also help. Comparators are very sensitive to input noise.

The LMV7239-Q1 requires a high-speed layout. Follow these layout guidelines:

1. Use printed-circuit board with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-µF, ceramic surface-mount capacitor) as close as possible to V_{CC} pin.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from output.
4. Solder the device directly to the printed-circuit board rather than using a socket.
5. For slow moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to t_{PD} when the source impedance is low.
6. The top-side ground plane runs between the output and inputs.
7. Ground trace from the ground pin runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

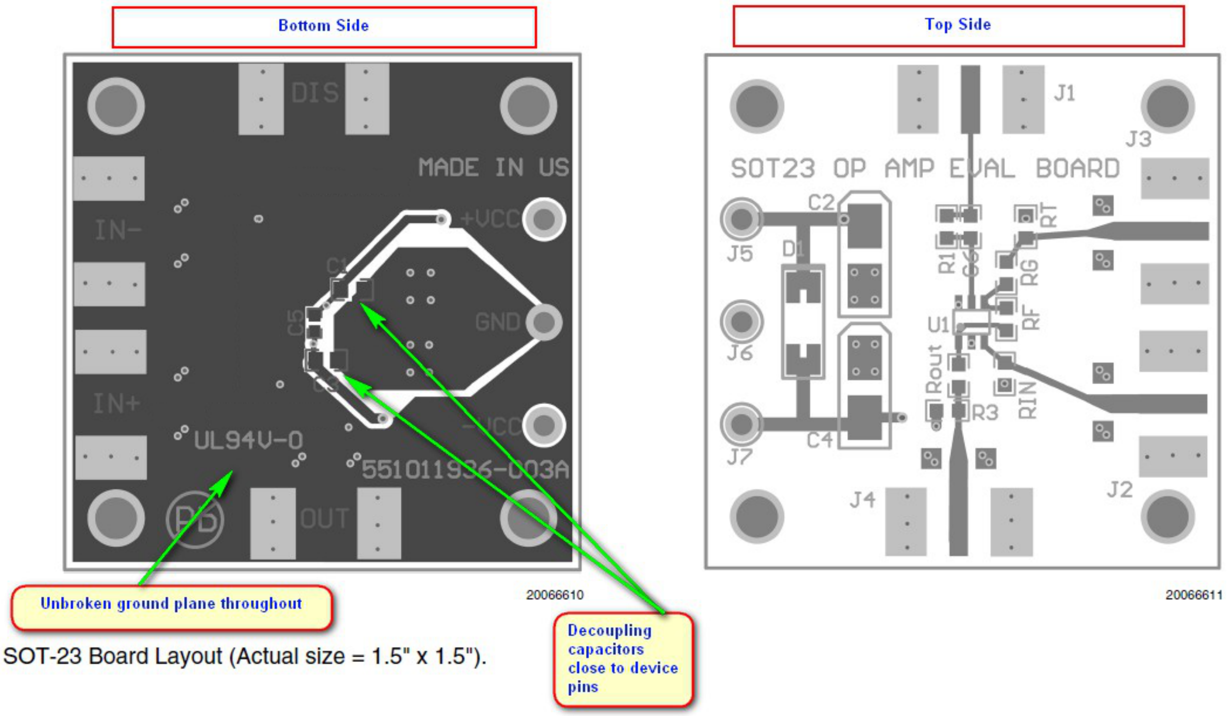

Figure 31. SOT-23 Board Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

11.2 Documentation Support

11.2.1 Related Documentation

A Quad of Independently Func Comparators (SNOA654)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV7239QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ZBMX
LMV7239QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ZBMX
LMV7239QM7/NOPB	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C42
LMV7239QM7/NOPB.A	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C42
LMV7239QM7X/NOPB	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C42
LMV7239QM7X/NOPB.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	C42

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LMV7239-Q1 :

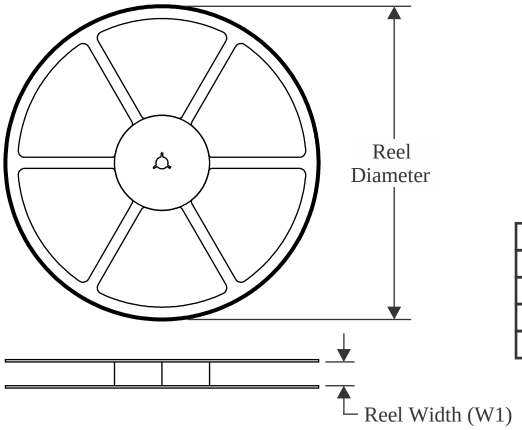
- Catalog : LMV7239

NOTE: Qualified Version Definitions:

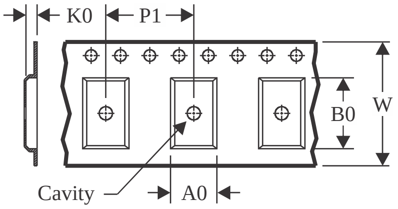
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

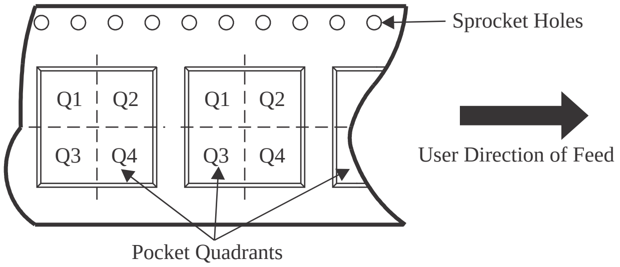


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

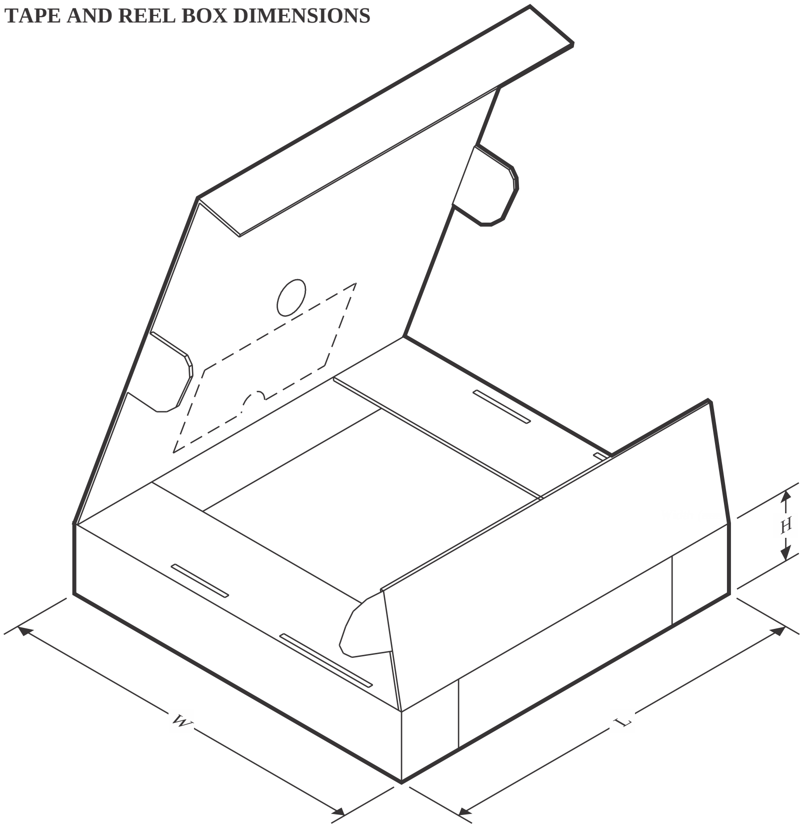
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

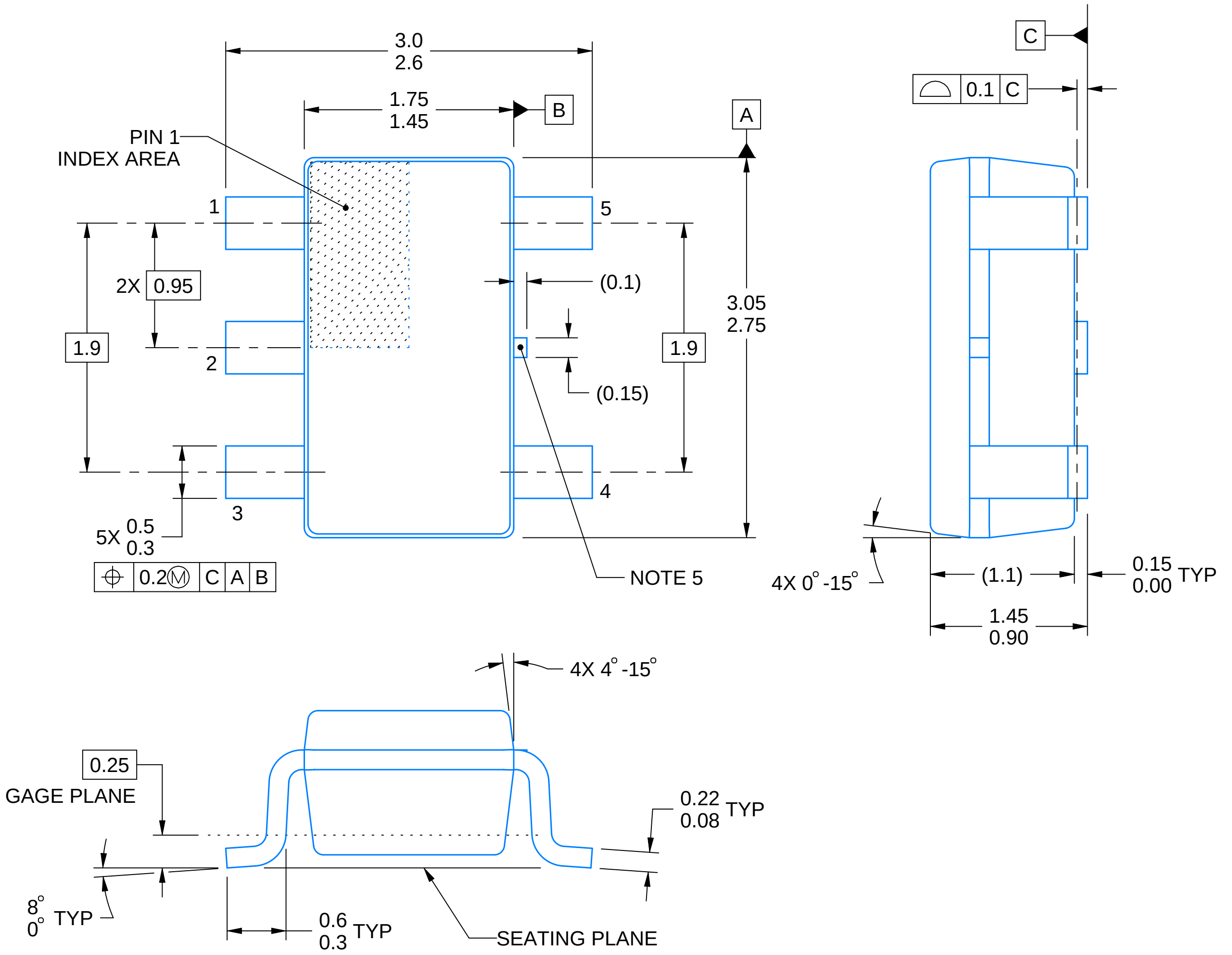
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7239QDBVRQ1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239QM7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239QM7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



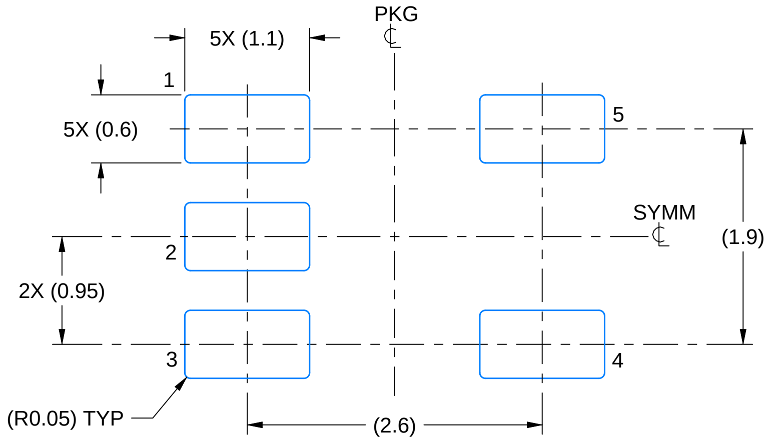
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7239QDBVRQ1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV7239QM7/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV7239QM7X/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0

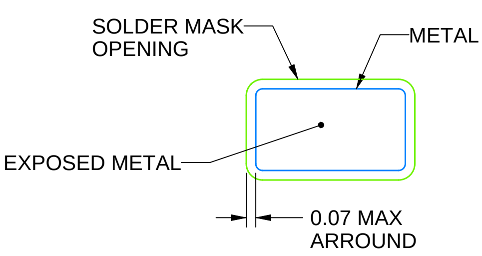


NOTES:

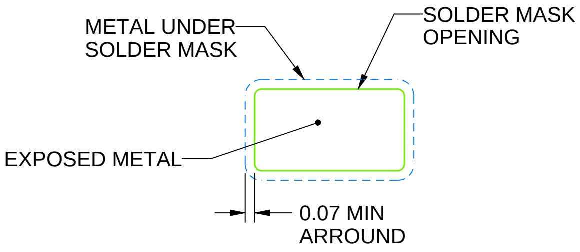
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)



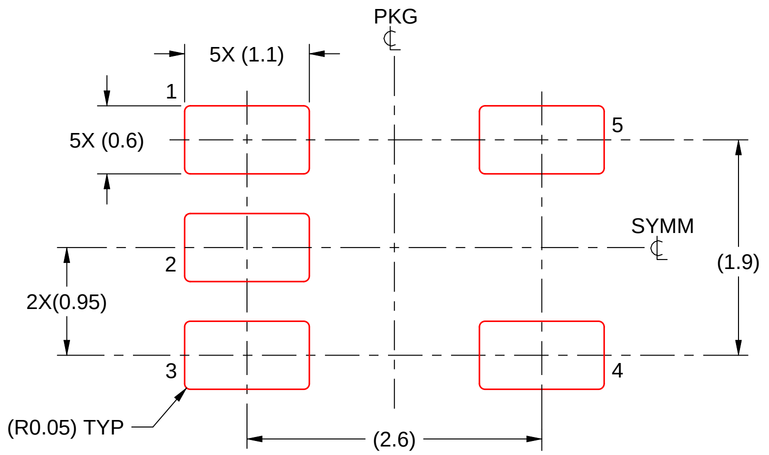
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

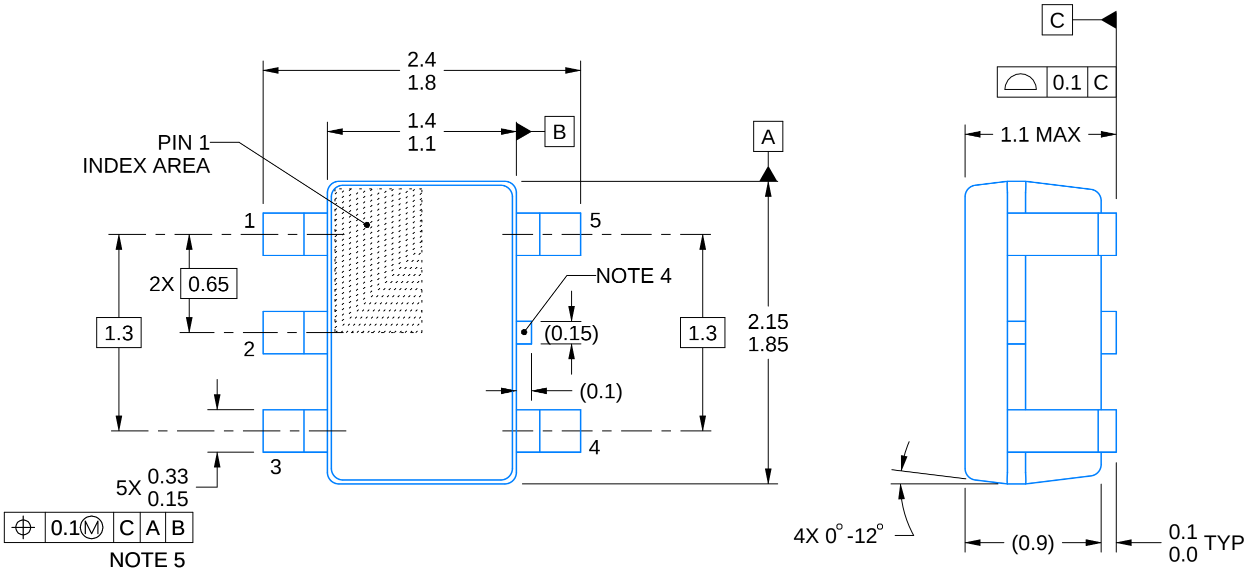
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

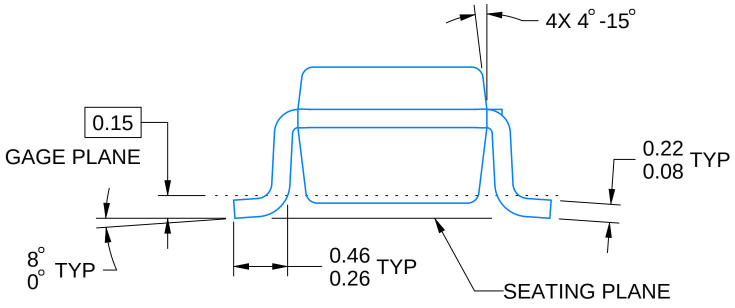
DCK0005A

PACKAGE OUTLINE

SOT - 1.1 max height

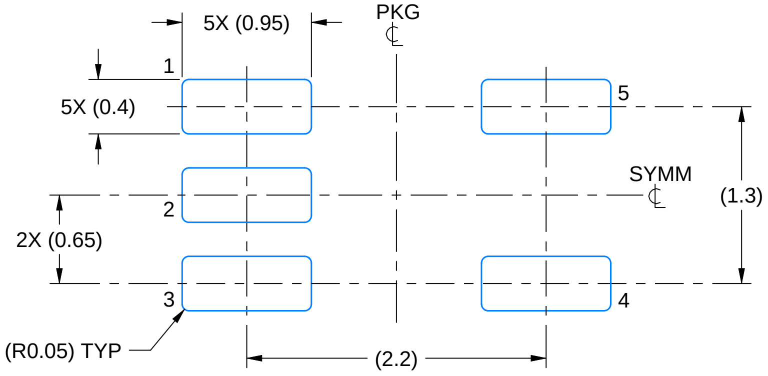
SMALL OUTLINE TRANSISTOR



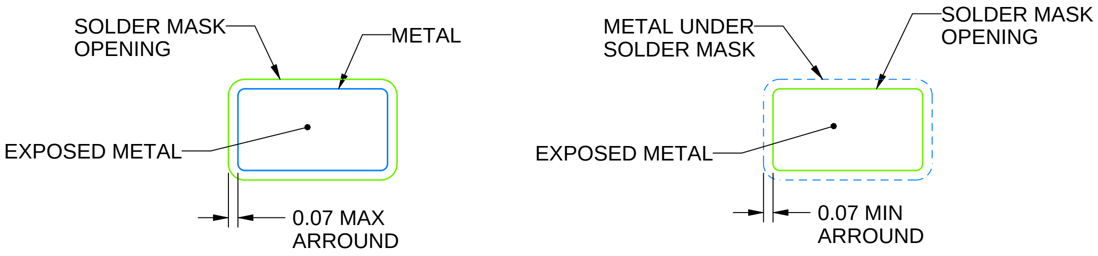


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



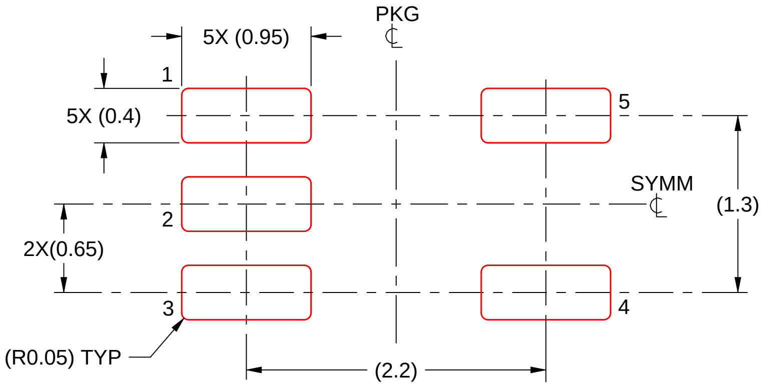
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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