LMV861/LMV862 30 MHz Low Power CMOS, EMI Hardened Operational Amplifiers

Check for Samples: LMV861, LMV862

FEATURES

Unless Otherwise Noted, Typical Values at T_A = 25°C, V^+ = 3.3V

- **Supply Voltage 2.7V to 5.5V**
- **Supply Current (per Channel) 2.25 mA**
- **Input Offset Voltage 1 mV Max**
- **Input Bias Current 0.1 pA**
- **GBW 30 MHz**
- **EMIRR at 1.8 GHz 105 dB**
- **Input Noise Voltage at 1 kHz 8 nV/$\sqrt{Hz}$**
- **Slew Rate 18 V/µs**
- **Output Voltage Swing Rail-to-Rail**
- **Output Current Drive 67 mA**
- **Operating Ambient Temperature Range −40°C to 125°C**

APPLICATIONS

- **Photodiode Preamp**
- **Weight Scale Systems**
- **Filters/Buffers**
- **Medical Diagnosis Equipment**

DESCRIPTION

TI's LMV861 and LMV862 are CMOS input, low power op amp IC's, providing a low input bias current, a wide temperature range of −40°C to +125°C and exceptional performance making them robust general purpose parts. Additionally, the LMV861 and LMV862 are EMI hardened to minimize any interference so they are ideal for EMI sensitive applications.

The unity gain stable LMV861 and LMV862 feature 30 MHz of bandwidth while consuming only 2.25 mA of current per channel. These parts also maintain stability for capacitive loads as large as 200 pF. The LMV861 and LMV862 provide superior performance and economy in terms of power and space usage.

This family of parts has a maximum input offset voltage of 1 mV, a rail-to-rail output stage and an input common-mode voltage range that includes ground. Over an operating range from 2.7V to 5.5V the LMV861 and LMV862 provide a PSRR of 93 dB, and a CMRR of 93 dB. The LMV861 is offered in the space saving 5-Pin SC70 package, and the LMV862 in the 8-Pin VSSOP.

Typical Application

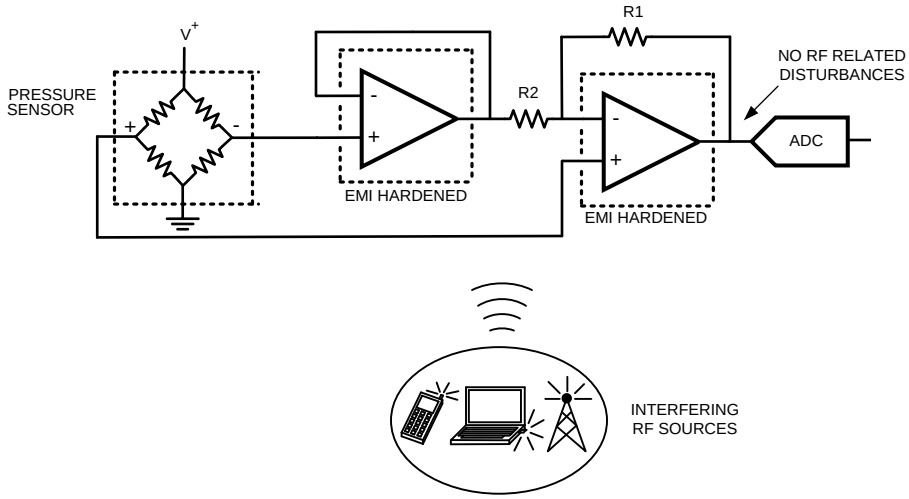

Figure 1. EMI Hardened Sensor Application

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2 kV
	Charge-Device Model	1 kV
	Machine Model	200V
V_{IN} Differential		± Supply Voltage
Supply Voltage ($V_S = V^+ – V^–$)		6V
Voltage at Input/Output Pins		V^+ +0.4V $V^–$ −0.4V
Storage Temperature Range		−65°C to +150°C
Junction Temperature(4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Temperature Range(2)		−40°C to +125°C
Supply Voltage ($V_S = V^+ – V^–$)		2.7V to 5.5V
Package Thermal Resistance (θ_{JA}(2))	5-Pin SC70	302°C/W
	8-Pin VSSOP	217°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3.3V Electrical Characteristics(1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 3.3V, $V^–$ = 0V, $V_{CM} = V^+/2$, and R_L =10 kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage(4)			±273	±1000 **1260**	µV
TCV_{OS}	Input Offset Voltage Temperature Drift(4)(5)			±0.7	±2.6	µV/°C
I_B	Input Bias Current(5)			0.1	10 **500**	pA
I_{OS}	Input Offset Current			1		pA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The typical value is calculated by applying absolute value transform to the distribution, then taking the statistical average of the resulting distribution
(5) This parameter is specified by design and/or characterization and is not tested in production.

3.3V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
CMRR	Common-Mode Rejection Ratio[4]	0.2V ≤ V_{CM} ≤ V^+ - 1.2V	77 **75**	93		dB
PSRR	Power Supply Rejection Ratio[4]	2.7V ≤ V^+ ≤ 5.5V, V_{OUT} = 1V	77 **76**	93		dB
EMIRR	EMI Rejection Ratio, IN+ and IN−[6]	V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 400 MHz		70		dB
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 900 MHz		80		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 1800 MHz		105		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 2400 MHz		110		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB	−0.1		2.1	V
A_{VOL}	Large Signal Voltage Gain[7]	R_L = 2 kΩ V_{OUT} = 0.15V to 1.65V, V_{OUT} = 3.15V to 1.65V	100 **97**	110		dB
		R_L = 10 kΩ V_{OUT} = 0.1V to 1.65V, V_{OUT} = 3.2V to 1.65V	100 **98**	113		
V_{OUT}	Output Voltage Swing High	LMV861, R_L = 2 kΩ to V^+/2		12	14 **18**	mV from either rail
		LMV862, R_L = 2 kΩ to V^+/2		12	16 **19**	
		LMV861, R_L = 10 kΩ to V^+/2		3	4 **5**	
		LMV862, R_L = 10 kΩ to V^+/2		3	6 **7**	
	Output Voltage Swing Low	LMV861, R_L = 2 kΩ to V^+/2		8	12 **16**	
		LMV862, R_L = 2 kΩ to V^+/2		10	14 **17**	
		LMV861, R_L = 10 kΩ to V^+/2		2	4 **5**	
		LMV862, R_L = 10 kΩ to V^+/2		3	7 **8**	
I_{OUT}	Output Short Circuit Current	Sourcing, V_{OUT} = V_{CM}, V_{IN} = 100 mV	61 **52**	70		mA
		Sinking, V_{OUT} = V_{CM}, V_{IN} = −100 mV	72 **58**	86		
I_S	Supply Current	LMV861		2.25	2.59 **3.00**	mA
		LMV862		4.42	5.02 **5.77**	
SR	Slew Rate[8]	A_V = +1, V_{OUT} = 1 V_{PP}, 10% to 90%		18		V/µs
GBW	Gain Bandwidth Product			30		MHz
Φ_m	Phase Margin			70		deg
e_n	Input Referred Voltage Noise Density	f = 1 kHz		8		nV/√Hz
		f = 100 kHz		5		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.015		pA/√Hz

(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).
(7) The specified limits represent the lower of the measured values for each output range condition.
(8) Number specified is the slower of positive and negative slew rates.

3.3V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
R_{OUT}	Closed Loop Output Impedance	f = 20 MHz		80		Ω
C_{IN}	Common-Mode Input Capacitance			21		pF
	Differential-Mode Input Capacitance			15		
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, BW ≥ 500 kHz		0.02		%

5V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage[4]			±273	±1000 **1260**	µV
TCV_{OS}	Input Offset Voltage Temperature Drift[4][5]			±0.7	±2.6	µV/°C
I_B	Input Bias Current[5]			0.1	10 **500**	pA
I_{OS}	Input Offset Current			1		pA
CMRR	Common-Mode Rejection Ratio[4]	0V ≤ V_{CM} ≤ V^+ –1.2V	78 **77**	94		dB
PSRR	Power Supply Rejection Ratio[4]	2.7V ≤ V^+ ≤ 5.5V, V_{OUT} = 1V	77 **76**	93		dB
EMIRR	EMI Rejection Ratio, IN+ and IN−[6]	V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 400 MHz		70		dB
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 900 MHz		80		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 1800 MHz		105		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 2400 MHz		110		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB	−0.1		3.9	V
A_{VOL}	Large Signal Voltage Gain[7]	R_L = 2 kΩ V_{OUT} = 0.15V to 2.5V, V_{OUT} = 4.85V to 2.5V	103 **100**	111		dB
		R_L = 10 kΩ V_{OUT} = 0.1V to 2.5V, V_{OUT} = 4.9V to 2.5V	103 **100**	113		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The typical value is calculated by applying absolute value transform to the distribution, then taking the statistical average of the resulting distribution
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).
(7) The specified limits represent the lower of the measured values for each output range condition.

5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for T = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OUT}	Output Voltage Swing High,	LMV861, R_L = 2 kΩ to V^+/2		13	15 **19**	mV from either rail
		LMV862, R_L = 2 kΩ to V^+/2		13	17 **20**	
		LMV861, R_L = 10 kΩ to V^+/2		3	4 **5**	
		LMV862, R_L = 10 kΩ to V^+/2		3	6 **7**	
	Output Voltage Swing Low,	LMV861, R_L = 2 kΩ to V^+/2		10	14 **18**	
		LMV862, R_L = 2 kΩ to V^+/2		12	17 **20**	
		LMV861, R_L = 10 kΩ to V^+/2		3	4 **5**	
		LMV862, R_L = 10 kΩ to V^+/2		3	7 **8**	
I_{OUT}	Output Short Circuit Current	Sourcing, V_{OUT} = V_{CM}, V_{IN} = 100 mV	90 **86**	150		mA
		Sinking, V_{OUT} = V_{CM}, V_{IN} = −100 mV	90 **86**	150		
I_S	Supply Current	LMV861		2.47	2.84 **3.27**	mA
		LMV862		4.85	5.63 **6.35**	
SR	Slew Rate[8]	A_V = +1, V_{OUT} = $2V_{PP}$, 10% to 90%		20		V/µs
GBW	Gain Bandwidth Product			31		MHz
Φ_m	Phase Margin			71		deg
e_n	Input Referred Voltage Noise Density	f = 1 kHz		8		nV/√Hz
		f = 100 kHz		5		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.015		pA/√Hz
R_{OUT}	Closed Loop Output Impedance	f = 20 MHz		60		Ω
C_{IN}	Common-Mode Input Capacitance			20		pF
	Differential-Input Capacitance			15		
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V= 1, BW ≥ 500 kHz		0.02		%

(8) Number specified is the slower of positive and negative slew rates.

Connection Diagram

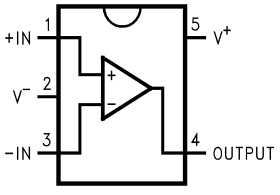

Figure 2. 5-Pin SC70 (Top View)

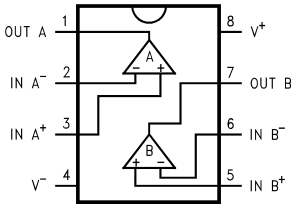

Figure 3. 8-Pin VSSOP (Top View)

Typical Performance Characteristics

At T_A = 25°C. R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, unless otherwise specified.

V_{OS} vs. V_{CM} at V^+ = 3.3V

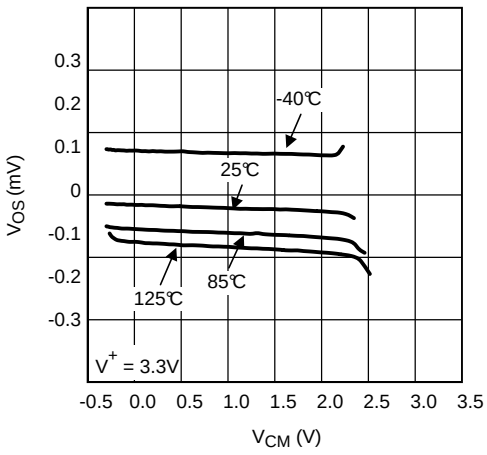

Figure 4.

V_{OS} vs. V_{CM} at V^+ = 5.0V

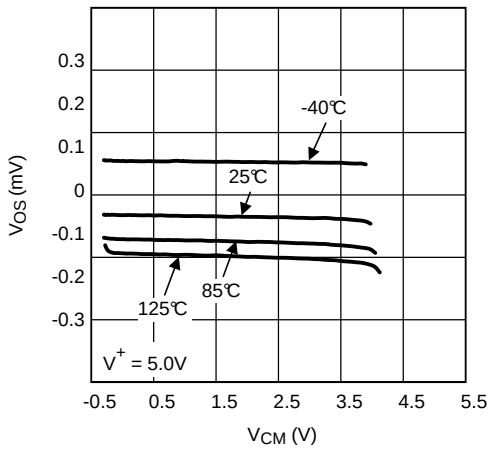

Figure 5.

V_{OS} vs. Supply Voltage

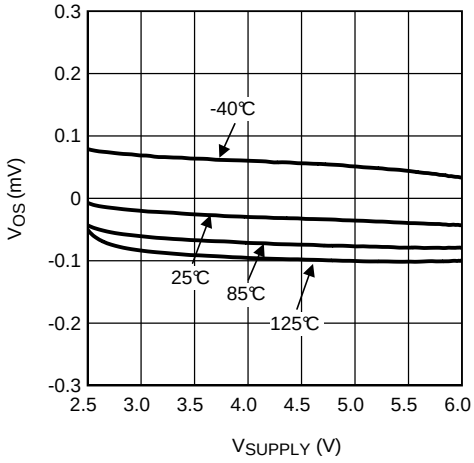

Figure 6.

V_{OS} vs. Temperature

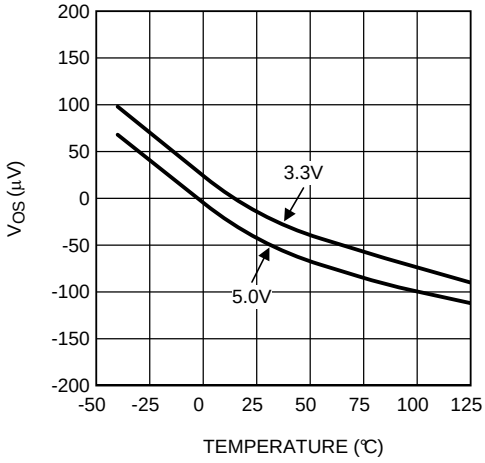

Figure 7.

V_{OS} vs. V_{OUT}

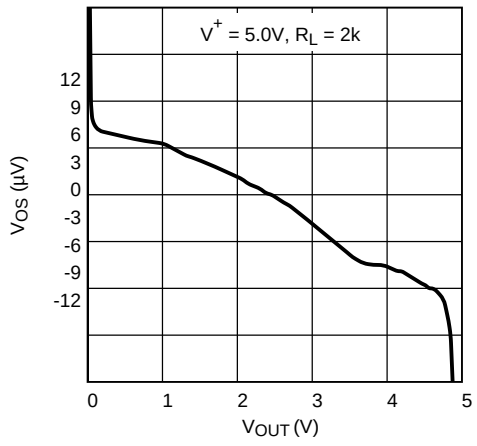

Figure 8.

Input Bias Current vs. V_{CM} at 25°C

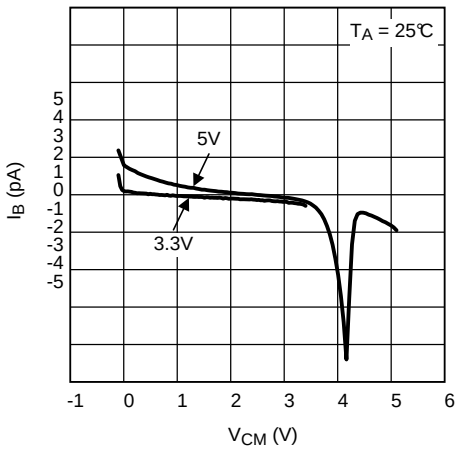

Figure 9.

Typical Performance Characteristics (continued)

At T_A = 25°C. R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, unless otherwise specified.

Input Bias Current vs. V_{CM} at 85°C

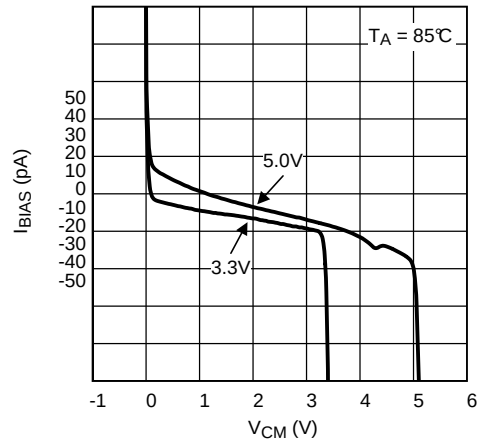

Figure 10.

Input Bias Current vs. V_{CM} at 125°C

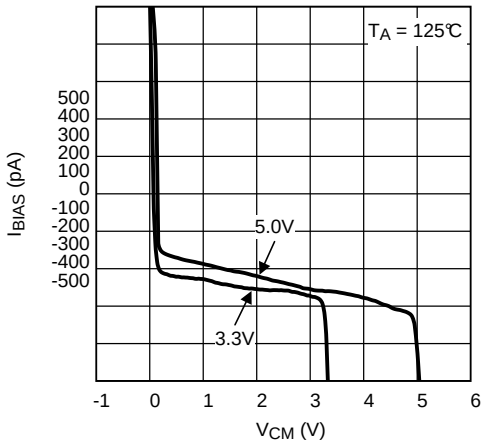

Figure 11.

Supply Current vs. Supply Voltage Single LMV861

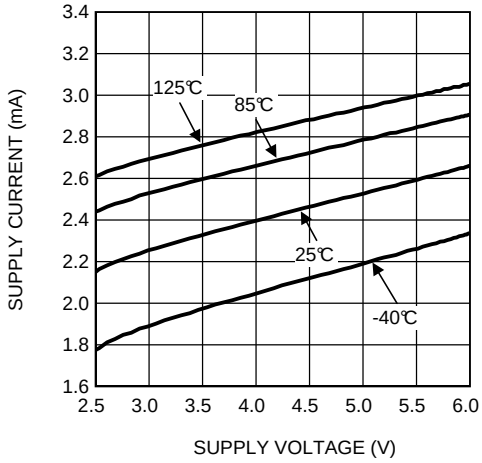

Figure 12.

Supply Current vs. Supply Voltage Dual LMV862

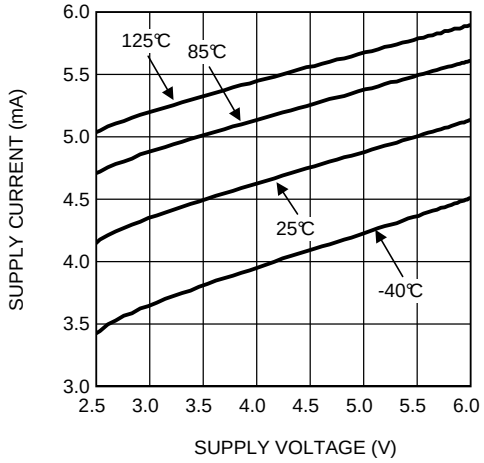

Figure 13.

Supply Current vs. Temperature Single LMV861

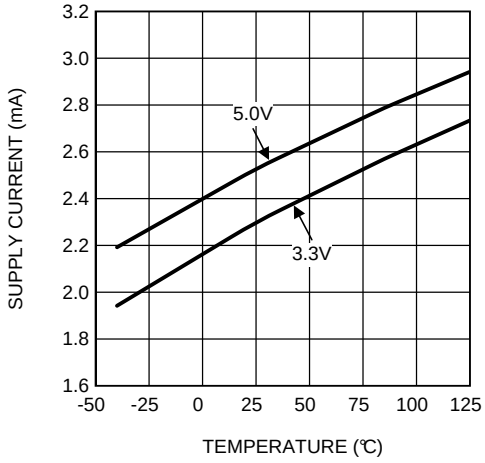

Figure 14.

Supply Current vs. Temperature Dual LMV862

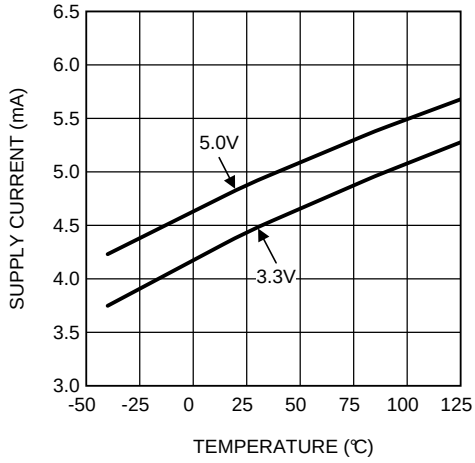

Figure 15.

Typical Performance Characteristics (continued)

At T_A = 25°C. R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, unless otherwise specified.

Sinking Current vs. Supply Voltage

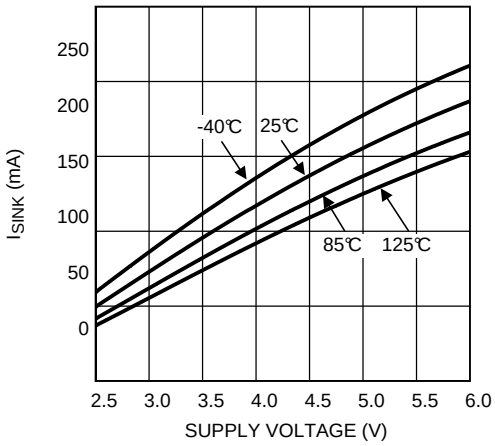

Figure 16.

Sourcing Current vs. Supply Voltage

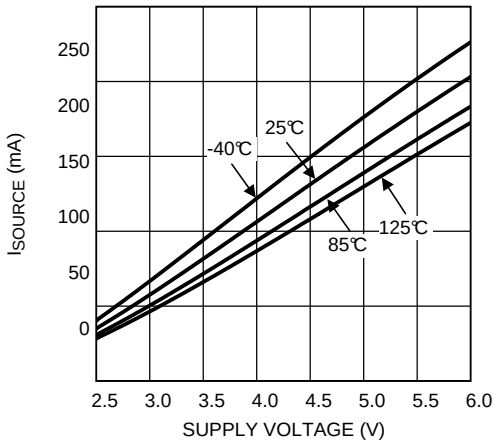

Figure 17.

Output Swing High vs. Supply Voltage R_L = 2 kΩ

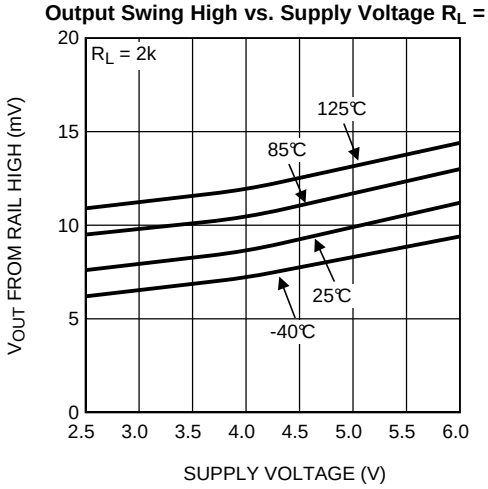

Figure 18.

Output Swing High vs. Supply Voltage R_L = 10 kΩ

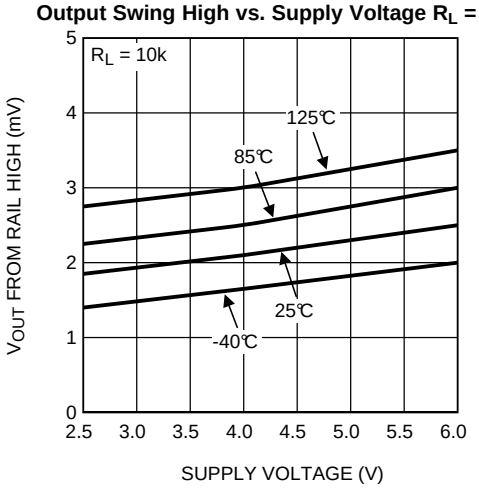

Figure 19.

Output Swing Low vs. Supply Voltage R_L = 2 kΩ

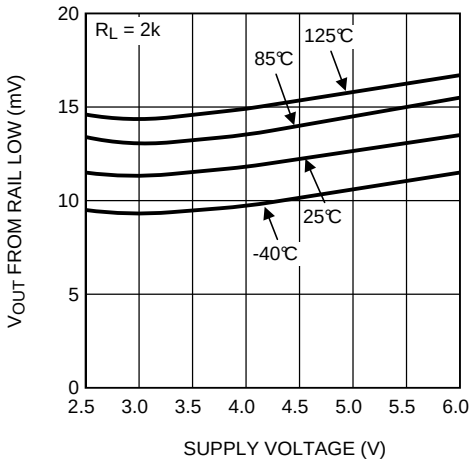

Figure 20.

Output Swing Low vs. Supply Voltage R_L = 10 kΩ

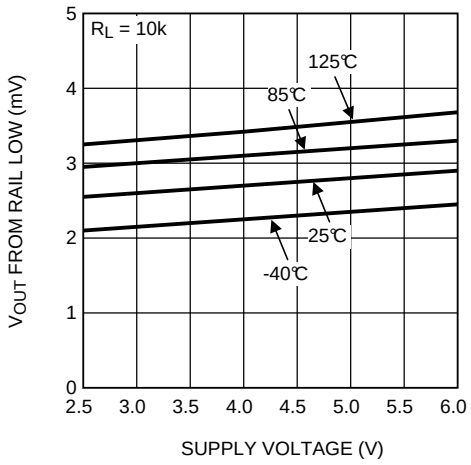

Figure 21.

Typical Performance Characteristics (continued)

At T_A = 25°C. R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, unless otherwise specified.

Output Voltage Swing vs. Load Current at V^+ = 3.3V

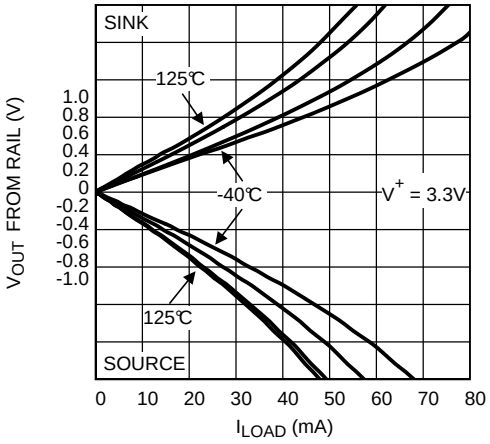

Figure 22.

Output Voltage Swing vs. Load Current at V^+ = 5.0V

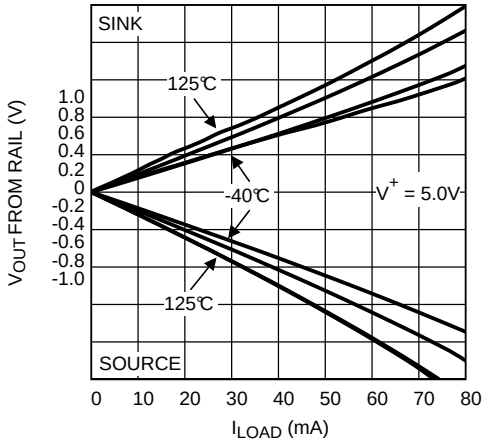

Figure 23.

Open Loop Frequency Response vs. Temperature

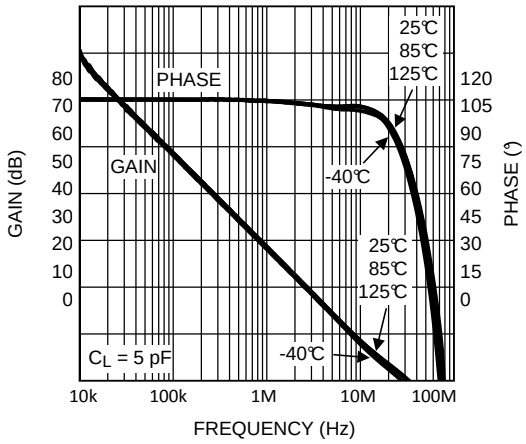

Figure 24.

Open Loop Frequency Response vs. Load Conditions

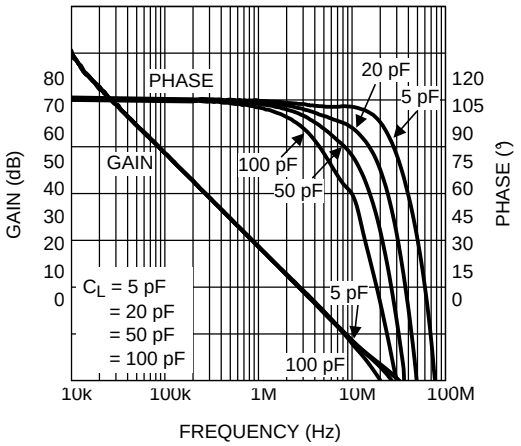

Figure 25.

Phase Margin vs. Capacitive Load

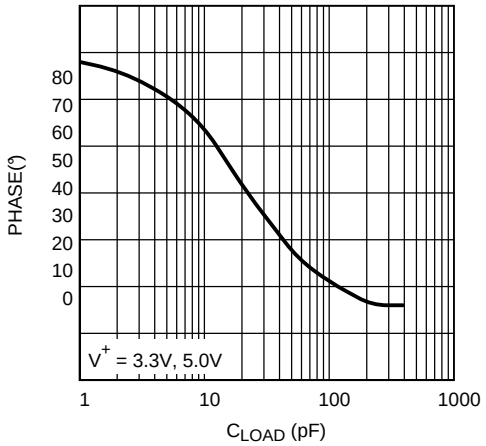

Figure 26.

PSRR vs. Frequency

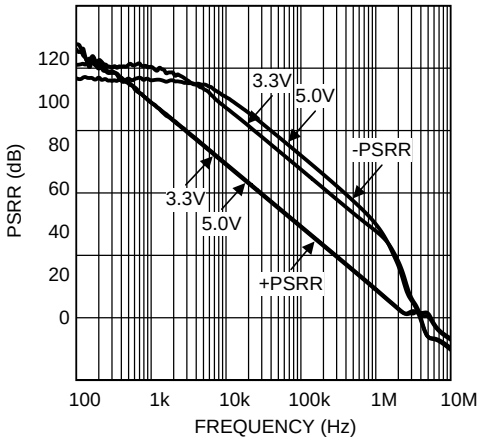

Figure 27.

Typical Performance Characteristics (continued)

At T_A = 25°C. R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, unless otherwise specified.

CMRR vs. Frequency

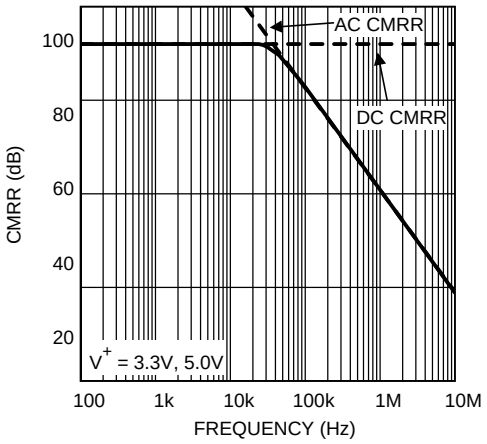

Figure 28.

Channel Separation vs. Frequency

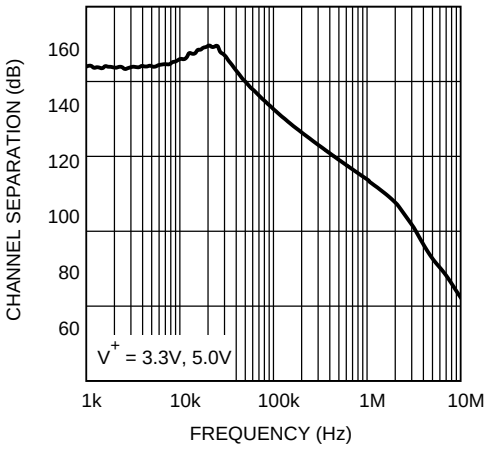

Figure 29.

Large Signal Step Response with Gain = 1

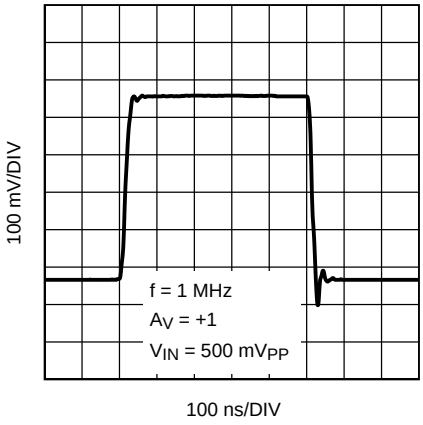

Figure 30.

Large Signal Step Response with Gain = 10

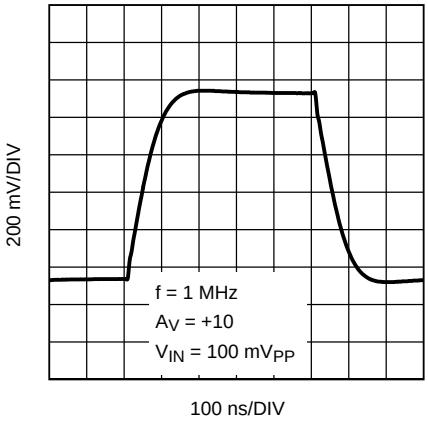

Figure 31.

Small Signal Step Response with Gain = 1

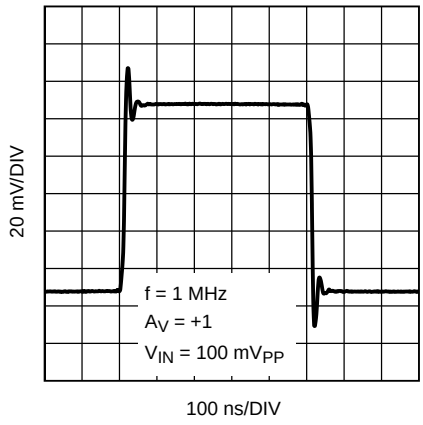

Figure 32.

Small Signal Step Response with Gain = 10

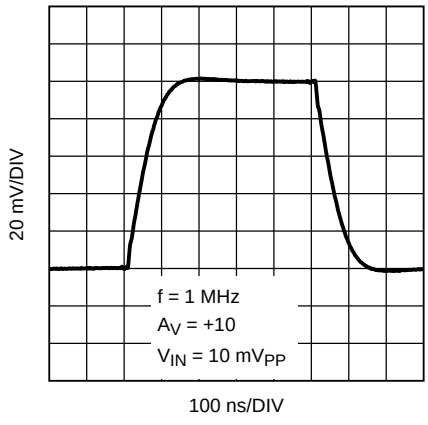

Figure 33.

Typical Performance Characteristics (continued)

At T_A = 25°C. R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, unless otherwise specified.

Slew Rate vs. Supply Voltage

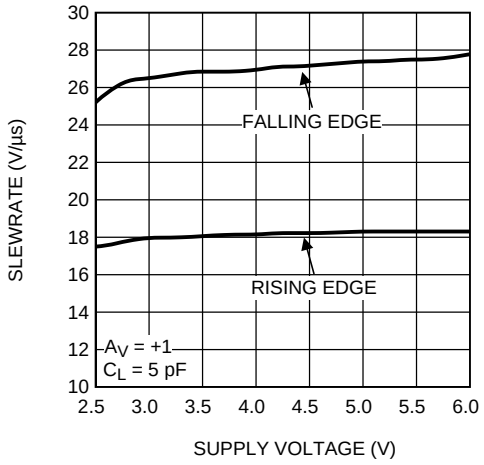

Figure 34.

Input Voltage Noise vs. Frequency

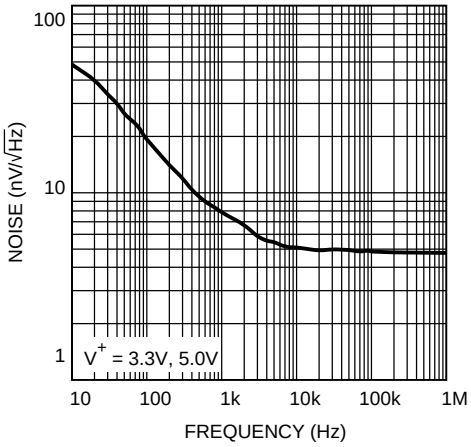

Figure 35.

THD+N vs. Frequency

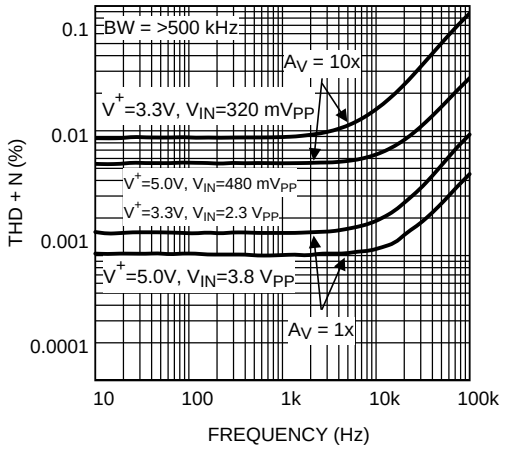

Figure 36.

THD+N vs. Amplitude

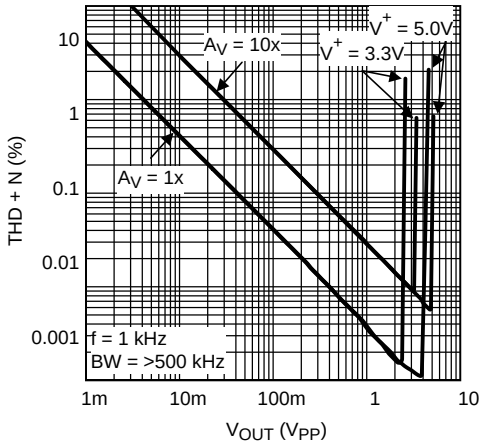

Figure 37.

R_{OUT} vs. Frequency

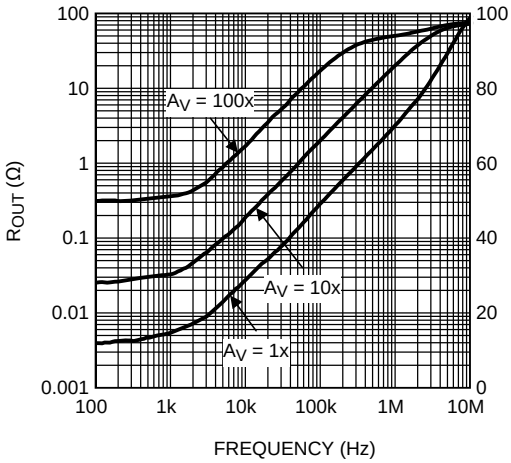

Figure 38.

EMIRR IN+ vs. Power at 400 MHz

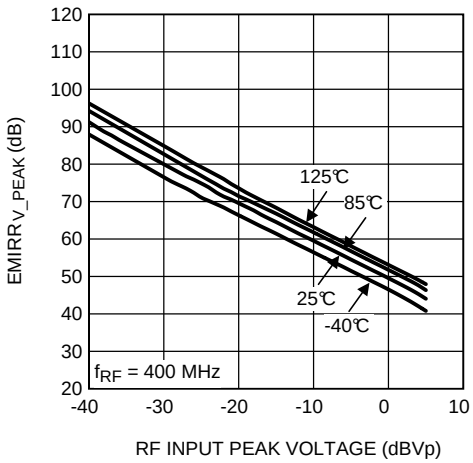

Figure 39.

Typical Performance Characteristics (continued)

At T_A = 25°C. R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, unless otherwise specified.

EMIRR IN+ vs. Power at 900 MHz

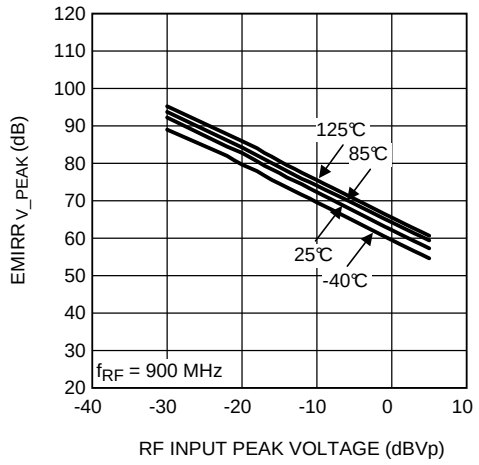

Figure 40.

EMIRR IN+ vs. Power at 1800 MHz

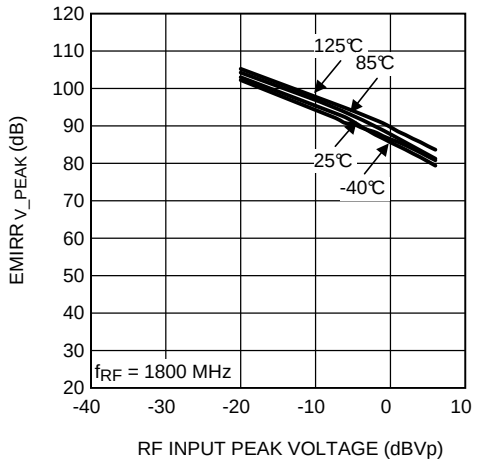

Figure 41.

EMIRR IN+ vs. Power at 2400 MHz

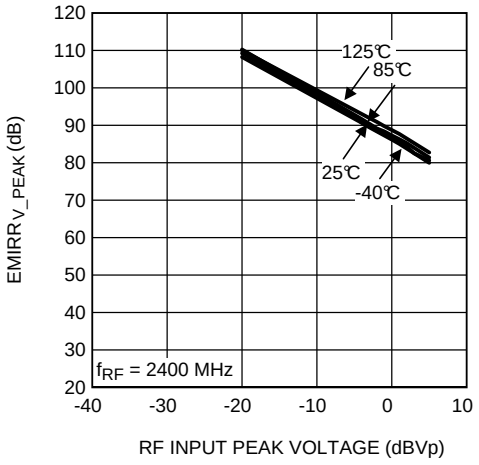

Figure 42.

EMIRR IN+ vs. Frequency

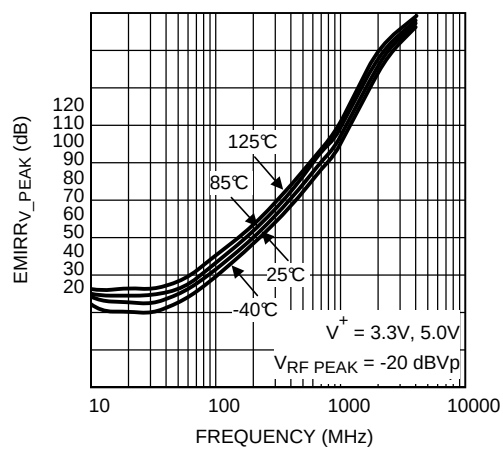

Figure 43.

APPLICATION INFORMATION

INTRODUCTION

The LMV861 and LMV862 are operational amplifiers with excellent specifications, such as low offset, low noise and a rail-to-rail output. These specifications make the LMV861 and LMV862 great choices for medical and instrumentation applications such as diagnosis equipment and power line monitors. The low supply current is perfect for battery powered equipment. The small packages, SC70 package for the LMV861, and the VSSOP package for the dual LMV862, make these parts a perfect choice for portable electronics. Additionally, the EMI hardening makes the LMV861 and LMV862 a must for almost all op amp applications. Most applications are exposed to Radio Frequency (RF) signals such as the signals transmitted by mobile phones or wireless computer peripherals. The LMV861 and LMV862 will effectively reduce disturbances caused by RF signals to a level that will be hardly noticeable. This again reduces the need for additional filtering and shielding. Using this EMI resistant series of op amps will thus reduce the number of components and space needed for applications that are affected by EMI, and will help applications, not yet identified as possible EMI sensitive, to be more robust for EMI.

INPUT CHARACTERISTICS

The input common mode voltage range of the LMV861 and LMV862 includes ground, and can even sense well below ground. The CMRR level does not degrade for input levels up to 1.2V below the supply voltage. For a supply voltage of 5V, the maximum voltage that should be applied to the input for best CMRR performance is thus 3.8V.

When not configured as unity gain, this input limitation will usually not degrade the effective signal range. The output is rail-to-rail and therefore will introduce no limitations to the signal range.

The typical offset is only 0.273 mV, and the TCV_{OS} is 0.7 µV/°C, specifications close to precision op amps.

CMRR MEASUREMENT

The CMRR measurement results may need some clarification. This is because different setups are used to measure the AC CMRR and the DC CMRR.

The DC CMRR is derived from ΔV_{OS} versus ΔV_{CM}. This value is stated in the tables, and is tested during production testing. The AC CMRR is measured with the test circuit shown in Figure 44.

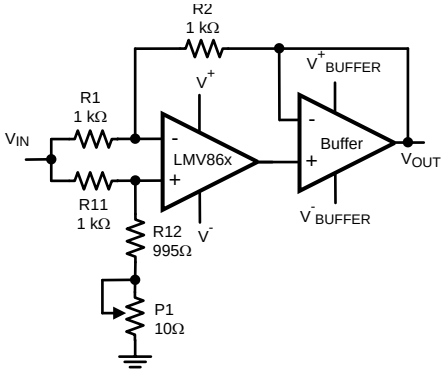

Figure 44. AC CMRR Measurement Setup

The configuration is largely the usually applied balanced configuration. With potentiometer P1, the balance can be tuned to compensate for the DC offset in the DUT. The main difference is the addition of the buffer. This buffer prevents the open-loop output impedance of the DUT from affecting the balance of the feedback network. Now the closed-loop output impedance of the buffer is a part of the balance. But as the closed-loop output impedance is much lower, and by careful selection of the buffer also has a larger bandwidth, the total effect is that the CMRR of the DUT can be measured much more accurately. The differences are apparent in the larger measured bandwidth of the AC CMRR.

One artifact from this test circuit is that the low frequency CMRR results appear higher than expected. This is because in the AC CMRR test circuit the potentiometer is used to compensate for the DC mismatches. So, mainly AC mismatch is all that remains. Therefore, the obtained DC CMRR from this AC CMRR test circuit tends to be higher than the actual DC CMRR based on DC measurements.

The CMRR curve in Figure 45 shows a combination of the AC CMRR and the DC CMRR.

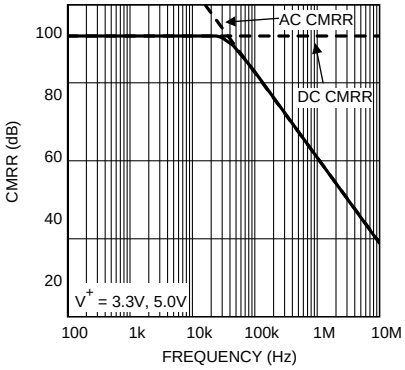

Figure 45. CMRR Curve

OUTPUT CHARACTERISTICS

As already mentioned the output is rail-to-rail. When loading the output with a 10 kΩ resistor the maximum swing of the output is typically 3 mV from the positive and negative rail.

The output of the LMV861 and LMV862 can drive currents up to 70 mA at 3.3V, and even up to 150 mA at 5V.

The LMV861 and LMV862 can be connected as non-inverting unity gain amplifiers. This configuration is the most sensitive to capacitive loading. The combination of a capacitive load placed at the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating. The LMV861 and LMV862 can directly drive capacitive loads up to 200 pF without any stability issues. In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 46. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

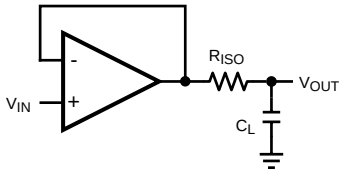

Figure 46. Isolating Capacitive Load

A resistor value of around 50Ω would be sufficient. As an example some values are given in the following table, for 5V and an open loop gain of 111 dB.

C_{LOAD}	R_{ISO}
300 pF	62Ω
400 pF	55Ω
500 pF	50Ω

When increasing the closed-loop gain the capacitive load can be increased even further. With a closed loop gain of 2 and a 27Ω isolation resistor, the load can be 1 nF

EMIRR

With the increase of RF transmitting devices in the world, the electromagnetic interference (EMI) between those devices and other equipment becomes a bigger challenge. The LMV861 and LMV862 are EMI hardened op amps which are specifically designed to overcome electromagnetic interference. Along with EMI hardened op amps, the EMIRR parameter is introduced to unambiguously specify the EMI performance of an op amp. This section presents an overview of EMIRR. A detailed description on this specification for EMI hardened op amps can be found in Application Note AN-1698.

The dimensions of an op amp IC are relatively small compared to the wavelength of the disturbing RF signals. As a result the op amp itself will hardly receive any disturbances. The RF signals interfering with the op amp are dominantly received by the PCB and wiring connected to the op amp. As a result the RF signals on the pins of the op amp can be represented by voltages and currents. This representation significantly simplifies the unambiguous measurement and specification of the EMI performance of an op amp.

RF signals interfere with op amps via the non-linearity of the op amp circuitry. This non-linearity results in the detection of the so called out-of-band signals. The obtained effect is that the amplitude modulation of the out-of-band signal is downconverted into the base band. This base band can easily overlap with the band of the op amp circuit. As an example Figure 47 depicts a typical output signal of a unity-gain connected op amp in the presence of an interfering RF signal. Clearly the output voltage varies in the rhythm of the on-off keying of the RF carrier.

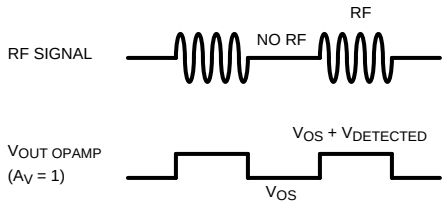

Figure 47. Offset voltage variation due to an interfering RF signal

EMIRR Definition

To identify EMI hardened op amps, a parameter is needed that quantitatively describes the EMI performance of op amps. A quantitative measure enables the comparison and the ranking of op amps on their EMI robustness. Therefore the EMI Rejection Ratio (EMIRR) is introduced. This parameter describes the resulting input-referred offset voltage shift of an op amp as a result of an applied RF carrier (interference) with a certain frequency and level. The definition of EMIRR is given by:

$$EMIRR_{V_{RF\_PEAK}} = 20 \log \left(\frac{V_{RF\_PEAK}}{\Delta V_{OS}} \right) \quad (1)$$

where

- V_{RF_PEAK} is the amplitude of the applied un-modulated RF signal (V)
- ΔV_{OS} is the resulting input-referred offset voltage shift (V)

The offset voltage depends quadratically on the applied RF level, and therefore, the RF level at which the EMIRR is determined should be specified. The standard level for the RF signal is 100 mV_P. Application Note AN-1698 addresses the conversion of an EMIRR measured for an other signal level than 100 mV_P. The interpretation of the EMIRR parameter is straightforward. When two op amps have EMIRRs which differ by 20 dB, the resulting error signals when used in identical configurations, differs by 20 dB as well. So, the higher the EMIRR, the more robust the op amp.

Coupling an RF Signal to the IN+ Pin

Each of the op amp pins can be tested separately on EMIRR. In this section the measurements on the IN+ pin (which, based on symmetry considerations, also apply to the IN- pin) are discussed. In Application Note AN-1698 the other pins of the op amp are treated as well. For testing the IN+ pin the op amp is connected in the unity gain configuration. Applying the RF signal is straightforward as it can be connected directly to the IN+ pin. As a result the RF signal path has a minimum of components that might affect the RF signal level at the pin. The circuit diagram is shown in Figure 48. The PCB trace from RF_{IN} to the IN+ pin should be a 50Ω stripline in order to match the RF impedance of the cabling and the RF generator. On the PCB a 50Ω termination is used. This 50Ω resistor is also used to set the bias level of the IN+ pin to ground level. For determining the EMIRR, two measurements are needed: one is measuring the DC output level when the RF signal is off; and the other is measuring the DC output level when the RF signal is switched on. The difference of the two DC levels is the output voltage shift as a result of the RF signal. As the op amp is in the unity gain configuration, the input referred offset voltage shift corresponds one-to-one to the measured output voltage shift.

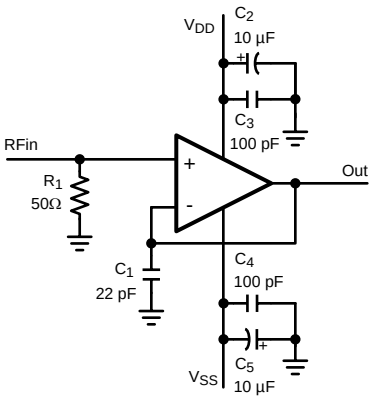

Figure 48. Circuit for coupling the RF signal to IN+

Cell Phone Call

The effect of electromagnetic interference is demonstrated in a setup where a cell phone interferes with a pressure sensor application. The application is show in Figure 50.

This application needs two op amps and therefore a dual op amp is used. The op amp configured as a buffer and connected at the negative output of the pressure sensor prevents the loading of the bridge by resistor R2. The buffer also prevents the resistors of the sensor from affecting the gain of the following gain stage. The op amps are placed in a single supply configuration.

The experiment is performed on two different op amps: a typical standard op amp and the LMV862, EMI hardened dual op amp. A cell phone is placed on a fixed position a couple of centimeters from the op amps in the sensor circuit.

When the cell phone is called, the PCB and wiring connected to the op amps receive the RF signal. Subsequently, the op amps detect the RF voltages and currents that end up at their pins. The resulting effect on the output of the second op amp is shown in Figure 49.

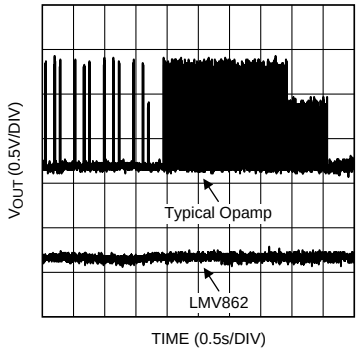

Figure 49. Comparing EMI Robustness

The difference between the two types of op amps is clearly visible. The typical standard dual op amp has an output shift (disturbed signal) larger than 1V as a result of the RF signal transmitted by the cell phone. The LMV862, EMI hardened op amp does not show any significant disturbances. This means that the RF signal will not disturb the signal entering the ADC when using the LMV862.

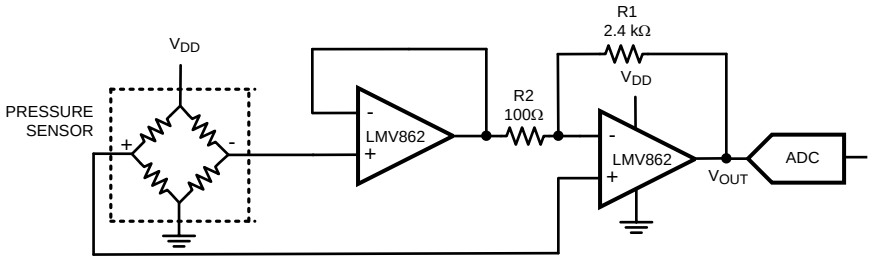

Figure 50. Pressure Sensor Application

DECOUPLING AND LAYOUT

Care must be given when creating a board layout for the op amp. For decoupling the supply lines it is suggested that 10 nF capacitors be placed as close as possible to the op amp. For single supply, place a capacitor between V^+ and V^-. For dual supplies, place one capacitor between V^+ and the board ground, and a second capacitor between ground and V^-.

Even with the LMV861 and LMV862 inherent hardening against EMI, it is still recommended to keep the input traces short and as far as possible from RF sources. Then the RF signals entering the chip are as low as possible, and the remaining EMI can be, almost, completely eliminated in the chip by the EMI reducing features of the LMV861 and LMV862.

LOAD CELL SENSOR APPLICATION

The LMV861 and LMV862 can be used for weight measuring system applications which use a load cell sensor. Examples of such systems are: bathroom weight scales, industrial weight scales and weight measurement devices on moving equipment such as forklift trucks.

The following example describes a typical load cell sensor application that can be used as a starting point for many different types of sensors and applications. Applications in environments where EMI may appear would especially benefit from the EMIRR performance of the LMV861 and LMV862.

Load Cell Characteristics

The load cell used in this example is a Wheatstone bridge. The value of the resistors in the bridge changes when pressure is applied to the sensor. This change of the resistor values will result in a differential output voltage depending on the sensitivity of the sensor, the used supply voltage and the applied pressure. The difference between the output at full scale pressure and the output at zero pressure is defined as the span of the load cell. A typical value for the span is 10 mV/V.

The circuit configuration should be chosen such that loading of the sensor is prevented. Loading of the resistor bridge due to the circuit following the sensor, could result in incorrect output voltages of the sensor.

Load Cell Example

Figure 51 shows a typical schematic for a load cell application. It uses a single supply and has an adjustment for both positive and negative offset of the load cell. An ADC converts the amplified signal to a digital signal.

The op amps A1 and A2 are configured as buffers, and are connected at both the positive and the negative output of the load cell. This is to prevent the loading of the resistor bridge in the sensor by the resistors configuring the differential op amp circuit (op amp A4). The buffers also prevent the resistors of the sensor from affecting the gain of the following gain stage. The third buffer (A3) is used to create a reference voltage, to correct for the offset in the system.

Given the differential output voltage V_S of the load cell, the output signal of this op amp configuration, V_{OUT}, equals:

$$V_{OUT} = \frac{R3}{R1} \times V_{SENSE} + \left(\frac{R3}{R5} + 1 \right) \times V_{REF} - \frac{R3}{R5} \times V_{DD} \quad (2)$$

To align the pressure range with the full range of an ADC the correct gain needs to be set. To calculate the correct gain, the power supply voltage and the span of the load cell are needed. For this example a power supply of 5V is used and the span of the sensor, in this case a 125 kg sensor, is 100 mV. With the configuration as shown in Figure 51, this signal is covering almost the full input range of the ADC. With no weight on the load cell, the output of the sensor and the op amp A4 will be close to 0V. With the full weight on the load cell, the output of the sensor is 100 mV, and will be amplified with the gain from the configuration. In the case of the configuration of Figure 51 the gain is R3/R1 = 51 kΩ/100Ω = 50. This will result in a maximum output of 100 mV x 50 = 5V, which covers the full range of the ADC.

For further processing the digital signal can be processed by a microprocessor following the ADC, this can be used to display or log the weight on the load cell. To get a resolution of 0.5 kg, the LSB of the ADC should be smaller then 0.5 kg/125 kg = 1/1000. A 12-bit ADC would be sufficient as this gives 4096 steps. A 12-bit ADC such as the two channel 12-bit ADC122S021 can be used for this application.

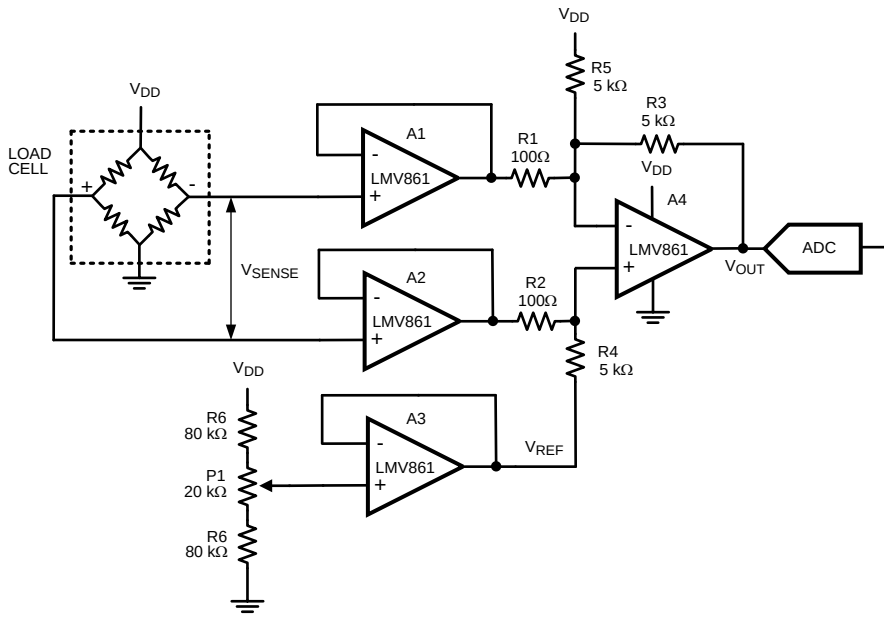

Figure 51. Load Cell Application

IR PHOTODIODE APPLICATION

The LMV861 and LMV862 are also very good choices to be used in photodiode applications, such as IR communication, monitoring, etc. The large bandwidth of the LMV861 and LM862 makes it possible to create high speed detection. This, together with the low noise, makes the LMV861 and LMV862 ideal for medical applications such as fetal monitors and bed side monitors. Another application where the LMV861 and LMV862 would fit perfectly is a bill validator, an instrument to detect counterfeit bank notes. The following example describes an application that can be used for different types of photodiode sensors and applications.

IR Photodiode Example

The circuit shown in Figure 53 is a typical configuration for the readout of a photodiode. The response of a photodiode to incoming light is a variation in the diode current. In many applications a voltage is required, i.e. when connecting to an ADC. Therefore the first step is to convert the diode signal current into a voltage by an I-V converter. In Figure 53 the left op amp is configured as an I-V converter, with a gain set by R1.

Some types of photodiodes can have a large capacitance. This could potentially lead to oscillation. The addition of resistor R2 isolates the photodiode capacitance from the feedback loop, thereby preventing the loop from oscillating.

The capacitor in between the two op amp configurations, blocks the DC component, thus removing the DC offset of the first op amp circuit, and the offset created by the ambient light entering the photodiode. The second op amp amplifies the signal to levels that can be converted to a digital signal by an ADC. To prevent floating of the input of the second op amp, resistor R5 is added. By allowing the input bias current of a few pA to flow through this resistor a stable input is ensured.

In Figure 52 a sensed and amplified signal is shown from an IR source, in this case an IR remote control.

The data from the ADC can then be used by a DSP or microprocessor for further processing.

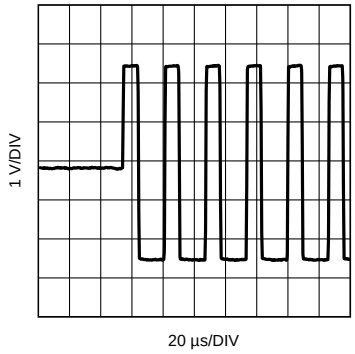

Figure 52. IR Photodiode Signal

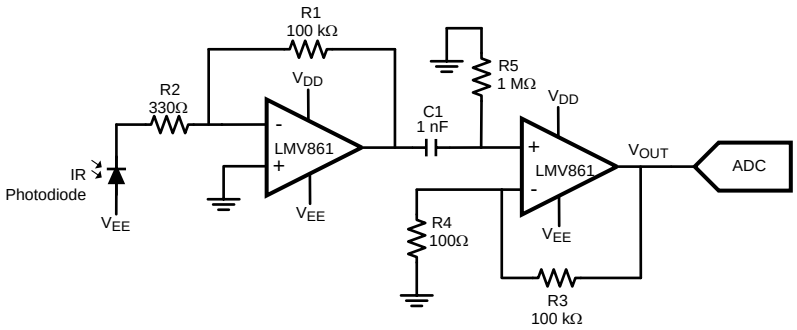

Figure 53. IR Photodiode Application

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV861MG/NOPB	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AEA
LMV861MG/NOPB.A	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AEA
LMV861MGE/NOPB	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AEA
LMV861MGE/NOPB.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AEA
LMV861MGX/NOPB	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AEA
LMV861MGX/NOPB.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AEA
LMV862MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AJ5A
LMV862MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AJ5A
LMV862MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AJ5A
LMV862MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AJ5A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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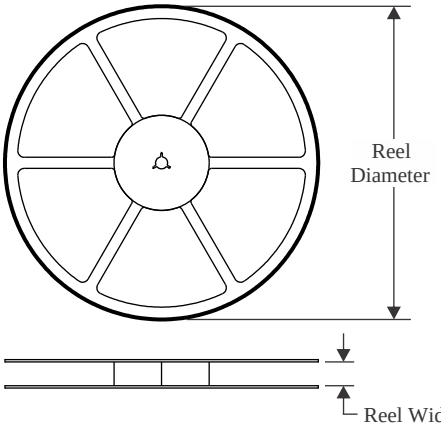
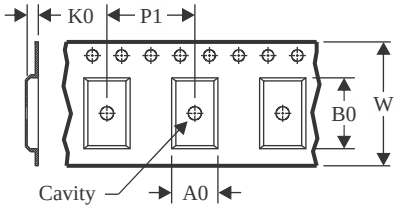
TAPE AND REEL INFORMATION

REEL DIMENSIONS

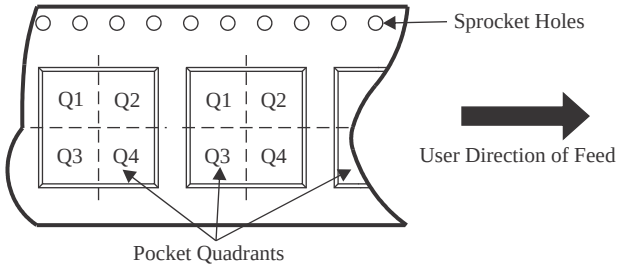


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

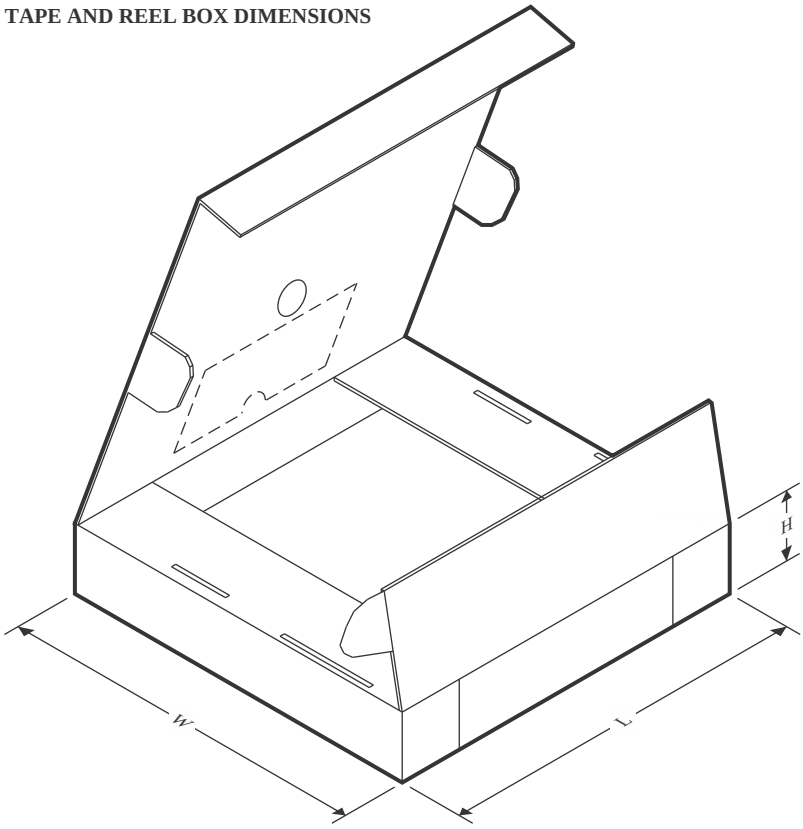
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV861MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV861MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV861MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV862MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV862MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

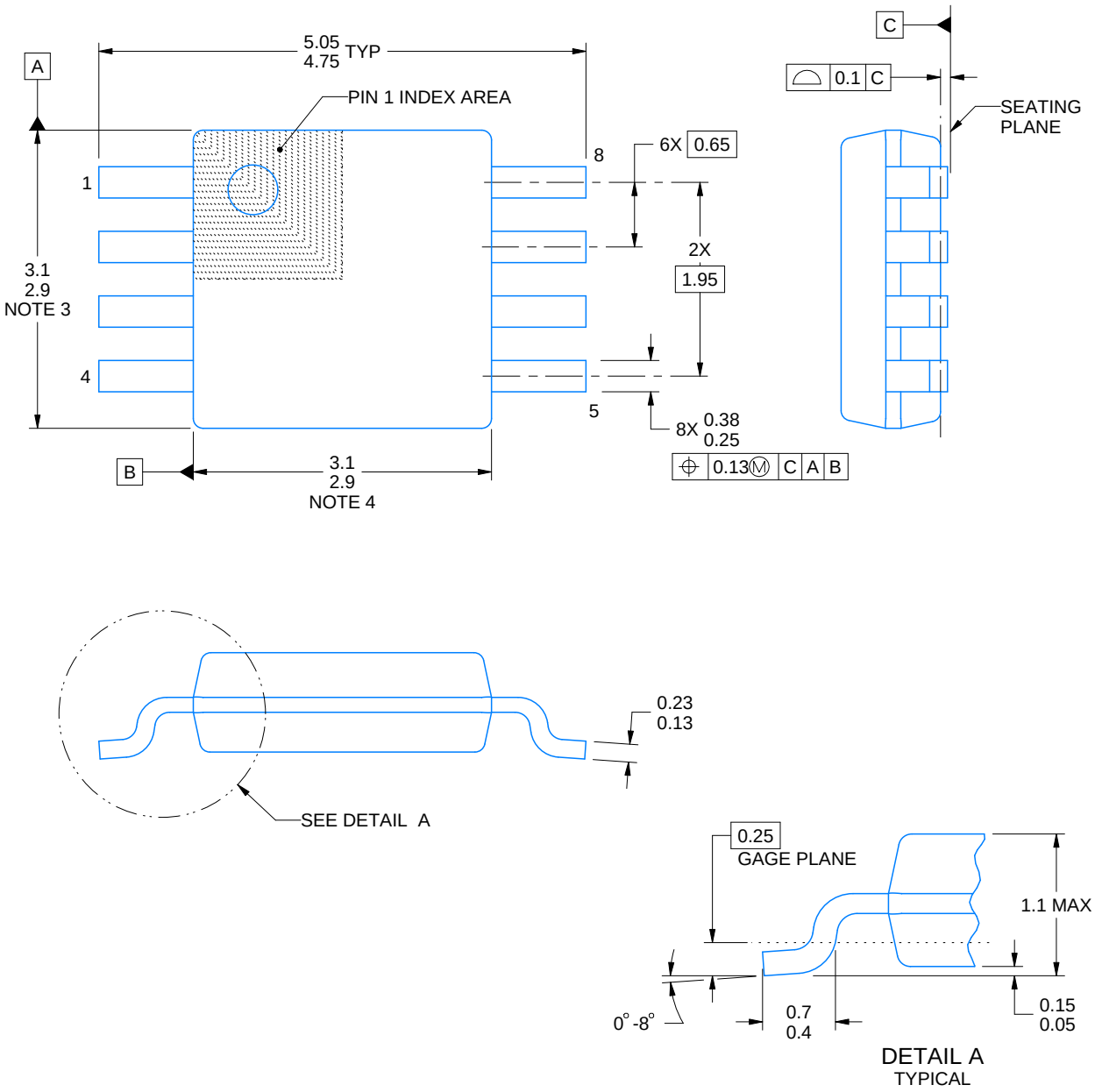
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV861MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV861MGE/NOPB	SC70	DCK	5	250	208.0	191.0	35.0
LMV861MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV862MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV862MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

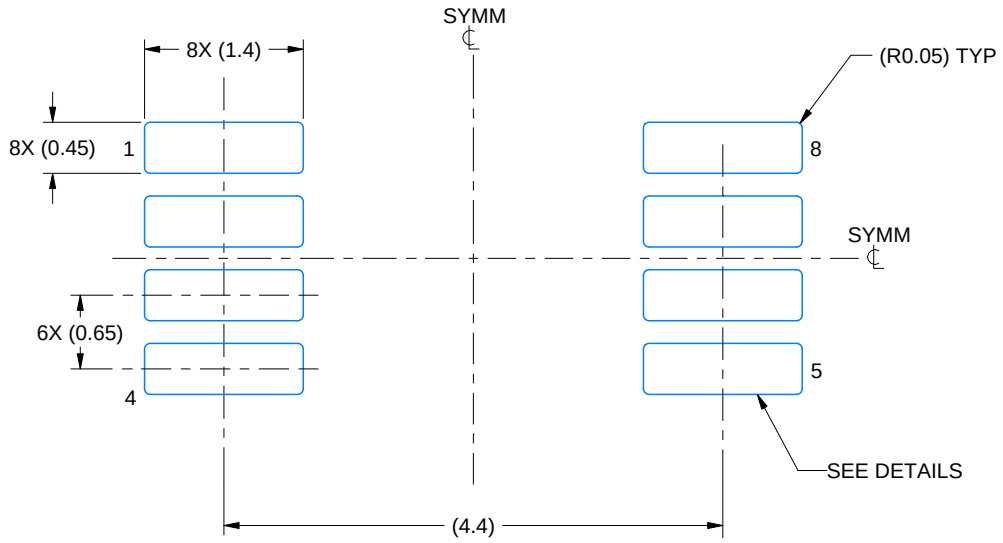
SMALL OUTLINE PACKAGE



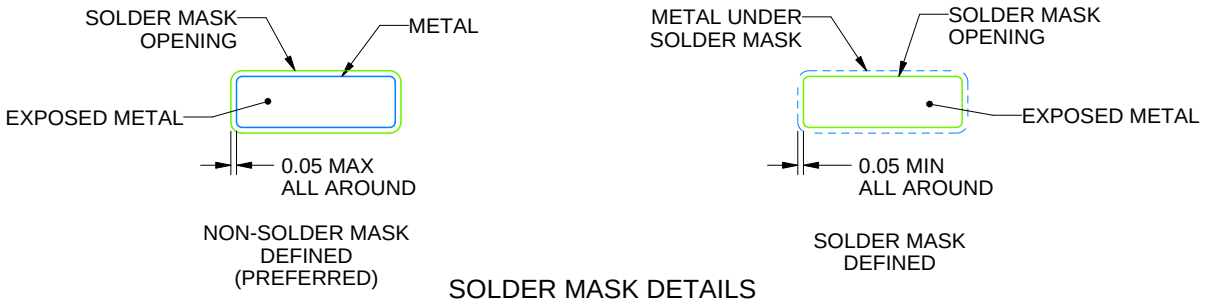
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

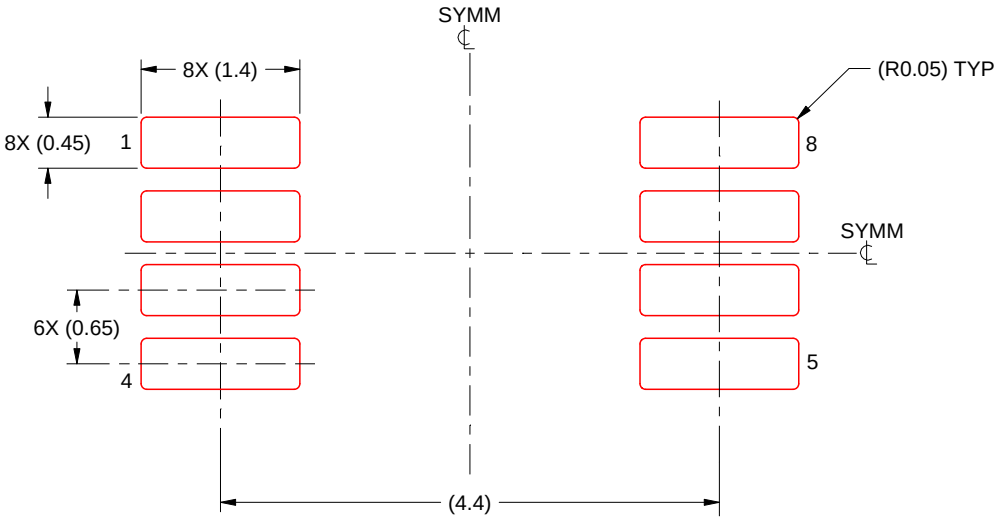


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

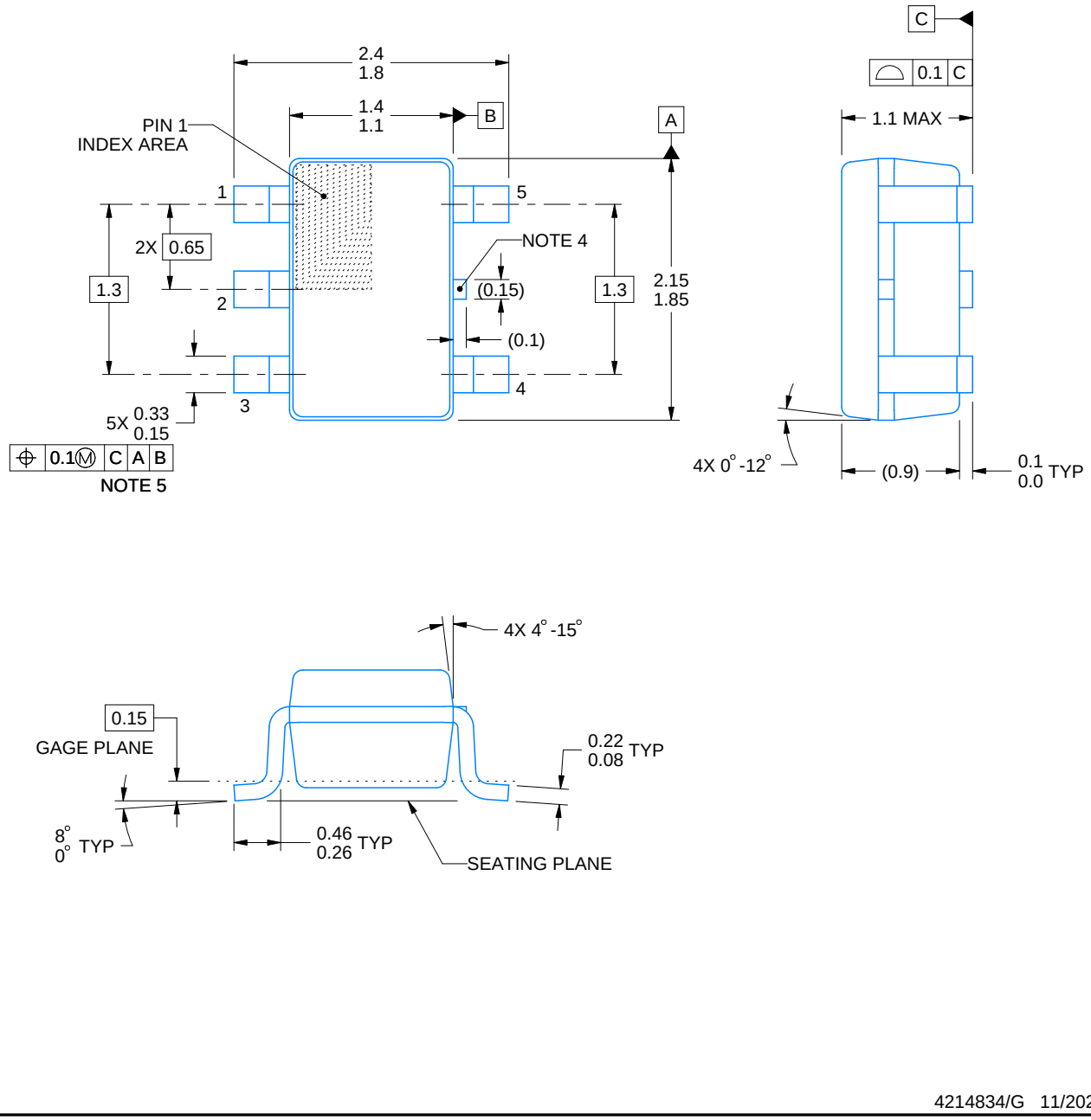
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

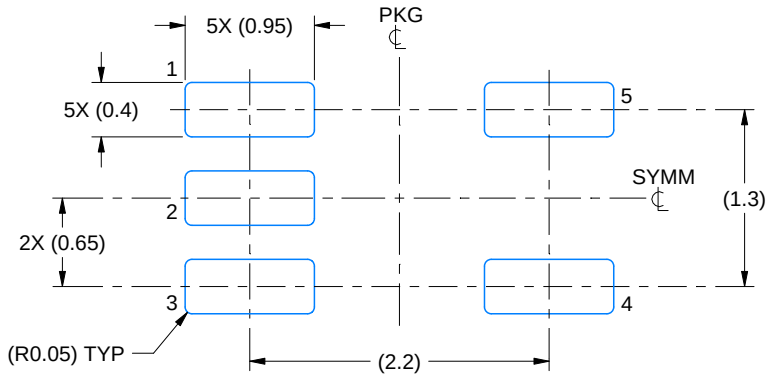
SMALL OUTLINE TRANSISTOR



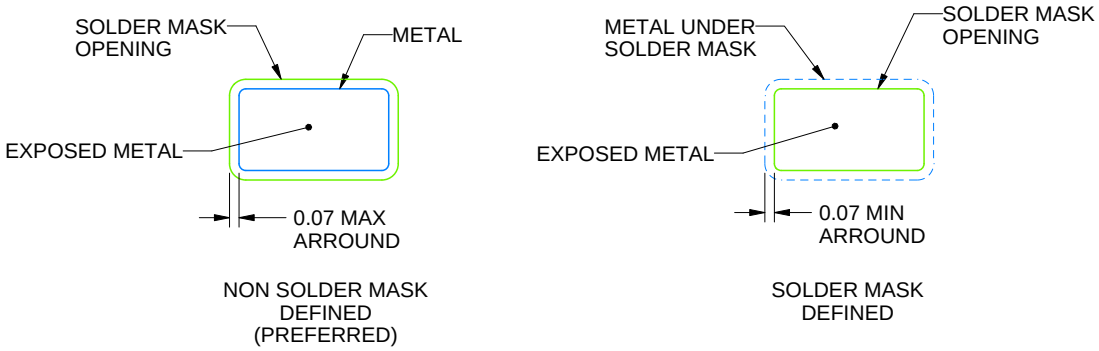
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

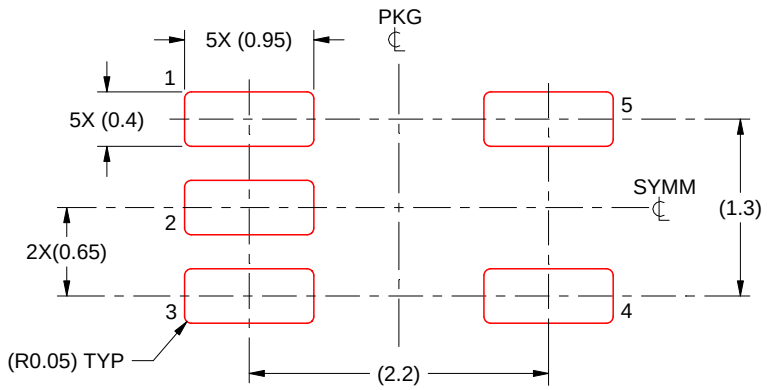


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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