LP324 LP2902 Ultra-Low-Power Quadruple Operational Amplifiers

1 Features

- Low supply current: 85µA typical
- Low offset voltage: 2mV typical
- Low input bias current: 2nA typical
- Input common mode to ground
- Wide supply voltage: 3V < V_{CC} < 32V
- Pin compatible with LM324

2 Applications

- LCD displays
- Portable instrumentation
- Sensor and metering equipment
- Consumer electronics:
  - MP3 players, toys, and more
- Power supplies

3 Description

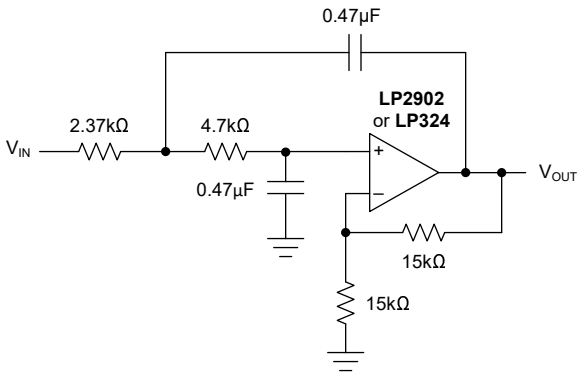
The LP324 and LP2902 are quadruple low-power operational amplifiers especially designed for battery-operated applications. Good input specifications and a wide supply-voltage range are achieved, despite the ultra-low supply current. Single-supply operation is achieved with an input common-mode range that includes ground (GND).

The LP324 and LP2902 are an excellent choice for applications where wide supply voltage and low power are more important than speed and bandwidth. These applications include portable instrumentation, LCD displays, consumer electronics (MP3 players, toys, and so forth), and power supplies.

Device Information

PART NUMBER	TEMPERATURE (T_A)	PACKAGE(1)
LP2902	−40°C to +85°C	D (SOIC, 14) N (PDIP, 14) PW (TSSOP, 14)
LP324	0°C to 70°C	

(1) For all available packages, see Section 8.



100Hz Low-Pass Filter With a Gain of 2

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

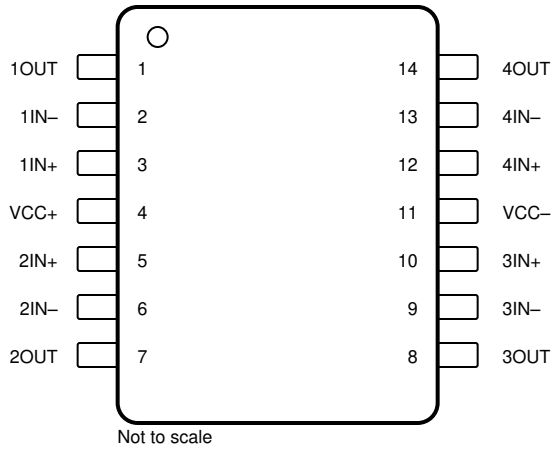


Figure 4-1. D Package, 14-Pin SOIC, N Package, 14-Pin PDIP, and PW Package, 14-Pin TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Negative input
1IN+	3	Input	Positive input
1OUT	1	Output	Output
2IN–	6	Input	Negative input
2IN+	5	Input	Positive input
2OUT	7	Output	Output
3IN–	9	Input	Negative input
3IN+	10	Input	Positive input
3OUT	8	Output	Output
4IN–	13	Input	Negative input
4IN+	12	Input	Positive input
4OUT	14	Output	Output
VCC–	11	Power	Negative (lowest) supply or ground (for single-supply operation)
VCC+	4	Power	Positive (highest) supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Single supply		32	V
		Dual supply		±16	
V_{ID}	Differential input voltage(3)			32	V
V_I	Input voltage (either input)		–0.3	32	V
	Duration of output short-circuit to ground (one amplifier) at or less than T_A = 25°C, V_{CC} ≤ 15V(4)		Unlimited		
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network ground (GND).
(3) Differential voltages are at IN+, with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±350	V

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature	LP2902	–40		85	°C
		LP324	0		70	

5.4 Thermal Information

THERMAL METRIC(1) (2)		LP2902, LP324			UNIT
		D (SOIC)	PW (TSSOP)	N (PDIP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140	154	90	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C potentially affects reliability.

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5.5 Electrical Characteristics

at T_A = 25°C, V_{CC} = 5V, V_{IC} = V_{CC} / 2, and R_L = 100kΩ connected to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage	LP2902			2	4	mV
			T_A = –40°C to +85°C			10	
		LP324			2	4	
			T_A = 0°C to 70°C			9	
dV_{IO}/dT	Input offset voltage drift	LP2902, T_A = 0°C to 70°C			10		µV/°C
		LP324, T_A = –40°C to +85°C			10		
PSRR	Power supply rejection ratio	V_{CC} = 5V to 30V		80	90		dB
			LP2902 T_A = –40°C to +85°C	75			
			LP324 T_A = 0°C to 70°C	75			
CMRR	Common-mode rejection ratio	V_{CC} = 30V, V_{IC} = 0V to V_{CC} – 1.5V		80	90		dB
			LP2902 T_A = –40°C to +85°C	75			
			LP324 T_A = 0°C to 70°C	75			
INPUT BIAS CURRENT							
I_{IB}	Input bias current	LP2902			2	20	nA
			T_A = –40°C to +85°C			40	
		LP324			2	10	
			T_A = 0°C to 70°C			20	
I_{IO}	Input offset current	LP2902			0.5	4	nA
			T_A = –40°C to +85°C			8	
		LP324			0.2	2	
			T_A = 0°C to 70°C			4	
I_{IO}/dT	Input offset current drift	LP2902			10		pA/°C
		LP324			10		
OPEN-LOOP GAIN							
A_V	Large-signal voltage gain	V_{CC} = 30V, R_L = 10kΩ to GND	LP2902	40	70		V/mV
			LP2902 T_A = –40°C to +85°C	30			
			LP324	50	100		
			LP324 T_A = 0°C to 70°C	40			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product	V_{CC} = ±15V			100		kHz
SR	Slew rate	V_{CC} = ±15V			50		V/ms
OUTPUT							
V_O	Output voltage swing	I_L = 350µA to ground, V_{IC} = 0V		3.4	3.6		V
			LP2902 T_A = –40°C to +85°C	(V_{CC}) – 1.9			
			LP324 T_A = 0°C to 70°C	(V_{CC}) – 1.9			
		I_L = 350µA to V_{CC}, V_{IC} = 0V		0.82	0.7		
			LP2902 T_A = –40°C to +85°C	1			
			LP324 T_A = 0°C to 70°C	1			

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5.5 Electrical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5V, V_{IC} = V_{CC} / 2, and R_L = 100kΩ connected to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	Output current	Source, V_O = 3V, V_{ID} = 1V		7	10		mA
			LP2902 T_A = –40°C to +85°C	4			
			LP324 T_A = 0°C to 70°C	4			
		Sink, V_O = 1.5V, V_{ID} = –1V		4	5		
			LP2902 T_A = –40°C to +85°C	3			
			LP324 T_A = 0°C to 70°C	3			
		Sink, V_O = 1.5V, V_{ID} = –1V, V_{IC} = 0V		2	4		
			LP2902 T_A = –40°C to +85°C	1			
			LP324 T_A = 0°C to 70°C	1			
I_{SC}	Short circuit current	Short to ground, V_{ID} = 1V			20	35	mA
			LP2902 T_A = –40°C to +85°C			40	
			LP324 T_A = 0°C to 70°C			40	
		Short to V_{CC}, V_{ID} = –1V			15	30	
			LP2902 T_A = –40°C to +85°C			45	
			LP324 T_A = 0°C to 70°C			45	
POWER SUPPLY							
I_{CC}	Supply current	No load			85	150	µA
			LP2902 T_A = –40°C to +85°C			275	
			LP324 T_A = 0°C to 70°C			250	

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6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2005) to Revision B (September 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Pin Configuration and Functions*, *Specifications*, *Recommended Operating Conditions*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Updated front page figure	1
• Deleted figure, *Schematic (Each Amplifier)*	2
• Deleted note 6 in *Absolute Maximum Ratings*	3
• Moved package thermal impedance information from *Absolute Maximum Ratings* to *Thermal Information*	3
• Changed human body model value from ±2kV to ±350V in *ESD Ratings*	3
• Added *Thermal Information* and updated values	3
• Deleted notes 1, 2 and 3	4
• Changed power supply rejection ratio units from V to dB (typo)	4

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2902D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LP2902
LP2902DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LP2902N
LP2902N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LP2902N
LP2902PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	LP2902
LP2902PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902
LP2902PWRE4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LP324D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LP324
LP324DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LP324
LP324DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP324N
LP324N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP324N
LP324PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	LP324
LP324PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LP324
LP324PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324
LP324PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

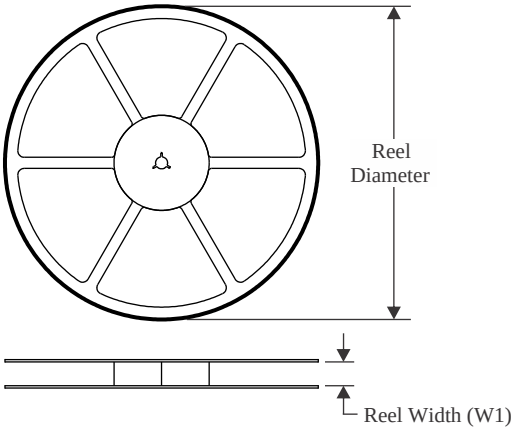
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

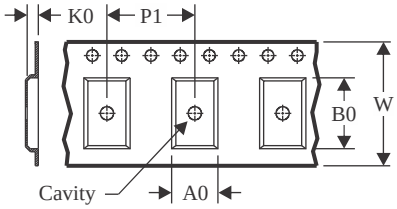
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

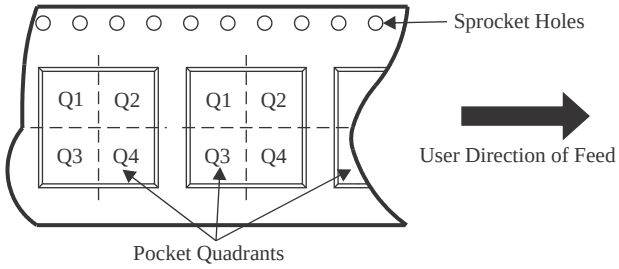


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

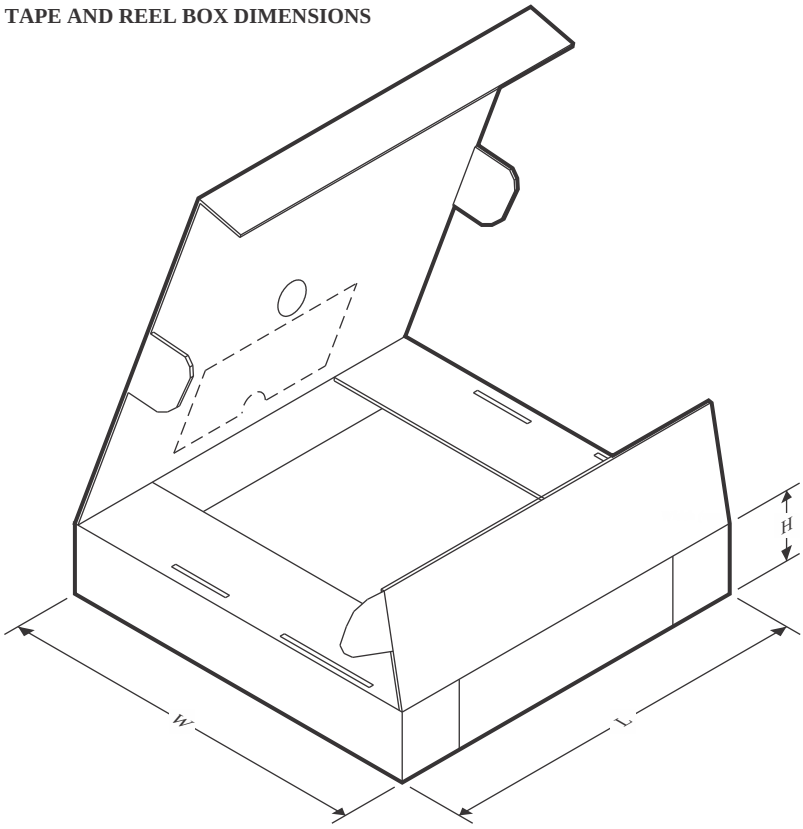
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LP2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LP324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LP324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

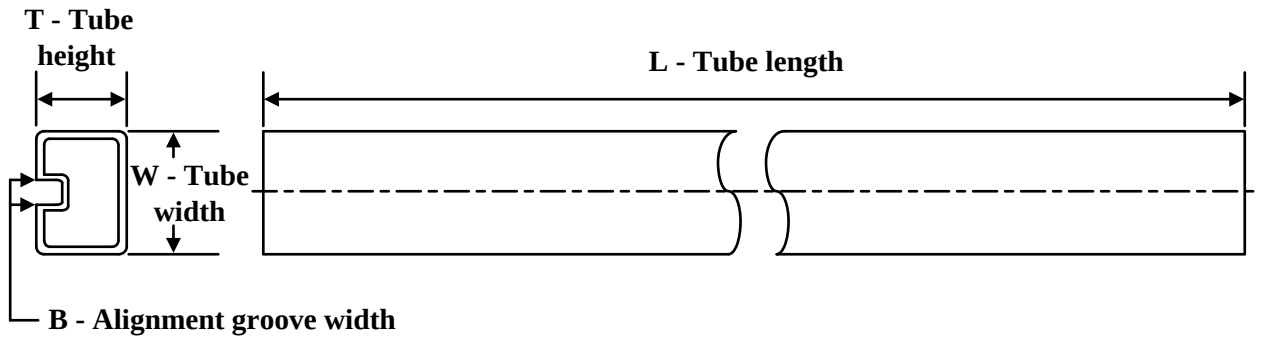
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2902DR	SOIC	D	14	2500	367.0	367.0	35.0
LP2902PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LP324DR	SOIC	D	14	2500	367.0	367.0	35.0
LP324DRG4	SOIC	D	14	2500	340.5	336.1	32.0
LP324PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



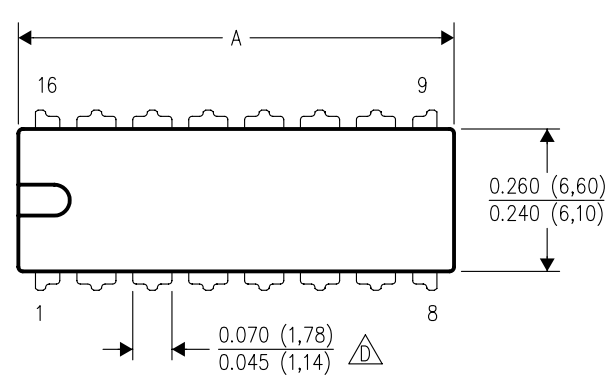
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2902N	N	PDIP	14	25	506	13.97	11230	4.32
LP2902N.A	N	PDIP	14	25	506	13.97	11230	4.32
LP324N	N	PDIP	14	25	506	13.97	11230	4.32
LP324N.A	N	PDIP	14	25	506	13.97	11230	4.32

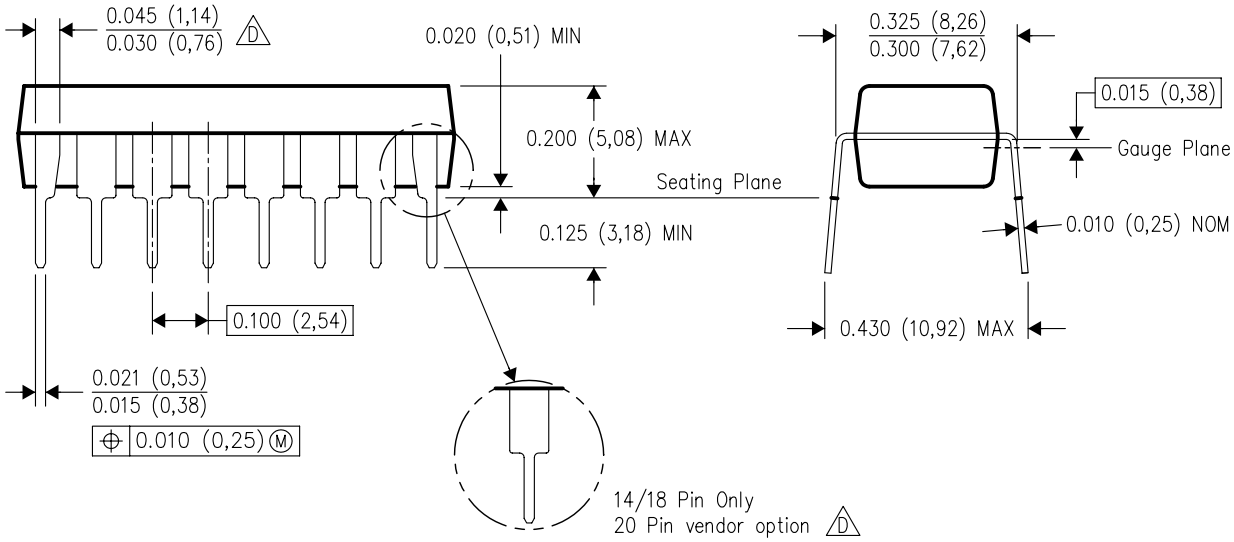
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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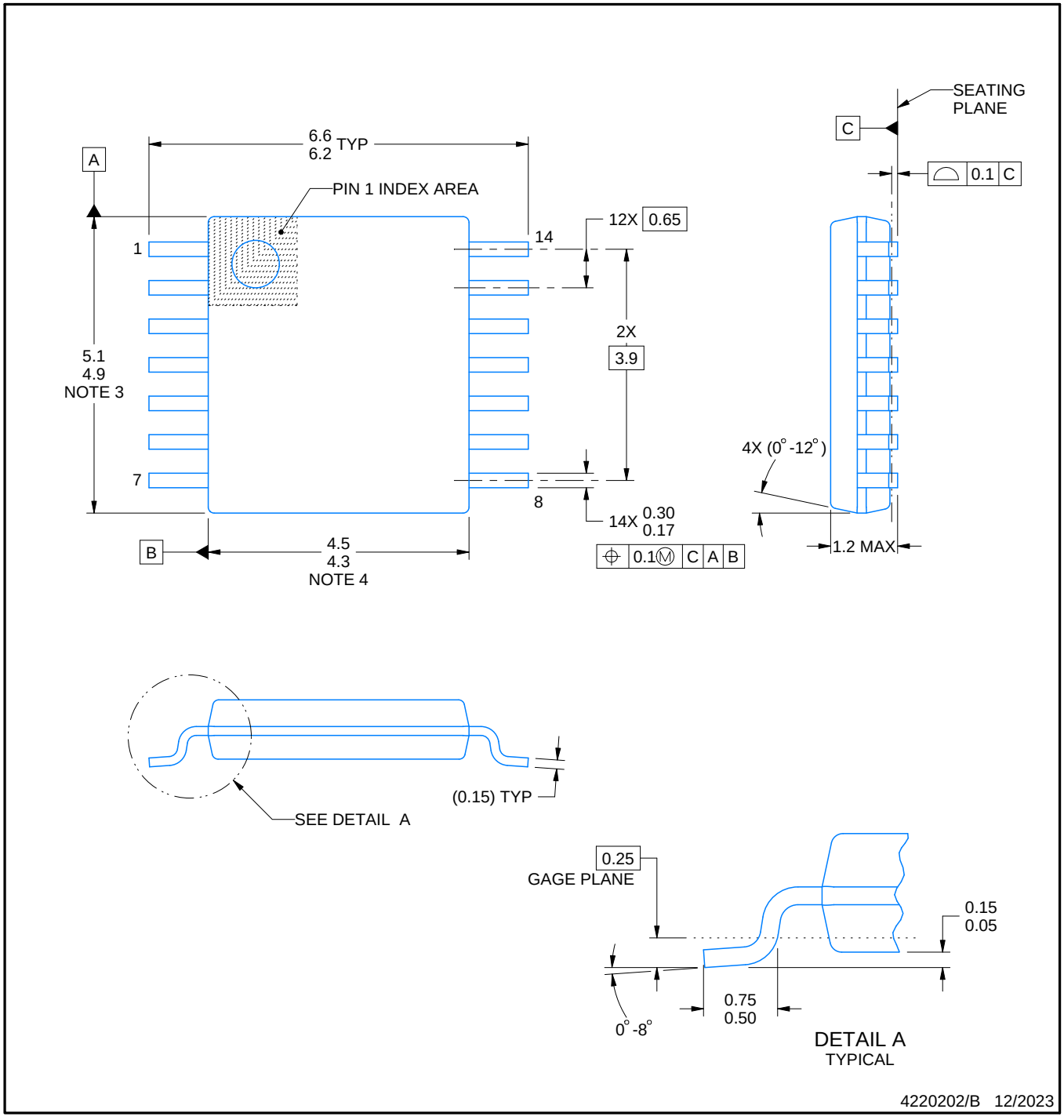
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

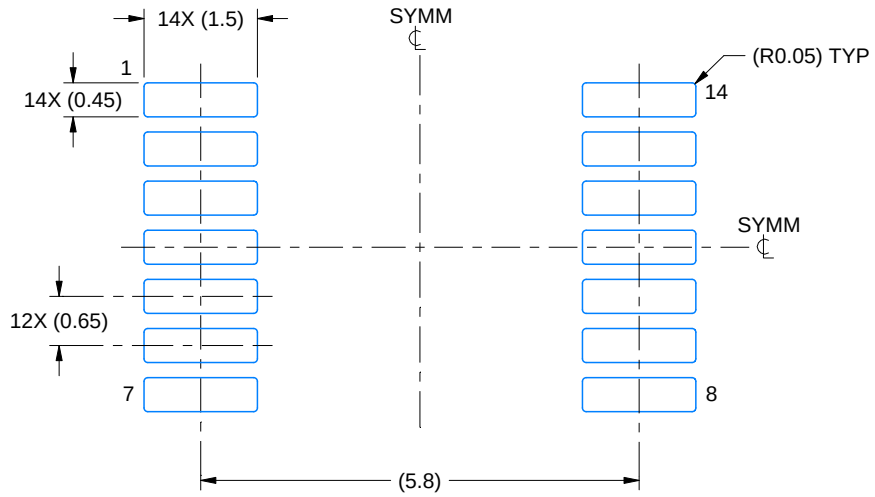
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

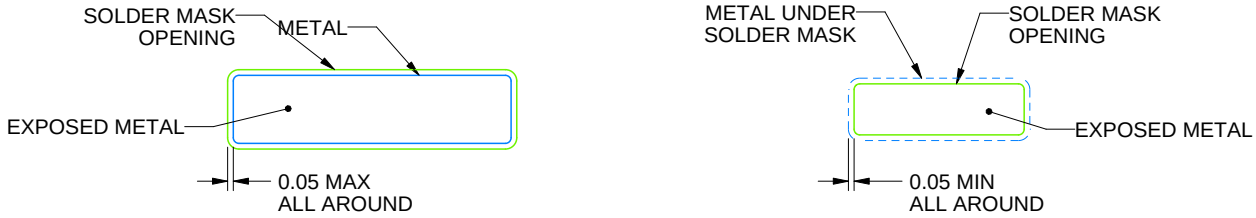


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

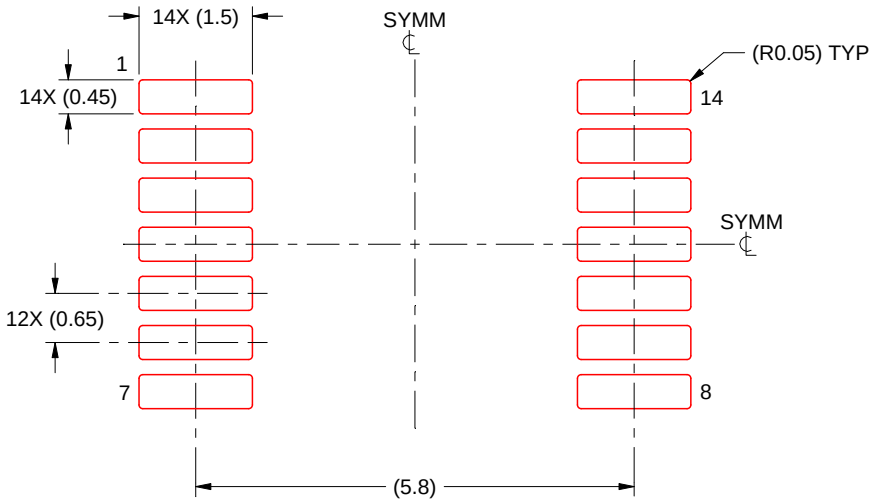


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

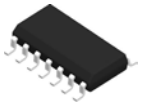


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

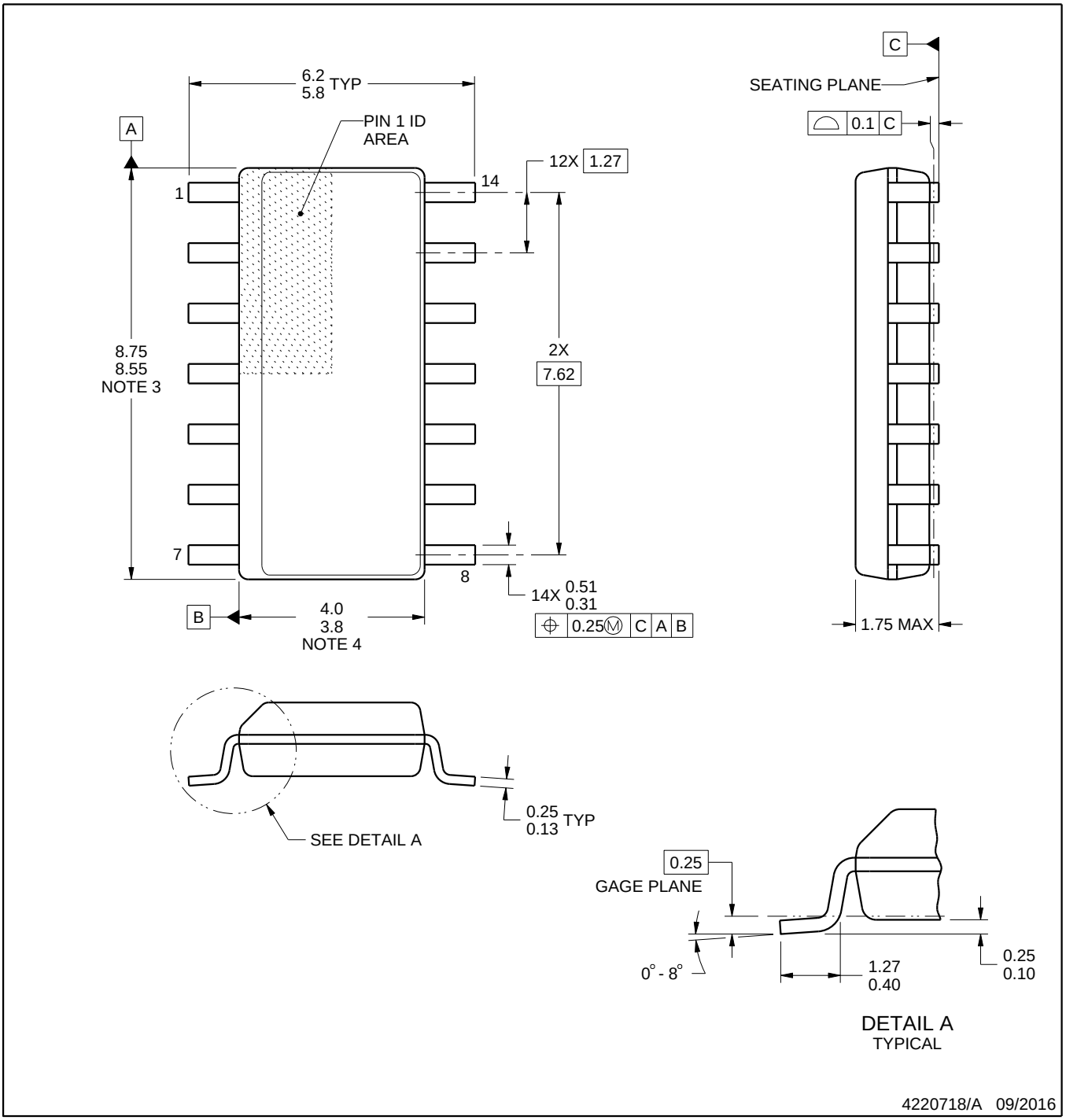


PACKAGE OUTLINE

D0014A

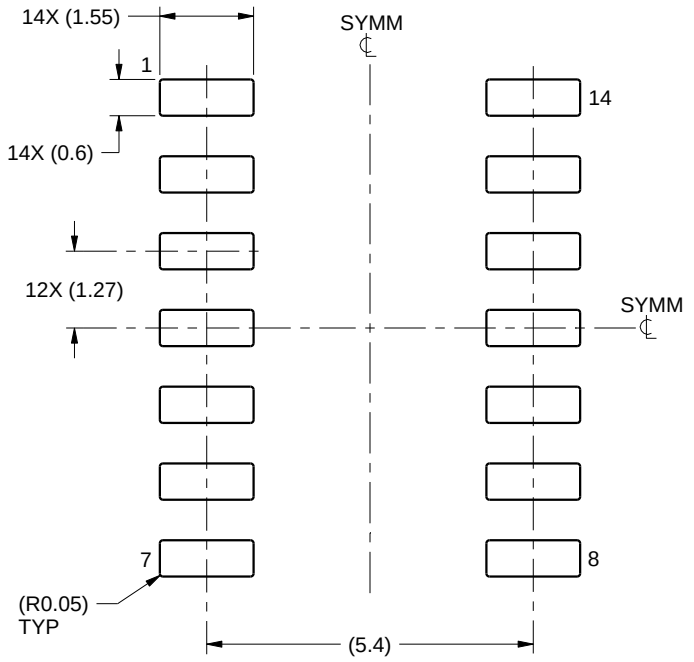
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

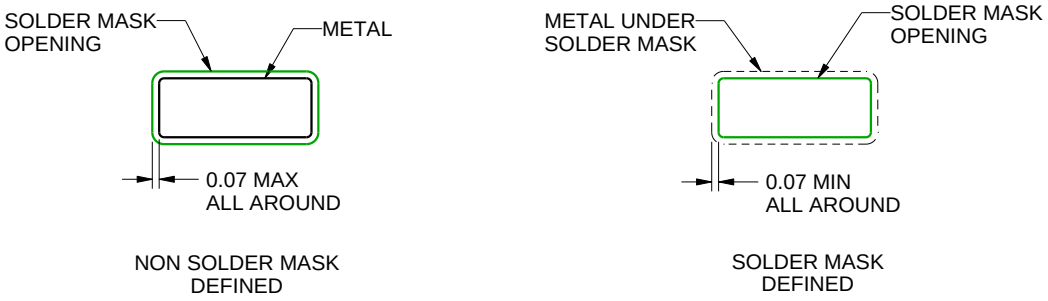


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

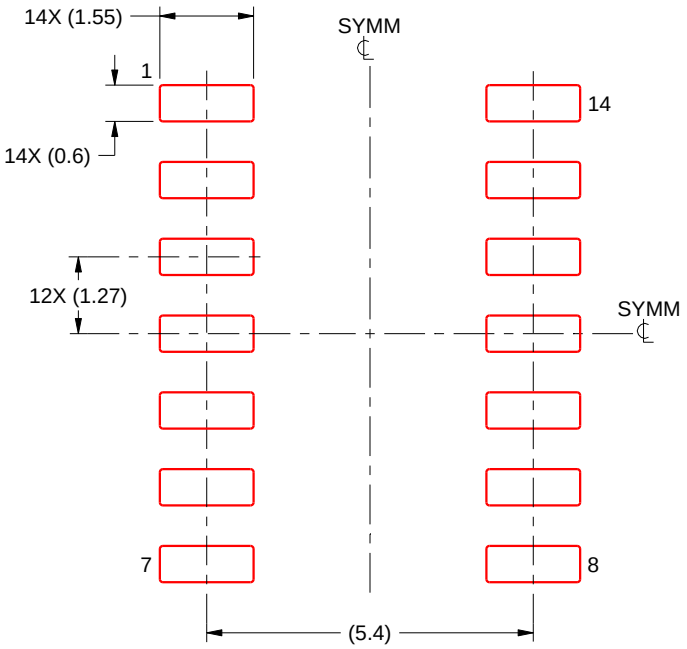
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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