LP2980-ADJ 16-V, 50-mA, Low-Power, Adjustable Low-Dropout Regulator

1 Features

- V_{IN} range:
  - Legacy chip: 2.2 V to 16 V
  - New chip: 2.5 V to 16V
- V_{OUT} range:
  - Legacy chip: 1.23 V to 15.0 V
  - New chip: 1.2 V to 15.0 V
- V_{OUT}(typ) accuracy:
  - Legacy chip: ±1%
  - New chip: ±0.5%
- Output accuracy over load and temperature:
  - Legacy chip: ±3.5%
  - New chip: ±1%
- Output current: Up to 50 mA
- Quiescent current, low I_Q (new chip):
  - 55 µA at I_{LOAD} = 0 mA
  - 350 µA at I_{LOAD} = 50 mA
- Shutdown current over temperature:
  - Legacy chip: < 1 µA
  - New chip: ≤ 0.8 µA
- Output current limiting and thermal protection
- Stable with 2.2-µF ceramic capacitors (new chip)
- High PSRR (new chip):
  - 70 dB at 1 kHz, 42 dB at 1 MHz
- Operating junction temperature: –40°C to +125°C
- Package: 5-pin SOT-23 (DBV)

2 Applications

- Residential breakers
- Solid state drives (SSD)
- Electricity meters
- Appliances
- Building automation

3 Description

The LP2980-ADJ is an adjustable-output, wide-input, low-dropout voltage regulator supporting an input voltage range up to 16 V and up to 50 mA of load current. The LP2980-ADJ supports an output range of 1.2 V to 15.0 V (new chip) and 1.23 V to 15.0 V (legacy chip).

Additionally, the LP2980-ADJ (new chip) has a 1% output accuracy across load and temperature that can meet the needs of low-voltage microcontrollers (MCUs) and processors.

In the new chip, wide bandwidth PSRR performance of greater than 70 dB at 1 kHz and 45 dB at 1 MHz helps attenuate the switching frequency of an upstream DC/DC converter and minimize post regulator filtering.

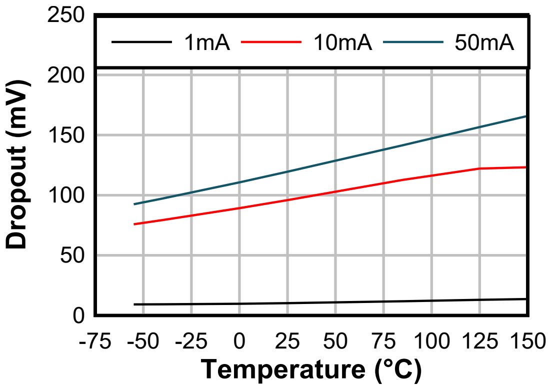
The internal soft-start time and current-limit protection reduce inrush current during start up, thus minimizing input capacitance. Standard protection features, such as overcurrent and overtemperature protection, are included.

The LP2980-ADJ is available in a 5-pin, 2.9-mm × 1.6-mm SOT-23 (DBV) package.

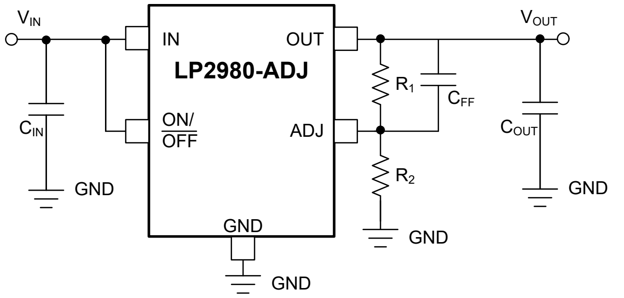
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LP2980-ADJ	DBV (SOT-23, 5)	2.9 mm × 2.8 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Dropout Voltage vs Temperature for New Chip



Typical Application Circuit

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F (July 2023)	Page
• Added *ESD Ratings* table, *Overview* section, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Typical Application* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added new chip (M3 suffix) information to document	1
• Changed document title, *Features*, *Applications*, and *Description* sections	1
• Deleted *Application Hints* section	1
• Changed *Pin Configuration and Functions* title and section	3
• Changed title, condition statement, and curve titles and added curves for new chip in *Typical Characteristics* section	9
• Changed *Functional Block Diagram* figure	17
• Added *Device Nomenclature* section	29

Changes from Revision D (April 2013) to Revision E (April 2013)	Page
• Changed layout of National Data Sheet to TI format	26

5 Pin Configuration and Functions

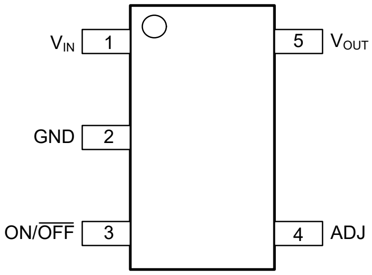


Figure 5-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADJ	4	I/O	Feedback pin to set the output voltage with help of the feedback divider. See the *Recommended Operating Conditions* section for more information.
GND	2	—	Ground
ON/$\overline{OFF}$	3	I	Enable pin for the LDO. Driving the ON/$\overline{OFF}$ pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. Tie this pin to V_{IN} if unused.
V_{IN}	1	I	Input supply pin. Use a capacitor with a value of 1 µF or larger from this pin to ground. See the *Input and Output Capacitor Requirements* section for more information.
V_{OUT}	5	O	Output of the regulator. Use a capacitor with a value of 4.7 µF (for legacy chip) and 2.2 µF (for new chip) or larger from this pin to ground.(1) See the *Input and Output Capacitor Requirements* section for more information.

(1) The nominal output capacitance must be greater than 1 µF (for the new chip) and 2.2 µF (for the legacy chip). Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 µF (for the new chip) and 2.2 µF (for the legacy chip).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range (for legacy chip)	–0.3	16	V
	Continuous input voltage range (for new chip)	–0.3	18	
V_{OUT}	Output voltage range (for legacy chip)	–0.3	16	
	Output voltage range (for new chip)	–0.3	V_{IN} + 0.3 or 18 (whichever is smaller)	
V_{ADJ}	ADJ pin voltage range (for new chip)	–0.3	3	
$V_{IN} – V_{OUT}$ (3)	Input – Output voltage (for legacy chip)	–0.3	16	
$V_{ON/\overline{OFF}}$	ON/$\overline{\text{OFF}}$ pin voltage range (for legacy chip)	–0.3	16	
	ON/$\overline{\text{OFF}}$ pin voltage range (for new chip)	–0.3	18	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) In legacy chip, the output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} will turn on this diode

6.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	NA	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	2.2		16	V
	Supply input voltage (for new chip)	2.5		16	
V_{OUT}	Output voltage (for legacy chip)	1.225		15.0	
	Output voltage (for new chip)	1.2		15.0	
V_{ADJ}	ADJ voltage (for legacy chip)		1.225		
	ADJ voltage (for new chip)		1.2		
$V_{ON/\overline{OFF}}$	Enable voltage (for legacy chip)	0		V_{IN}	
	Enable voltage (for new chip)	0		16	
I_{OUT}	Output current	0		50	mA
C_{IN} (3)	Input capacitor		1		µF
C_{OUT}	Output capacitor (for legacy chip) (2)	2.2	4.7		
	Output capacitance (for new chip) (1)	1	2.2	200	
C_{FF} (4)	Feed-forward capacitor (for legacy chip)		7		pF
	Feed-forward capacitor (for new chip)		10		
T_J	Operating junction temperature	–40		125	°C

(1) For new chip, all capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.
(2) For legacy chip, minimum output capacitance of 2.2 µF is required with ESR range suggested in the *Recommended Capacitor Types* section
(3) For legacy chip, an input capacitor of value ≥1 µF is required. It must be located not more than 0.5″ from the input pin and returned to a clean analog ground.
(4) Regarding the requirement of feed-forward capacitor (C_{FF}), see the *Feed-Forward Capacitor* section.

6.4 Thermal Information

THERMAL METRIC (2) (1)		Legacy Chip	New Chip	UNIT
		DBV (SOT23-5)	DBV (SOT23-5)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.4	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	47.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.3	15.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46.3	46.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application report.

6.5 Electrical Characteristics

specified at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	Legacy Chip	I_L = 1mA	1.213	1.225	1.237	V
		New Chip		1.194	1.2	1.206	
		Legacy Chip	1 mA < I_L < 50 mA, $V_{OUT} + 1 \le V_{IN} \le$ 16V, T_J = 25°C	1.206	1.225	1.243	
		New Chip		1.1928	1.2	1.206	
		Legacy Chip	1 mA < I_L < 50 mA, $V_{OUT} + 1 \le V_{IN} \le$ 16V, –40°C ≤ T_J ≤ 125°C	1.182	1.225	1.268	
		New Chip		1.1892	1.2	1.2108	
$\Delta V_{REF/}$ ΔV_{IN}	Reference Voltage Line Regulation	Legacy Chip	2.5V ≤ VIN ≤ 16V, T_J = 25°C		3.0	6.0	mV
		New Chip			–0.5	4.0	
		Legacy Chip	2.5V ≤ VIN ≤ 16V, –40°C ≤ T_J ≤ 125°C			15.0	
		New Chip				4.25	
V_{IN} - V_{OUT}	Dropout voltage	Legacy Chip	I_L = 0mA		1	3	mV
		New Chip			1	3.5	
		Legacy Chip	I_L = 0mA, –40°C ≤ T_J ≤ 125°C			5	
		New Chip				5.5	
		Legacy Chip	I_L = 1mA		7	10	
		New Chip			10.5	15.5	
		Legacy Chip	I_L = 1mA, –40°C ≤ T_J ≤ 125°C			15	
		New Chip				18.5	
		Legacy Chip	I_L = 10mA		40	60	
		New Chip			95	115	
		Legacy Chip	I_L = 10mA, –40°C ≤ T_J ≤ 125°C			90	
		New Chip				148	
		Legacy Chip	I_L = 50mA		120	150	
		New Chip			120	145	
		Legacy Chip	I_L = 50mA, –40°C ≤ T_J ≤ 125°C			225	
		New Chip				184	

6.5 Electrical Characteristics (continued)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GND}	Ground Pin Current	Legacy Chip	I_L = 0mA		60	95	µA
		New Chip			55	70	
		Legacy Chip	I_L = 0mA, –40°C ≤ T_J ≤ 125°C			125	
		New Chip				90	
		Legacy Chip	I_L = 1mA		80	110	
		New Chip			70	82	
		Legacy Chip	I_L = 1mA, –40°C ≤ T_J ≤ 125°C			170	
		New Chip				105	
		Legacy Chip	I_L = 10mA		120	220	
		New Chip			150	188	
		Legacy Chip	I_L = 10mA, –40°C ≤ T_J ≤ 125°C			460	
		New Chip				220	
		Legacy Chip	I_L = 50mA		320	600	
		New Chip			350	420	
		Legacy Chip	I_L = 50mA, –40°C ≤ T_J ≤ 125°C			1200	
		New Chip				600	
		Legacy Chip	$V_{ON/OFF}$ < 0.18V, V_{IN} ≤ 4.3V, –40°C ≤ T_J ≤ 125°C		0.01	1	
		New Chip			0.2	0.8	
		New Chip	$V_{ON/OFF}$ < 0.18V, V_{IN} = 16V, –40°C ≤ T_J ≤ 125°C			2.5	
I_{ADJ}	ADJ Pin Bias Current	Legacy Chip	1 mA ≤ I_L ≤ 50 mA		150	350	nA
		New Chip			0.35	30	
V_{UVLO+}	Rising bias supply UVLO	New Chip	V_{IN} rising, –40°C ≤ T_J ≤ 125°C		2.2	2.4	V
V_{UVLO-}	Falling bias supply UVLO		V_{IN} falling, –40°C ≤ T_J ≤ 125°C	1.9	2.07		
$V_{UVLO(HYST)}$	UVLO hysteresis		–40°C ≤ T_J ≤ 125°C		0.130		
$V_{ON/OFF}$	ON/OFF input voltage	Legacy Chip	High = O/P ON	1.6	1.4		V
			Low = O/P OFF		0.55	0.18	
		New Chip	High = O/P ON	1.6	0.82		
			Low = O/P OFF		0.7	0.18	
$I_{ON/OFF}$	ON/OFF input Current	Legacy Chip	$V_{ON/OFF}$ = 0		0.01	–1	µA
			$V_{ON/OFF}$ = 5V		5	15	
		New Chip	$V_{ON/OFF}$ = 0		–0.35	–0.7	
			$V_{ON/OFF}$ = 5V		0.008	0.5	
I_O(PK)	Peak Output Current	Legacy Chip	V_{OUT} ≥ V_O(NOM) – 5%	100	150		mA
		New Chip		130	150		
I_O(MAX)	Short Circuit Current	Legacy Chip	R_L = 0 (Steady State)		150		
		New Chip			160		
e_n	Output Noise Voltage (RMS)	Legacy Chip	BW = 300 Hz to 50 kHz, C_{OUT} = 10µF		160		µV
		New Chip	BW = 300 Hz to 50 kHz, C_{OUT} = 2.2µF		160		
			BW = 10 Hz to 100 kHz, C_{OUT} = 2.2µF		220		
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple Rejection	Legacy Chip	f = 1 kHz, C_{OUT} = 10µF		68		dB
		New Chip	f = 1 kHz, C_{OUT} = 2.2µF		68		
			f = 100 kHz, C_{OUT} = 2.2µF		45		

6.5 Electrical Characteristics (continued)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{sd(shutdown)}$	Thermal shutdown threshold	New Chip	Shutdown, temperature increasing		170		°C
$T_{sd(reset)}$			Reset, temperature decreasing		150		

6.6 Typical Characteristics

at operating temperature T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

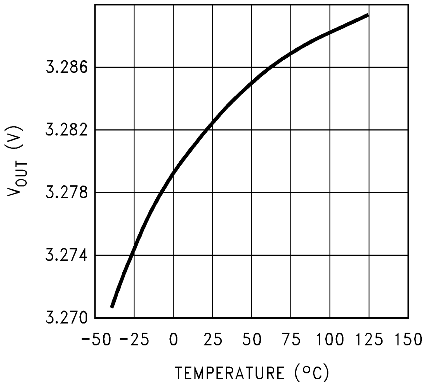
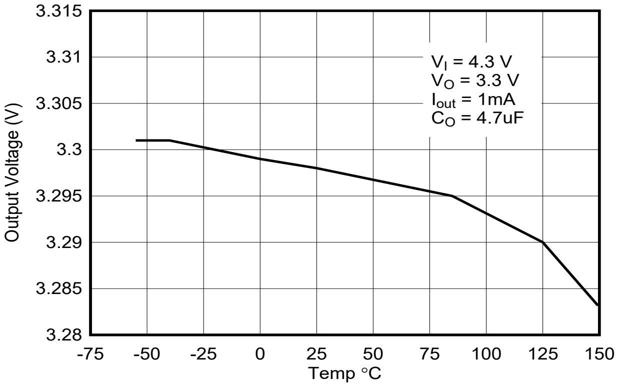


Figure 6-1. Output Voltage vs Temperature for Legacy Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V

Figure 6-2. Output Voltage vs Temperature for New Chip

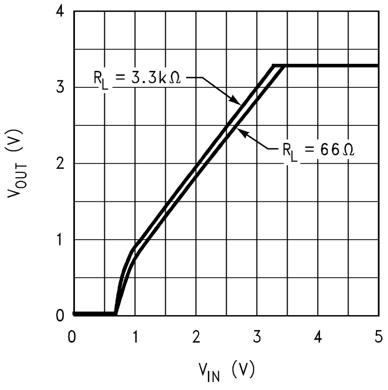


Figure 6-3. Output Voltage vs V_{IN} for Legacy Chip

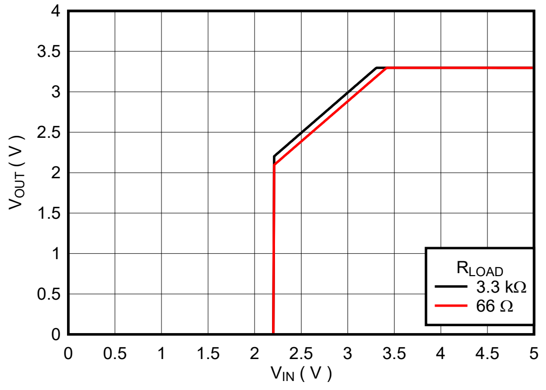


Figure 6-4. Output Voltage vs V_{IN} for New Chip

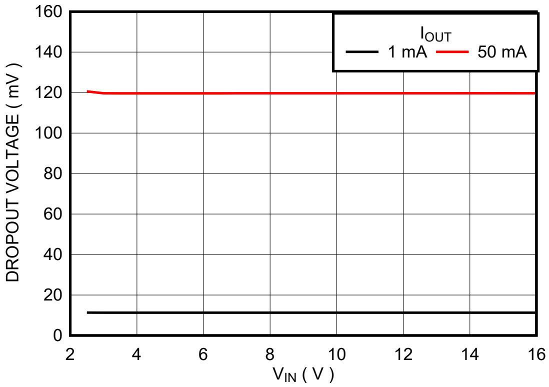


Figure 6-5. Dropout Voltage vs V_{IN} for New Chip

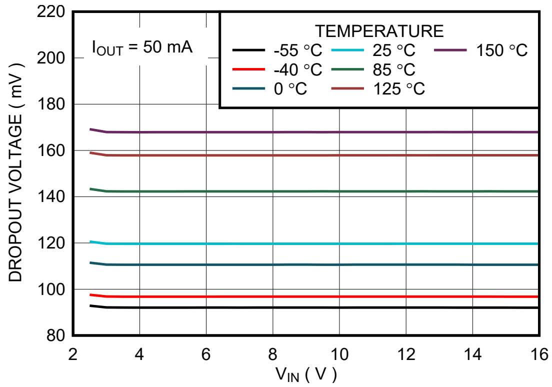


Figure 6-6. Dropout Voltage vs V_{IN} and Temperature for New Chip

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

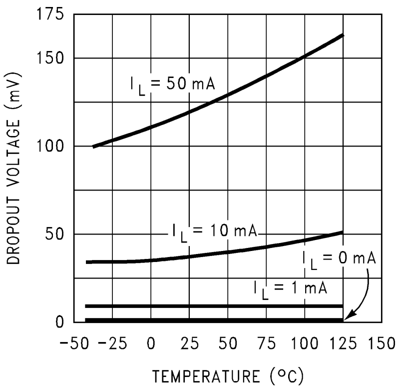


Figure 6-7. Dropout Voltage vs Temperature for Legacy Chip

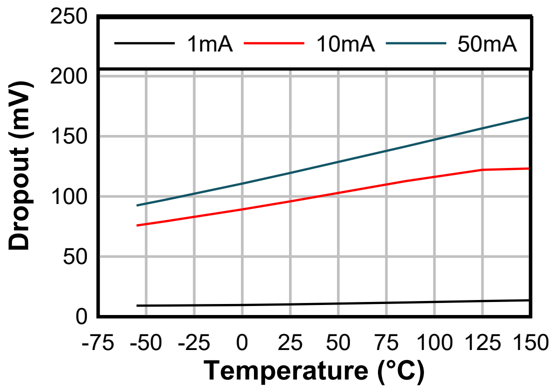


Figure 6-8. Dropout Voltage vs Temperature for New Chip

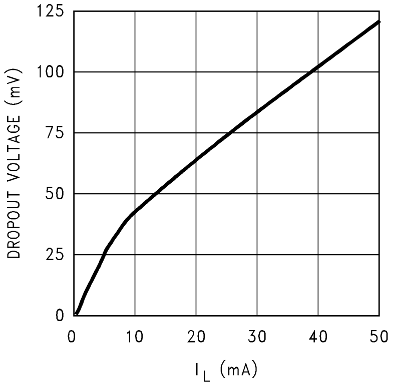


Figure 6-9. Dropout Voltage vs Load Current for Legacy Chip

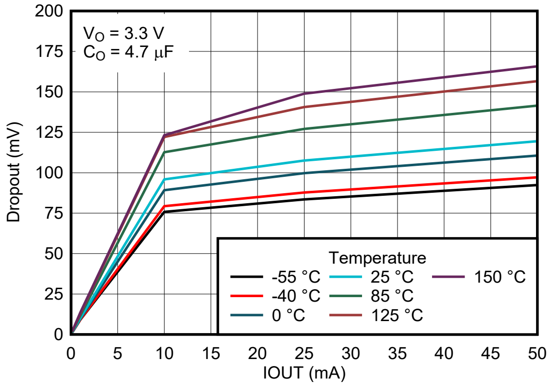


Figure 6-10. Dropout Voltage vs Load Current for New Chip

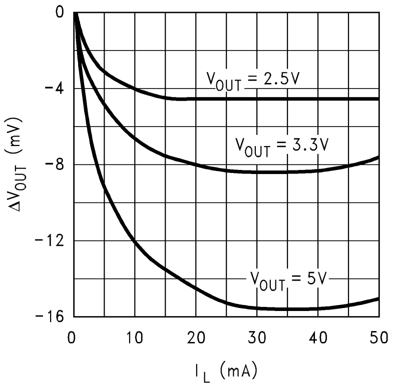


Figure 6-11. Output Regulation vs Load Current for Legacy Chip

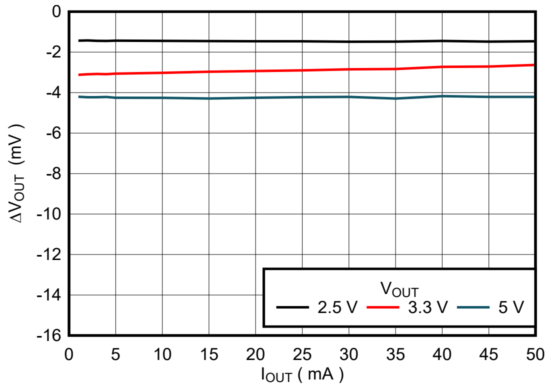


Figure 6-12. Output Regulation vs Load Current for New Chip

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

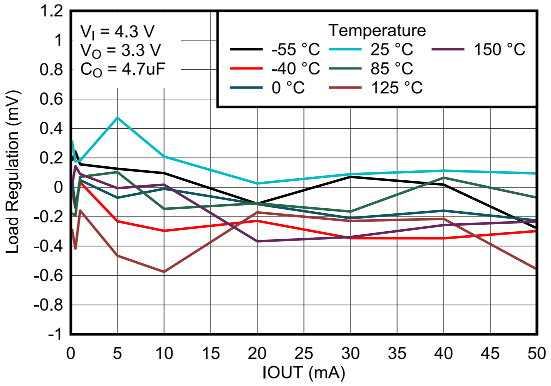


Figure 6-13. Output Regulation vs Load Current and Temperature for New Chip

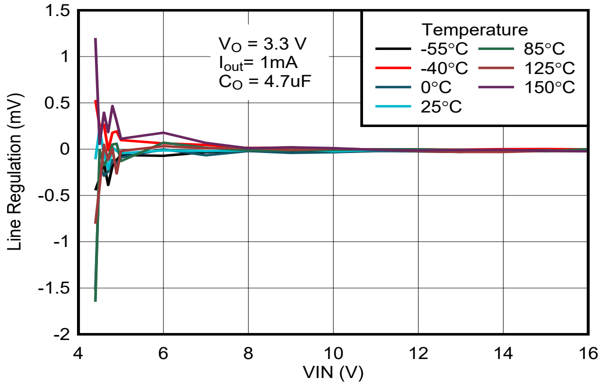


Figure 6-14. Output Regulation vs Input Voltage for New Chip

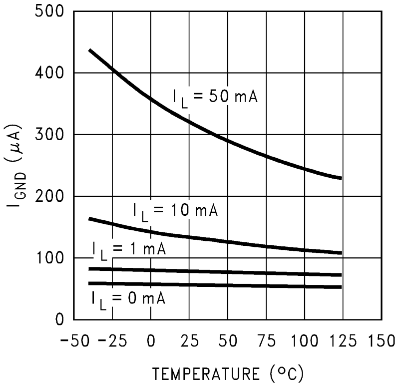


Figure 6-15. Ground-Pin Current vs Temperature for Legacy Chip

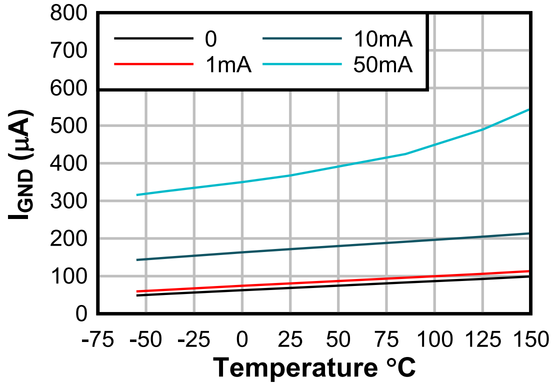


Figure 6-16. Ground-Pin Current vs Temperature for New Chip

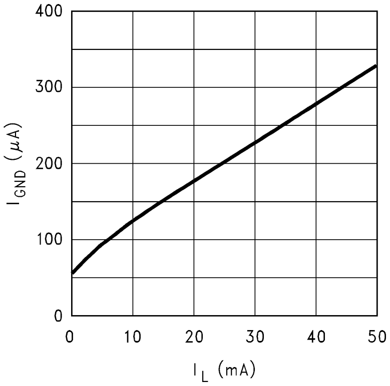


Figure 6-17. Ground Pin Current vs Load Current for Legacy Chip

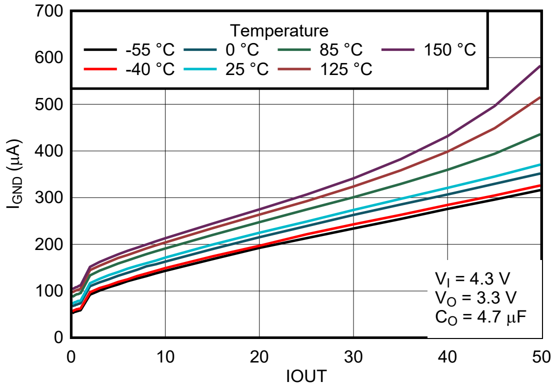


Figure 6-18. Ground Pin Current vs Load Current for New Chip

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

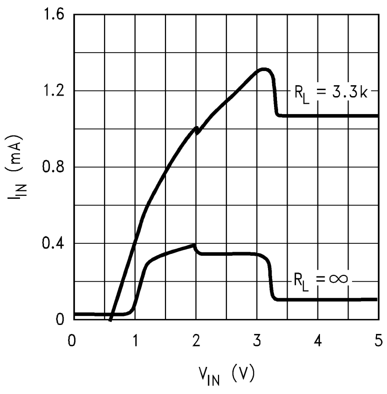


Figure 6-19. Input Current vs Input Voltage for Legacy Chip

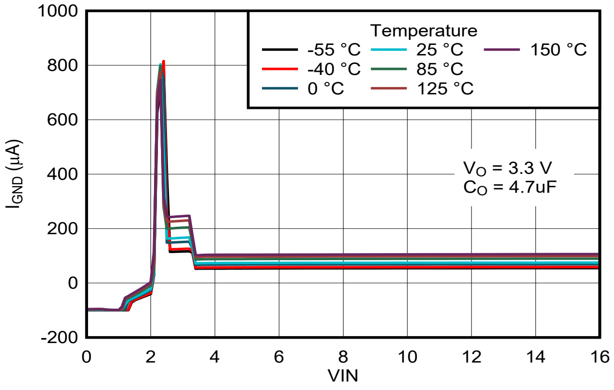


Figure 6-20. Input Current vs Input Voltage for New Chip

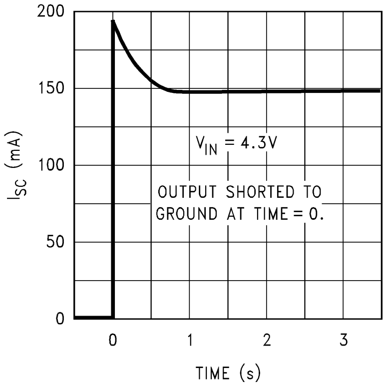
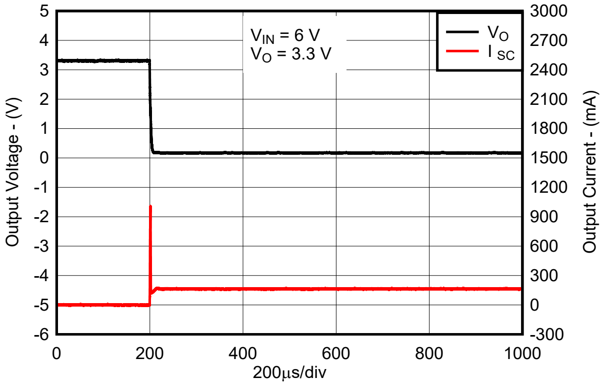


Figure 6-21. Short-Circuit Current vs Time for Legacy Chip



V_{IN} = 6 V

Figure 6-22. Short-Circuit Current vs Time for New Chip

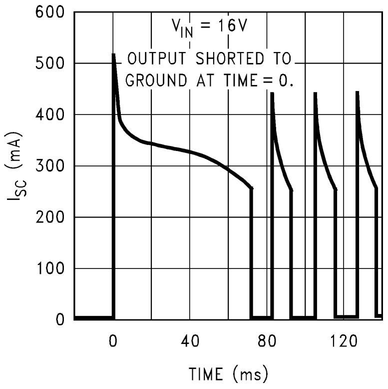


Figure 6-23. Short-Circuit Current vs Time for Legacy Chip

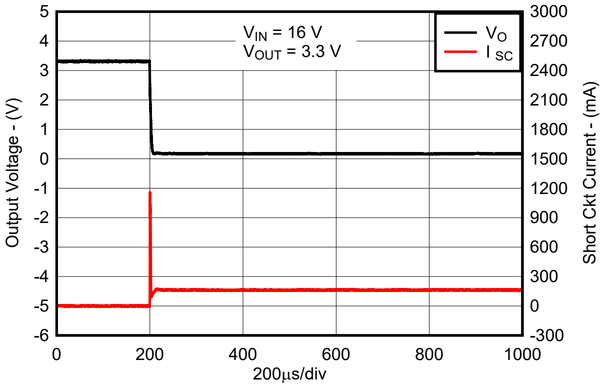


Figure 6-24. Short-Circuit Current vs Time for New Chip

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

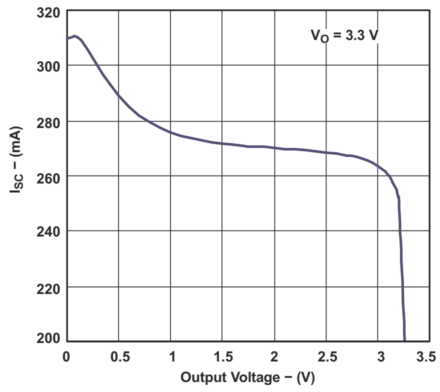


Figure 6-25. Short-Circuit Current vs Output Voltage for Legacy Chip

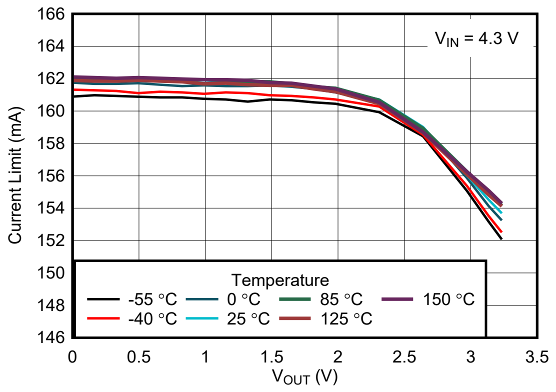


Figure 6-26. Short-Circuit Current vs Output Voltage for New Chip

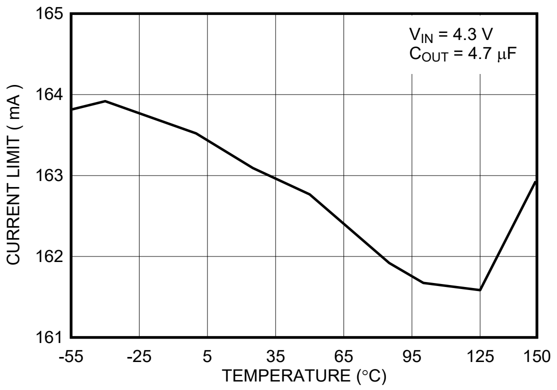


Figure 6-27. Short-Circuit Current vs Temperature for New Chip

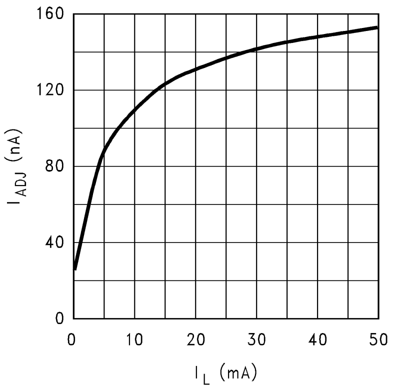


Figure 6-28. ADJ Pin Bias Current vs. Load Current for Legacy Chip

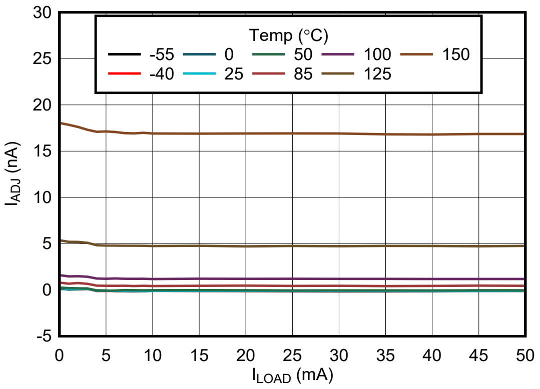


Figure 6-29. ADJ Pin Bias Current vs Load Current for New Chip

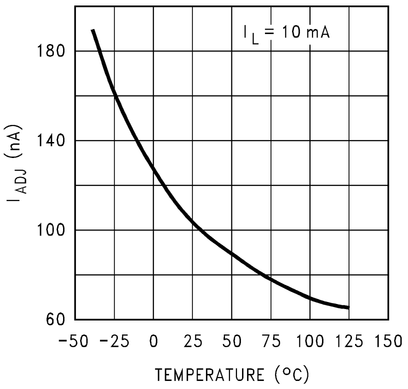


Figure 6-30. ADJ Pin Bias Current vs Temperature for Legacy Chip

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{IN} = V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

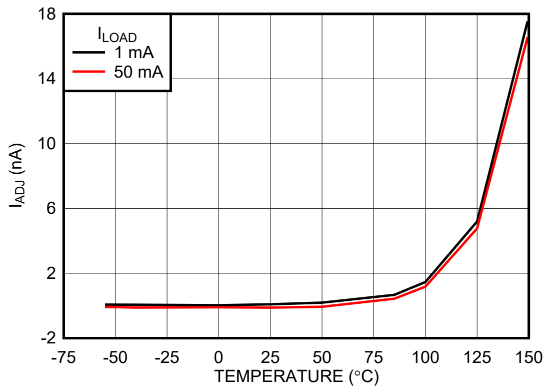


Figure 6-31. ADJ Pin Bias Current vs Temperature for New Chip

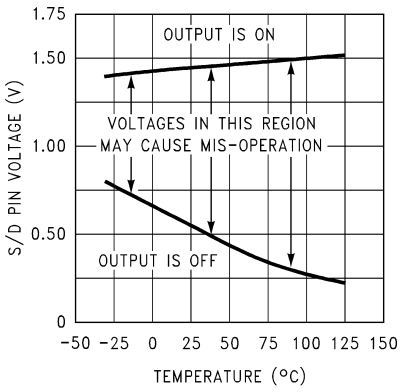


Figure 6-32. ON/OFF Threshold vs Temperature for Legacy Chip

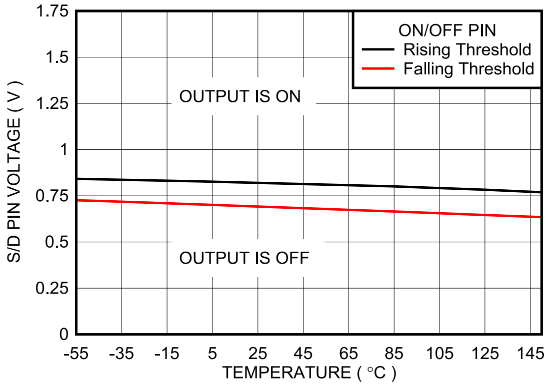


Figure 6-33. ON/OFF Threshold vs Temperature for New Chip

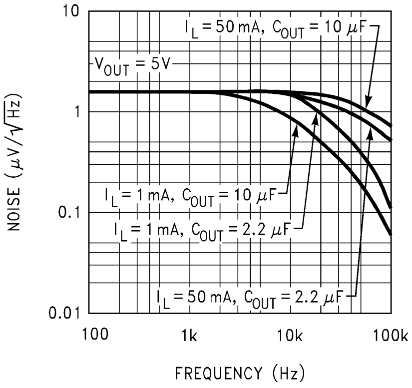
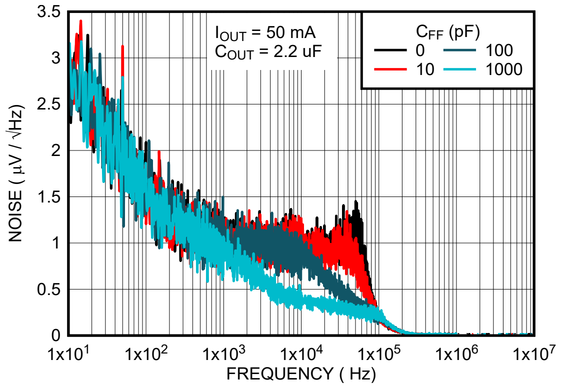
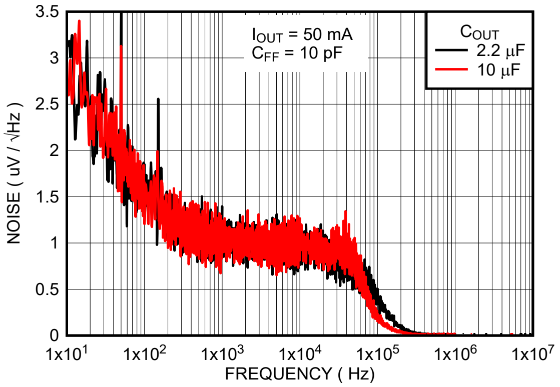


Figure 6-34. Output Noise Density for Legacy Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 50 mA, C_{OUT} = 2.2 µF

Figure 6-35. Output Noise Density vs C_{FF} for New Chip

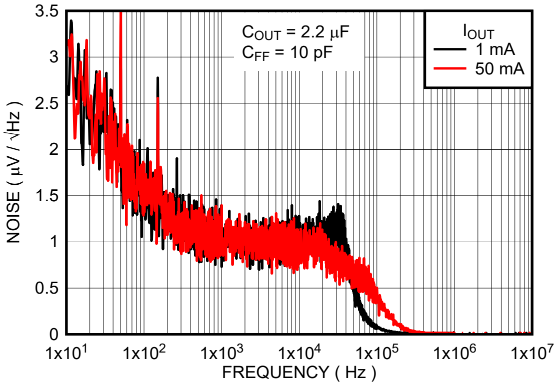


V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 50 mA, C_{FF} = 10 pF

Figure 6-36. Output Noise Density vs C_{OUT} for New Chip

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF, C_{FF} = 10 pF

Figure 6-37. Output Noise Density vs I_{OUT} for New Chip

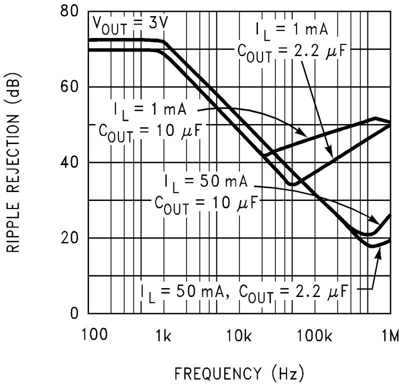
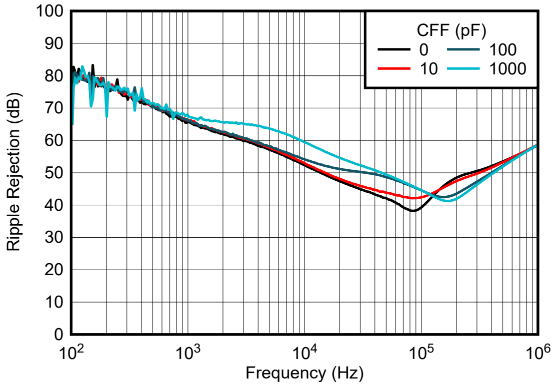
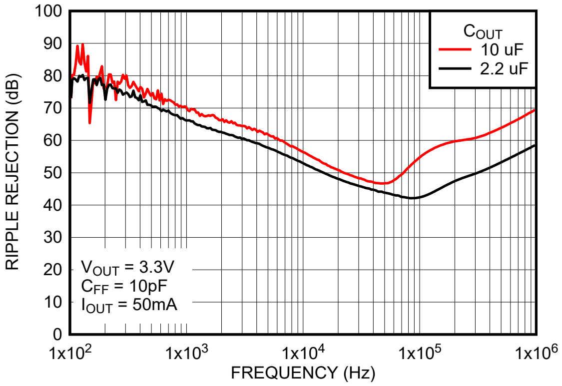


Figure 6-38. Ripple Rejection for Legacy Chip



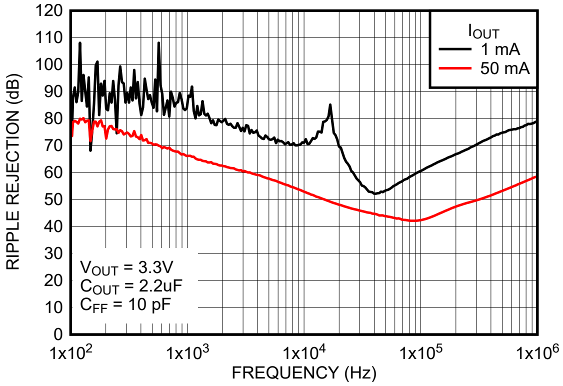
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 50 mA, C_{OUT} = 2.2 µF

Figure 6-39. Ripple Rejection vs C_{FF} for New Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 50 mA, C_{FF} = 10 pF

Figure 6-40. Ripple Rejection vs C_{OUT} for New Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF, C_{FF} = 10 pF

Figure 6-41. Ripple Rejection vs I_{OUT} for New Chip

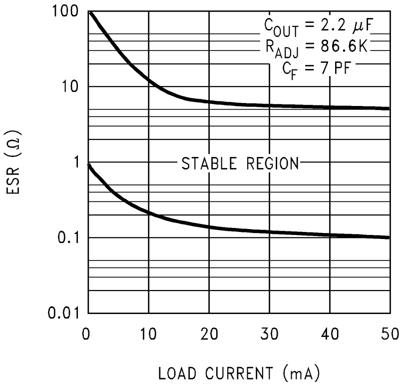


Figure 6-42. 2.2-µF ESR Curves for Legacy Chip

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

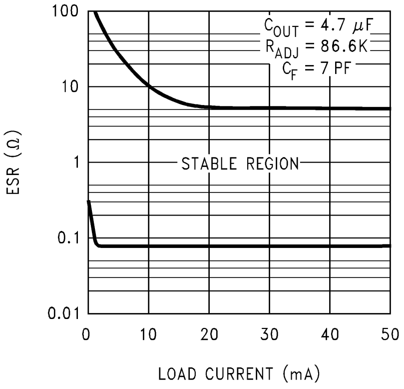


Figure 6-43. 4.7-µF ESR Curves for Legacy Chip

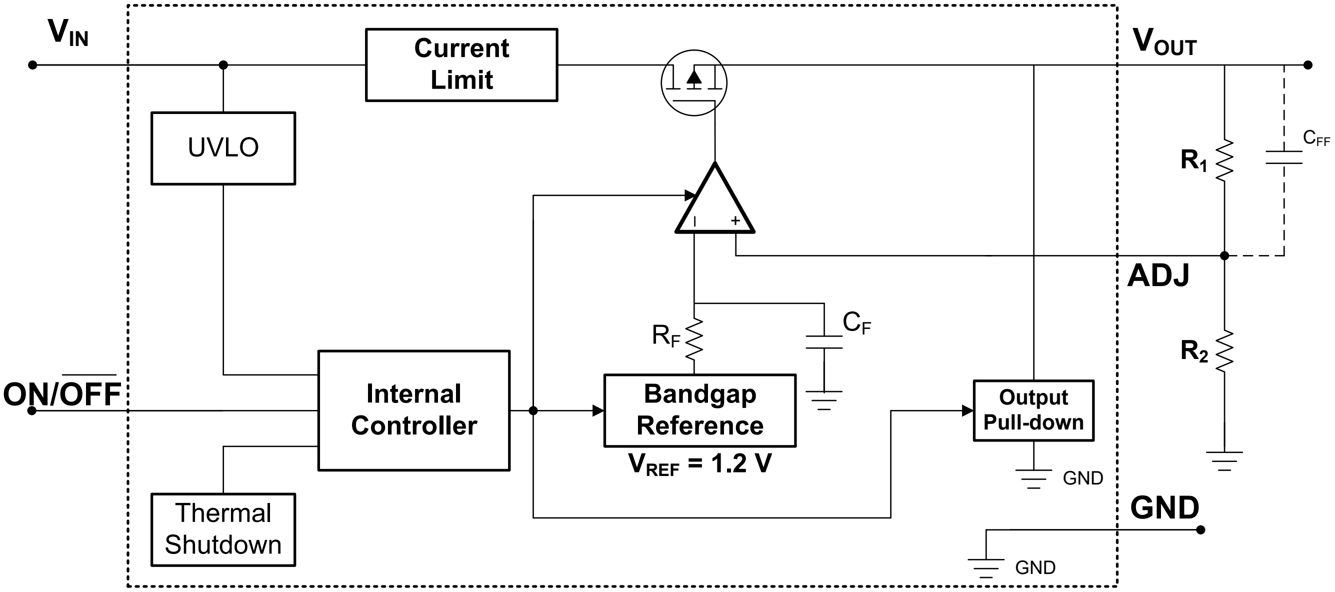
7 Detailed Description

7.1 Overview

The LP2980-ADJ is an adjustable-output, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2980-ADJ has an output tolerance of 1% across line, load, and temperature variation (for the new chip) and is capable of delivering 50 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown, output enable, and internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Enable

The ON/$\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/$\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/$\overline{\text{OFF}}$ pin and disabled when the ON/$\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/$\overline{\text{OFF}}$ pin to the input of the device.

For the new chip, the device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/$\overline{\text{OFF}}$ pin voltage lower than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin, to actively discharge the output voltage.

7.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} - V_{OUT}) \times I_{CL}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 7-1 shows a diagram of the current limit.

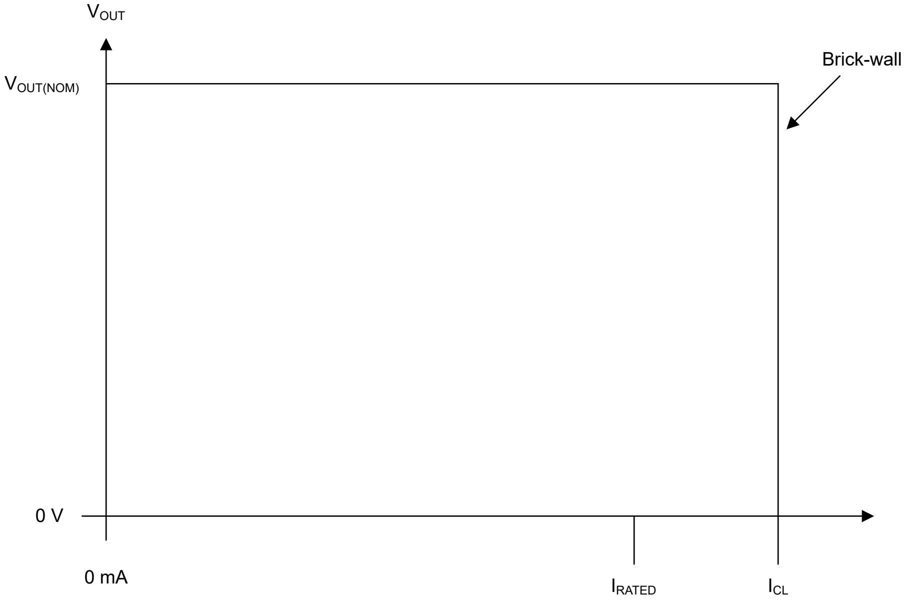


Figure 7-1. Current Limit

7.3.4 Undervoltage Lockout (UVLO)

For the new chip, the device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$)
- If 1.0 V < $V_{IN} < V_{UVLO}$

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

Table 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/\overline{OFF}}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output voltage is set by using ADJ pin (see *External Feedback Resistors*)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/$\overline{\text{OFF}}$ voltage has previously exceeded the ON/$\overline{\text{OFF}}$ rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/$\overline{\text{OFF}}$ pin to less than the maximum ON/$\overline{\text{OFF}}$ pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 External Feedback Resistors

The output voltage is set using the ADJ pin with help of the external feedback resistors, R_1 and R_2 (see Figure 8-2), according to the following equation:

$$V_{OUT} = V_{ADJ} \times \left(1 + R_1 / R_2\right) \tag{2}$$

For the legacy chip, use a resistor from the ADJ pin to ground with a value of 51.1 kΩ.

For the new chip, to ignore the ADJ pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the ADJ pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / \left(I_{ADJ} \times 100\right) \tag{3}$$

8.1.2 Recommended Capacitor Types

This section describes the recommended capacitors for both the new chip and the legacy chip.

8.1.2.1 Recommended Capacitors for the New Chip

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2.2 Recommended Capacitors for the Legacy Chip

The ESR of a good-quality tantalum capacitor is almost directly centered in the middle of the *stable* range of the ESR curve (approximately 0.5 Ω–1 Ω). The temperature stability of tantalum capacitors is typically very good, with a total variation of only approximately 2:1 over the temperature range of –40°C to +125°C (ESR increases at colder temperatures). Avoid off-brand capacitors because some poor-quality tantalum capacitors are available with ESR values greater than 10 Ω, which usually causes oscillation problems. One caution regarding tantalum capacitors is that if used on the input, the ESR is low enough to be destroyed by a surge current if the capacitor is powered up from a low impedance source (such as a battery) that has no limit on inrush current. In this case, use a ceramic input capacitor that does not have this problem.

Ceramic capacitors are generally larger and more costly than tantalum capacitors for a given amount of capacitance. These capacitors also have a very low ESR that is quite stable with temperature. However, the ESR of a ceramic capacitor is typically low enough to make an LDO oscillate. A 2.2-µF ceramic demonstrated an ESR of approximately 15 mΩ when tested. If used as an output capacitor, this ESR can cause instability (see the ESR curves in the *Typical Characteristics* section). If a ceramic capacitor is used on the output of an LDO, place a small resistor (approximately 1 Ω) in series with the capacitor. If used as an input capacitor, no resistor is needed because there is no requirement for ESR on capacitors used on the input.

8.1.3 Input and Output Capacitor Requirements

For the legacy chip, an input capacitor (C_{IN}) ≥1 µF is required (the amount of capacitance can be increased without limit). Any good-quality tantalum or ceramic capacitor can be used. The capacitor must be located no more than half an inch from the input pin and returned to a clean analog ground.

For the new chip, although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.1.4 Feed-Forward Capacitor (C_{FF})

A feed-forward capacitor (C_{FF}) can be connected from the V_{OUT} pin to the ADJ pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, whereas C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \tag{4}$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \tag{5}$$

For the legacy chip, a feed-forward capacitor (C_{FF}) of 7 pF is required, because this capacitor provides the lead compensation necessary for loop stability. Use a temperature-stable ceramic capacitor (NPO or COG type).

For the new chip, a C_{FF} ≥ 10 pF is required for stability only if the feedback divider current is less than 5 µA. The following equation calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \tag{6}$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$ µs.

For an output voltage of 1.2 V with the ADJ pin tied to the V_{OUT} pin, no C_{FF} is used.

8.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 8-1 shows one approach for protecting the device.

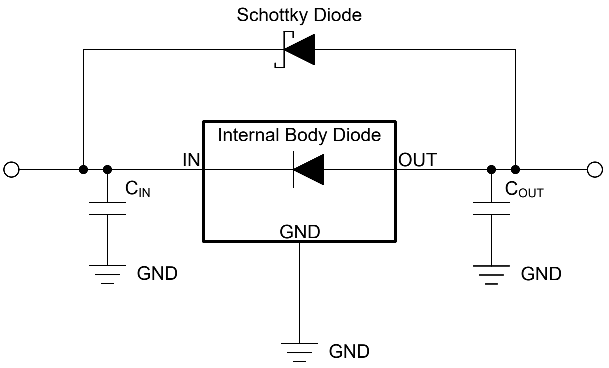


Figure 8-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (7)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ can be improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.

8.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{9}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{10}$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.2 Typical Application

Figure 8-2 shows the standard usage of the LP2980-ADJ as a low-dropout regulator.

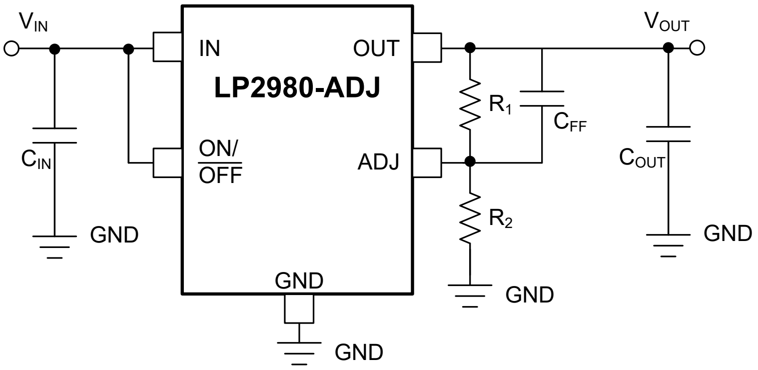


Figure 8-2. LP2980-ADJ Typical Application

8.2.1 Design Requirements

For this design, use the minimum C_{OUT} value for stability (which can be increased without limit for improved stability and transient response). The ON/$\overline{\text{OFF}}$ pin must be actively terminated. Connect this pin to V_{IN} if the shutdown feature is not used. Set the output voltage using a feedback divider between the V_{OUT} pin and the ADJ pin. Use an optional C_{FF} capacitor for improved transient, noise, and PSRR performance.

For the new chip, Table 8-1 summarizes the design requirements for Figure 8-2.

Table 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	12 V
Output voltage	2.5 V
Output current	50 mA
R_1 (feedback resistance)	108.33 kΩ
R_2 (feedback resistance)	100.00 kΩ

8.2.2 Detailed Design Procedure

8.2.2.1 Setting V_{OUT} For the LP2980-ADJ LDO

As illustrated in Figure 8-2, the LP2980-ADJ uses the feedback divider to set the output voltage. The output voltage operating range is 1.2 V to 15 V, and is calculated using:

$$V_{OUT} = V_{ADJ} \times \left(1 + R_1/R_2\right) \tag{11}$$

where:

- V_{REF} = 1.2 V (typical)

Choose resistors R1 and R2 as suggested in the *External Feedback Resistors* section.

Figure 8-2 depicts this configuration.

8.2.2.2 ON/OFF Input Operation

The LP2980-ADJ is shut off by driving the ON/OFF input low, and turned on by pulling the ON/OFF input high. If this feature is not used, the ON/OFF input must be tied to V_{IN} to keep the regulator output on at all times (the ON/OFF input must not be left floating).

To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds that specify an ON or OFF state (see the *Electrical Characteristics* table).

For the legacy chip, the turn-on (and turn-off) voltage signals applied to the ON/OFF input must have a slew rate which is greater than 40 mV/µs.

For the new chip, there is no restriction on the slew rate of the voltage signals applied to the ON/OFF input. Both fast and slow ramping voltage signals can be used to drive the ON/OFF pin.

Note

For the legacy chip only, the ON/OFF function does not operate correctly if a slow-moving signal is used to drive the ON/OFF input.

8.2.3 Application Curves

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

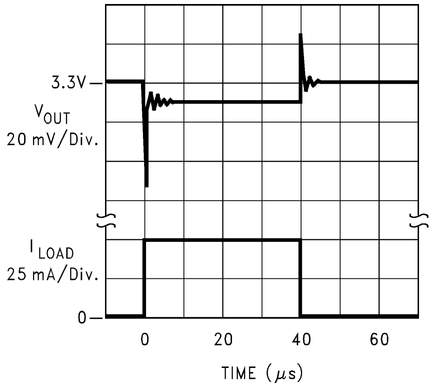
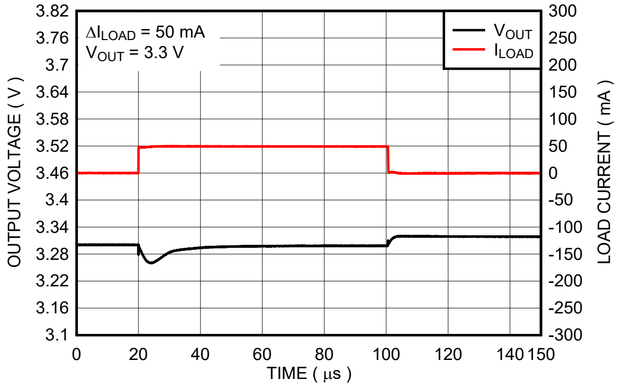


Figure 8-3. Load Transient Response for Legacy Chip



dI/dt = 1 A/µF

Figure 8-4. Load Transient Response for New Chip

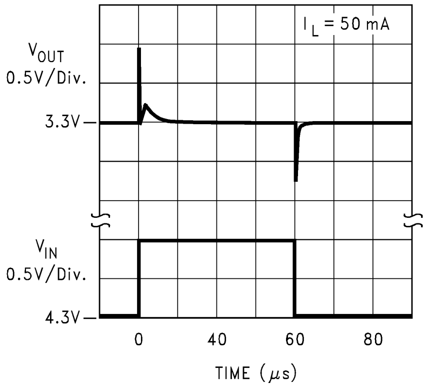
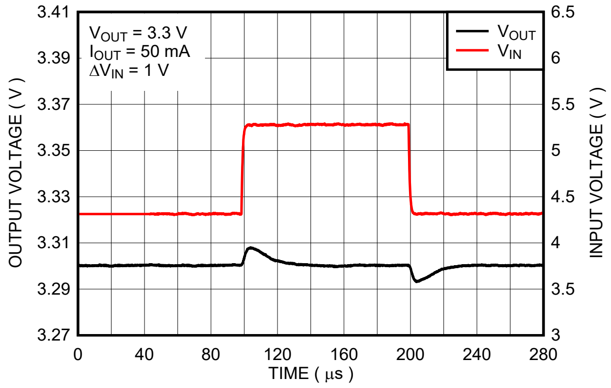
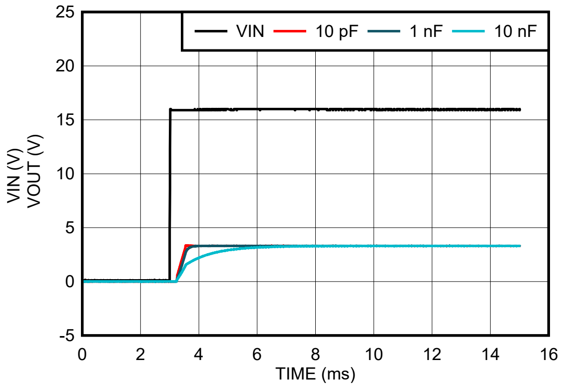


Figure 8-5. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, ΔV_{IN} = 1 V, I_{OUT} = 50 mA, dV/dt = 1 V/µs

Figure 8-6. Line Transient Response for New Chip



V_{OUT} = 3.3 V, dV/dt = 1 V/µs

Figure 8-7. Start-Up vs C_{FF} for New Chip

8.3 Power Supply Recommendations

A power supply can be used at the input voltage within the ranges given in the *Recommended Operating Conditions* table. Use bypass capacitors as described in the *Layout Guidelines* section.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass the input pin to ground with a bypass capacitor.
- The optimum placement of the bypass capacitor is closest to the V_{IN} of the device and GND of the system. Care must be taken to minimize the loop area formed by the bypass capacitor connection, the V_{IN} pin, and the GND pin of the system.
- For operation at full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

8.4.2 Layout Example

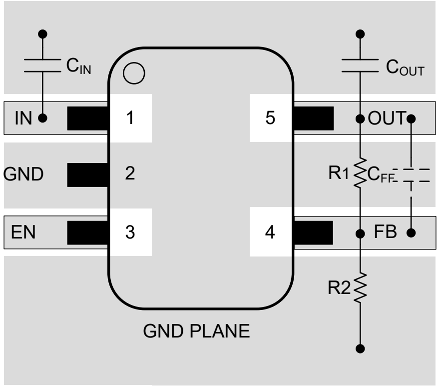


Figure 8-8. Layout Diagram

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Available Options(1)

PRODUCT	V_{OUT}
LP2980**cxxxz**-ADJ/NOPB Legacy chip	**A** is for higher accuracy and non-A is for standard grade. **c** is the accuracy specification. **xxx** is the package designator. **z** is the package quantity. X is for large quantity reel and non-X is for small quantity reel.
LP2980**Axxxz**-ADJ/**M3** New chip	**A** is for higher accuracy and non-A is for standard grade. **xxx** is the package designator. **z** is the package quantity. X is for large quantity reel and non-X is for small quantity reel. **M3** is a suffix designator for newer chip redesigns, fabricated on the latest TI process technology.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2980IM5-ADJ/NOM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L06B
LP2980IM5-ADJ/NOM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L06B
LP2980IM5-ADJ/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L06B
LP2980IM5-ADJ/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L06B
LP2980IM5X-ADJ/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L06B
LP2980IM5X-ADJ/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L06B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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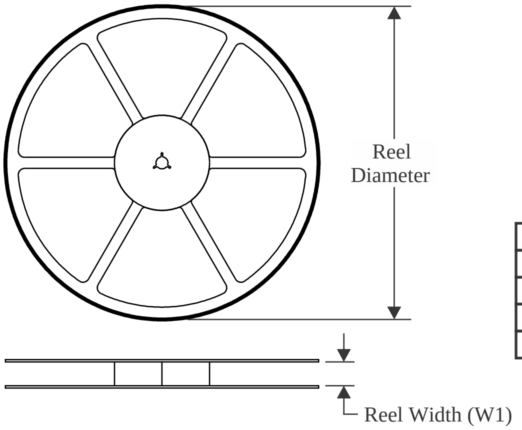
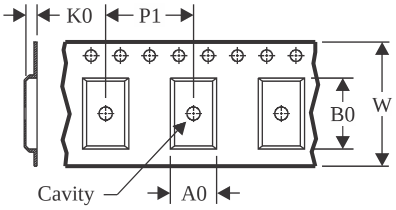
TAPE AND REEL INFORMATION

REEL DIMENSIONS

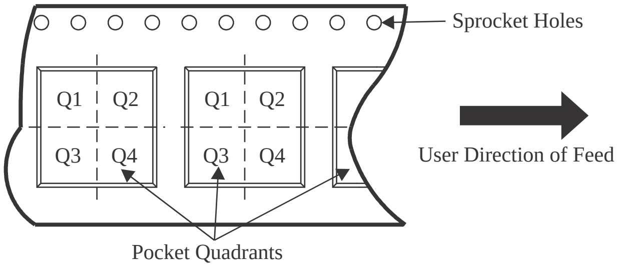


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

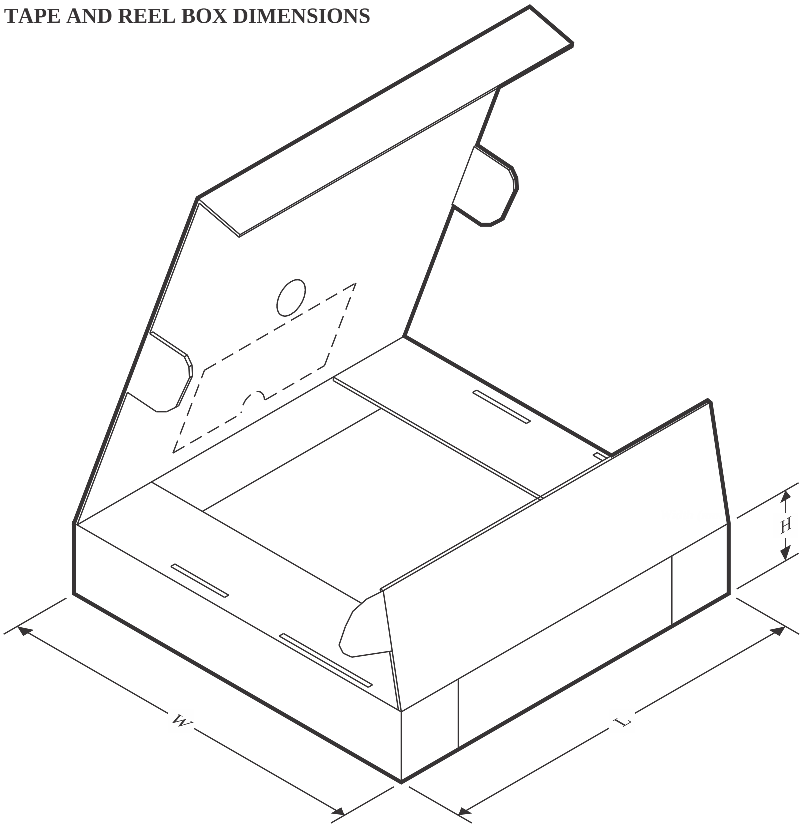
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

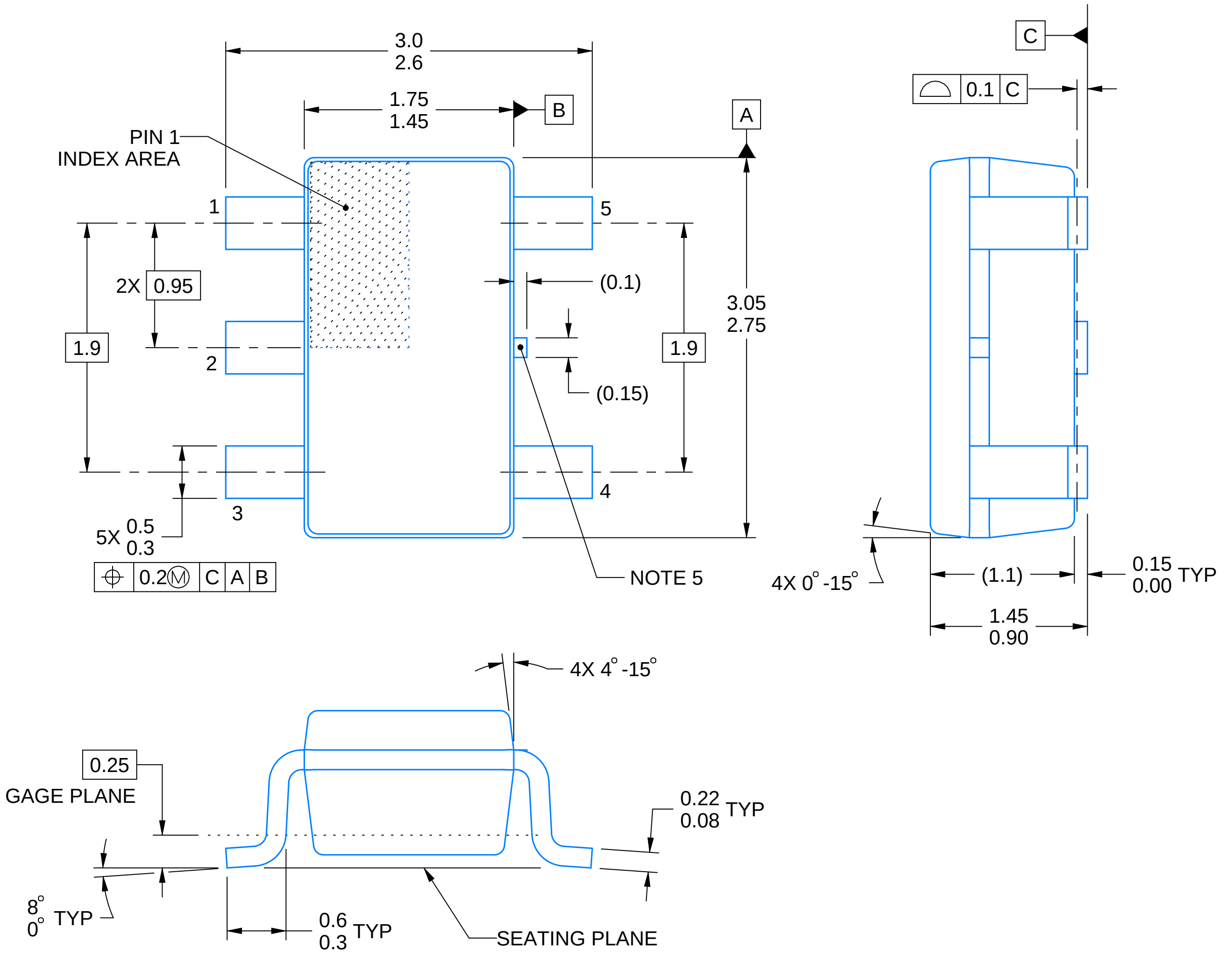
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2980IM5-ADJ/NOM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-ADJ/NOM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



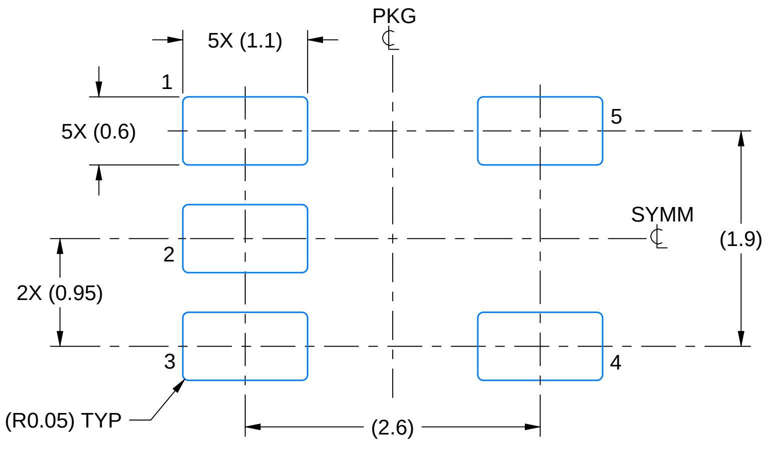
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2980IM5-ADJ/NOM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5-ADJ/NOM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5-ADJ/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2980IM5X-ADJ/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

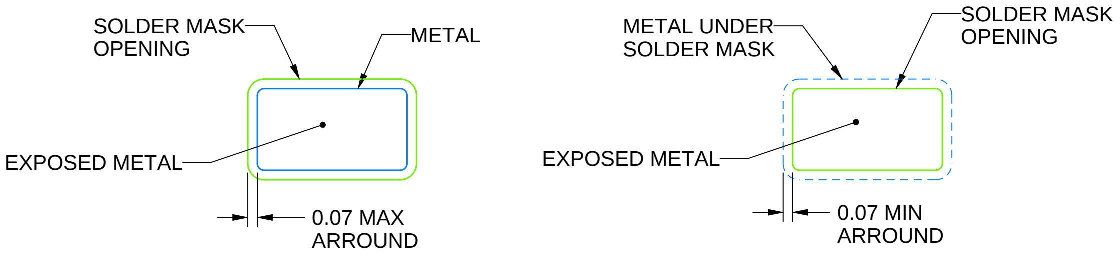


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



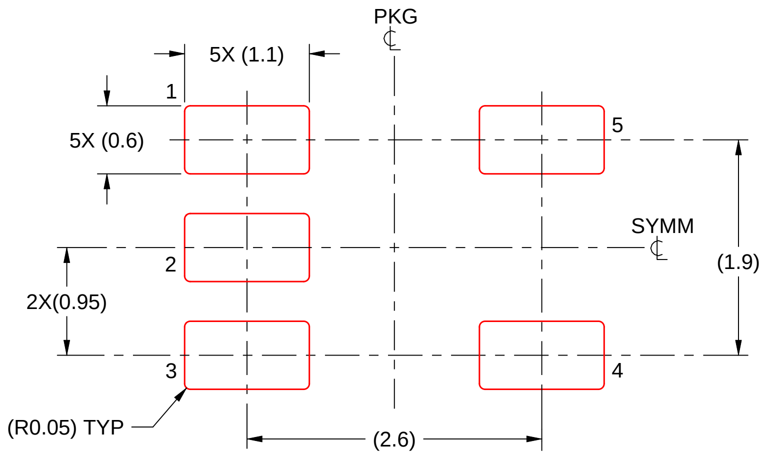
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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