LP2987/LP2988 Micropower, 200 mA Ultra Low-Dropout Voltage Regulator with Programmable Power-On Reset Delay; Low Noise Version Available (LP2988)

Check for Samples: LP2987, LP2988

FEATURES

- **Ultra Low Dropout Voltage**
- **Power-ON Reset Delay Requires Only One Component**
- **Bypass Pin for Reduced Output Noise (LP2988)**
- **Specified Continuous Output Current 200 mA**
- **Specified Peak Output Current > 250 mA**
- **SOIC-8 and VSSOP-8 Surface Mount Packages**
- **<2 µA Quiescent Current when Shutdown**
- **Low Ground Pin Current at All Loads**
- **0.5% Output Voltage Accuracy (“A” Grade)**
- **Wide Supply Voltage Range (16V Max)**
- **Overtemperature/overcurrent Protection**
- **−40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **Cellular Phone**
- **Palmtop/Laptop Computer**
- **Camcorder, Personal Stereo, Camera**

DESCRIPTION

The LP2987/8 are fixed-output 200 mA precision LDO voltage regulators with power-ON reset delay which can be implemented using a single external capacitor.

The LP2988 is specifically designed for noise-critical applications. A single external capacitor connected to the Bypass pin reduces regulator output noise.

Using an optimized VIP (Vertically Integrated PNP) process, these regulators deliver superior performance:

Dropout Voltage: 180 mV @ 200 mA load, and 1 mV @ 1 mA load (typical).

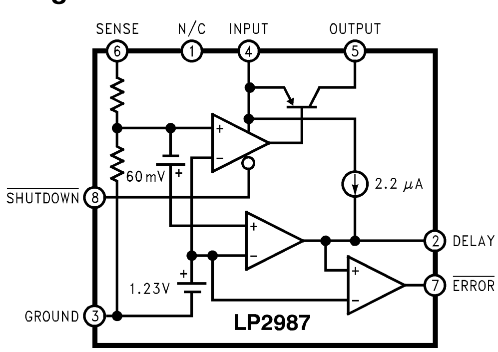
Ground Pin Current: 1 mA @ 200 mA load, and 200 µA @ 10 mA load (typical).

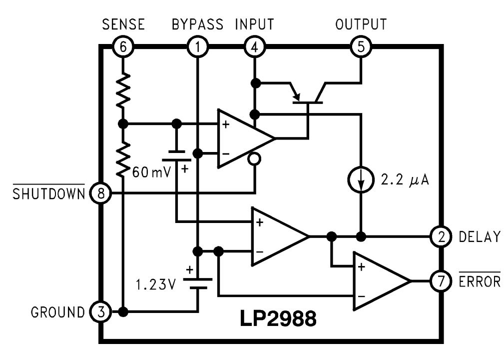
Sleep Mode: The LP2987/8 draws less than 2 µA quiescent current when shutdown pin is held low.

Error Flag/Reset: The error flag goes low when the output drops approximately 5% below nominal. This pin also provides a power-ON reset signal if a capacitor is connected to the DELAY pin.

Precision Output: Standard product versions of the LP2987 and LP2988 are available with output voltages of 5.0V, 3.8V, 3.3V, 3.2V, 3.0V, or 2.8V, with specified accuracy of 0.5% (“A” grade) and 1% (standard grade) at room temperature.

Block Diagram





Connection Diagram (LP2987)

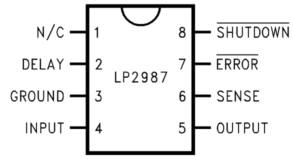


Figure 1. Top View
SOIC-8/VSSOP-8 Package
Surface Mount Packages
See Package Drawing Number D0008A/DGK0008A

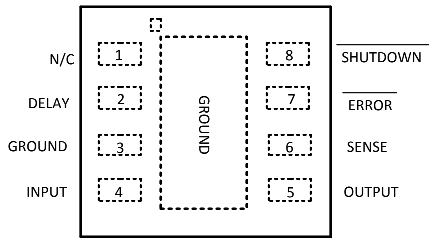


Figure 2. Top View
8-Lead WSON Surface Mount Package
See Package Drawing Number NGN0008A

Connection Diagram (LP2988)

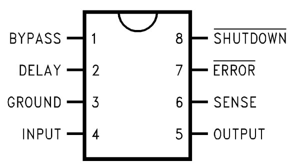


Figure 3. Top View
SOIC-8/VSSOP-8 Package
Surface Mount Packages
See Package Drawing Number D0008A/DGK0008A

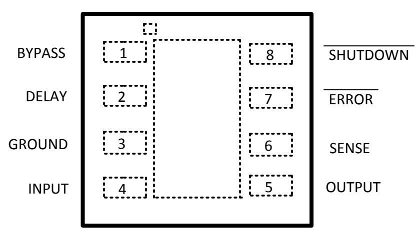


Figure 4. Top View
8-Lead WSON Surface Mount Package
See Package Drawing Number NGN0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS [1][2]

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating [3]	2 kV
Power Dissipation [4]	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +16V
Input Supply Voltage (Operating)	2.1V to +16V
Shutdown Pin	−0.3V to +16V
Sense Pin	−0.3V to +6V
Output Voltage (Survival) [5]	−0.3V to +16V
I_{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival) [6]	−0.3V to +16V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The ESD rating of the Bypass pin is 500V (LP2988 only). The ESD rating of the V_{IN} pin is 1kV and the Delay pin is ESD rated at 1.5kV.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$ The value of θ_{J-A} for the SOIC-8 (D) package is 160°C/W, and the VSSOP-8 (DGK) package is 200°C/W. The value θ_{J-A} for the WSON (NGN) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (literature number SNOA401). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LM2987/8 output must be diode-clamped to ground.
(6) The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see APPLICATION HINTS).

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X [1]		LM2987/8I-X.X [1]		Units
				Min	Max	Min	Max	
ΔV_O	Output Voltage Tolerance			−0.5	0.5	−1.0	1.0	$\%V_{NOM}$
		$0.1 mA < I_L < 200 mA$		−0.8	0.8	−1.6	1.6	
				−1.8	**1.8**	**−2.8**	**2.8**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation	$V_O(NOM) + 1V \le V_{IN} \le 16V$	0.007		0.014		0.014	%/V
					0.032		**0.032**	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X (1)		LM2987/8I-X.X (1)		Units
				Min	Max	Min	Max	
$V_{IN}–V_O$	Dropout Voltage (2)	I_L = 100 µA	1		2.0		2.0	mV
					3.5		**3.5**	
		I_L = 75 mA	90		120		120	
					170		**170**	
		I_L = 200 mA	180		230		230	
					350		**350**	
I_{GND}	Ground Pin Current	I_L = 100 µA	100		120		120	µA
					150		**150**	
		I_L = 75 mA	500		800		800	
					1400		**1400**	
		I_L = 200 mA	1		2.1		2.1	mA
					3.7		**3.7**	
		$V_{S/D}$ < 0.3V	0.05		**1.5**		**1.5**	µA
$I_O(PK)$	Peak Output Current	$V_{OUT} \geq V_O(NOM) - 5\%$	400	250		250		mA
$I_O(MAX)$	Short Circuit Current	R_L = 0 (Steady State) (3)	400					
e_n	LP2987 Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, V_{OUT} = 3.3V C_{OUT} = 10 µF	100					µV(RMS)
	LP2988 Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, V_{OUT} = 3.3V C_{OUT} = 10 µF C_{BYPASS} = .01 µF	20					
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple Rejection	f = 1 kHz, C_{OUT} = 10 µF C_{BYP} = 0 (LP2988)	65					dB
$\Delta V_{OUT}/\Delta T$	Output Voltage Temperature Coefficient	(4)	20					ppm/°C
I_{DELAY}	Delay Pin Current Source		2.2	1.6	2.8	1.6	2.8	µA
				1.4	**3.0**	**1.4**	**3.0**	
SHUTDOWN INPUT								
$V_{S/D}$	S/D Input Voltage (5)	V_H = O/P ON	1.4	**1.6**		**1.6**		V
		V_L = O/P OFF	0.55		**0.18**		**0.18**	
$I_{S/D}$	S/D Input Current	$V_{S/D}$ = 0	0		**−1**		**−1**	µA
		$V_{S/D}$ = 5V	5		**15**		**15**	

(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential.
(3) See TYPICAL PERFORMANCE CHARACTERISTICS curves.
(4) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.
(5) To prevent mis-operation, the Shutdown input must be driven by a signal that swings above V_H and below V_L with a slew rate not less than 40 mV/µs (see APPLICATION HINTS).

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X (1)		LM2987/8I-X.X (1)		Units
				Min	Max	Min	Max	
ERROR COMPARATOR								
I_{OH}	Output "HIGH" Leakage	V_{OH} = 16V	0.01		1		1	µA
					2		**2**	
V_{OL}	Output "LOW" Voltage	V_{IN} = V_O(NOM) − 0.5V, I_O(COMP) = 300 µA	150		220		220	mV
					350		**350**	
V_{THR} (MAX)	Upper Threshold Voltage		−4.6	−5.5	−3.5	−5.5	−3.5	%V_{OUT}
				−7.7	**−2.5**	**−7.7**	**−2.5**	
V_{THR} (MIN)	Lower Threshold Voltage		−6.6	−8.9	−4.9	−8.9	−4.9	
				−13.0	**−3.3**	**−13.0**	**−3.3**	
HYST	Hysteresis		2.0					

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA.

V_{OUT} vs Temperature

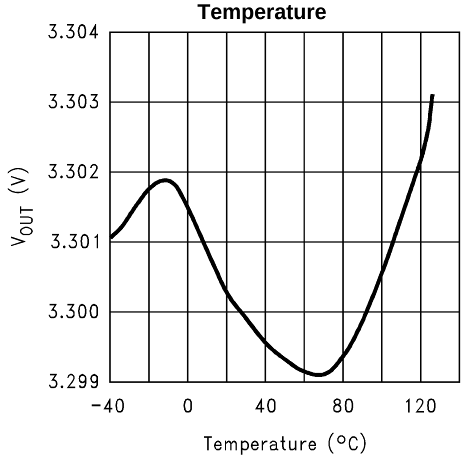


Figure 5.

Dropout Voltage vs Temperature

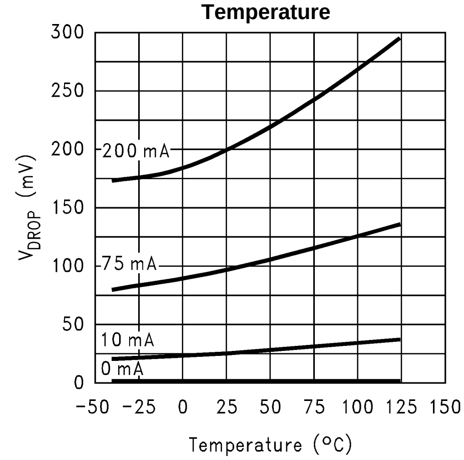


Figure 6.

Dropout Voltage vs Load Current

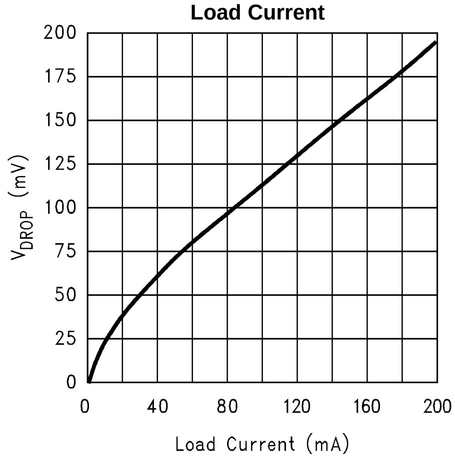


Figure 7.

Dropout Characteristics

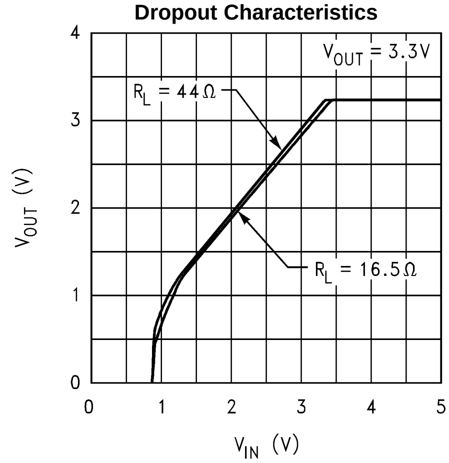


Figure 8.

Ground Pin Current vs Temperature and Load

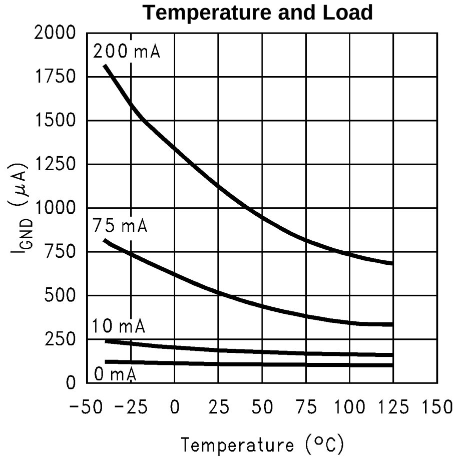


Figure 9.

Ground Pin Current vs Load Current

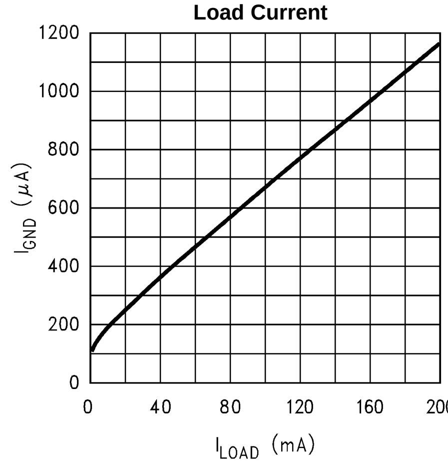


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA.

Input Current vs V_{IN}

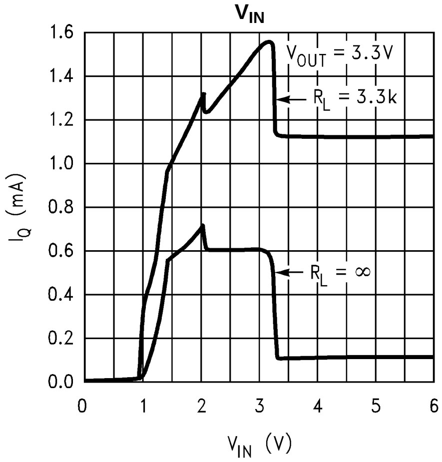


Figure 11.

Input Current vs V_{IN}

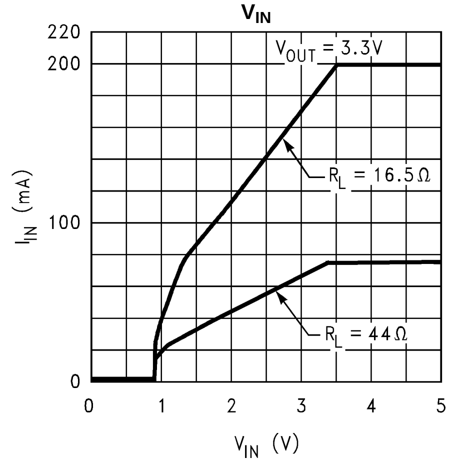


Figure 12.

Load Transient Response

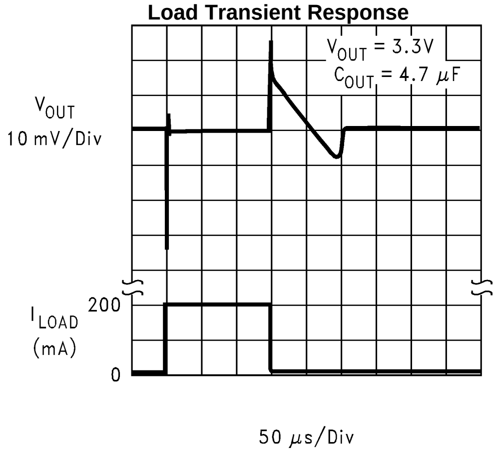


Figure 13.

Load Transient Response

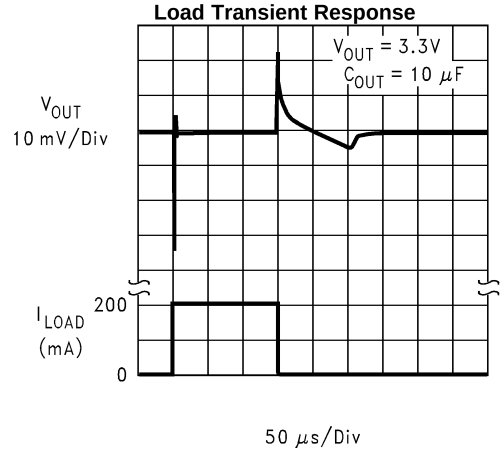


Figure 14.

Line Transient Response

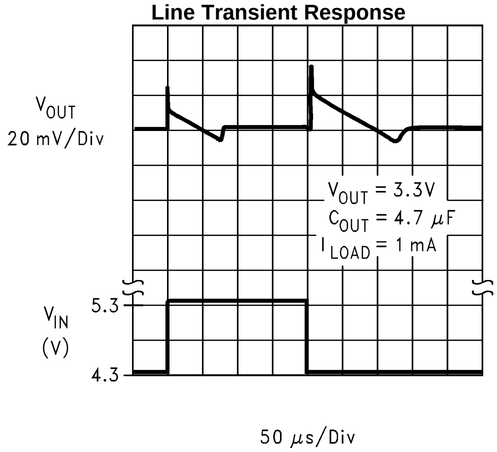


Figure 15.

Line Transient Response

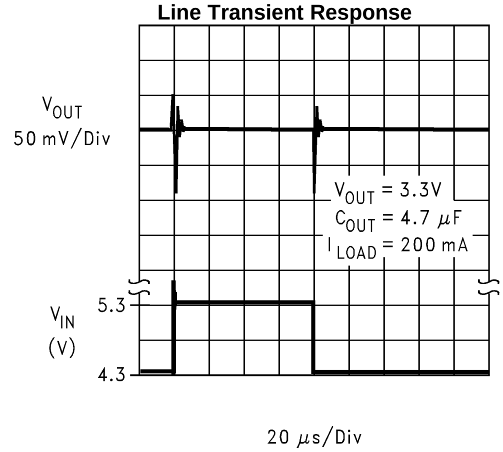


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA.

Turn-On Waveform

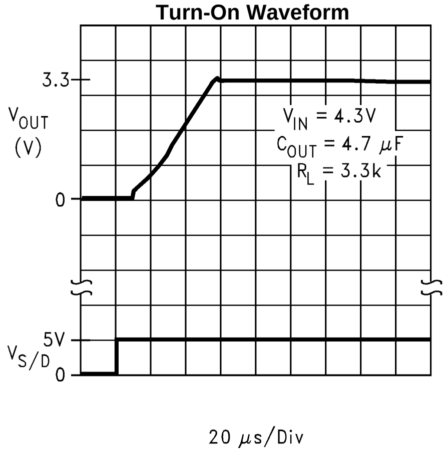


Figure 17.

Turn-On Waveform

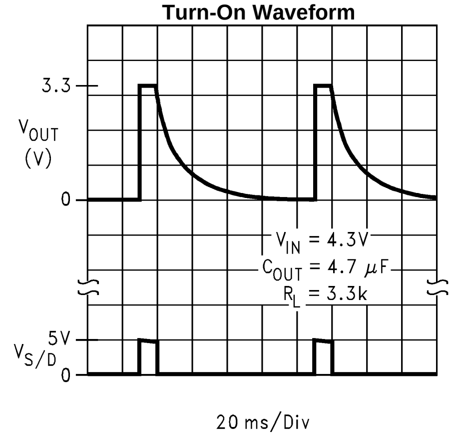


Figure 18.

Short Circuit Current

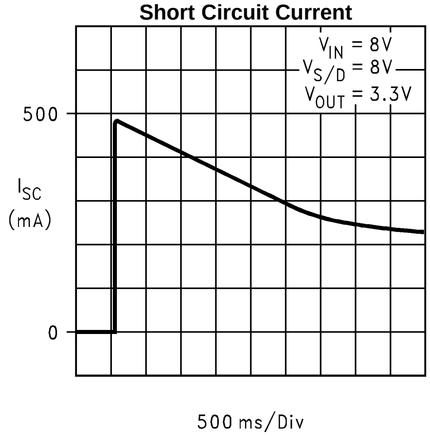


Figure 19.

Short Circuit Current

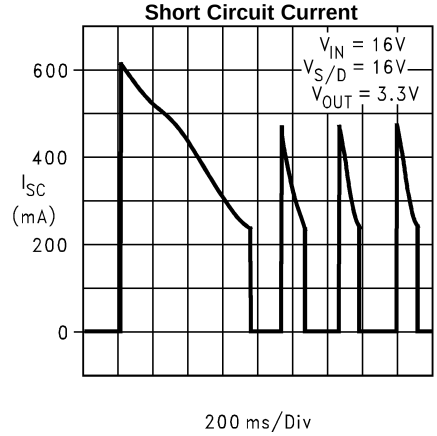


Figure 20.

Short Circuit Current vs Output Voltage

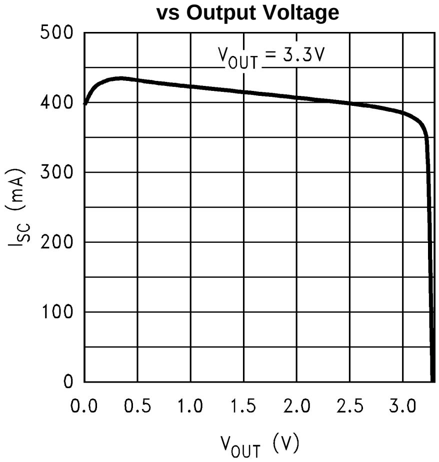


Figure 21.

Instantaneous Short Circuit Current vs Temperature

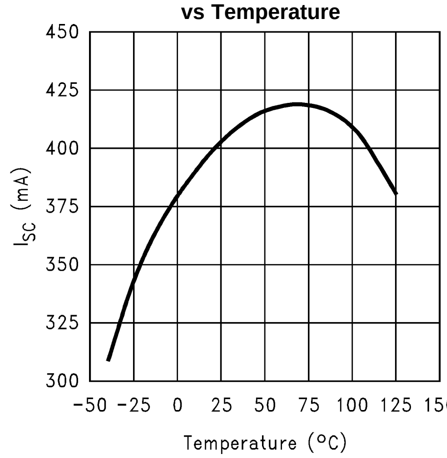


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA.

DC Load Regulation

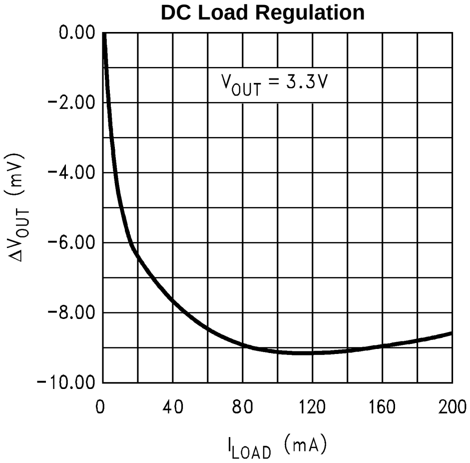


Figure 23.

Shutdown Pin Current vs Shutdown Pin Voltage

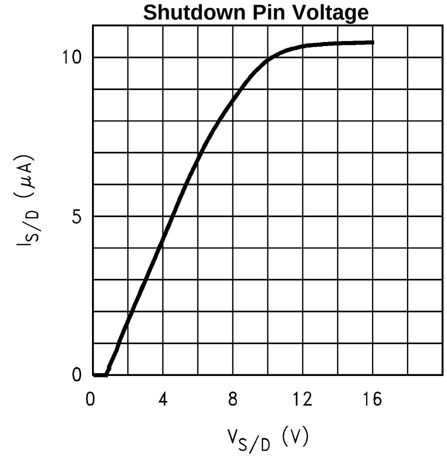


Figure 24.

Shutdown Voltage vs Temperature

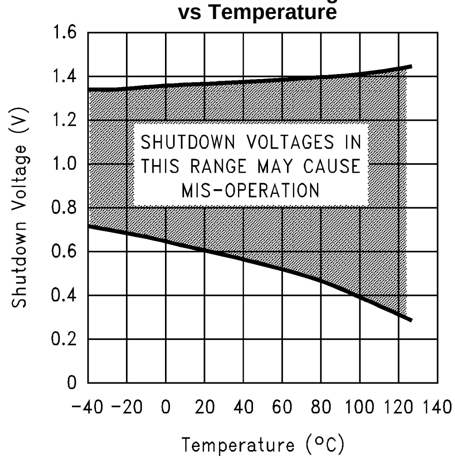


Figure 25.

Input to Output Leakage vs Temperature

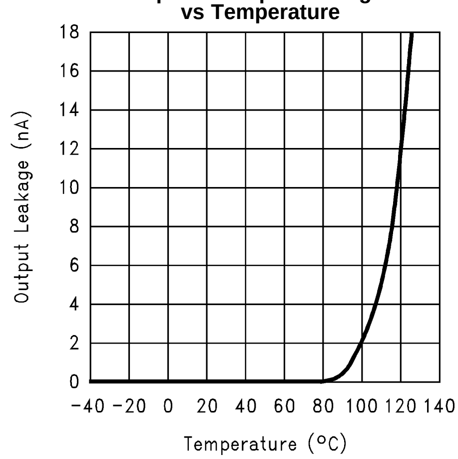


Figure 26.

Delay Pin Current vs V_{IN}

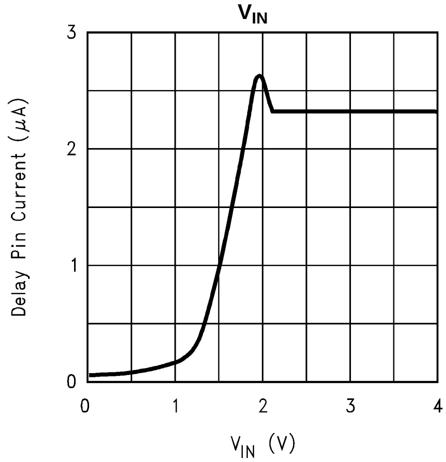


Figure 27.

Delay Pin Current vs Delay Pin Voltage

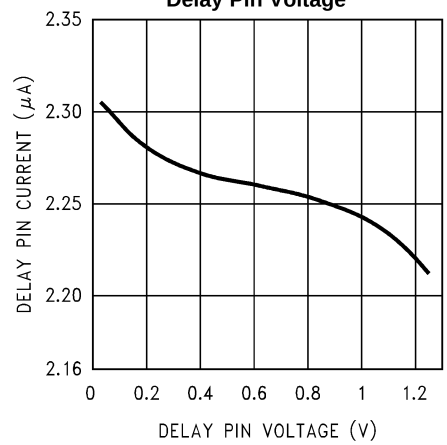


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA.

Delay Sink Current vs Temperature

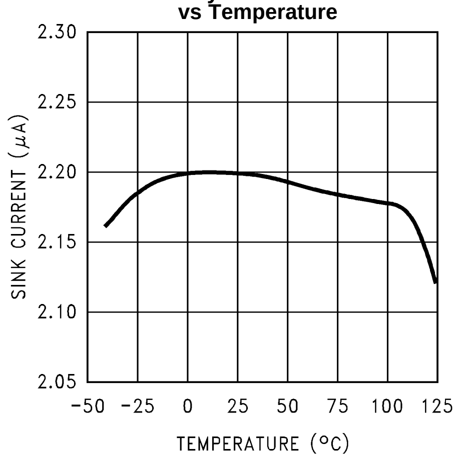


Figure 29.

Delay Sink Current vs Temperature

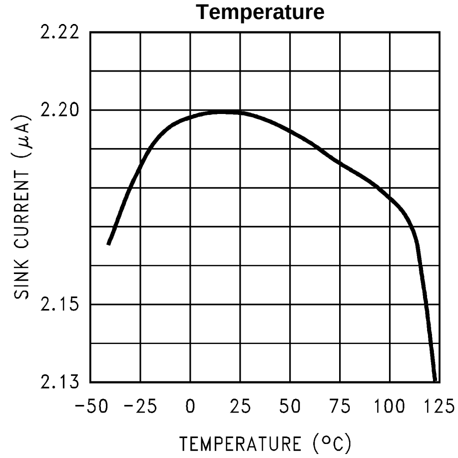


Figure 30.

Output Impedance vs Frequency

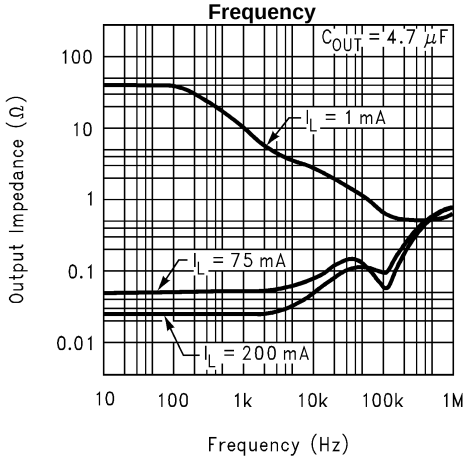


Figure 31.

Output Impedance vs Frequency

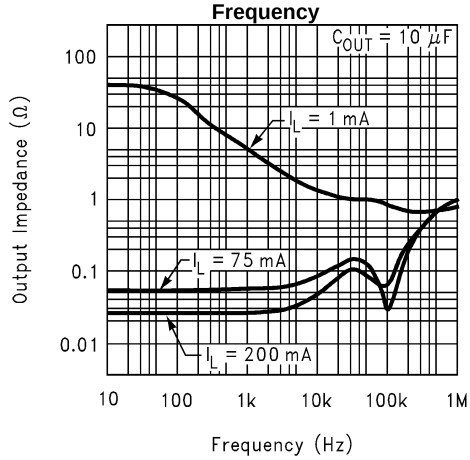


Figure 32.

Ripple Rejection (LP2987)

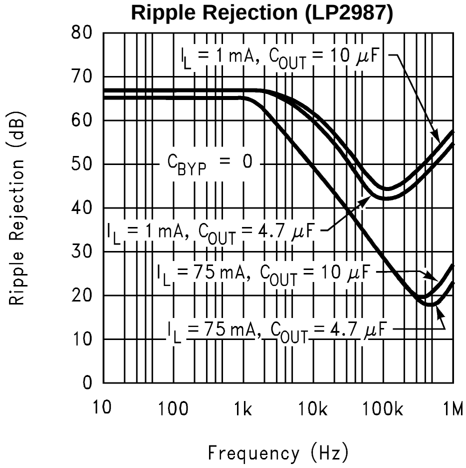


Figure 33.

Ripple Rejection (LP2988)

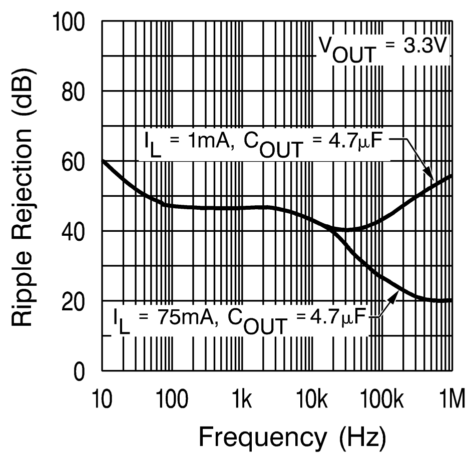


Figure 34.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA.

Output Noise Density (LP2987)

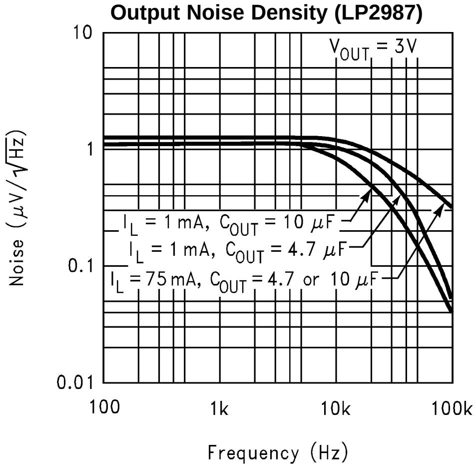


Figure 35.

Output Noise Voltage (LP2988)

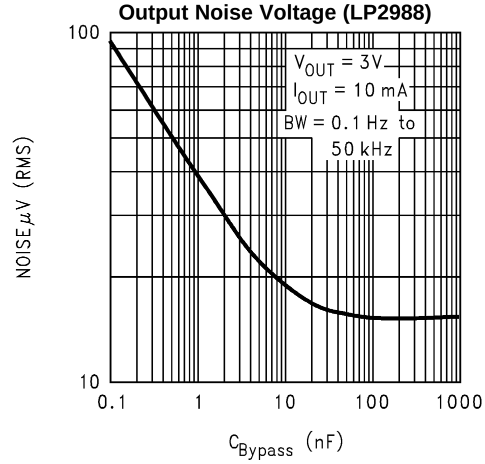


Figure 36.

Output Noise Density (LP2988)

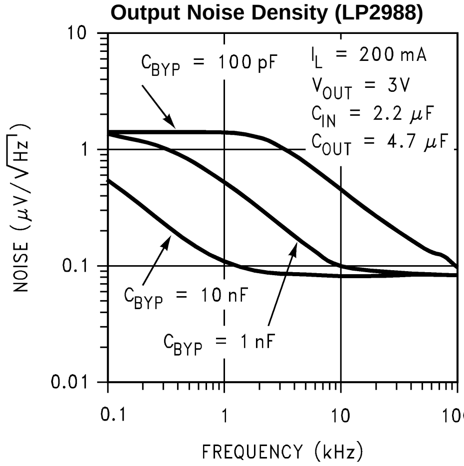


Figure 37.

Output Noise Density (LP2988)

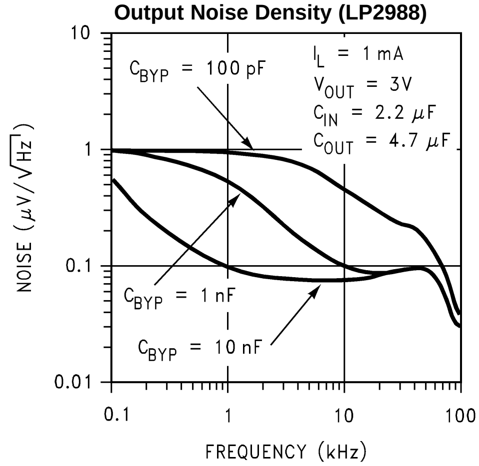


Figure 38.

Turn-On Time (LP2988)

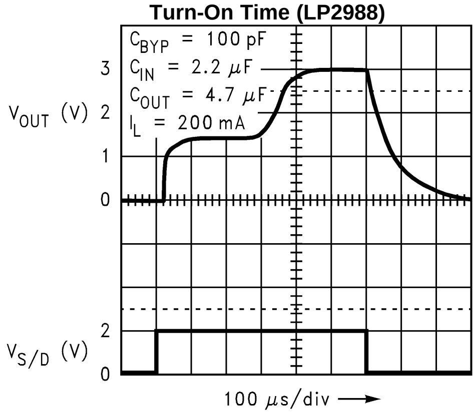


Figure 39.

Turn-On Time (LP2988)

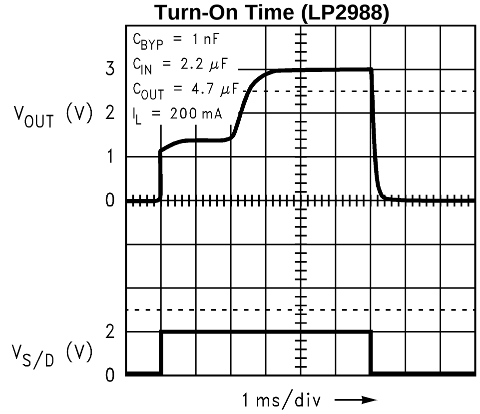


Figure 40.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA.

Turn-On Time (LP2988)

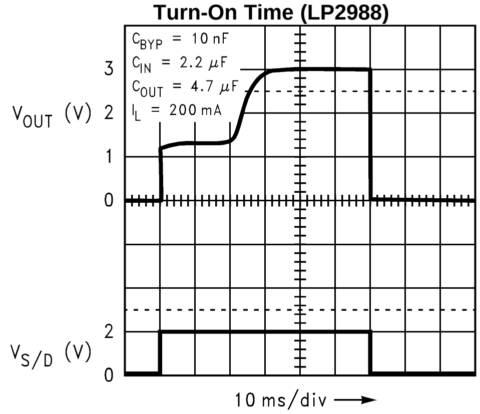


Figure 41.

BASIC APPLICATION CIRCUITS

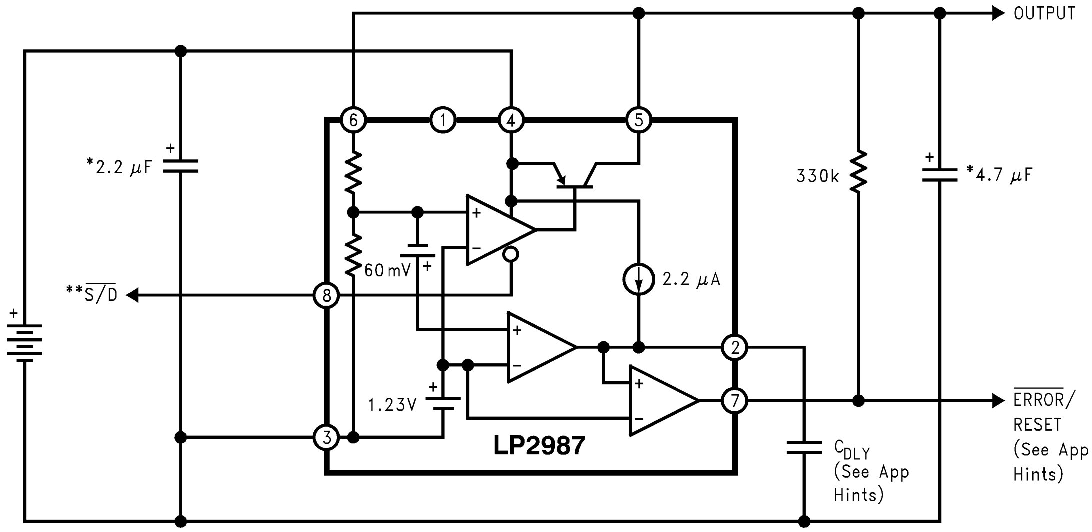
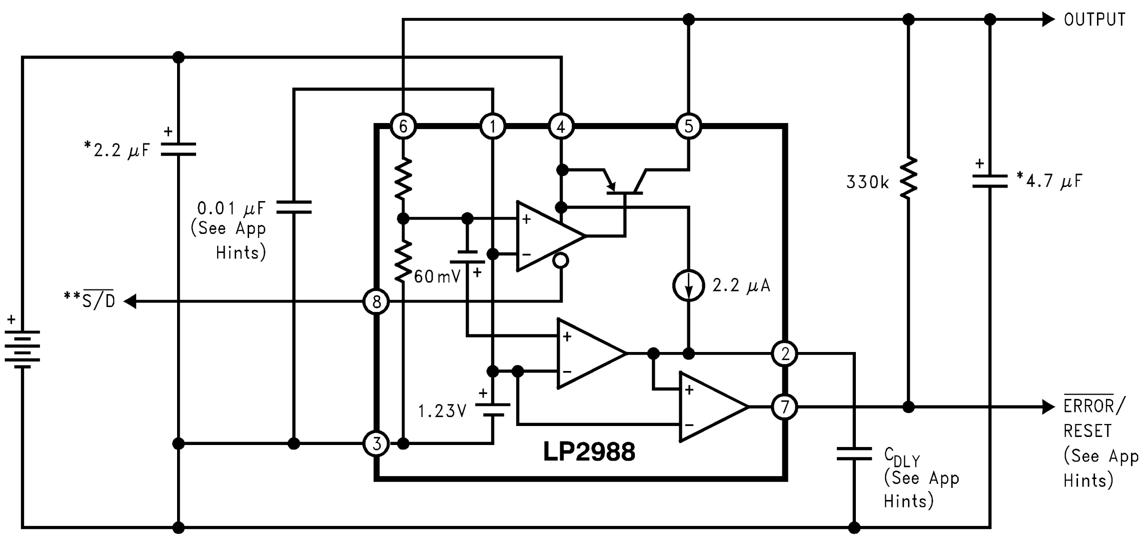


Figure 42.



*Capacitance value shown is minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.
**Shutdown must be actively terminated (see APPLICATION HINTS). Tie to INPUT (pin 4) if not used.

Figure 43.

APPLICATION HINTS

WSON Package Devices

The LP2987/LP2988 is offered in the 8 lead WSON surface mount package to allow for increased power dissipation compared to the SOIC-8 and the VSSOP-8. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187 (literature number SNOA401).

EXTERNAL CAPACITORS

As with any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor (≥ 2.2 µF) is required between the LP2987/8 input and ground (amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 0.5” from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor.

OUTPUT CAPACITOR: The output capacitor must meet the requirement for minimum amount of capacitance and also have an appropriate E.S.R. (equivalent series resistance) value.

Curves are provided which show the allowable ESR range as a function of load current for 3V and 5V outputs.

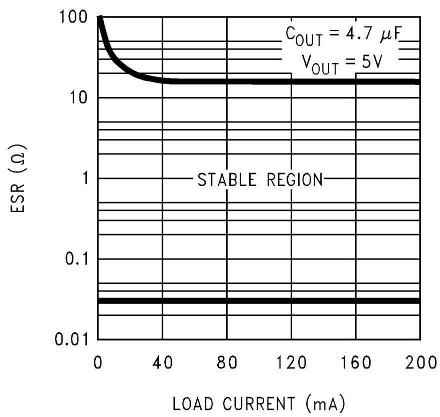


Figure 44. ESR Curves For 5V Output

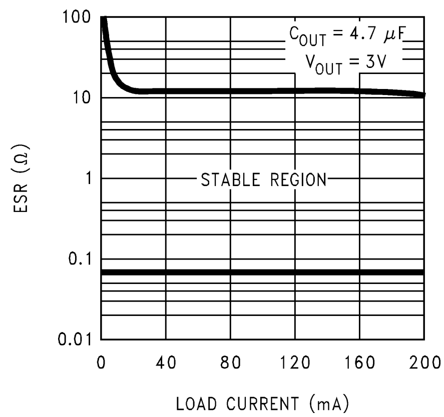


Figure 45. ESR Curves For 3V Output

IMPORTANT: The output capacitor must maintain its ESR in the stable region *over the full operating temperature range of the application* to assure stability.

The minimum required amount of output capacitance is 4.7 µF. Output capacitor size can be increased without limit.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. A good Tantalum capacitor will show very little variation with temperature, but a ceramic may not be as good (see next section).

The output capacitor should be located not more than 0.5” from the output pin and returned to a clean analog ground.

CAPACITOR CHARACTERISTICS

TANTALUM: A solid tantalum capacitor is the best choice for the output capacitor on the LM2987/8. Available from many sources, their typical ESR is very close to the ideal value required on the output of many LDO regulators.

Tantalums also have good temperature stability: a 4.7 µF was tested and showed only a 10% decline in capacitance as the temperature was decreased from +125°C to −40°C. The ESR increased only about 2:1 over the same range of temperature.

However, it should be noted that the increasing ESR at lower temperatures present in all tantalums can cause oscillations when marginal quality capacitors are used (where the ESR of the capacitor is near the upper limit of the stability range at room temperature).

CERAMIC: The ESR of ceramic capacitor can be low enough to cause an LDO regulator to oscillate: a 2.2 µF ceramic was measured and found to have an ESR of 15 mΩ.

If a ceramic capacitor is to be used on the LP2987/8 output, a 1Ω resistor should be placed in series with the capacitor to provide a minimum ESR for the regulator.

A disadvantage of ceramic capacitors is that their capacitance varies a lot with temperature: Large ceramic capacitors are typically manufactured with the Z5U temperature characteristic, which results in the capacitance dropping by 50% as the temperature goes from 25°C to 80°C.

This means you have to buy a capacitor with twice the minimum C_{OUT} to assure stable operation up to 80°C.

ALUMINUM: The large physical size of aluminum electrolytics makes them unsuitable for most applications. Their ESR characteristics are also not well suited to the requirements of LDO regulators. The ESR of a typical aluminum electrolytic is higher than a tantalum, and it also varies greatly with temperature.

A typical aluminum electrolytic can exhibit an ESR increase of 50X when going from 20°C to −40°C. Also, some aluminum electrolytics can not be used below −25°C because the electrolyte will freeze.

POWER-ON RESET DELAY

A power-on reset function can be easily implemented using the LP2987/8 by adding a single external capacitor to the Delay pin. The Error output provides the power-on reset signal when input power is applied to the regulator.

The reset signal stays low for a pre-set time period after power is applied to the regulator, and then goes high (see Timing Diagram below).

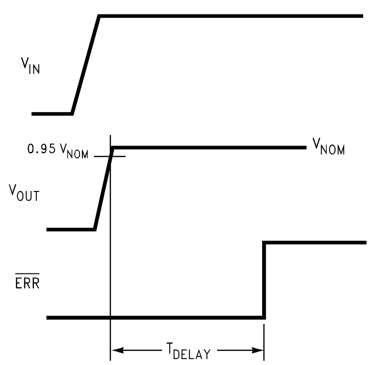


Figure 46. Timing Diagram for Power-Up

The external capacitor c_{DLY} sets the delay time (T_{DELAY}). The value of capacitor required for a given time delay may be calculated using the formula:

$C_{DLY} = T_{DELAY}/(5.59 \text{ X } 10^5)$

To simplify design, a plot is provided below which shows values of C_{DLY} versus delay time.

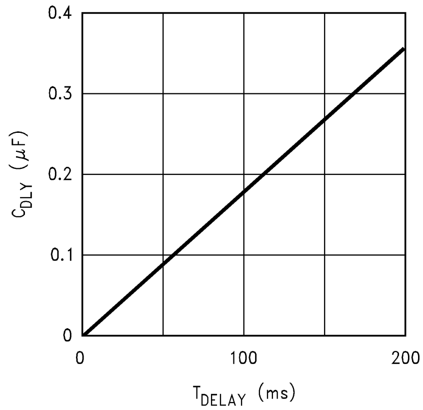


Figure 47. Plot of C_{DLY} vs T_{DELAY}

DETAILS OF ERR/RESET CIRCUIT OPERATION: (Refer to LP2987/8 Equivalent Circuit).

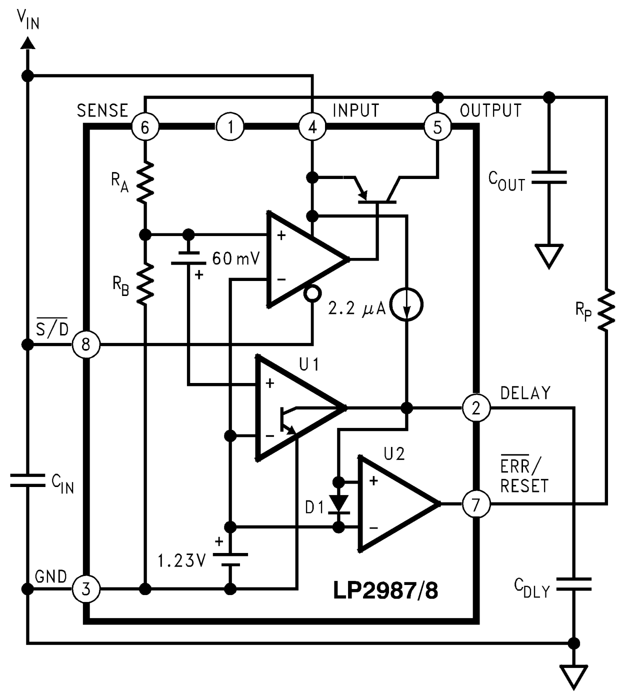


Figure 48. LP2987/8 Equivalent Circuit

The output of comparator U2 is the ERR/RESET flag. Since it is an open-collector output, it requires the use of a pull-up resistor (R_P). The 1.23V reference is tied to the inverting input of U2, which means that its output is controlled by the voltage applied to the non-inverting input.

The output of U1 (also an open-collector) will force the non-inverting input of U2 to go low whenever the LP2987/8 regulated output drops about 5% below nominal.

U1's inverting input is also held at 1.23V. The other input samples the regulated output through a resistive divider (R_A and R_B). When the regulated output is at nominal voltage, the voltage at the divider tap point will be 1.23V. If this voltage drops about 60 mV below 1.23V, the output of U1 will go low forcing the output of U2 low (which is the ERROR state).

Power-ON reset delay occurs when a capacitor (shown as C_{DLY}) is connected to the Delay pin. At turn-ON, this capacitor is initially fully discharged (which means the voltage at the Delay pin is 0V). The output of U1 keeps C_{DLY} fully discharged (by sinking the 2.2 µA from the current source) until the regulator output voltage comes up to within about 5% of nominal. At this point, U1's output stops sinking current and the 2.2 µA starts charging up C_{DLY}.

When the voltage across C_{DLY} reaches 1.23V, the output of U2 will go high (note that D1 limits the maximum voltage to about 2V).

SELECTING C_{DLY}: The maximum recommended value for this capacitor is 1 µF. The capacitor must not have excessively high leakage current, since it is being charged from a 2.2 µA current source.

Aluminum electrolytics can not be used, but good-quality tantalum, ceremic, mica, or film types will work.

SHUTDOWN INPUT OPERATION

The LP2987/8 is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed as V_H and V_L, respectively (see Electrical Characteristics).

It is also important that the turn-on (and turn-off) voltage signals applied to the Shutdown input have a slew rate which is not less than 40 mV/µs.

CAUTION

The regulator output state can not be ensured if a slow-moving AC (or DC) signal is applied that is in the range between V_H and V_L.

REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP2987/8 has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP2987/8 to 0.3V (see Absolute Maximum Ratings).

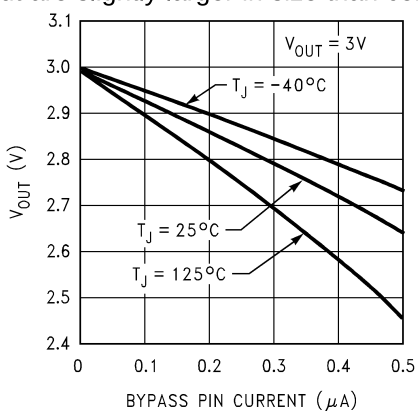
BYPASS CAPACITOR (LP2988)

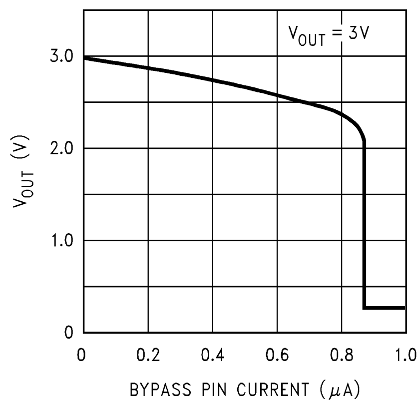
The capacitor connected to the Bypass pin must have very low leakage. The current flowing out of the Bypass pin comes from the Bandgap reference, which is used to set the output voltage. Since the Bandgap circuit has only a few microamps flowing in it, loading effects due to leakage current will cause a change in the regulated output voltage.

Curves are provided which show the effect of loading the Bypass pin on the regulated output voltage.

Care must be taken to ensure that the capacitor selected for bypass will not have significant leakage current over the operating temperature range of the application.

A high quality ceramic capacitor which uses either NPO or COG type dielectiric material will typically have very low leakage. Small surface-mount polypropolene or polycarbonate film capacitors also have extremely low leakage, but are slightly larger in size than ceramics.





REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2987AILD-3.0/NO.A	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L007A
LP2987AILD-3.0/NOPB	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L007A
LP2987AILD-5.0/NO.A	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L009A
LP2987AILD-5.0/NOPB	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L009A
LP2987AILDX-5.0/NO.A	Active	Production	WSON (NGN) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L009A
LP2987AILDX-5.0/NOPB	Active	Production	WSON (NGN) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L009A
LP2987AIMM-5.0/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L44A
LP2987AIMM-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L44A
LP2987AIMX-5.0/NO.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987A IM5.0
LP2987AIMX-5.0/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987A IM5.0
LP2987ILD-3.3/NOPB	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L008A B
LP2987ILD-3.3/NOPB.A	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L008A B
LP2987ILD-3.3/NOPB.B	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L008A B
LP2987IM-3.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0
LP2987IM-3.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0
LP2987IM-3.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0
LP2987IM-3.3/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.3
LP2987IM-3.3/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.3
LP2987IM-3.3/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.3
LP2987IM-5.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2987IM-5.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0
LP2987IM-5.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0
LP2987IMM-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L43B
LP2987IMM-3.3/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L43B
LP2987IMM-3.3/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L43B
LP2987IMM-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L44B
LP2987IMM-5.0/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L44B
LP2987IMM-5.0/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L44B
LP2987IMMX-3.3/NO.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L43B
LP2987IMMX-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L43B
LP2987IMX-3.0/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0
LP2987IMX-3.0/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0
LP2987IMX-3.0/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0
LP2987IMX-5.0/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0
LP2987IMX-5.0/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0
LP2987IMX-5.0/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0
LP2988AIM-5.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988A IM5.0
LP2988AIM-5.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988A IM5.0
LP2988AIM-5.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988A IM5.0
LP2988AIMM-3.0/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L49A
LP2988AIMM-3.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L49A
LP2988AIMM-3.3/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L50A
LP2988AIMM-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L50A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2988AIMM-5.0/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L51A
LP2988AIMM-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L51A
LP2988AIMX-3.3/NO.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988A IM3.3
LP2988AIMX-3.3/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988A IM3.3
LP2988ILD-3.8/NOPB	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L083A B
LP2988ILD-3.8/NOPB.A	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L083A B
LP2988ILD-3.8/NOPB.B	Active	Production	WSON (NGN) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L083A B
LP2988IM-5.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0
LP2988IM-5.0/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0
LP2988IM-5.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0
LP2988IMM-3.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L49B
LP2988IMM-3.0/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L49B
LP2988IMM-3.0/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L49B
LP2988IMM-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L50B
LP2988IMM-3.3/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L50B
LP2988IMM-3.3/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L50B
LP2988IMM-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L51B
LP2988IMM-5.0/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L51B
LP2988IMM-5.0/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L51B
LP2988IMMX-3.3/NO.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L50B
LP2988IMMX-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L50B
LP2988IMX-5.0/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0
LP2988IMX-5.0/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0
LP2988IMX-5.0/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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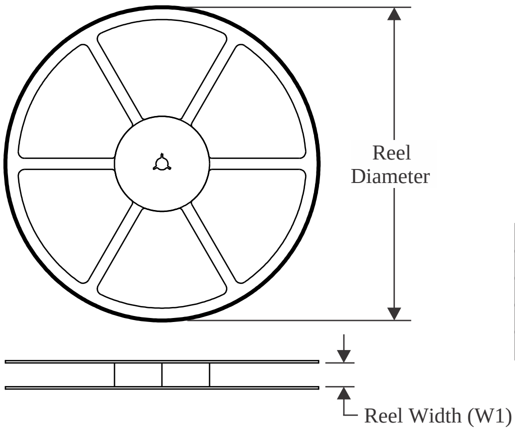
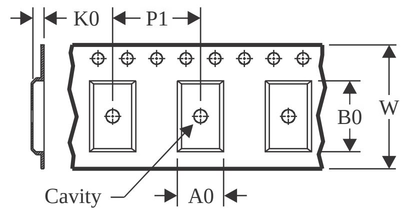
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

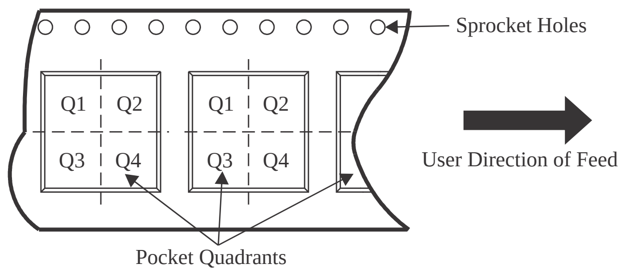


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

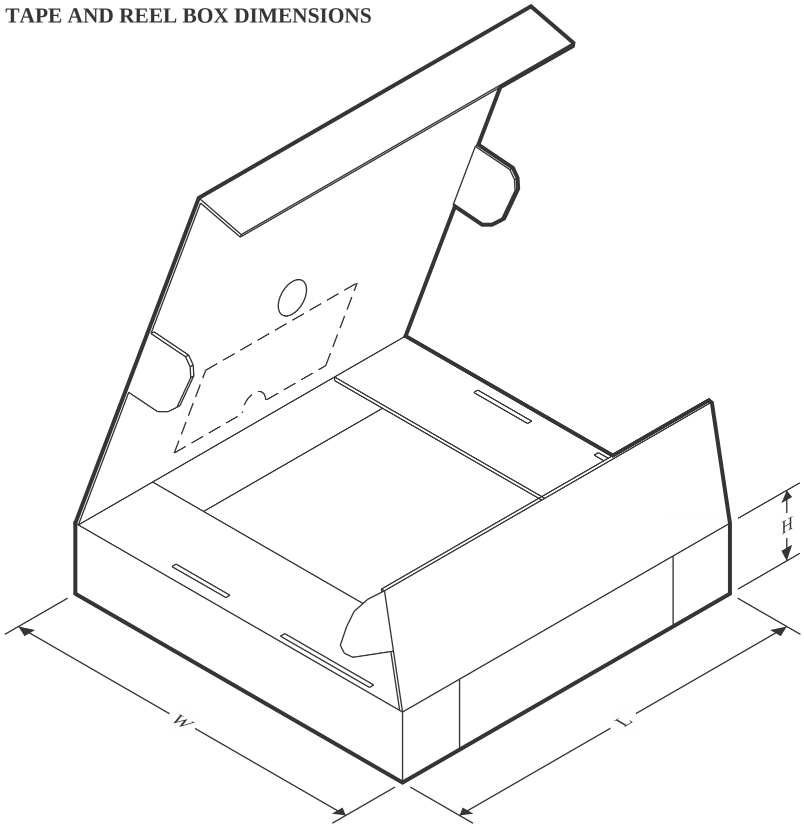


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2987AILD-3.0/NOPB	WSON	NGN	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AILD-5.0/NOPB	WSON	NGN	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AILDX-5.0/NOPB	WSON	NGN	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AIMM-5.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987AIMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2987ILD-3.3/NOPB	WSON	NGN	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987IMM-3.3/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMM-5.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMX-3.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2987IMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2988AIMM-3.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMM-3.3/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMM-5.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2988ILD-3.8/NOPB	WSON	NGN	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2988IMM-3.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMM-3.3/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMM-5.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

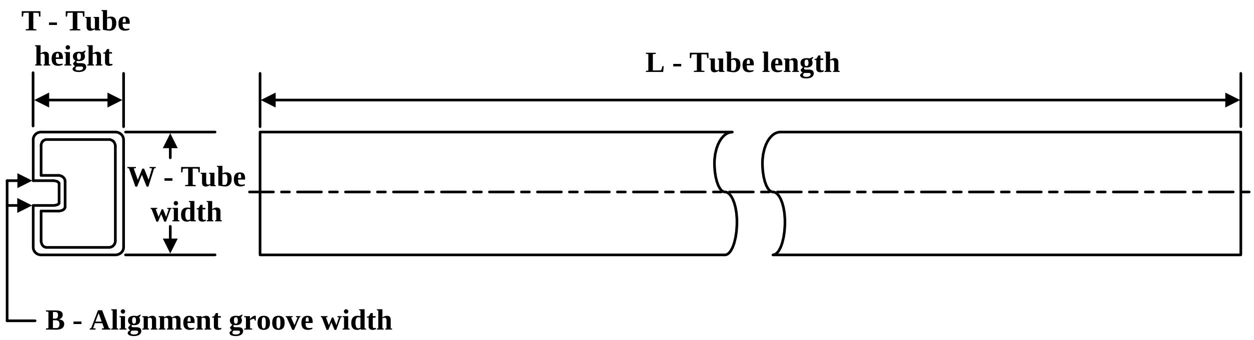


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2987AILD-3.0/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
LP2987AILD-5.0/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
LP2987AILDX-5.0/NOPB	WSON	NGN	8	4500	356.0	356.0	36.0
LP2987AIMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2987AIMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2987ILD-3.3/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
LP2987IMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2987IMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2987IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2987IMX-3.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2987IMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2988AIMM-3.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2988AIMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2988AIMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2988AIMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2988ILD-3.8/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
LP2988IMM-3.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2988IMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

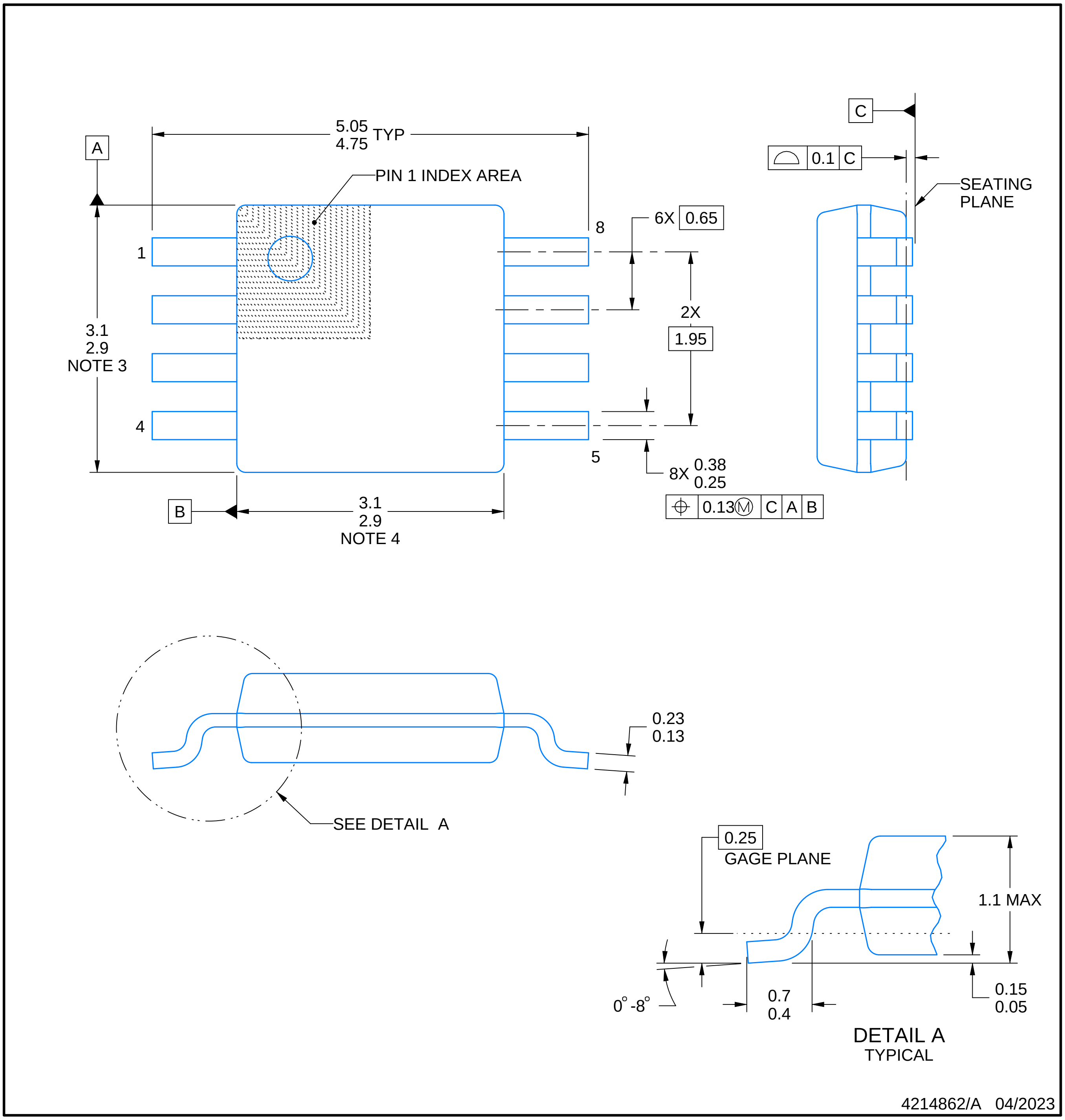
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2988IMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP2988IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2988IMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2987IM-3.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-3.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-3.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-3.3/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-3.3/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-3.3/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-5.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2987IM-5.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2988AIM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2988AIM-5.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2988AIM-5.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LP2988IM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2988IM-5.0/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2988IM-5.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

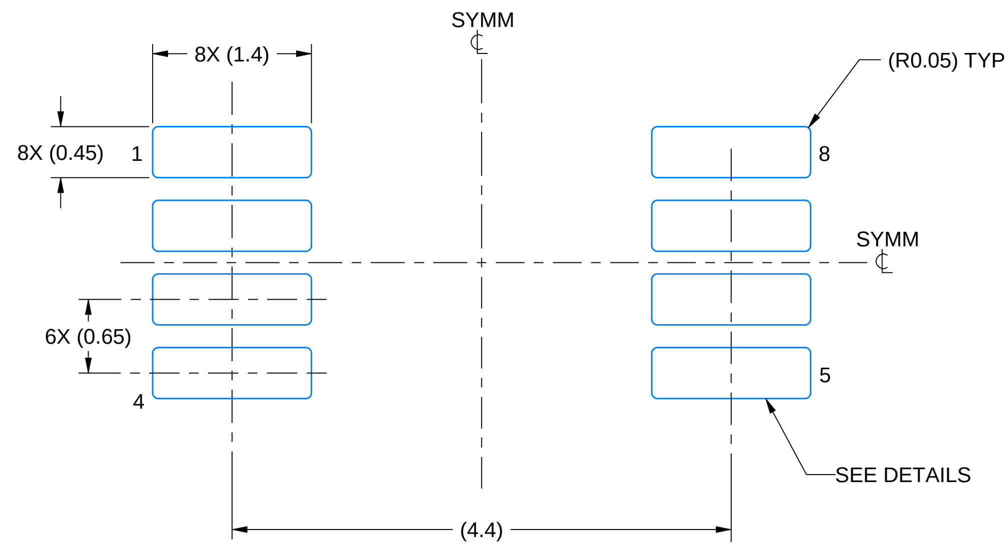


4214862/A 04/2023

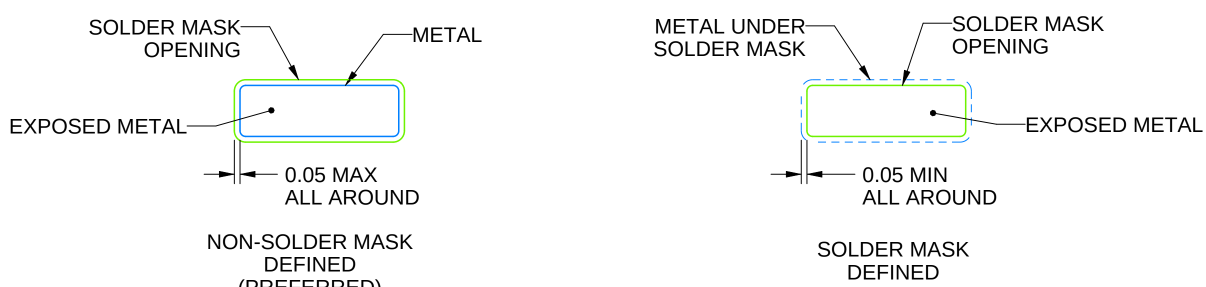
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

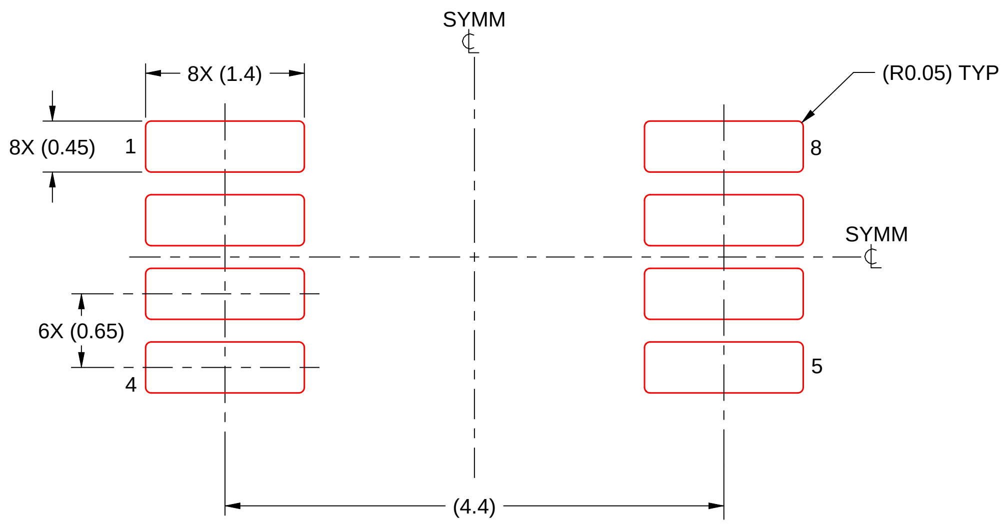


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

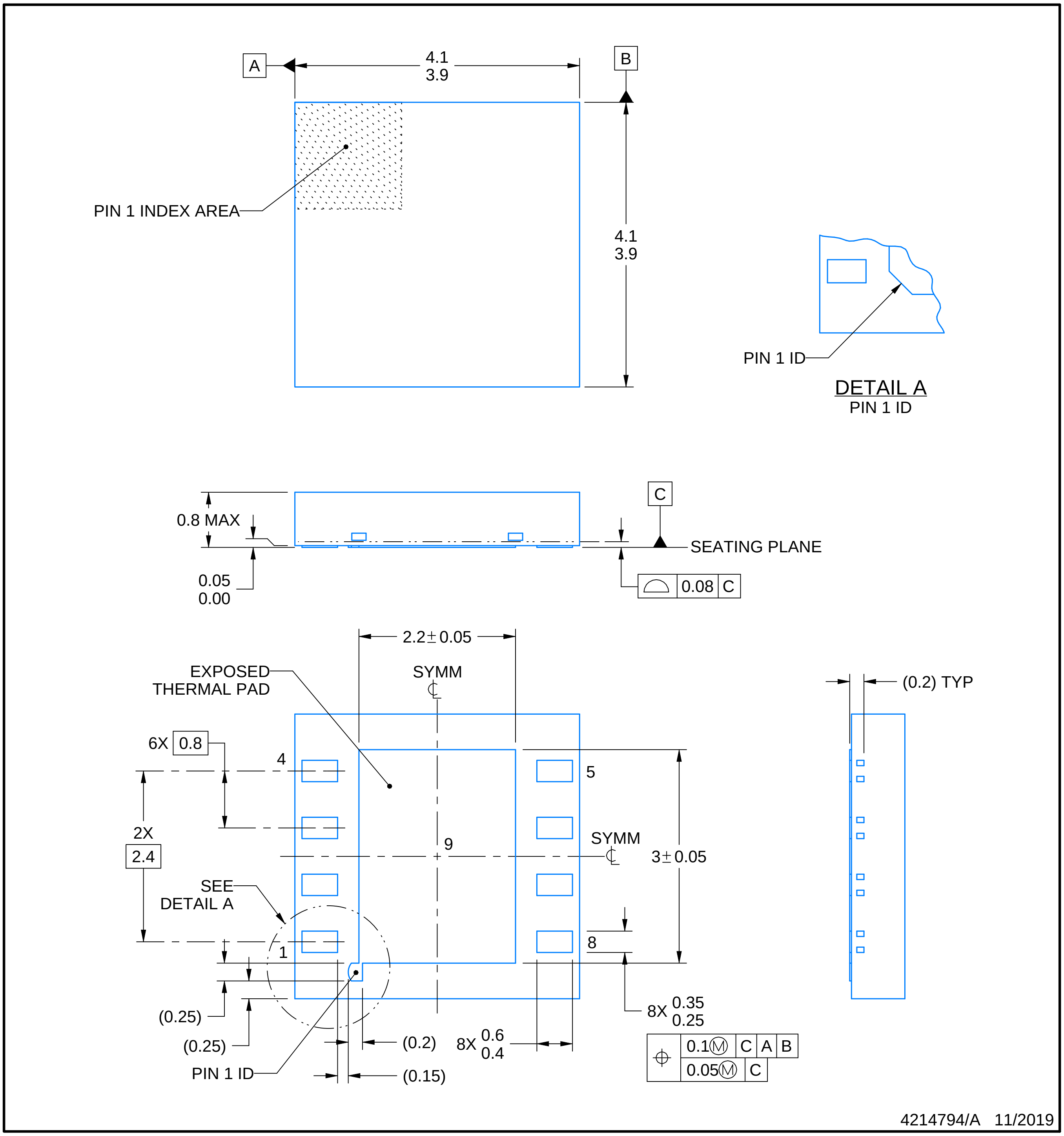


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

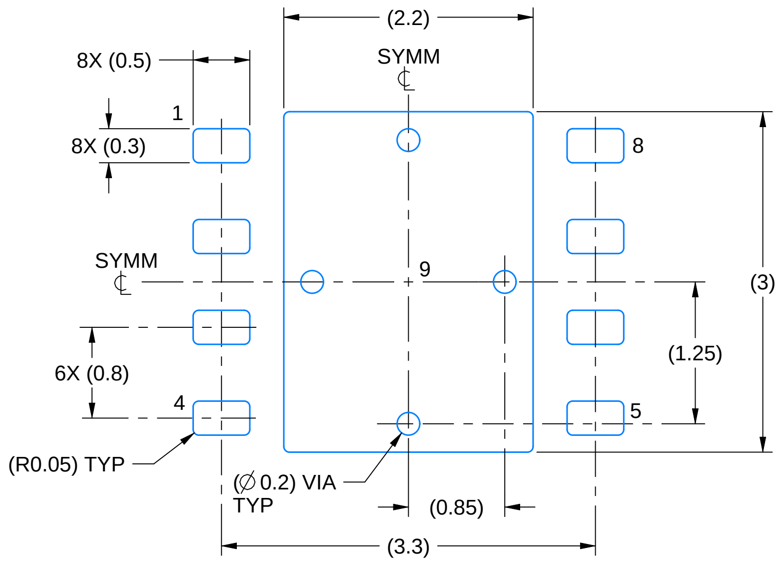
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

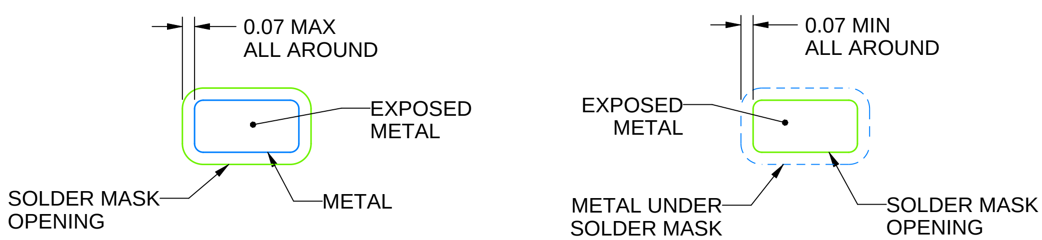


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

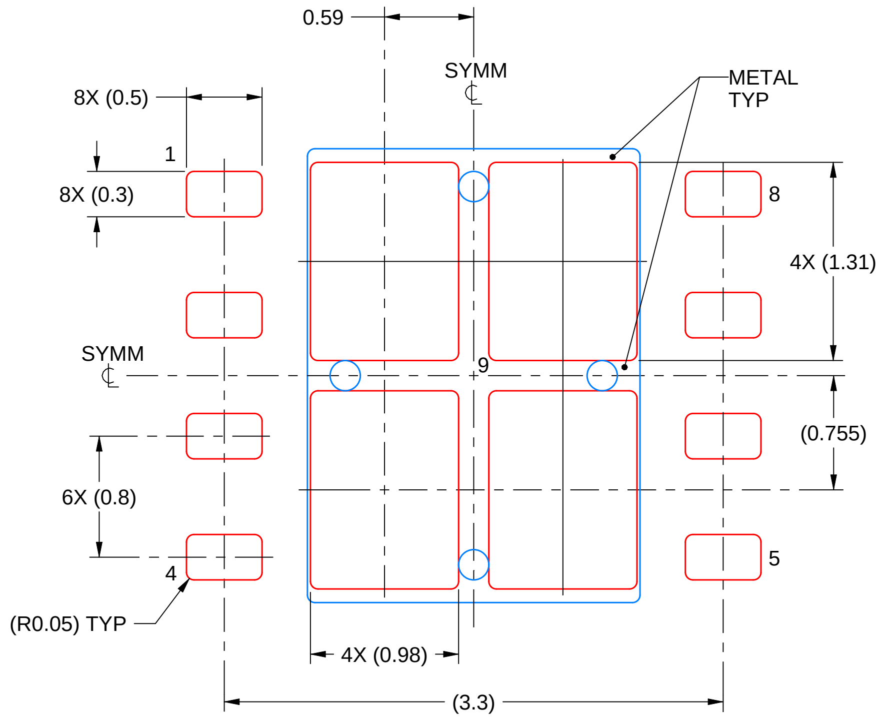
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214794/A 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



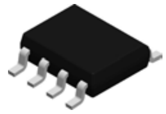
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214794/A 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

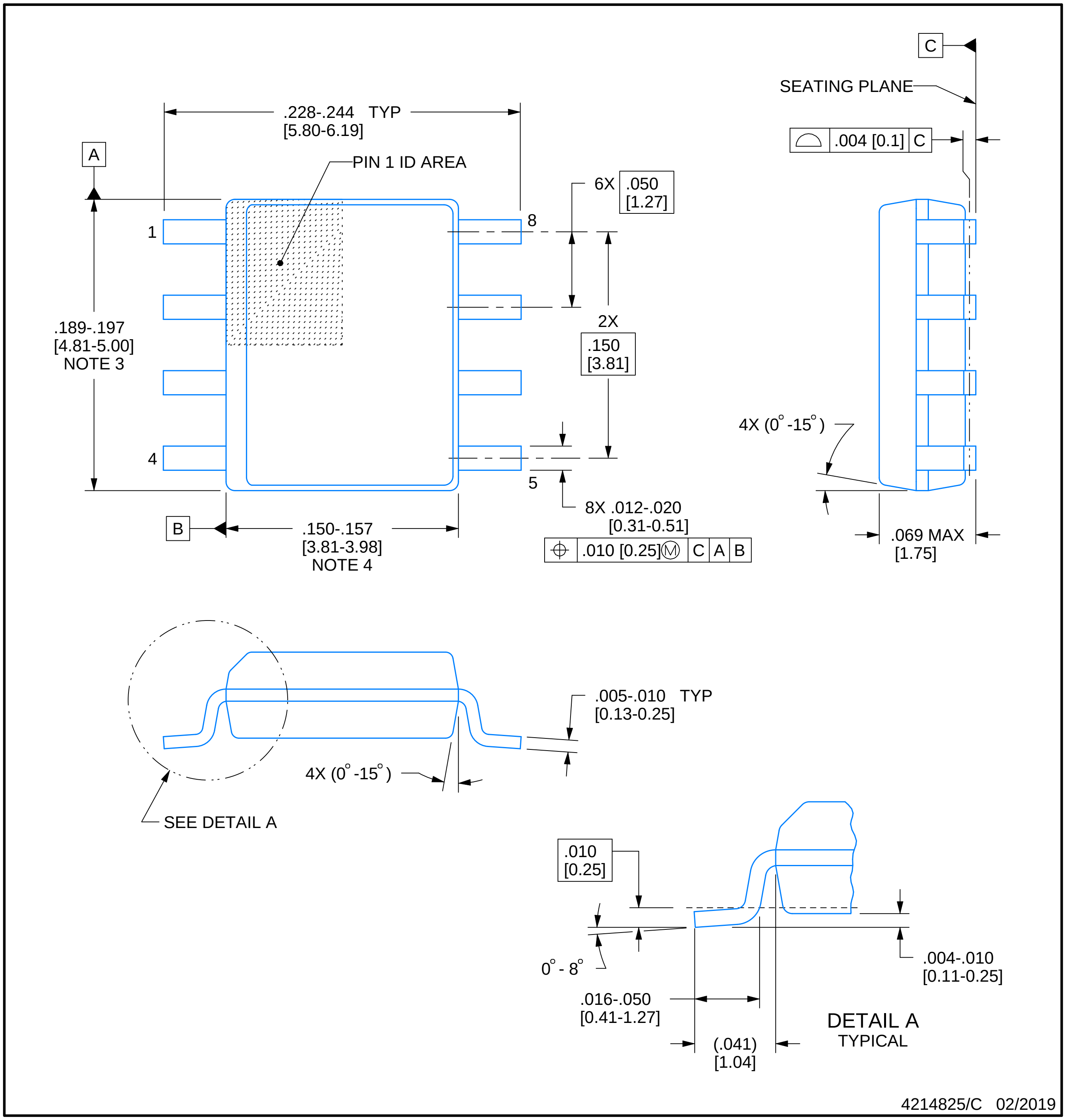


PACKAGE OUTLINE

D0008A

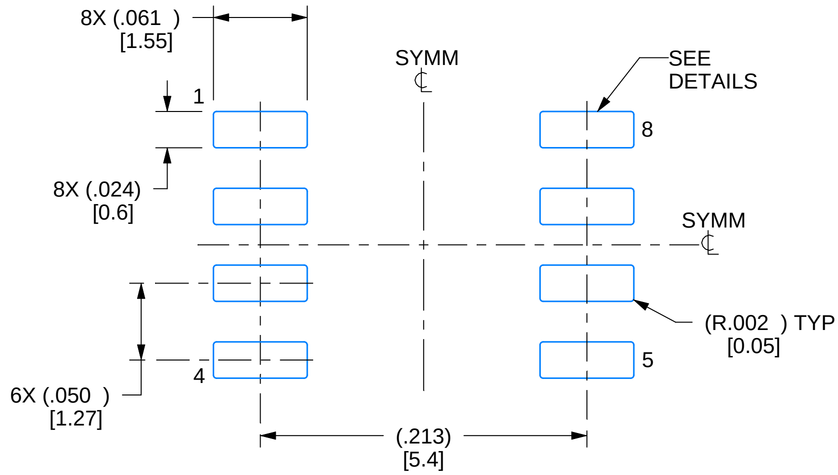
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

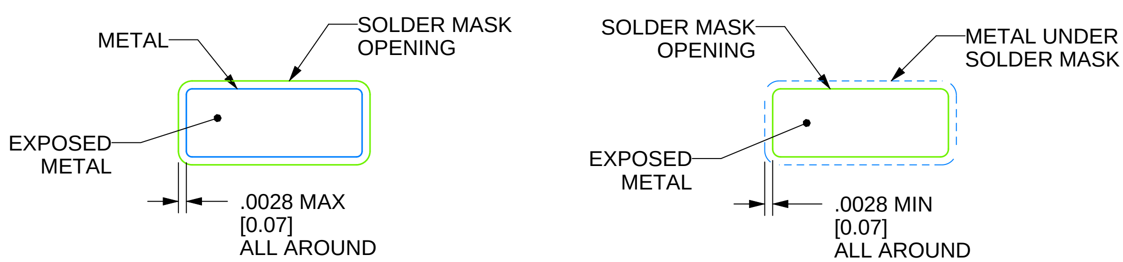


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

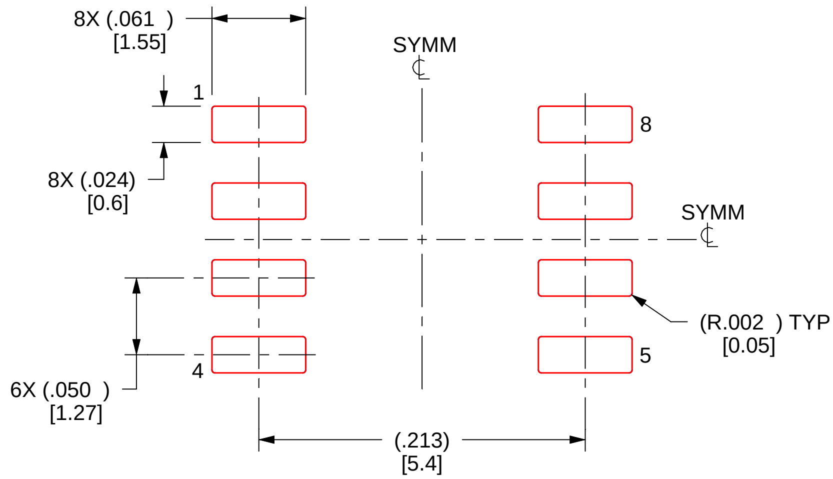
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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