

# LP3470A Ultra Low Power Voltage Supervisor With Programmable Delay and 1% Reset Threshold

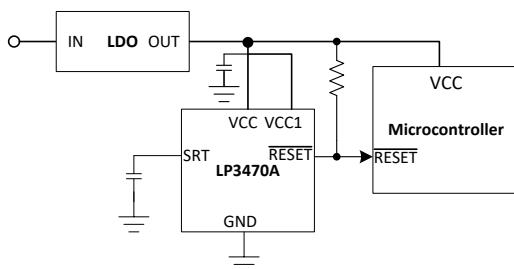
## 1 Features

- Pin-to-pin compatible with LP3470
- 5-Pin SOT-23 package
- Open-drain **RESET** output
- Programmable reset time-out period using an external capacitor
- Immune to short VCC transients
- $\pm 1\%$  Reset threshold accuracy (typical)
- Ultra-low quiescent current (0.3  $\mu$ A typical)
- **RESET** valid down to  $VCC = 0.95$  V

## 2 Applications

- Critical  $\mu$ P and  $\mu$ C power monitoring
- Intelligent instruments
- Computers
- Portable and battery-powered equipment
- Building automation: building security system, video surveillance
- Factory automation: field transmitters, position and proximity sensors
- Motor drives

### Basic Operating Circuit



## 3 Description

The LP3470A device is a micropower voltage supervisory circuit designed to monitor voltages within 1% of reset threshold overtemperature and is pin-to-pin compatible with existing TI device LP3470. The LP3470A device provides accurate, nano-power voltage monitoring with programmable delay.

The LP3470A asserts a reset signal whenever the VCC supply voltage falls below a reset threshold. The reset time-out period is adjustable using an external capacitor. Reset remains asserted for an interval (programmed by an external capacitor) after VCC has risen above the threshold voltage plus hysteresis.

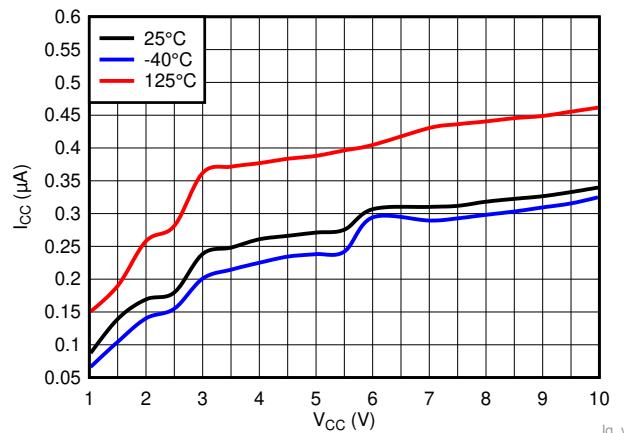
For information on available reset threshold voltage options, see *Mechanical, Packaging, and Orderable Information*.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3470A	SOT-23 (5)	1.60 mm x 2.90 mm

(1) For all available packages, see the Package Option Addendum at the end of the data sheet.

### Typical Supply Current for LP3470A



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2019) to Revision C	Page
• Changed Figure 12 caption to 0.01 $\mu$ F	13

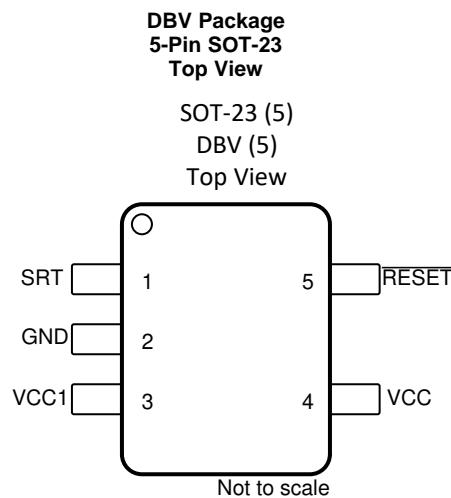
Changes from Revision A (October 2019) to Revision B	Page
• Changed Ultra-low quiescent current 0.35 to 0.3 to align with the Electrical Characteristics table	1
• Changed the typical value of $I_{CC}$ in the Electrical Characteristics table from 300 to 0.3 to match with the units of $\mu$ A	6

Changes from Original (July 2019) to Revision A	Page
• Initial Public Release	1

## 5 Device Comparison Table

PART NUMBER	$V_{IT^-}$ (typ) (VCC RAMPING DOWN)	$V_{IT^+}$ (typ) (VCC RAMPING UP)
LP3470A263	2.63 V	2.73 V
LP3470A275	2.75 V	2.85 V
LP3470A293	2.93 V	3.03 V
LP3470A308	3.08 V	3.28 V
LP3470A365	3.65 V	3.85 V
LP3470A400	4.0 V	4.2 V
LP3470A438	4.38 V	4.58 V
LP3470A463	4.63 V	4.83 V

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SRT	I	Set reset time-out. Connect a capacitor between this pin and ground to select the reset time-out period ( $t_D$ ). $t_D = 619 \times C_1 (C_{SRT} \text{ in } \mu\text{F} \text{ and } t_D \text{ in ms})$ . If no capacitor is connected, leave this pin floating.
2	GND	—	Ground pin.
3	VCC1	I	Can be connected to VCC or left floating. DO NOT CONNECT TO GND.
4	VCC	I	Supply voltage, and reset threshold monitor input.
5	RESET	O	Open-drain, active-low reset output. Connect to an external pullup resistor. $\overline{\text{RESET}}$ changes from high to low whenever the monitored voltage (VCC) drops below the reset threshold voltage ( $V_{IT}$ ). Once VCC exceeds the reset threshold ( $V_{IT}$ ) + hysteresis ( $V_{HYS}$ ), $\overline{\text{RESET}}$ remains low for the reset time-out period ( $t_D$ ) and then deasserts to logic high.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	VCC	−0.3	12	V
	RESET	−0.3	12	
	SRT	−0.3	5.5	
Current	RESET		±70	mA
Temperature <sup>(2)</sup>	Operating junction temperature, $T_J$	−40	150	°C
	Storage, $T_{stg}$	−65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) As a result of the low dissipated power in this device, it is assumed that  $T_J = T_A$ .

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	± 2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
$V_{CC}$	Input supply voltage	0.95	10	V
$V_{RESET}$ , $V_{\bar{RESET}}$	RESET pin voltage	0	10	V
$I_{RESET}$ , $I_{\bar{RESET}}$	RESET pin current	0	±5	mA
$T_J$	Junction temperature (free air temperature)	−40	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP3470A	UNIT
		DBV (SOT23-5)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.5	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	109.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	35.4	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	92.5	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

At  $0.95 \text{ V} \leq V_{CC} \leq 10 \text{ V}$ , SRT = Open,  $\overline{\text{RESET}}$  pull-up resistor ( $R_{\text{pull-up}}$ ) =  $100 \text{ k}\Omega$  to VCC, output reset load ( $C_{\text{LOAD}}$ ) =  $10 \text{ pF}$  and over the operating free-air temperature range –  $40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_J = 25^\circ\text{C}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{CC}$	Input supply voltage		0.95	10	V	
$V_{IT-}$	Negative-going input threshold accuracy	- $40^\circ\text{C}$ to $125^\circ\text{C}$	-1.5	1	1.5	%
$V_{HYS}$	Hysteresis on $V_{IT-}$ pin	$V_{IT-} = 3.08 \text{ V}$ to $4.63 \text{ V}$	175	200	225	mV
$V_{HYS}$	Hysteresis on $V_{IT-}$ pin	$V_{IT-} = 2.64 \text{ V}$ to $2.93 \text{ V}$	75	100	125	mV
$I_{CC}$	Supply current into VCC pin	$VCC = 0.95 \text{ V} < V_{CC} < 10 \text{ V}$ $VCC > V_{IT+}^{(1)}$ $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		0.3	1	$\mu\text{A}$
$R_{SRT}$	SRT pin internal resistance <sup>(2)</sup>		350	500	650	$\text{k}\Omega$
$V_{POR}$	Power on Reset Voltage <sup>(3)</sup>	$V_{OL(\text{max})} = 0.2 \text{ V}$ $I_{OUT(\text{Sink})} = 5.6 \mu\text{A}$			950	mV
$V_{OL}$	Low level output voltage	$1.5 \text{ V} < V_{CC} < 5 \text{ V}$ $V_{CC} < V_{IT-}$ $I_{OUT(\text{Sink})} = 2 \text{ mA}$			200	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	$\overline{\text{RESET}}$ pin in High Impedance, $V_{CC} = V_{RESET} = 5.5 \text{ V}$ $V_{IT+} < V_{CC}$			90	nA

(1)  $V_{IT+} = V_{HYS} + V_{IT-}$ .

(2) This parameter is guaranteed by design and characterization

(3)  $V_{POR}$  is the minimum  $V_{DD}$  voltage level for a controlled output state.  $V_{DD}$  slew rate  $\leq 100\text{mV}/\mu\text{s}$

## 7.6 Timing Requirements

At  $0.95 \text{ V} \leq V_{CC} \leq 10 \text{ V}$ , SRT = Open,  $\overline{\text{RESET}}$  pull-up resistor ( $R_{\text{pull-up}}$ ) =  $100 \text{ k}\Omega$  to VCC, output reset load ( $C_{\text{LOAD}}$ ) =  $10 \text{ pF}$  and over the operating free-air temperature range –  $40^\circ\text{C}$  to  $125^\circ\text{C}$ , VCC slew rate  $< 100\text{mV} / \mu\text{s}$ , unless otherwise noted. Typical values are at  $T_J = 25^\circ\text{C}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{P\_HL}$	Propagation detect delay for VCC falling below $V_{IT-}$	$V_{CC} = V_{IT+} \text{ to } (V_{IT-}) - 10\%^{(1)}$		15	30	$\mu\text{s}$
$t_D$	Reset time delay	$SRT \text{ pin = open}$ $V_{CC} = (V_{IT-} - 1\text{V}) \text{ to } (V_{IT+} + 1\text{V})$			50	$\mu\text{s}$
		$SRT \text{ pin = } 10 \text{ nF}^{(2)(3)}$		6.2		ms
		$SRT \text{ pin = } 1 \mu\text{F}^{(2)(3)}$		619		ms
$t_{GI\_VIT-}$	Glitch immunity $V_{IT-}$	5% $V_{IT-}$ overdrive <sup>(3)(4)</sup>		10		$\mu\text{s}$

(1)  $t_{P\_HL}$  measured from threshold trip point ( $V_{IT-}$ ) to  $V_{OL}$

(2) Ideal capacitor

(3) Parameter is guaranteed by design.

(4) Overdrive % =  $[(V_{CC}/V_{IT-}) - 1] \times 100\%$

## 7.7 Typical Characteristics

Typical characteristics show the typical performance of the LP3470A device. Test conditions are at  $T_A = T_J = 25^\circ\text{C}$  (unless otherwise noted).

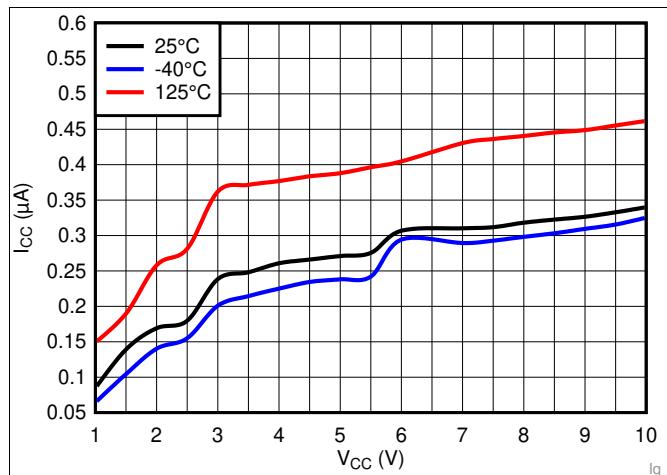


Figure 1. Supply Current vs Supply Voltage

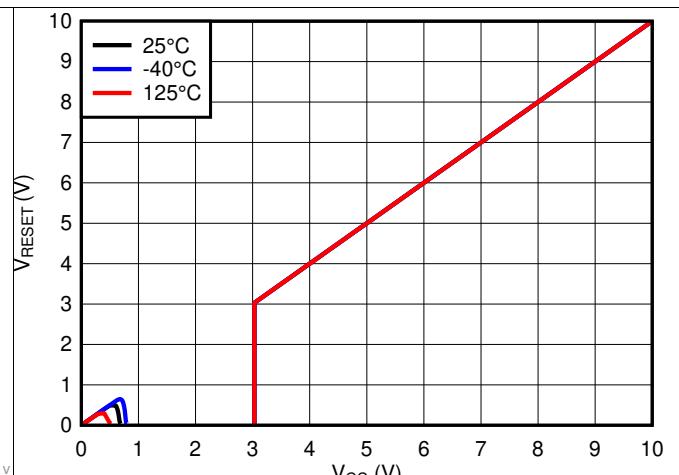


Figure 2. Output Voltage vs Supply Voltage for LP3470A293

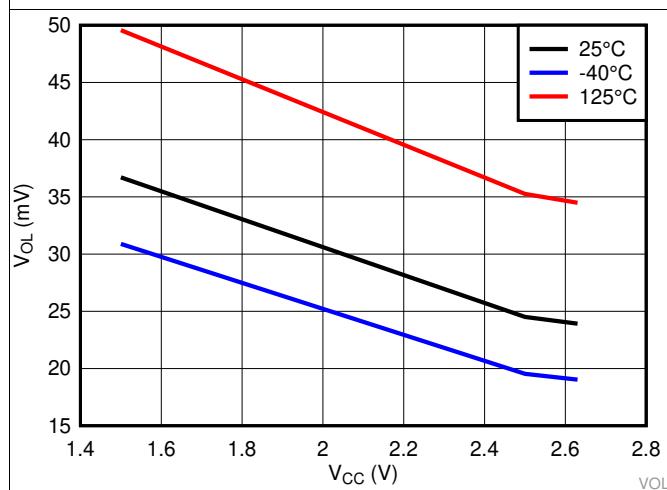


Figure 3. Low Level Output Voltage vs Supply Voltage

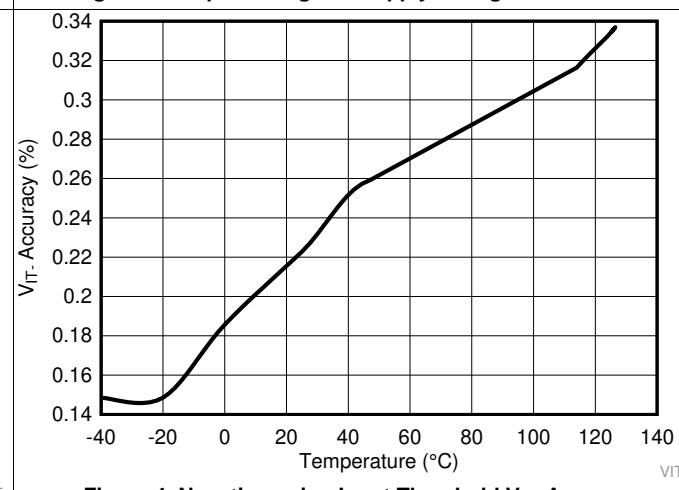


Figure 4. Negative-going Input Threshold  $V_{IT^-}$  Accuracy vs Temperature

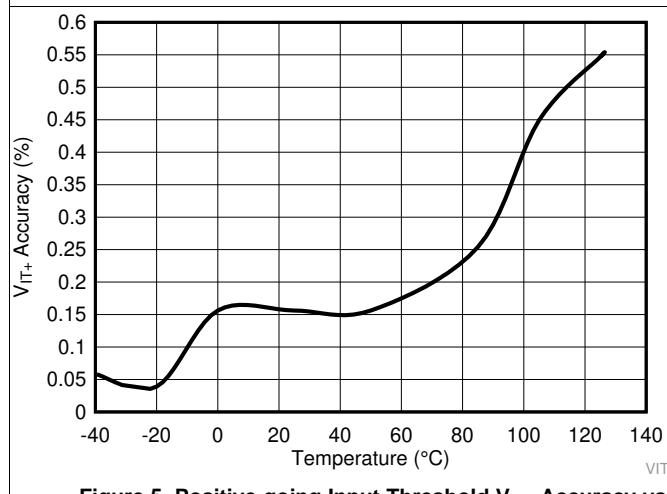


Figure 5. Positive-going Input Threshold  $V_{IT^+}$  Accuracy vs Temperature

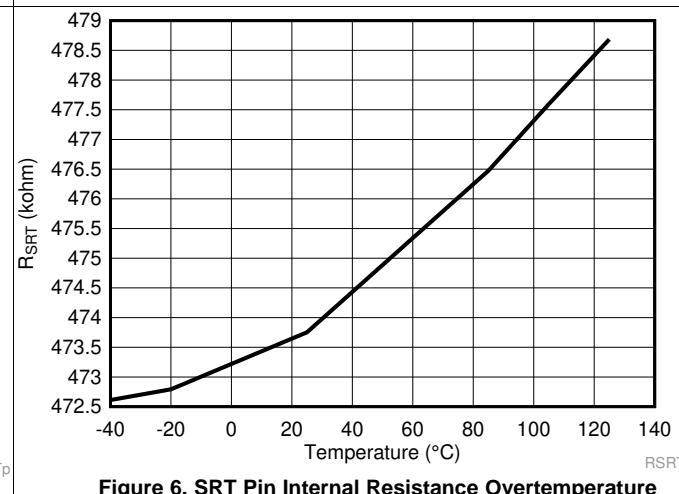


Figure 6. SRT Pin Internal Resistance Overtemperature

## Typical Characteristics (continued)

Typical characteristics show the typical performance of the LP3470A device. Test conditions are at  $T_A = T_J = 25^\circ\text{C}$  (unless otherwise noted).

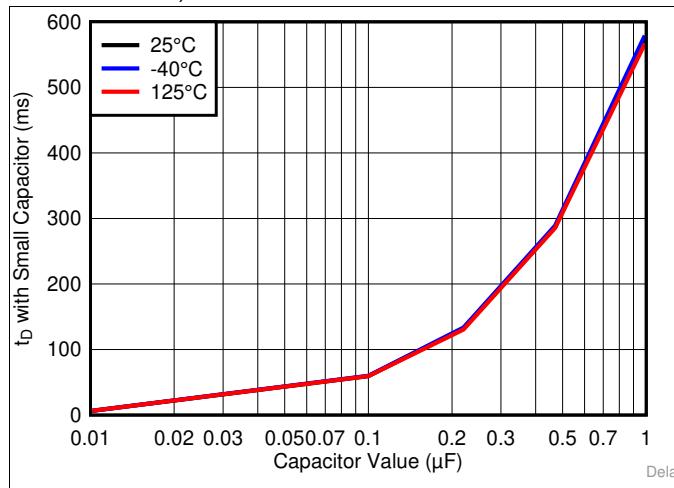


Figure 7. Reset Time Delay vs Small Capacitor Values

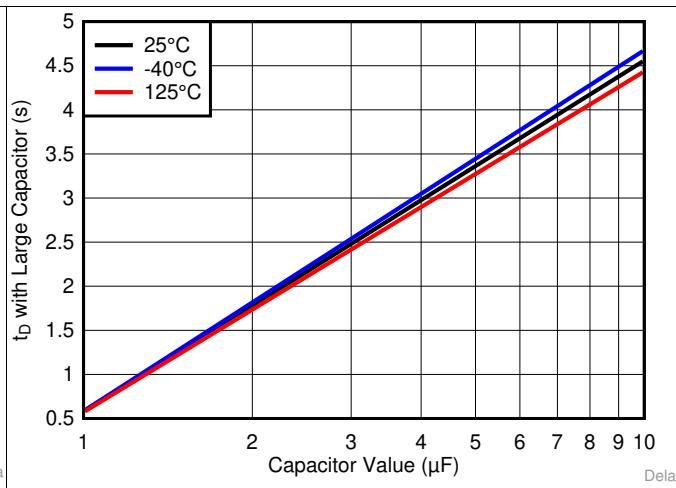


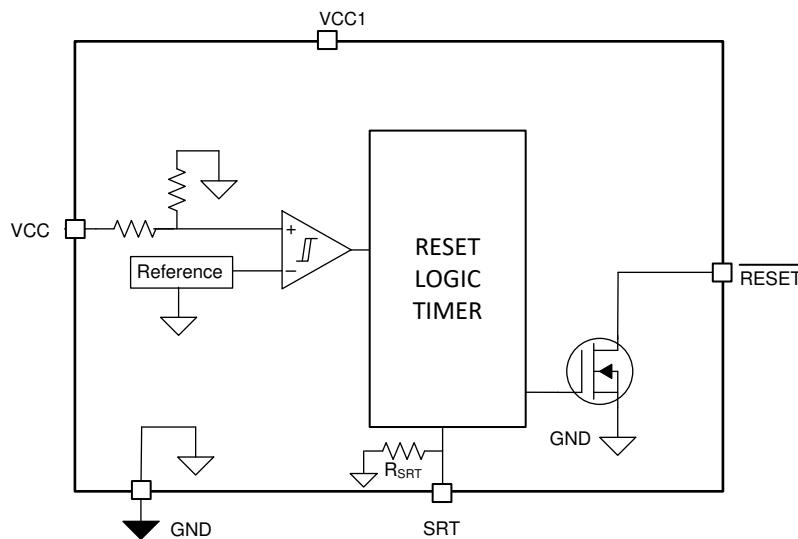
Figure 8. Reset Time Delay vs Large Capacitor Values

## 8 Detailed Description

### 8.1 Overview

The LP3470A micropower voltage supervisory circuit provides a simple solution to monitor the power supplies in microprocessor and digital systems and provides a reset controlled by the factory-programmed reset threshold on the VCC supply voltage pin. When the voltage declines below the reset threshold, the reset signal is asserted and remains asserted for an interval programmed by an external capacitor after VCC has risen above the threshold voltage. The reset threshold options are 2.63 V, 2.75 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 RESET Time-Out Period

The reset time delay can be set to a minimum value of 50  $\mu$ s by leaving the SRT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10  $\mu$ F delay capacitor. The reset time delay ( $t_D$ ) can be programmed by connecting a capacitor no larger than 10  $\mu$ F between SRT pin and GND.

The relationship between external capacitor ( $C_{SRT}$ ) in Farads at SRT pin and the time delay ( $t_D$ ) in seconds is given by [Equation 1](#).

$$t_D = -\ln(0.29) \times R_{SRT} \times C_{SRT} + t_{D(\text{no cap})} \quad (1)$$

[Equation 1](#) is simplified to [Equation 2](#) by plugging  $R_{SRT}$  and  $t_{D(\text{no cap})}$  given in [Electrical Characteristics](#) section:

$$t_D = 618937 \times C_{SRT} + 50 \mu\text{s} \quad (2)$$

[Equation 3](#) solves for external capacitor value ( $C_{SRT}$ ) in units of Farads where  $t_D$  is in units of seconds

$$C_{SRT} = (t_D - 50 \mu\text{s}) \div 618937 \quad (3)$$

The reset delay varies according to three variables: the external capacitor variance ( $C_{SRT}$ ), SRT pin internal resistance ( $R_{SRT}$ ) provided in the Electrical Characteristics table, and a constant. The minimum and maximum variance due to the constant is shown in [Equation 5](#) and [Equation 6](#).

$$t_{D(\text{minimum})} = -\ln(0.36) \times R_{SRT(\text{min})} \times C_{SRT(\text{min})} + t_{D(\text{no cap, min})} \quad (4)$$

$$t_{D(\text{maximum})} = -\ln(0.26) \times R_{SRT(\text{max})} \times C_{SRT(\text{max})} + t_{D(\text{no cap, max})} \quad (5)$$

## Feature Description (continued)

The recommended maximum delay capacitor for the LP3470A is limited to 10  $\mu\text{F}$  as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

### 8.3.2 RESET Output

In applications like microprocessor ( $\mu\text{P}$ ) systems, errors might occur in system operation during power up, power down, or brownout conditions. It is imperative to monitor the power supply voltage to prevent these errors from occurring.

The LP3470A asserts a reset signal whenever the VCC supply voltage is below a threshold ( $V_{IT+}$ ) voltage. RESET is ensured to be a logic low for  $VCC > 0.95$  V. Once VCC exceeds the reset threshold plus a hysteresis voltage, the reset is kept asserted for a time period ( $t_D$ ) programmed by an external capacitor ( $C_{SRT}$ ); after this interval RESET goes to logic high. If a brownout condition occurs (monitored voltage falls below the reset threshold), RESET goes low. When VCC returns above the reset threshold plus a hysteresis voltage, RESET remains low for a time period  $t_D$  before going to logic high. [Figure 9](#) shows this behavior.

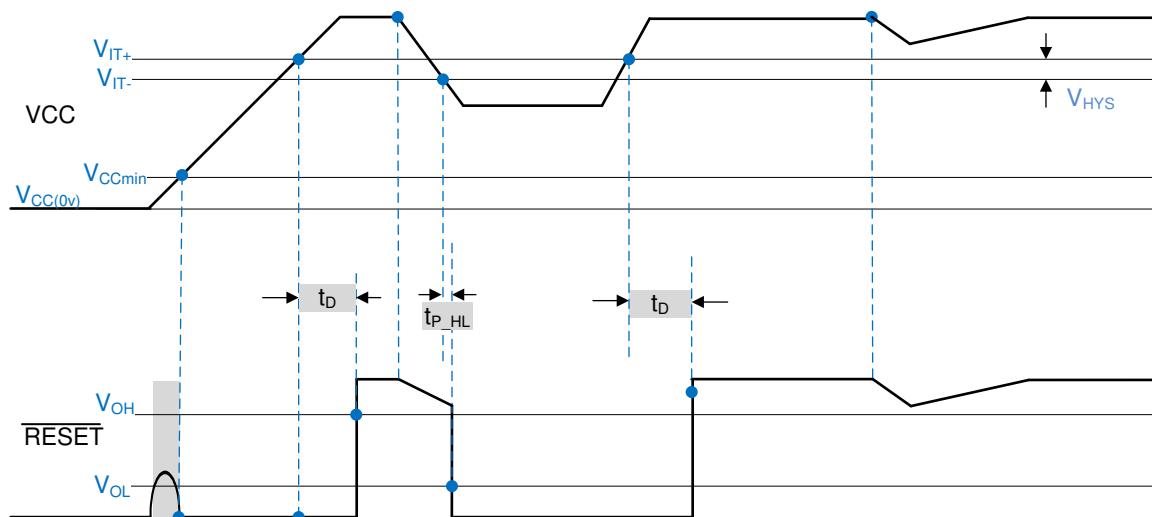


Figure 9. RESET Output Timing Diagram

### 8.3.3 Pull-up Resistor Selection

The RESET output structure of the LP3470A is an open-drain N-channel MOSFET switch. A pull-up resistor ( $R_{\text{pull-up}}$ ) must be connected to VCC to keep the output logic high when RESET is not asserted.

Connect the pull-up resistor to the desired pull-up voltage source and RESET can be pulled up to any voltage up to 10 V independent of the VCC voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values.  $R_{\text{pull-up}}$  must be large enough to limit the current through the output within the recommended operating conditions. The pull-up resistor value determines the actual VOL, the output capacitive loading, and the output leakage current ( $I_{LKG(OD)}$ ). A typical pull-up resistor value of 20 k $\Omega$  is sufficient in most applications.

### 8.3.4 VCC Transient Immunity

The LP3470A is immune to quick voltage transients or excursions on VCC. Sensitivity to transients depends on both pulse duration and overdrive. Overdrive is defined by how much VCC deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in [Equation 6](#). A 0.1- $\mu\text{F}$  bypass capacitor mounted close to VCC provides additional transient immunity.

$$\text{Overdrive} = |(V_{CC} / V_{IT-} - 1) \times 100\%| \quad (6)$$

## Feature Description (continued)

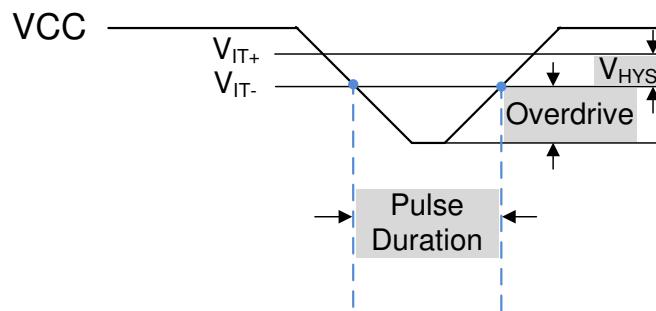


Figure 10. Overdrive vs Pulse Duration

## 8.4 Device Functional Modes

### 8.4.1 RESET Output Low

When the VCC supply voltage is below the reset threshold ( $V_{IT-}$ ), the RESET pin will output logic low. RESET is ensured to be a logic low for  $VCC > 0.95$  V.

### 8.4.2 RESET Output High

When the VCC supply voltage exceeds the reset threshold ( $V_{IT-}$ ) plus the hysteresis voltage ( $V_{HYS}$ ), the RESET remains asserted for a time period ( $t_D$ ) programmed by an external capacitor ( $C_{SRT}$ ); after this interval RESET goes to logic high.

## 9 Application and Implementation

### NOTE

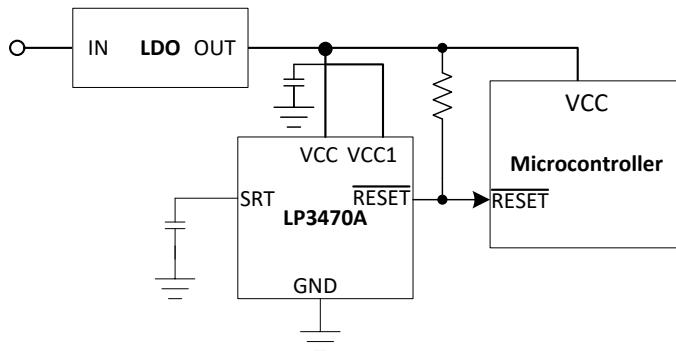
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LP3470A is a micropower CMOS voltage supervisor that is ideal for use in battery-powered microprocessor and other digital systems. It is small in size and provides voltage monitoring and supervisory functions with nano-lQ and programmable delay, making it a good solution in a variety of applications. The LP3470A is available in six standard reset threshold voltage options, and the reset time-out period is adjustable using an external capacitor providing maximum flexibility in any application. This device can ensure system reliability and ensures that a connected microprocessor will operate only when a minimum voltage supply is satisfied.

### 9.2 Typical Application

The LP3470A can be used as a simple supervisor circuit to monitor the input supply to a microprocessor as shown in [Figure 11](#).



**Figure 11. Power-On Reset Circuit**

#### 9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

**Table 1. Design Parameters**

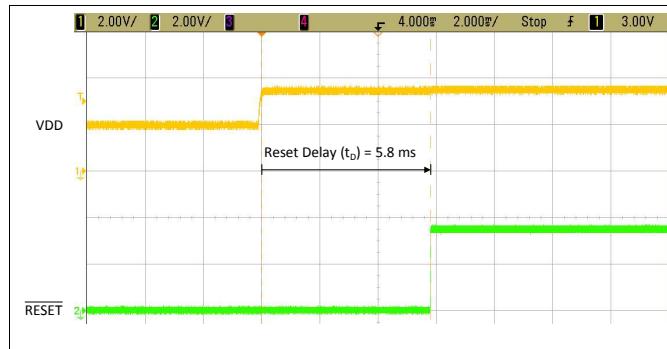
DESIGN PARAMETER	EXAMPLE VALUE
Input supply voltage	0.95 to 10 V
Reset threshold voltage	2.63 V, 2.75 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V
External pullup resistor	0.68 to 68 kΩ
External reset time-out period capacitor	$C_{SRT} = 1 \text{ nF}$
Reset time-out period	619 $\mu\text{s}$

#### 9.2.2 Detailed Design Procedure

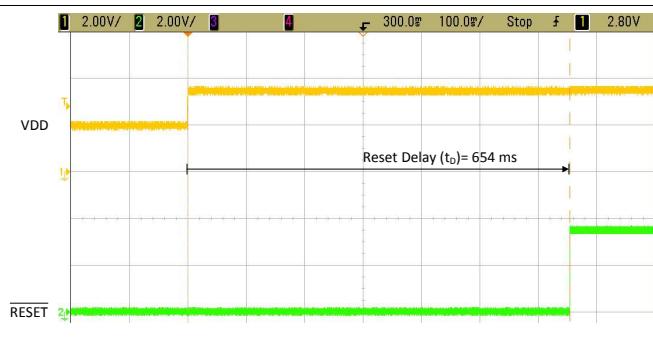
The minimum application circuit requires the LP3470A Power-On Reset Circuit IC and a pullup resistor connecting the reset pin to VCC. The reset delay can be programmed with an additional capacitor connected from the SRT pin to GND. See [RESET Time-Out Period](#) and [Pull-up Resistor Selection](#) for information on choosing specific values for components.

### 9.2.3 Application Curves

Two capacitor values for  $C_{SRT}$  (0.01  $\mu$ F and 1  $\mu$ F) are used as examples to show the programmability of the output time delay as shown in [Figure 12](#) and [Figure 13](#).



**Figure 12.** Reset Delay Time with 0.01- $\mu$ F Capacitor at SRT



**Figure 13.** Reset Delay Time with 1- $\mu$ F Capacitor at SRT

## 10 Power Supply Recommendations

The input of the LP3470A is designed to handle up to the supply voltage absolute maximum rating of 12 V. If the input supply is susceptible to any large transients above the maximum rating, then take extra precautions. An input capacitor is optional but not required to help avoid false reset output triggers due to noise.

## 11 Layout

### 11.1 Layout Guidelines

- Good analog design practice recommends placing a minimum of 0.1- $\mu$ F ceramic capacitor as near as possible to the VCC pin.
- Place components as close as possible to the IC
- Keep traces short between the IC and the  $C_{SRT}$  capacitor to ensure the timing delay is as accurate as possible.
- For VCC slew rate > 100 mV/ $\mu$ s, increase input capacitance and pull-up resistor value

### 11.2 Layout Example

Figure 14 shows a layout example.

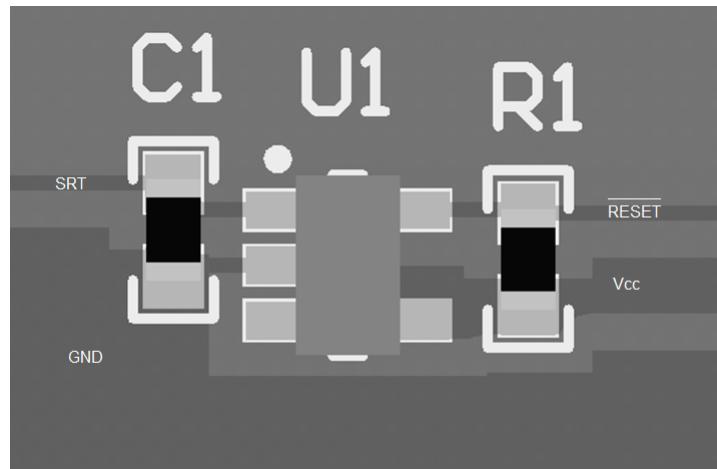


Figure 14. LP3470A Layout Example

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLY022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3470A263DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D263
LP3470A263DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D263
LP3470A275DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D275
LP3470A275DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D275
LP3470A293DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D293
LP3470A293DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D293
LP3470A308DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D308
LP3470A308DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D308
LP3470A365DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D365
LP3470A365DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D365
LP3470A400DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D400
LP3470A400DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D400
LP3470A438DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D438
LP3470A438DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D438
LP3470A463DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	D463
LP3470A463DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D463

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

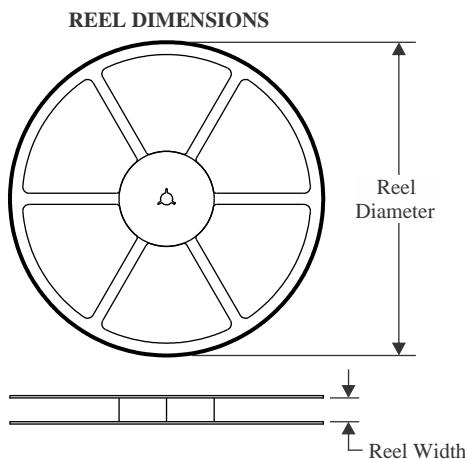
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3470A263DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A275DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A293DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A308DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A365DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A400DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A438DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A463DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3470A263DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A275DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A293DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A308DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A365DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A400DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A438DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A463DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

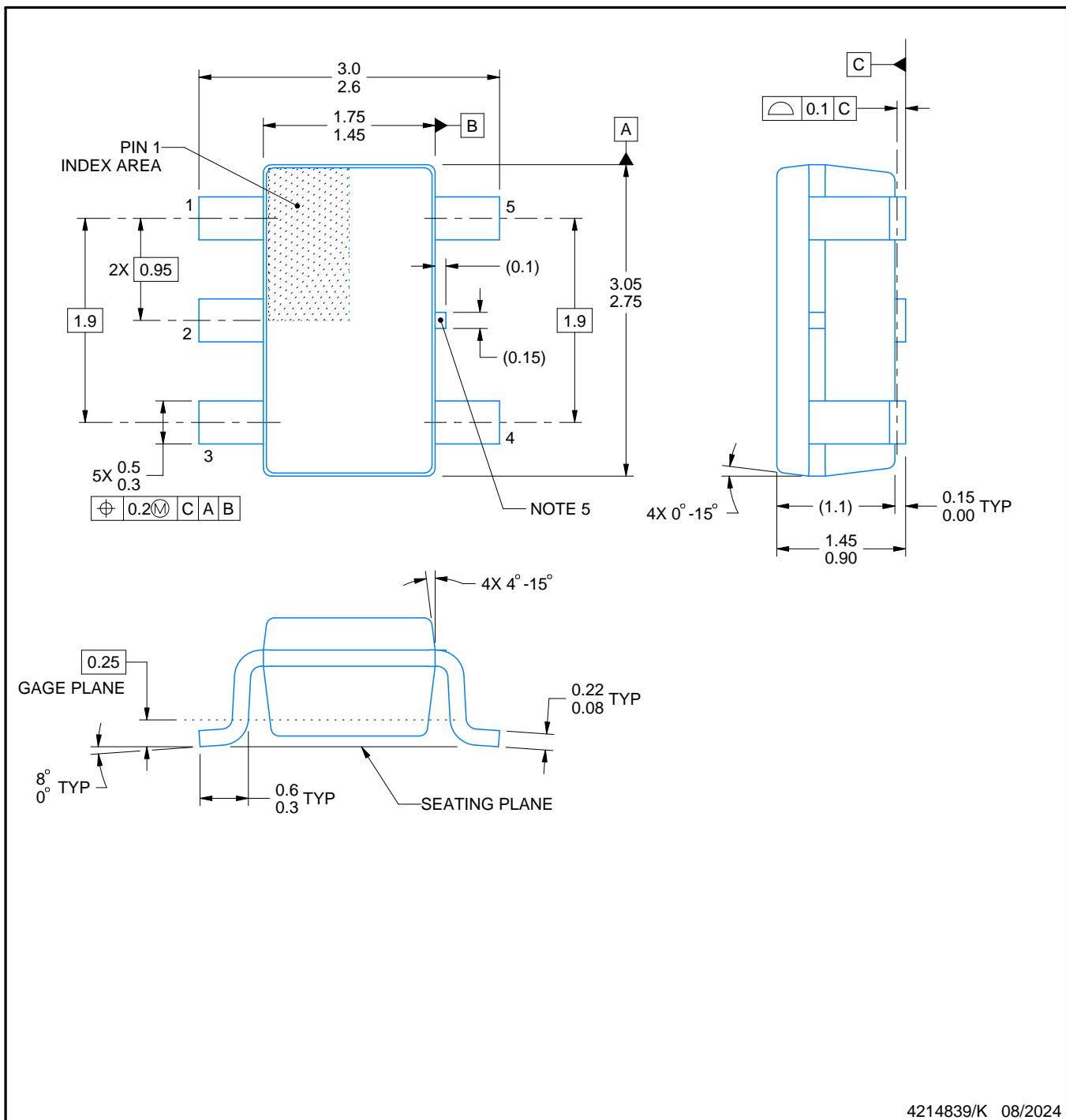
# PACKAGE OUTLINE

DBV0005A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

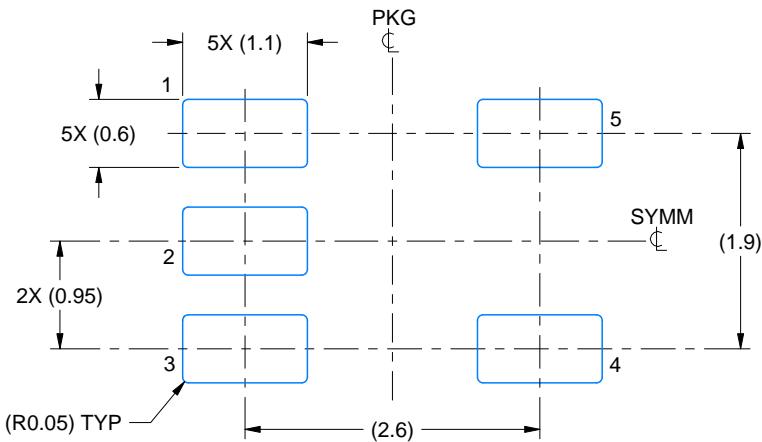
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

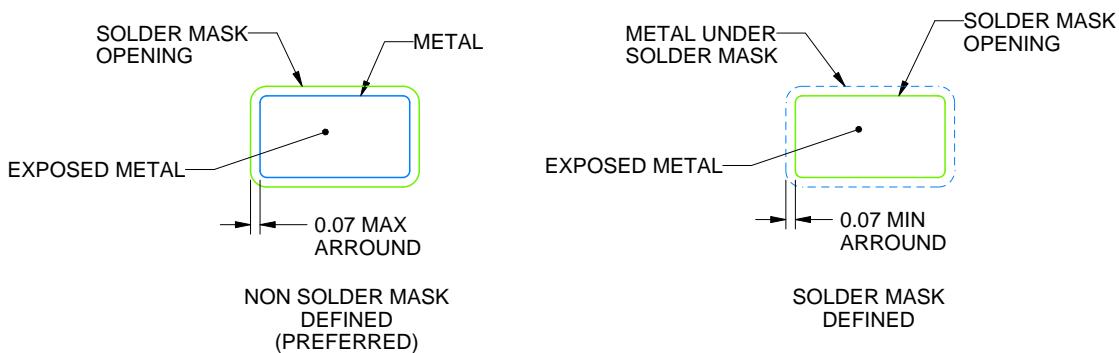
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



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NOTES: (continued)

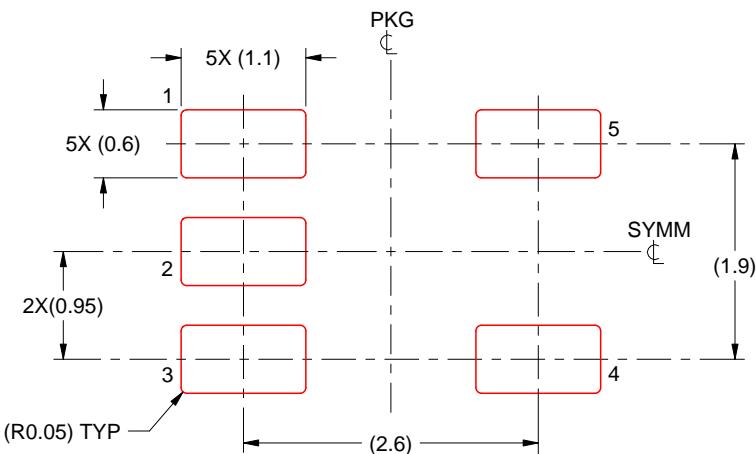
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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