LP38841-ADJ 0.8A Ultra Low Dropout Adjustable Linear Regulators
Stable with Ceramic Output Capacitors

Check for Samples: LP38841-ADJ

FEATURES

- **Ideal for Conversion from 1.8V or 1.5V Inputs**
- **Designed for Use with Low ESR Ceramic Capacitors**
- **Ultra Low Dropout Voltage (75mV @ 0.8A Typ)**
- **0.56V to 1.5V Adjustable Output Range**
- **Load Regulation of 0.1%/A (Typ)**
- **30nA Quiescent Current in Shutdown (Typ)**
- **Low Ground Pin Current at all Loads**
- **Over Temperature/Over Current Protection**
- **Available in 8 Lead SO**
- **−40°C to +125°C Junction Temperature Range**
- **UVLO Disables Output when V_{BIAS} < 3.8V**

APPLICATIONS

- **ASIC Power Supplies In:**
  - **Desktops, Notebooks, and Graphics Cards, Servers**
  - **Gaming Set Top Boxes, Printers and Copiers**
- **Server Core and I/O Supplies**
- **DSP and FPGA Power Supplies**
- **SMPS Post-Regulators**

DESCRIPTION

The LP38841-ADJ is a high current, fast response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in the SO package.

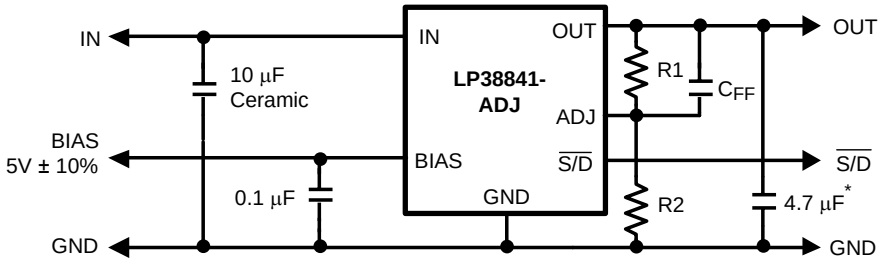
Dropout Voltage: 75 mV (typ) @ 0.8A load current.

Quiescent Current: 30 mA (typ) at full load.

Shutdown Current: 30 nA (typ) when S/D pin is low.

Precision Reference Voltage: 1.5% room temperature accuracy.

Typical Application Circuit



* Minimum value required if Tantalum capacitor is used (see APPLICATION HINTS).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2005–2013, Texas Instruments Incorporated

Connection Diagram

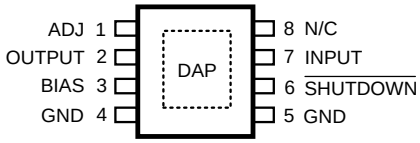
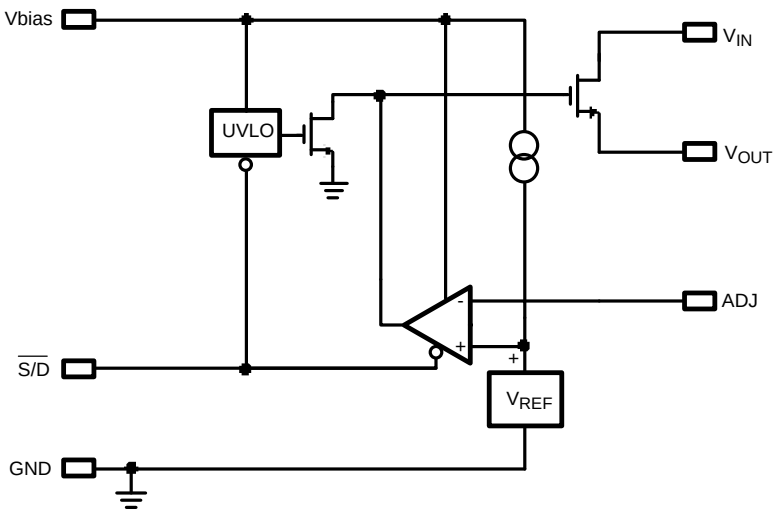


Figure 1. SO-8 – Top View

PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1	ADJ	The Adjust pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2 (see Typical Application Circuit).
2	OUTPUT	The regulated output voltage is connected to this pin.
3	BIAS	The Bias pin is used to provide the low current bias voltage to the chip which operates the internal circuitry and provides drive voltage for the N-FET.
4, 5	GND	These are the power and analog grounds for the IC. Connect both pins to ground.
6	$\overline{\text{SHUTDOWN}}$	This provides a low power shutdown function which turns the regulated output OFF. Tie to V_{BIAS} if this function is not used.
7	INPUT	The high current input voltage which is regulated down to the nominal output voltage must be connected to this pin. Because the bias voltage to operate the chip is provided separately, the input voltage can be as low as a few hundred millivolts above the output voltage.
8	N/C	This pin is floating, it has no internal connection.
DAP	DAP	The SO DAP is a thermal connection that is physically connected to the backside of the die, and is used as a thermal connection to the PC Board copper. The DAP is not a ground pin connection, but should be connected to ground potential.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2005–2013, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS(1)(2)

Storage Temperature Range		−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)		260°C
ESD Rating	Human Body Model(3)	2 kV
	Machine Model(4)	200V
Power Dissipation(5)		Internally Limited
V_{IN} Supply Voltage (Survival)		−0.3V to +6V
V_{BIAS} Supply Voltage (Survival)		−0.3V to +7V
Shutdown Input Voltage (Survival)		−0.3V to +7V
V_{ADJ}		-0.3V to +6V
I_{OUT} (Survival)(6)		Internally Limited
Output Voltage (Survival)		−0.3V to +6V
Junction Temperature		−40°C to +150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see the ELECTRICAL CHARACTERISTICS. Specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.
(4) The machine model is a 220 pF capacitor discharged directly into each pin.
(5) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.
(6) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

OPERATING RATINGS

V_{IN} Supply Voltage	(V_{OUT} + V_{DO}) to 5.5V
Shutdown Input Voltage	0 to +5.5V
I_{OUT}	0.8A
Operating Junction Temperature Range	−40°C to +125°C
V_{BIAS} Supply Voltage	4.5V to 5.5V
V_{OUT}	0.56V to 1.5V

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = V_O(NOM) + 1V, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, $V_{S/D}$ = V_{BIAS}. Min/Max limits are specified through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	MIN	TYP(1)	MAX	Units
V_{ADJ}	Adjust Pin Voltage	10 mA < I_L < 0.8A V_O(NOM) + 1V ≤ V_{IN} ≤ 5.5V 4.5V ≤ V_{BIAS} ≤ 5.5V	0.552 **0.543**	0.56	0.568 **0.577**	V
I_{ADJ}	Adjust Pin Bias Current	10 mA < I_L < 0.8A V_O(NOM) + 1V ≤ V_{IN} ≤ 5.5V 4.5V ≤ V_{BIAS} ≤ 5.5V		1		µA
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation(2)	V_O(NOM) + 1V ≤ V_{IN} ≤ 5.5V		0.01		%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation(3)	10 mA < I_L < 0.8A		0.1	0.4 **1.3**	%/A
V_{DO}	Dropout Voltage(4)	I_L = 0.8A		75	120 **205**	mV

(1) Typical numbers represent the most likely parametric norm for 25°C operation.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(4) Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

Copyright © 2005–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, $V_{S/D} = V_{BIAS}$. Min/Max limits are specified through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	MIN	TYP(1)	MAX	Units
$I_Q(V_{IN})$	Quiescent Current Drawn from V_{IN} Supply	10 mA < I_L < 0.8A		30	35 **40**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.06	1 **30**	µA
$I_Q(V_{BIAS})$	Quiescent Current Drawn from V_{BIAS} Supply	10 mA < I_L < 0.8A		2	4 **6**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.03	1 **30**	µA
UVLO	V_{BIAS} Voltage Where Regulator Output Is Enabled			3.8		V
I_{SC}	Short-Circuit Current	V_{OUT} = 0V		2.6		A
Shutdown Input						
V_{SDT}	Output Turn-off Threshold	Output = ON		0.7	**1.3**	V
		Output = OFF	**0.3**	0.7		
Td (OFF)	Turn-OFF Delay	R_{LOAD} X C_{OUT} << Td (OFF)		20		µs
Td (ON)	Turn-ON Delay	R_{LOAD} X C_{OUT} << Td (ON)		15		
$I_{\overline{S/D}}$	$\overline{S/D}$ Input Current	$V_{\overline{S/D}}$ =1.3V		1		µA
		$V_{\overline{S/D}} \le 0.3V$		−1		
θ_{J-A}	Junction to Ambient Thermal Resistance	SO-8 Package(5)		43		°C/W
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT}$ +1V, f = 120 Hz		80		dB
		$V_{IN} = V_{OUT}$ + 1V, f = 1 kHz		65		
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT}$ + 3V, f = 120 Hz		58		
		$V_{BIAS} = V_{OUT}$ + 3V, f = 1 kHz		58		
	Output Noise Density	f = 120 Hz		1		µV/root−Hz
e_n	Output Noise Voltage V_{OUT} = 1.5V	BW = 10 Hz − 100 kHz		150		µV (rms)
		BW = 300 Hz − 300 kHz		90		

(5) For optimum heat dissipation, the exposed DAP on the bottom of the SO package must be soldered to a copper plane or connected using thermal vias to an internal copper plane.

Copyright © 2005–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_J = 25°C, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $\overline{S/D}$ Pin is tied to V_{BIAS}, V_{OUT} = 1.2V, I_L = 10mA, V_{BIAS} = 5V, V_{IN} = V_{OUT} + 1V.

V_{BIAS} Transient Response

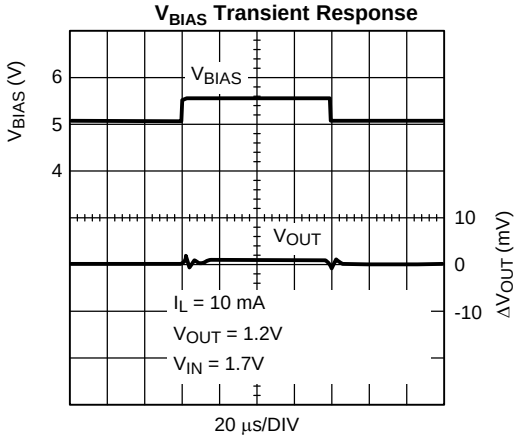


Figure 2.

Dropout Voltage Over Temperature

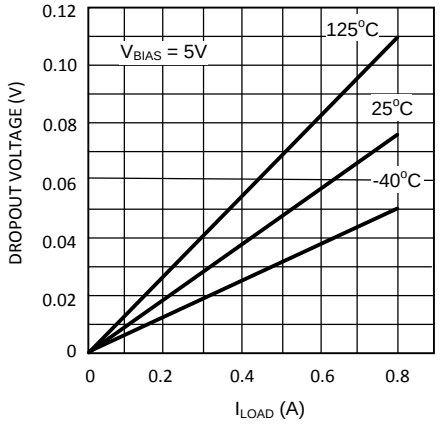


Figure 3.

V_{BIAS} PSRR

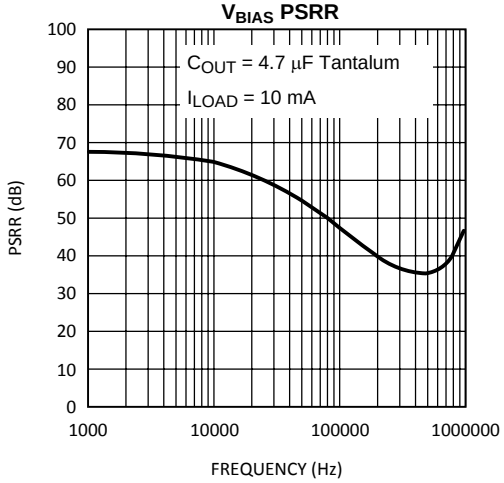


Figure 4.

V_{BIAS} PSRR

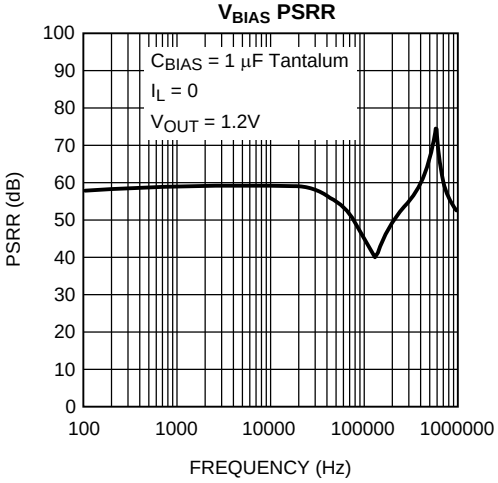


Figure 5.

V_{IN} PSRR

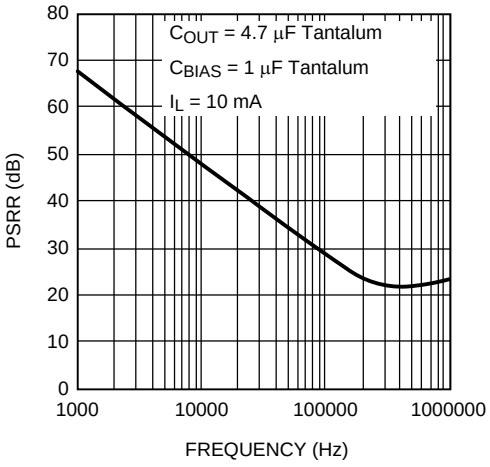


Figure 6.

V_{ADJ} / I_{ADJ} vs Temperature

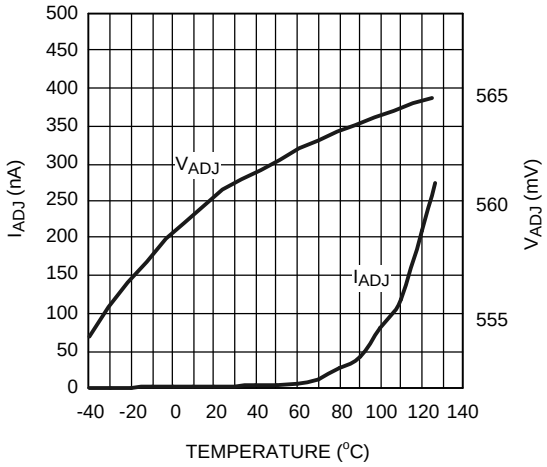


Figure 7.

Copyright © 2005–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $\overline{S/D}$ Pin is tied to V_{BIAS}, V_{OUT} = 1.2V, I_L = 10mA, V_{BIAS} = 5V, V_{IN} = V_{OUT} + 1V.

Load Transient Response

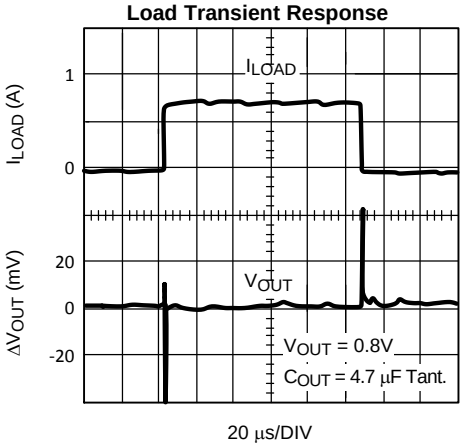


Figure 8.

Load Transient Response

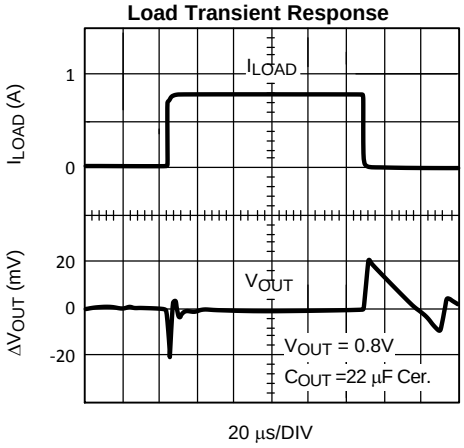


Figure 9.

Copyright © 2005–2013, Texas Instruments Incorporated

APPLICATION HINTS

SETTING THE OUTPUT VOLTAGE

(Refer to Typical Application Circuit)

The output voltage is set using the resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + R1 / R2) \quad (1)$$

The value of R2 must be 10k or less for proper operation.

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

OUTPUT CAPACITOR

An output capacitor is required on the LP3884X devices for loop stability. The minimum value of capacitance necessary depends on type of capacitor: if a solid Tantalum capacitor is used, the part is stable with capacitor values as low as 4.7µF. If a ceramic capacitor is used, a minimum of 22 µF of capacitance must be used (capacitance may be increased without limit). The reason a larger ceramic capacitor is required is that the output capacitor sets a pole which limits the loop bandwidth. The Tantalum capacitor has a higher ESR than the ceramic which provides more phase margin to the loop, thereby allowing the use of a smaller output capacitor because adequate phase margin can be maintained out to a higher crossover frequency. The tantalum capacitor will typically also provide faster settling time on the output after a fast changing load transient occurs, but the ceramic capacitor is superior for bypassing high frequency noise.

The output capacitor must be located less than one centimeter from the output pin and returned to a clean analog ground. Care must be taken in choosing the output capacitor to ensure that sufficient capacitance is provided over the full operating temperature range. If ceramics are selected, only X7R or X5R types may be used because Z5U and Y5F types suffer severe loss of capacitance with temperature and applied voltage and may only provide 20% of their rated capacitance in operation.

INPUT CAPACITOR

The input capacitor is also critical to loop stability because it provides a low source impedance for the regulator. The minimum required input capacitance is 10 µF ceramic (Tantalum not recommended). The value of C_{IN} may be increased without limit. As stated above, X5R or X7R must be used to ensure sufficient capacitance is provided. The input capacitor must be located less than one centimeter from the input pin and returned to a clean analog ground.

FEED FORWARD CAPACITOR

(Refer to Typical Application Circuit)

A capacitor placed across R1 can provide some additional phase margin and improve transient response. The capacitor C_{FF} and R1 form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (2)$$

For best effect, select C_{FF} so the zero frequency is approximately 70 kHz. The phase lead provided by C_{FF} drops as the output voltage gets closer to 0.56V (and R1 reduces in value). The reason is that C_{FF} also forms a pole whose frequency is given by:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times R1 // R2) \quad (3)$$

As R1 reduces, the two equations come closer to being equal and the pole and zero begin to cancel each other out which removes the beneficial phase lead of the zero.

BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

Copyright © 2005–2013, Texas Instruments Incorporated

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 5.5V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 3.8V.

SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. The $\overline{S/D}$ pin must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

POWER DISSIPATION/HEATSINKING

Heatsinking for the SO-8 package is accomplished by allowing heat to flow through the exposed DAP on the bottom of the package into the copper on the PC board. The exposed DAP must be soldered down to a copper plane to get good heat transfer. It can also be connected through thermal vias to internal copper planes. Since the DAP is physically connected to the backside of the die, it must be held at ground potential. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

Copyright © 2005–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	8

Copyright © 2005–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP38841MR-ADJ/NOPB	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38841 MRADJ
LP38841MR-ADJ/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38841 MRADJ
LP38841MRX-ADJ/NO.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38841 MRADJ
LP38841MRX-ADJ/NOPB	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38841 MRADJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

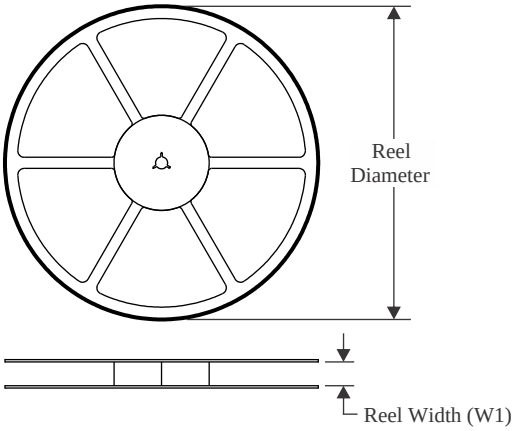
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

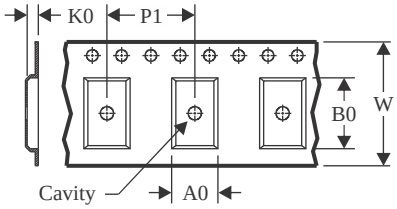
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

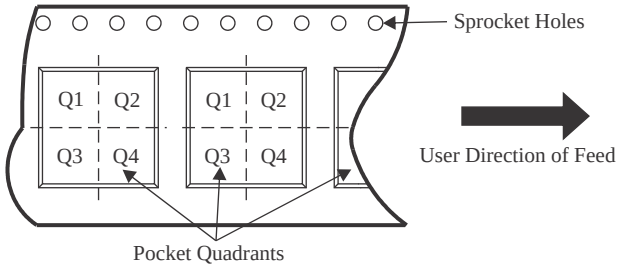


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

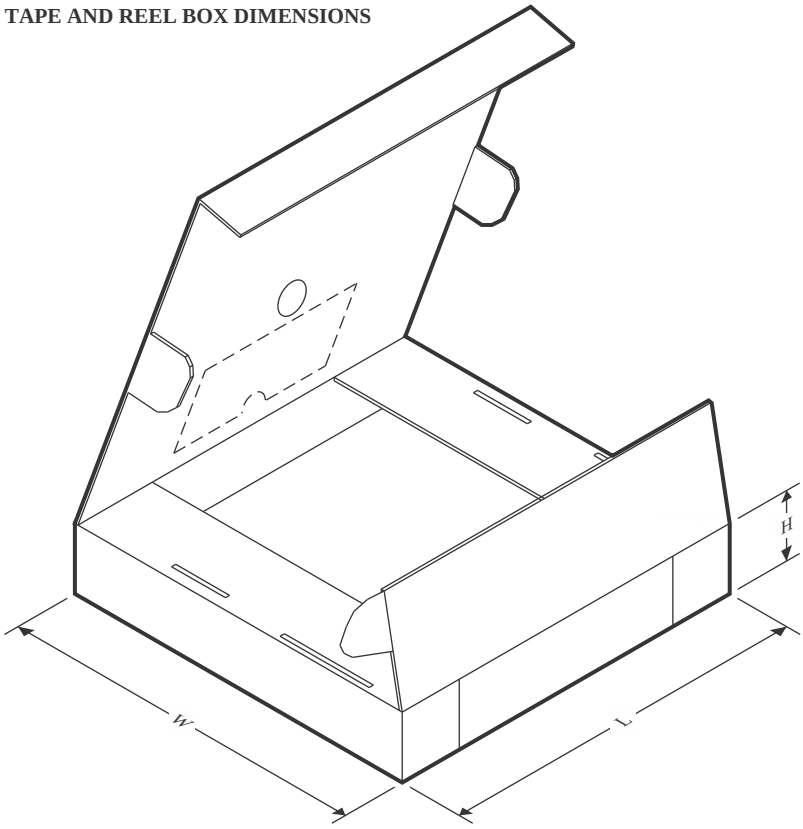
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38841MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

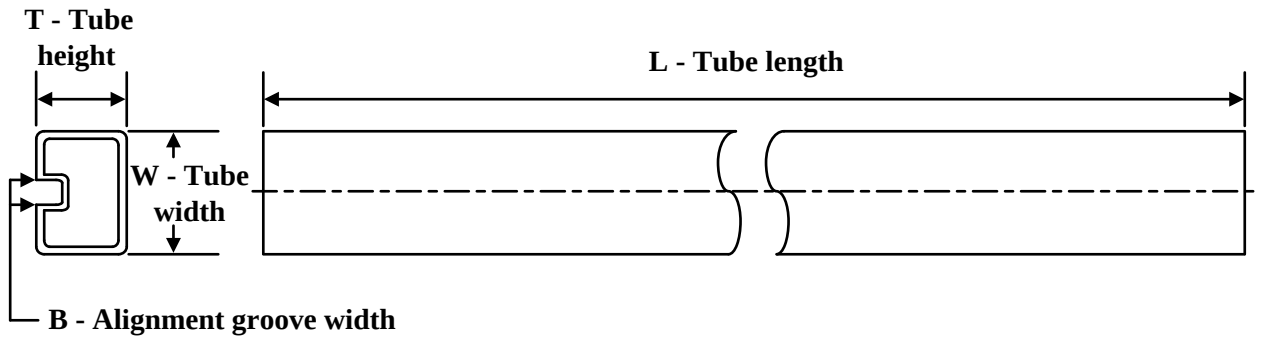
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38841MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0

TUBE



*All dimensions are nominal

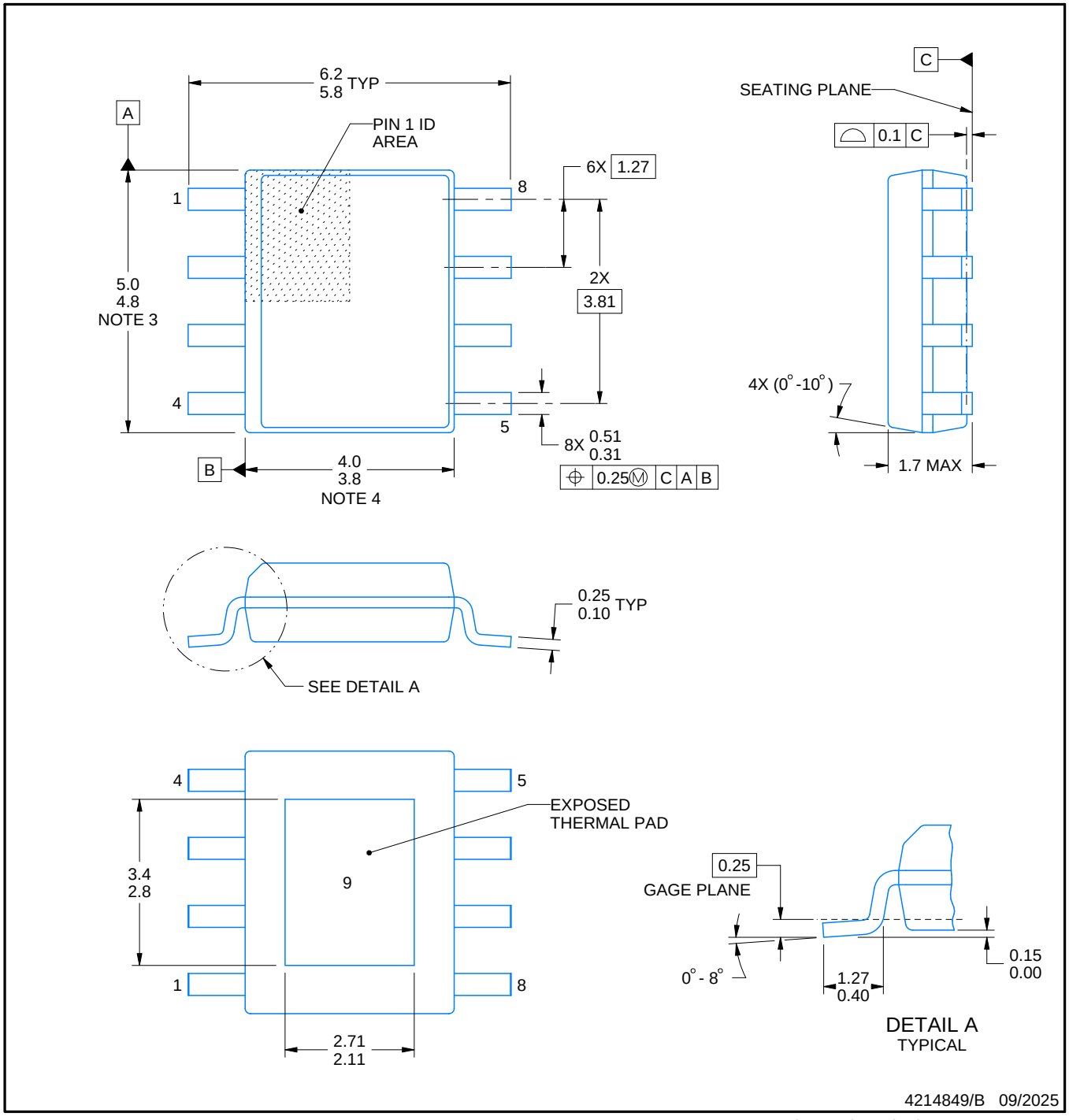
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38841MR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP38841MR-ADJ/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

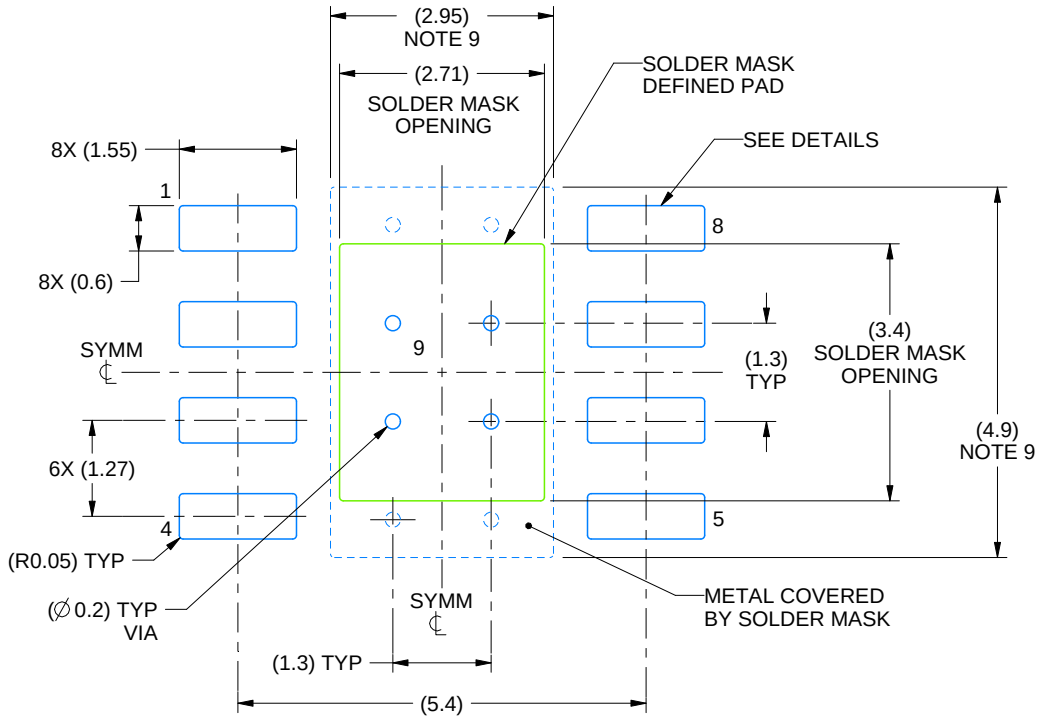
PLASTIC SMALL OUTLINE



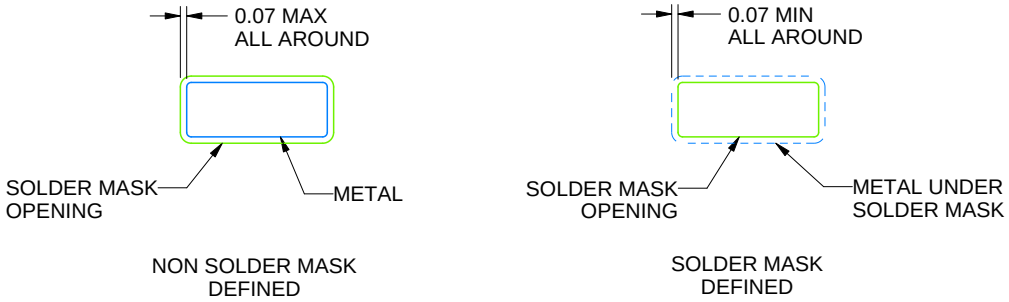
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

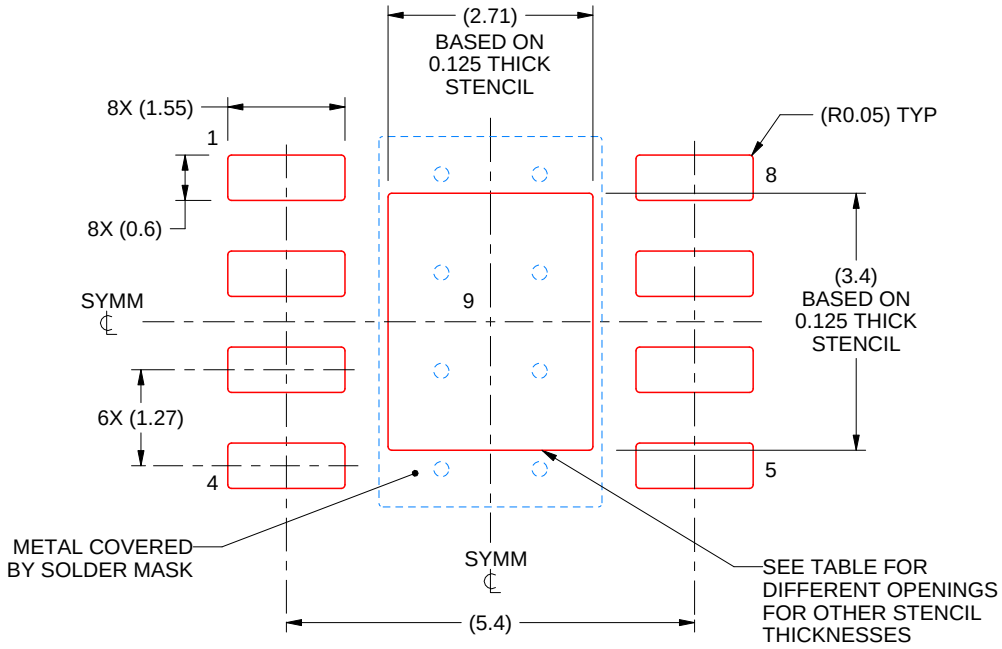
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025