LP4950C-5V and LP4951C Adjustable Micropower Voltage Regulators

Check for Samples: LP4950C-5V, LP4951C

FEATURES

- **High Accuracy 5V Specified 100mA Output**
- **Extremely Low Quiescent Current**
- **Low Dropout Voltage**
- **Extremely Tight Load and Line Regulation**
- **Very Low Temperature Coefficient**
- **Use as Regulator or Reference**
- **Needs Only 1µF for Stability**
- **Current and Thermal Limiting**

LP4951C VERSIONS ONLY

- **Error Flag Warns of Output Dropout**
- **Logic-controlled Electronic Shutdown**
- **Output Pogrammable From 1.24 to 29V**

DESCRIPTION

The LP4950C and LP4951C are micropower voltage regulators with very low quiescent current (75µA typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP4950C/LP4951C increases only slightly in dropout, prolonging battery life.

The LP4950C in the popular 3-pin TO-92 package is pin compatible with older 5V regulators. The 8-lead LP4951C is available in a plastic surface mount package and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V output or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP4950C/LP4951C has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

BLOCK DIAGRAM AND TYPICAL APPLICATIONS

LP4950C

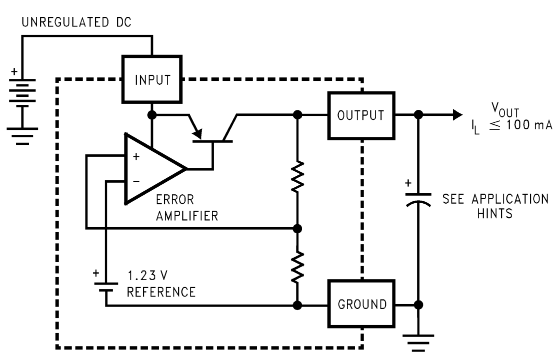


Figure 1.

LP4951C

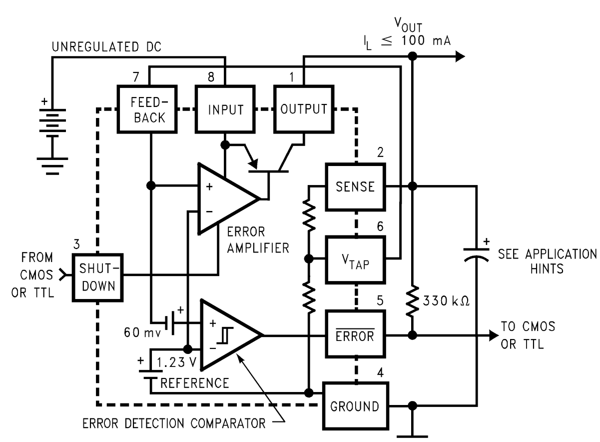


Figure 2.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS [1]

Input Supply Voltage	−0.3 to +30V
SHUTDOWN Input Voltage, Error Comparator Output Voltage, [2]	−0.3 to +30V
FEEDBACK Input Voltage [2] [3]	−1.5 to +30V
Power Dissipation	Internally Limited
Junction Temperature (T_J)	+150°C
Ambient Storage Temperature	−65° to +150°C
ESD Rating Human Body Model [4]	2 kV
For soldering specifications, see the following document: www.ti.com/lit/snoa549	

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) May exceed input supply voltage.
(3) When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.
(4) Human Body Model 1.5 kΩ in series with 100 pF. LP4950 - passes 2 kV HBM. LP4951 - All pins pass 2 kV except Vfb -1000V.

OPERATING RATINGS [1]

Maximum Input Supply Voltage	30V
Junction Temperature Range [2]	
LP4950C, LP4951C	−40°C to 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) The junction-to-ambient thermal resistances are as follows: 180°C/W and 160°C/W for the TO-92 package with 0.40 inch and 0.25 inch leads to the printed circuit board (PCB) respectively, 160°C/W for the molded plastic SOIC (D). The above thermal resistances for the SOIC package apply when the package is soldered directly to the PCB.

ELECTRICAL CHARACTERISTICS (1)

Parameter	Conditions (1)	LP4950CZ / LP4951CM Typ	Tested Limit(2)	Design Limit(3)	Units
Output Voltage	T_J = 25°C	5.0	5.1		V max
			4.9		V min
	−25°C ≤ T_J ≤ 85°C			5.15	V max
				4.85	V min
	Full Operating Temperature Range			**5.2**	V max
				4.8	V min
Output Voltage	100 µA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}			**5.24**	V max
				4.76	V min
Output Voltage Temperature Coefficient	(4)			**150**	ppm/°C
Line Regulation(5)	6V ≤ V_{IN} ≤ 30V (6)	0.04	0.2		% max
				0.4	% max
Load Regulation(5)	100µA ≤ I_L ≤ 100mA	0.1	0.2		% max
				0.3	% max
Dropout Voltage(7)	I_L = 100µA	50	80		mV max
				150	mV max
	I_L = 100mA	380	450		mV max
				600	mV max
Ground Current	I_L = 100µA	75	150		µA max
				170	µA max
	I_L = 100mA	8	15		mA max
				19	mA max
Dropout Ground Current	V_{IN} = 4.5V I_L = 100µA	110	200		µA max
				230	µA max
Current Limit	V_{OUT} = 0	160	200		mA max
				220	mA max
Thermal Regulation	(8)	0.05	0.2		%/W max
Output Noise, 10 Hz to 100 kHz	C_L = 1µF	430			µV rms
	C_L = 200µF	160			µV rms
	C_L = 3.3µF (Bypass = 0.01µF Pins 7 to 1 (LP4951C)	100			µV rms

(1) Unless otherwise noted all limits specified for V_{IN} = 6V, I_L = 100µA and C_L = 1µF. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25°C. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE (V_{OUT} = 5V), and $V_{SHUTDOWN}$ ≤ 0.8V.
(2) Specified and 100% production tested.
(3) Specified but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
(4) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
(5) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(6) Line regulation for the LP4951C is tested at 150°C for I_L = 1 mA. For I_L = 100µA and T_J = 125°C, line regulation is specified by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.
(7) Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.
(8) Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10ms.

ELECTRICAL CHARACTERISTICS

		LP4951C			
Parameter	Conditions (1)	Typ	Tested Limit (2)	Design Limit (3)	Units
8-PIN VERSIONS ONLY					
Reference Voltage		1.235	1.285		V max
				1.295	V max
			1.185		V min
				1.165	Vmin
Reference Voltage	(4)			**1.335**	V max
				1.135	V min
Feedback Pin Bias Current		20	40		nA max
				60	nA max
Reference Voltage Temperature Coefficient	(5)	50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1			nA/°C
Error Comparator					
Output Leakage Current	V**OH** = 30V	0.01	1		μA max
				2	μA max
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 400μA	150	250		mV max
				400	mV max
Upper Threshold Voltage	(3)	60	40		mV min
				25	mV min
Lower Threshold Voltage	(6)	75	95		mV max
				140	mV max
Hysteresis	(6)	15			mV
Shutdown Input					
Input Logic Voltage		1.3			V
	Low (Regulator ON)			**0.7**	V max
	High (Regulator OFF)			**2.0**	V min
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V	30	50		μA max
				100	μA max
	$V_{SHUTDOWN}$ = 30V	450	600		μA max
				750	μA max
Regulator Output Current in Shutdown	(7)	3	10		μA max
				20	μA max

(1) Unless otherwise noted all limits specified for V_{IN} = 6V, I_L = 100μA and C_L = 1μF. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for $T_A = T_J$ = 25°C. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE (V_{OUT} = 5V), and $V_{SHUTDOWN}$ ≤ 0.8V.
(2) Specified and 100% production tested.
(3) Specified but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
(4) $V_{REF} \le V_{OUT} \le (V_{IN} - 1V)$, 2.3V ≤ V_{IN} ≤ 30V, 100μA ≤ I_L ≤ 100mA, $T_J \le T_{JMAX}$.
(5) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
(6) Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at V_{IN} = 6V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2.For example, at a programmed output voltage of 5V, the Error output is specified to go low when the output drops by 95 mV × 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% specified.
(7) $V_{SHUTDOWN}$ ≥ 2V, V_{IN} ≤ 30V, V_{OUT} = 0, Feedback pin tied to V_{TAP}.

CONNECTION DIAGRAMS

TO-92 Plastic Package

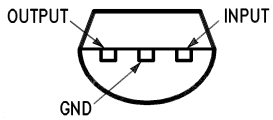


Figure 3. Bottom View

Surface-Mount Package (SOIC)

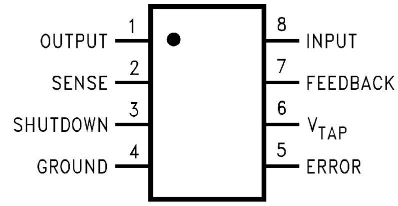


Figure 4. Top View

TYPICAL PERFORMANCE CHARACTERISTICS

Quiescent Current

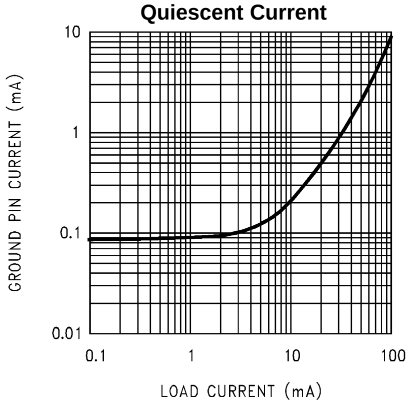


Figure 5.

Dropout Characteristics

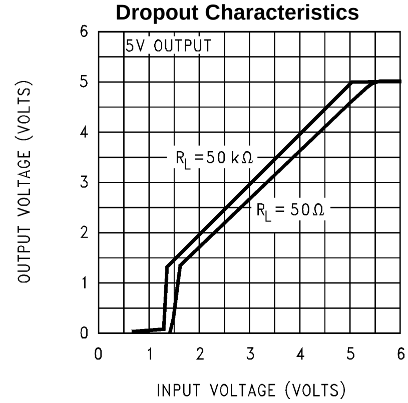


Figure 6.

Input Current

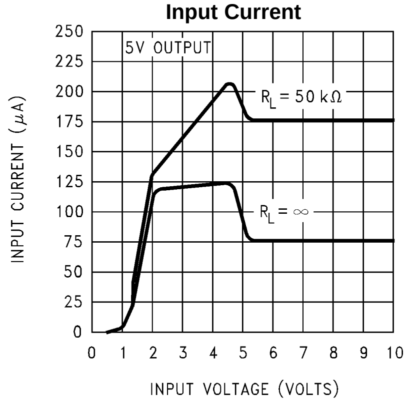


Figure 7.

Input Current

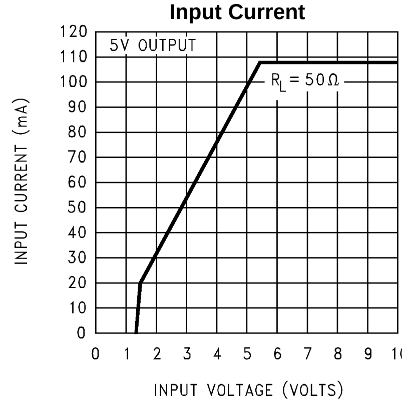


Figure 8.

Output Voltage vs. Temperature of 3 Representative Units

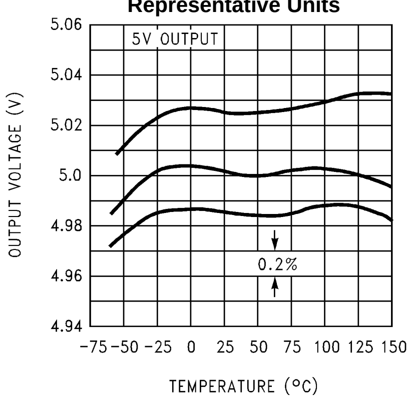


Figure 9.

Quiescent Current

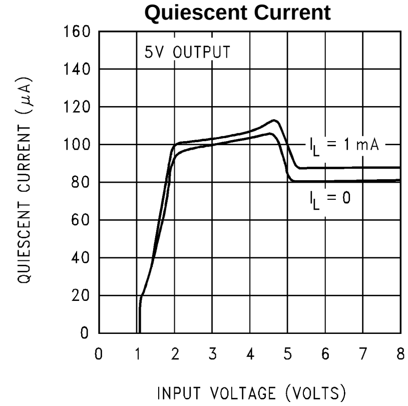


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Quiescent Current

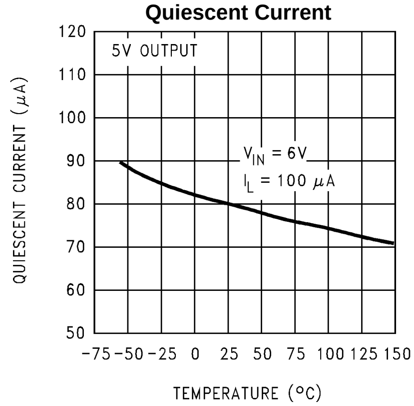


Figure 11.

Quiescent Current

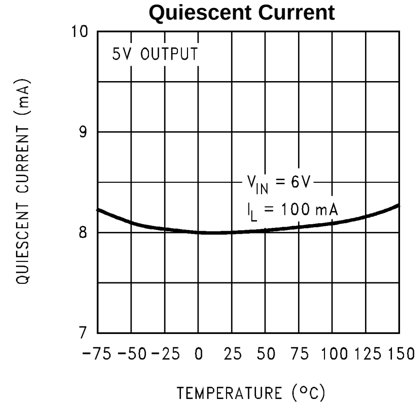


Figure 12.

Quiescent Current

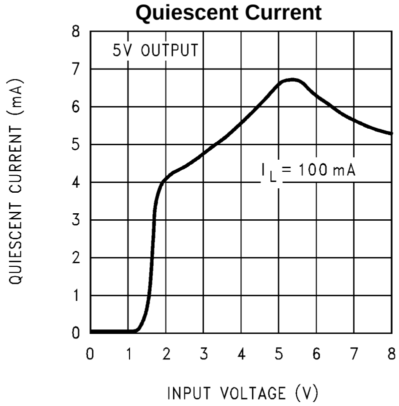


Figure 13.

Short Circuit Current

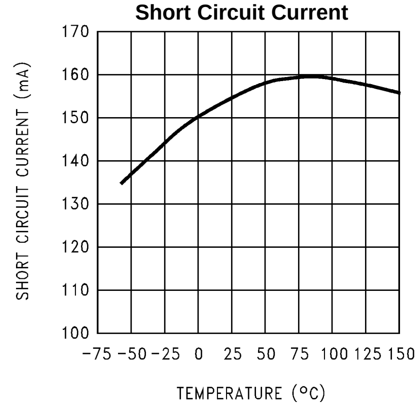


Figure 14.

Dropout Voltage

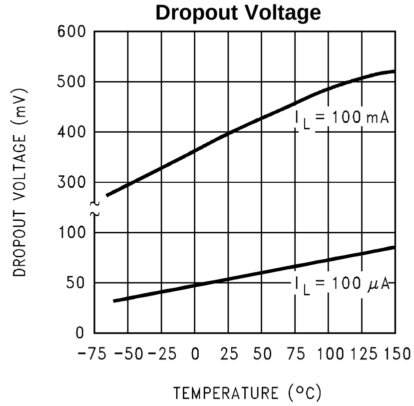


Figure 15.

Dropout Voltage

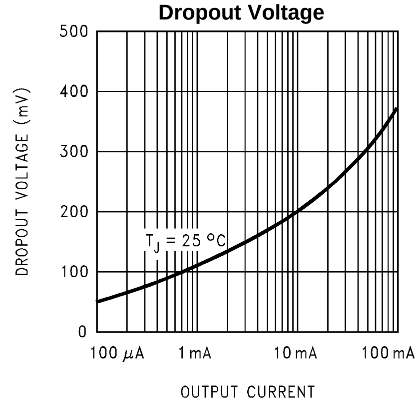


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

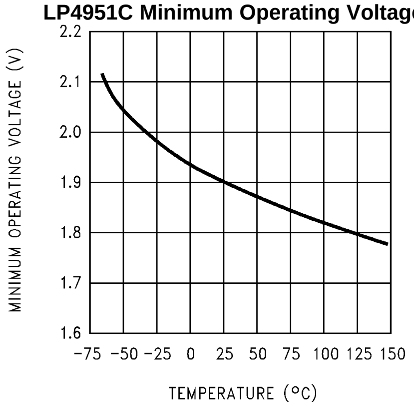


Figure 17.

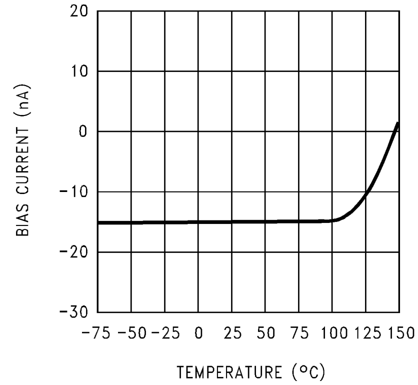


Figure 18.

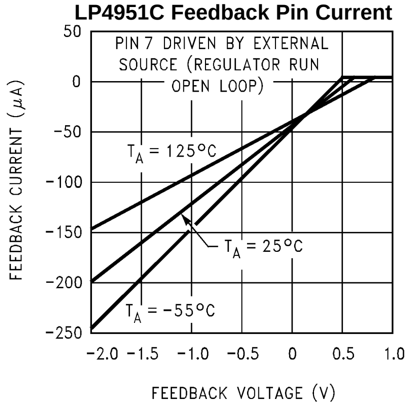


Figure 19.

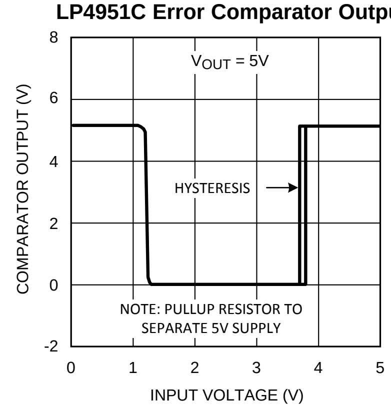


Figure 20.

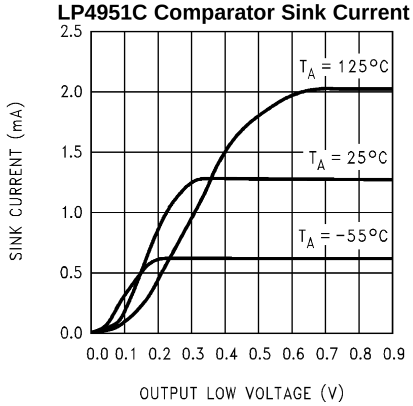


Figure 21.

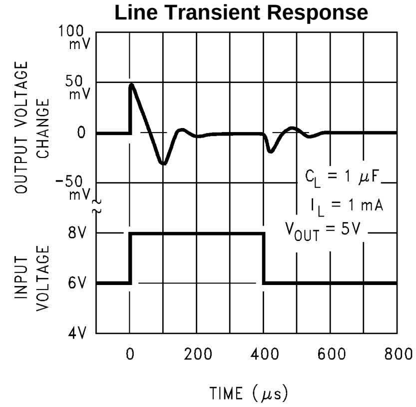


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Load Transient Response

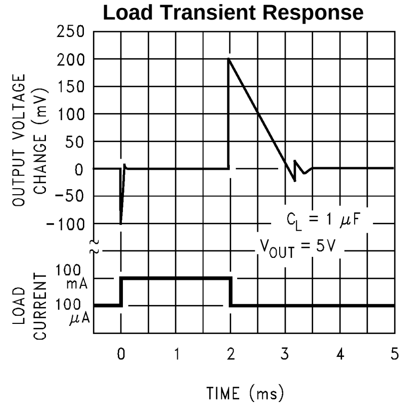


Figure 23.

Load Transient Response

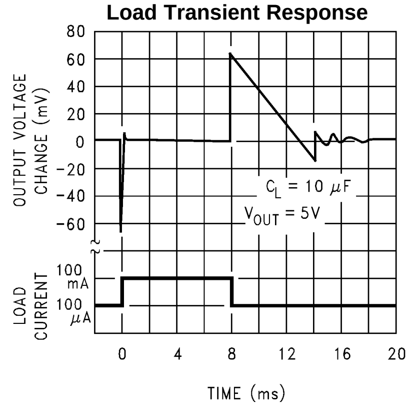


Figure 24.

LP4951C Enable Transient

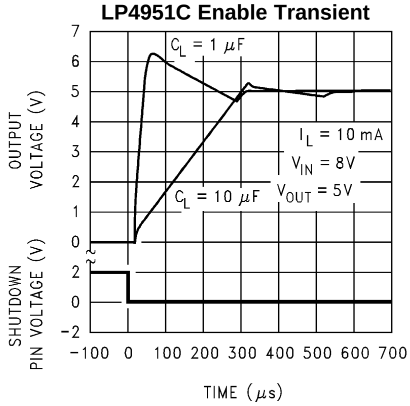


Figure 25.

Output Impedance

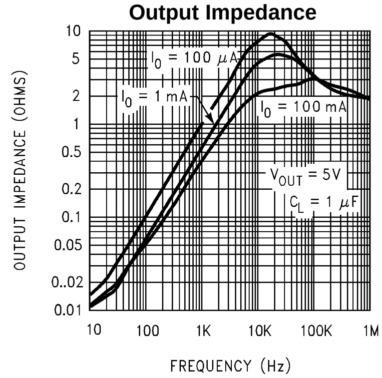


Figure 26.

Ripple Rejection

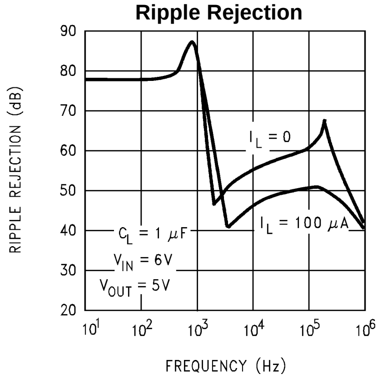


Figure 27.

Ripple Rejection

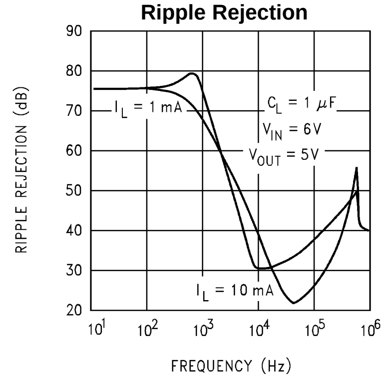


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Ripple Rejection

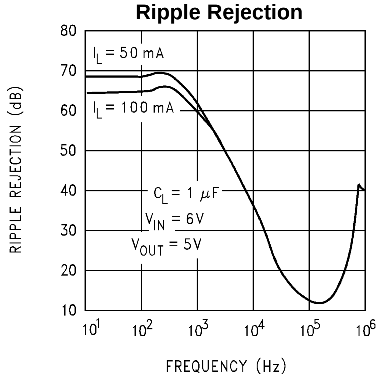


Figure 29.

Output Noise

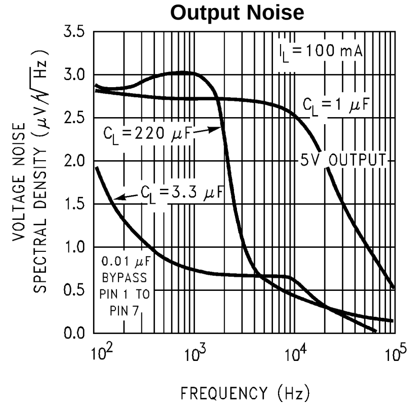


Figure 30.

LP4951C Divider Resistance

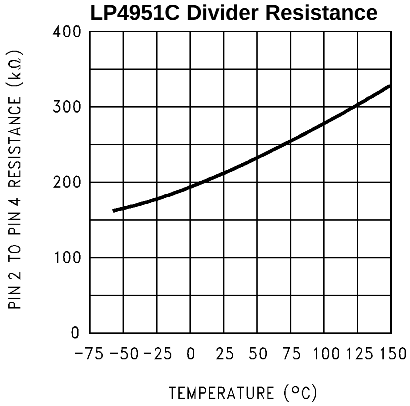


Figure 31.

Shutdown Threshold Voltage

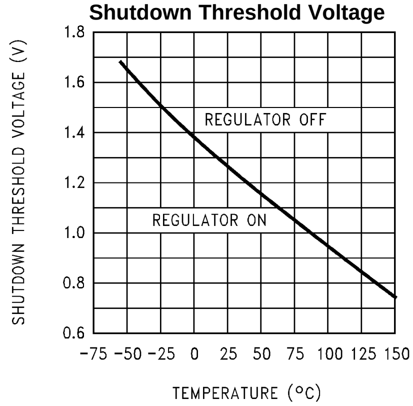


Figure 32.

Line Regulation

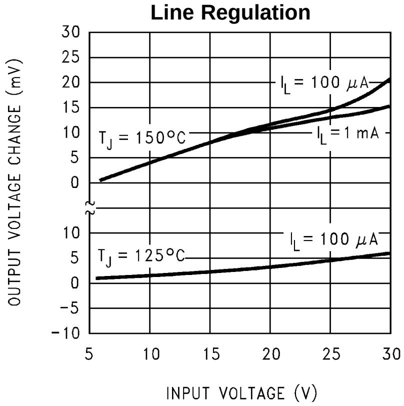


Figure 33.

LP4951C Maximum Rated Output Current

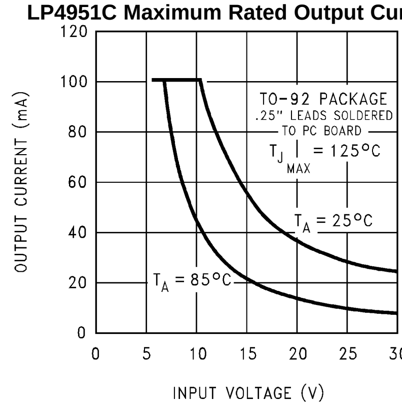


Figure 34.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

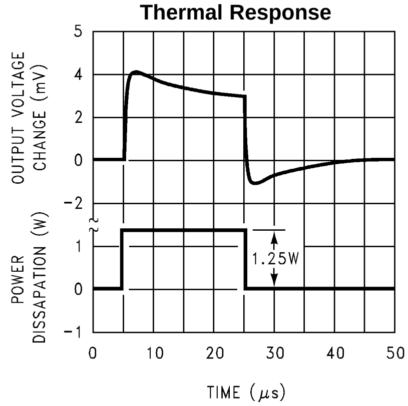


Figure 35.

APPLICATION HINTS

EXTERNAL CAPACITORS

A 1.0µF (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or more. At lower output voltages, more capacitance is required. Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 µF for currents below 10 mA or 0.1 µF for currents below 1 mA. Using the 8-pin version at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 µF (or greater) capacitor should be used.

Unlike many other regulators, the LP4950C will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP4951C version with external resistors, a minimum load of 1µA is recommended.

A 0.1µF capacitor should be placed from the LP4950C/LP4951C input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

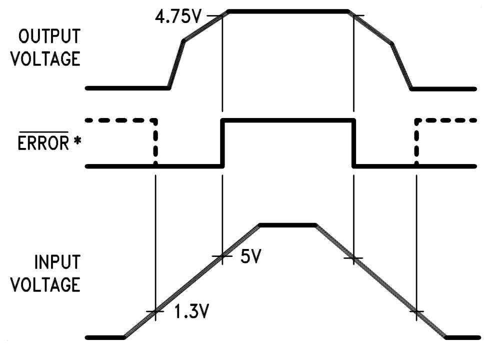
Stray capacitance to the LP4951C Feedback terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3µF will fix this problem.

ERROR DETECTION COMPARATOR OUTPUT

The comparator produces a logic low output whenever the LP4951C output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (See to the block diagram in the front of the datasheet.) This trip level remains “5% below normal” regardless of the programmed output voltage of the 4951C. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 36 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP4951C input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75V). Since the LP4951C's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 MΩ. The resistor is not required if this output is unused.



*When V_{IN} ≤ 1.3V, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see Figure 37), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

Figure 36. $\overline{\text{ERROR}}$ Output Timing

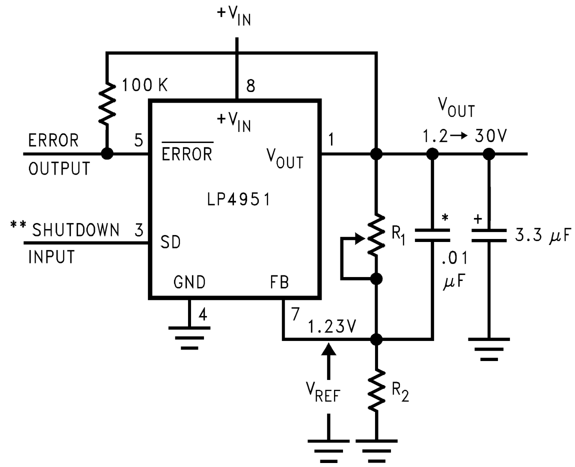
PROGRAMMING THE OUTPUT VOLTAGE (LP4951C)

The LP4951C may be pin-strapped for 5V using its internal voltage divider by tying the pin 1 (output) to pin 2 (sense) pins together, and also tying the pin 7 (feedback) and pin 6 (V_{TAP}) pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 37, an external pair of resistors is required.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1 \quad (1)$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1µA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the LP4951C typically draws 60µA at no load with Pin 2 open-circuited, this is a small price to pay.



*See Application Hints

$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

Figure 37. Adjustable Regulator (LP4951C)

REDUCING OUTPUT NOISE

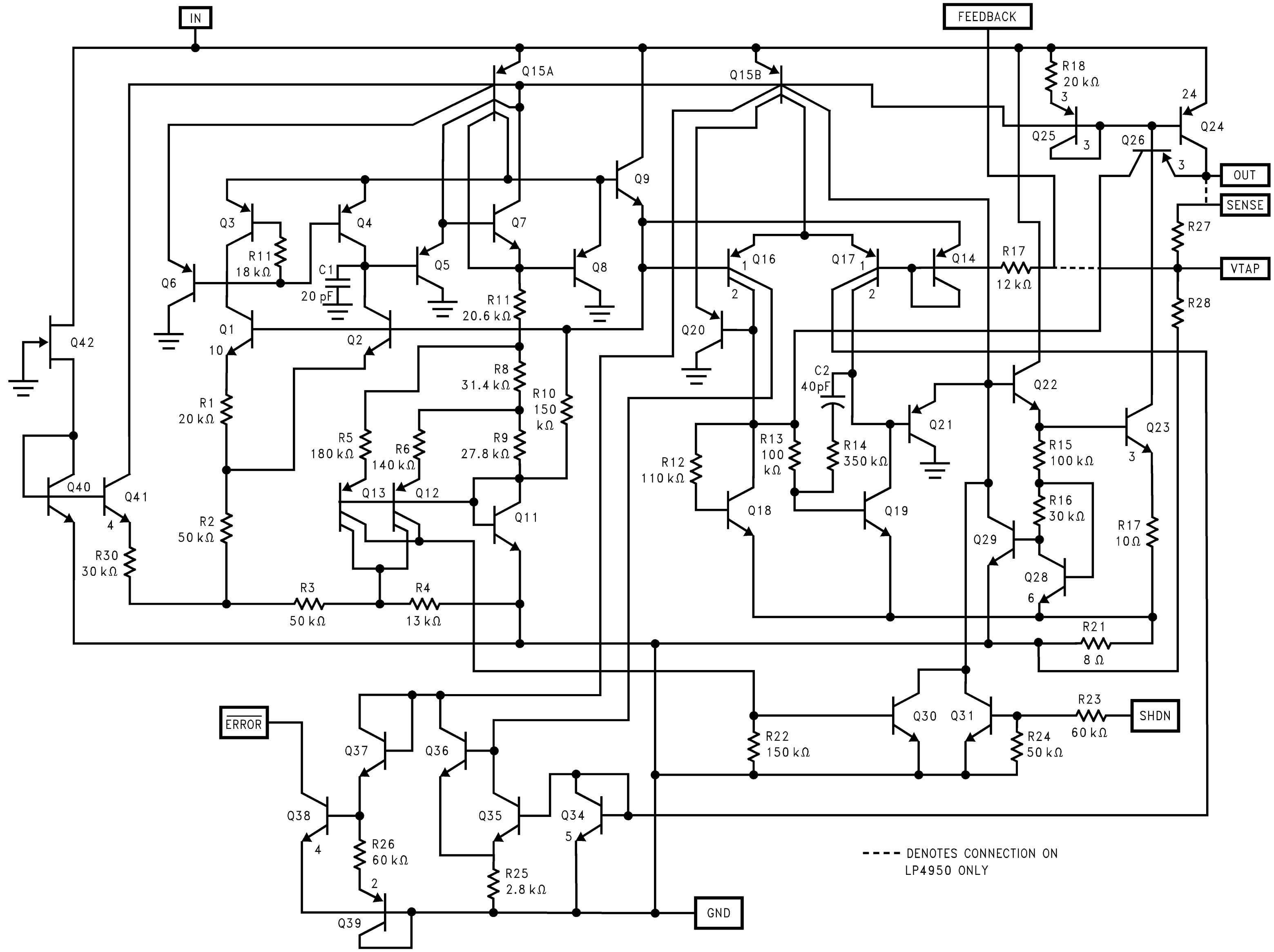
In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP4950C but is relatively inefficient, as increasing the capacitor from 1µF to 220µF only decreases the noise from 430µV to 160µV rms for a 100kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ \text{Hz}} \tag{2}$$

or about 0.01µF. When doing this, the output capacitor must be increased to 3.3µF to maintain stability. These changes reduce the output noise from 430µV to 100µV rms for a 100kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

SCHEMATIC DIAGRAM



REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP4951CM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP495 1CM
LP4951CM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP495 1CM
LP4951CMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP495 1CM
LP4951CMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LP495 1CM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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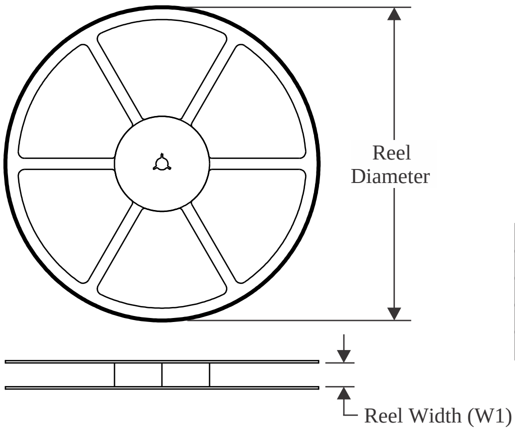
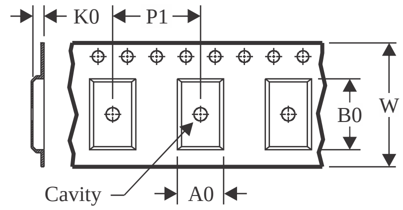
TAPE AND REEL INFORMATION

REEL DIMENSIONS

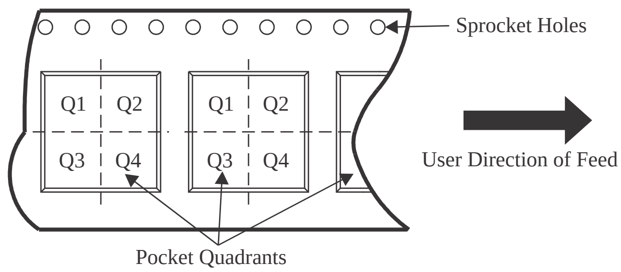


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

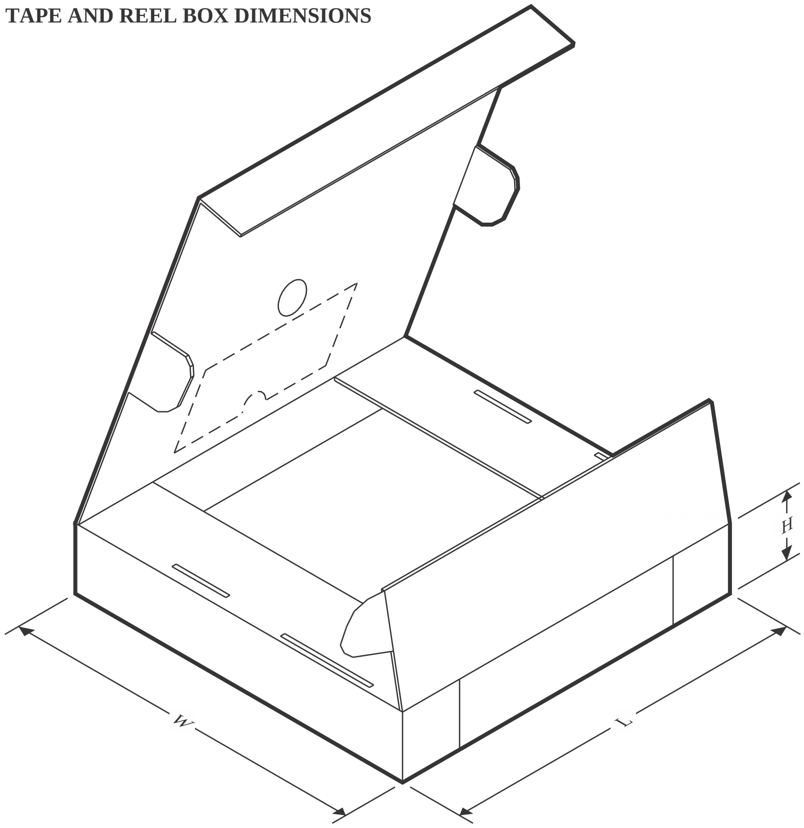
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP4951CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

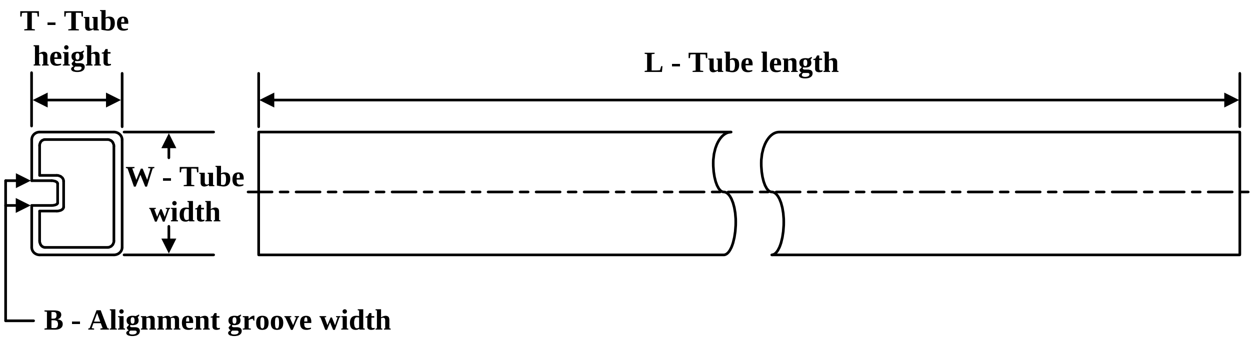
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

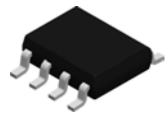
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP4951CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP4951CM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP4951CM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

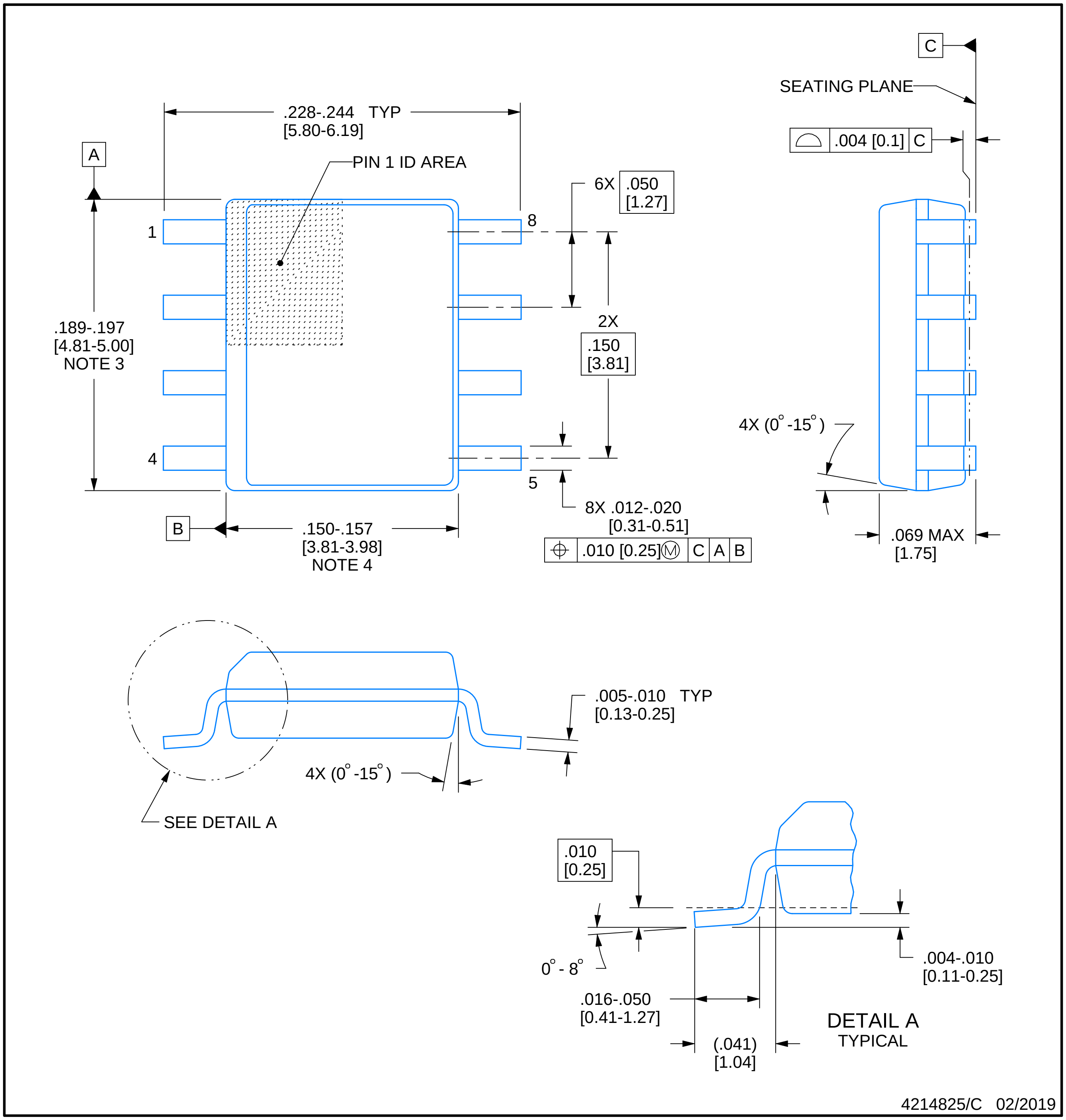


PACKAGE OUTLINE

D0008A

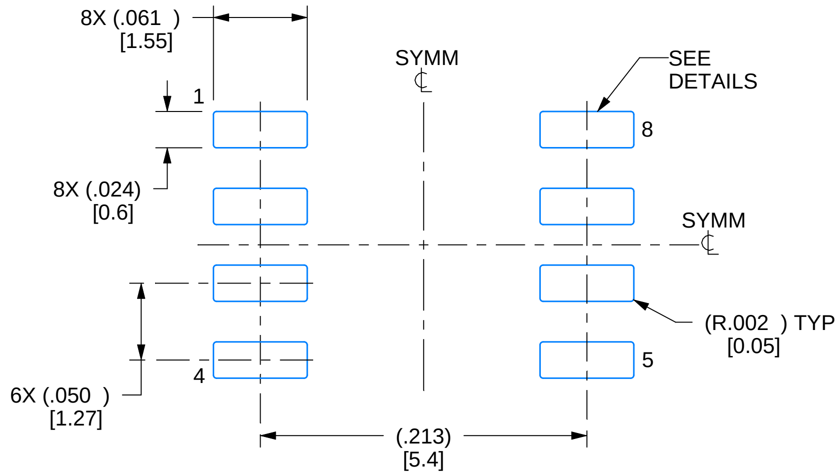
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

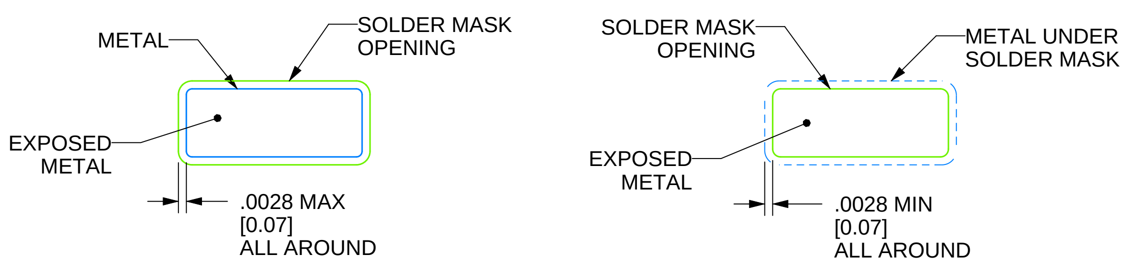


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

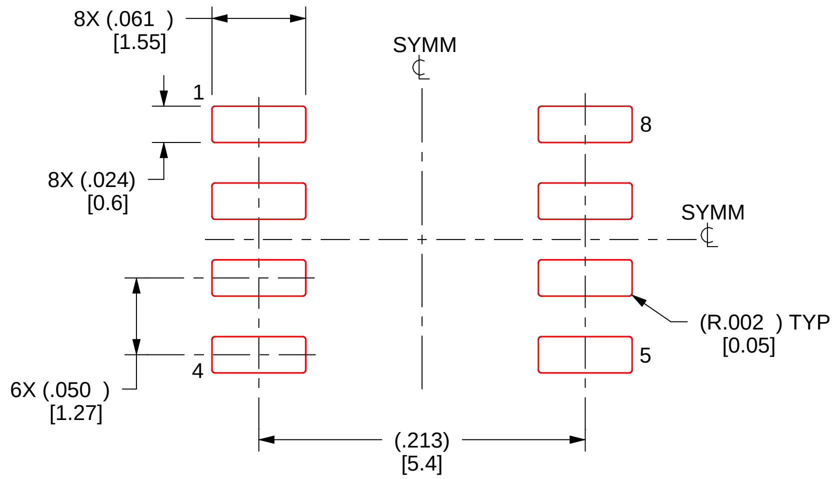
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.