# LP5814 4-Channel I²C Interface RGBW LED Driver with Auto Animation Control

## 1 Features

- Operating voltage range
  - $V_{CC}$ range: 2.5V to 5.5V
  - Logic pins compatible with 1.8V, 3.3V, and 5V
  - Output voltage up to 5.5V
- 4 constant current sinks with high precision
  - 0.1mA to 51mA per channel
  - Device-to-device error: ±8% (max.)
  - Channel-to-channel error: ±3% (max.)
  - Ultra-low headroom voltage: 135mV (max.) at 25.5mA; 275mV (max.) at 51mA
- Ultra-low power consumption
  - Shutdown: $I_{SD}$ = 0.1µA (typ.)
  - Standby: $I_{STB}$ = 22µA (typ.)
  - Active:
    - $I_{NOR}$ = 0.15mA(typ.), when disable output channel
    - $I_{NOR}$ = 0.23mA(typ.), LED current = 25.5mA
- Analog dimming (current gain control)
  - Global 1-bit Maximum Current (MC) 25.5mA/ 51mA
  - Individual 8-bits Dot Current (DC) setting
- PWM dimming up to audible-noise-free 23kHz
  - Individual 8-bits PWM dimming resolution
  - Linear or exponential dimming curves
- Autonomous animation engine control
- 1MHz (max.) I²C interface
- ESD: 4kV HBM, 1.5kV CDM
- Package
  - 1.6 x 2.1mm SOT583-8, 0.5mm pitch
  - 1.36 x 0.8mm DSBGA-8, 0.35mm pitch
- –40°C to 125°C operating temperature range

## 2 Applications

LED animation and indication for:

- Personal Electronics
  - Virtual Reality (VR) Headset
  - Gaming Controller and Peripherals
  - Electronic and Robotic Toys
  - Smart Speaker
  - Wireless Speaker
  - Solid State Drive (SSD)
  - Electronic Smart Lock
  - Headsets/Headphones and Earbuds
  - GPS Personal Navigation Device
- WLAN/Wi-Fi Access Point
- Video Doorbell
- Video Conference System

## 3 Description

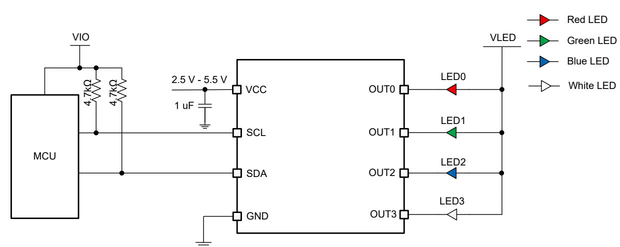
The LP5814 is a 4-channel RGBW LED driver with autonomous animation engine control. The device has ultra-low operation current with 0.1µA (typical) in shutdown mode, 0.1mA (typical) when enable device and 0.2mA (typical) when illuminate LEDs.

Both analog dimming and PWM dimming methods are adopted to achieve powerful dimming performance. The output current of each LED can be adjusted with 256 steps from 0.1mA to 25.5mA or 0.2mA to 51mA. The 8-bits PWM generator enables smooth and audible-noise-free dimming control for LED brightness.

The autonomous animation engine can significantly reduce the real-time loading of controller. Each LED can be configured through the related registers to realize vivid and fancy lighting effects.

**Package Information**

| PART NUMBER | PACKAGE | PACKAGE SIZE (NOM) |
|---|---|---|
| LP5814DRLR | SOT583 (8) | 1.6mm × 2.1mm |
| LP5814YCHR | DSBGA (8) | 1.36mm × 0.8mm |




**LP5814 Simplified Schematic**

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# 4 Device Comparison

<table>
<tr><th>PART NUMBER</th><th>PACKAGE (1)</th><th>MATERIAL</th><th>LED NUMBER</th><th>AUTO ANIMATIO</th><th>INSTANT BLINKING</th><th>I²C ADDRESS</th><th>SOFTWARE COMPATIBLE</th></tr>
<tr><td rowspan="3">LP5814</td><td>SOT583-8</td><td>LP5814DRLR</td><td rowspan="3">4</td><td rowspan="5">Yes</td><td rowspan="2">No</td><td rowspan="3">0x2C</td><td rowspan="9">Yes</td></tr>
<tr><td>DSBGA-8</td><td>LP5814YCHR</td></tr>
<tr><td>DSBGA-8</td><td>LP5814IYCHR</td><td rowspan="3">Yes</td></tr>
<tr><td rowspan="2">LP5815</td><td>SOT583-8</td><td>LP5815DRLR</td><td rowspan="2">3</td><td rowspan="2">0x2D</td></tr>
<tr><td>DSBGA-8</td><td>LP5815YCHR</td></tr>
<tr><td rowspan="2">LP5816</td><td>SOT583-8</td><td>LP5816DRLR</td><td rowspan="2">4</td><td rowspan="4">No</td><td rowspan="4">No</td><td rowspan="2">0x2C</td></tr>
<tr><td>DSBGA-8</td><td>LP5816YCHR</td></tr>
<tr><td rowspan="2">LP5817</td><td>SOT583-8</td><td>LP5817DRLR</td><td rowspan="2">3</td><td rowspan="2">0x2D</td></tr>
<tr><td>DSBGA-8</td><td>LP5817YCHR</td></tr>
</table>

(1) For the most up-to-date packaging information refer to the Section 11.

# 5 Pin Configuration and Functions

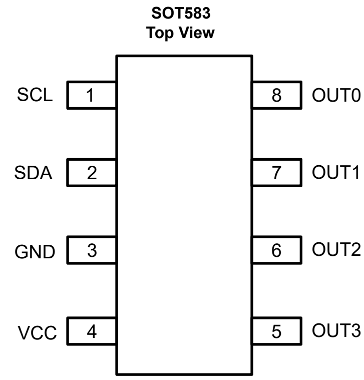



**Figure 5-1. LP5814 DRL Package 8-Pin SOT583 Top View**

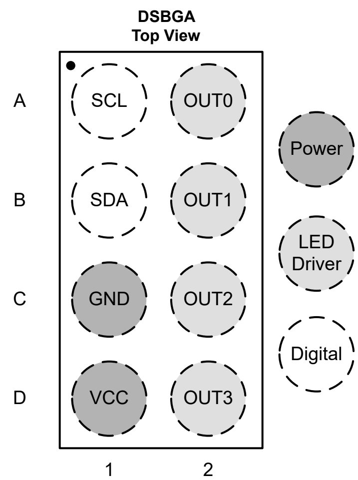



**Figure 5-2. LP5814 YCH Package 8-Pin DSBGA Top View**

**Table 5-1. Pin Functions**

| PIN | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NAME | DRL | YCH | | |
| SCL | 1 | A1 | I | $I^2C$ serial interface clock input. |
| SDA | 2 | B1 | I/O | $I^2C$ serial interface data input/output. |
| GND | 3 | C1 | P | Ground. |
| VCC | 4 | D1 | P | Power supply of the device. A 1 µF capacitor is recommended to be connected between this pin with GND and be placed as close to the device as possible. |
| OUT3 | 5 | D2 | O | Constant current sink output 3. |
| OUT2 | 6 | C2 | O | Constant current sink output 2. |
| OUT1 | 7 | B2 | O | Constant current sink output 1. |
| OUT0 | 8 | A2 | O | Constant current sink output 0. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range at terminals | VCC, SCL, SDA, OUT0, OUT1, OUT2, OUT3 | –0.3 | 6 | V |
| $T_J$ | Junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±4000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2] | ±1500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Input voltage range | 2.5 | | 5.5 | V |
| $C_{IN}$ | Effective input capacitance range | 1 | 4.7 | | µF |
| OUT0, OUT1, OUT2, OUT3 | Voltage on OUT0, OUT1, OUT2, OUT3 pins | 0 | | 5.5 | V |
| SCL, SDA | Voltage on SCL, SDA pins | 0 | | 5.5 | V |
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | LP5814 DRL (SOT583) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 118.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 47.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 27.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 27.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < $T_A$ < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1μF.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{CC}$ | Input voltage range | | 2.5 | | 5.5 | V |
| $V_{CC\_UVLO}$ | Under-voltage lockout threshold | $V_{CC}$ rising | 2.2 | 2.3 | 2.4 | V |
| | | $V_{CC}$ falling | 2 | 2.1 | 2.2 | V |
| $I_{SD}$ | Shutdown current into VCC pin | $V_{CC}$ = 3.6V | | 0.1 | 0.3 | μA |
| $I_{STB}$ | Standby current into VCC pin | $V_{CC}$ = 3.6V, CHIP_EN = 0 (bit) | | 22 | 26 | μA |
| $I_{NOR}$ | Normal operation current into VCC pin | $V_{CC}$ = 3.6V, CHIP_EN = 1 (bit), OUT0_EN = OUT1_EN = OUT2_EN = OUT3_EN = 0 (bit) | | 0.15 | 0.17 | mA |
| $I_{NOR}$ | Normal operation current into VCC pin | $V_{CC}$ = 3.6V, CHIP_EN = 1 (bit), OUT0_EN = OUT1_EN = OUT2_EN = OUT3_EN = 1 (bit), $I_{OUT0}$ = $I_{OUT1}$ = $I_{OUT2}$ = $I_{OUT3}$ = 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh) | | 0.23 | 0.29 | mA |
| **LED Driver Output** | | | | | | |
| $I_{CS}$ | Constant current sink output range | $V_{CC}$ = 3.6V, VLED = 5V, MAX_CURRENT = 0 (bit), OUTx_MANUAL_PWM = FFh (100% ON) | 0.1 | | 25.5 | mA |
| | | $V_{CC}$ = 3.6V, VLED = 5V, MAX_CURRENT = 1 (bit), OUTx_MANUAL_PWM = FFh (100% ON) | 0.2 | | 51 | mA |
| $I_{CS\_LKG}$ | Constant current sink leakage current | $V_{CC}$ = 3.6V, OUTx = 1V, OUTx_MANUAL_PWM = 0 (0%) | | 0.1 | 1 | μA |
| $I_{ERR\_D2D}$ | Device to device current error, $I_{ERR\_D2D} = (I_{AVE}-I_{SET})/I_{SET}\times100\%$ | All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh) | –8 | | 8 | % |
| | | All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh) | –8 | | 8 | % |
| $I_{ERR\_C2C}$ | Channel to Channel current error $I_{ERR\_C2C} = (I_{OUTX}-I_{AVE})/I_{AVE}\times100\%$ | All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh) | –3 | | 3 | % |
| | | All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh) | –2 | | 2 | % |
| $V_{HR}$ | LED driver output headroom voltage | All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), $V_{CC}$ = 3.6V | | | 0.135 | V |
| | | All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), $V_{CC}$ = 3.6V | | | 0.275 | V |
| | | All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), $V_{CC}$ = 2.5V | | | 0.15 | V |
| | | All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), , $V_{CC}$ = 2.5V | | | 0.3 | V |
| $f_{LED\_PWM}$ | PWM dimming frequency | | | 23 | | kHz |
| $f_{OSC}$ | Internal oscillator frequency | | | 6 | | MHz |

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < $T_A$ < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1μF.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Logic Interface** | | | | | | |
| $V_{IH\_LOGIC}$ | High level input voltage of SDA, SCL | | 1.4 | | | V |
| $V_{IL\_LOGIC}$ | Low level input voltage of SDA, SCL | | | | 0.4 | V |
| $V_{OL\_LOGIC}$ | Low level output voltage of SDA | | | | 0.4 | V |
| **Protection** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold for LED driver part | $T_J$ rising | | 150 | | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | $T_J$ falling below $T_{SD}$ | | 15 | | °C |

## 6.6 Timing Requirements

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < TA < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1μF.

| $I^2C$ Timing Requirements | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Standard-mode** | | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | | 100 | kHz |
| 1 | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4 | | | μs |
| 2 | LOW period of the SCL clock | 4.7 | | | μs |
| 3 | HIGH period of the SCL clock | 4 | | | μs |
| 4 | Set-up time for a repeated START condition | 4.7 | | | μs |
| 5 | Data hold time | 0 | | | μs |
| 6 | Data set-up time | 250 | | | ns |
| 7 | Rise time of both SDA and SCL signals | | | 1000 | ns |
| 8 | Fall time of both SDA and SCL signals | | | 300 | ns |
| 9 | Set-up time for STOP condition | 4 | | | μs |
| 10 | Bus free time between a STOP and START condition | 4.7 | | | μs |
| $C_b$ | Capacitive load for each bus line | | | 400 | pF |
| **Fast-mode** | | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | | 400 | kHz |
| 1 | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.6 | | | μs |
| 2 | LOW period of the SCL clock | 1.3 | | | μs |
| 3 | HIGH period of the SCL clock | 0.6 | | | μs |
| 4 | Set-up time for a repeated START condition | 0.6 | | | μs |
| 5 | Data hold time | 0 | | | μs |
| 6 | Data set-up time | 100 | | | ns |
| 7 | Rise time of both SDA and SCL signals | | | 300 | ns |
| 8 | Fall time of both SDA and SCL signals | | | 300 | ns |
| 9 | Set-up time for STOP condition | 0.6 | | | μs |
| 10 | Bus free time between a STOP and START condition | 1.3 | | | μs |
| $C_b$ | Capacitive load for each bus line | | | 400 | pF |
| **Fast-mode Plus** | | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | | 1000 | kHz |
| 1 | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26 | | | μs |

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < TA < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1µF.

| $I^2C$ Timing Requirements | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| 2 | LOW period of the SCL clock | 0.5 | | | µs |
| 3 | HIGH period of the SCL clock | 0.26 | | | µs |
| 4 | Set-up time for a repeated START condition | 0.26 | | | µs |
| 5 | Data hold time | 0 | | | µs |
| 6 | Data set-up time | 50 | | | ns |
| 7 | Rise time of both SDA and SCL signals | | | 120 | ns |
| 8 | Fall time of both SDA and SCL signals | | | 120 | ns |
| 9 | Set-up time for STOP condition | 0.26 | | | µs |
| 10 | Bus free time between a STOP and START condition | 0.5 | | | µs |
| $C_b$ | Capacitive load for each bus line | | | 550 | pF |

## 6.7 Timing Diagrams

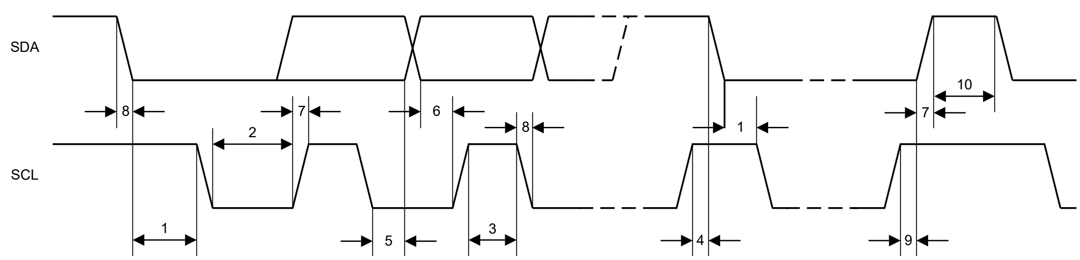



**Figure 6-1. $I^2C$ Timing Parameters**

## 6.8 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < $T_A$ < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1µF

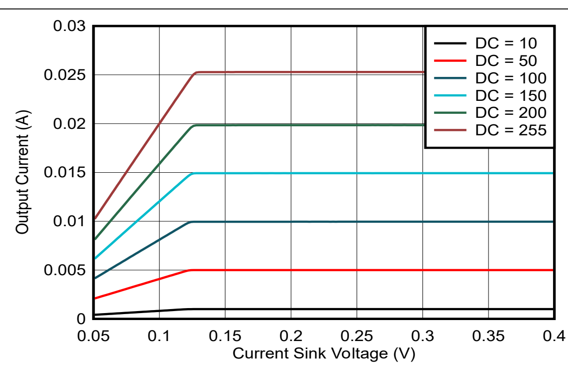



**Figure 6-2. Current Sinks Voltage vs Current (MC = 0, VCC = 2.5V)**

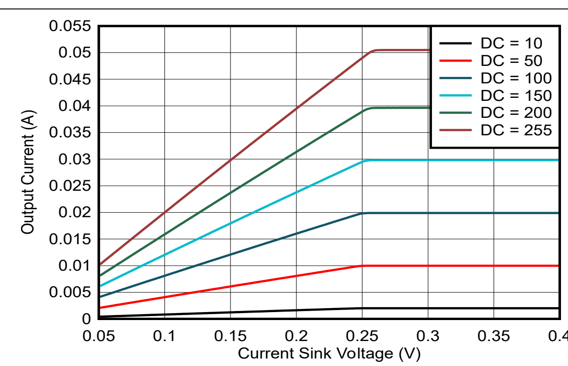



**Figure 6-3. Current Sinks Voltage vs Current (MC = 1, VCC = 2.5V)**

## 6.8 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < $T_A$ < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1μF

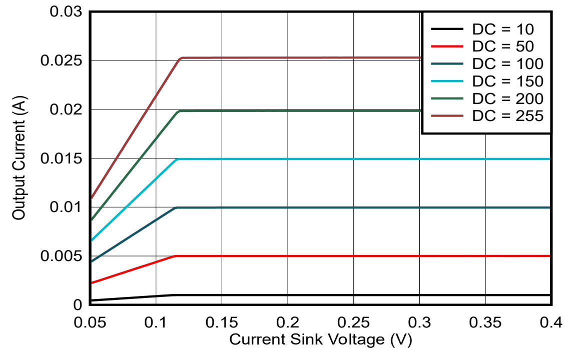



**Figure 6-4. Current Sinks Voltage vs Current (MC = 0, VCC = 3.6V)**

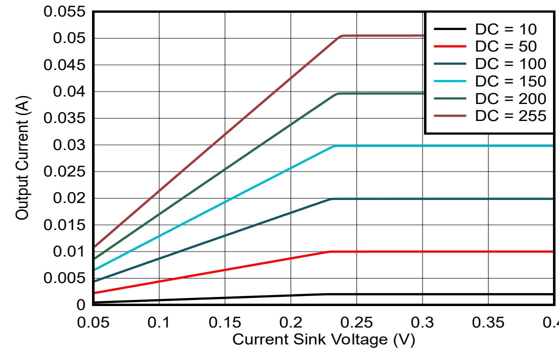



**Figure 6-5. Current Sinks Voltage vs Current (MC = 1, VCC = 3.6V)**

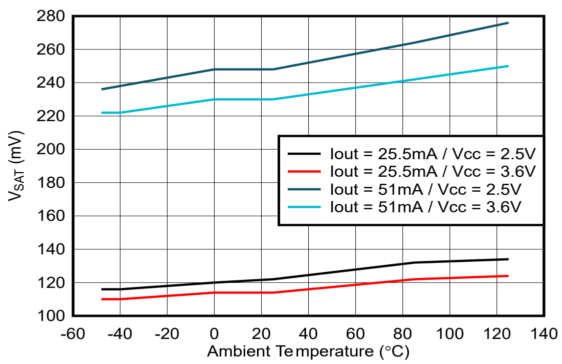



**Figure 6-6. $V_{SAT}$ vs Temperature**

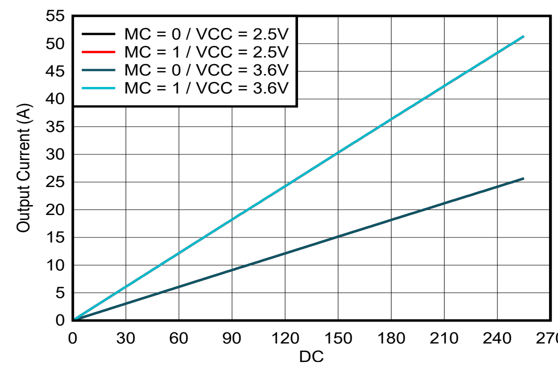



**Figure 6-7. DC vs Current**

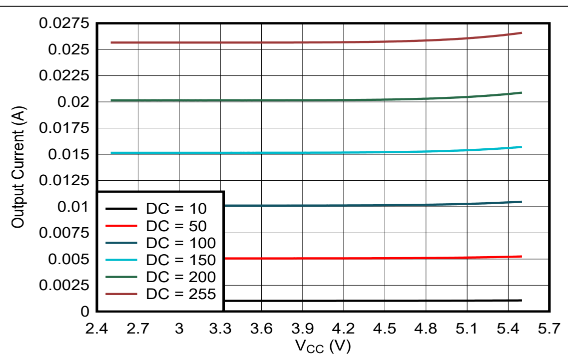



**Figure 6-8. $V_{CC}$ vs Current (MC = 0)**

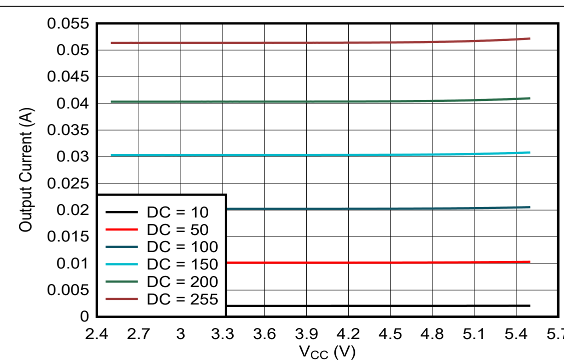



**Figure 6-9. $V_{CC}$ vs Current (MC = 1)**

## 6.8 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < $T_A$ < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1µF

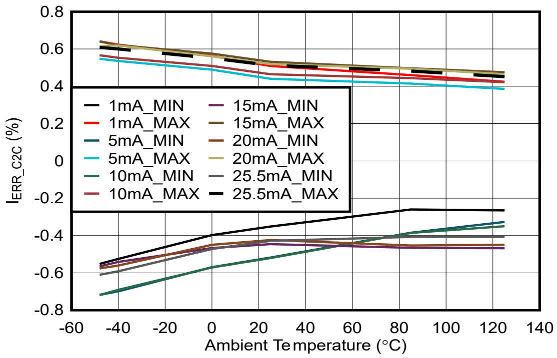



**Figure 6-10. Channel-to-Channel Current Accuracy vs Temperature (MC = 0, VCC = 2.5V)**

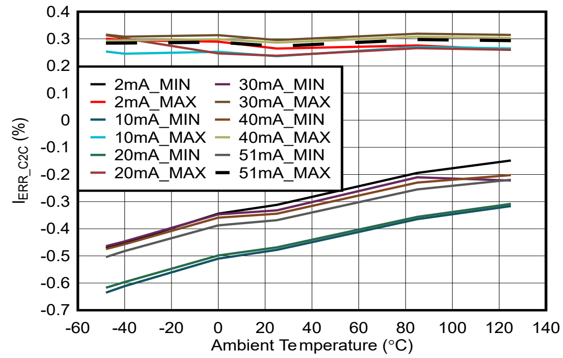



**Figure 6-11. Channel-to-Channel Current Accuracy vs Temperature (MC = 1, VCC = 2.5V)**

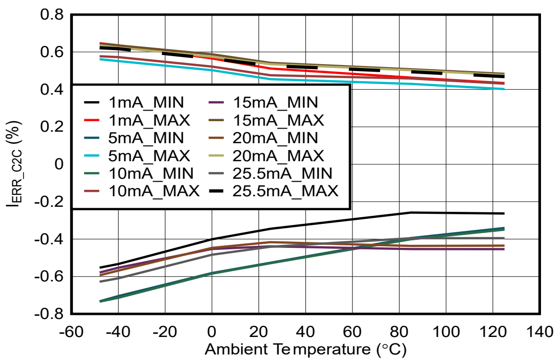



**Figure 6-12. Channel-to-Channel Current Accuracy vs Temperature (MC = 0, VCC = 3.6V)**

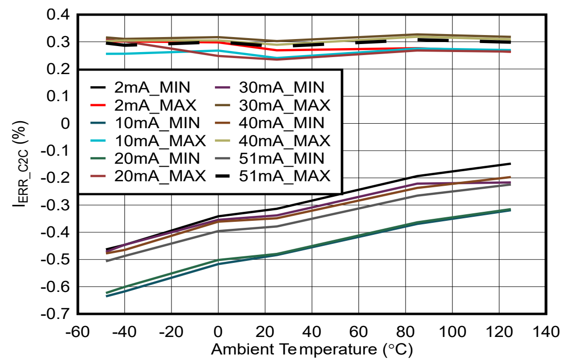



**Figure 6-13. Channel-to-Channel Current Accuracy vs Temperature (MC = 1, VCC = 3.6V)**

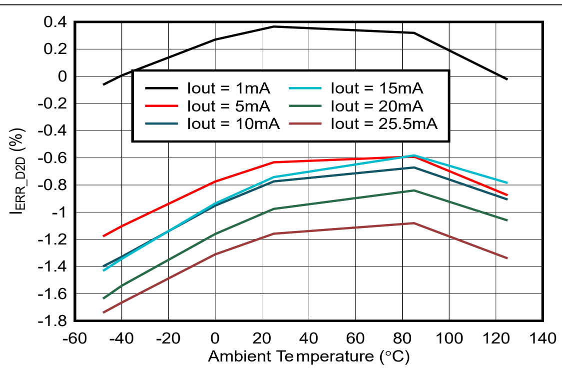



**Figure 6-14. Device-to-Device Current Accuracy vs Temperature (MC = 0, VCC = 2.5V)**

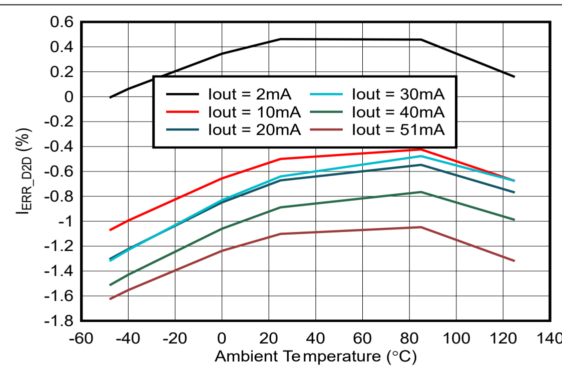



**Figure 6-15. Device-to-Device Current Accuracy vs Temperature (MC = 1, VCC = 2.5V)**

## 6.8 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < $T_A$ < +85°C ), $V_{CC}$ = 3.6V, $C_{IN}$ = 1µF

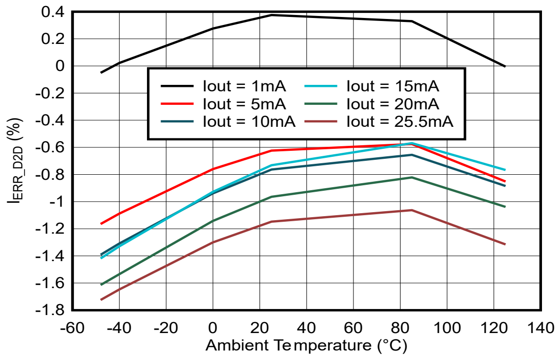



**Figure 6-16. Device-to-Device Current Accuracy vs Temperature (MC = 0, VCC = 3.6V)**

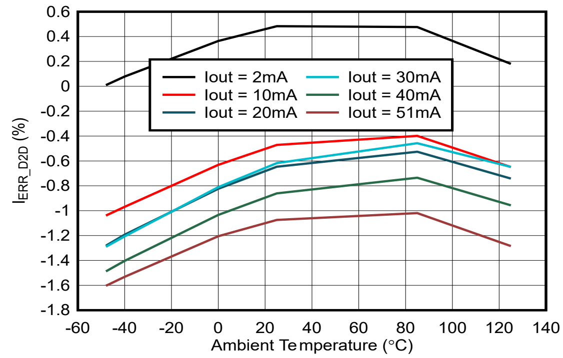



**Figure 6-17. Device-to-Device Current Accuracy vs Temperature (MC = 1, VCC = 3.6V)**

# 7 Detailed Description

## 7.1 Overview

The LP5814 is a 4 channel RGBW LED driver and autonomous animation control. The maximum output current of each channel is up to 51mA and can be adjusted by 256 steps from 0 to the full current. Besides the annalog dimming, every channel supports 8-bit PWM dimming in both manaul mode and autonomous animation mode.

The LP5814 features ultra-low shutdown current that is about 0.1uA. Two approaches are provided to control the LP5814 enter shutdown mode, sending shutdown command or constantly pulling down SCL, which improves the flexibility in system design for different application requirements.

The LP5814 integrates advanced autonomous animation control architecture. Four basic configurable independent pattern units can be selected and organized for each channel arbitrarily to realize both simple and complicated pattern effects.

## 7.2 Functional Block Diagram

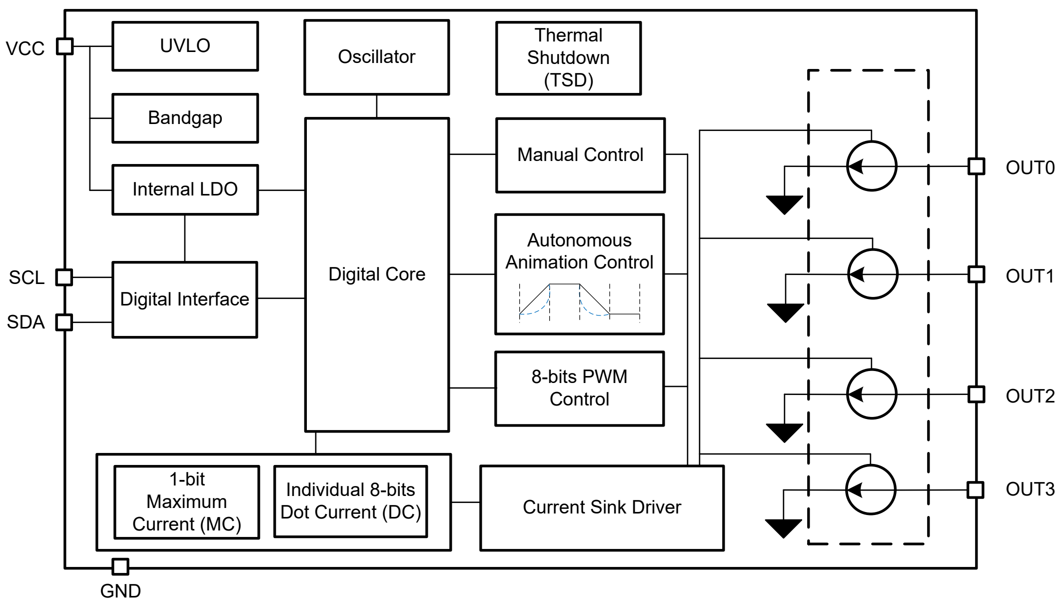



**Figure 7-1. LP5814 Function Block**

## 7.3 Feature Description

### *7.3.1 Analog Dimming*

There are two methods to control the current gain of each output channel.

- Global 1-bit Maximum Current (MC) control for all channels without external resistor
- Individual 8-bit Dot Current (DC) control for each channel

The maximum output current $I_{OUT\_max}$ of each channel can be programmed by the 1 bit MAX_CURRENT. When the device is powered on, the default value of MC is 0h, which is 25.5mA.

**Table 7-1. Maximum Current (MC) Bit Setting**

| 1-bit Maximum Current (MC) | | $I_{OUT\_MAX}$ (mA) |
|---|---|---|
| Binary | Decimal | |
| 0 (default) | 0 (default) | 25.5 (default) |
| 1 | 1 | 51 |

The LP5814 can individually adjust the analog output current of each channel by using Dot Current (DC) function. The brightness deviation among the LED bins can be miminized to achieve uniform display performance through the DC setting. The DC is programmed in an 8-bit depth, so the analog current can be adjusted with 256 steps from 0 to 100% of $I_{OUT\_MAX}$.. The default value of all DC is 0h, which is not current output.

**Table 7-2. Dot Current (DC) Bits Setting**

| 8-bits Dot Current (DC) Register | | Ratio of $I_{OUT\_MAX}$ |
|---|---|---|
| Binary | Decimal | |
| 0000 0000 (default) | 0 (default) | 0% (default) |
| 0000 0001 | 1 | 0.39% |
| 0000 0010 | 2 | 0.78% |
| --- | --- | --- |
| 1000 0000 | 128 | 50.2% |
| --- | --- | --- |
| 1111 1101 | 253 | 99.2% |
| 1111 1110 | 254 | 99.6% |
| 1111 1111 | 255 | 100% |

By configuring the MC and DC, the analog output current of each channel can be calculated as Equation 1:

$$I_{OUT}\left(mA\right) = I_{OUT\_MAX} \times \frac{DC}{255} \tag{1}$$

The average output current of each channel can be caculated asEquation 2:

$$I_{AVE}\left(mA\right) = I_{OUT\_MAX} \times \frac{DC}{255} \times D_{PWM} \tag{2}$$

- $D_{PWM}$ is the PWM duty.

### 7.3.2 PWM Dimming

The LP5814 supports 8-bit PWM dimming with 23kHz frequency in both manual mode and autonomous animation mode. The device integrates an internal 6MHz oscillator to generate the PWM clock.

The LP5814 allows users to configure the dimming scale as exponential curve or linear curve for each channel separately through the OUT0_EXP_EN, OUT1_EXP_EN, OUT2_EXP_EN and OUT3_EXP_EN in DEV_CONFIG3 register. A human-eye-friendly visual performance can be achieved by using the internal exponential scale. The linear scale has great linearity between PWM duty cycle and PWM setting value, which provides flexible approach for external controlled gamma correction algorithm. The 8-bit linear and exponential curves are shown as Figure 7-2.

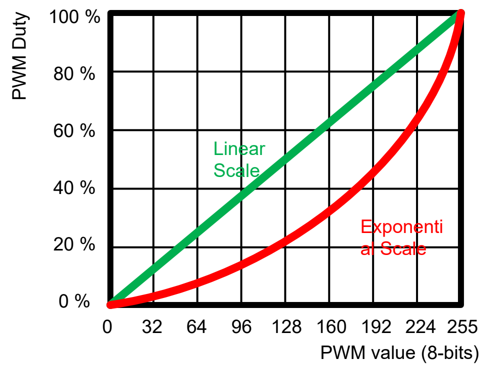



**Figure 7-2. Linear and Exponential PWM Dimming Curves**

### 7.3.3 Sloper

In manual control mode, output fade in or out is supported when LED0_FADE_EN, LED1_FADE_EN, LED2_FADE_EN and LED3_FADE_EN bit in DEV_CONFIG2 register is set as 1. Sloper is the basic element to achieve autonomous fade in and fade out animations. The output can achieve 256 steps fade in or fade out effects from 'PWM_Start' to 'PWM_End' within a specified time period T as shown in Figure 7-3. Exponential dimming curve can also be supported in the sloper.

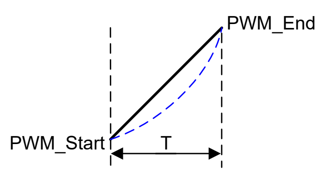



**Figure 7-3. Sloper Curve Demonstration**

The programable time T is selectable from 0 to around 8s with 16 levels shown in Table 7-3.

**Table 7-3. Programable Time Options**

| Register Value | 0h | 1h | 2h | 3h | 4h | 5h | 6h | 7h | 8h | 9h | Ah | Bh | Ch | Dh | Eh | Fh |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Time (Typ.) | 0s | 0.05s | 0.1s | 0.15s | 0.2s | 0.25s | 0.3s | 0.35s | 0.4s | 0.45s | 0.5s | 1s | 2s | 4s | 6s | 8s |

### 7.3.4 Autonomous Animation Control

The LP5814 supports autonomous animation control for each channel. With the animation engine the device can realize vivid lighting effects while releasing the loading of external controller.

As showed in Figure 7-4 , the LP5814 has 4 independent configurable animation engine units, ENGINE0, ENGINE1, ENGINE2 and ENGINE3. Any one of the 4 engines can be selected by each output channel. There are 4 engine orders to construct one engine unit. For each engine order, one pattern unit can be selected to execute when the engine order is enabled. At the bottom layer, there are 4 independent configurable pattern units.

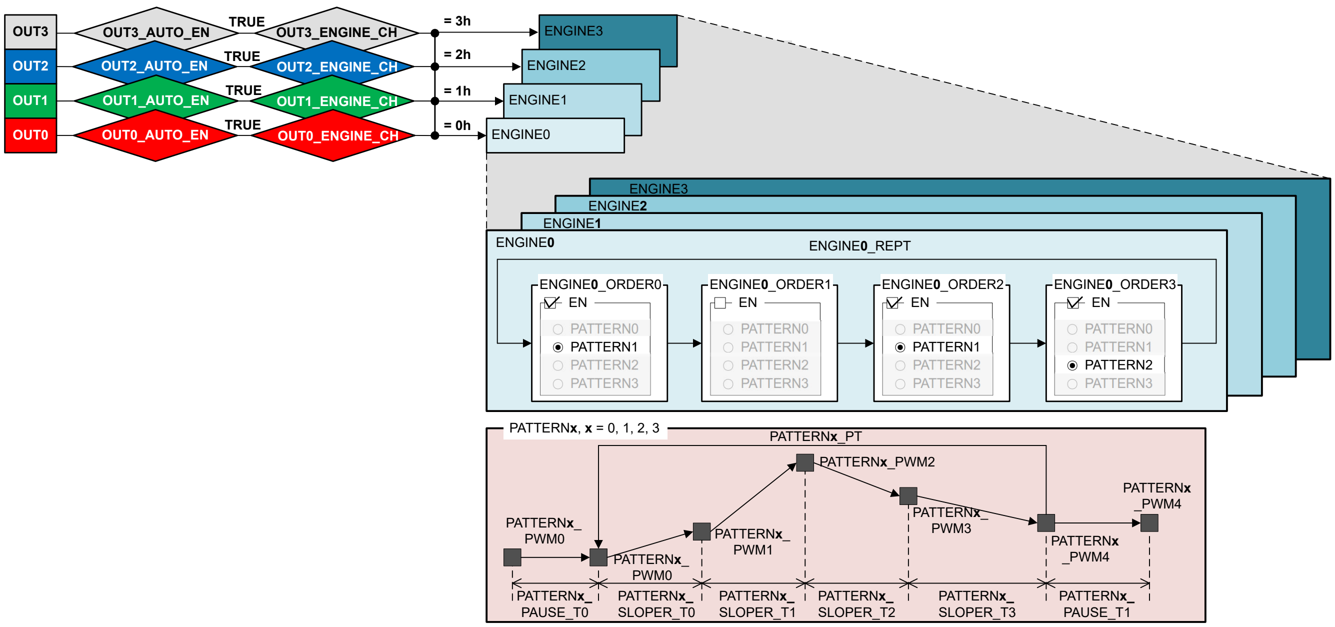



**Figure 7-4. Animation Pattern Overview**

#### 7.3.4.1 Animation Engine Unit

The LP5814 has 4 independent animation engine units ENGINE0, ENGINE1, ENGIN2 and ENGINE3. For each output, any one of the 4 engines can be selected by setting the register OUT*x*_ENGINE_CH bits in DEV_CONFIG4 register (*x* = 0, 1, 2 , 3).

- OUT*x*_ENGINE_CH = 0, ENGINE0 is selected
- OUT*x*_ENGINE_CH = 1, ENGINE1 is selected
- OUT*x*_ENGINE_CH = 2, ENGINE2 is selected
- OUT*x*_ENGINE_CH = 3, ENGINE3 is selected

There are 4 engine orders, ENGINE*x*_ORDER0, ENGINE*x*_ORDER1, ENGINE*x*_ORDER2 and ENGINE*x*_ORDER3, to construct one engine unit ENGINE*x* (*x* = 0, 1, 2, 3). The 4 engine orders in one engine unit is executed sequentially. But any one of the 4 engine orders can be skipped by disabling the engine order through setting the corresponding E*x*O*y*_EN bit as 0 (*x*, *y* = 0, 1, 2, 3) in ENGINE_CONFIG4 and ENGINE_CONFIG5 registers.

If 4 engine orders in one engine unit are all disabled, the engine unit is not started after sending the Start_command. The corresponding internal engine busy flag is not set as shown in Figure 7-7.

The engine unit ENGINE*x* can be defined to execute repeately as the times specified in ENGINE*x*_REPT in ENGINE_CONFIG6 register.

- ENGINE*x*_REPT = 0, ENGINEx does not repeat
- ENGINE*x*_REPT = 1, ENGINEx repeats 1 time
- ENGINE*x*_REPT = 2, ENGINEx repeats 2 times

- ENGINE*x*_REPT = 3, ENGINEx repeats infinitely

Engine order is enabled by setting the corresponding E*x*O*y*_EN bit as 1. Any one of 4 basic patterns can be selected through the ENGINE*x*_ORDER*y* from ENGINE_CONFIG0 to ENGINE_CONFIG3 registers (*x*, *y* = 0, 1, 2, 3).

- ENGINEx_ORDERy = 0, PATTERN0 is selected
- ENGINEx_ORDERy = 1, PATTERN1 is selected
- ENGINEx_ORDERy = 2, PATTERN2 is selected
- ENGINEx_ORDERy = 3, PATTERN3 is selected

#### 7.3.4.2 Animation Pattern Unit

The LP5814 has 4 independent configurable pattern units, PATTERN0, PATTERN1, PATTERN2 and PATTERN3. Every pattern unit has 5 PWM values, 6 time values and 1 play times value.

For PATTERN*x* (*x* = 0, 1, 2, 3),

- The 5 PWM values are stored in PATTERN*x*_PWM0, PATTERN*x*_PWM1, PATTERN*x*_PWM2, PATTERN*x*_PWM3 and PATTERN*x*_PWM4. The 8 bits PWM value can be programmed from 0 to 255. Exponential dimming curve can also be supported in the sloper time.
- The 6 time values are devided into 2 types, pause time and sloper time. There are 2 pause time, PATTERN*x*_PAUSE_T0 and PATTERN*x*_PAUSE_T1. 4 sloper time, PATTERN*x*_SLOPER_T0, PATTERN*x*_SLOPER_T1, PATTERN*x*_SLOPER_T2 and PATTERN*x*_SLOPER_T3. Evey time value can be configured from 0 to 8s with 16 options.
- The pattern play times value is stored in PATTERN*x*_PT and can be configued from 0 to infinite times with 16 options. When the PATTERN*x*_PT = 0, the 2 pause time, output PWM0 for PAUSE_T0 and output PWM4 for PAUSE_T1, are still executed to construct the pattern unit.

Typical breathing effect example is illustrated as shown in Figure 7-5.

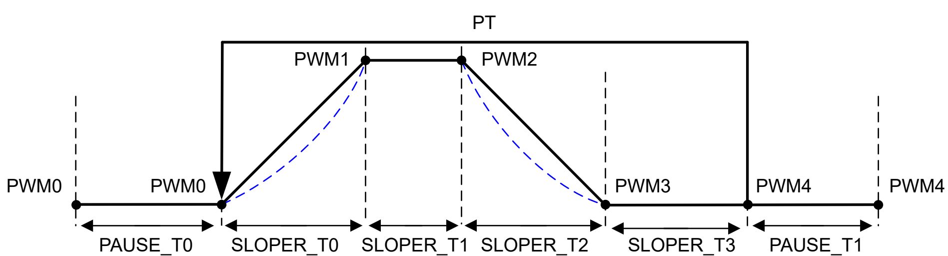



**Figure 7-5. Animation Pattern Unit - Example 1**

Advanced breathing effect example is shown in Figure 7-6. There are 2 different fading speeds are set in the PWM rising and falling phases, to achieve a complex animation.

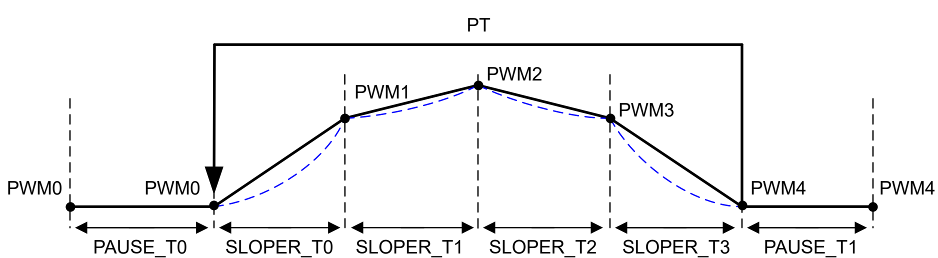



**Figure 7-6. Animation Pattern Unit - Example 2**

#### 7.3.4.3 Animation Control

The LP5814 has individual engine busy flag for each output channel, OUT0_ENGINE_BUSY, OUT1_ENGINE_BUSY, OUT2_ENGINE_BUSY and OUT3_ENGINE_BUSY, to indicate whether the engine selected by the output channel is under running or not. Besides the individule output busy flag there is a global engine busy flag, ENGINE_BUSY, to indicate if there is engine under running or not.

When the ENGINE_BUSY is set as 1, the engine configure registers and pattern configure registers shown in Table 7-4 are locked for modification protection. These engine busy lock registers can only be modified when **ENGINE_BUSY = 0**.

**Table 7-4. Engine Busy Lock Registers**

| Description | Register Address | Register Acronym |
|---|---|---|
| Engine configure registers | 0x06 to 0x0C | ENGINE_CONFIG0 to ENGINE_CONFIG6 |
| Pattern configure registers | 0x1C to 0x3F | • PATTERN*x*_PAUSE_TIME<br>• PATTERN*x*_REPEAT_TIME<br>• PATTERN*x*_PWM0<br>• PATTERN*x*_PWM1<br>• PATTERN*x*_PWM2<br>• PATTERN*x*_PWM3<br>• PATTERN*x*_PWM4<br>• PATTERN*x*_SLOPER_TIME1<br>• PATTERN*x*_SLOPER_TIME2<br>*x* = 0, 1, 2, 3 |

The LP5814 has 4 internal engine busy flags, ENGINE0_BUSY, ENGINE1_BUSY, ENGINE2_BUSY and ENGINE3_BUSY, as shown in Figure 7-7. The ENGINEy_BUSY is set as 1 after Start_command is received with all the below conditions.

- The engine has been selected by at least one channel, for example OUTx, and there is at least one engine order enabled in this engine
- The autonomous enable bit is set as 1 of the OUTx

The internal ENGINEy_BUSY flag keeps as 1 until the engine has completed or there is Stop_command received.

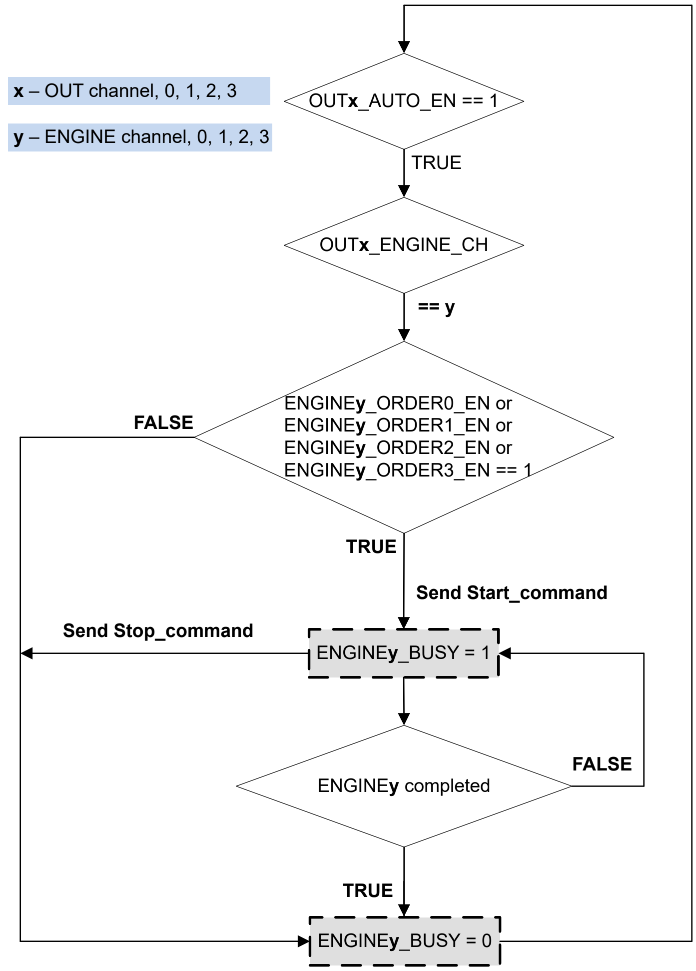



**Figure 7-7. Internal Engine Busy Status**

Any one of the internal engine busy flag, ENGINEx_BUSY, set to 1 leads to the global engine busy flag, ENGINE_BUSY, being 1, as shown in Figure 7-8.

The individual engine busy flag, OUTx_ENGINE_BUSY, is dependent on the internal engine busy flag selected by the correpsonding engine channel register value.

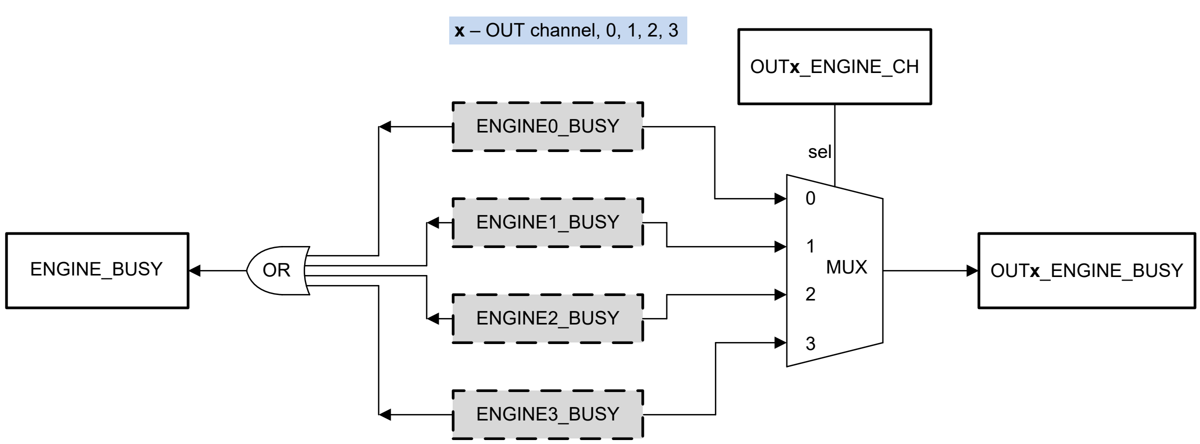



**Figure 7-8. Individual and Global Engine Busy Flag**

### 7.3.5 Protections

#### 7.3.5.1 UVLO

The LP5814 has an internal comparator that monitors the voltage at VCC. When $V_{CC}$ is below $V_{CC\_UVLO}$, the device resets and keeps in Power On Reset (POR) state. When $V_{CC}$ ramps above $V_{CC\_UVLO}$, the device enters INITIALIZATION mode and the POR flag is set. The POR flag needs manual clear by setting POR_CLR bit when CHIP_EN = 1.

#### 7.3.5.2 Thermal Shutdown

The LP5814 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature of the device rises to 155ºC (typical), the device turns off all output channels. The TSD flag is set to indicate thermal shutdown is triggered. The LP5814 releases thermal shutdown when the junction temperature reduces to 140ºC (typical). The TSD flag needs manual clear by setting TSD_CLR bit when CHIP_EN = 1.

### 7.4 Device Functional Modes

The Figure 7-9 shows the function modes of the LED driver.

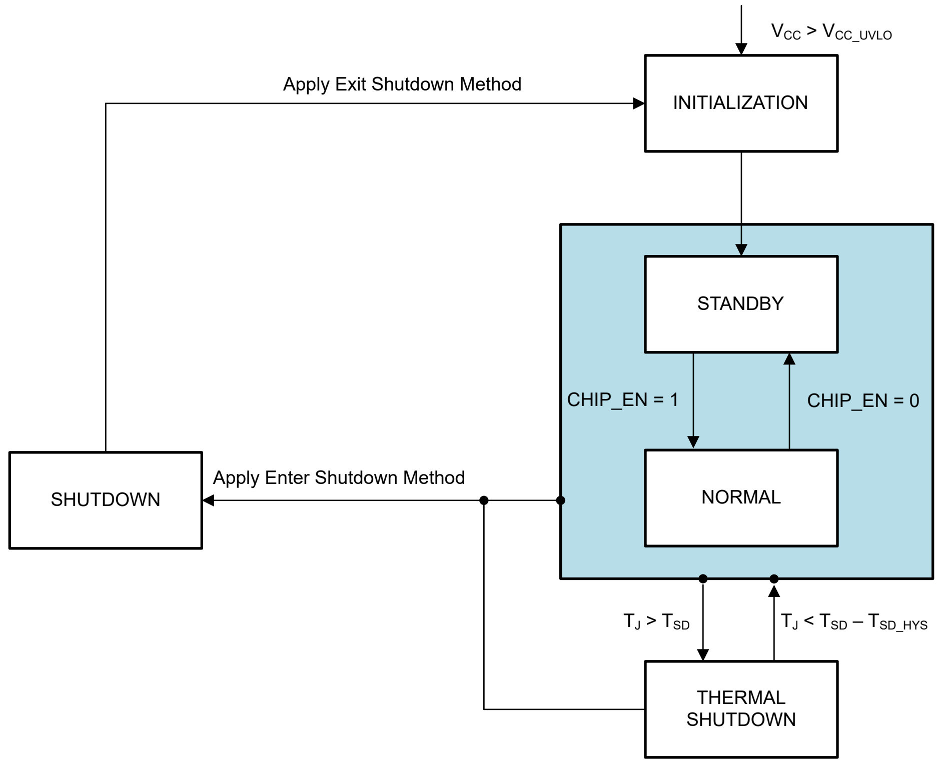



**Figure 7-9. Functional Modes**

#### *7.4.1 Initialization Mode*

The LP5814 enters INITIALIZATION mode when VCC voltage ramps above the $V_{CC\_UVLO}$ or exits from SHUTDOWN mode. The LP5814 reset all registers to default value in INITIALIZATION mode. The POR flag is set to 1 after exiting from INITIALIZATION mode to indicate the reset history.

#### *7.4.2 Standby and Normal Mode*

The LP5814 enters STANDBY mode when CHIP_EN = 0 or NORMAL mode when CHIP_EN = 1 after exiting from INITIALIZATION mode or THERMAL SHUTDOWN mode.

While staying in STANDBY or NORMAL mode,

- when Enter Shutdown Method is applied, the LP5814 enters SHUTDOWN mode. The Enter Shutdown Method is described in Shutdown Mode.
- when the junction temperature of the LP5814 rises above the thermal shutdown threshold $T_{SD}$, the LP5814 turns off all output channels and enters THERMAL SHUTDOWN mode.

#### *7.4.3 Shutdown Mode*

The LP5814 supports shutdown mode to minimize the power consumption from VCC. The quscient current from VCC decreases to 0.1 uA (typical) in SHUTDOWN mode. The LP5814 provides two pairs of methods to control the device enter and exit SHUTDOWN mode.

- Figure 7-10 shows the method 1
  - **Enter shutdown**, send Shutdown_command by writing 0x33 to register 0xD though $I^2C$ communication.
  - **Exit shutdown**, toggle SDA 8 times to generate 8 falling edges while keeping SCL as high. The supported maximum toggle frequency for SDA is 100kHz.

- Figure 7-11 shows the method 2
  - **Enter shutdown**, pull down SCL for 100ms while keeping SDA as high.
  - **Exit shutdown**, pull up SCL to generate one rising edge regardless of SDA state.

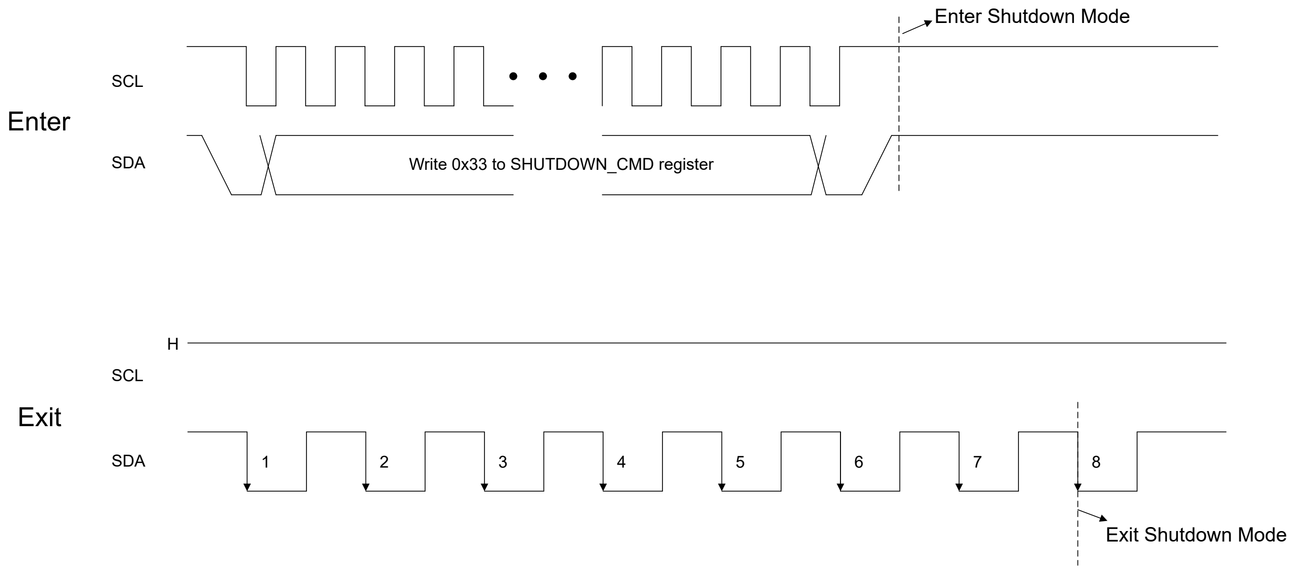



**Figure 7-10. Enter and Exit Shutdown Mode Method Pair 1**

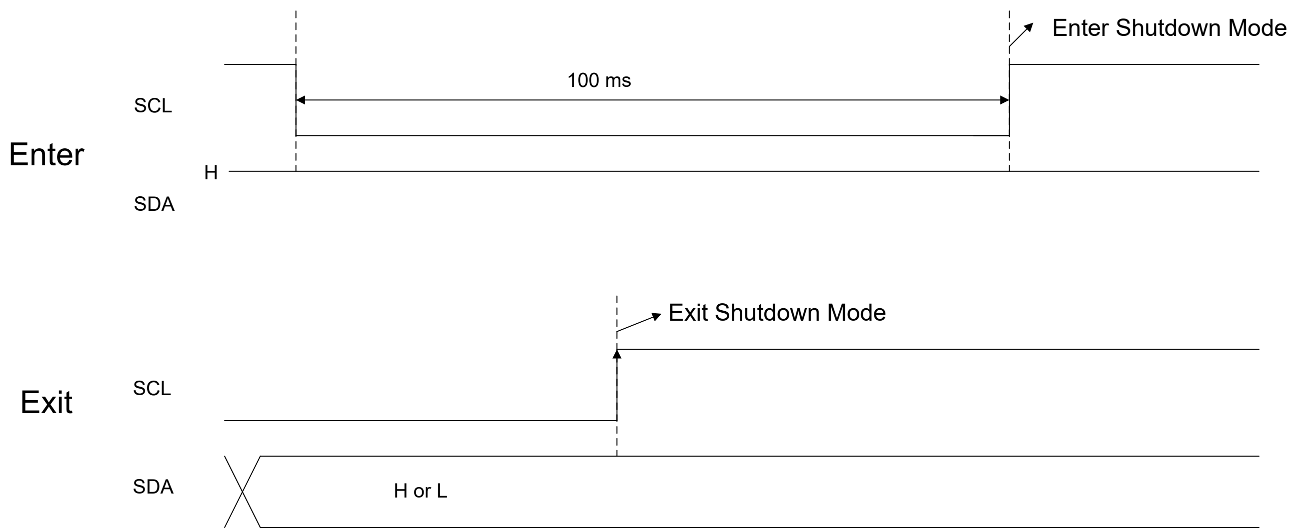



**Figure 7-11. Enter and Exit Shutdown Mode Method Pair 2**

### *7.4.4 Thermal Shutdown Mode*

All output channels are turned off while the LP5814 staying in THERMAL SHUTDOWN mode. The I2C interface is still active and the LP5814 enters SHUTDOWN mode when Enter Shutdown Method is applied.

When the junction temperature of LP5814 falles blow the thermal shutdown threshold, the LP5814 enters STANDBY mode when CHIP_EN = 0 or NORMAL mode when CHIP_EN = 1 after exiting from THERMAL SHUTDOWN mode. The TSD flag needs manual clear through setting TSD_CLR bit when CHIP_EN = 1.

## 7.5 Programming

The LP5814 is compatible with $I^2C$ standard specification. The device supports standard mode (100kHz maximum), fast mode (400kHz maximum) and fast plus mode (1MHz maximum). The device chip address is 0x2C.

### *7.5.1 $I^2C$ Data Tansactions*

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge after every byte rule. When the leader is the receiver, the receiver must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

### *7.5.2 $I^2C$ Data Format*

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 7 bits of the chip address and 1 read/write bit. The 8 bits of register address are put in Address Byte 2. The device supports both independent mode and broadcast mode. The auto-increment feature allows writing / reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

**Table 7-5. $I^2C$ Data Format**

| Address Byte1 | Chip Address | | | | | | | R/W |
|---|---|---|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Independent | 0 | 1 | 0 | 1 | 1 | 0 | 0 | R: 1 W: 0 |
| Broadcast | 0 | 1 | 1 | 0 | 1 | 0 | 0 | |
| Address Byte2 | Register Address | | | | | | | |
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | $7^{th}$ bit | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | 0 bit |

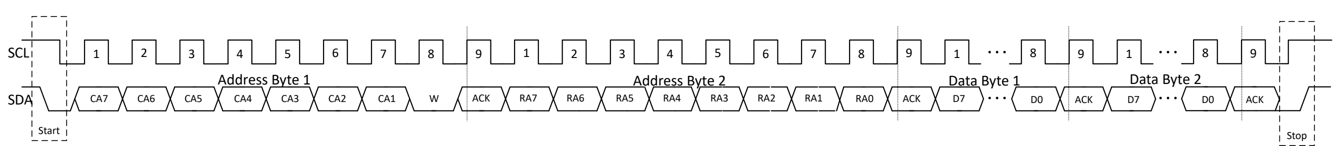



**Figure 7-12. $I^2C$ Write Timming**

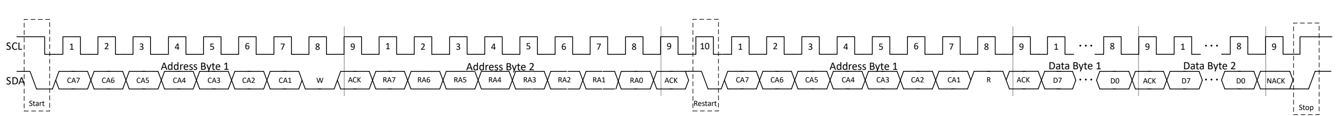



**Figure 7-13. $I^2C$ Read Timming**

### *7.5.3 Command Description*

The LP5814 has 5 dedicated software commands, Shutdown_command, Reset_command, Update_command, Start_command and Stop_command. Besides the 5 software commands, there is another PAUSE_CONTINUE bit used to control the execution of the autonomous animation.

- Send **Shutdown_command** is one of the 2 methods to make the device enter SHUTDOWN mode as described in Shutdown Mode .
- Send **Reset_command** to reset all registers to default value.
- Send **Update_command** to make the modified value in the device configuration registers as shown in Table 7-6 to take effect. The LP5814 responds to the Update_command only when CHIP_EN = 1.
- Send **Start_command** to start running the configured autonomous animation patterns on the outputs. The LP5814 responds to the Start_command only when CHIP_EN = 1.
- Send **Stop_command** to stop running the configured autonomous animation patterns on the outputs. The LP5814 responds to the Stop_command only when CHIP_EN = 1.
- Set **PAUSE_CONTINUE** bit as 1 to pause the running of the configured autonomous animation patterns on the outputs. Clear **PAUSE_CONTINUE** bit as 0 to continue the running of the previous paused autonomous animation patterns on the outputs. When the PAUSE_CONTINUE = 1, the configured autonomous animation pattern is not started after Start_command is sent.

**Table 7-6. Update_command Control Registers**

| Register Address | Register Acronym |
|---|---|
| 0x01 to 0x05 | DEV_CONGIF*x*, *x* = 0, 1, 2, 3, 4 |

## 7.6 Register Maps

**Table 7-7. Register Maps**

| Address | Acronym | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0h | CHIP_EN | RESERVED | | | | | | | CHIP_EN |
| 1h | DEV_CONFIG0 | RESERVED | | | | | | | MAX_CURRENT |
| 2h | DEV_CONFIG1 | RESERVED | | | | OUT3_EN | OUT2_EN | OUT1_EN | OUT0_EN |
| 3h | DEV_CONFIG2 | LED_FADE_TIME | | | | OUT3_FADE_EN | OUT2_FADE_EN | OUT1_FADE_EN | OUT0_FADE_EN |
| 4h | DEV_CONFIG3 | OUT3_EXP_EN | OUT2_EXP_EN | OUT1_EXP_EN | OUT0_EXP_EN | OUT3_AUTO_EN | OUT2_AUTO_EN | OUT1_AUTO_EN | OUT0_AUTO_EN |
| 5h | DEV_CONFIG4 | OUT3_ENGINE_CH | | OUT2_ENGINE_CH | | OUT1_ENGINE_CH | | OUT0_ENGINE_CH | |
| 6h | ENGINE_CONFIG0 | ENGINE0_ORDER3 | | ENGINE0_ORDER2 | | ENGINE0_ORDER1 | | ENGINE0_ORDER0 | |
| 7h | ENGINE_CONFIG1 | ENGINE1_ORDER3 | | ENGINE1_ORDER2 | | ENGINE1_ORDER1 | | ENGINE1_ORDER0 | |
| 8h | ENGINE_CONFIG2 | ENGINE2_ORDER3 | | ENGINE2_ORDER2 | | ENGINE2_ORDER1 | | ENGINE2_ORDER0 | |
| 9h | ENGINE_CONFIG3 | ENGINE3_ORDER3 | | ENGINE3_ORDER2 | | ENGINE3_ORDER1 | | ENGINE3_ORDER0 | |
| Ah | ENGINE_CONFIG4 | E1O3_EN | E1O2_EN | E1O1_EN | E1O0_EN | E0O3_EN | E0O2_EN | E0O1_EN | E0O0_EN |
| Bh | ENGINE_CONFIG5 | E3O3_EN | E3O2_EN | E3O1_EN | E3O0_EN | E2O3_EN | E2O2_EN | E2O1_EN | E2O0_EN |
| Ch | ENGINE_CONFIG6 | ENGINE3_REPT | | ENGINE2_REPT | | ENGINE1_REPT | | ENGINE0_REPT | |
| Dh | SHUTDOWN_CMD | SHUTDOWN | | | | | | | |
| Eh | RESET_CMD | RESET | | | | | | | |
| Fh | UPDATE_CMD | UPDATE | | | | | | | |
| 10h | START_CMD | START | | | | | | | |
| 11h | STOP_CMD | STOP | | | | | | | |
| 12h | PAUSE_CONTINUE | RESERVED | | | | | | | PAUSE_CONTINUE |
| 13h | FLAG_CLR | RESERVED | | | | | | TSD_CLR | POR_CLR |
| 14h | OUT0_DC | OUT0_DC | | | | | | | |
| 15h | OUT1_DC | OUT1_DC | | | | | | | |
| 16h | OUT2_DC | OUT2_DC | | | | | | | |
| 17h | OUT3_DC | OUT3_DC | | | | | | | |
| 18h | OUT0_MANUAL_PWM | OUT0_MANUAL_PWM | | | | | | | |
| 19h | OUT1_MANUAL_PWM | OUT1_MANUAL_PWM | | | | | | | |
| 1Ah | OUT2_MANUAL_PWM | OUT2_MANUAL_PWM | | | | | | | |
| 1Bh | OUT3_MANUAL_PWM | OUT3_MANUAL_PWM | | | | | | | |
| 1Ch | PATTERN0_PAUSE_TIME | PATTERN0_PAUSE_T0 | | | | PATTERN0_PAUSE_T1 | | | |
| 1Dh | PATTERN0_REPEAT_TIME | RESERVED | | | | PATTERN0_PT | | | |
| 1Eh | PATTERN0_PWM0 | PATTERN0_PWM0 | | | | | | | |
| 1Fh | PATTERN0_PWM1 | PATTERN0_PWM1 | | | | | | | |
| 20h | PATTERN0_PWM2 | PATTERN0_PWM2 | | | | | | | |
| 21h | PATTERN0_PWM3 | PATTERN0_PWM3 | | | | | | | |
| 22h | PATTERN0_PWM4 | PATTERN0_PWM4 | | | | | | | |
| 23h | PATTERN0_SLOPER_TIME1 | PATTERN0_SLOPER_T1 | | | | PATTERN0_SLOPER_T0 | | | |
| 24h | PATTERN0_SLOPER_TIME2 | PATTERN0_SLOPER_T3 | | | | PATTERN0_SLOPER_T2 | | | |
| 25h | PATTERN1_PAUSE_TIME | PATTERN1_PAUSE_T0 | | | | PATTERN1_PAUSE_T1 | | | |
| 26h | PATTERN1_REPEAT_TIME | RESERVED | | | | PATTERN1_PT | | | |
| 27h | PATTERN1_PWM0 | PATTERN1_PWM0 | | | | | | | |

**Table 7-7. Register Maps (continued)**

| Address | Acronym | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 28h | PATTERN1_PWM1 | PATTERN1_PWM1 | | | | | | | |
| 29h | PATTERN1_PWM2 | PATTERN1_PWM2 | | | | | | | |
| 2Ah | PATTERN1_PWM3 | PATTERN1_PWM3 | | | | | | | |
| 2Bh | PATTERN1_PWM4 | PATTERN1_PWM4 | | | | | | | |
| 2Ch | PATTERN1_SLOPER_TIME1 | PATTERN1_SLOPER_T1 | | | | PATTERN1_SLOPER_T0 | | | |
| 2Dh | PATTERN1_SLOPER_TIME2 | PATTERN1_SLOPER_T3 | | | | PATTERN1_SLOPER_T2 | | | |
| 2Eh | PATTERN2_PAUSE_TIME | PATTERN2_PAUSE_T0 | | | | PATTERN2_PAUSE_T1 | | | |
| 2Fh | PATTERN2_REPEAT_TIME | RESERVED | | | | PATTERN2_PT | | | |
| 30h | PATTERN2_PWM0 | PATTERN2_PWM0 | | | | | | | |
| 31h | PATTERN2_PWM1 | PATTERN2_PWM1 | | | | | | | |
| 32h | PATTERN2_PWM2 | PATTERN2_PWM2 | | | | | | | |
| 33h | PATTERN2_PWM3 | PATTERN2_PWM3 | | | | | | | |
| 34h | PATTERN2_PWM4 | PATTERN2_PWM4 | | | | | | | |
| 35h | PATTERN2_SLOPER_TIME1 | PATTERN2_SLOPER_T1 | | | | PATTERN2_SLOPER_T0 | | | |
| 36h | PATTERN2_SLOPER_TIME2 | PATTERN2_SLOPER_T3 | | | | PATTERN2_SLOPER_T2 | | | |
| 37h | PATTERN3_PAUSE_TIME | PATTERN3_PAUSE_T0 | | | | PATTERN3_PAUSE_T1 | | | |
| 38h | PATTERN3_REPEAT_TIME | RESERVED | | | | PATTERN3_PT | | | |
| 39h | PATTERN3_PWM0 | PATTERN3_PWM0 | | | | | | | |
| 3Ah | PATTERN3_PWM1 | PATTERN3_PWM1 | | | | | | | |
| 3Bh | PATTERN3_PWM2 | PATTERN3_PWM2 | | | | | | | |
| 3Ch | PATTERN3_PWM3 | PATTERN3_PWM3 | | | | | | | |
| 3Dh | PATTERN3_PWM4 | PATTERN3_PWM4 | | | | | | | |
| 3Eh | PATTERN3_SLOPER_TIME1 | PATTERN3_SLOPER_T1 | | | | PATTERN3_SLOPER_T0 | | | |
| 3Fh | PATTERN3_SLOPER_TIME2 | PATTERN3_SLOPER_T3 | | | | PATTERN3_SLOPER_T2 | | | |
| 40h | FLAG | RESERVED | OUT3_ENGINE_BUSY | OUT2_ENGINE_BUSY | OUT1_ENGINE_BUSY | OUT0_ENGINE_BUSY | ENGINE_BUSY | TSD | POR |

Complex bit access types are encoded to fit into small table cells. Table 7-8 shows the codes that are used for access types in this section.

**Table 7-8. Register Maps Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| W1C | W<br>1C | Write<br>1 to clear |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 7.6.1 CHIP_EN (Address = 0h) [Reset = 00h]

CHIP_EN is shown in Figure 7-14 and described in Table 7-9.

Return to the Summary Table.

**Figure 7-14. CHIP_EN**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | CHIP_EN |
| R-0h | | | | | | | R/W-0h |

**Table 7-9. CHIP_EN Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R | 0h | Reserved |
| 0 | CHIP_EN | R/W | 0h | Device enable.<br>0x0 = Disable<br>0x1 = Enable |

### 7.6.2 DEV_CONFIG0 (Address = 1h) [Reset = 00h]

DEV_CONFIG0 is shown in Figure 7-15 and described in Table 7-10.

Return to the Summary Table.

**Figure 7-15. DEV_CONFIG0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | MAX_CURRENT |
| R-0h | | | | | | | R/W-0h |

**Table 7-10. DEV_CONFIG0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R | 0h | Reserved |
| 0 | MAX_CURRENT | R/W | 0h | Max output current.<br>0x0 = 25.5mA<br>0x1 = 51mA |

### 7.6.3 DEV_CONFIG1 (Address = 2h) [Reset = 00h]

DEV_CONFIG1 is shown in Figure 7-16 and described in Table 7-11.

Return to the Summary Table.

**Figure 7-16. DEV_CONFIG1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | OUT3_EN | OUT2_EN | OUT1_EN | OUT0_EN |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7-11. DEV_CONFIG1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |
| 3 | OUT3_EN | R/W | 0h | OUT3 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 2 | OUT2_EN | R/W | 0h | OUT2 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 1 | OUT1_EN | R/W | 0h | OUT1 enable.<br>0x0 = Disable<br>0x1 = Enable |

**Table 7-11. DEV_CONFIG1 Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | OUT0_EN | R/W | 0h | OUT0 enable.<br>0x0 = Disable<br>0x1 = Enable |

### 7.6.4 DEV_CONFIG2 (Address = 3h) [Reset = 00h]

DEV_CONFIG2 is shown in Figure 7-17 and described in Table 7-12.

Return to the Summary Table.

**Figure 7-17. DEV_CONFIG2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LED_FADE_TIME | | | | OUT3_FADE_EN | OUT2_FADE_EN | OUT1_FADE_EN | OUT0_FADE_EN |
| R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7-12. DEV_CONFIG2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | LED_FADE_TIME | R/W | 0h | OUT fade sloper time.<br>0x0 = 0s<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3 | OUT3_FADE_EN | R/W | 0h | OUT3 fade in and out enable.<br>0x0 = Disable<br>0x1 = Enable |
| 2 | OUT2_FADE_EN | R/W | 0h | OUT2 fade in and out enable.<br>0x0 = Disable<br>0x1 = Enable |
| 1 | OUT1_FADE_EN | R/W | 0h | OUT1 fade in and out enable.<br>0x0 = Disable<br>0x1 = Enable |
| 0 | OUT0_FADE_EN | R/W | 0h | OUT0 fade in and out enable.<br>0x0 = Disable<br>0x1 = Enable |

### 7.6.5 DEV_CONFIG3 (Address = 4h) [Reset = 00h]

DEV_CONFIG3 is shown in Figure 7-18 and described in Table 7-13.

Return to the Summary Table.

**Figure 7-18. DEV_CONFIG3**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

**Figure 7-18. DEV_CONFIG3 (continued)**

| OUT3_EXP_EN | OUT2_EXP_EN | OUT1_EXP_EN | OUT0_EXP_EN | OUT3_AUTO_EN | OUT2_AUTO_EN | OUT1_AUTO_EN | OUT0_AUTO_EN |
|---|---|---|---|---|---|---|---|
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7-13. DEV_CONFIG3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | OUT3_EXP_EN | R/W | 0h | OUT3 exponential PWM dimming enable.<br>0x0 = Disable<br>0x1 = Enable |
| 6 | OUT2_EXP_EN | R/W | 0h | OUT2 exponential PWM dimming enable.<br>0x0 = Disable<br>0x1 = Enable |
| 5 | OUT1_EXP_EN | R/W | 0h | OUT1 exponential PWM dimming enable.<br>0x0 = Disable<br>0x1 = Enable |
| 4 | OUT0_EXP_EN | R/W | 0h | OUT0 exponential PWM dimming enable.<br>0x0 = Disable<br>0x1 = Enable |
| 3 | OUT3_AUTO_EN | R/W | 0h | OUT3 autonomous animation enable.<br>0x0 = Disable<br>0x1 = Enable |
| 2 | OUT2_AUTO_EN | R/W | 0h | OUT2 autonomous animation enable.<br>0x0 = Disable<br>0x1 = Enable |
| 1 | OUT1_AUTO_EN | R/W | 0h | OUT1 autonomous animation enable.<br>0x0 = Disable<br>0x1 = Enable |
| 0 | OUT0_AUTO_EN | R/W | 0h | OUT0 autonomous animation enable.<br>0x0 = Disable<br>0x1 = Enable |

### 7.6.6 DEV_CONFIG4 (Address = 5h) [Reset = 00h]

DEV_CONFIG4 is shown in Figure 7-19 and described in Table 7-14.

Return to the Summary Table.

**Figure 7-19. DEV_CONFIG4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT3_ENGINE_CH | | OUT2_ENGINE_CH | | OUT1_ENGINE_CH | | OUT0_ENGINE_CH | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 7-14. DEV_CONFIG4 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | OUT3_ENGINE_CH | R/W | 0h | OUT3 engine channel selection.<br>0x0 = ENGINE0 is selected<br>0x1 = ENGINE1 is selected<br>0x2 = ENGINE2 is selected<br>0x3 = ENGINE3 is selected |
| 5-4 | OUT2_ENGINE_CH | R/W | 0h | OUT2 engine channel selection.<br>0x0 = ENGINE0 is selected<br>0x1 = ENGINE1 is selected<br>0x2 = ENGINE2 is selected<br>0x3 = ENGINE3 is selected |

**Table 7-14. DEV_CONFIG4 Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-2 | OUT1_ENGINE_CH | R/W | 0h | OUT1 engine channel selection.<br>0x0 = ENGINE0 is selected<br>0x1 = ENGINE1 is selected<br>0x2 = ENGINE2 is selected<br>0x3 = ENGINE3 is selected |
| 1-0 | OUT0_ENGINE_CH | R/W | 0h | OUT0 engine channel selection.<br>0x0 = ENGINE0 is selected<br>0x1 = ENGINE1 is selected<br>0x2 = ENGINE2 is selected<br>0x3 = ENGINE3 is selected |

### 7.6.7 ENGINE_CONFIG0 (Address = 6h) [Reset = 00h]

ENGINE_CONFIG0 is shown in Figure 7-20 and described in Table 7-15.

Return to the Summary Table.

**Figure 7-20. ENGINE_CONFIG0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ENGINE0_ORDER3 | | ENGINE0_ORDER2 | | ENGINE0_ORDER1 | | ENGINE0_ORDER0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 7-15. ENGINE_CONFIG0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | ENGINE0_ORDER3 | R/W | 0h | ENGINE0_ORDER3 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 5-4 | ENGINE0_ORDER2 | R/W | 0h | ENGINE0_ORDER2 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 3-2 | ENGINE0_ORDER1 | R/W | 0h | ENGINE0_ORDER1 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 1-0 | ENGINE0_ORDER0 | R/W | 0h | ENGINE0_ORDER0 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |

### 7.6.8 ENGINE_CONFIG1 (Address = 7h) [Reset = 00h]

ENGINE_CONFIG1 is shown in Figure 7-21 and described in Table 7-16.

Return to the Summary Table.

**Figure 7-21. ENGINE_CONFIG1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ENGINE1_ORDER3 | | ENGINE1_ORDER2 | | ENGINE1_ORDER1 | | ENGINE1_ORDER0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 7-16. ENGINE_CONFIG1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | ENGINE1_ORDER3 | R/W | 0h | ENGINE1_ORDER3 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 5-4 | ENGINE1_ORDER2 | R/W | 0h | ENGINE1_ORDER2 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 3-2 | ENGINE1_ORDER1 | R/W | 0h | ENGINE1_ORDER1 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 1-0 | ENGINE1_ORDER0 | R/W | 0h | ENGINE1_ORDER0 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |

### 7.6.9 ENGINE_CONFIG2 (Address = 8h) [Reset = 00h]

ENGINE_CONFIG2 is shown in Figure 7-22 and described in Table 7-17.

Return to the Summary Table.

**Figure 7-22. ENGINE_CONFIG2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ENGINE2_ORDER3 | | ENGINE2_ORDER2 | | ENGINE2_ORDER1 | | ENGINE2_ORDER0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 7-17. ENGINE_CONFIG2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | ENGINE2_ORDER3 | R/W | 0h | ENGINE2_ORDER3 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 5-4 | ENGINE2_ORDER2 | R/W | 0h | ENGINE2_ORDER2 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 3-2 | ENGINE2_ORDER1 | R/W | 0h | ENGINE2_ORDER1 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 1-0 | ENGINE2_ORDER0 | R/W | 0h | ENGINE2_ORDER0 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |

### 7.6.10 ENGINE_CONFIG3 (Address = 9h) [Reset = 00h]

ENGINE_CONFIG3 is shown in Figure 7-23 and described in Table 7-18.

Return to the Summary Table.

**Figure 7-23. ENGINE_CONFIG3**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ENGINE3_ORDER3 | | ENGINE3_ORDER2 | | ENGINE3_ORDER1 | | ENGINE3_ORDER0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 7-18. ENGINE_CONFIG3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | ENGINE3_ORDER3 | R/W | 0h | ENGINE3_ORDER3 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 5-4 | ENGINE3_ORDER2 | R/W | 0h | ENGINE3_ORDER2 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 3-2 | ENGINE3_ORDER1 | R/W | 0h | ENGINE3_ORDER1 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |
| 1-0 | ENGINE3_ORDER0 | R/W | 0h | ENGINE3_ORDER0 pattern selection.<br>0x0 = PATTERN0 is selected<br>0x1 = PATTERN1 is selected<br>0x2 = PATTERN2 is selected<br>0x3 = PATTERN3 is selected |

### 7.6.11 ENGINE_CONFIG4 (Address = Ah) [Reset = 00h]

ENGINE_CONFIG4 is shown in Figure 7-24 and described in Table 7-19.

Return to the Summary Table.

**Figure 7-24. ENGINE_CONFIG4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| E1O3_EN | E1O2_EN | E1O1_EN | E1O0_EN | E0O3_EN | E0O2_EN | E0O1_EN | E0O0_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7-19. ENGINE_CONFIG4 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | E1O3_EN | R/W | 0h | ENGINE1_ORDER3 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 6 | E1O2_EN | R/W | 0h | ENGINE1_ORDER2 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 5 | E1O1_EN | R/W | 0h | ENGINE1_ORDER1 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 4 | E1O0_EN | R/W | 0h | ENGINE1_ORDER0 enable.<br>0x0 = Disable<br>0x1 = Enable |

**Table 7-19. ENGINE_CONFIG4 Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3 | E0O3_EN | R/W | 0h | ENGINE0_ORDER3 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 2 | E0O2_EN | R/W | 0h | ENGINE0_ORDER2 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 1 | E0O1_EN | R/W | 0h | ENGINE0_ORDER1 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 0 | E0O0_EN | R/W | 0h | ENGINE0_ORDER0 enable.<br>0x0 = Disable<br>0x1 = Enable |

### 7.6.12 ENGINE_CONFIG5 (Address = Bh) [Reset = 00h]

ENGINE_CONFIG5 is shown in Figure 7-25 and described in Table 7-20.

Return to the Summary Table.

**Figure 7-25. ENGINE_CONFIG5**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| E3O3_EN | E3O2_EN | E3O1_EN | E3O0_EN | E2O3_EN | E2O2_EN | E2O1_EN | E2O0_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7-20. ENGINE_CONFIG5 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | E3O3_EN | R/W | 0h | ENGINE3_ORDER3 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 6 | E3O2_EN | R/W | 0h | ENGINE3_ORDER2 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 5 | E3O1_EN | R/W | 0h | ENGINE3_ORDER1 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 4 | E3O0_EN | R/W | 0h | ENGINE3_ORDER0 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 3 | E2O3_EN | R/W | 0h | ENGINE2_ORDER3 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 2 | E2O2_EN | R/W | 0h | ENGINE2_ORDER2 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 1 | E2O1_EN | R/W | 0h | ENGINE2_ORDER1 enable.<br>0x0 = Disable<br>0x1 = Enable |
| 0 | E2O0_EN | R/W | 0h | ENGINE2_ORDER0 enable.<br>0x0 = Disable<br>0x1 = Enable |

### 7.6.13 ENGINE_CONFIG6 (Address = Ch) [Reset = 00h]

ENGINE_CONFIG6 is shown in Figure 7-26 and described in Table 7-21.

Return to the Summary Table.

**Figure 7-26. ENGINE_CONFIG6**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ENGINE3_REPT | | ENGINE2_REPT | | ENGINE1_REPT | | ENGINE0_REPT | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 7-21. ENGINE_CONFIG6 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | ENGINE3_REPT | R/W | 0h | ENGINE3 repeat times.<br>0x0 = 0 times<br>0x1 = 1 times<br>0x2 = 2 times<br>0x3 = infinite times |
| 5-4 | ENGINE2_REPT | R/W | 0h | ENGINE2 repeat times.<br>0x0 = 0 times<br>0x1 = 1 times<br>0x2 = 2 times<br>0x3 = infinite times |
| 3-2 | ENGINE1_REPT | R/W | 0h | ENGINE1 repeat times.<br>0x0 = 0 times<br>0x1 = 1 times<br>0x2 = 2 times<br>0x3 = infinite times |
| 1-0 | ENGINE0_REPT | R/W | 0h | ENGINE0 repeat times.<br>0x0 = 0 times<br>0x1 = 1 times<br>0x2 = 2 times<br>0x3 = infinite times |

### 7.6.14 SHUTDOWN_CMD (Address = Dh) [Reset = 00h]

SHUTDOWN_CMD is shown in Figure 7-27 and described in Table 7-22.

Return to the Summary Table.

**Figure 7-27. SHUTDOWN_CMD**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SHUTDOWN | | | | | | | |
| W-0h | | | | | | | |

**Table 7-22. SHUTDOWN_CMD Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | SHUTDOWN | W | 0h | 0x33 = Enter shutdown mode |

### 7.6.15 RESET_CMD (Address = Eh) [Reset = 00h]

RESET_CMD is shown in Figure 7-28 and described in Table 7-23.

Return to the Summary Table.

**Figure 7-28. RESET_CMD**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESET | | | | | | | |
| W-0h | | | | | | | |

**Table 7-23. RESET_CMD Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | RESET | W | 0h | 0xCC = Reset all the registers to default value |

### 7.6.16 UPDATE_CMD (Address = Fh) [Reset = 00h]

UPDATE_CMD is shown in Figure 7-29 and described in Table 7-24.

Return to the Summary Table.

**Figure 7-29. UPDATE_CMD**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| UPDATE | | | | | | | |
| W-0h | | | | | | | |

**Table 7-24. UPDATE_CMD Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | UPDATE | W | 0h | 0x55 = Update all device configuration registers value |

### 7.6.17 START_CMD (Address = 10h) [Reset = 00h]

START_CMD is shown in Figure 7-30 and described in Table 7-25.

Return to the Summary Table.

**Figure 7-30. START_CMD**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| START | | | | | | | |
| W-0h | | | | | | | |

**Table 7-25. START_CMD Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | START | W | 0h | 0xFF = Start autonomous animation |

### 7.6.18 STOP_CMD (Address = 11h) [Reset = 00h]

STOP_CMD is shown in Figure 7-31 and described in Table 7-26.

Return to the Summary Table.

**Figure 7-31. STOP_CMD**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STOP | | | | | | | |
| W-0h | | | | | | | |

**Table 7-26. STOP_CMD Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | STOP | W | 0h | 0xAA = Stop autonomous animation |

### 7.6.19 PAUSE_CONTINUE (Address = 12h) [Reset = 00h]

PAUSE_CONTINUE is shown in Figure 7-32 and described in Table 7-27.

Return to the Summary Table.

**Figure 7-32. PAUSE_CONTINUE**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | PAUSE_CONTINUE |
| R-0h | | | | | | | R/W-0h |

**Table 7-27. PAUSE_CONTINUE Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R | 0h | Reserved |
| 0 | PAUSE_CONTINUE | R/W | 0h | Pause or continue autonomous animation.<br>0x0 = Continue<br>0x1 = Pause |

### 7.6.20 FLAG_CLR (Address = 13h) [Reset = 00h]

FLAG_CLR is shown in Figure 7-33 and described in Table 7-28.

Return to the Summary Table.

**Figure 7-33. FLAG_CLR**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | TSD_CLR | POR_CLR |
| R-0h | | | | | | W1C-0h | W1C-0h |

**Table 7-28. FLAG_CLR Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED | R | 0h | Reserved |
| 1 | TSD_CLR | W1C | 0h | Write 1 to clear TSD flag. |
| 0 | POR_CLR | W1C | 0h | Write 1 to clear POR flag. |

### 7.6.21 OUT0_DC (Address = 14h) [Reset = 00h]

OUT0_DC is shown in Figure 7-34 and described in Table 7-29.

Return to the Summary Table.

**Figure 7-34. OUT0_DC**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT0_DC | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-29. OUT0_DC Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT0_DC | R/W | 0h | OUT0 DC setting. |

### 7.6.22 OUT1_DC (Address = 15h) [Reset = 00h]

OUT1_DC is shown in Figure 7-35 and described in Table 7-30.

Return to the Summary Table.

**Figure 7-35. OUT1_DC**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT1_DC | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-30. OUT1_DC Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT1_DC | R/W | 0h | OUT1 DC setting. |

### 7.6.23 OUT2_DC (Address = 16h) [Reset = 00h]

OUT2_DC is shown in Figure 7-36 and described in Table 7-31.

Return to the Summary Table.

**Figure 7-36. OUT2_DC**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT2_DC | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-31. OUT2_DC Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT2_DC | R/W | 0h | OUT2 DC setting. |

### 7.6.24 OUT3_DC (Address = 17h) [Reset = 00h]

OUT3_DC is shown in Figure 7-37 and described in Table 7-32.

Return to the Summary Table.

**Figure 7-37. OUT3_DC**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT3_DC | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-32. OUT3_DC Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT3_DC | R/W | 0h | OUT3 DC setting. |

### 7.6.25 OUT0_MANUAL_PWM (Address = 18h) [Reset = 00h]

OUT0_MANUAL_PWM is shown in Figure 7-38 and described in Table 7-33.

Return to the Summary Table.

**Figure 7-38. OUT0_MANUAL_PWM**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT0_MANUAL_PWM | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-33. OUT0_MANUAL_PWM Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT0_MANUAL_PWM | R/W | 0h | OUT0 manual PWM setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.26 OUT1_MANUAL_PWM (Address = 19h) [Reset = 00h]

OUT1_MANUAL_PWM is shown in Figure 7-39 and described in Table 7-34.

Return to the Summary Table.

**Figure 7-39. OUT1_MANUAL_PWM**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT1_MANUAL_PWM | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-34. OUT1_MANUAL_PWM Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT1_MANUAL_PWM | R/W | 0h | OUT1 manual PWM setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.27 OUT2_MANUAL_PWM (Address = 1Ah) [Reset = 00h]

OUT2_MANUAL_PWM is shown in Figure 7-40 and described in Table 7-35.

Return to the Summary Table.

**Figure 7-40. OUT2_MANUAL_PWM**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUT2_MANUAL_PWM | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-35. OUT2_MANUAL_PWM Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT2_MANUAL_PWM | R/W | 0h | OUT2 manual PWM setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.28 OUT3_MANUAL_PWM (Address = 1Bh) [Reset = 00h]

OUT3_MANUAL_PWM is shown in Figure 7-41 and described in Table 7-36.

Return to the Summary Table.

**Figure 7-41. OUT3_MANUAL_PWM**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

**Figure 7-41. OUT3_MANUAL_PWM (continued)**

| OUT3_MANUAL_PWM |
|---|
| R/W-0h |

**Table 7-36. OUT3_MANUAL_PWM Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUT3_MANUAL_PWM | R/W | 0h | OUT3 manual PWM setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.29 PATTERN0_PAUSE_TIME (Address = 1Ch) [Reset = 00h]

PATTERN0_PAUSE_TIME is shown in Figure 7-42 and described in Table 7-37.

Return to the Summary Table.

**Figure 7-42. PATTERN0_PAUSE_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_PAUSE_T0 | | | | PATTERN0_PAUSE_T1 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-37. PATTERN0_PAUSE_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN0_PAUSE_T0 | R/W | 0h | Start animation pause time of pattern0.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN0_PAUSE_T1 | R/W | 0h | End animation pause time of pattern0.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.30 PATTERN0_REPEAT_TIME (Address = 1Dh) [Reset = 00h]

PATTERN0_REPEAT_TIME is shown in Figure 7-43 and described in Table 7-38.

Return to the Summary Table.

**Figure 7-43. PATTERN0_REPEAT_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | PATTERN0_PT | | | |
| R-0h | | | | R/W-0h | | | |

**Table 7-38. PATTERN0_REPEAT_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |
| 3-0 | PATTERN0_PT | R/W | 0h | Pattern0 repeat times.<br>0x0 = 0 time<br>0x1 = 1 time<br>0x2 = 2 times<br>0x3 = 3 times<br>0x4 = 4 times<br>0x5 = 5 times<br>0x6 = 6 times<br>0x7 = 7 times<br>0x8 = 8 times<br>0x9 = 9 times<br>0xA = 10 times<br>0xB = 11 times<br>0xC = 12 times<br>0xD = 13 times<br>0xE = 14 times<br>0xF = infinite times |

### 7.6.31 PATTERN0_PWM0 (Address = 1Eh) [Reset = 00h]

PATTERN0_PWM0 is shown in Figure 7-44 and described in Table 7-39.

Return to the Summary Table.

**Figure 7-44. PATTERN0_PWM0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_PWM0 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-39. PATTERN0_PWM0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN0_PWM0 | R/W | 0h | Pattern0 PWM0 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.32 PATTERN0_PWM1 (Address = 1Fh) [Reset = 00h]

PATTERN0_PWM1 is shown in Figure 7-45 and described in Table 7-40.

Return to the Summary Table.

**Figure 7-45. PATTERN0_PWM1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_PWM1 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-40. PATTERN0_PWM1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN0_PWM1 | R/W | 0h | Pattern0 PWM1 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.33 PATTERN0_PWM2 (Address = 20h) [Reset = 00h]

PATTERN0_PWM2 is shown in Figure 7-46 and described in Table 7-41.

Return to the Summary Table.

**Figure 7-46. PATTERN0_PWM2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_PWM2 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-41. PATTERN0_PWM2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN0_PWM2 | R/W | 0h | Pattern0 PWM2 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.34 PATTERN0_PWM3 (Address = 21h) [Reset = 00h]

PATTERN0_PWM3 is shown in Figure 7-47 and described in Table 7-42.

Return to the Summary Table.

**Figure 7-47. PATTERN0_PWM3**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_PWM3 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-42. PATTERN0_PWM3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN0_PWM3 | R/W | 0h | Pattern0 PWM3 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.35 PATTERN0_PWM4 (Address = 22h) [Reset = 00h]

PATTERN0_PWM4 is shown in Figure 7-48 and described in Table 7-43.

Return to the Summary Table.

**Figure 7-48. PATTERN0_PWM4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_PWM4 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-43. PATTERN0_PWM4 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN0_PWM4 | R/W | 0h | Pattern0 PWM4 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.36 PATTERN0_SLOPER_TIME1 (Address = 23h) [Reset = 00h]

PATTERN0_SLOPER_TIME1 is shown in Figure 7-49 and described in Table 7-44.

Return to the Summary Table.

**Figure 7-49. PATTERN0_SLOPER_TIME1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_SLOPER_T1 | | | | PATTERN0_SLOPER_T0 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-44. PATTERN0_SLOPER_TIME1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN0_SLOPER_T1 | R/W | 0h | Pattern0 sloper time 1 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

**Table 7-44. PATTERN0_SLOPER_TIME1 Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | PATTERN0_SLOPER_T0 | R/W | 0h | Pattern0 sloper time 0 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.37 PATTERN0_SLOPER_TIME2 (Address = 24h) [Reset = 00h]

PATTERN0_SLOPER_TIME2 is shown in Figure 7-50 and described in Table 7-45.

Return to the Summary Table.

**Figure 7-50. PATTERN0_SLOPER_TIME2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN0_SLOPER_T3 | | | | PATTERN0_SLOPER_T2 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-45. PATTERN0_SLOPER_TIME2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN0_SLOPER_T3 | R/W | 0h | Pattern0 sloper time 3 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

**Table 7-45. PATTERN0_SLOPER_TIME2 Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | PATTERN0_SLOPER_T2 | R/W | 0h | Pattern0 sloper time 2 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.38 PATTERN1_PAUSE_TIME (Address = 25h) [Reset = 00h]

PATTERN1_PAUSE_TIME is shown in Figure 7-51 and described in Table 7-46.

Return to the Summary Table.

**Figure 7-51. PATTERN1_PAUSE_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN1_PAUSE_T0 | | | | PATTERN1_PAUSE_T1 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-46. PATTERN1_PAUSE_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN1_PAUSE_T0 | R/W | 0h | Start animation pause time of pattern1.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

**Table 7-46. PATTERN1_PAUSE_TIME Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | PATTERN1_PAUSE_T1 | R/W | 0h | End animation pause time of pattern1.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.39 PATTERN1_REPEAT_TIME (Address = 26h) [Reset = 00h]

PATTERN1_REPEAT_TIME is shown in Figure 7-52 and described in Table 7-47.

Return to the Summary Table.

**Figure 7-52. PATTERN1_REPEAT_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | PATTERN1_PT | | | |
| R-0h | | | | R/W-0h | | | |

**Table 7-47. PATTERN1_REPEAT_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |
| 3-0 | PATTERN1_PT | R/W | 0h | Pattern1 repeat times.<br>0x0 = 0 time<br>0x1 = 1 time<br>0x2 = 2 times<br>0x3 = 3 times<br>0x4 = 4 times<br>0x5 = 5 times<br>0x6 = 6 times<br>0x7 = 7 times<br>0x8 = 8 times<br>0x9 = 9 times<br>0xA = 10 times<br>0xB = 11 times<br>0xC = 12 times<br>0xD = 13 times<br>0xE = 14 times<br>0xF = infinite times |

### 7.6.40 PATTERN1_PWM0 (Address = 27h) [Reset = 00h]

PATTERN1_PWM0 is shown in Figure 7-53 and described in Table 7-48.

Return to the Summary Table.

**Figure 7-53. PATTERN1_PWM0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

**Figure 7-53. PATTERN1_PWM0 (continued)**

| |
|---|
| PATTERN1_PWM0 |
| R/W-0h |

**Table 7-48. PATTERN1_PWM0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN1_PWM0 | R/W | 0h | Pattern1 PWM0 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.41 PATTERN1_PWM1 (Address = 28h) [Reset = 00h]

PATTERN1_PWM1 is shown in Figure 7-54 and described in Table 7-49.

Return to the Summary Table.

**Figure 7-54. PATTERN1_PWM1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN1_PWM1 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-49. PATTERN1_PWM1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN1_PWM1 | R/W | 0h | Pattern1 PWM1 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.42 PATTERN1_PWM2 (Address = 29h) [Reset = 00h]

PATTERN1_PWM2 is shown in Figure 7-55 and described in Table 7-50.

Return to the Summary Table.

**Figure 7-55. PATTERN1_PWM2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN1_PWM2 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-50. PATTERN1_PWM2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN1_PWM2 | R/W | 0h | Pattern1 PWM2 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.43 PATTERN1_PWM3 (Address = 2Ah) [Reset = 00h]

PATTERN1_PWM3 is shown in Figure 7-56 and described in Table 7-51.

Return to the Summary Table.

**Figure 7-56. PATTERN1_PWM3**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN1_PWM3 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-51. PATTERN1_PWM3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN1_PWM3 | R/W | 0h | Pattern1 PWM3 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.44 PATTERN1_PWM4 (Address = 2Bh) [Reset = 00h]

PATTERN1_PWM4 is shown in Figure 7-57 and described in Table 7-52.

Return to the Summary Table.

**Figure 7-57. PATTERN1_PWM4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN1_PWM4 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-52. PATTERN1_PWM4 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN1_PWM4 | R/W | 0h | Pattern1 PWM4 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.45 PATTERN1_SLOPER_TIME1 (Address = 2Ch) [Reset = 00h]

PATTERN1_SLOPER_TIME1 is shown in Figure 7-58 and described in Table 7-53.

Return to the Summary Table.

**Figure 7-58. PATTERN1_SLOPER_TIME1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN1_SLOPER_T1 | | | | PATTERN1_SLOPER_T0 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-53. PATTERN1_SLOPER_TIME1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN1_SLOPER_T1 | R/W | 0h | Pattern1 sloper time 1 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN1_SLOPER_T0 | R/W | 0h | Pattern1 sloper time 0 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.46 PATTERN1_SLOPER_TIME2 (Address = 2Dh) [Reset = 00h]

PATTERN1_SLOPER_TIME2 is shown in Figure 7-59 and described in Table 7-54.

Return to the Summary Table.

**Figure 7-59. PATTERN1_SLOPER_TIME2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN1_SLOPER_T3 | | | | PATTERN1_SLOPER_T2 | | | |
| R/W-0h | | | | R/W-0h | | | |

### Table 7-54. PATTERN1_SLOPER_TIME2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN1_SLOPER_T3 | R/W | 0h | Pattern1 sloper time 3 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN1_SLOPER_T2 | R/W | 0h | Pattern1 sloper time 2 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.47 PATTERN2_PAUSE_TIME (Address = 2Eh) [Reset = 00h]

PATTERN2_PAUSE_TIME is shown in Figure 7-60 and described in Table 7-55.

Return to the Summary Table.

**Figure 7-60. PATTERN2_PAUSE_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN2_PAUSE_T0 | | | | PATTERN2_PAUSE_T1 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-55. PATTERN2_PAUSE_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN2_PAUSE_T0 | R/W | 0h | Start animation pause time of pattern2.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN2_PAUSE_T1 | R/W | 0h | End animation pause time of pattern2.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.48 PATTERN2_REPEAT_TIME (Address = 2Fh) [Reset = 00h]

PATTERN2_REPEAT_TIME is shown in Figure 7-61 and described in Table 7-56.

Return to the Summary Table.

**Figure 7-61. PATTERN2_REPEAT_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | PATTERN2_PT | | | |
| R-0h | | | | R/W-0h | | | |

**Table 7-56. PATTERN2_REPEAT_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |

**Table 7-56. PATTERN2_REPEAT_TIME Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | PATTERN2_PT | R/W | 0h | Pattern2 repeat times.<br>0x0 = 0 time<br>0x1 = 1 time<br>0x2 = 2 times<br>0x3 = 3 times<br>0x4 = 4 times<br>0x5 = 5 times<br>0x6 = 6 times<br>0x7 = 7 times<br>0x8 = 8 times<br>0x9 = 9 times<br>0xA = 10 times<br>0xB = 11 times<br>0xC = 12 times<br>0xD = 13 times<br>0xE = 14 times<br>0xF = infinite times |

### 7.6.49 PATTERN2_PWM0 (Address = 30h) [Reset = 00h]

PATTERN2_PWM0 is shown in Figure 7-62 and described in Table 7-57.

Return to the Summary Table.

**Figure 7-62. PATTERN2_PWM0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN2_PWM0 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-57. PATTERN2_PWM0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN2_PWM0 | R/W | 0h | Pattern2 PWM0 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.50 PATTERN2_PWM1 (Address = 31h) [Reset = 00h]

PATTERN2_PWM1 is shown in Figure 7-63 and described in Table 7-58.

Return to the Summary Table.

**Figure 7-63. PATTERN2_PWM1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN2_PWM1 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-58. PATTERN2_PWM1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN2_PWM1 | R/W | 0h | Pattern2 PWM1 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.51 PATTERN2_PWM2 (Address = 32h) [Reset = 00h]

PATTERN2_PWM2 is shown in Figure 7-64 and described in Table 7-59.

Return to the Summary Table.

**Figure 7-64. PATTERN2_PWM2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN2_PWM2 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-59. PATTERN2_PWM2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN2_PWM2 | R/W | 0h | Pattern2 PWM2 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.52 PATTERN2_PWM3 (Address = 33h) [Reset = 00h]

PATTERN2_PWM3 is shown in Figure 7-65 and described in Table 7-60.

Return to the Summary Table.

**Figure 7-65. PATTERN2_PWM3**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN2_PWM3 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-60. PATTERN2_PWM3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN2_PWM3 | R/W | 0h | Pattern2 PWM3 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.53 PATTERN2_PWM4 (Address = 34h) [Reset = 00h]

PATTERN2_PWM4 is shown in Figure 7-66 and described in Table 7-61.

Return to the Summary Table.

**Figure 7-66. PATTERN2_PWM4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

**Figure 7-66. PATTERN2_PWM4 (continued)**

| PATTERN2_PWM4 |
|---|
| R/W-0h |

**Table 7-61. PATTERN2_PWM4 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN2_PWM4 | R/W | 0h | Pattern2 PWM4 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.54 PATTERN2_SLOPER_TIME1 (Address = 35h) [Reset = 00h]

PATTERN2_SLOPER_TIME1 is shown in Figure 7-67 and described in Table 7-62.

Return to the Summary Table.

**Figure 7-67. PATTERN2_SLOPER_TIME1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN2_SLOPER_T1 | | | | PATTERN2_SLOPER_T0 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-62. PATTERN2_SLOPER_TIME1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN2_SLOPER_T1 | R/W | 0h | Pattern2 sloper time 1 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN2_SLOPER_T0 | R/W | 0h | Pattern2 sloper time 0 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.55 PATTERN2_SLOPER_TIME2 (Address = 36h) [Reset = 00h]

PATTERN2_SLOPER_TIME2 is shown in Figure 7-68 and described in Table 7-63.

Return to the Summary Table.

**Figure 7-68. PATTERN2_SLOPER_TIME2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN2_SLOPER_T3 | | | | PATTERN2_SLOPER_T2 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-63. PATTERN2_SLOPER_TIME2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN2_SLOPER_T3 | R/W | 0h | Pattern2 sloper time 3 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN2_SLOPER_T2 | R/W | 0h | Pattern2 sloper time 2 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.56 PATTERN3_PAUSE_TIME (Address = 37h) [Reset = 00h]

PATTERN3_PAUSE_TIME is shown in Figure 7-69 and described in Table 7-64.

Return to the Summary Table.

**Figure 7-69. PATTERN3_PAUSE_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN3_PAUSE_T0 | | | | PATTERN3_PAUSE_T1 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-64. PATTERN3_PAUSE_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN3_PAUSE_T0 | R/W | 0h | Start animation pause time of pattern3.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN3_PAUSE_T1 | R/W | 0h | End animation pause time of pattern3.<br>0x0 = no pause time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.57 PATTERN3_REPEAT_TIME (Address = 38h) [Reset = 00h]

PATTERN3_REPEAT_TIME is shown in Figure 7-70 and described in Table 7-65.

Return to the Summary Table.

**Figure 7-70. PATTERN3_REPEAT_TIME**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | PATTERN3_PT | | | |
| R-0h | | | | R/W-0h | | | |

**Table 7-65. PATTERN3_REPEAT_TIME Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |

**Table 7-65. PATTERN3_REPEAT_TIME Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | PATTERN3_PT | R/W | 0h | Pattern3 repeat times.<br>0x0 = 0 time<br>0x1 = 1 time<br>0x2 = 2 times<br>0x3 = 3 times<br>0x4 = 4 times<br>0x5 = 5 times<br>0x6 = 6 times<br>0x7 = 7 times<br>0x8 = 8 times<br>0x9 = 9 times<br>0xA = 10 times<br>0xB = 11 times<br>0xC = 12 times<br>0xD = 13 times<br>0xE = 14 times<br>0xF = infinite times |

### 7.6.58 PATTERN3_PWM0 (Address = 39h) [Reset = 00h]

PATTERN3_PWM0 is shown in Figure 7-71 and described in Table 7-66.

Return to the Summary Table.

**Figure 7-71. PATTERN3_PWM0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN3_PWM0 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-66. PATTERN3_PWM0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN3_PWM0 | R/W | 0h | Pattern3 PWM0 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.59 PATTERN3_PWM1 (Address = 3Ah) [Reset = 00h]

PATTERN3_PWM1 is shown in Figure 7-72 and described in Table 7-67.

Return to the Summary Table.

**Figure 7-72. PATTERN3_PWM1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN3_PWM1 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-67. PATTERN3_PWM1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN3_PWM1 | R/W | 0h | Pattern3 PWM1 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.60 PATTERN3_PWM2 (Address = 3Bh) [Reset = 00h]

PATTERN3_PWM2 is shown in Figure 7-73 and described in Table 7-68.

Return to the Summary Table.

**Figure 7-73. PATTERN3_PWM2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN3_PWM2 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-68. PATTERN3_PWM2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN3_PWM2 | R/W | 0h | Pattern3 PWM2 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.61 PATTERN3_PWM3 (Address = 3Ch) [Reset = 00h]

PATTERN3_PWM3 is shown in Figure 7-74 and described in Table 7-69.

Return to the Summary Table.

**Figure 7-74. PATTERN3_PWM3**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN3_PWM3 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 7-69. PATTERN3_PWM3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN3_PWM3 | R/W | 0h | Pattern3 PWM3 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.62 PATTERN3_PWM4 (Address = 3Dh) [Reset = 00h]

PATTERN3_PWM4 is shown in Figure 7-75 and described in Table 7-70.

Return to the Summary Table.

**Figure 7-75. PATTERN3_PWM4**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

**Figure 7-75. PATTERN3_PWM4 (continued)**

| |
|---|
| PATTERN3_PWM4 |
| R/W-0h |

**Table 7-70. PATTERN3_PWM4 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PATTERN3_PWM4 | R/W | 0h | Pattern3 PWM4 setting.<br>0x00 = 0%<br>...<br>0x80 = 50%<br>...<br>0xFF = 100% |

### 7.6.63 PATTERN3_SLOPER_TIME1 (Address = 3Eh) [Reset = 00h]

PATTERN3_SLOPER_TIME1 is shown in Figure 7-76 and described in Table 7-71.

Return to the Summary Table.

**Figure 7-76. PATTERN3_SLOPER_TIME1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN3_SLOPER_T1 | | | | PATTERN3_SLOPER_T0 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-71. PATTERN3_SLOPER_TIME1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN3_SLOPER_T1 | R/W | 0h | Pattern3 sloper time 1 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN3_SLOPER_T0 | R/W | 0h | Pattern3 sloper time 0 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.64 PATTERN3_SLOPER_TIME2 (Address = 3Fh) [Reset = 00h]

PATTERN3_SLOPER_TIME2 is shown in Figure 7-77 and described in Table 7-72.

Return to the Summary Table.

**Figure 7-77. PATTERN3_SLOPER_TIME2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PATTERN3_SLOPER_T3 | | | | PATTERN3_SLOPER_T2 | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 7-72. PATTERN3_SLOPER_TIME2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PATTERN3_SLOPER_T3 | R/W | 0h | Pattern3 sloper time 3 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |
| 3-0 | PATTERN3_SLOPER_T2 | R/W | 0h | Pattern3 sloper time 2 setting.<br>0x0 = no sloper time<br>0x1 = 0.05s<br>0x2 = 0.10s<br>0x3 = 0.15s<br>0x4 = 0.20s<br>0x5 = 0.25s<br>0x6 = 0.30s<br>0x7 = 0.35s<br>0x8 = 0.40s<br>0x9 = 0.45s<br>0xA = 0.50s<br>0xB = 1.00s<br>0xC = 2.00s<br>0xD = 4.00s<br>0xE = 6.00s<br>0xF = 8.00s |

### 7.6.65 FLAG (Address = 40h) [Reset = 00h]

FLAG is shown in Figure 7-78 and described in Table 7-73.

Return to the Summary Table.

**Figure 7-78. FLAG**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | OUT3_ENGINE_BUSY | OUT2_ENGINE_BUSY | OUT1_ENGINE_BUSY | OUT0_ENGINE_BUSY | ENGINE_BUSY | TSD | POR |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

**Table 7-73. FLAG Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6 | OUT3_ENGINE_BUSY | R | 0h | Engine selected by OUT3 busy flag.<br>0x0 = The selected Engine is not running<br>0x1 = The selected Engine is running |
| 5 | OUT2_ENGINE_BUSY | R | 0h | Engine selected by OUT2 busy flag.<br>0x0 = The selected Engine is not running<br>0x1 = The selected Engine is running |
| 4 | OUT1_ENGINE_BUSY | R | 0h | Engine selected by OUT1 busy flag<br>0x0 = The selected Engine is not running<br>0x1 = The selected Engine is running |
| 3 | OUT0_ENGINE_BUSY | R | 0h | Engine selected by OUT0 busy flag.<br>0x0 = The selected Engine is not running<br>0x1 = The selected Engine is running |
| 2 | ENGINE_BUSY | R | 0h | Engine busy flag.<br>0x0 = All 4 engines are not running<br>0x1 = At leaset 1 engine is running |
| 1 | TSD | R | 0h | TSD flag.<br>0x0 = TSD is not triggered<br>0x1 = TSD is triggered |
| 0 | POR | R | 0h | POR flag.<br>0x0 = POR is not triggered<br>0x1 = POR is triggered |

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The LP5814 is a 4 channel RGBW LED driver with autonomous animation control. The device has ultra-low operation current at active mode and only consumes 0.25mA when LED current is set at 25mA. In battery powered applications like e-tag, ear bud, e-cigarettes, VR headset, RGB mouse, smart speaker, and other hand-held devices, LP5814 can provide premium LED lighting effects with low power consumption and small package.

## 8.2 Typical Application

### *8.2.1 Application*

Figure 8-1 shows an example of typical application, which uses one LP5814 to drive RGBW LEDs through $I^2C$ communication.

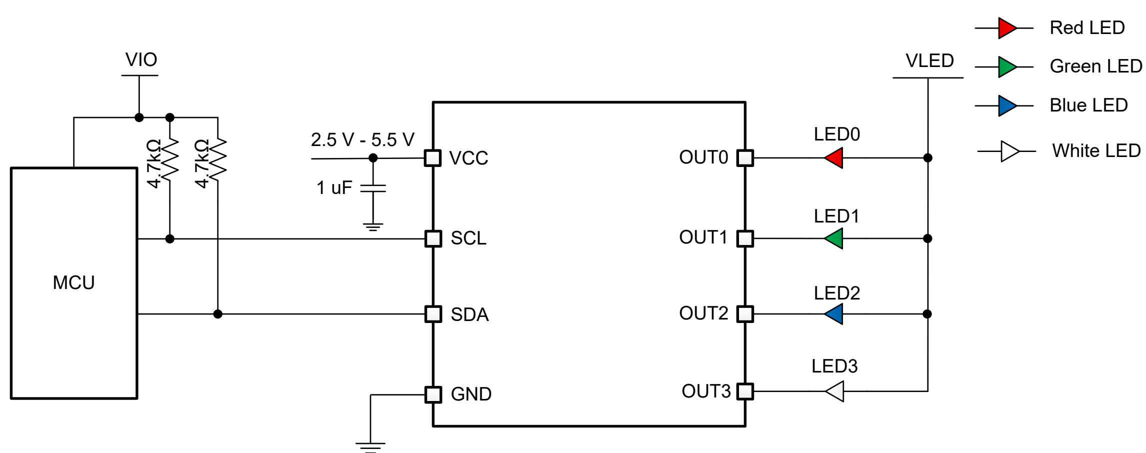



**Figure 8-1. Typical Application - LP5814 Driving RGBW LEDs**

### 8.2.2 Design Parameters

Design Parameters shows the typical design parameters of Application.

**Table 8-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage | 3.6V to 4.2V by one Li-on battery cell |
| RGBW LED count | 1 |
| LED maximum average current (red, green, blue, white) | 51mA, 40.8mA, 40.8mA, 40.8mA |
| LED PWM frequency | 23kHz |
| Red LED Mode | Manual Mode, Contsant ON with 50% PWM Duty Cycle |
| Green LED Mode | Animation Mode, Blinking with 5Hz Frequency |
| Blue LED Mode | Animation Mode, Breathing with 1s Exponential Ramping Up and 1s Exponential Ramping Down |
| White LED Mode | Animation Mode, Blinking with 1Hz Frequency |

### 8.2.3 Detailed Design Procedure

This section showcases the detailed design procedures for LP5814 including components selection, program procedure and examples.

#### 8.2.3.1 Program Procedure

After VCC powering up, the device is enabled by setting CHIP_EN = 1. Set the maximum current for each output. Then set the device configuration registers to enbale the output, select the dimming control mode for each output, and select the animation engine for the output in autonomous animation mode. Finally, Send UPDATE_CMD to make the prior configuration settings take effect.

For the output channel that is configured in manual mode, the output PWM changes immediately when the corresponding manual PWM register value is set.

For the output channel that is configured in autonomous animation mode, firstly, select animation engine for output. Secondly, construct the animation engine by setting the engine configure registers to select the animation pattern to map to the engine order and enable or disable the engine order. Then, build the animation patterns as required by setting pattern unit paramters. Finally, send START_CMD to initiate the autonomous animation.

The detailed program procedure is illustrated in Figure 8-2.

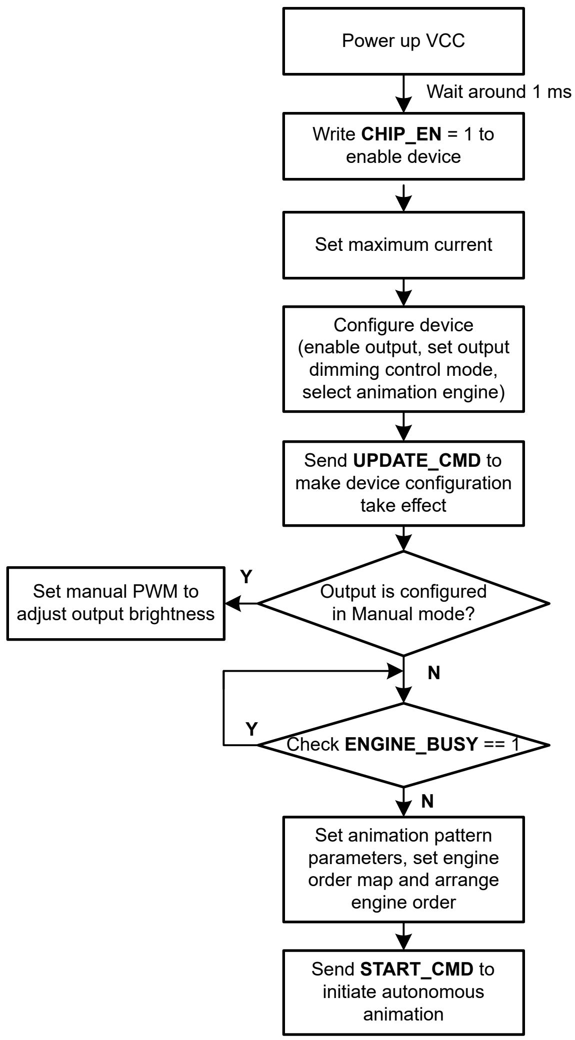



**Figure 8-2. Program Procedure**

#### 8.2.3.2 Programming Example

To get the design parameters in Section 8.2.2, the following program steps can be referred.

After VCC powering up and wait around 1ms,

1. Set CHIP_EN = 1 to enable the device(**Write 01h to register 00h**)
2. Set MAX_CURRENT = 1h to set 51mA maximum output LED current (**Write 01h to register 01h**)
3. Set 51mA maximum current for red LEDs, 40.8mA maximum current for green, blue and white LEDs (**Write FFh to registers 14h, write CCh to registers 15h, 16h and 17h**)
4. Enable all 4 LEDs (**Write 0Fh to register 02h**)
5. Set red LED in manual mode, set green, blue and white LEDs in autonomous animation mode, and enable blue LED exponential PWM dimming (**Write 4Eh to register 04h**)
6. Select ENGINE0 for green LED, ENGINE1 for blue LED and ENGINE2 for white LED (**Write 90h to register 05h**)
7. Send **UPDATE_CMD** to make above step2, step4, step5 and step6 configurations take effect (**Write 55h to register 0Fh**)
8. Set red LED PWM duty cycle as 50% (**Write 80h to register 18h**)

   **After this step, the read LED is turned on.**
9. Check **ENGINE_BUSY** flag by reading the FLAG register (**Read register 40h**)
   - If **ENGINE_BUSY = 1**, send **STOP_CMD** to clear ENGINE_BUSY flag as showed in Internal Engine Busy Status (**Write AAh to register 11h**), then move to next step.
   - If **ENGINE_BUSY = 0**, move to next step directly.
10. Select PATTERN0 for ENGINE0_ORDER0, PATTERN1 for ENGINE1_ORDER0 and PATTERN2 for ENGINE2_ORDER0 (**Write 00h to register 06h, write 01h to register 07h, write 02h to register 08h**)
11. Enable ENGINE0_ORDER0, ENGINE1_ORDER0 and ENGINE2_ORDER0 (**Write 11h to register 0Ah, write 01h to register 0Bh**)
12. Set PATTERN0 parameters as showed in Table 8-2 to realize 5Hz blinking effect on green LED, set PATTERN1 parameters as showed in Table 8-3 to realize breathing effect on blue LED and set PATTERN2 parameters as showed in Table 8-4 to realize 1Hz blinking effect on white LED.
13. Send **START_CMD** to intiate the animation (**Write FFh to register 10h**)

After this step, the red LED keeps constant ON, the green LED keeps blinking with 5Hz frequency and blue LED keeps breathing in 2.4s period and white LED keeps blinking with 1Hz frequency.

**Table 8-2. PATTERN0 5Hz Blinking Register Setting**

| Address | Register | Set Value | Description |
|---|---|---|---|
| 1Ch | PATTERN0_PAUSE_TIME | 00h | No pause time |
| 1Dh | PATTERN0_REPEAT_TIME | 0Fh | Infinite repeat times |
| 1Eh | PATTERN0_PWM0 | FFh | PATTERN0_PWM0 = FFh |
| 1Fh | PATTERN0_PWM1 | FFh | PATTERN0_PWM1 = FFh |
| 20h | PATTERN0_PWM2 | 00h | PATTERN0_PWM2 = 0 |
| 21h | PATTERN0_PWM3 | 00h | PATTERN0_PWM3 = 0 |
| 22h | PATTERN0_PWM4 | 00h | PATTERN0_PWM4 = 0 |
| 23h | PATTERN0_SLOPER_TIME1 | 02h | PATTERN0_SLOPER_T1 = 0, PATTERN0_SLOPER_T0 = 0.1s |
| 24h | PATTERN0_SLOPER_TIME2 | 02h | PATTERN0_SLOPER_T3 = 0, PATTERN0_SLOPER_T2 = 0.1s |

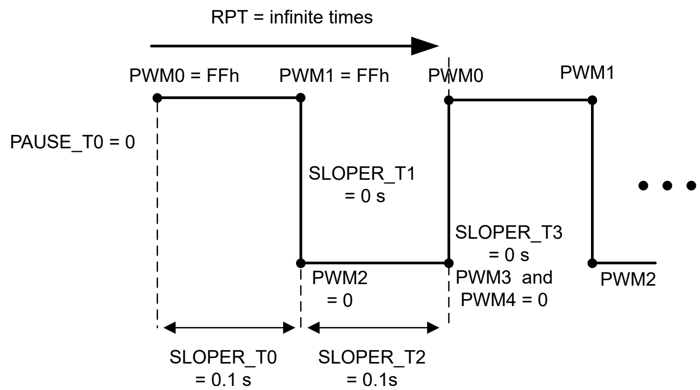



**Figure 8-3. PATTERN0 5Hz Blinking Example**

**Table 8-3. PATTERN1 Breathing Register Setting**

| Address | Register | Set Value | Description |
|---|---|---|---|
| 25h | PATTERN1_PAUSE_TIME | 00h | No pause time |
| 26h | PATTERN1_REPEAT_TIME | 0Fh | Infinite repeat times |
| 27h | PATTERN1_PWM0 | 00h | PATTERN1_PWM0 = 0 |
| 28h | PATTERN1_PWM1 | FFh | PATTERN1_PWM1 = FFh |
| 29h | PATTERN1_PWM2 | FFh | PATTERN1_PWM2 = FFh |
| 2Ah | PATTERN1_PWM3 | 00h | PATTERN1_PWM3 = 0 |
| 2Bh | PATTERN1_PWM4 | 00h | PATTERN1_PWM4 = 0 |
| 2Ch | PATTERN1_SLOPER_TIME1 | 4Bh | PATTERN1_SLOPER_T1 = 0.2s, PATTERN1_SLOPER_T0 = 1s |
| 2Dh | PATTERN1_SLOPER_TIME2 | 4Bh | PATTERN1_SLOPER_T3 = 0.2s, PATTERN1_SLOPER_T2 = 1s |

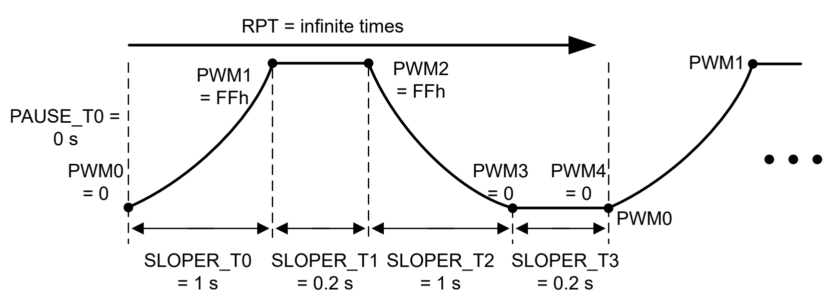



**Figure 8-4. PATTERN1 Breathing Example**

**Table 8-4. PATTERN2 1Hz Blinking Register Setting**

| Address | Register | Set Value | Description |
|---|---|---|---|
| 2Eh | PATTERN2_PAUSE_TIME | 00h | No pause time |
| 2Fh | PATTERN2_REPEAT_TIME | 0Fh | Infinite repeat times |
| 30h | PATTERN2_PWM0 | 80h | PATTERN2_PWM0 = FFh |
| 31h | PATTERN2_PWM1 | 80h | PATTERN2_PWM1 = FFh |

**Table 8-4. PATTERN2 1Hz Blinking Register Setting (continued)**

| Address | Register | Set Value | Description |
|---|---|---|---|
| 32h | PATTERN2_PWM2 | 00h | PATTERN2_PWM2 = 0 |
| 33h | PATTERN2_PWM3 | 00h | PATTERN2_PWM3 = 0 |
| 34h | PATTERN2_PWM4 | 00h | PATTERN2_PWM4 = 0 |
| 35h | PATTERN2_SLOPER_TIME1 | 0Ah | PATTERN2_SLOPER_T1 = 0, PATTERN2_SLOPER_T0 = 0.5s |
| 36h | PATTERN2_SLOPER_TIME2 | 0Ah | PATTERN2_SLOPER_T3 = 0, PATTERN2_SLOPER_T2 = 0.5s |

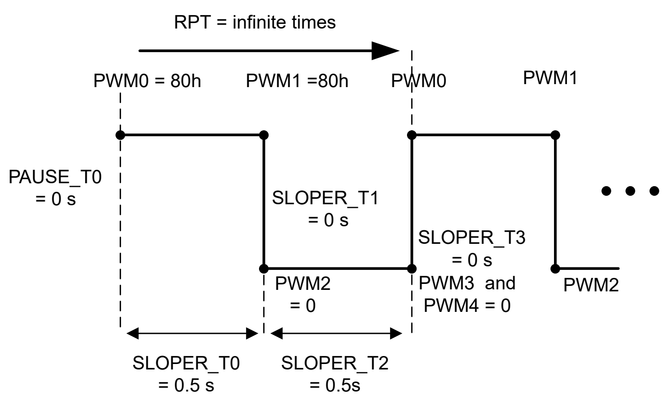
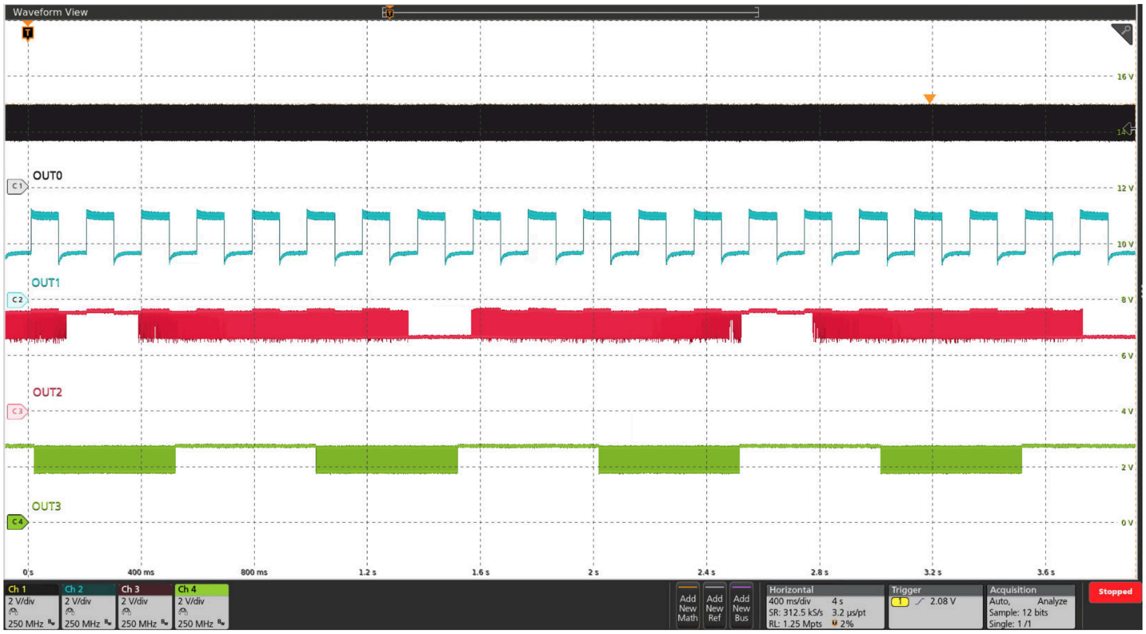



**Figure 8-5. PATTERN2 1Hz Blinking Example**

### 8.2.4 Application Performance Plots

The following figures show the application performance plots.




| | |
|---|---|
| OUT0 | Manual Mode, Contsant ON with 50% PWM Duty Cycle |
| OUT1 | Animation Mode, Blinking with 5Hz Frequency |
| OUT2 | Animation Mode, Breathing with 1s Exponential Ramping Up and 1s Ramping Down |
| OUT3 | Animation Mode, Blinking with 1Hz Frequency |

**Figure 8-6. Current Sinks Waveforms of OUT0, OUT1, OUT2, OUT3**

## 8.3 Power Supply Recommendations

The LP5814 is designed to operate from an input voltage supply range from 2.5V to 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance is required close to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100μF.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

The input capacitor needs not only to be close to the VCC pin, but also to the GND pin to reduce input supply ripple. For OUTx (x = 0, 1, 2, 3), low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of adjecent outputs must be short and wide and avoid parallel wiring and narrow trace. For better thermal performance, TI suggest to make copper polygon connected with each pin bigger.

### *8.4.2 Layout Example*

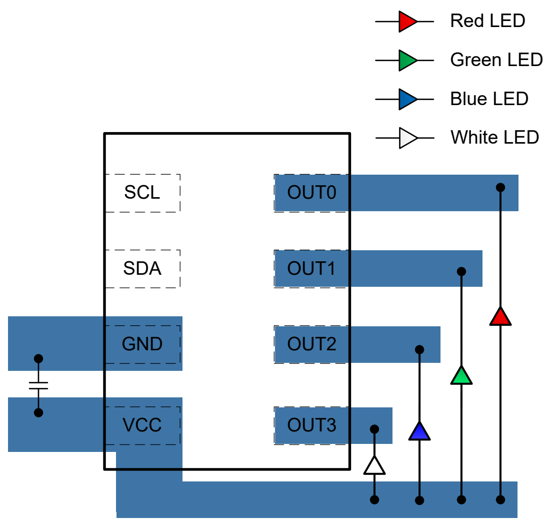



**Figure 8-7. LP5814 DRL Package Layout Example**

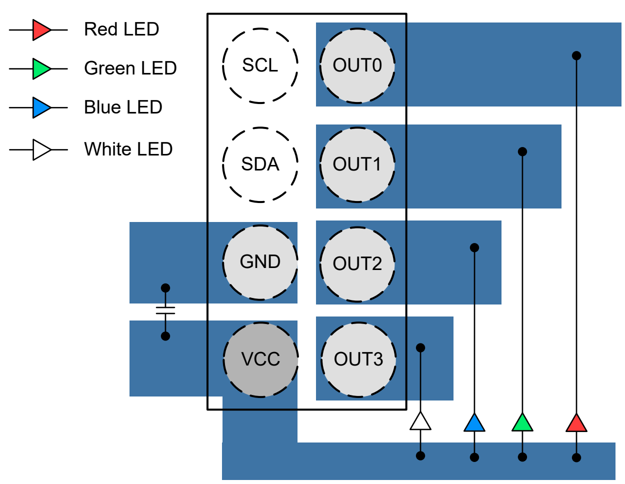



**Figure 8-8. LP5814 YCH Package Layout Example**

# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

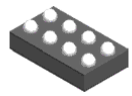
# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| March 2025 | * | Initial Release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

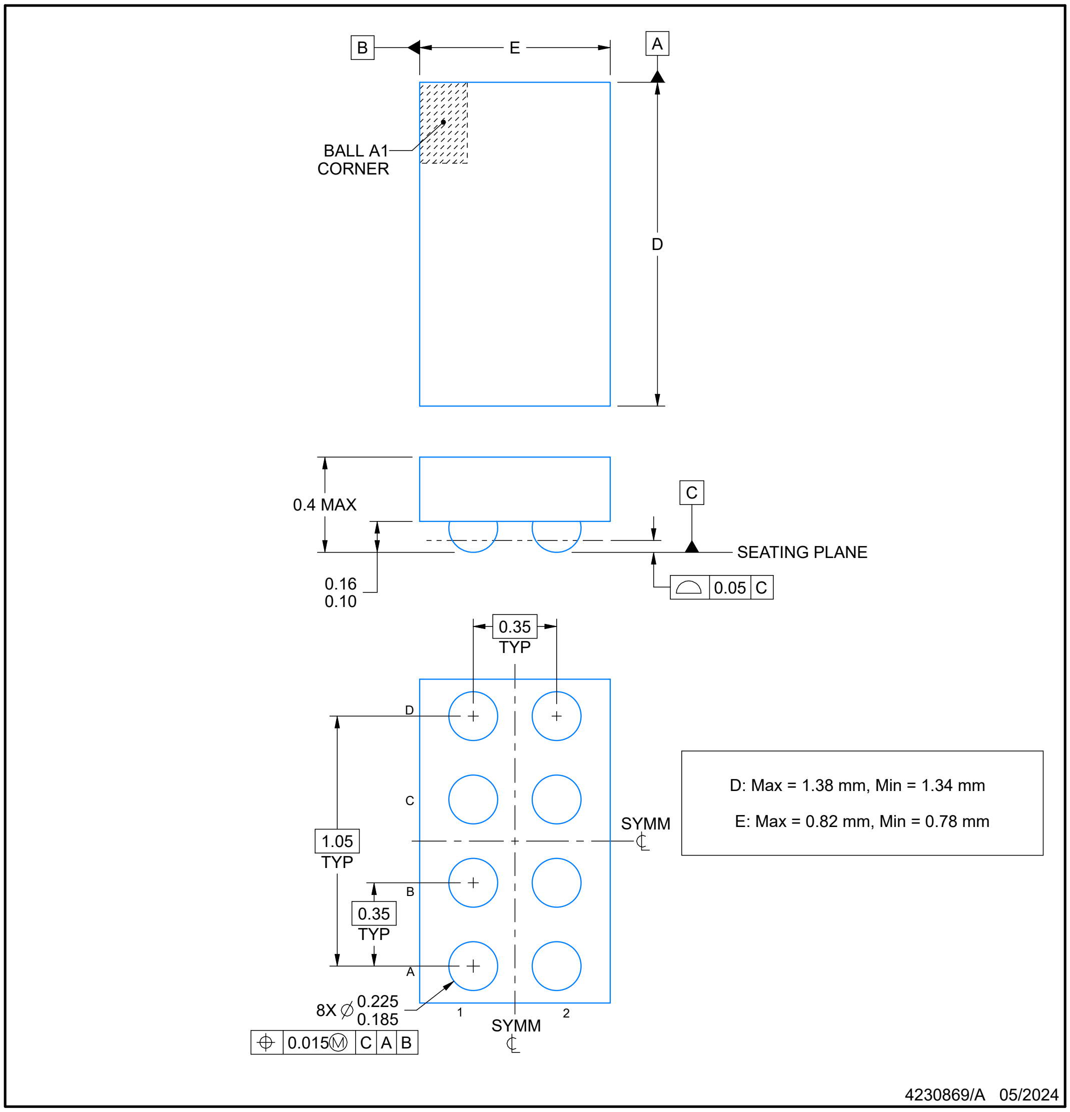


# PACKAGE OUTLINE

## YCH0008-C02

**DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



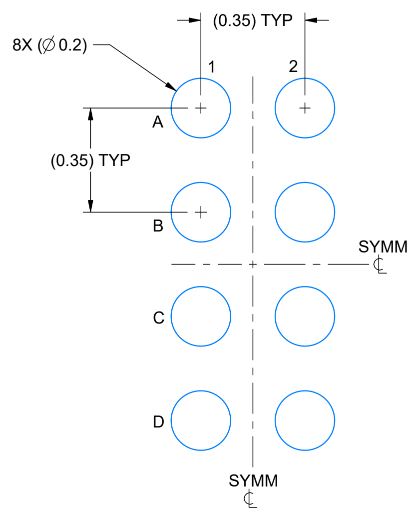

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

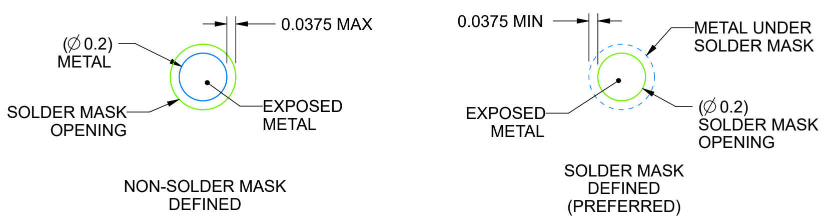
## EXAMPLE BOARD LAYOUT

**YCH0008-C02** **DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

4230869/A 05/2024

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

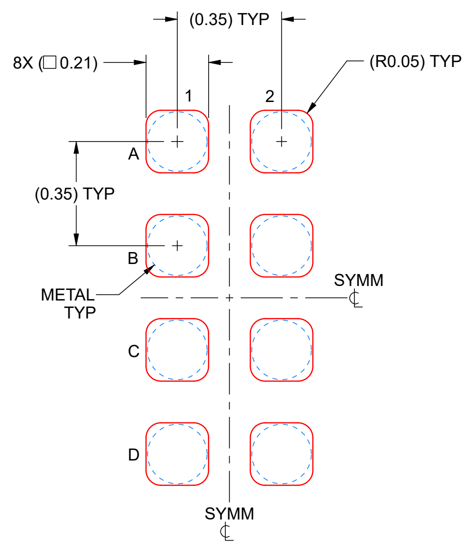
www.ti.com

# EXAMPLE STENCIL DESIGN

## YCH0008-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4230869/A 05/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LP5814DRLR | Active | Production | SOT-5X3 (DRL) \| 8 | 4000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 5814 |
| LP5814DRLR.A | Active | Production | SOT-5X3 (DRL) \| 8 | 4000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 5814 |
| LP5814YCHR | Active | Production | DSBGA (YCH) \| 8 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | G |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

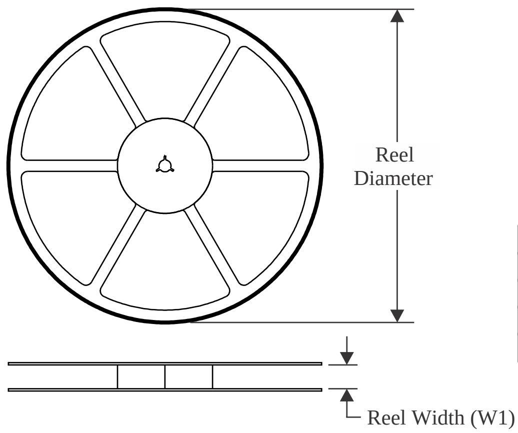
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

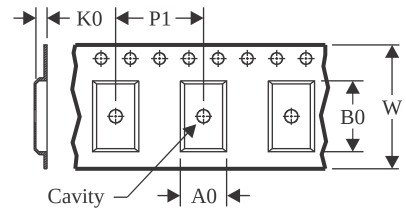
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

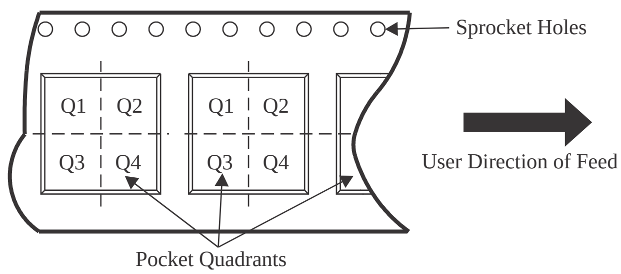



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

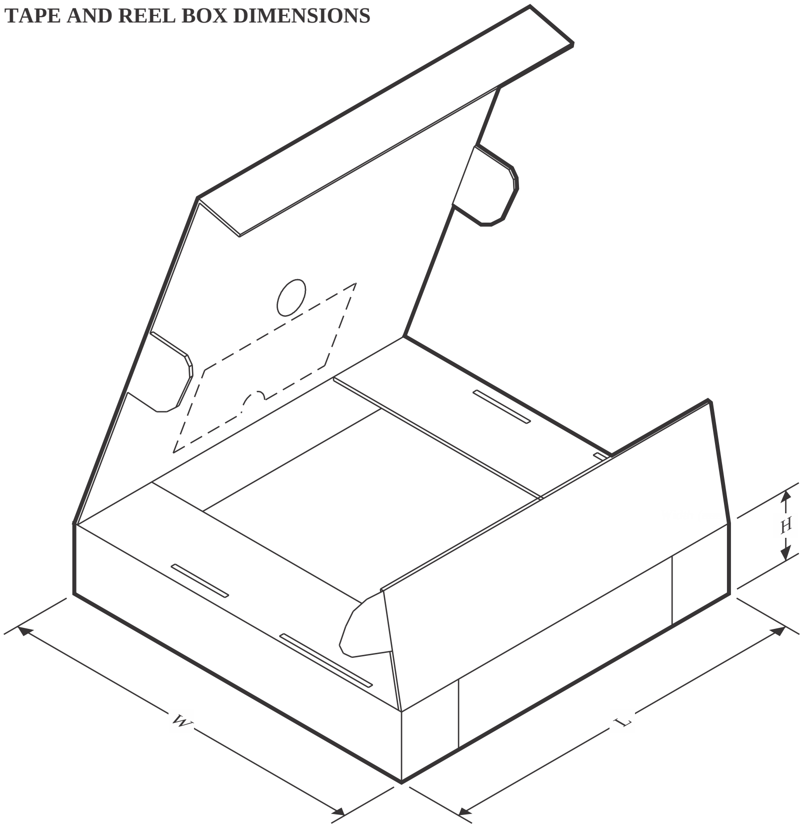
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

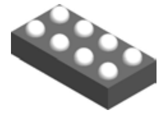
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP5814DRLR | SOT-5X3 | DRL | 8 | 4000 | 180.0 | 8.4 | 2.75 | 1.9 | 0.8 | 4.0 | 8.0 | Q3 |
| LP5814YCHR | DSBGA | YCH | 8 | 12000 | 180.0 | 8.4 | 0.92 | 1.48 | 0.43 | 2.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP5814DRLR | SOT-5X3 | DRL | 8 | 4000 | 210.0 | 185.0 | 35.0 |
| LP5814YCHR | DSBGA | YCH | 8 | 12000 | 182.0 | 182.0 | 20.0 |

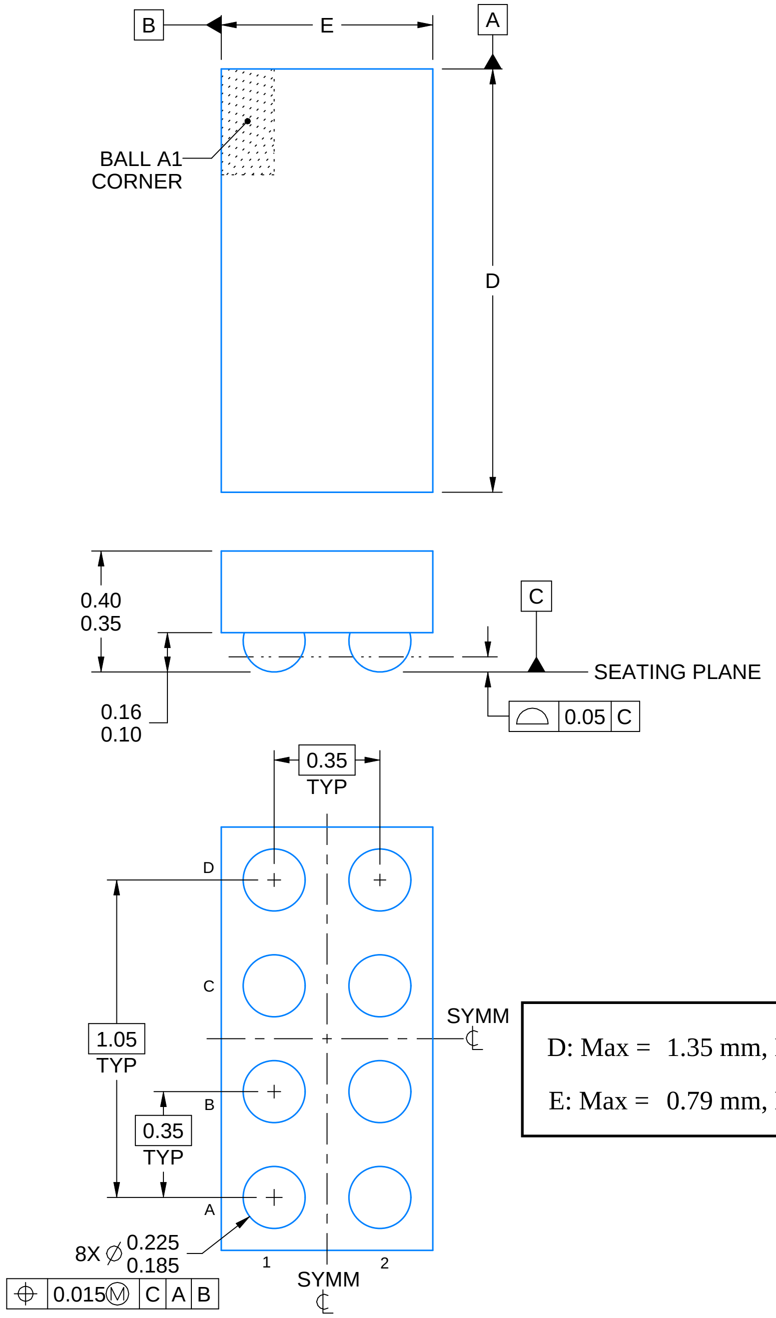


# YCH0008

# PACKAGE OUTLINE

## DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY

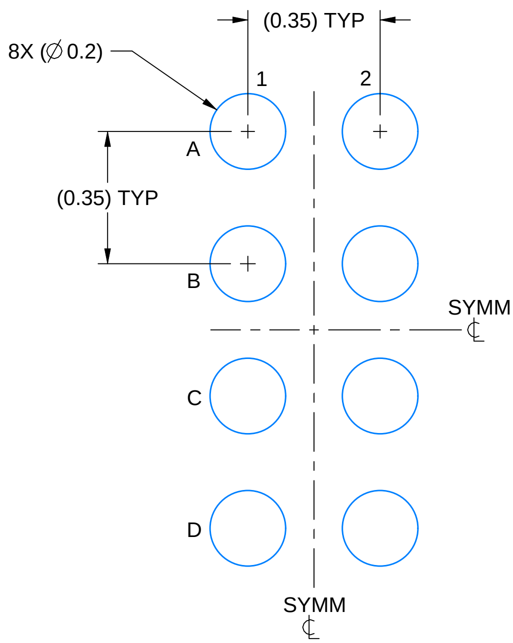



| | |
|---|---|
| D: Max = 1.35 mm, | Min = 1.289 mm |
| E: Max = 0.79 mm, | Min = 0.73 mm |

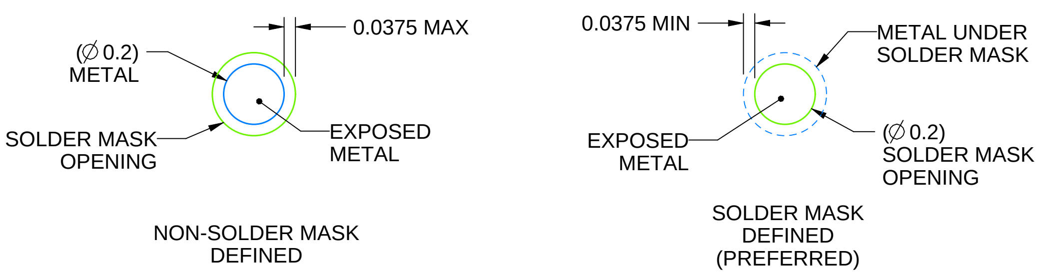
4225328/B 06/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

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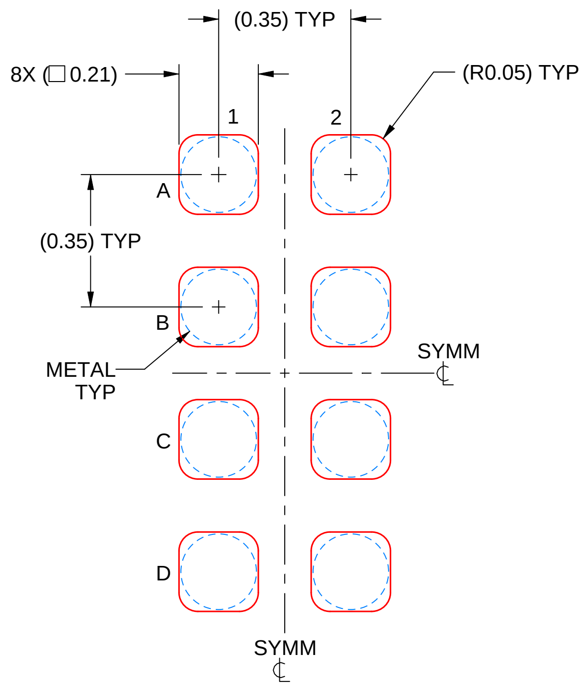
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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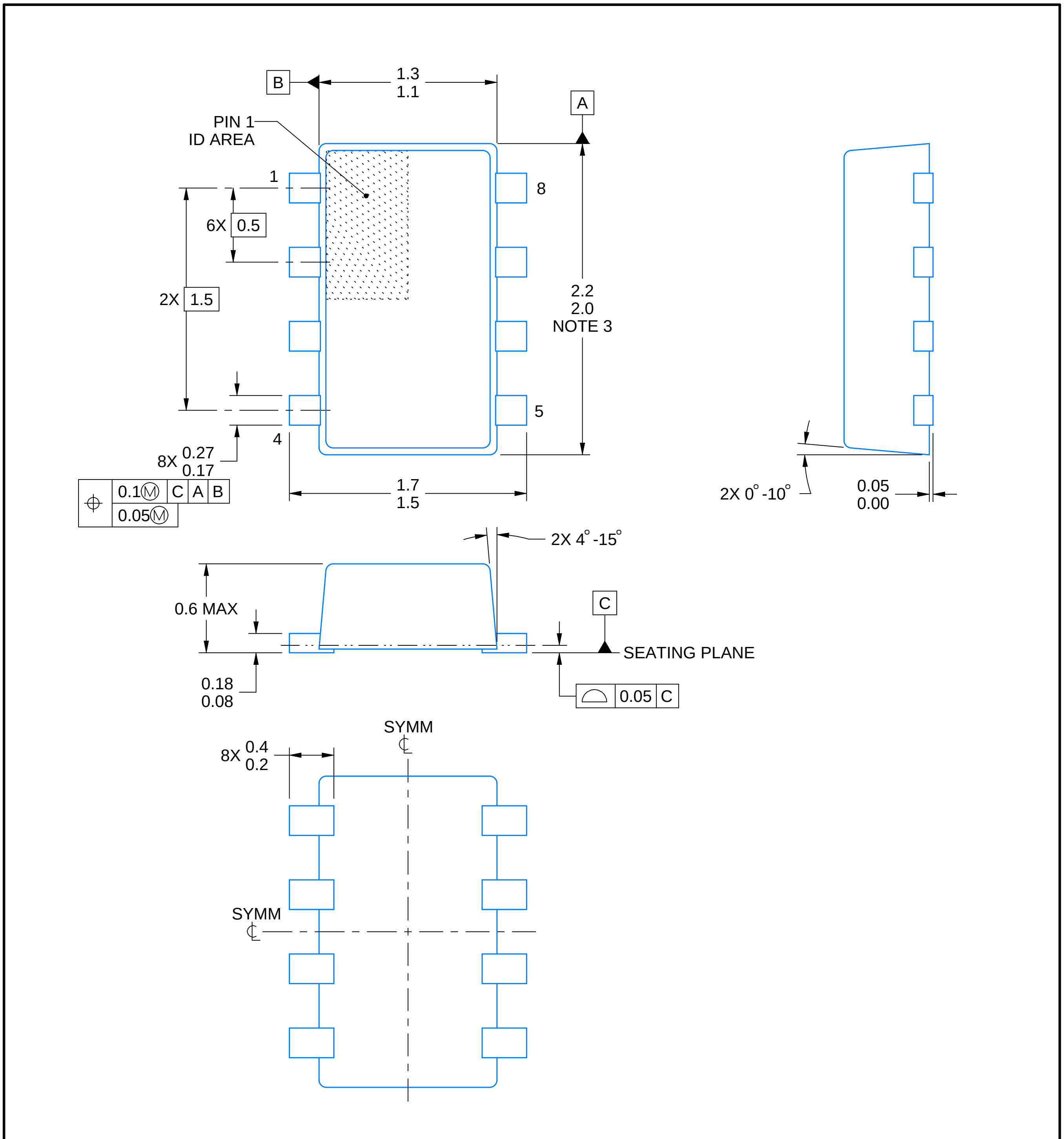
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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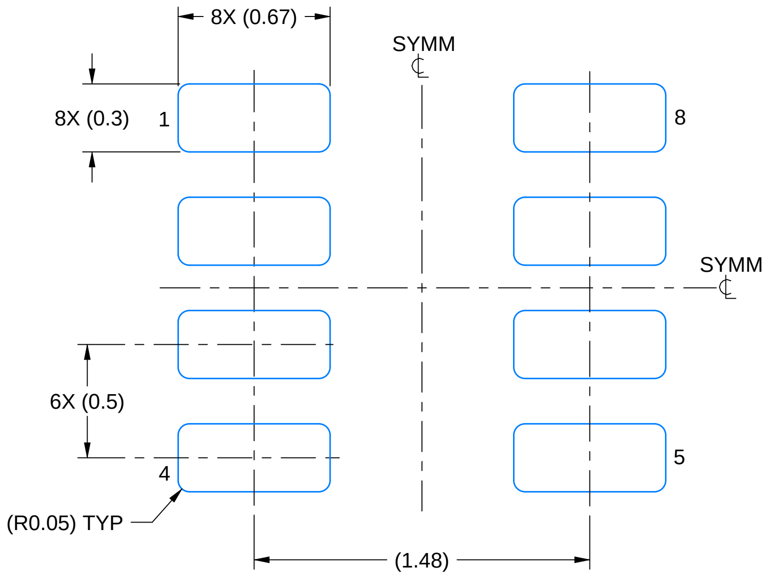
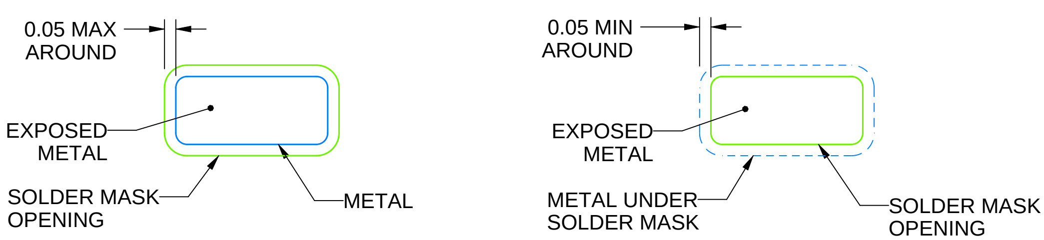
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X




NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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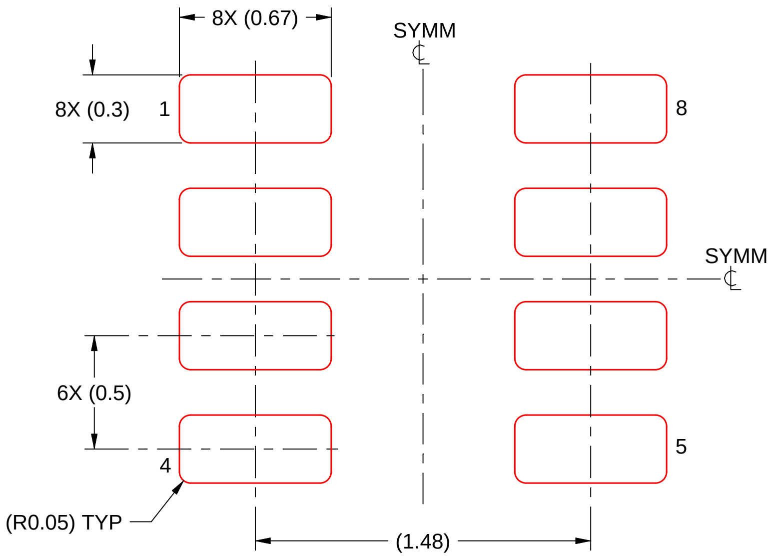
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.