LPV821, 650nA, Precision, Nanopower, Zero-Drift Amplifier

1 Features

- Quiescent Current: 650 nA
- Low Offset Voltage: ±10 µV (Maximum)
- Offset Voltage Drift: ±0.096 µV/°C (Maximum)
- 0.1-Hz to 10-Hz Noise: 3.9 μV_{PP}
- Input Bias Current: ±7 pA
- Gain Bandwidth: 8 kHz
- Supply Voltage: 1.7 V to 3.6 V
- Rail-to-Rail Input/Output
- Industry Standard Package
  – Single in 5-pin SOT-23
- EMI Hardened

2 Applications

- Battery-Powered Instruments
- Gas Detection
- Process Analytics
- Fault Monitoring
- Current Sensing
  – Shunt Resistor
  – Current Transformer
- Temperature Measurements
  – High Impedance Thermistors
  – RTD's, Thermocouples
- Strain Gauges
  – Electronic Scales
  – Pressure Sensors

3 Description

The LPV821 is a single-channel, nanopower, zero-drift operational amplifier for “Always ON” sensing applications in wireless and wired equipment where low input offset is required. With the combination of low initial offset, low offset drift, and 8 kHz of bandwidth from 650 nA of quiescent current, the LPV821 is the industry's lowest power zero-drift amplifier that can be used for end equipment that monitor current consumption, temperature, gas, or strain gauges.

The LPV821 zero-drift operational amplifier uses a proprietary auto-calibration technique to simultaneously provide low offset voltage (10 µV, maximum) and minimal drift over time and temperature. In addition to having low offset and ultra-low quiescent current, the LPV821 amplifier has pico-amp bias currents which reduce errors commonly introduced in applications monitoring sensors with high output impedance and amplifier configurations with megaohm feedback resistors.

Device Information(1)

PART NUMBER	CHAN COUNT	PACKAGE	BODY SIZE (NOM)
LPV821	1	SOT-23 (5)	2.90 mm × 1.60 mm
LPV822 (2)	2	WSON (8)	2.00 mm × 2.00 mm

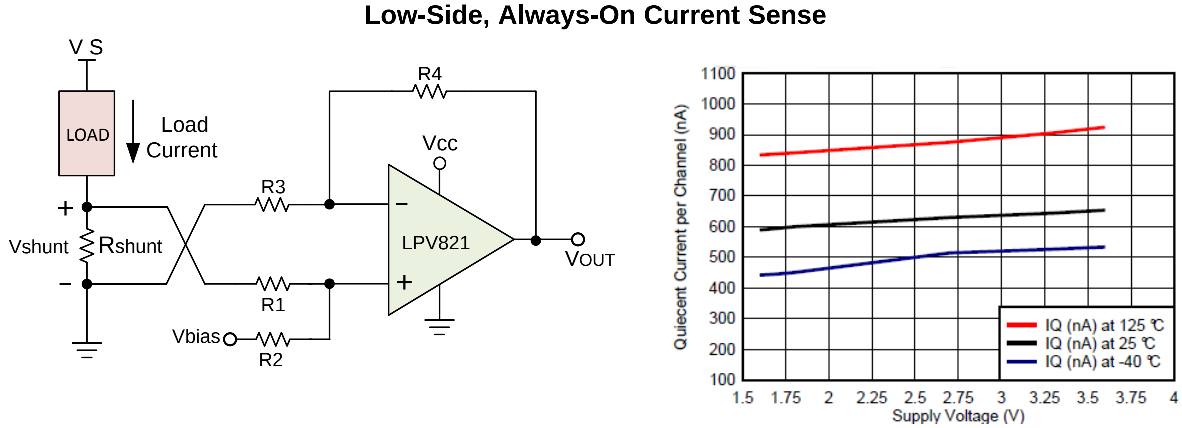
Precision Nano-Power Amplifier Family

FAMILY	CHAN COUNT	I_Q PER CHAN	V_{OS} (MAX)	V_{SUPPLY}
LPV821	1	650 nA	10 µV	1.7 to 3.6 V
LPV811	1	450 nA	370 µV	1.6 to 5.5 V
LPV812	2	425 nA	300 µV	1.6 to 5.5 V
OPA369	1,2	800 nA	750 µV	1.8 to 5.5 V

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Planned for near-future release

Low-Side, Always-On Current Sense



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (August 2017) to Revision A **Page**

- Changed Advanced Information to Production Data Release 1

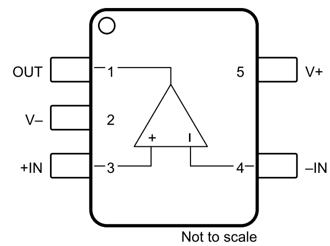
5 Description (continued)

The LPV821 amplifier also features an input stage with rail-to-rail input common mode range and an output stage that swings within 12 mV of the rails, maintaining the widest dynamic range possible. The device is EMI hardened to reduce system sensitivity to unwanted RF signals from mobile phones, WiFi, radio transmitters, and tag readers.

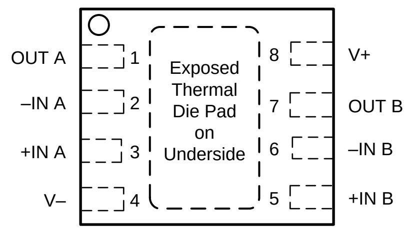
The LPV821 zero-drift amplifier operates with a single supply voltage as low as 1.7V, ensuring continuous performance in low battery situations over the extended temperature range of -40ºC to 125ºC. The LPV821 (single) is available in industry standard 5-pin SOT-23.

6 Pin Configuration and Functions

LPV821 5-Pin SOT-23
DBV Package
Top View



LPV822 8-Pin WSON
DSG Package
Top View



Pin Functions: LPV821 DBV

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Output
V–	2	P	Negative (lowest) power supply
+IN	3	I	Non-Inverting Input
–IN	4	I	Inverting Input
V+	5	P	Positive (highest) power supply

Pin Functions: LPV822 DSG (Preview)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

See [1]

		MIN	MAX	UNIT
Voltage	Supply, V_S = (V+) - (V–)	-0.3	4	V
	Input/Output Pin Voltage[2] [3]	(V–) - 0.3	(V+) + 0.3	
	Differential Input Voltage +IN - (-IN)[2]	- 0.3	+ 0.3	
Current	Signal input terminals[2]	–10	10	mA
	Output short-circuit[4]	Continuous	Continuous	
Junction temperature			150	°C
Operating ambient temperature		–40	125	
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Not to exceed -0.3V or +4.0V on ANY pin, referred to V-
(4) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	V_S = (V+) - (V–)	1.7		3.6	V
Specified temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC		LPV821 DBV (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	101.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

7.5 Electrical Characteristics

T_A = 25°C, V_S = 1.8 V to 3.3 V, V_{CM} = V_{OUT} = V_S/2, and R_L ≥ 10 MΩ to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 3.3 V			±1.5	±10	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C, V_S = 3.3 V			±0.02	±0.096	µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 3.3 V			0.4	4.5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	+IN	T_A= 25°C		7		pA
			T_A= 125°C		7		
		-IN	T_A= 25°C		-7		
			T_A= 125°C		-250		
I_{OS}	Input offset current				14		pA
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			3.9		$µV_{PP}$
e_n	Input voltage noise density	f = 100 Hz			215		nV/√Hz
i_n	Input current noise density	f = 100 Hz			1		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+), V_S = 3.3 V		100	125		dB
INPUT CAPACITANCE							
	Differential				3.3		pF
	Common-mode				3.7		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.1 V ≤ V_O ≤ (V+) – 0.1 V, R_L = 100 kΩ to V_S / 2			135		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ			8		kHz
SR	Slew rate	G = +1, C_L = 20 pF			3.3		V/ms
OUTPUT							
V_{OH}	Voltage output swing from positive rail	R_L = 100 kΩ to V^+/2, V_S = 3.3 V				12	mV
V_{OL}	Voltage output swing from negative rail	R_L = 100 kΩ to V^+/2, V_S = 3.3 V				12	
I_{SC}	Short-circuit current	Sourcing, V_O to V–, $V_{IN\ (diff)}$ = 100 mV, V_S = 3.3 V			21		mA
		Sinking, V_O to V+, $V_{IN\ (diff)}$ = –100 mV, V_S = 3.3 V			50		
C_L	Capacitive load drive				See Table 1		
Z_O	Open-loop output impedance	f = 100 Hz, I_O = 0 A			80		kΩ
POWER SUPPLY							
I_Q	Quiescent current per channel	V_{CM} = V_S/2, I_O = 0, V_S = 3.3 V			650	790	nA

7.6 Typical Characteristics

At T_A = 25°C, V_S = 3.3 V, V_{CM} = V_{OUT} = V_S/2, C_L = 20 pF, and R_L≥ 10 MΩ, unless otherwise noted.

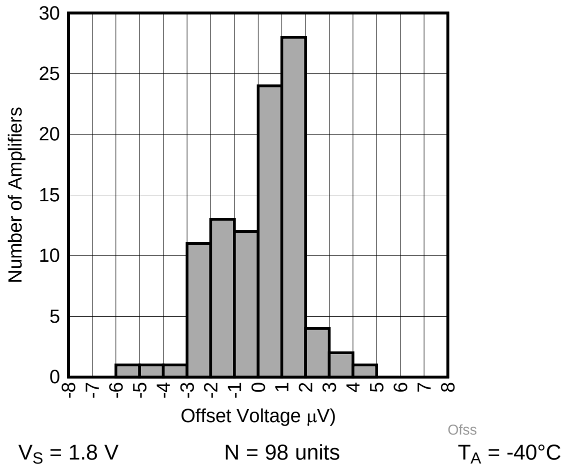


Figure 1. Offset Voltage Distribution, Vs = 1.8 V

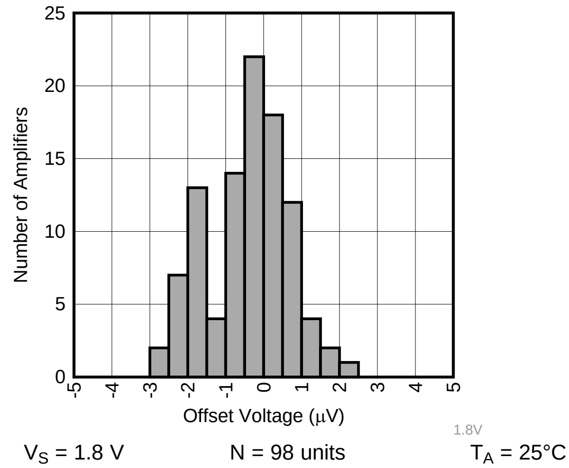


Figure 2. Offset Voltage Distribution, Vs = 1.8 V

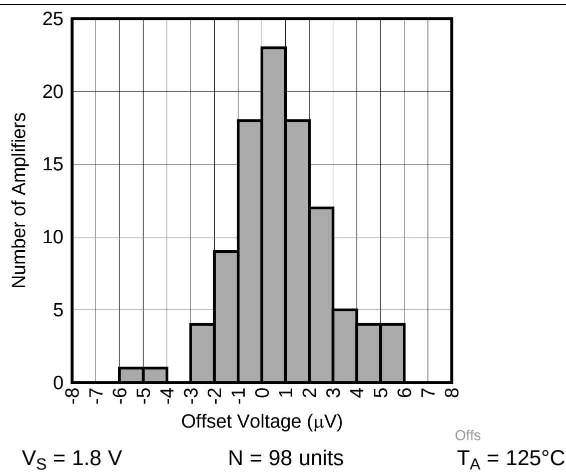


Figure 3. Offset Voltage Distribution, Vs = 1.8 V

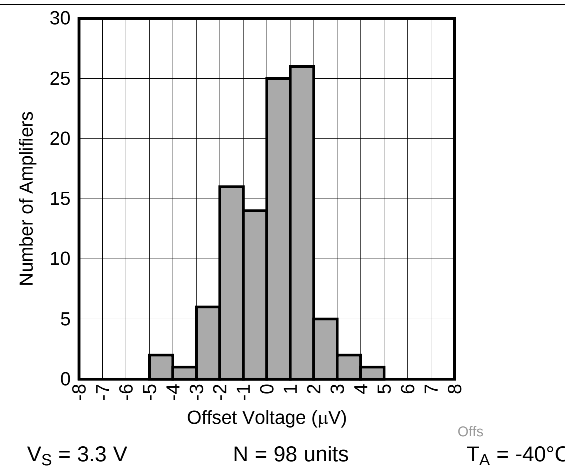


Figure 4. Offset Voltage Distribution, Vs = 3.3 V

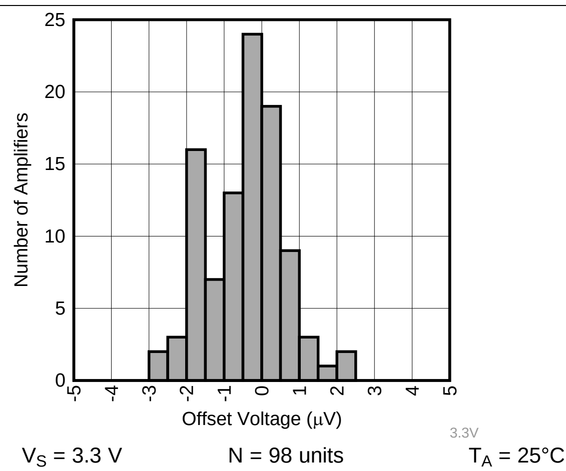


Figure 5. Offset Voltage Distribution, Vs = 3.3 V

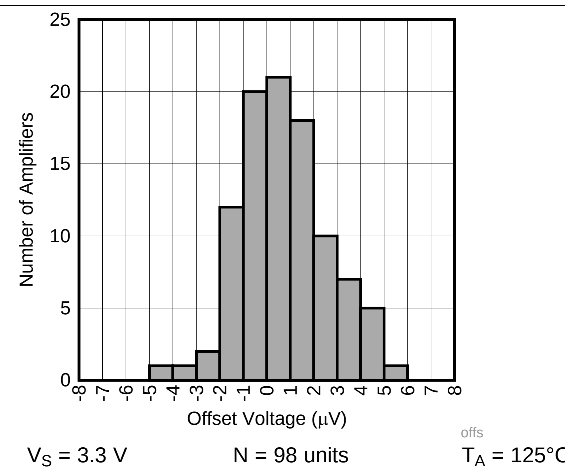
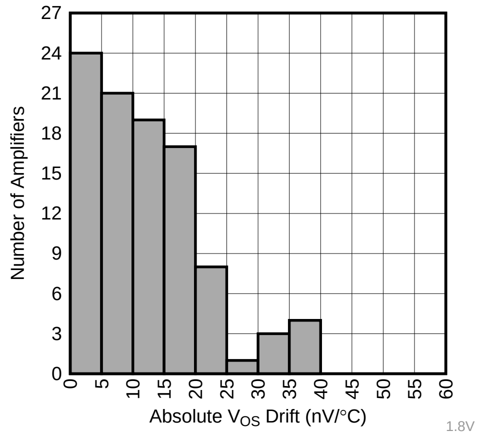


Figure 6. Offset Voltage Distribution, Vs = 3.3 V

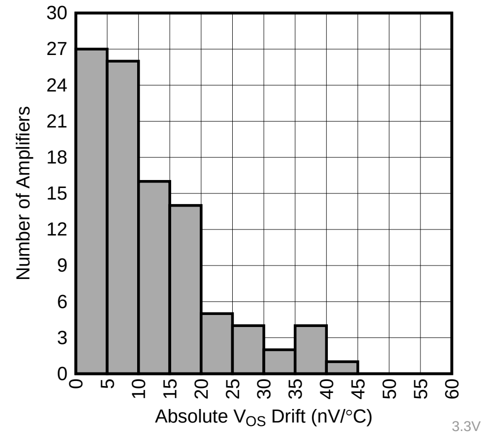
Typical Characteristics (continued)

At T_A = 25°C, V_S = 3.3 V, V_{CM} = V_{OUT} = V_S/2, C_L = 20 pF, and R_L ≥ 10 MΩ, unless otherwise noted.



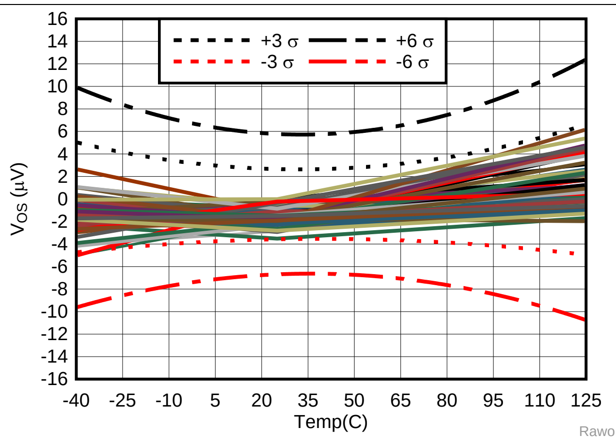
V_S = 1.8 V N = 98 units

Figure 7. Offset Voltage Drift Distribution, Vs = 1.8 V



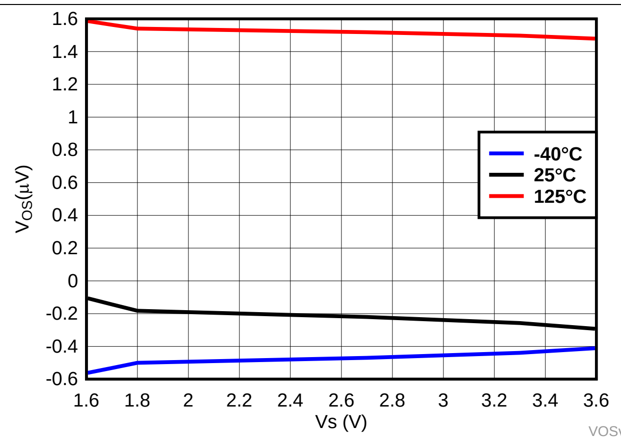
V_S = 3.3 V N = 98 units

Figure 8. Offset Voltage Drift Distribution, Vs = 3.3 V



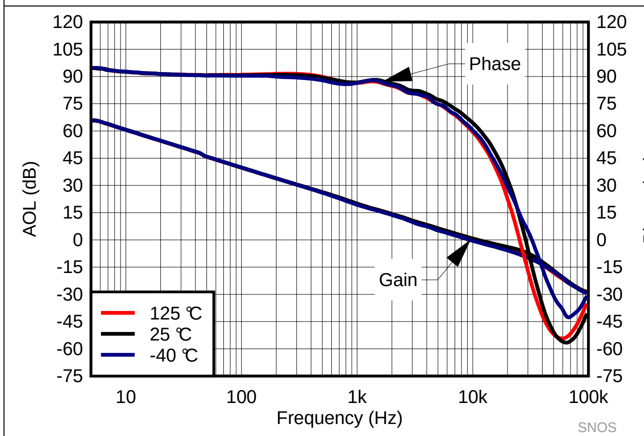
V_S = 3.3 V N = 98 units

Figure 9. Offset Voltage vs Temperature, Vs = 3.3 V



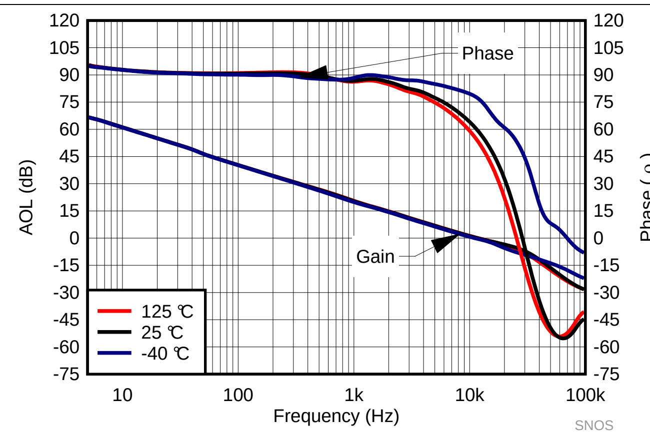
T_A = –40, 25, 125°C

Figure 10. Offset Voltage vs Supply Voltage



V_S = 1.8 V C_L = 20 pF T_A = –40, 25, 125°C

Figure 11. Open-Loop Gain and Phase vs Frequency

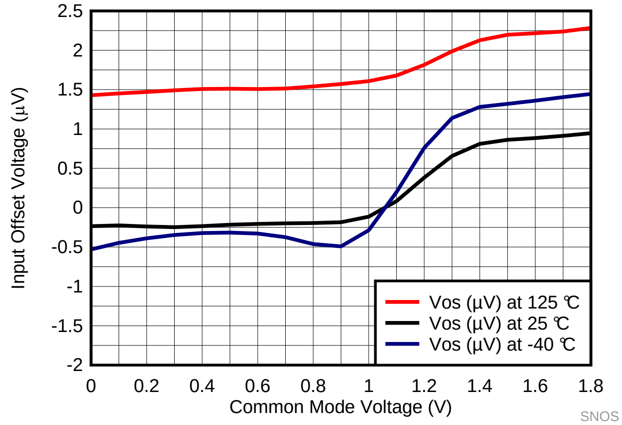


V_S = 3.3 V C_L = 20 pF T_A = –40, 25, 125°C

Figure 12. Open-Loop Gain and Phase vs Frequency

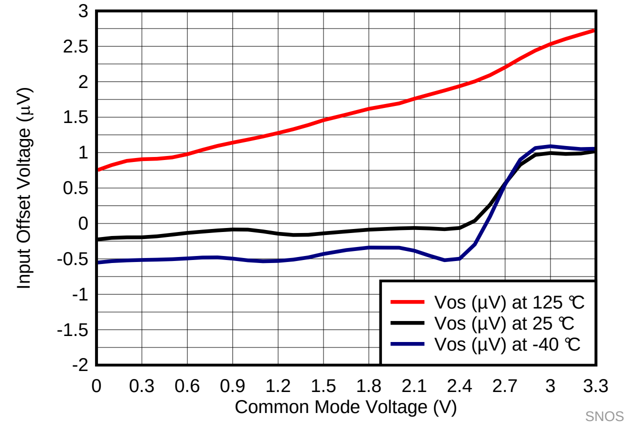
Typical Characteristics (continued)

At T_A = 25°C, V_S = 3.3 V, V_{CM} = V_{OUT} = V_S/2, C_L = 20 pF, and R_L ≥ 10 MΩ, unless otherwise noted.



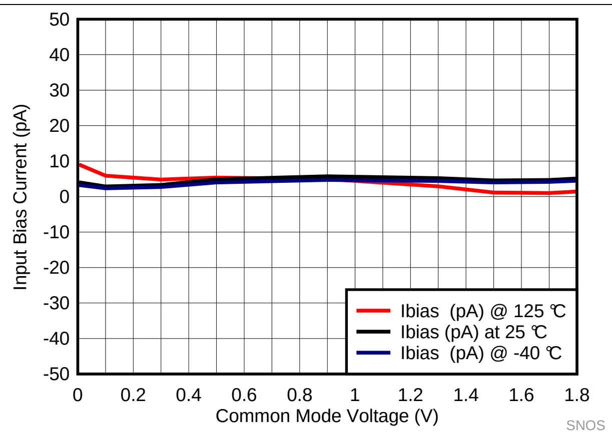
V_S = 1.8 V

Figure 13. Input Offset Voltage vs Input Common Mode Voltage



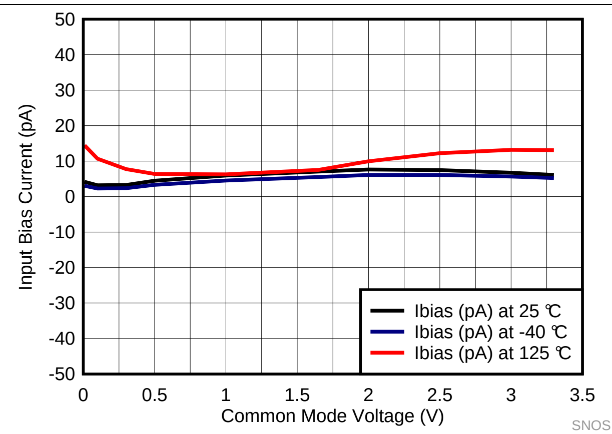
V_S = 3.3 V

Figure 14. Input Offset Voltage vs Input Common Mode Voltage



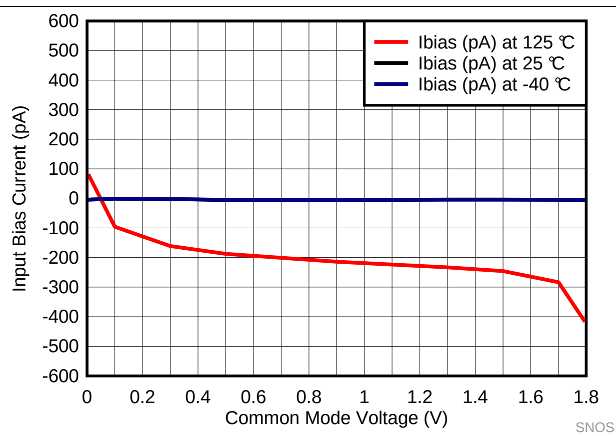
V_S = 1.8 V

Figure 15. Input Bias Current on +IN Input Pin vs Common Mode Voltage



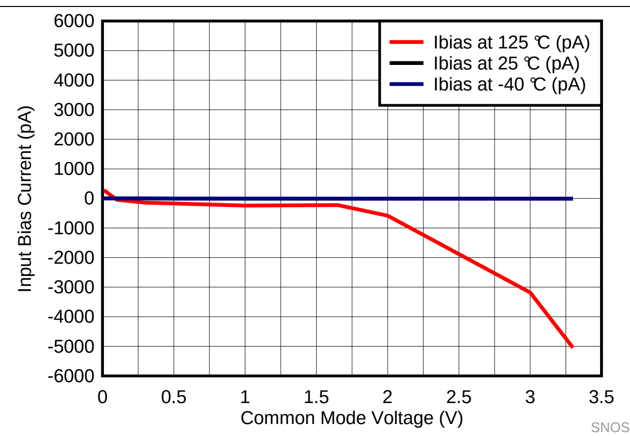
V_S = 3.3 V

Figure 16. Input Bias Current on +IN Input Pin vs Common Mode Voltage



V_S = 1.8 V

Figure 17. Input Bias Current on –IN Pin vs Common Mode Voltage

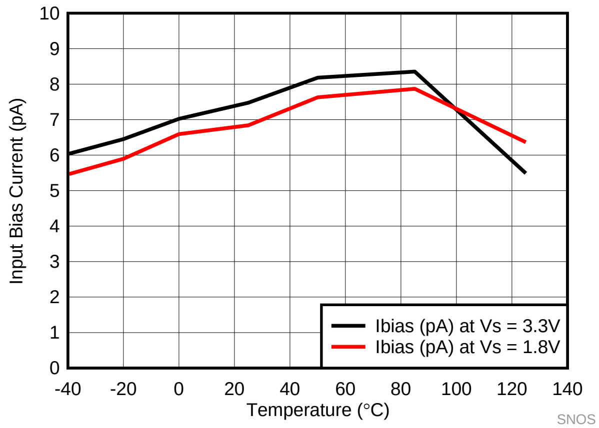


V_S = 3.3 V

Figure 18. Input Bias Current on –IN Input Pin vs Common Mode Voltage

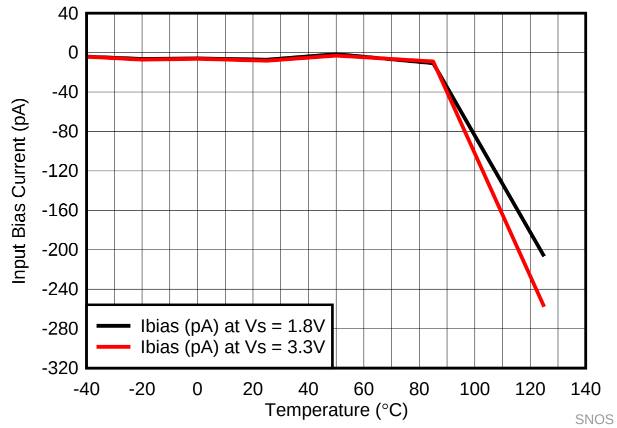
Typical Characteristics (continued)

At T_A = 25°C, V_S = 3.3 V, V_{CM} = V_{OUT} = V_S/2, C_L = 20 pF, and R_L ≥ 10 MΩ, unless otherwise noted.



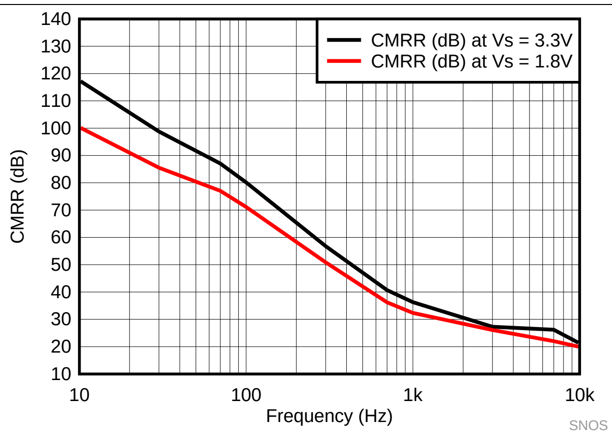
V_S = 3.3 V and 1.8 V

Figure 19. Input Bias Current ON +IN Input vs Temperature



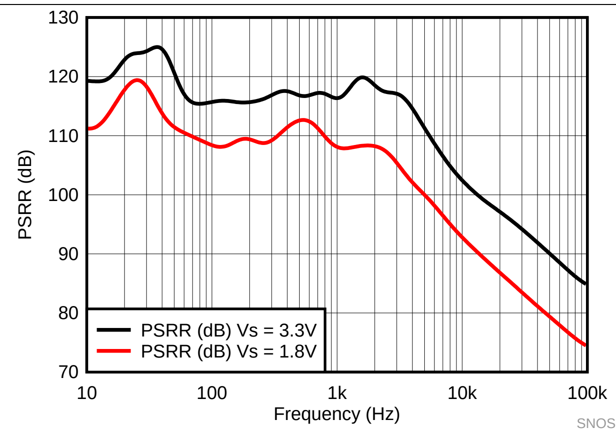
V_S = 3.3 V and 1.8 V

Figure 20. Input Bias Current on –IN Input Pin vs Temperature



V_S = 3.3 V and 1.8 V

Figure 21. CMRR vs Frequency



V_S = 3.3 V and 1.8 V

Figure 22. PSRR vs Frequency

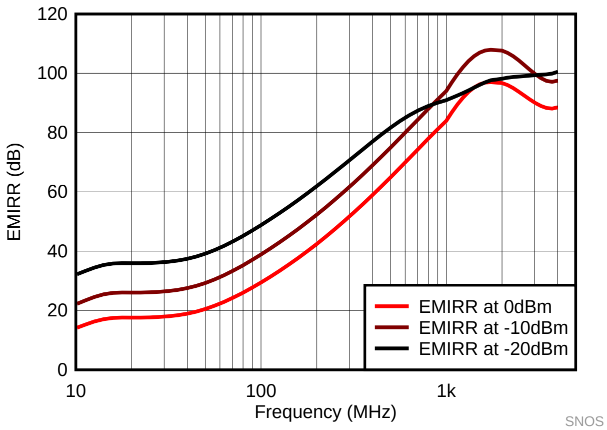
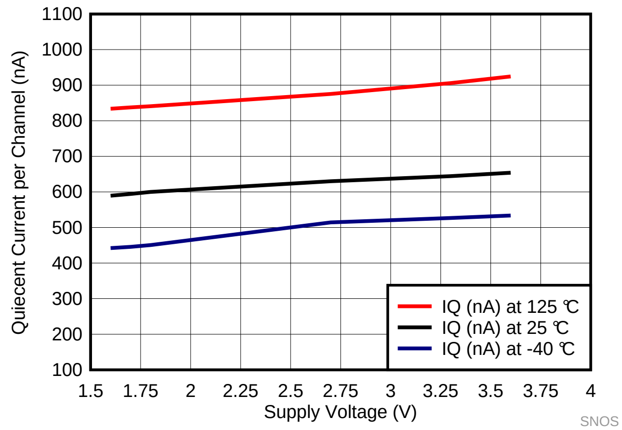


Figure 23. EMIRR Performance

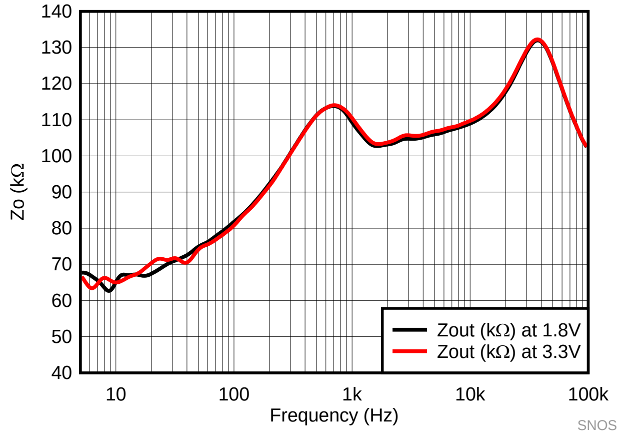


T_A = –40, 25, 125°C

Figure 24. Per Channel Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = 3.3 V, V_{CM} = V_{OUT} = V_S/2, C_L = 20 pF, and R_L≥ 10 MΩ, unless otherwise noted.



V_S = 3.3 V and 1.8 V

Figure 25. Open Loop Output Impedance

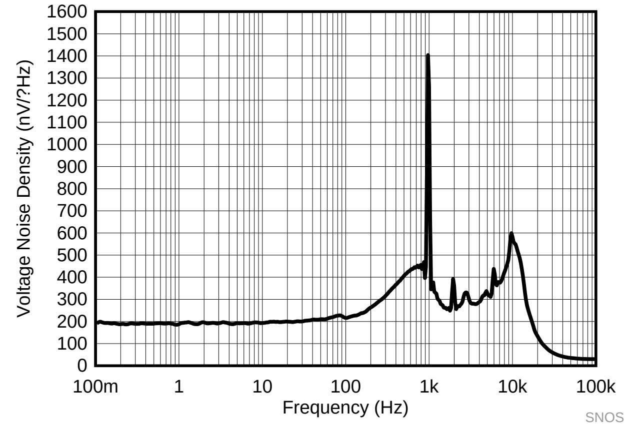
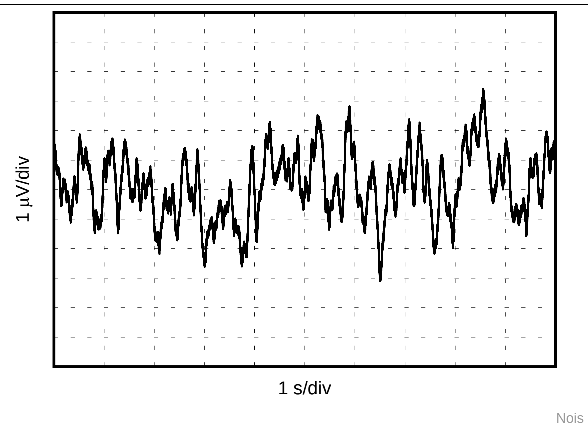
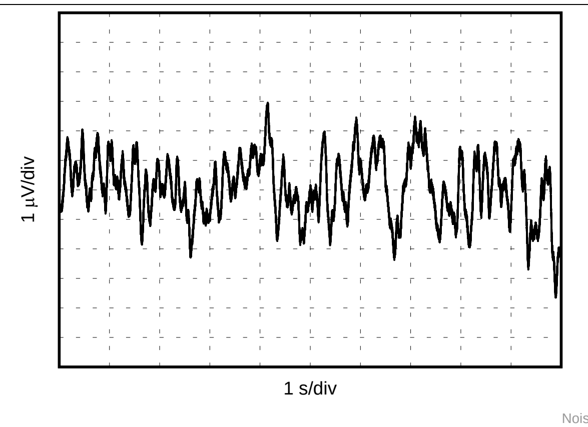


Figure 26. Voltage Noise Spectral Density vs Frequency



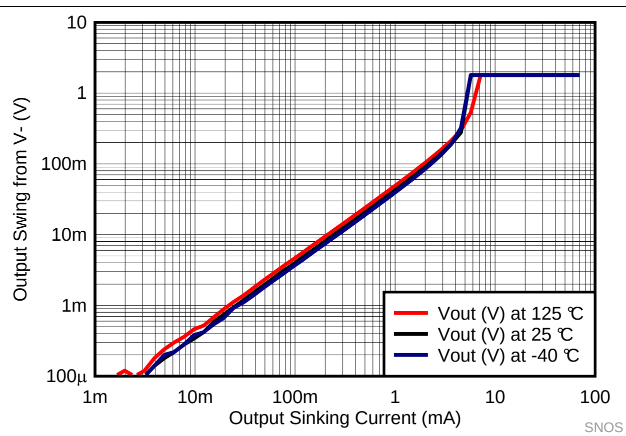
V_S = 3.3 V

Figure 27. 0.1-Hz to 10-Hz Noise, Vs = 3.3 V



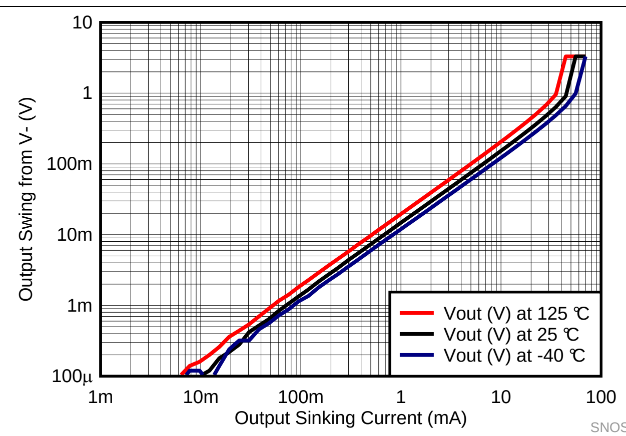
V_S = 1.8 V

Figure 28. 0.1-Hz to 10-Hz Noise, Vs = 1.8 V



V_S = 1.8 V TA = –40, 25, 125°C

Figure 29. Output Swing vs. Sinking Current, 1.8 V

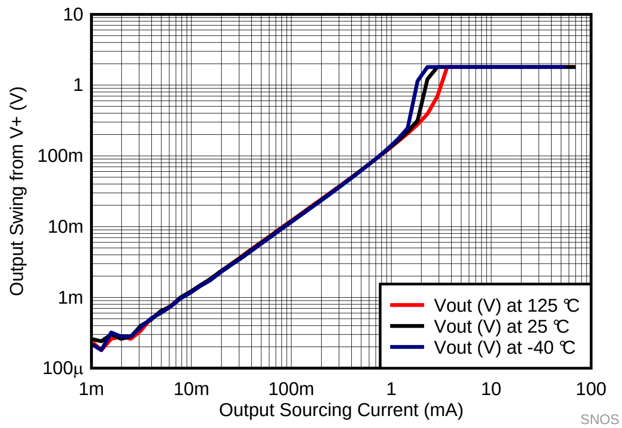


V_S = 3.3 V T_A = –40, 25, 125°C

Figure 30. Output Swing vs. Sinking Current, 3.3 V

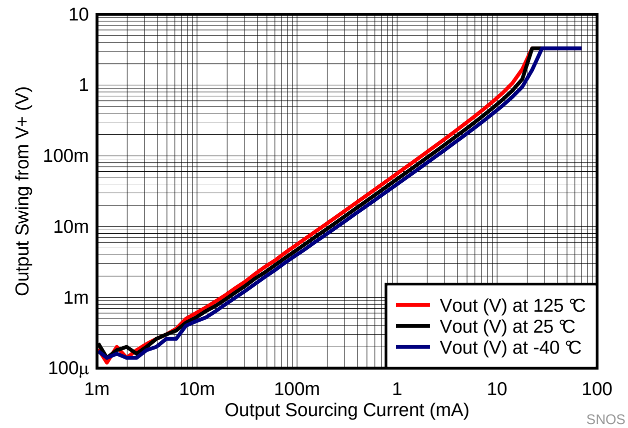
Typical Characteristics (continued)

At T_A = 25°C, V_S = 3.3 V, V_{CM} = V_{OUT} = V_S/2, C_L = 20 pF, and R_L ≥ 10 MΩ, unless otherwise noted.



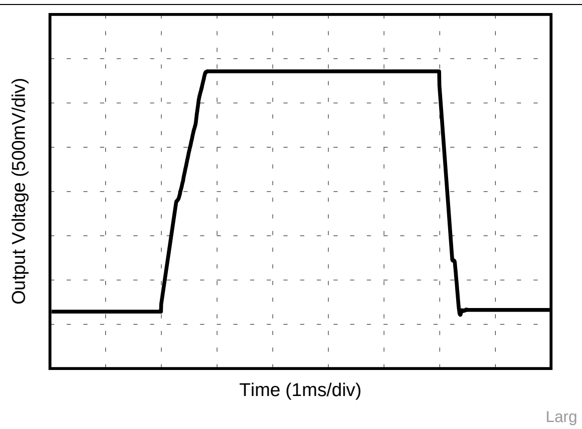
V_S = 1.8 V TA = –40, 25, 125°C

Figure 31. Output Swing vs Sourcing Current, 1.8 V



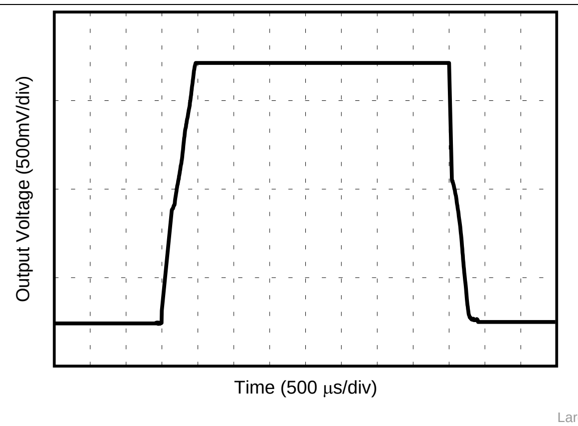
V_S = 3.3 V T_A = –40, 25, 125°C

Figure 32. Output Swing vs Sourcing Current, 3.3 V



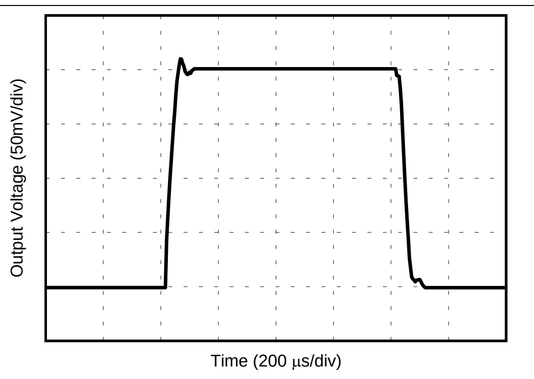
V_{IN} = 2.64 V_{PP} G = 1 R_L = 1 MΩ

Figure 33. Large-Signal Response, 3.3V



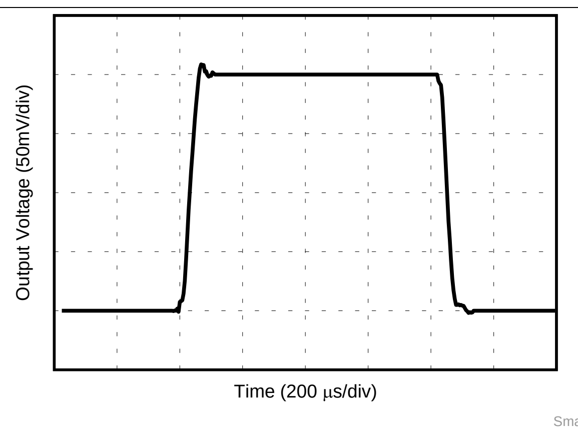
V_{IN} = 1.44 V_{PP} G = 1 R_L = 1 MΩ

Figure 34. Large-Signal Response, 1.8V



V_{IN} = 0.2 V_{PP} G = 1 R_L = 1 MΩ

Figure 35. Small Signal Response, 3.3V



V_{IN} = 0.2 V_{PP} G = 1 R_L = 1 MΩ

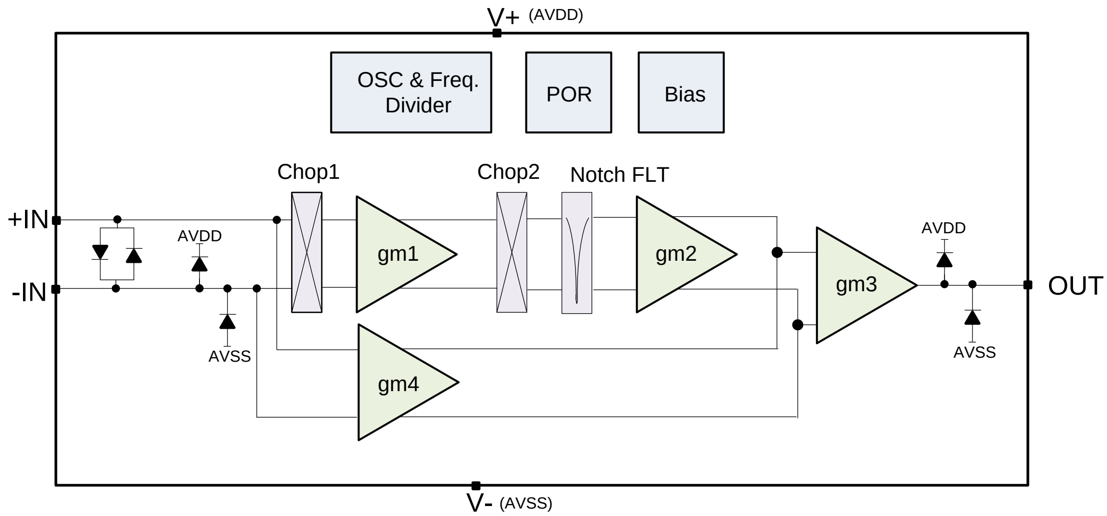
Figure 36. Small-Signal Response, 1.8V

8 Detailed Description

8.1 Overview

The LPV821 is a zero-drift, nanopower, rail-to-rail input and output operational amplifier. The device operates from 1.7 V to 3.7 V, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The zero-drift architecture provides ultra low offset voltage and near-zero offset voltage drift.

8.2 Functional Block Diagram



8.3 Feature Description

The LPV821 is unity-gain stable and uses an auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

8.3.1 Operating Voltage

The LPV821 operational amplifier operates over a power-supply range of 1.7 V to 3.6 V (±0.85 V to ± 1.8 V). Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section.

CAUTION

Supply voltages higher than 4 V (absolute maximum) can permanently damage the device.

Feature Description (continued)

8.3.2 Input

The LPV821 input common-mode voltage range extends to the supply rails. Typically, the input bias current is approximately 7 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with adding a resistor in series with the input, as shown in Figure 37.

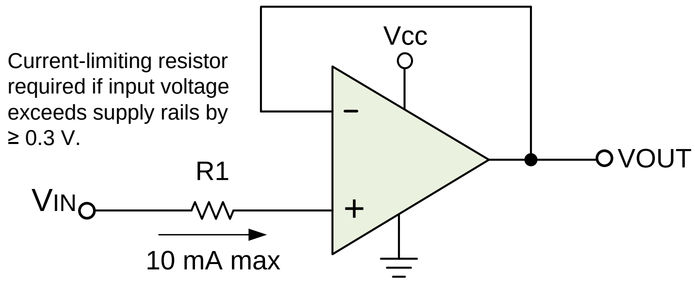


Figure 37. Input Current Protection

8.3.3 Internal Offset Correction

The LPV821 operational amplifier combines an auto-calibration technique with a time-continuous 8-kHz operational amplifier in the signal path. The amplifier's offset is zero-corrected every 1 ms using a proprietary technique. This design has no aliasing or flicker (1/f) noise.

8.3.4 Input Offset Voltage Drift

The LPV821 operational amplifier's input voltage offset drift is defined over the entire temperature range of –40°C to 125°C. The maximum input voltage drift allows designers to calculate the worst-case input offset change over this temperature range. The maximum input voltage drift over temperature is defined using Equation 1:

$$dV_{OS}/dT = \Delta V_{OS} / \Delta T$$

where

- ΔV_{OS} = Change in input offset voltage
- ΔT = Change in temperature (125°C - (-40°C) = 165°C)
- dV_{OS}/dT = Input offset voltage drift (1)

The LPV821 datasheet maximum value for input offset voltage drift is specified for a sample size with a C_{pk} (process capability index) of 2.0.

8.4 Device Functional Modes

The LPV821 has a single functional mode. The device is powered on as long as the power supply voltage is between 1.7 V (±0.85 V) and 3.6 V (±1.8 V).

8.4.1 EMI Performance and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The LPV821 operational amplifier incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common mode and differential-mode filtering are provided by the input filter.

Device Functional Modes (continued)

8.4.2 Driving Capacitive Load

The LPV821 is internally compensated for stable unity-gain operation, with a 8-kHz typical gain bandwidth. However, the unity-gain follower is the most sensitive configuration-to-capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is under-damped, which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

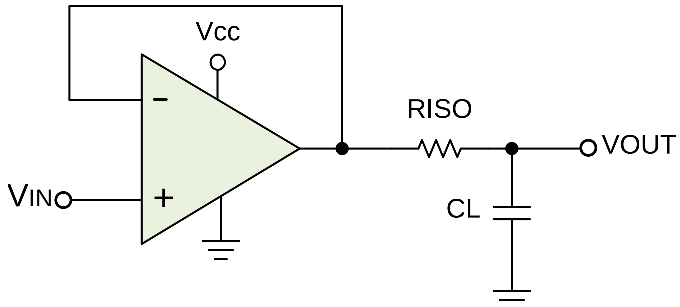


Figure 38. Resistive Isolation of Capacitive Load

In order to drive heavy (> 50 pF) capacitive loads, use an isolation resistor, R_{ISO}, as shown in Figure 38. The value of the R_{ISO} to be used should be decided depending on the size of the $C_L$and the level of performance desired. Recommended minimum values for R_{ISO} are given in the following table, for 3.3V supply. Figure 39 shows the typical response obtained with the C_L = 50 pF R_{ISO} = 160 kΩ. By using the isolation resistor, the capacitive load is isolated from the output of the amplifier. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop is stable, independent of the value of C_L. However, larger values of R_{ISO} (e.g. 50 kΩ) result in reduced output swing and reduced output current drive.

Table 1. Capacitive Loads vs. Needed Isolation Resistors

C_L	R_{ISO}
0 – 20 pF	not needed
50 pF	160 kΩ
100 pF	140 kΩ
500 pF	54.9 kΩ
1 nF	33 kΩ
5 nF	15 kΩ
10 nF	5.62 kΩ

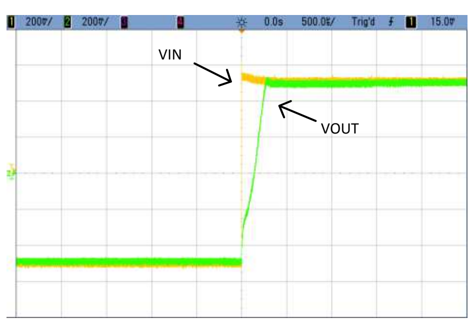


Figure 39. Typical Step Response

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LPV821 is a unity-gain stable, precision operational amplifier with very low offset voltage drift; the device is also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-μF capacitors are adequate.

9.2 Typical Applications

9.2.1 Low-Side Current Measurement

This single-supply, low-side, current-sensing solution shown in Figure 40 detects load currents up to 1 A. This design uses the LPV821 because of its low offset voltage and rail-to-rail input and output. The LPV821 in the main signal path is configured as a difference amplifier and a second LPV821 provides a buffered bias voltage to allow transition of signal below and above the bias level for bi-direction current sensing. The low offset voltage and offset drift of the LPV821 facilitate excellent dc accuracy for the circuit.

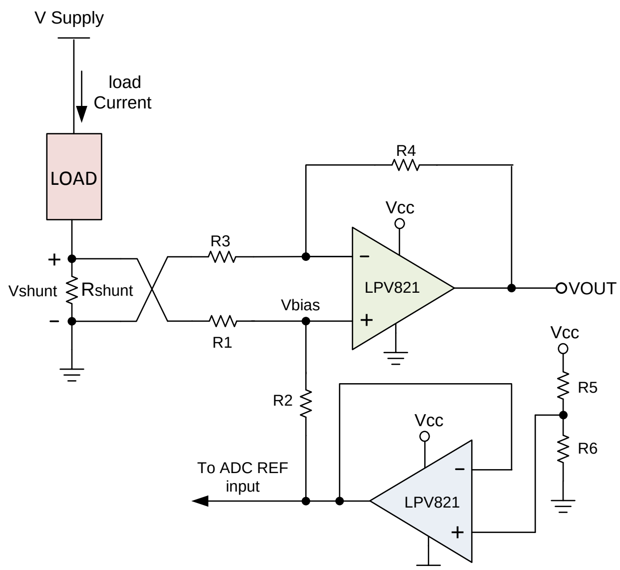


Figure 40. Low-Side Current Measurement

9.2.1.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 3.3 V DC
- Input: 1 A (Max)
- Output: 1.65V ± 1.54 V ; (110 mV to 3.19 V)

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Referring to Figure 40, the load current passing though the shunt resistor (Rshunt) develops the shunt voltage, Vshunt across the resistor. The shunt voltage is then amplified by the LPV821 by the ratio of R4 by R3 . The gain of the difference amplifier is set by the ratio of R4 to R3 . To minimize errors, set R2 = R4 and R1 = R3 . The bias voltage is supplied by buffering a resistor divider using a second LPV821 nanopower op amp. The circuit equations are provided below.

$$V_{out} = V_{shunt} * Gain_{Diff} + V_{bias} \quad (2)$$

$$V_{shunt} = I_{load} * R_{shunt} \quad (3)$$

$$Gain_{Diff} = R_4 / R_3 \quad (4)$$

$$V_{bias} = [R_6 / (R_6 + R_5)] * V_{CC} \quad (5)$$

$$R_{shunt} = [V_{shunt}(max)] / [I_{load}(max)] \quad (6)$$

Because V_{shunt} is a low-side measurement, a maximum value 100 mV was selected.

$$R_{shunt} = V_{shunt} / I_{load} = 100mV / 1A = 100m\Omega \quad (7)$$

The tolerance of the shunt resistor, the ratio of R4 to R3 and the ratio of R2 to R1 are the main sources of gain error in the signal path. To optimize the cost, a shut resistor with a tolerance of 0.5% was chosen. The main sources of offset errors in the circuit are the voltage divider network comprise of R5, R6 and how closely the ratio of R4 / R3 matches the ration of R2 / R1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The shunt voltage is scaled down by a divider network made of R1 and R2 before reaching the LPV821 amplifier stage. The voltage present at the non-inverting node of the LPV821 should not exceed the common-mode range of the device. The extremely low offset voltage and drift of the LPV821 ensures minimized offset error in the measurement.

In case a bi-direction current sensing is required, for symmetric load current of –1 A to 1 A, the voltage divider resistors R5 and R6 must be equal. To minimize power consumption, 100-kΩ resistors with a tolerance of 0.5% were selected.

To set the gain of the difference amplifier, the common-mode range and output swing of the LPV821 must be considered. The gain of the difference amplifier can now be calculated as shown below

$$Gain = [Vout(max) - Vout(min)] / [R_{shunt} * (I_{max} - I_{min})] = [3.2\ V - 100\ mV] / [100\ m\Omega] * [1A - (-1A)] = 15.5\ V/V \quad (8)$$

10 Power Supply Recommendations

The LPV821 is specified for operation from 1.7 V to 3.6 (±0.85 V to ±1.8 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 4 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

11 Layout

11.1 Layout Guidelines

11.1.1 General Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The LPV821 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

11.2 Layout Example

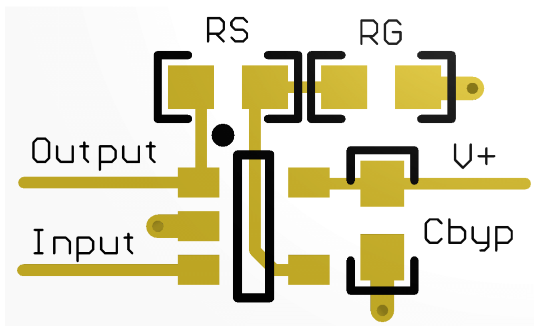


Figure 41. SOT-23 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

TINA-TI SPICE-Based Analog Simulation Program

DIP Adapter Evaluation Module

TI Universal Operational Amplifier Evaluation Module

TI FilterPro Filter Design Software

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LPV821	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LPV821DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1CHF
LPV821DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1CHF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

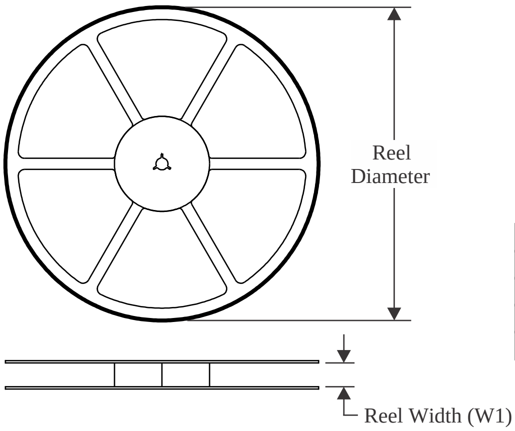
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

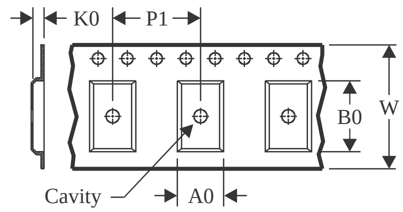
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

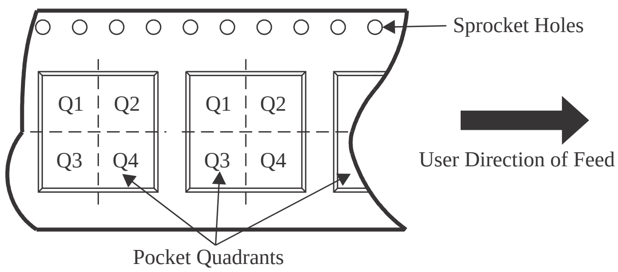


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

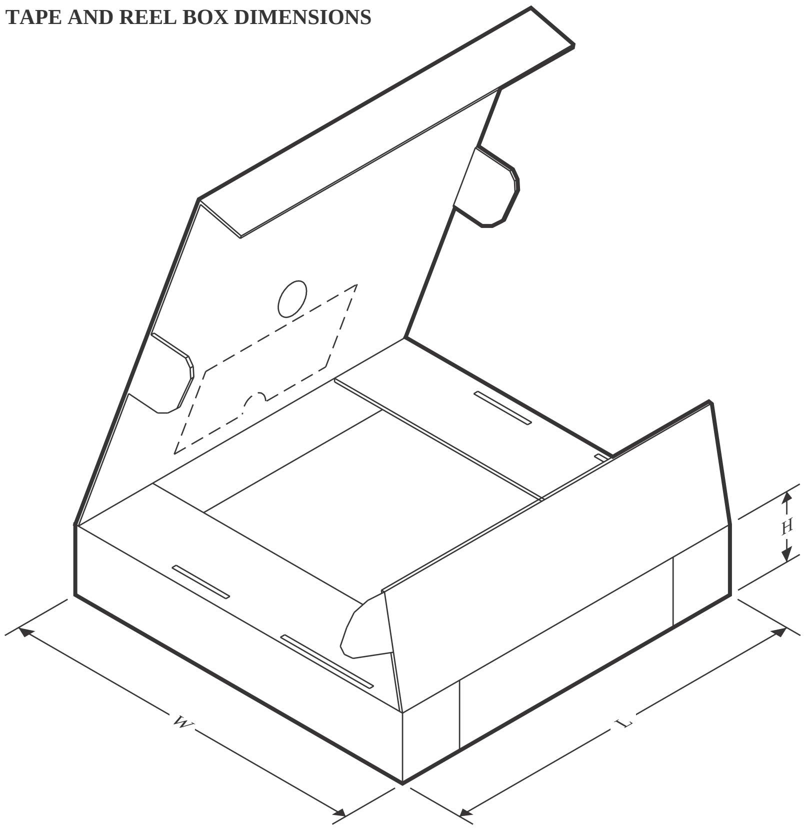
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

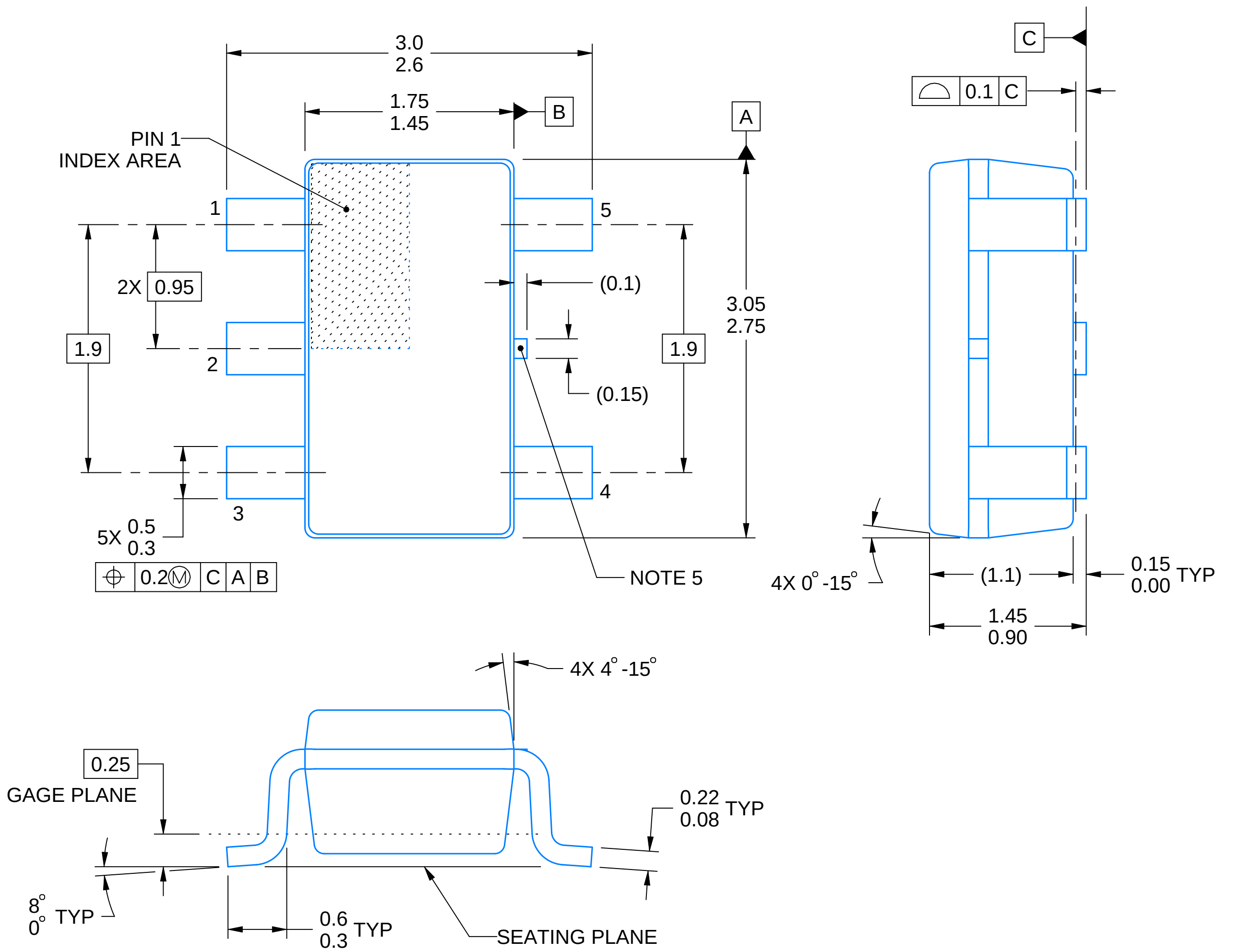
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV821DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV821DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0



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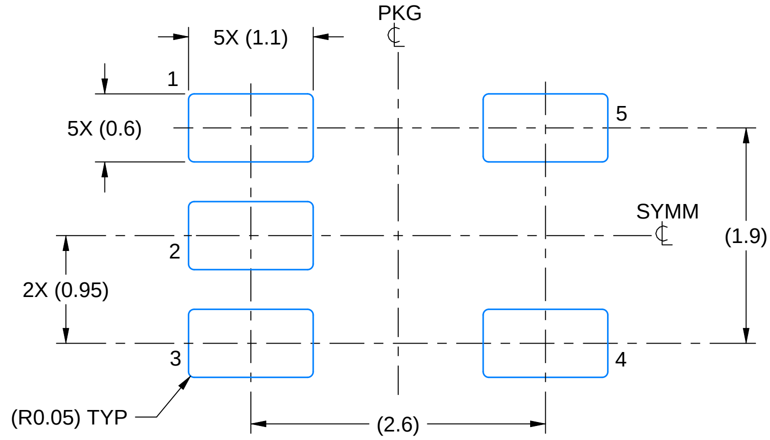
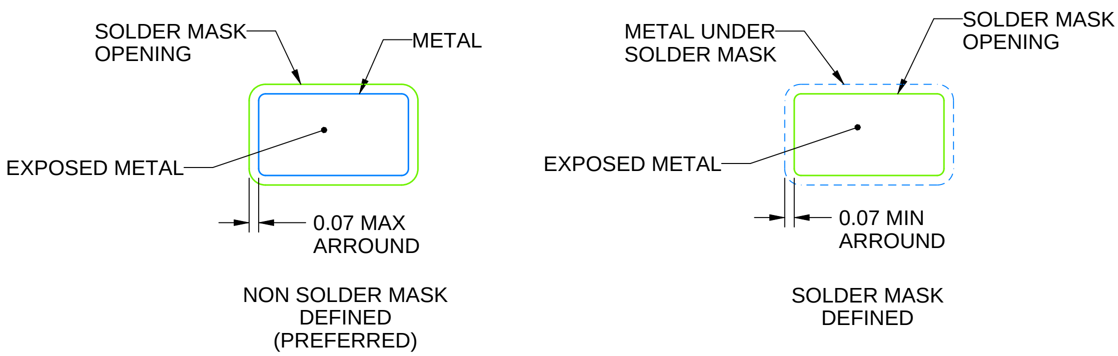
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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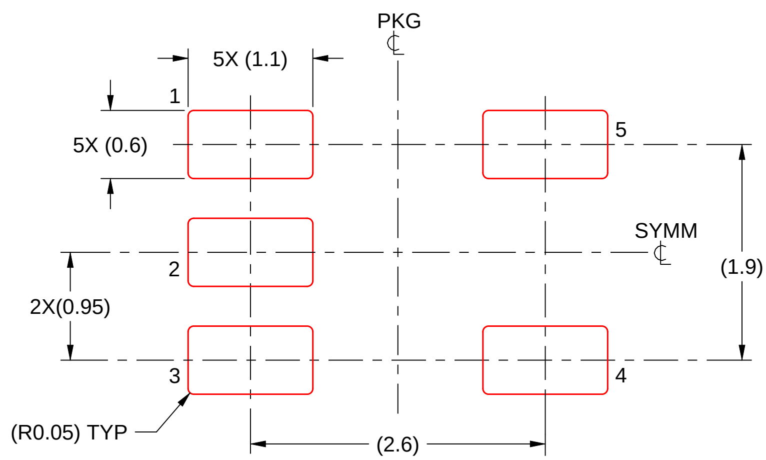
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.