

MAX3221 3-V to 5.5-V RS-232 Line Driver and Receiver

With ± 15 -kV ESD Protection

1 Features

- RS-232 Bus-pin ESD protection exceeds ± 15 kV using human body model (HBM)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU V.28 standards
- Operates with 3-V to 5.5-V V_{CC} supply
- Operates up to 250 kbps
- One driver and one receiver
- Low standby current: 1 μ A typical
- External capacitors: $4 \times 0.1 \mu$ F
- Accepts 5-V logic input with 3.3-V supply
- Alternative high-speed pin-compatible device (1 Mbps)
 - SNx5C3221
- Automatic power-down feature automatically disables drivers for power savings

2 Applications

- [Industrial PCs](#)
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Battery-powered systems](#)
- [PDAs](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

3 Description

The MAX3221 device consists of one line driver, one line receiver with dedicated enable pin, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. These devices operate at data signaling rates up to 250 kbps and a maximum of 30-V/ μ s driver output slew rate.

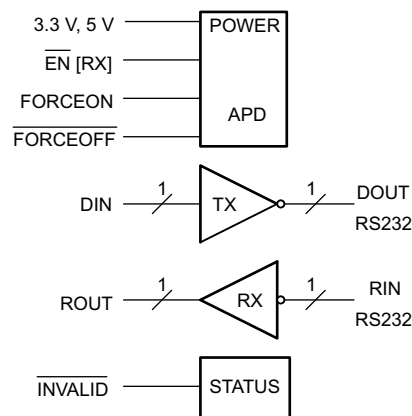
Flexible control options for power management are available when the serial port is inactive. The automatic power-down feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid

RS-232 signal on the receiver input, the driver output is disabled and the supply current is reduced to 1 μ A. The INVALID output notifies the user if an RS-232 signal is present at the receiver input.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
MAX3221	SSOP (DB) (32)	6.20 mm $\times$ 5.30 mm
	TSSOP (PW) (32)	5.00 mm $\times$ 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (June 2015) to Revision P (July 2021)	Page
• Changed the <i>Applications</i> list.....	1
• Changed the values in the <i>Thermal Information</i> table for DB and PW packages.....	5

Changes from Revision N (January 2014) to Revision O (June 2015)	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

Changes from Revision M (March 2004) to Revision N (January 2013)	Page
• Updated document to new TI data sheet format - no specification changes.....	1
• Deleted <i>Ordering Information</i> table.....	1

5 Pin Configuration and Functions

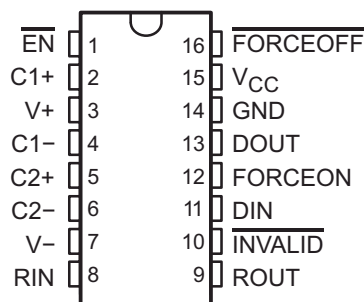


Figure 5-1. DB or PW Package, 16-Pin SSOP or TSSOP, Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2+	5		
C1-	4	—	Negative terminals of the voltage-doubler charge-pump capacitors
C2-	6		
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
EN	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
FORCEOFF	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	—	Ground
INVALID	10	O	Invalid output pin. Output low when all RIN inputs are unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V _{CC}	15	—	3-V to 5.5-V supply voltage
V+	3	O	5.5-V supply generated by the charge pump
V-	7	O	–5.5-V supply generated by the charge pump

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC} to GND			–0.3	6	V
$V+$ to GND			–0.3	7	
$V-$ to GND			0.3	–7	
$V+ + V- $ ⁽²⁾				13	
V_I	Input voltage	DIN, $\overline{EN}$, FORCEOFF, and FORCEON to GND	–0.3	6	V
		RIN to GND		±25	
V_O	Output voltage	DOUT to GND		±13.2	V
		ROUT to GND	–0.3	$V_{CC} + 0.3$	
T_J	Junction temperature ⁽³⁾			150	°C
T_{stg}	Storage temperature range		–65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) $V+$ and $V-$ can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.
- (3) Maximum power dissipation is a function of $T_J(\max)$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except 8, 13 ±3000	V
			Pins 8, 13 ±15,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see Figure 9-1)⁽¹⁾

				MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3$ V		3	3.3	3.6	V
				4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN, FORCEOFF, FORCEON, $\overline{EN}$	$V_{CC} = 3.3$ V	2			V
			$V_{CC} = 5$ V	2.4			
V_{IL}	Driver low-level input voltage	DIN, FORCEOFF, FORCEON, $\overline{EN}$				0.8	V
V_I	Driver input voltage	DIN, FORCEOFF, FORCEON, $\overline{EN}$		0		5.5	V
	Receiver input voltage			–25		25	
T_A	Operating free-air temperature	MAX3221C		0		70	°C
		MAX3221I		–40		85	

- (1) Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V $\pm$ 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V $\pm$ 0.5 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		MAX3221		UNIT
		DB (SSOP)	PW (TSSOP)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	105.8	110.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.9	41.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	57.6	57.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	14.1	4.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	56.8	56.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics – Power

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON, EN			±0.01	±1	μA
I _{CC}	Supply current	Automatic power-down disabled	No load, FORCEOFF and FORCEON at V _{CC}		0.3	1	mA
		Powered off	No load, FORCEOFF at GND		1	10	μA
		Automatic power-down enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded		1	10	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.6 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = GND		5	5.4		V
V _{OL}	Low-level output voltage	D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = V _{CC}		–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}			±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND			±0.01	±1	μA
I _{OS}	Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V	V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V	V _O = 0 V		±35	±60	
r _O	Output resistance	V _{CC} , V+, and V– = 0 V	V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V			±25	μA
			V _O = ±12 V, V _{CC} = 4.5 V to 5.5 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5

6.7 Electrical Characteristics – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1	V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA		0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V	1.5	2.4	V
		V _{CC} = 5 V	1.8	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1	V
		V _{CC} = 5 V	0.8	1.4	
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})		0.5		V
I _{off}	Output leakage current	FORCEOFF = 0 V	±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7 kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.8 Electrical Characteristics – Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{T+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}		2.7	V
V _{T–(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	–2.7		V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	–0.3	0.3	V
V _{OH}	INVALID high-level output voltage	I _{OH} = –1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} – 0.6		V
V _{OL}	INVALID low-level output voltage	I _{OH} = –1 mA, FORCEON = GND, FORCEOFF = V _{CC}		0.4	V

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.9 Switching Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate	C _L = 1000 pF, R _L = 3 kΩ, see Figure 7-1	150	250		kbps
t _{sk(p)}	Pulse skew ⁽²⁾ C _L = 150 to 2500 pF, R _L = 3 kΩ to 7 kΩ, see Figure 7-2		100		ns
SR(tr)	Slew rate, transition region (see Figure 7-1) V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ	C _L = 150 to 1000 pF	6	30	V/μs
		C _L = 150 to 2500 pF	4	30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.10 Switching Characteristics – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$C_L = 150$ pF, see Figure 7-3		150		ns
t_{PHL} Propagation delay time, high- to low-level output	$C_L = 150$ pF, see Figure 7-3		150		ns
t_{en} Output enable time	$C_L = 150$ pF, $R_L = 3$ k Ω , see Figure 7-4		200		ns
t_{dis} Output disable time	$C_L = 150$ pF, $R_L = 3$ k Ω , see Figure 7-4		200		ns
$t_{sk(p)}$ Pulse skew ⁽²⁾	See Figure 7-3		50		ns

(1) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

(3) Test conditions are $C1-C4 = 0.1$ μF at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $C1 = 0.047$ μF , $C2-C4 = 0.33$ μF at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

6.11 Switching Characteristics – Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾

PARAMETER	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{valid} Propagation delay time, low- to high-level output		1		μs
$t_{invalid}$ Propagation delay time, high- to low-level output		30		μs
t_{en} Supply enable time		100		μs

(1) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are $C1-C4 = 0.1$ μF at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $C1 = 0.047$ μF , $C2-C4 = 0.33$ μF at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

6.12 Typical Characteristics

$V_{CC} = 3.3$ V

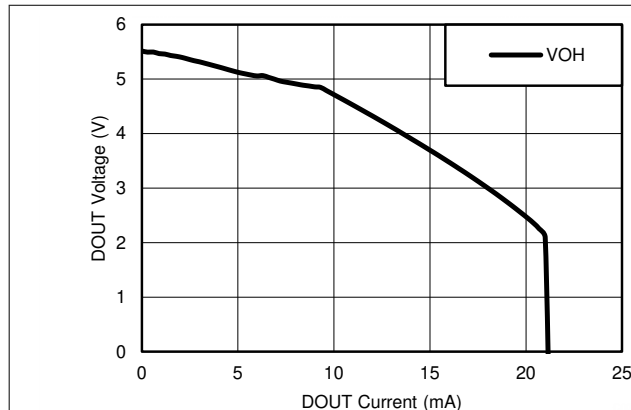


Figure 6-1. DOUT V_{OH} vs Load Current

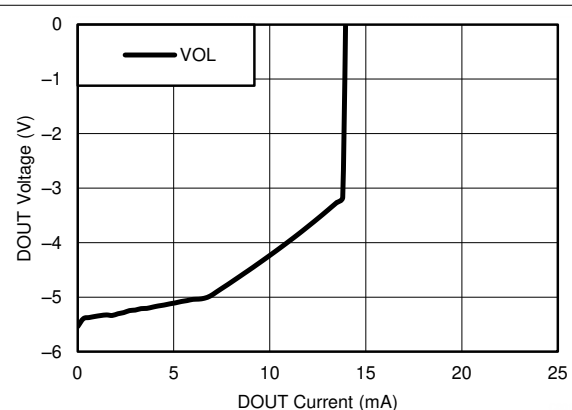
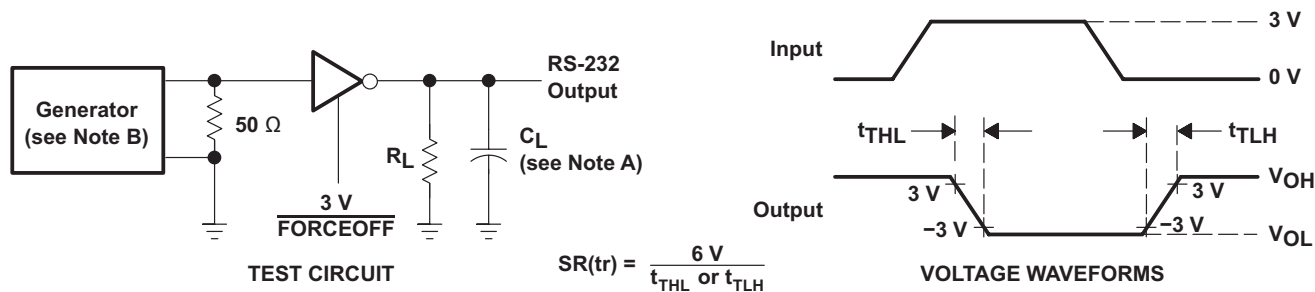


Figure 6-2. DOUT V_{OL} vs Load Current

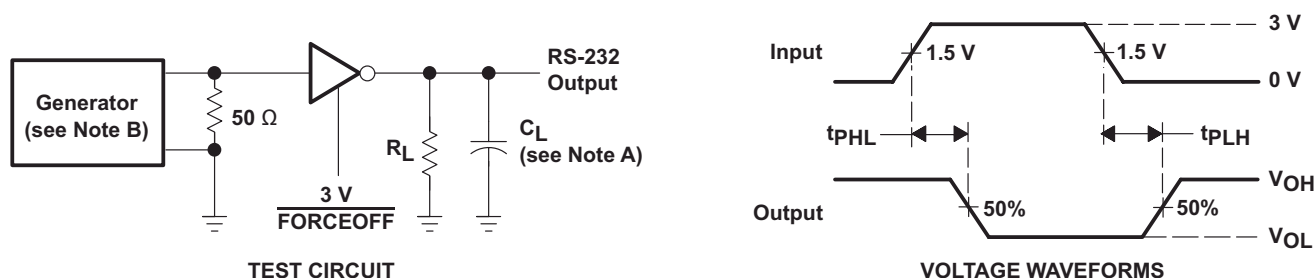
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

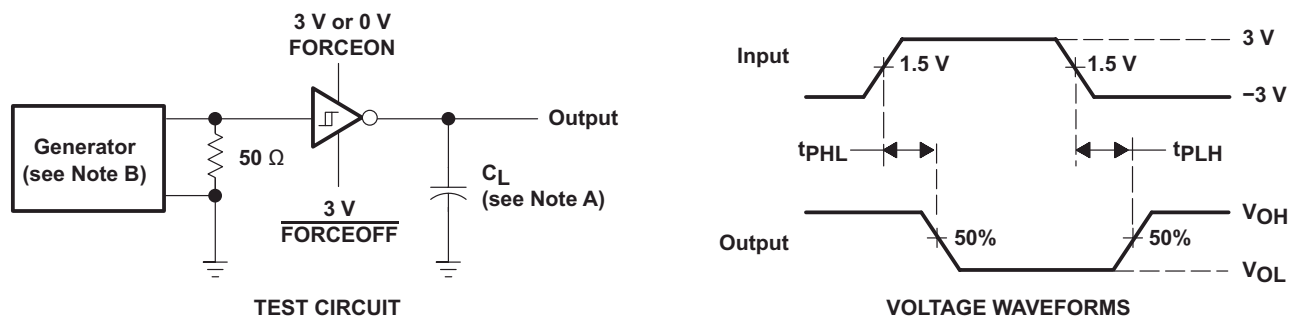
Figure 7-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

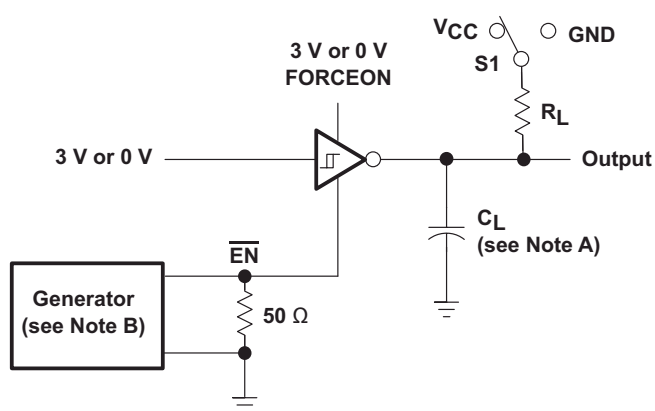
Figure 7-2. Driver Pulse Skew



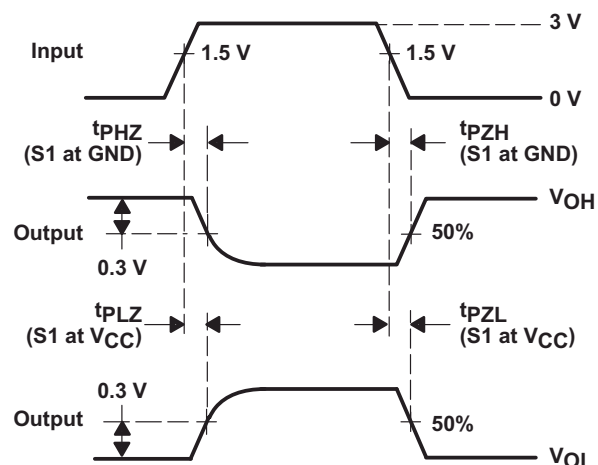
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 7-3. Receiver Propagation Delay Times



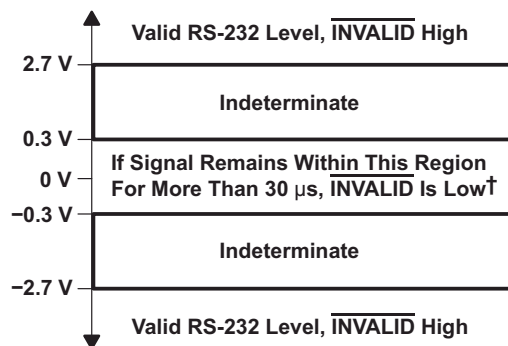
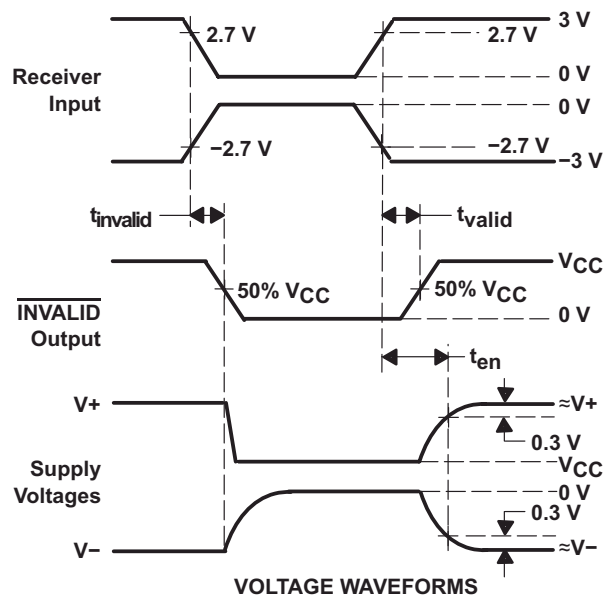
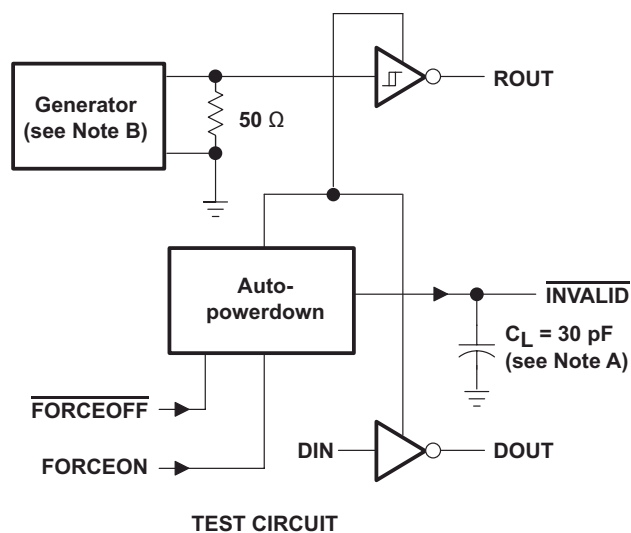
TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 7-4. Receiver Enable and Disable Times



[†] Auto-powerdown disables drivers and reduces supply current to 1 μA .

Figure 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

8 Detailed Description

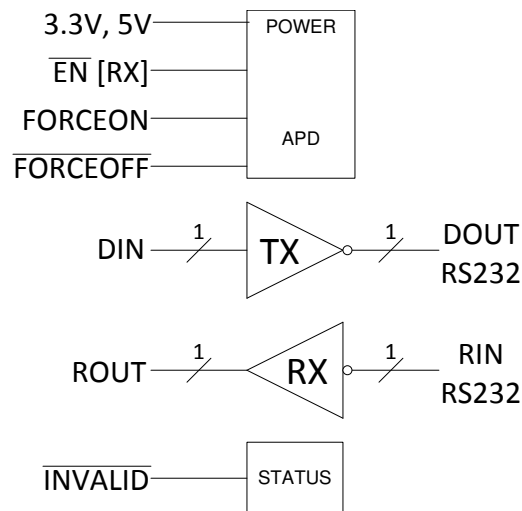
8.1 Overview

The MAX3221 device is a one-driver and one-receiver RS-232 interface device. All RS-232 inputs and outputs are protected to ± 15 kV using the Human Body Model. The charge pump requires only four small 0.1- μ F capacitors for operation from a 3.3-V supply. The MAX3221 is capable of running at data rates up to 250 kbps, while maintaining RS-232-compliant output levels.

Automatic power-down can be disabled when $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ are high. With automatic power-down plus enabled, the device activates automatically when a valid signal is applied to any receiver input. The device can automatically power down the driver to save power when the RIN input is unpowered.

$\overline{\text{INVALID}}$ is high (valid data) if receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. $\overline{\text{INVALID}}$ is low (invalid data) if receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to [Figure 7-5](#) for receiver input levels.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. See [Table 8-1](#) and [Table 8-2](#).

When MAX3221 is unpowered, it can be safely connected to an active remote RS232 device.

8.3.2 RS232 Driver

One driver interfaces standard logic level to RS232 levels. DIN input must be valid high or low.

8.3.3 RS232 Receiver

One receiver interfaces RS232 levels to standard logic levels. An open input will result in a high output on ROUT. RIN input includes an internal standard RS232 load. A logic high input on the $\overline{\text{EN}}$ pin will shutdown the receiver output.

8.3.4 RS232 Status

The $\overline{\text{INVALID}}$ output goes low when RIN input is unpowered for more than 30 μ s. The $\overline{\text{INVALID}}$ output goes high when receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when V_{CC} is powered regardless of $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ inputs (see [Table 8-3](#)).

8.4 Device Functional Modes

Table 8-1, Table 8-2, and Table 8-3 show the behavior of the driver, receiver, and INVALID(active-low) features under all possible relevant combinations of inputs.

Table 8-1. Driver⁽¹⁾

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with automatic power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by automatic power down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, Yes = $|RIN| > 2.7\text{ V}$, No = $|RIN| < 0.3\text{ V}$

Table 8-2. Receiver⁽¹⁾

INPUTS			OUTPUT	RECEIVER STATUS
RIN	EN	VALID RIN RS-232 LEVEL	ROUT	
X	H	X	Z	Output off
L	L	X	H	Normal operation
H	L	X	L	
Open	L	No	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 8-3. INVALID⁽¹⁾

INPUTS				OUTPUT
RIN	FORCEON	FORCEOFF	EN	INVALID
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

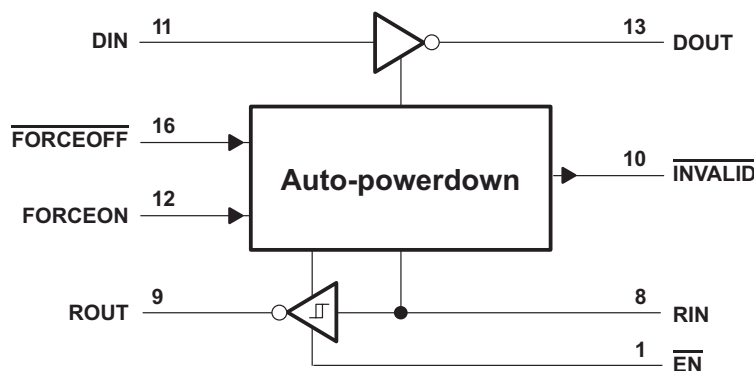


Figure 8-1. Logic Diagram

9 Application and Implementation

Note

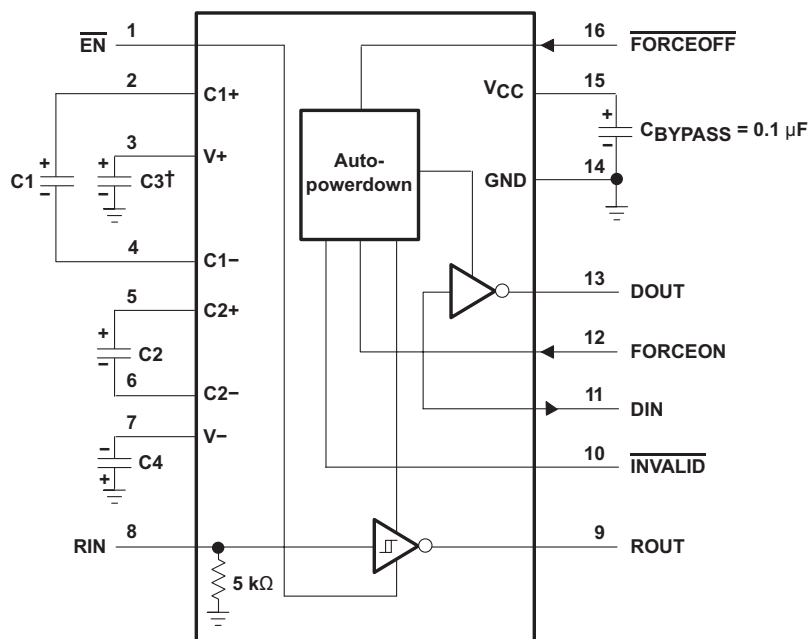
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The MAX3221 line driver and receiver is a specialized device for 3-V to 5.5-V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in [Figure 9-1](#).

9.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC} . $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 9-1. Typical Operating Circuit and Capacitor Values

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V.
 - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbps.
- Use capacitors as shown in [Figure 9-1](#).

9.2.2 Detailed Design Procedure

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

Curves for V_{CC} of 3.3 V and 250 kbps alternative bit data stream.

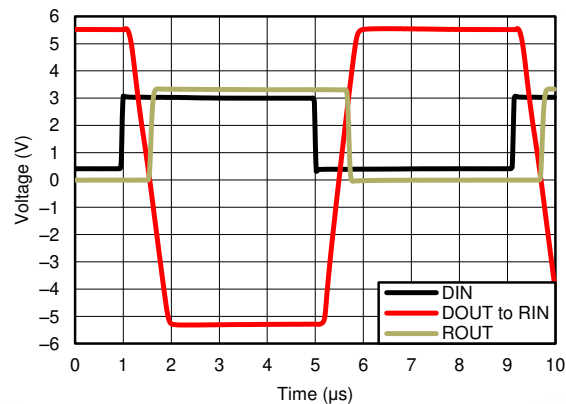


Figure 9-2. 250-kbps Driver to Receiver Loopback Timing Waveform, $V_{CC} = 3.3 \text{ V}$

10 Power Supply Recommendations

TI recommends a 0.1- μF capacitor to filter noise on the power supply pin. For additional filter capability, a 0.01- μF capacitor may be added in parallel as well. Power supply input voltage is recommended to be any valid level in [Recommended Operating Conditions](#).

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

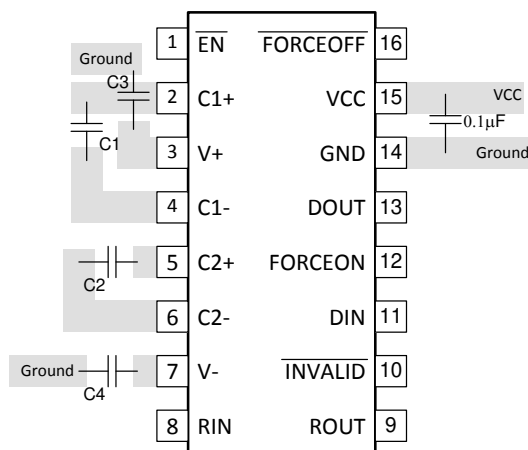


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3221CDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C
MAX3221CDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C
MAX3221CDBRG4	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C
MAX3221CPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C
MAX3221CPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C
MAX3221CPWRE4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C
MAX3221CPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C
MAX3221IDBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I
MAX3221IDBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I
MAX3221IDBRE4	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I
MAX3221IDBRG4	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I
MAX3221IPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	MB3221I
MAX3221IPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I
MAX3221IPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I
MAX3221IPWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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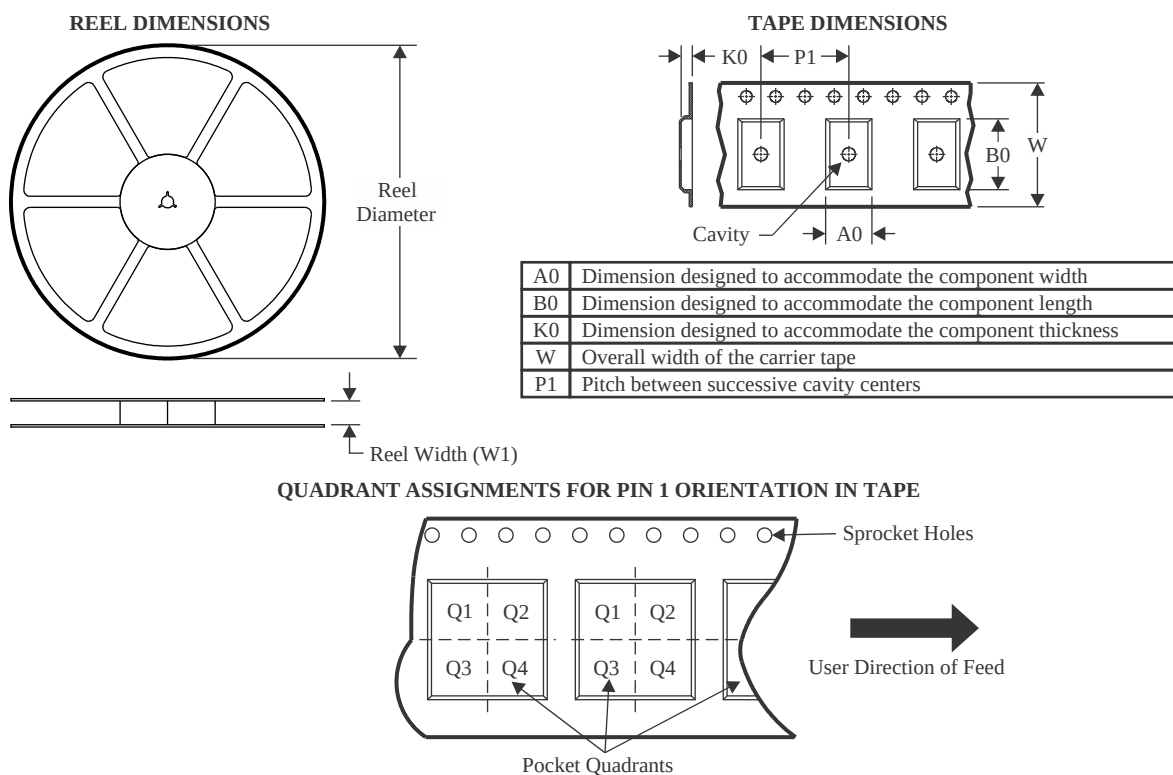
OTHER QUALIFIED VERSIONS OF MAX3221 :

- Enhanced Product : [MAX3221-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

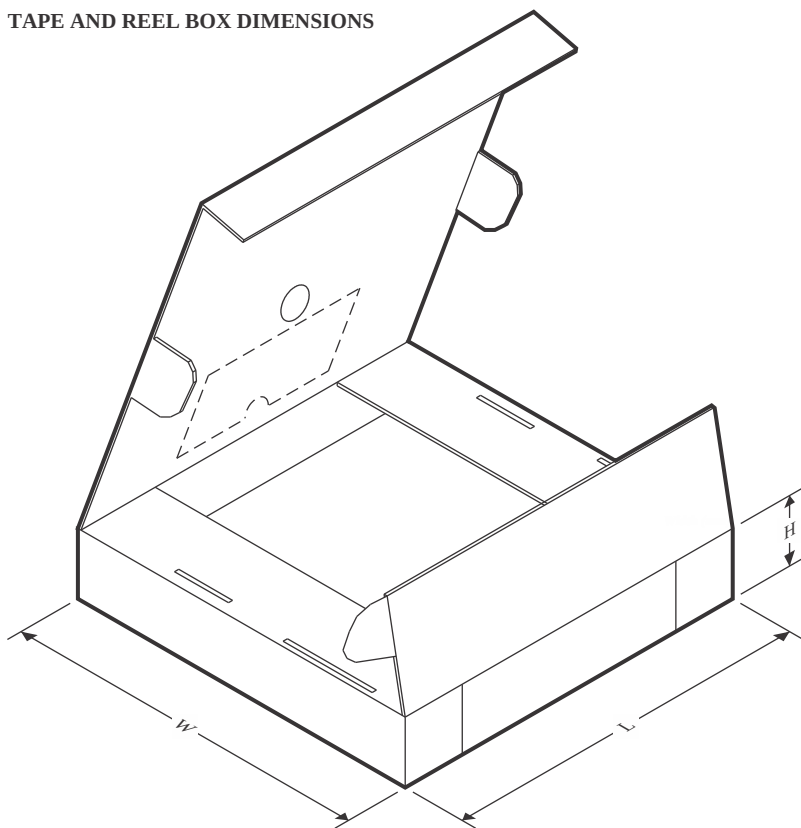
TAPE AND REEL INFORMATION



*All dimensions are nominal

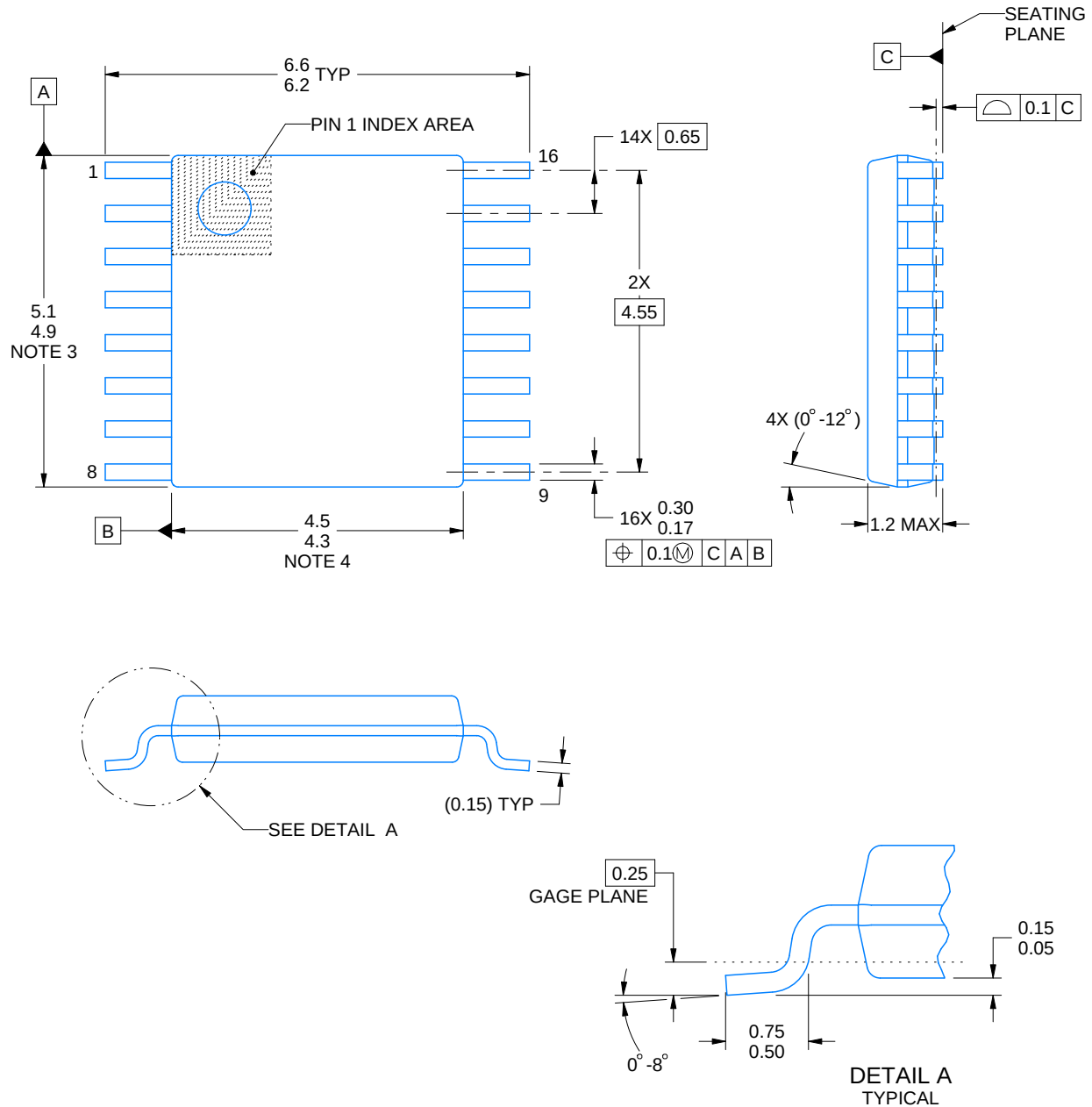
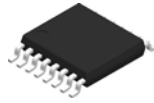
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3221CDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
MAX3221IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3221CDBR	SSOP	DB	16	2000	353.0	353.0	32.0
MAX3221CPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3221IDBR	SSOP	DB	16	2000	353.0	353.0	32.0
MAX3221IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX3221IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3221IPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX3221IPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0



4220204/B 12/2023

NOTES:

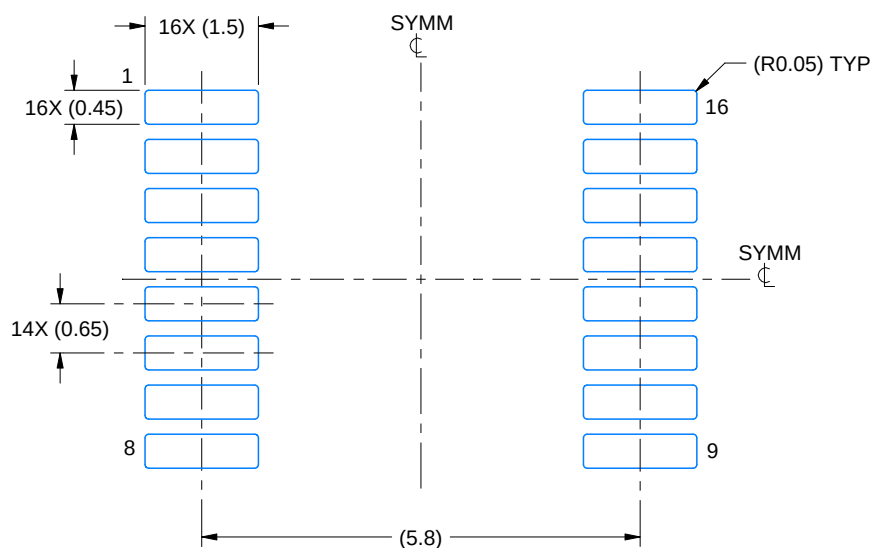
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

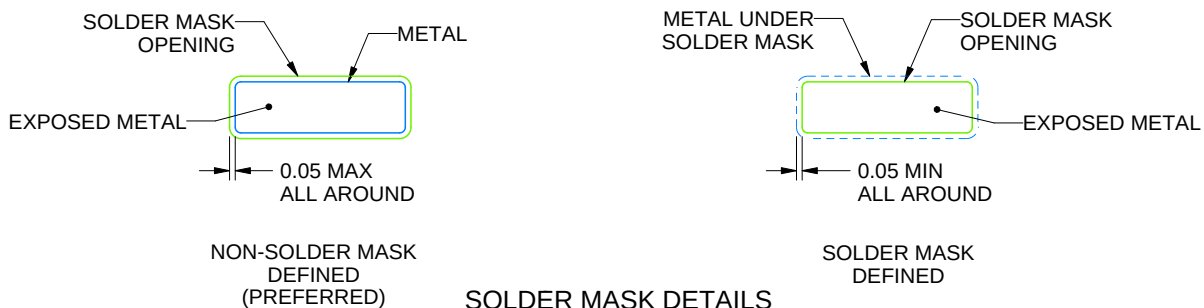
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

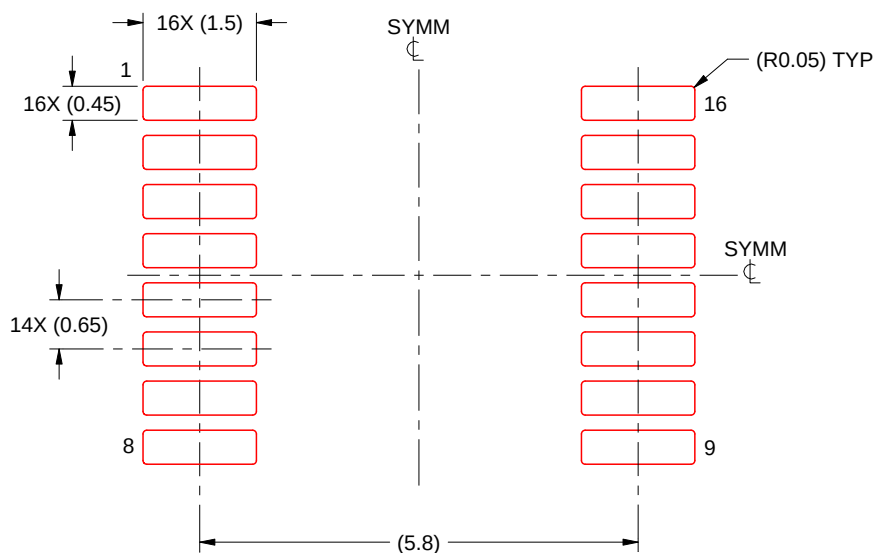
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

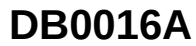


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



SSOP - 2 mm max height

Technical drawing of a 16-pin connector, showing top, side, and detail views.

Top View:

- Overall width: 8.2 TYP, 7.4
- Overall height: 6.5, 5.9 (NOTE 3)
- Pin 1 Index Area: Indicated by a circle and dashed lines.
- Pin 1: Located at the top left corner.
- Pin 16: Located at the top right corner.
- Pin 8: Located at the bottom left corner.
- Pin 9: Located at the bottom right corner.
- Pin 14: Located at the top right, 14X 0.65.
- Pin 2: Located at the bottom right, 2X 4.55.
- Pin 16: Located at the bottom right, 16X 0.38, 0.22.
- Pin 5.6, 5.0 (NOTE 4): Dimension across the bottom pins.
- Feature Control Frame: $\oplus$ 0.1 M C A B

Side View:

- Seating Plane: Indicated by a dashed line.
- Feature Control Frame: C 0.1 C

Detail A (Typical):

- Feature Control Frame: 0.25, 0.09
- Gage Plane: Indicated by a dashed line.
- Angle: $0^\circ - 8^\circ$
- Dimensions: 0.95, 0.55, 2 MAX, 0.05 MIN

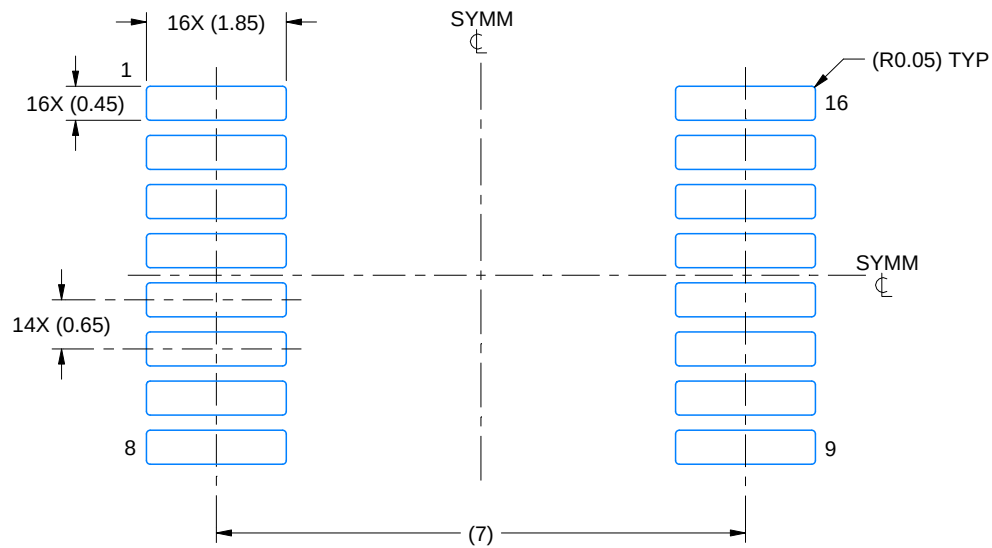
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

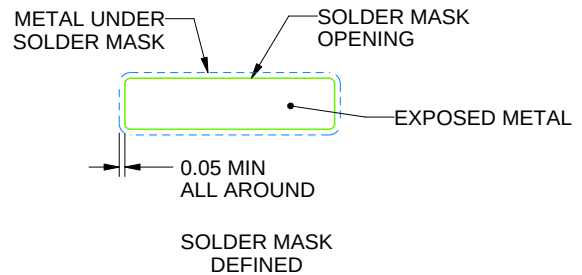
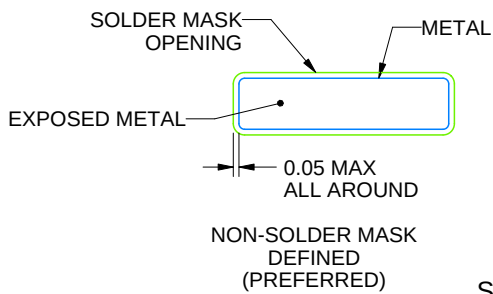
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

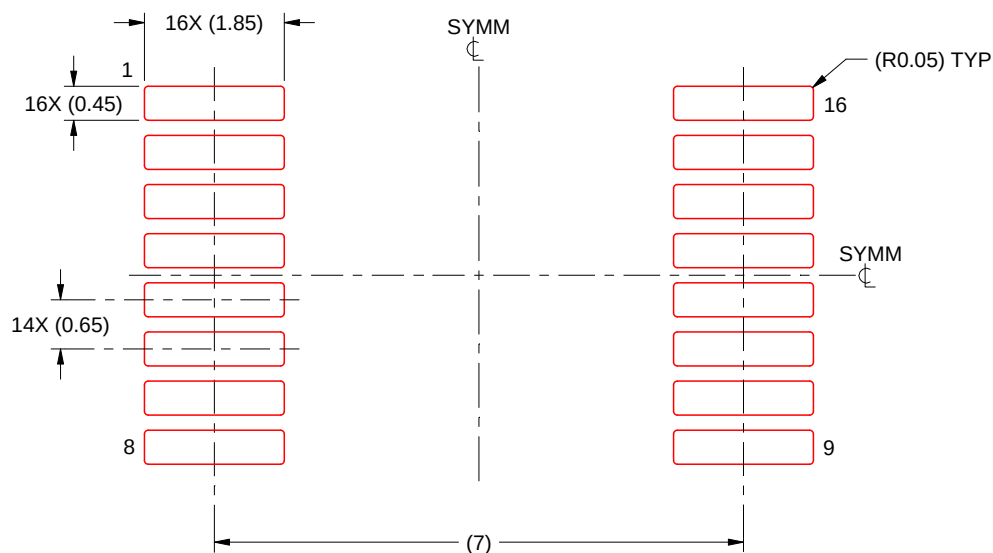
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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