MAX3222 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ±15-kV ESD Protection

1 Features

- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up to 250 kbps
- Two Drivers and Two Receivers
- Low Standby Current: 1 µA Typical
- External Capacitors: 4 × 0.1 µF
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbps)
  - SNx5C3222

2 Applications

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-held Equipment

3 Description

The MAX3222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

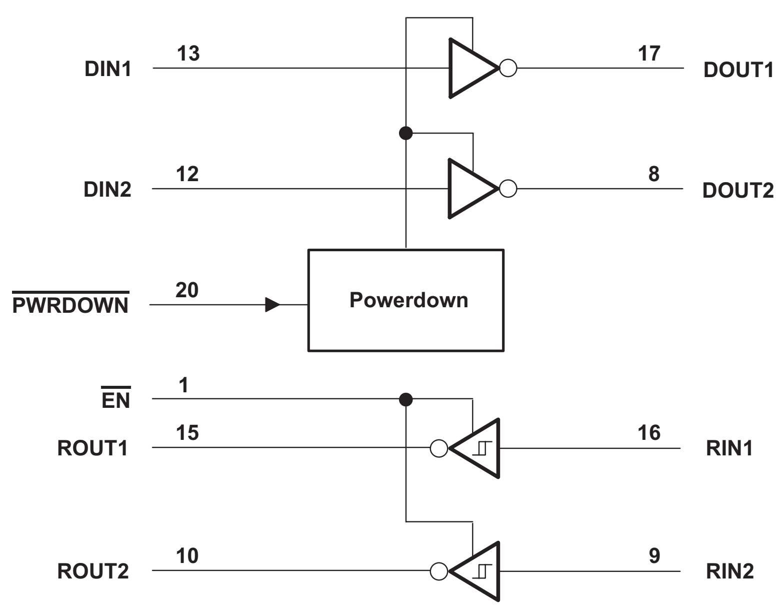
The MAX3222 can be placed in the power-down mode by setting $\overline{\text{PWRDOWN}}$ low, which draws only 1 µA from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Receiver outputs also can be placed in the high-impedance state by setting $\overline{\text{EN}}$ high.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MAX3222CDW, MAX322IDW	SOIC (20)	12.80 mm × 7.50 mm
MAX3222CDB, MAX322IDB	SSOP (20)	7.20 mm × 5.30 mm
MAX3222CPW, MAX322IPW	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

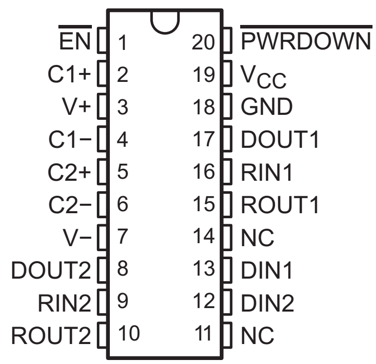
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2004) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *ODERING INFORMATION* table; see POA at the end of the datasheet. ... 3
- Changed $R_{\theta JA}$ for DB, DW and PW package from: 70 °C/W to 84.4°C/W (DB), 58 °C/W to 70.2 °C/W (DW) and 83 °C/W to 94.3 °C/W (PW) in the *Thermal Information* table. ... 5

5 Pin Configuration and Functions

DB, DW, or PW Package
20-Pin SOIC, SSOP, TSSOP
Top View



NC − No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	2	—	Charge pump capacitor pin
C1-	4	—	Charge pump capacitor pin
C2+	5	—	Charge pump capacitor pin
C2-	6	—	Charge pump capacitor pin
DIN1	13	I	Driver logic input
DIN2	12	I	Driver logic input
DOUT1	17	O	RS-232 driver output
DOUT2	8	O	RS-232 driver output
$\overline{\text{EN}}$	1	I	Receiver enable, active low
GND	18	—	Ground
NC	11,14	—	No internal connection
$\overline{\text{PWRDOWN}}$	20	I	Driver disable, active low
RIN1	16	I	RS-232 receiver input
RIN2	9	I	RS-232 receiver input
ROUT1	15	O	Receiver logic output
ROUT2	10	O	Receiver logic output
V_{CC}	19	—	Power Supply
V+	3	—	Charge pump capacitor pin
V-	7	—	Charge pump capacitor pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{CC} [2]		–0.3	6	V
Positive output supply voltage, V+ [2]		–0.3	7	V
Negative output supply voltage, V– [2]		0.3	-7	V
Supply voltage difference, V+ – V–			13	V
Input voltage, V_I	Drivers, $\overline{EN}$, $\overline{PWRDOWN}$	–0.3	6	V
	Receiver	–25	25	
Output voltage, V_O	Drivers	–13.2	13.2	V
	Receivers	–0.3	V_{CC} + 0.3	
Operating virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN, DOUT, and GND pins [1]	Pins 8, 9, 16, 17 and 18	±15000	V
			All other pins	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]. See Figure 8.

				MIN	NOM	MAX	UNIT
	Supply voltage	V_{CC} = 3.3 V		3	3.3	3.6	V
		V_{CC} = 5 V		4.5	5	5.5	
VIH	Driver and control high-level input voltage	DIR, $\overline{EN}$, $\overline{PWRDOWN}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
VIL	Driver and control low-level input voltage	DIR, $\overline{EN}$, $\overline{PWRDOWN}$				0.8	V
VI	Driver and control input voltage	DIR, $\overline{EN}$, $\overline{PWRDOWN}$		0		5.5	V
VI	Receiver input voltage			–25		25	V
TA	Operating free-air temperature	MAX3222C		0		70	ºC
		MAX3222I		–40		85	

(1) Test conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC [1][2][3]		MAX3222 DB (SSOP) 20 PINS	MAX3222 DW (SOIC) 20 PINS	MAX3222 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.4	70.2	94.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.1	36.2	29.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40	37.9	45.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	11.1	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.5	37.5	44.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics: Device

over operating free-air temperature range (unless otherwise noted)[1]. See Figure 8.

PARAMETER		TEST CONDITIONS	MIN	TYP [2]	MAX	UNIT
II	Input leakage current ($\overline{EN}$, PWRDOWN)			±0.01	±1	µA
I_{CC}	Supply current	No load, $\overline{PWRDOWN}$ at V_{CC}		0.3	1	mA
	Supply current (powered off)	No load, $\overline{PWRDOWN}$ at GND		1	10	µA

(1) Test conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.6 Electrical Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)[1]. See Figure 8.

PARAMETER		TEST CONDITIONS	MIN	TYP [2]	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND, DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND, DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	$V_I = V_{CC}$		±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND		±0.01	±1	µA
I_{OS}	Short-circuit output current	V_{CC} = 3.6 V, V_O = 0 V V_{CC} = 5.5 V, V_O = 0 V		±35	±60	mA
r_o	Output resistance	V_{CC}, V+, and V– = 0 V, V_O = ±2 V	300	10M		Ω
I_{off}	Output leakage current	$\overline{PWRDOWN}$ = GND, V_O = ±12 V, V_{CC} = 3 V to 3.6 V			±25	µA
		$\overline{PWRDOWN}$ = GND, V_O = ±10 V, V_{CC} = 4.5 V to 5.5 V			±25	

(1) Test conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.7 Electrical Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)[1]. See Figure 8.

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.3		V
I_{off}	Output leakage current	$\overline{EN}$ = V_{CC}		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Switching Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)[1]. See Figure 8.

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, R_L = 3 kΩ, One DOUT switching, see Figure 3		150	250		kbps
$t_{sk(p)}$	Pulse skew[3]	C_L = 150 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ, see Figure 4			300		ns
SR(tr)	Slew rate, transition region (see Figure 3)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as |tPLH − tPHL| of each channel of the same device.

6.9 Switching Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)[1]. See Figure 8.

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, see Figure 5		300		ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, see Figure 5		300		ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, see Figure 6		200		ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, see Figure 6		200		ns
$t_{sk(p)}$	Pulse skew[3]	See Figure 5		300		ns

(1) Test conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as |tPLH − tPHL| of each channel of the same device.

6.10 Typical Characteristics

T_A = 25° C; V_{CC} = 3.3V

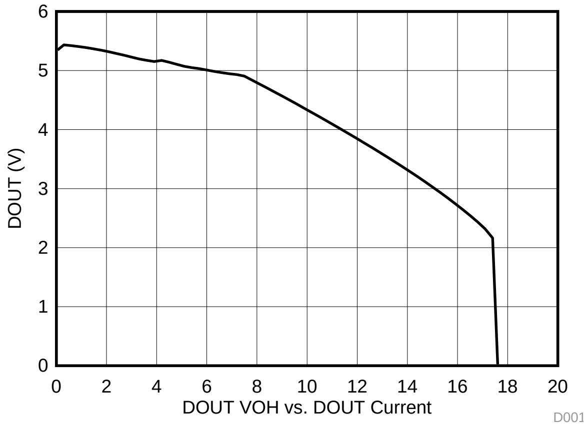


Figure 1. Driver VOH vs Load Current

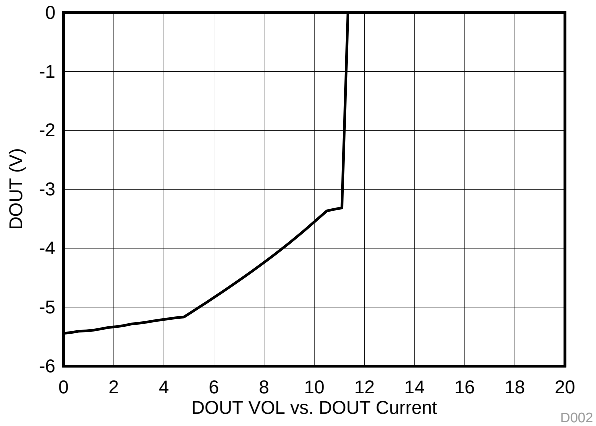
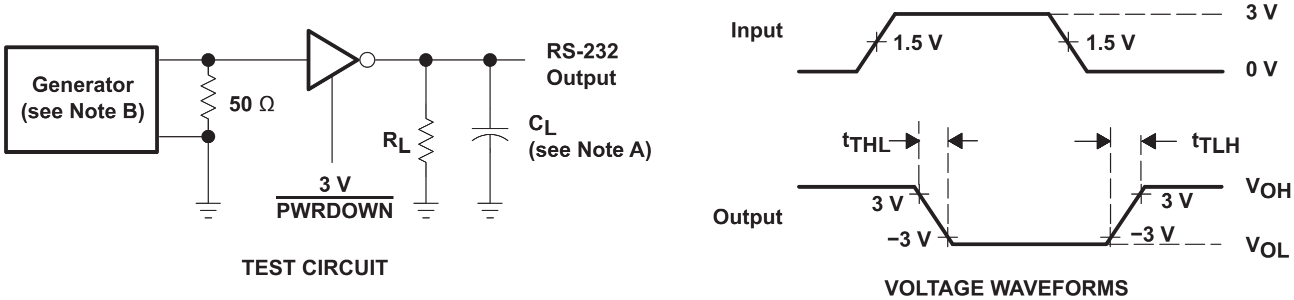


Figure 2. Driver VOL vs Load Current

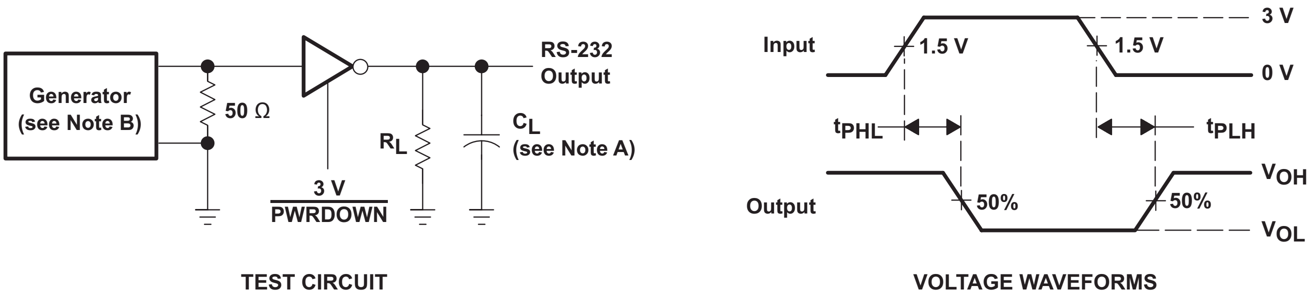
7 Parameter Measurement Information



$$SR(tr) = \frac{6\ V}{t_{THL}\ \text{or}\ t_{TLH}}$$

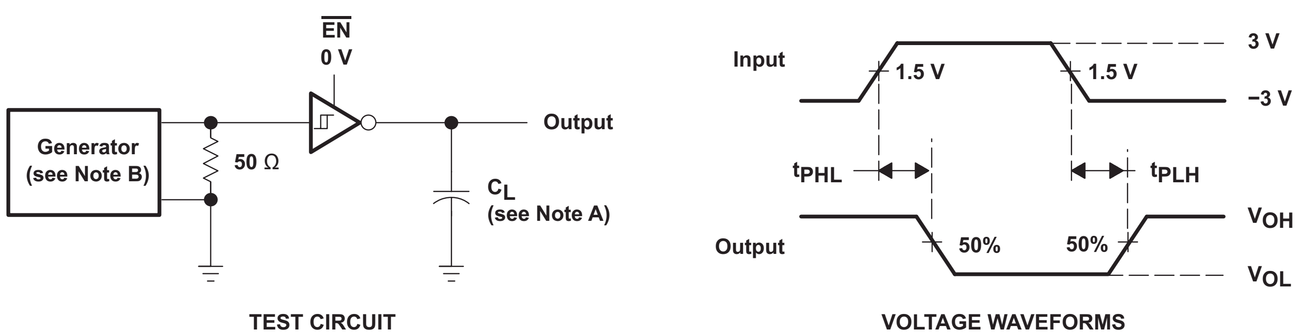
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 3. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

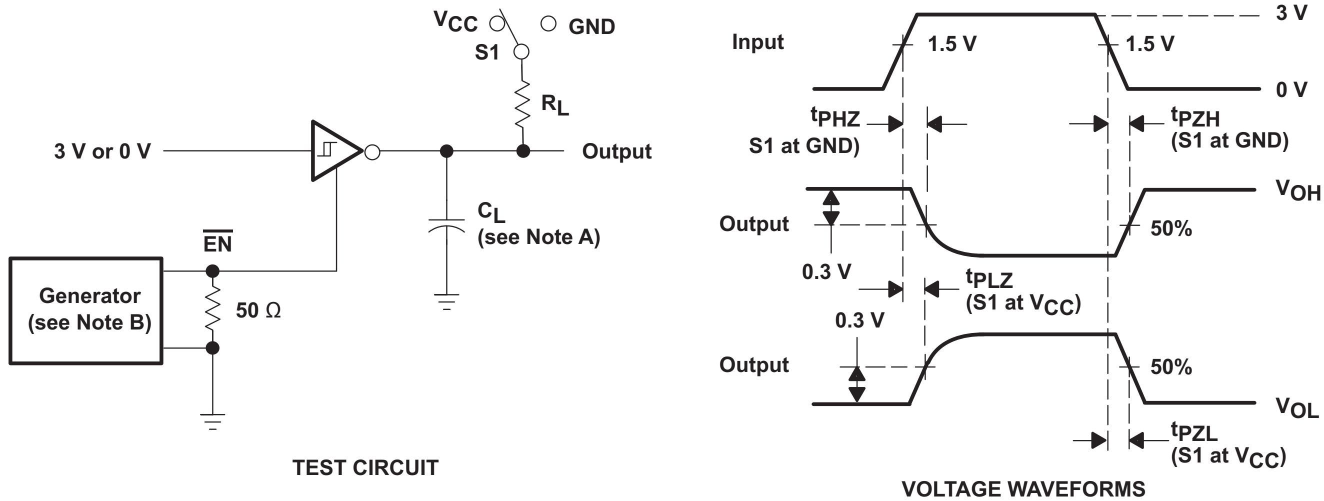
Figure 4. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. Receiver Propagation Delay Times

Parameter Measurement Information (continued)



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 6. Receiver Enable and Disable Times

8 Detailed Description

8.1 Overview

The MAX3222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew rate.

The MAX3222 can be placed in the power-down mode by setting $\overline{\text{PWRDOWN}}$ low, which draws only 1 μA from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; V+ is lowered to V_{CC}, and V− is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting EN high.

8.2 Functional Block Diagram

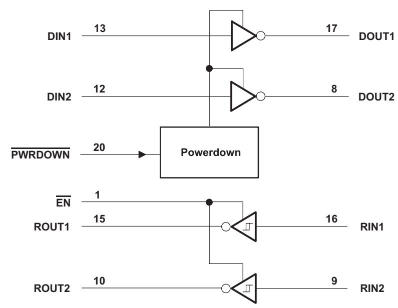


Figure 7. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors.

8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. $\overline{\text{PWRDOWN}}$ input low turns driver off and $\overline{\text{PWRDOWN}}$ input high turns driver on. Both DIN inputs and $\overline{\text{PWRDOWN}}$ input must be valid high or low. Do not float logic input pins.

8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load. $\overline{\text{EN}}$ input low turns on both ROUT pins. $\overline{\text{EN}}$ input high puts both ROUT pins into high impedance state, output off. $\overline{\text{EN}}$ input must be valid high or low. Do not float logic input pins.

8.4 Device Functional Modes

Driver and receiver outputs are controlled by the functional truth tables.

Table 1. Functional Table - Each Driver(1)

INPUTS		OUTPUT DOUT
DIN	$\overline{\text{PWRDOWN}}$	
X	L	Z
L	H	H
H	H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 2. Functional Table - Each Receiver(1)

INPUTS		OUTPUT ROUT
RIN	$\overline{\text{EN}}$	
L	L	H
H	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

9 Application and Implementation

NOTE

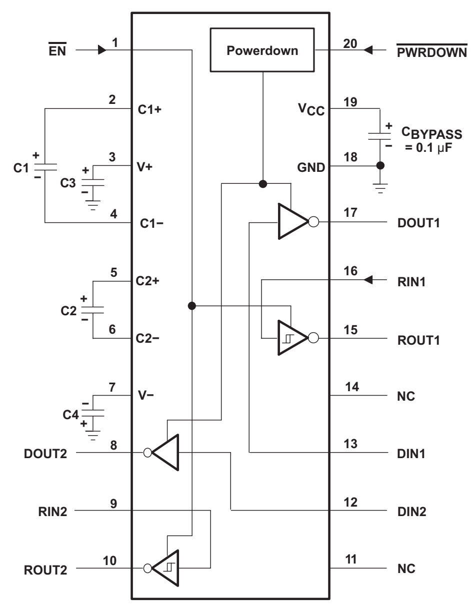
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MAX3222 interfaces a universal asynchronous receiver / transmitter (UART) to RS-232 port voltage levels. External capacitors are used to generate RS-232 compliant voltages. For proper operation, add capacitors as shown in Figure 8.

9.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



C3 can be connected to V_{CC} or GND.

Resistor values shown are nominal.

NC − No internal connection

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 8. Recommended Application Schematic

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V. 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbit/s.

Table 3. V_{CC} vs Capacitor Values

VCC	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V ± 5.5 V	0.1 µF	0.47 µF

9.2.2 Detailed Design Procedure

- All DIN, $\overline{\text{PWRDOWN}}$ and $\overline{\text{EN}}$ inputs must be connected to valid low or high logic levels.
- Select capacitor values based on VCC level for best performance.

9.2.3 Application Curves

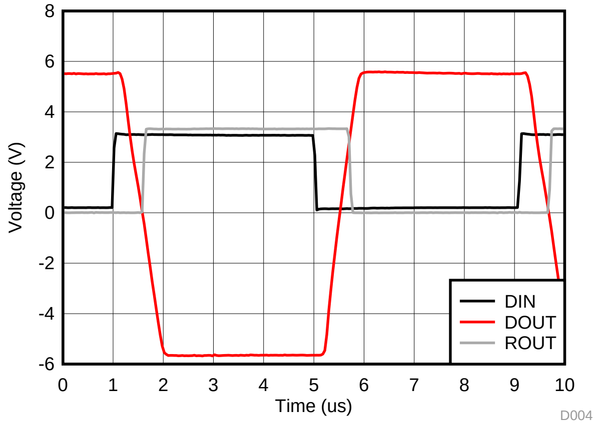


Figure 9. Loopback Waveforms
V_{CC} = 3.3 V, Data Rate 250 kbit/s

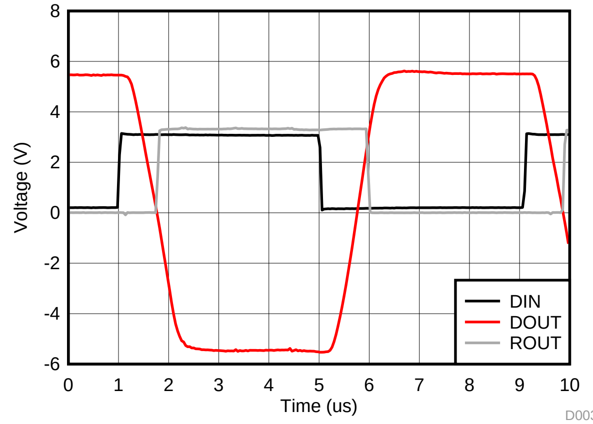


Figure 10. Loopback Waveforms with 1-nF load
V_{CC} = 3.3 V, Data Rate 250 kbit/s

10 Power Supply Recommendations

V_{CC} should be between 3 V and 5.5 V. Charge pump capacitors should be chosen using table in Table 3.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX3222 ground pin and circuit board's ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin

11.2 Layout Example

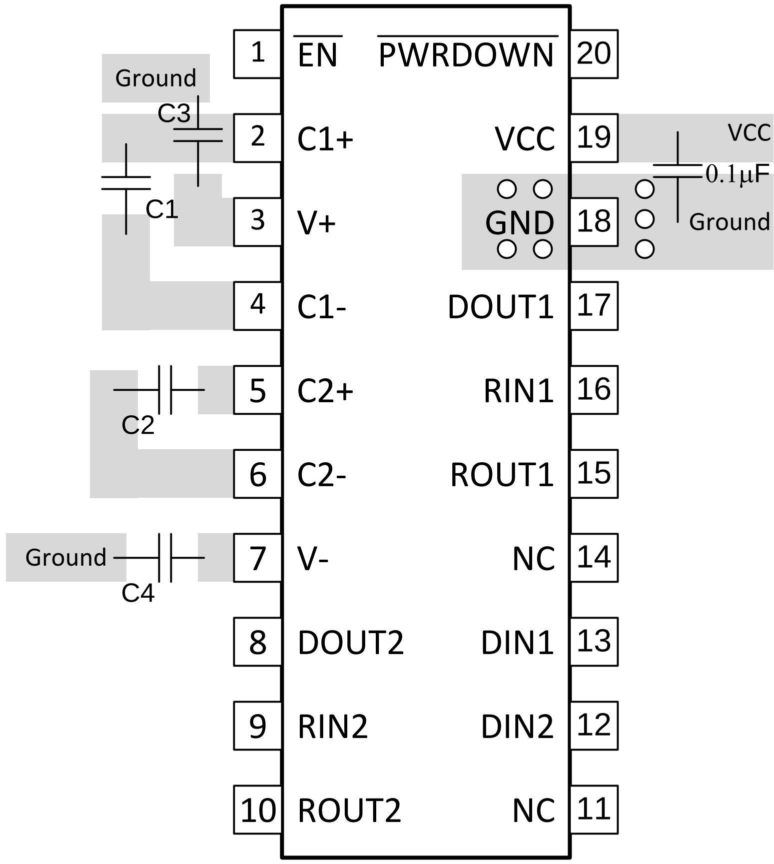


Figure 11. MAX3222 Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3222CDW	NRND	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222C	
MAX3222CDWR	NRND	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222C	
MAX3222CPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222IDW	NRND	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222I	
MAX3222IDWR	NRND	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222I	
MAX3222IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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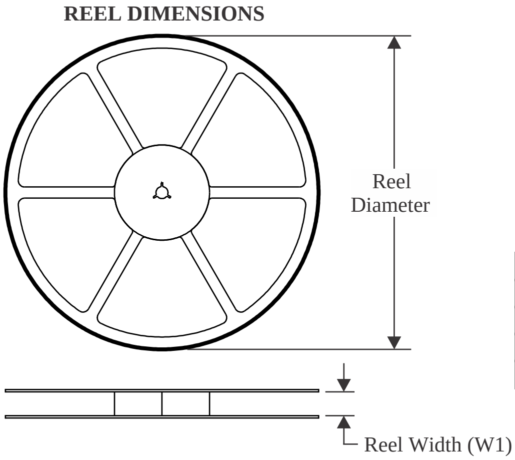
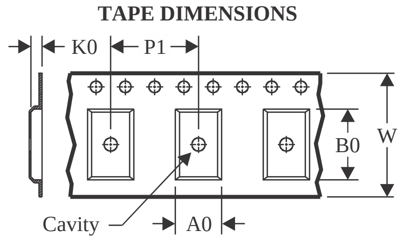
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

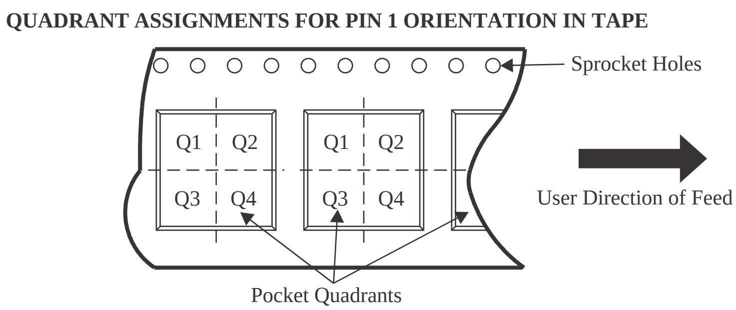
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





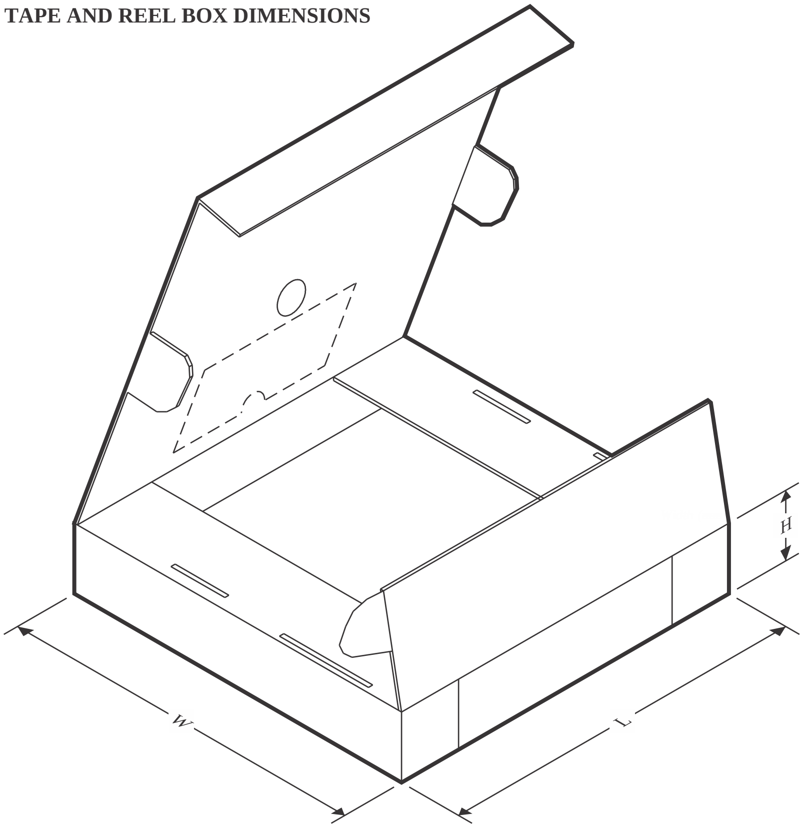
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3222CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3222CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
MAX3222CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MAX3222IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3222IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

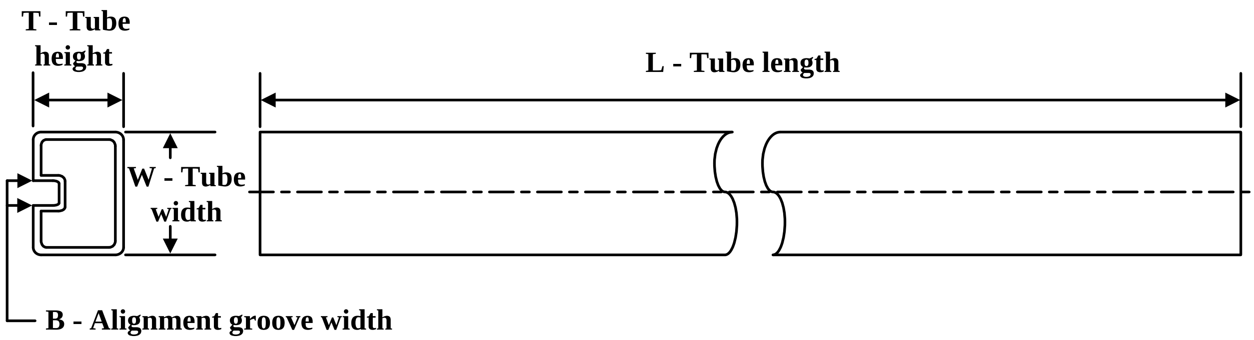
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

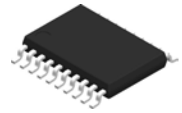
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3222CDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3222CPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MAX3222CPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MAX3222IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3222IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

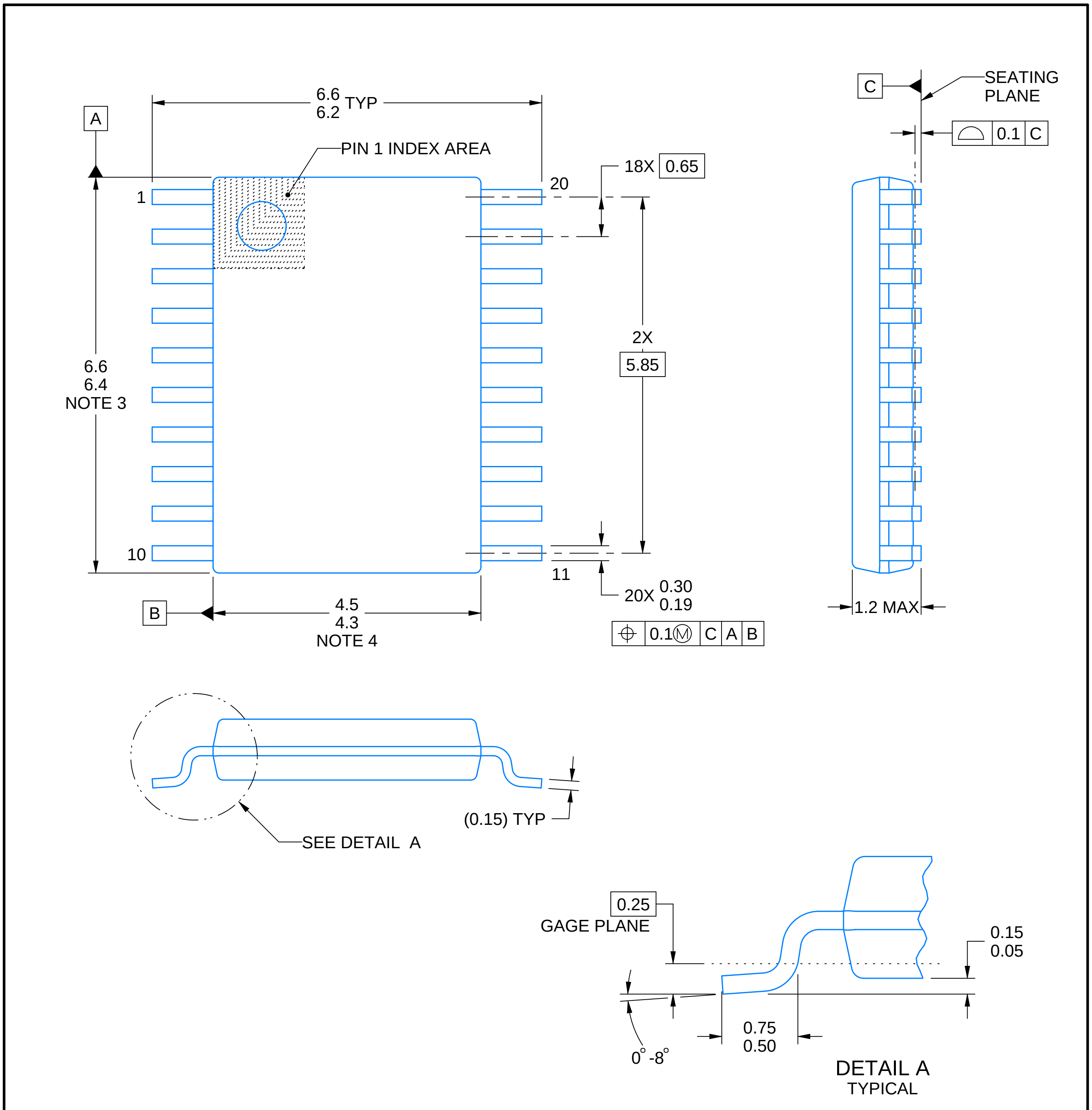
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX3222CDW	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3222IDW	DW	SOIC	20	25	507	12.83	5080	6.6



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

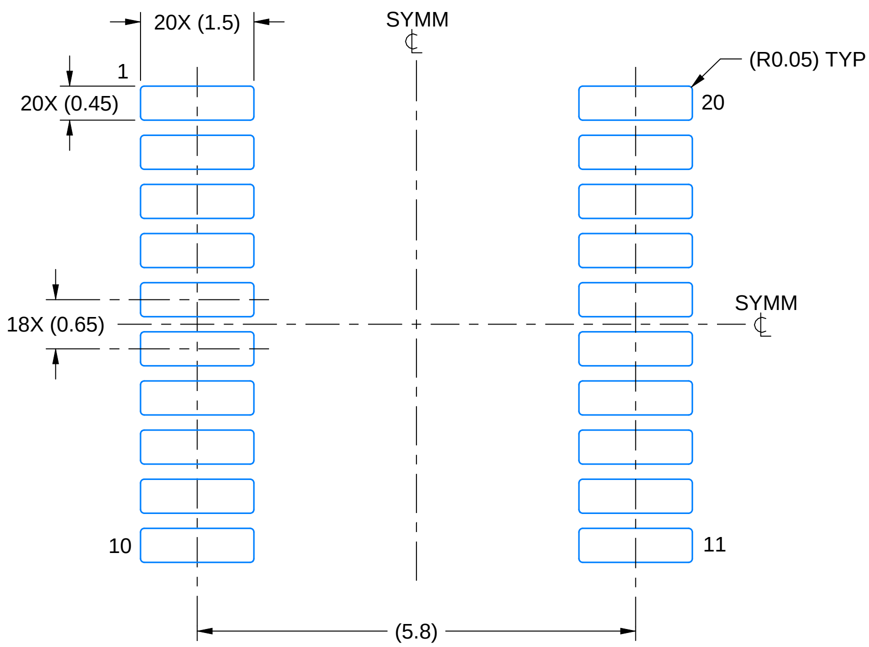
SMALL OUTLINE PACKAGE



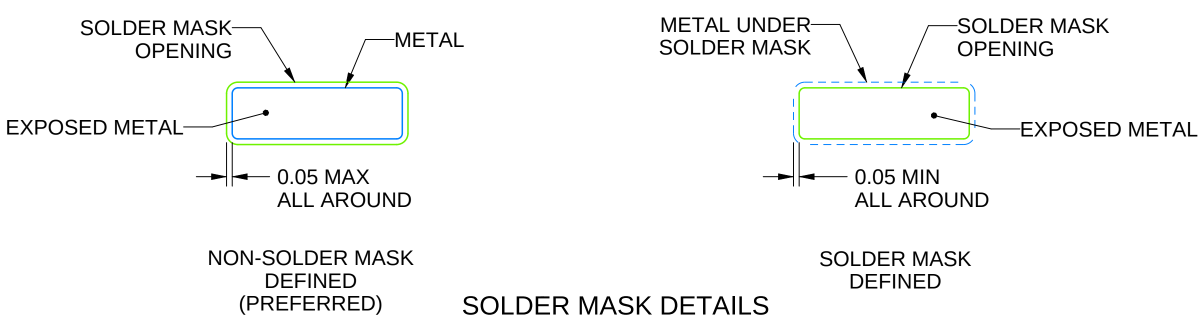
4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

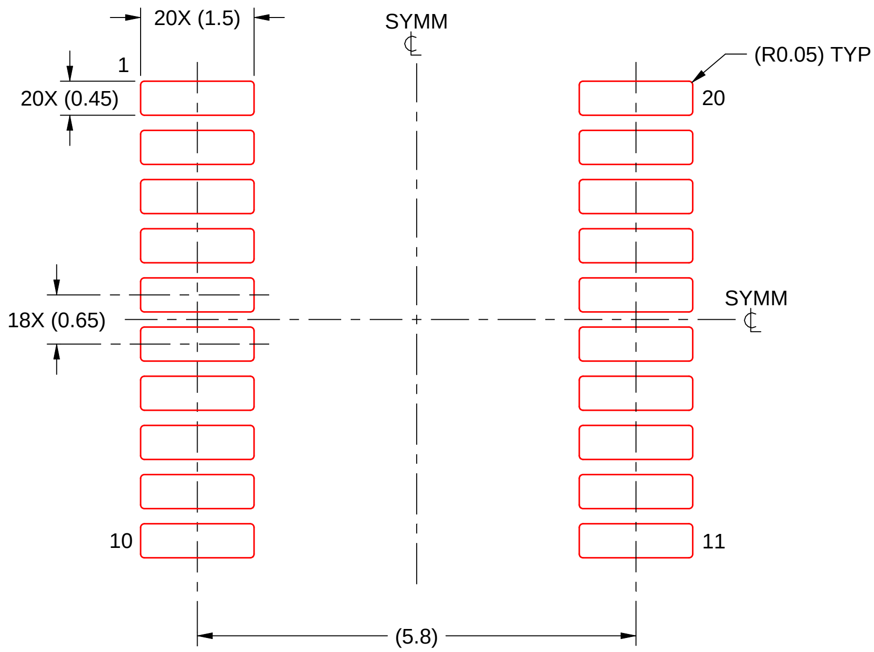


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

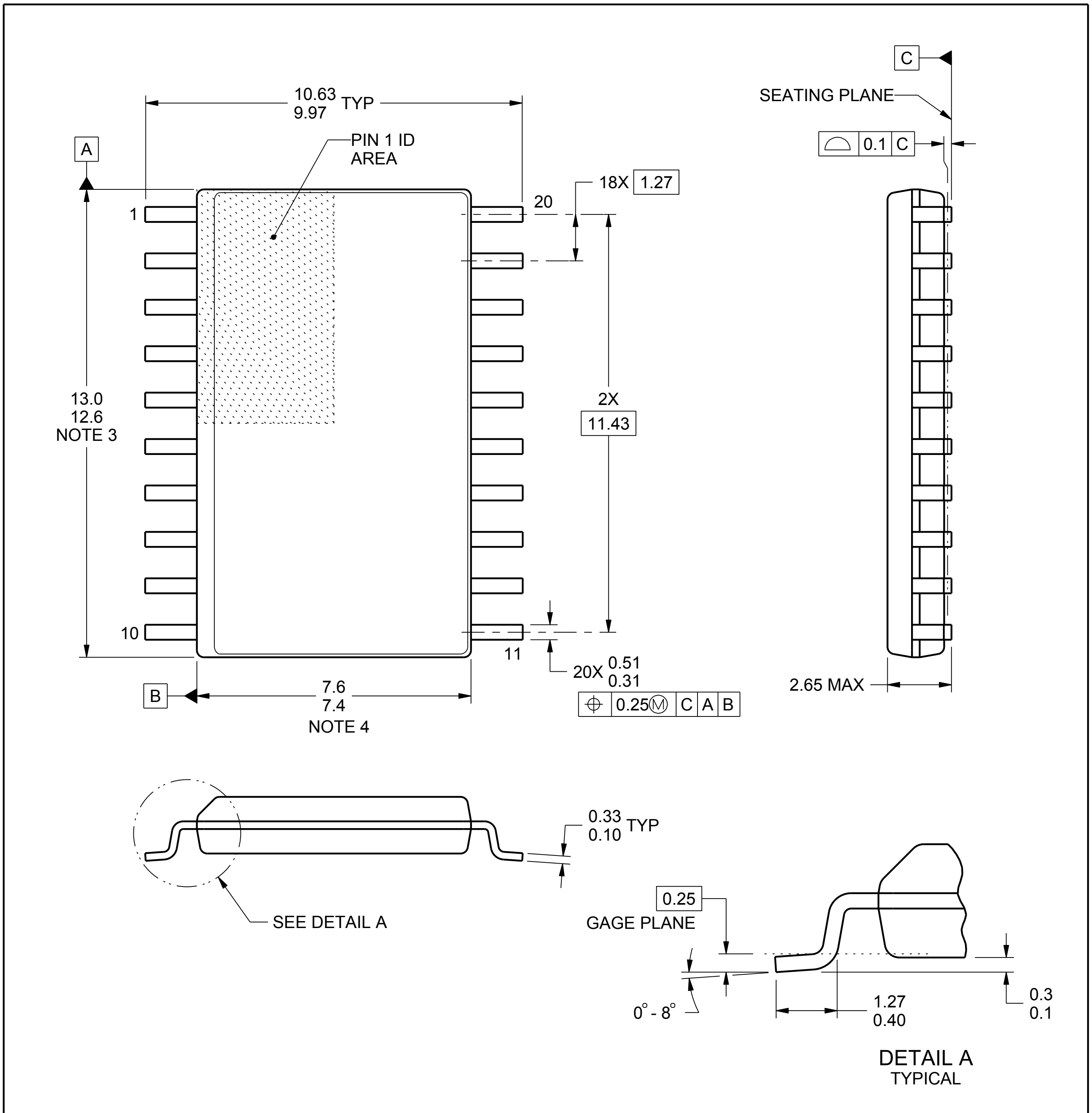


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

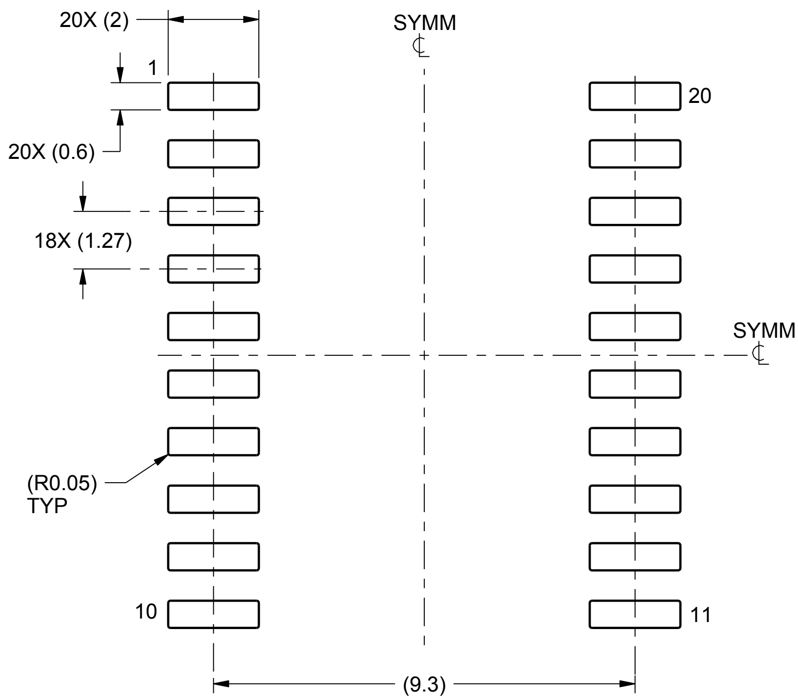
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



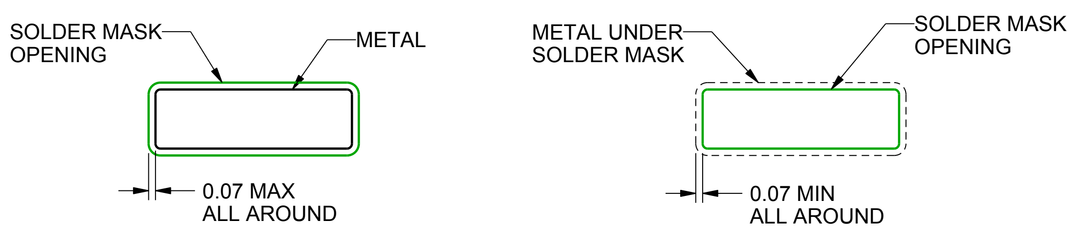
4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

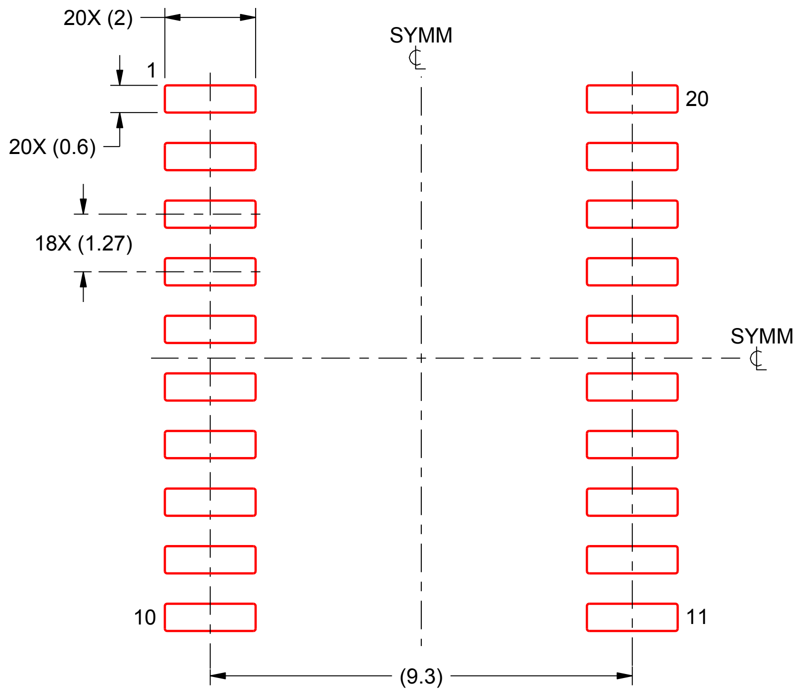
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.