



MPY100

MULTIPLIER-DIVIDER

FEATURES

- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- NO EXTERNAL TRIMMING REQUIRED
- LOW NOISE: 90 μ Vrms, 10Hz to 10kHz
- HIGHLY RELIABLE ONE-CHIP DESIGN
- DIP OR TO-100 TYPE PACKAGE
- WIDE TEMPERATURE OPERATION

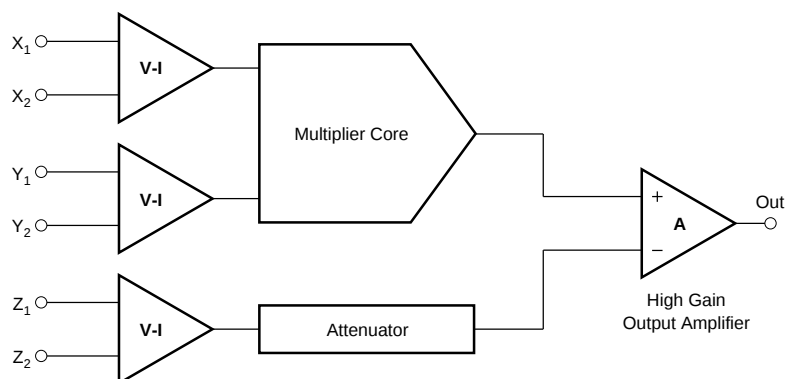
APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The MPY100 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers or potentiometers. Laser-trimmed one-chip design offers the most in highly

reliable operation with guaranteed accuracies. Because of the internal reference and pretrimmed accuracies the MPY100 does not have the restrictions of other low cost multipliers. It is available in both TO-100 and DIP ceramic packages.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25^\circ\text{C}$ and $\pm V_S = 15\text{VDC}$, unless otherwise specified.

		MPY100A			MPY100B/C			MPY100S			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE											
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$				*/*			*		
Total Error	$-10\text{V} \leq X, Y \leq 10\text{V}$										
Initial	$T_A = +25^\circ\text{C}$			± 2.0			$\pm 1.0/0.5$			± 0.5	% FSR
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.017	± 0.05		$\pm 0.008/0.008$	$\pm 0.02/0.02$				% FSR/°C
vs Temperature	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$								± 0.025	± 0.05	% FSR/°C
vs Supply ⁽¹⁾			± 0.05			*/*			*		% FSR/%
Individual Errors											
Output Offset											
Initial	$T_A = +25^\circ\text{C}$		± 50	± 100		$\pm 10/7$	$\pm 50/25$		± 7	± 50	mV
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.7	± 2.0		$\pm 0.7/0.3$	$\pm 2.0/\pm 0.7$				mV/°C
vs Temperature	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$								± 0.3	± 0.7	mV/°C
vs Supply ⁽¹⁾			± 0.25			*/*			*		mV/%
Scale Factor Error											
Initial	$T_A = +25^\circ\text{C}$		± 0.12			*/*			*		% FSR
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.008			*/*					% FSR/°C
vs Temperature	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$								± 0.008		% FSR/°C
vs Supply ⁽¹⁾			± 0.05			*/*			*		% FSR %
Nonlinearity											
X Input	$X = 20\text{Vp-p}; Y = \pm 10\text{VDC}$		± 0.08			*/*			*		% FSR
Y Input	$Y = 20\text{Vp-p}; X = \pm 10\text{VDC}$		± 0.08			*/*			*		% FSR
Feedthrough	$f = 50\text{Hz}$										
X Input	$X = 20\text{Vp-p}; Y = 0$		100			30/30			30		mVp-p
Y Input	$Y = 20\text{Vp-p}; X = 0$		6			*/*			*		mVp-p
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1			*/*					mVp-p/°C
vs Temperature	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$								0.1		mVp-p/°C
vs Supply ⁽¹⁾			0.15			*/*			*		mVp-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$	$\frac{10(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$				*/*			*		
Total Error (with external adjustments)	$X = 10\text{V}$										
	$-10\text{V} \leq Z \leq +10\text{V}$		± 1.5			$\pm 0.75/0.35$			± 0.35		% FSR
	$X = 1\text{V}$										
	$-1\text{V} \leq Z \leq +1\text{V}$		± 4.0			$\pm 2.0/1.0$			± 1.0		% FSR
	$+0.2\text{V} \leq X \leq +10\text{V}$										
	$-10\text{V} \leq Z \leq +10\text{V}$		± 5.0			$\pm 2.5/1.0$			± 1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function		$\frac{(X_1 - X_2)^2}{10} + Z_2$				*/*			*		
Total Error	$-10\text{V} \leq X \leq +10\text{V}$		± 1.2			$\pm 0.6/0.3$			± 0.3		% FSR
SQUARE ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$	$+\sqrt{10(Z_2 - Z_1)} + X_2$				*/*			*		
Total Error	$1\text{V} \leq Z \leq 10\text{V}$		± 2			$\pm 1/0.5$			± 0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth			550			*/*			*		kHz
% Amplitude Error	Small-Signal		70			*/*			*		kHz
% (0.57°) Vector Error	Small-Signal		5			*/*			*		kHz
Full Power Bandwidth	$ V_{OL} = 10\text{V}, R_L = 2\text{k}\Omega$		320			*/*			*		kHz
Slew Rate	$ V_{OL} = 10\text{V}, R_L = 2\text{k}\Omega$		20			*/*			*		V/μs
Settling Time	$\varepsilon = \pm 1\%, \Delta V_O = 20\text{V}$		2			*/*			*		μs
Overload Recovery	50% Output Overload		0.2			*/*			*		μs
INPUT CHARACTERISTICS											
Input Voltage Range		± 10			*/*			*			V
Rated Operation				$\pm V_{CC}$			*/*			*	V
Absolute Maximum											
Input Resistance	$X, Y, Z^{(2)}$		10			*/*			*		MΩ
Input Bias Current	X, Y, Z		1.4			*/*			*		μA
OUTPUT CHARACTERISTICS											
Rated Output		± 10			*/*			*			V
Voltage	$I_O = \pm 5\text{mA}$	± 5			*/*			*			mA
Current	$V_O = \pm 10\text{V}$										
Output Resistance	$f = \text{DC}$		1.5			*/*			*		Ω

SPECIFICATIONS (CONT)

At $T_A = +25^\circ\text{C}$ and $\pm V_S = 15\text{VDC}$, unless otherwise specified.

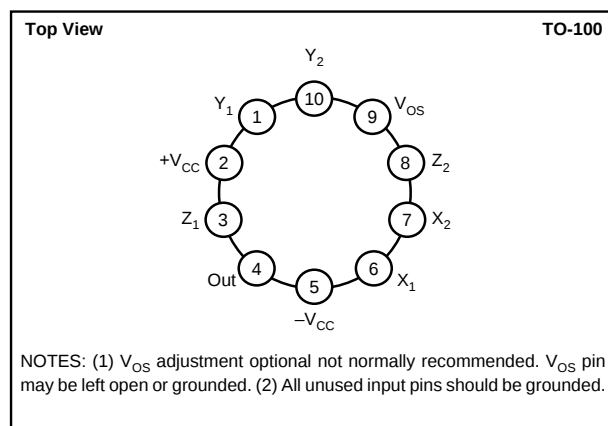
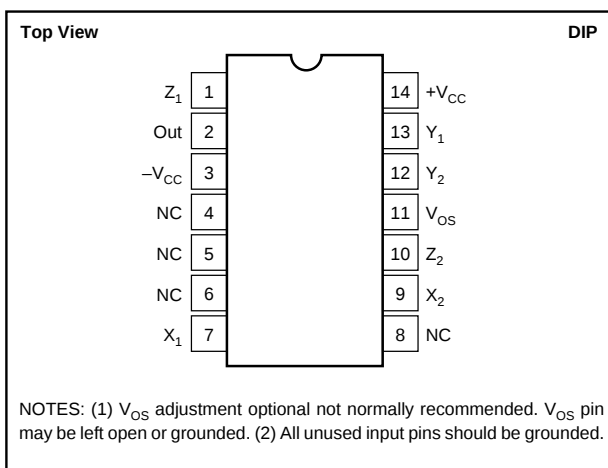
PARAMETER	CONDITIONS	MPY100A			MPY100B/C			MPY100S			UNITS		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
OUTPUT NOISE VOLTAGE X = Y = 0													
f _O = 1Hz			6.2			*/*			*		μV/√Hz		
f _O = 1kHz			0.6			*/*			*		μV/√Hz		
1/f Corner Frequency			110			*/*			*		Hz		
f _B = 5Hz to 10kHz			60			*/*			*		μVrms		
f _B = 5Hz to 5MHz			1.3			*/*			*		mVrms		
POWER SUPPLY REQUIREMENTS													
Rated Voltage	Derated Performance	±8.5	±15	±20	*/*	*/*	*/*	*	*	*	VDC		
Operating Range													VDC
Quiescent Current			±5.5			*/*			*			mA	
TEMPERATURE RANGE (Ambient)													
Specification	Derated Performance	−25		+85	*/*		*/*	−55		+125	°C		
Operating Range		−55		+125	*/*		*/*	*		*	°C		
Storage		−65		+150	*/*		*/*	*		*	°C		

* Same as MPY100A specification.

*/ B/C grades same as MPY100A specification.

NOTES: (1) Includes effects of recommended null pots. (2) Z_2 input resistance is $10\text{M}\Omega$, typical, with V_{OS} pin open. If V_{OS} pin is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as $25\text{k}\Omega$.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 20\text{VDC}$
Internal Power Dissipation ⁽¹⁾	500mW
Differential Input Voltage ⁽²⁾	$\pm 40\text{VDC}$
Input Voltage Range ⁽²⁾	$\pm 20\text{VDC}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Output Short-circuit Duration ⁽³⁾	Continuous
Junction Temperature	$+150^\circ\text{C}$

NOTES: (1) Package must be derated on $\theta_{JC} = 15^\circ\text{C/W}$ and $\theta_{JA} = 165^\circ\text{C/W}$ for the metal package and $\theta_{JC} = 35^\circ\text{C/W}$ and $\theta_{JA} = 220^\circ\text{C/W}$ for the ceramic package. (2) For supply voltages less than $\pm 20\text{VDC}$, the absolute maximum input voltage is equal to the supply voltage. (3) Short-circuit may be to ground only. Rating applies to $+85^\circ\text{C}$ ambient for the metal package and $+65^\circ\text{C}$ for the ceramic package.

ORDERING INFORMATION

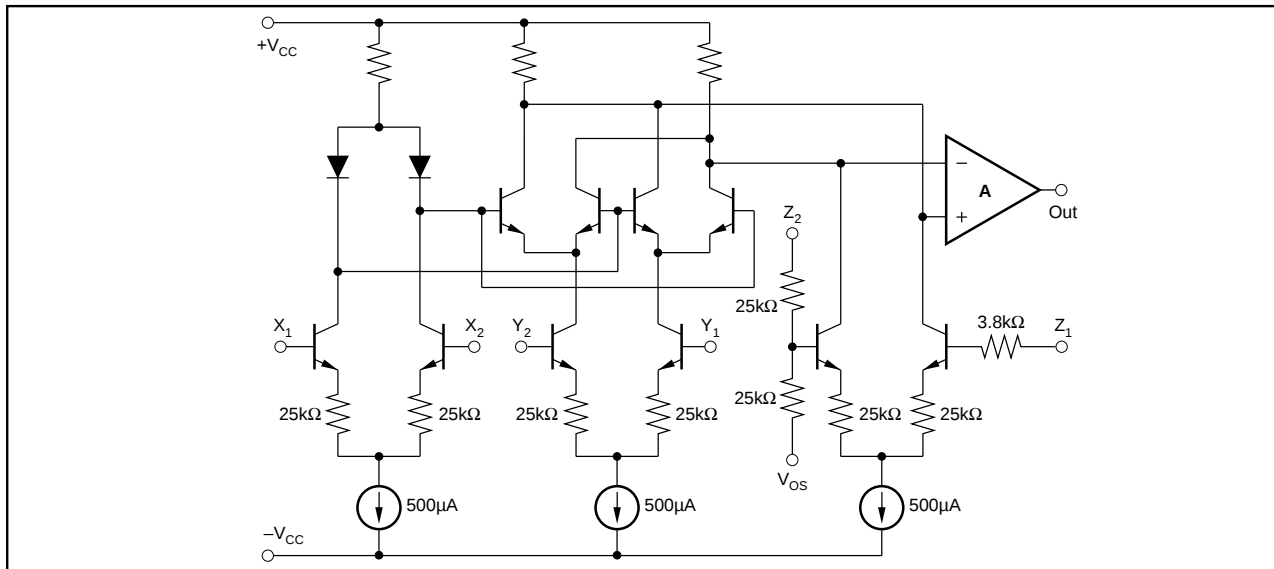
MODEL	PACKAGE	TEMPERATURE RANGE
MPY100AG	14-Pin Ceramic DIP	-25°C to $+85^\circ\text{C}$
MPY100AM	Metal TO-100	-25°C to $+85^\circ\text{C}$
MPY100BG	14-Pin Ceramic DIP	-25°C to $+85^\circ\text{C}$
MPY100BM	Metal TO-100	-25°C to $+85^\circ\text{C}$
MPY100CG	14-Pin Ceramic DIP	-25°C to $+85^\circ\text{C}$
MPY100CM	Metal TO-100	-25°C to $+85^\circ\text{C}$
MPY100SG	14-Pin Ceramic DIP	-55°C to $+125^\circ\text{C}$
MPY100SM	Metal TO-100	-55°C to $+125^\circ\text{C}$

PACKAGE INFORMATION

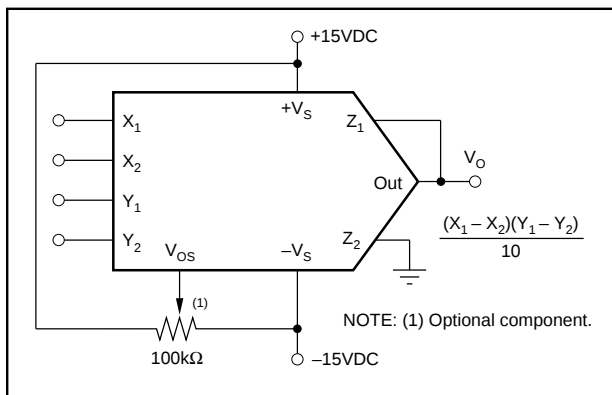
MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
MPY100AG	14-Pin Ceramic DIP	169
MPY100AM	Metal TO-100	007
MPY100BG	14-Pin Ceramic DIP	169
MPY100BM	Metal TO-100	007
MPY100CG	14-Pin Ceramic DIP	169
MPY100CM	Metal TO-100	007
MPY100SG	14-Pin Ceramic DIP	169
MPY100SM	Metal TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

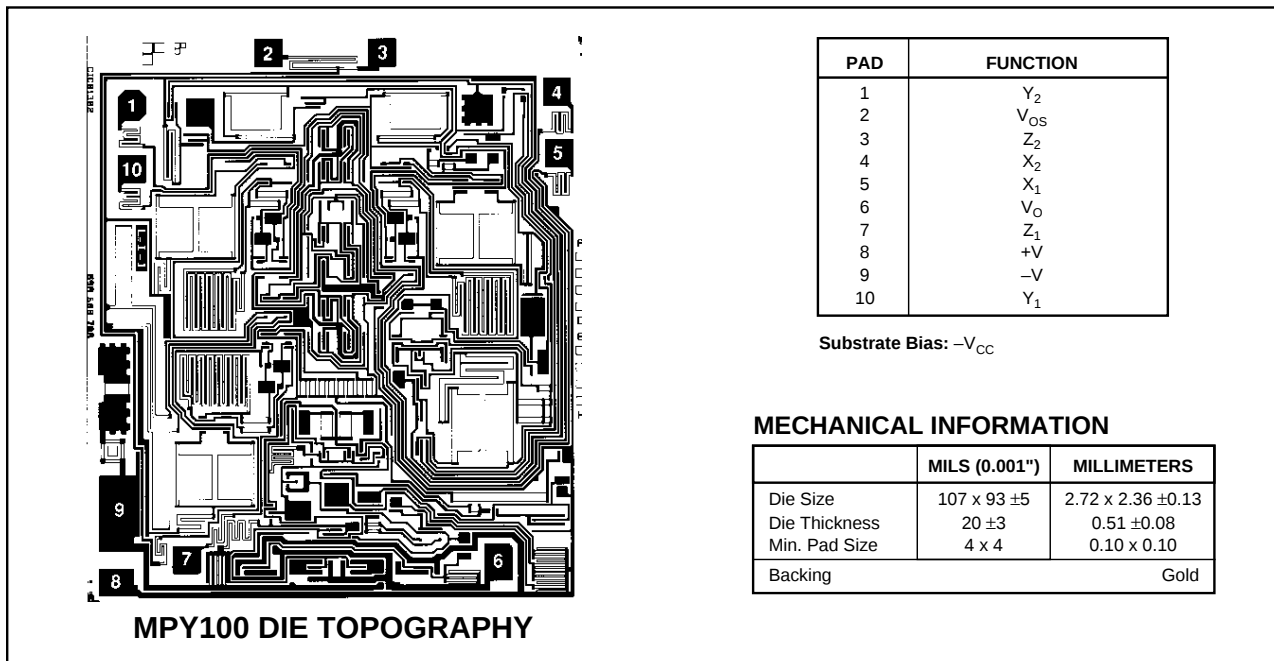
SIMPLIFIED SCHEMATIC



CONNECTION DIAGRAM

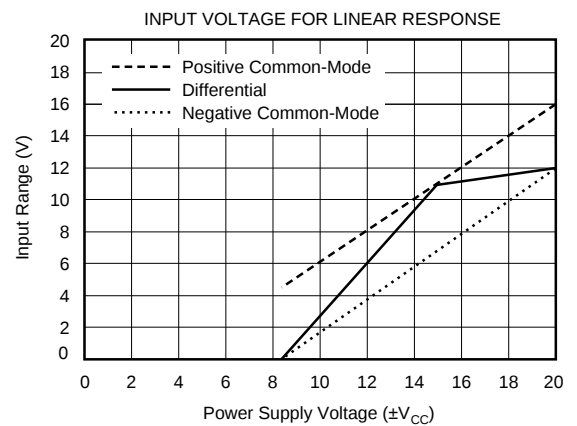
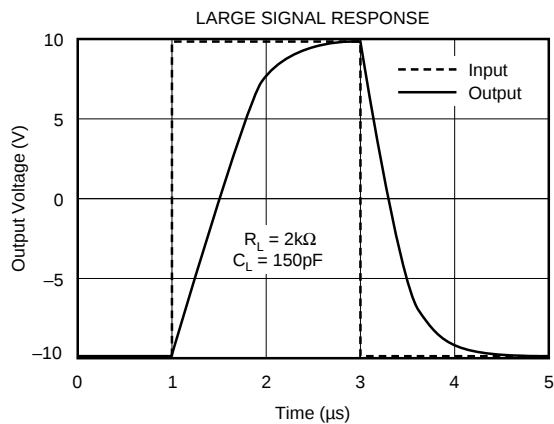
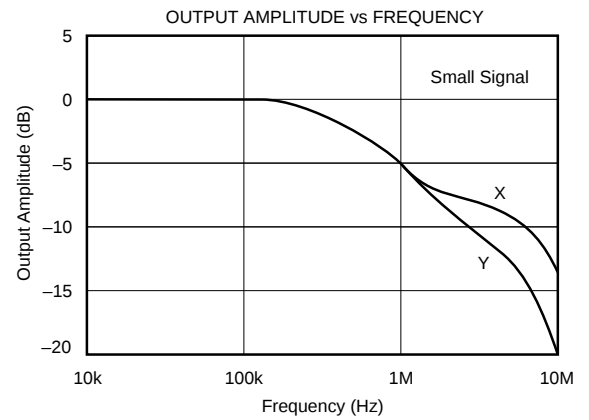
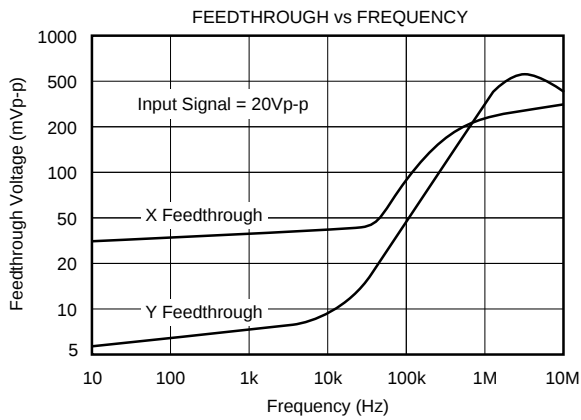
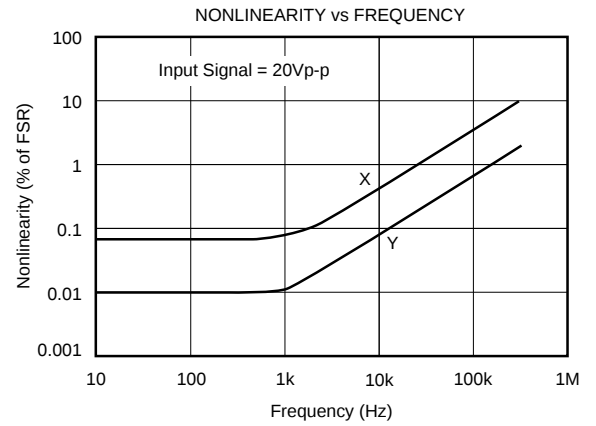
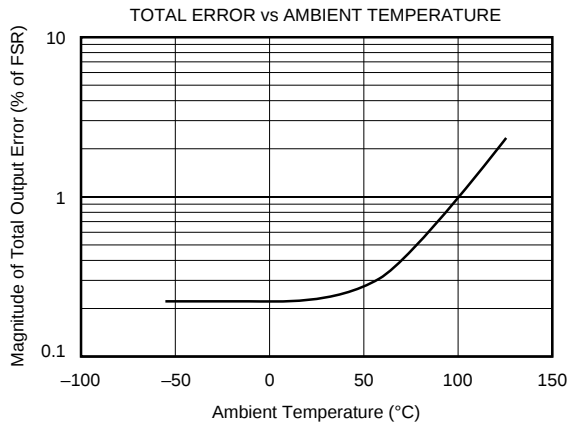


DICE INFORMATION



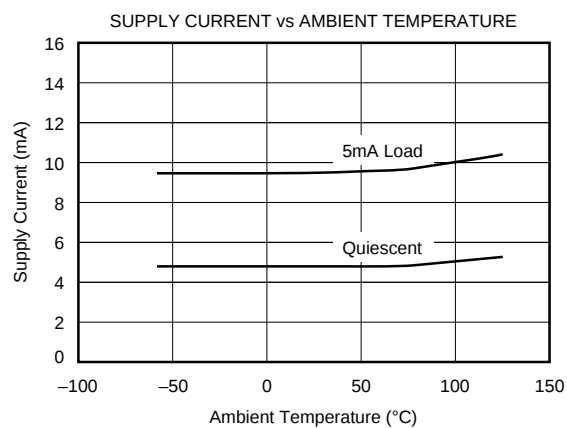
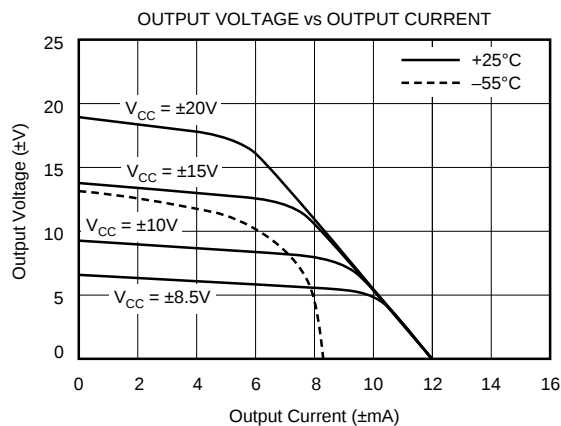
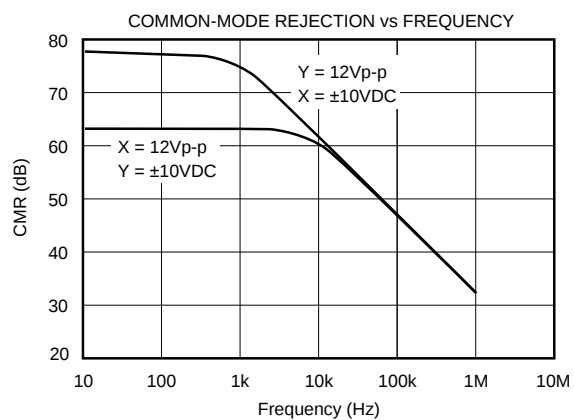
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$ and $\pm V_S = 15\text{VDC}$, unless otherwise specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$ and $\pm V_S = 15\text{VDC}$, unless otherwise specified.



THEORY OF OPERATION

The MPY100 is a variable transconductance multiplier consisting of three differential voltage-to-current converters, a multiplier core and an output differential amplifier as illustrated in Figure 1.

The basic principle of the transconductance multiplier can be demonstrated by the differential stage in Figure 2.

For small values of the input voltage, V_1 , that are much smaller than V_T , the transistor's thermal voltage, the differential output voltage, V_O , is:

$$V_O = g_m R_L V_1$$

The transconductance g_m of the stage is given by:

$$g_m = I_E/V_T$$

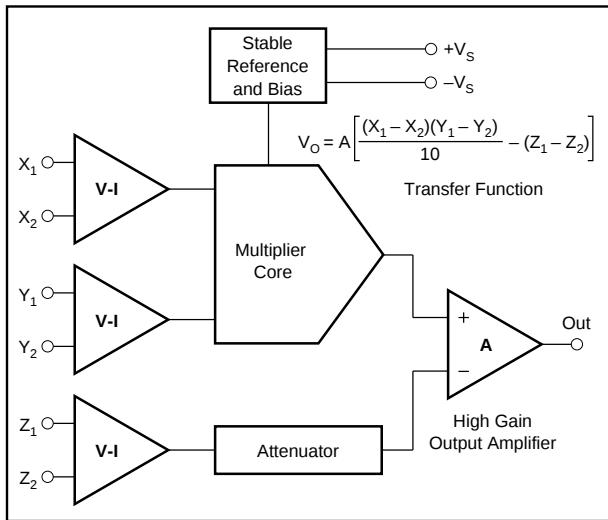


FIGURE 1. MPY100 Functional Block Diagram.

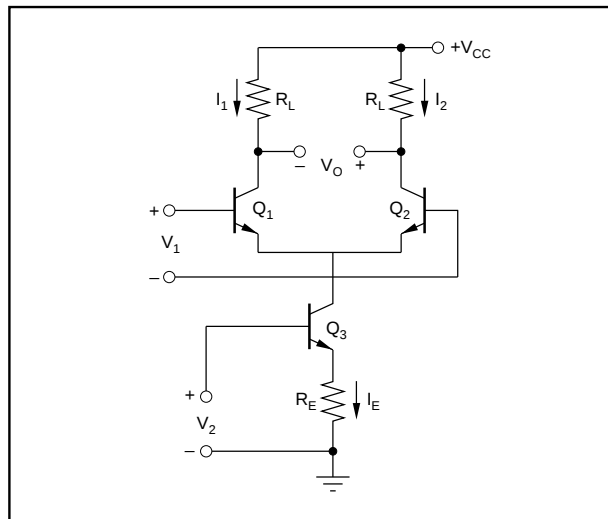


FIGURE 2. Basic Differential Stage as a Transconductance Multiplier.

and is modulated by the voltage, V_2 , to give

$$g_m \approx V_2/V_T R_E$$

Substituting this into the original equation yields the overall transfer function

$$V_O = g_m R_L V_1 = V_1 V_2 (R_L/V_T R_E)$$

which shows the output voltage to be the product of the two input voltages, V_1 and V_2 .

Variations in I_E due to V_2 cause a large common-mode voltage swing in the circuit. The errors associated with this common-mode voltage can be eliminated by using two differential stages in parallel and cross-coupling their outputs as shown in Figure 3.

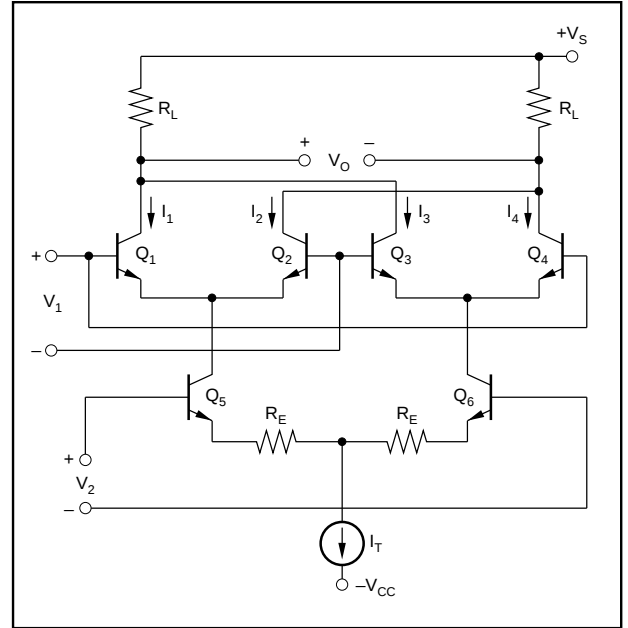


FIGURE 3. Cross-Coupled Differential Stages as a Variable-Transconductance Multiplier.

An analysis of the circuit in Figure 3 shows it to have the same overall transfer function as before:

$$V_O = V_1 V_2 (R_L/V_T R_E).$$

For input voltages larger than V_T , the voltage-to-current transfer characteristics of the differential pair Q_1 , Q_2 or Q_3 and Q_4 are no longer linear. Instead, their collector currents are related to the applied voltage V_1

$$\frac{I_1}{I_2} = \frac{I_3}{I_4} = e^{\frac{V_1}{V_T}}$$

The resultant nonlinearity can be overcome by developing V_1 logarithmically to exactly cancel the exponential relationship just derived. This is done by diodes D_1 and D_2 in Figure 4.

The emitter degeneration resistors, R_X and R_Y , in Figure 4, provide a linear conversion of the input voltages to differential current, I_X and I_Y , where:

$$I_X = V_X/R_X \text{ and } I_Y = V_Y/R_Y$$

Analysis of Figure 4 shows the voltage V_A to be:

$$V_A = (2R_L/I_1)(I_X I_Y)$$

Since I_X and I_Y are linearly related to the input voltages V_X and V_Y , V_A may also be written:

$$V_A = KV_X V_Y$$

where K is a scale factor. In the MPY100, K is chosen to be 0.1.

The addition of the Z input alters the voltage V_A to:

$$V_A = KV_X V_Y - V_Z$$

Therefore, the output of the MPY100 is:

$$V_O = A[KV_X V_Y - V_Z]$$

where A is the open-loop gain of the output amplifier. Writing this last equation in terms of the separate inputs to the MPY100 gives

$$V_O = A \left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2) \right]$$

the transfer function of the MPY100.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10 μ F tantalum capacitor in parallel with a 1000pF ceramic capacitor from the + V_{CC} and - V_{CC} pins of the MPY100 to the power supply common. The connection of these capacitors should be as close to the MPY100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100 Ω resistor is connected in series with the MPY100's output.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and V_Y are 0V.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

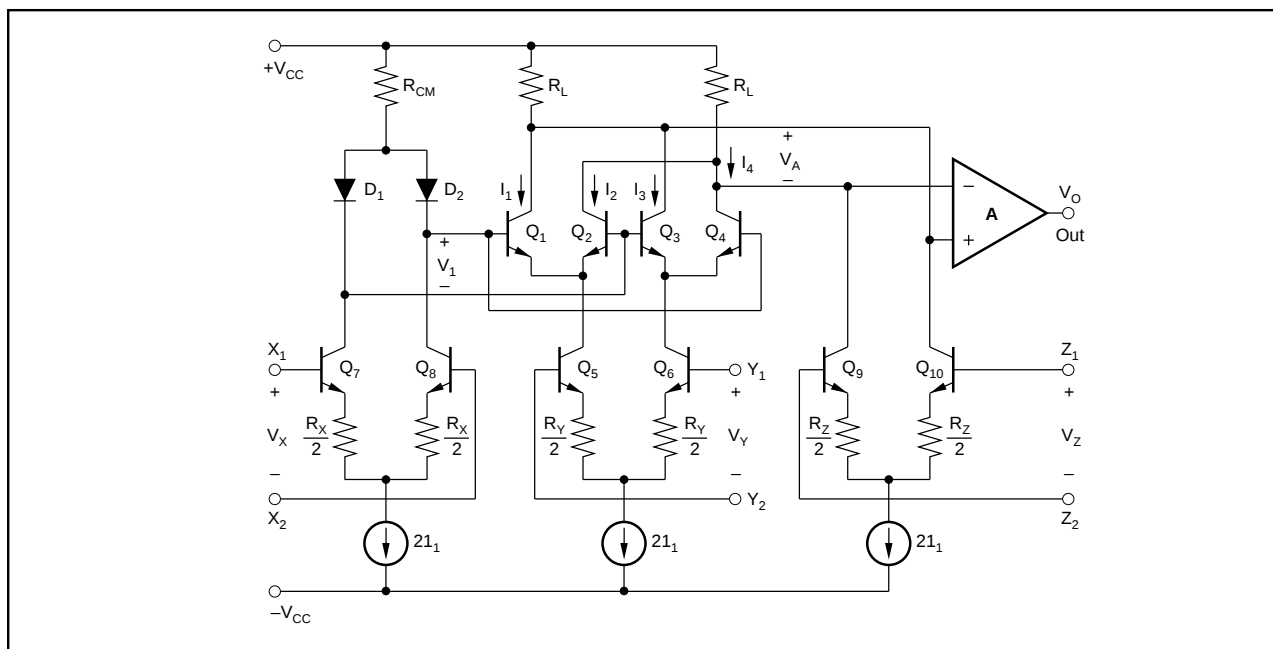


FIGURE 4. MPY100 Simplified Circuit Diagram.

SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value for nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

TYPICAL APPLICATIONS

MULTIPLICATION

Figure 5 shows the basic connection for four-quadrant multiplication.

The MPY100 meets all of its specifications without trimming. Accuracy can, however be improved over a limited range by nulling the output offset voltage using the 100Ω optional balance potentiometer shown in Figure 5.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 6.

Z₂, the optional summing input, may be used to sum a voltage into the output of the MPY100. If not used, this terminal, as well as the X and Y input terminals, should be grounded. All inputs should be referenced to power supply common.

Figure 7 shows how to achieve a scale factor larger than the nominal 1/10. In this case, the scale factor is unity which makes the transfer function

$$V_O = KV_X V_Y = K(X_1 - X_2)(Y_1 - Y_2)K = \left[\frac{1 + (R_1/R_2)}{10} \right]$$

$$0.1 \leq K \leq 1$$

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10, which may require the use of the optional balance control as in Figure 1 for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 8 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the MPY100, this operational amplifier is the output amplifier shown in Figure 1.

The divider error with a multiplier-inverted analog divider is approximately:

$$\epsilon_{\text{DIVIDER}} = 10 \epsilon_{\text{MULTIPLIER}} / (X_1 - X_2)$$

It is obvious from this error equation that divider error becomes excessively large for small values of $X_1 - X_2$. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be

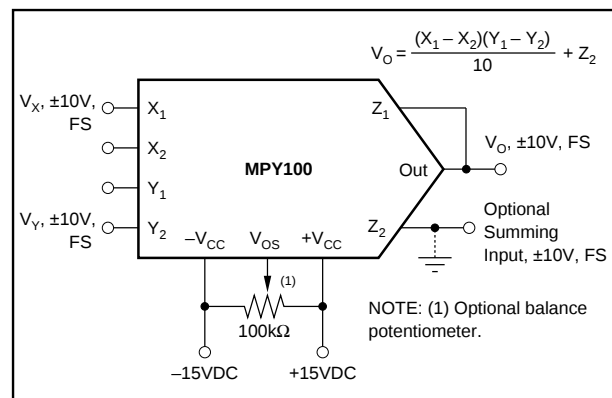


FIGURE 5. Multiplier Connection.

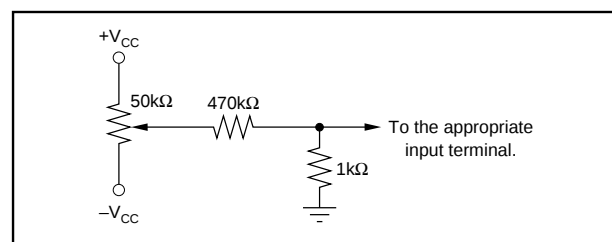


FIGURE 6. Optional Trimming Configuration.

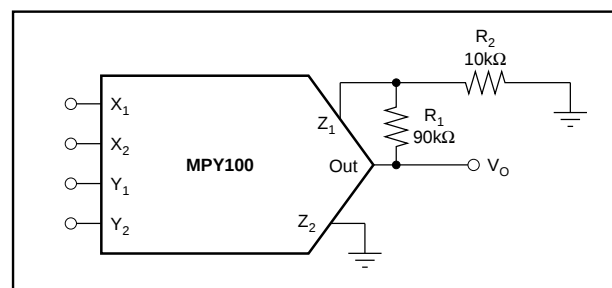


FIGURE 7. Connection for Unity Scale Factor.

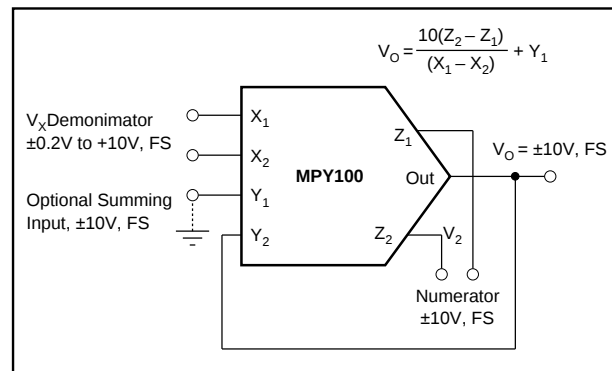


FIGURE 8. Divider Connection.

applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown DIV100, a precision log-antilog divider.

SQUARING

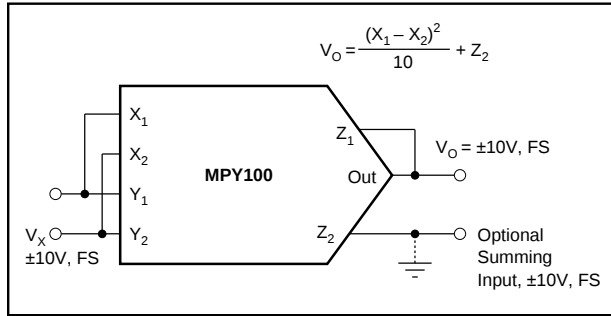


FIGURE 9. Squarer Connection.

SQUARE ROOT

Figure 10 shows the connection for taking the square root of the voltage V_Z . The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the MPY100, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

The load resistance, R_L , must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

PERCENTAGE COMPUTATION

The circuit of Figure 11 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1 .

BRIDGE LINEARIZATION

The use of the MPY100 to linearize the output from a bridge circuit makes the output V_O independent of the bridge supply voltage. See Figure 12.

TRUE RMS-TO-DC CONVERSION

The rms-to-DC conversion circuit of Figure 13 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

SINE FUNCTION GENERATOR

The circuit in Figure 14 uses implicit feedback to implement the following sine function approximation:

$$V_O = (1.5715V_1 - 0.004317V_1^3)/(1 + 0.001398V_1^2) \\ = 10 \sin(9V_1)$$

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown/McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

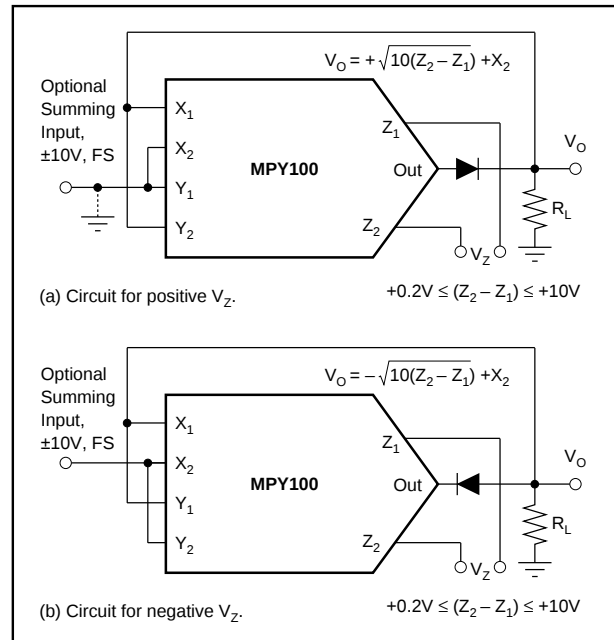


FIGURE 10. Square Root Connection.

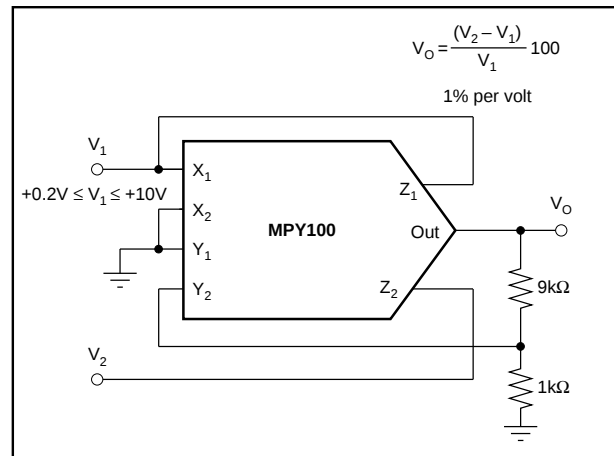


FIGURE 11. Percentage Computation.

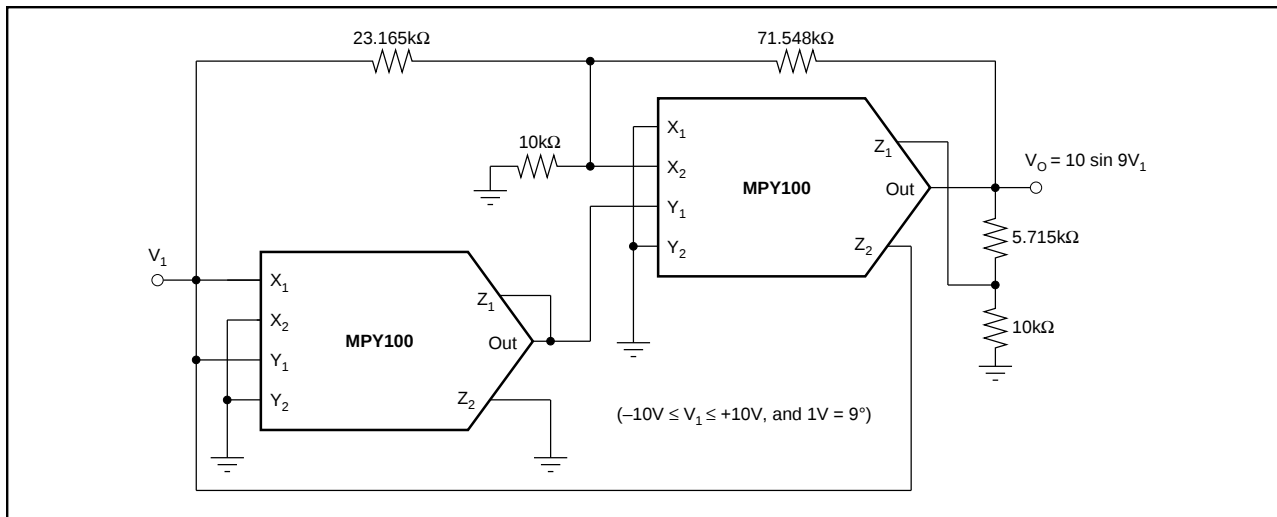


FIGURE 14. Sine Function Generator

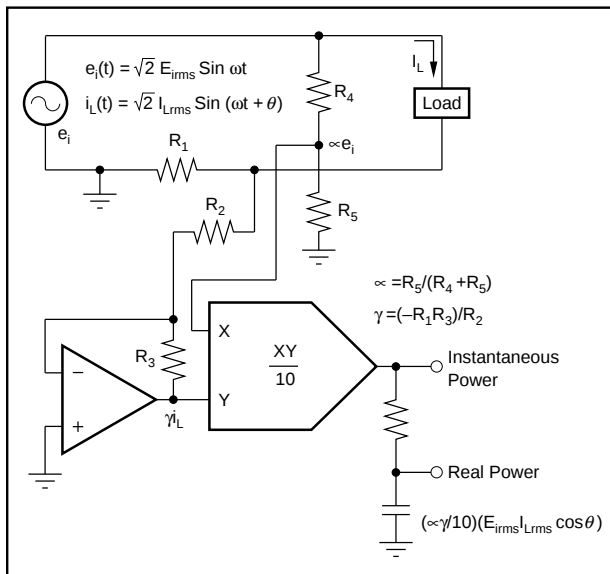


FIGURE 15. Single-Phase Instantaneous and Real Power Measurement.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MPY100AG	Last Time Buy	Production	CDIP SB (JD) 14	24 TUBE	Yes	Call TI	N/A for Pkg Type	-	MPY100AG
MPY100AG.A	NRND	Production	CDIP SB (JD) 14	24 TUBE	Yes	Call TI	N/A for Pkg Type	See MPY100AG	MPY100AG
MPY100BG	Last Time Buy	Production	CDIP SB (JD) 14	24 TUBE	Yes	Call TI	N/A for Pkg Type	-	MPY100BG
MPY100BG.A	NRND	Production	CDIP SB (JD) 14	24 TUBE	Yes	Call TI	N/A for Pkg Type	See MPY100BG	MPY100BG
MPY100CG	Last Time Buy	Production	CDIP SB (JD) 14	24 TUBE	Yes	Call TI	N/A for Pkg Type	-	MPY100CG
MPY100CG.A	NRND	Production	CDIP SB (JD) 14	24 TUBE	Yes	Call TI	N/A for Pkg Type	See MPY100CG	MPY100CG

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MPY100AG	JD	CDIP SB	14	24	506.98	15.24	12290	NA
MPY100AG.A	JD	CDIP SB	14	24	506.98	15.24	12290	NA
MPY100BG	JD	CDIP SB	14	24	506.98	15.24	12290	NA
MPY100BG.A	JD	CDIP SB	14	24	506.98	15.24	12290	NA
MPY100CG	JD	CDIP SB	14	24	506.98	15.24	12290	NA
MPY100CG.A	JD	CDIP SB	14	24	506.98	15.24	12290	NA

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Last updated 10/2025