

## MIXED SIGNAL MICROCONTROLLER

Check for Samples: [MSP430F2274-EP](#)

### FEATURES

- Low Supply Voltage Range 1.8 V to 3.6 V
- Ultralow-Power Consumption
  - Active Mode: 270  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 0.7  $\mu$ A
  - Off Mode (RAM Retention): 0.1  $\mu$ A
- Ultrafast Wake-Up From Standby Mode in Less than 1  $\mu$ s
- 16-Bit RISC Architecture, 62.5 ns Instruction Cycle Time
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to  $\pm 1\%$
  - Internal Very Low Power LF Oscillator
  - 32-kHz Crystal (Available Only from  $-55^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ )
  - High-Frequency Crystal up to 16 MHz (Available Only from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ )
  - Resonator
  - External Digital Clock Source
  - External Resistor
- 16-Bit Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer\_B With Three Capture/Compare Registers
- Universal Serial Communication Interface
  - Enhanced UART Supporting Auto-Baud-Rate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I<sup>2</sup>C™
- 10-Bit, 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan and Data Transfer Controller
- Two Configurable Operational Amplifiers
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Bootstrap Loader
- On-Chip Emulation Logic
- Family Members Include the MSP430F2274 With 32KB + 256B Flash Memory, 1KB RAM
- Available in 40-Pin QFN Package and 38-Pin Thin Shrink Small-Outline DA Package
- For Complete Module Descriptions, Refer to the *MSP430x2xx Family User's Guide*

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}/125^{\circ}\text{C}$ ) Temperature Range<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

<sup>(1)</sup> Custom temperature ranges available

### DESCRIPTION

The Texas Instruments MSP430 family of ultralow power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1  $\mu$ s.

The MSP430F2274M series is an ultralow-power mixed signal microcontroller with two built-in 16-bit timers, a universal serial communication interface, 10-bit A/D converter with integrated reference and data transfer controller (DTC), two general-purpose operational amplifiers in the MSP430F2274M devices, and 32 I/O pins.



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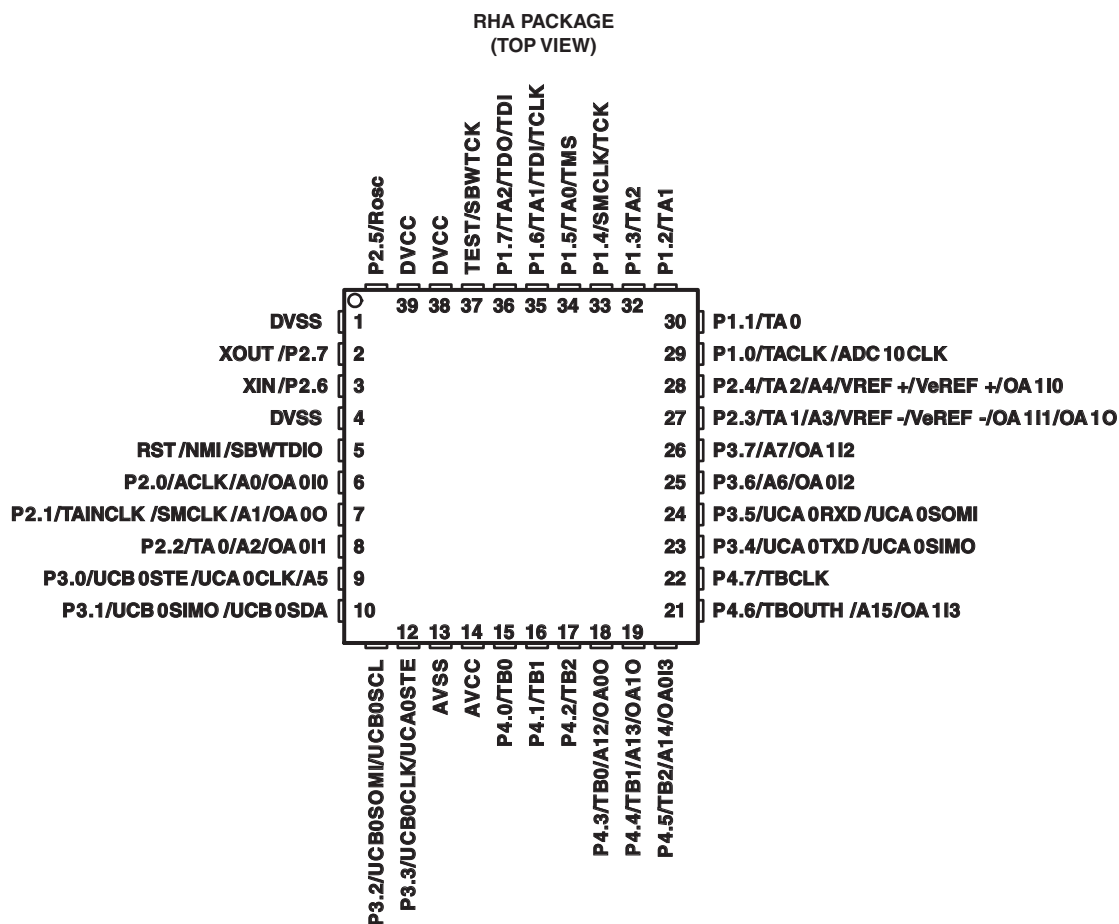
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Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand-alone RF sensor front end is another area of application.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

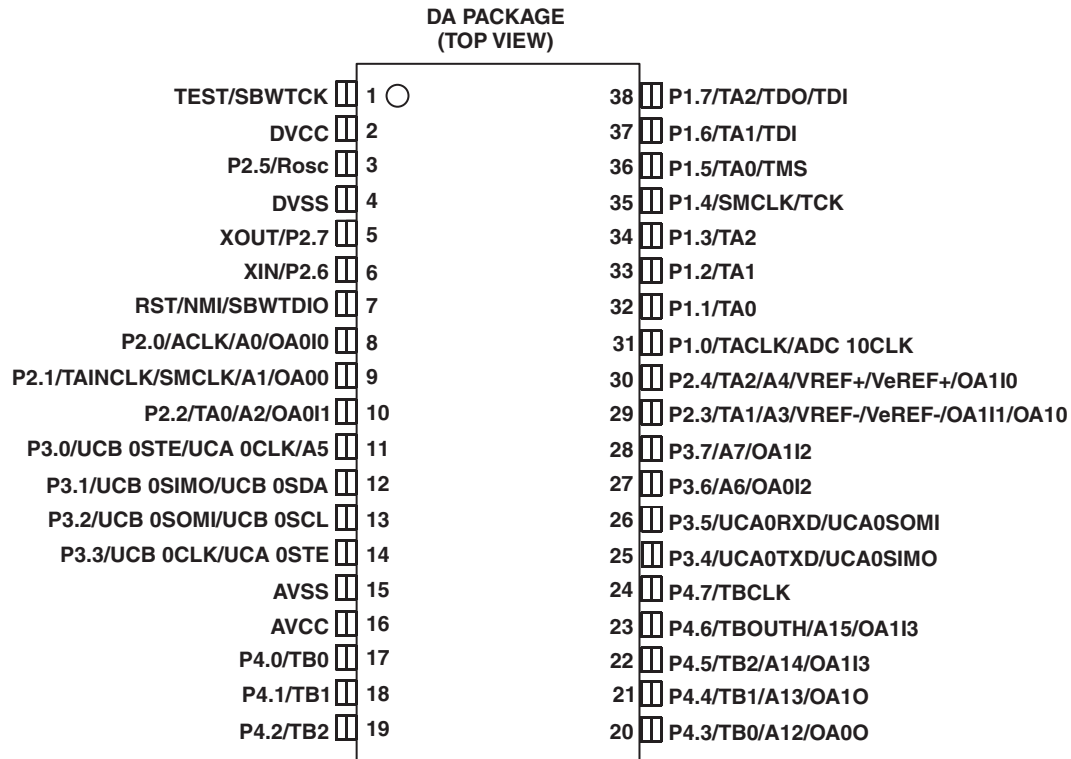
| T <sub>A</sub> | PACKAGE <sup>(2)</sup> | ORDERABLE PART NUMBER |
|----------------|------------------------|-----------------------|
| –55°C to 125°C | QFN (RHA)              | MSP430F2274MRHATEP    |
|                | DA (TSSOP)             | MSP430F2274MDATEP     |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

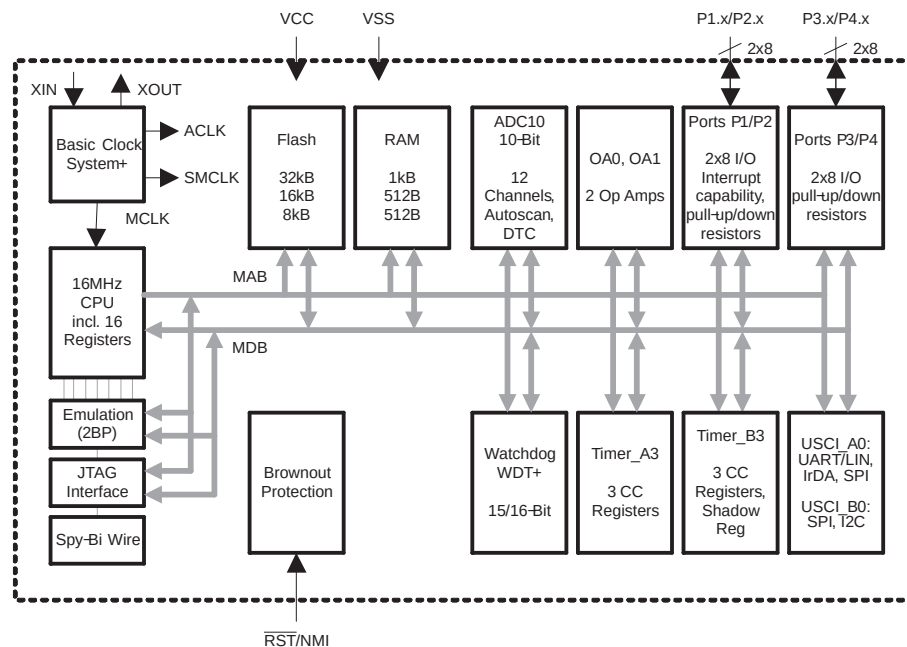
**DEVICE PINOUTS**

○ M4F2274  
MRHATEP  
TI YMS  
LLLLG4

TI = TI  
YM = YEAR/MONTH  
LLLL = LOT TRACE CODE  
S = ASSEMBLY SITE CODE  
G4 = RoHS with underscore  
O = PIN 1 indicator



## FUNCTIONAL BLOCK DIAGRAM



NOTE: See port schematics section for detailed I/O information.

**TERMINAL FUNCTIONS<sup>(1)</sup>**

| TERMINAL                                                      |        |         | I/O | DESCRIPTION                                                                                                                                                                                          |
|---------------------------------------------------------------|--------|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                          | DA NO. | RHA NO. |     |                                                                                                                                                                                                      |
| P1.0/TACLK/ADC10CLK                                           | 31     | 29      | I/O | General-purpose digital I/O pin<br>Timer_A, clock signal TACLK input<br>ADC10, conversion clock                                                                                                      |
| P1.1/TA0                                                      | 32     | 30      | I/O | General-purpose digital I/O pin<br>Timer_A, capture: CC10A input, compare: OUT0 output/BSL transmit                                                                                                  |
| P1.2/TA1                                                      | 33     | 31      | I/O | General-purpose digital I/O pin<br>Timer_A, capture: CC11A input, compare: OUT1 output                                                                                                               |
| P1.3/TA2                                                      | 34     | 32      | I/O | General-purpose digital I/O pin<br>Timer_A, capture: CC12A input, compare: OUT2 output                                                                                                               |
| P1.4/SMCLK/TCK                                                | 35     | 33      | I/O | General-purpose digital I/O pin/SMCLK signal output<br>Test Clock input for device programming and test                                                                                              |
| P1.5/TA0/TMS                                                  | 36     | 34      | I/O | General-purpose digital I/O pin/Timer_A, compare: OUT0 output<br>Test Mode Select input for device programming and test                                                                              |
| P1.6/TA1/TDI/TCLK                                             | 37     | 35      | I/O | General-purpose digital I/O pin/Timer_A, compare: OUT1 output<br>Test Data Input or Test Clock Input for programming and test                                                                        |
| P1.7/TA2/TDO/TDI <sup>(2)</sup>                               | 38     | 36      | I/O | General-purpose digital I/O pin/Timer_A, compare: OUT2 output<br>Test Data Output or Test Data Input for programming and test                                                                        |
| P2.0/ACLK/A0/OA0I0                                            | 8      | 6       | I/O | General-purpose digital I/O pin/ACLK output<br>ADC10, analog input A0 / OA0, analog input I0                                                                                                         |
| P2.1/TAINCLK/SMCLK/A1/OA0O                                    | 9      | 7       | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK<br>SMCLK signal output<br>ADC10, analog input A1/OA0, analog output                                                                   |
| P2.2/TA0/A2/OA0I1                                             | 10     | 8       | I/O | General-purpose digital I/O pin<br>Timer_A, capture: CC10B input/BSL receive, compare: OUT0 output<br>ADC10, analog input A2/OA0, analog input I1                                                    |
| P2.3/TA1/A3/V <sub>REF-</sub> /V <sub>eREF-</sub> /OA1I1/OA1O | 29     | 27      | I/O | General-purpose digital I/O pin<br>Timer_A, capture CC11B input, compare: OUT1 output<br>ADC10, analog input A3 / negative reference voltage output/input<br>OA1, analog input I1/OA1, analog output |
| P2.4/TA2/A4/V <sub>REF+</sub> /V <sub>eREF+</sub> /OA1I0      | 30     | 28      | I/O | General-purpose digital I/O pin/Timer_A, compare: OUT2 output<br>ADC10, analog input A4/positive reference voltage output/input<br>OA1, analog input I0                                              |
| P2.5/R <sub>OSC</sub>                                         | 3      | 40      | I/O | General-purpose digital I/O pin<br>Input for external DCO resistor to define DCO frequency                                                                                                           |
| XIN/P2.6                                                      | 6      | 3       | I/O | Input terminal of crystal oscillator<br>General-purpose digital I/O pin                                                                                                                              |
| XOUT/P2.7                                                     | 5      | 2       | I/O | Output terminal of crystal oscillator<br>General-purpose digital I/O pin                                                                                                                             |
| P3.0/UCB0STE/UCA0CLK/A5                                       | 11     | 9       | I/O | General-purpose digital I/O pin<br>USCI_B0 slave transmit enable/USCI_A0 clock input/output<br>ADC10, analog input A5                                                                                |
| P3.1/UCB0SIMO/UCB0SDA                                         | 12     | 10      | I/O | General-purpose digital I/O pin<br>USCI_B0 slave in/master out in SPI mode, SDA I <sup>2</sup> C data in I <sup>2</sup> C mode                                                                       |
| P3.2/UCB0SOMI/UCB0SCL                                         | 13     | 11      | I/O | General-purpose digital I/O pin<br>USCI_B0 slave out/master in SPI mode, SCL I <sup>2</sup> C clock in I <sup>2</sup> C mode                                                                         |
| P3.3/UCB0CLK/UCA0STE                                          | 14     | 12      | I/O | General-purpose digital I/O pin<br>USCI_B0 clock input/output/USCI_A0 slave transmit enable                                                                                                          |
| P3.4/UCA0TXD/UCA0SIMO                                         | 25     | 23      | I/O | General-purpose digital I/O pin<br>USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode                                                                                        |

(1) If XOUT/P2.7ca7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

(2) TDO or TDI is selected via JTAG instruction.

**TERMINAL FUNCTIONS<sup>(1)</sup> (continued)**

| TERMINAL             |        |             | I/O | DESCRIPTION                                                                                                                                            |
|----------------------|--------|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                 | DA NO. | RHA NO.     |     |                                                                                                                                                        |
| P3.5/UCARXD/UCASOMI  | 26     | 24          | I/O | General-purpose digital I/O pin<br>USCI_A0 receive data input in UART mode, slave out/master in in SPI mode                                            |
| P3.6/A6/OA0I2        | 27     | 25          | I/O | General-purpose digital I/O pin<br>ADC10 analog input A6/OA0 analog input I2                                                                           |
| P3.7/A7/OA1I2        | 28     | 26          | I/O | General-purpose digital I/O pin<br>ADC10 analog input A7/OA1 analog input I2                                                                           |
| P4.0/TB0             | 17     | 15          | I/O | General-purpose digital I/O pin<br>Timer_B, capture: CCI0A input, compare: OUT0 output                                                                 |
| P4.1/TB1             | 18     | 16          | I/O | General-purpose digital I/O pin<br>Timer_B, capture: CCI1A input, compare: OUT1 output                                                                 |
| P4.2/TB2             | 19     | 17          | I/O | General-purpose digital I/O pin<br>Timer_B, capture: CCI2A input, compare: OUT2 output                                                                 |
| P4.3/TB0A12/OA0O     | 20     | 18          | I/O | General-purpose digital I/O pin<br>Timer_B, capture: CCI0B input, compare: OUT0 output<br>ADC10 analog input A12/OA0 analog output                     |
| P4.4/TB1A13/OA1O     | 21     | 19          | I/O | General-purpose digital I/O pin<br>Timer_B, capture: CCI1B input, compare: OUT1 output<br>ADC10 analog input A13/OA1 analog output                     |
| P4.5/TB2A14/OA0I3    | 22     | 20          | I/O | General-purpose digital I/O pin<br>Timer_B, compare: OUT2 output<br>ADC10 analog input A14/OA0 analog input I3                                         |
| P4.6/TBOUTHA15/OA1I3 | 23     | 21          | I/O | General-purpose digital I/O pin<br>Timer_B, switch all TB0 to TB3 outputs to high impedance<br>ADC10 analog input A15/OA1 analog input I3              |
| P4.7/TBCLK           | 24     | 22          | I/O | General-purpose digital I/O pin<br>Timer_B, clock signal TBCLK input                                                                                   |
| RST/NMI/SBWDIO       | 7      | 5           | I   | Reset or nonmaskable interrupt input<br>Spy-Bi-Wire test data input/output during programming and test                                                 |
| TEST/SBWTCK          | 1      | 37          | I   | Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST.<br>Spy-Bi-Wire test clock input during programming and test |
| DV <sub>CC</sub>     | 2      | 38, 39      |     | Digital supply voltage                                                                                                                                 |
| AV <sub>CC</sub>     | 16     | 14          |     | Analog supply voltage                                                                                                                                  |
| DV <sub>SS</sub>     | 4      | 1, 4        |     | Digital ground reference                                                                                                                               |
| AV <sub>SS</sub>     | 15     | 13          |     | Analog ground reference                                                                                                                                |
| QFN Pad              | NA     | Package Pad | NA  | QFN package pad connection to DV <sub>SS</sub> recommended.                                                                                            |

## SHORT-FORM DESCRIPTION

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

### Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 2](#) shows examples of the three types of instruction formats; the address modes are listed in [Table 3](#).

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 2. Instruction Word Formats**

|                                   |                 |                                           |
|-----------------------------------|-----------------|-------------------------------------------|
| Dual operands, source-destination | e.g., ADD R4,R5 | $R4 + R5 \rightarrow R5$                  |
| Single operands, destination only | e.g., CALL R8   | $PC \rightarrow (TOS), R8 \rightarrow PC$ |
| Relative jump, un/conditional     | e.g., JNE       | Jump-on-equal bit = 0                     |

**Table 3. Address Mode Descriptions**

| ADDRESS MODE           | S <sup>(1)</sup> | D <sup>(2)</sup> | SYNTAX          | EXAMPLE          | OPERATION                                             |
|------------------------|------------------|------------------|-----------------|------------------|-------------------------------------------------------|
| Register               | •                | •                | MOV Rs,Rd       | MOV R10,R11      | $R10 \rightarrow R11$                                 |
| Indexed                | •                | •                | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6)  | $M(2+R5) \rightarrow M(6+R6)$                         |
| Symbolic (PC relative) | •                | •                | MOV EDE,TONI    |                  | $M(EDE) \rightarrow M(TONI)$                          |
| Absolute               | •                | •                | MOV &MEM,&TCDAT |                  | $M(MEM) \rightarrow M(TCDAT)$                         |
| Indirect               | •                |                  | MOV @Rn,Y(Rm)   | MOV @R10,Tab(R6) | $M(R10) \rightarrow M(Tab+R6)$                        |
| Indirect autoincrement | •                |                  | MOV @Rn+,Rm     | MOV @R10+,R11    | $M(R10) \rightarrow R11$<br>$R10 + 2 \rightarrow R10$ |
| Immediate              | •                |                  | MOV #X,TONI     | MOV #45,TONI     | $\#45 \rightarrow M(TONI)$                            |

(1) S = source

(2) D = destination

## Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.  
ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled. ACLK and SMCLK remain active. MCLK is disabled.  
DCO's dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.  
MCLK and SMCLK are disabled.  
DCO's dc-generator remains enabled.  
ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.  
MCLK and SMCLK are disabled.  
DCO's dc-generator is disabled.  
ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.  
ACLK is disabled.  
MCLK and SMCLK are disabled.  
DCO's dc-generator is disabled.  
Crystal oscillator is stopped.

## Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh–0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g., flash is not programmed), the CPU goes into LPM4 immediately after power up.

| INTERRUPT SOURCE                                                                                | INTERRUPT FLAG                                             | SYSTEM INTERRUPT                                     | WORD ADDRESS      | PRIORITY         |
|-------------------------------------------------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------|-------------------|------------------|
| Power up<br>External reset<br>Watchdog<br>Flash key violation<br>PC out-of-range <sup>(1)</sup> | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV <sup>(2)</sup>          | Reset                                                | 0FFFEh            | 31, highest      |
| NMI<br>Oscillator fault<br>Flash memory access violation                                        | NMIIFG<br>OFIFG<br>ACCVIFG <sup>(2) (3)</sup>              | (non)-maskable,<br>(non)-maskable,<br>(non)-maskable | 0FFFCh            | 30               |
| Timer_B3                                                                                        | TBCCR0 CCIFG <sup>(4)</sup>                                | maskable                                             | 0FFFAh            | 29               |
| Timer_B3                                                                                        | TBCCR1 and TBCCR2<br>CCIFGs, TBIFG <sup>(2) (4)</sup>      | maskable                                             | 0FFF8h            | 28               |
|                                                                                                 |                                                            |                                                      | 0FFF6h            | 27               |
| Watchdog Timer                                                                                  | WDTIFG                                                     | maskable                                             | 0FFF4h            | 26               |
| Timer_A3                                                                                        | TACCR0 CCIFG <sup>(4)</sup>                                | maskable                                             | 0FFF2h            | 25               |
| Timer_A3                                                                                        | TACCR1 CCIFG,<br>TACCR2 CCIFG,<br>TAIFG <sup>(2) (4)</sup> | maskable                                             | 0FFF0h            | 24               |
| USCI_A0/USCI_B0 Receive                                                                         | UCA0RXIFG, UCB0RXIFG <sup>(2)</sup>                        | maskable                                             | 0FFEEh            | 23               |
| USCI_A0/USCI_B0 Transmit                                                                        | UCA0TXIFG, UCB0TXIFG <sup>(2)</sup>                        | maskable                                             | 0FFECCh           | 22               |
| ADC10                                                                                           | ADC10IFG <sup>(4)</sup>                                    | maskable                                             | 0FFEAh            | 21               |
|                                                                                                 |                                                            |                                                      | 0FFE8h            | 20               |
| I/O Port P2 (eight flags)                                                                       | P2IFG.6 to P2IFG.7 <sup>(2) (4)</sup>                      | maskable                                             | 0FFE6h            | 19               |
| I/O Port P1 (eight flags)                                                                       | P1IFG.0 to P1IFG.7 <sup>(2) (4)</sup>                      | maskable                                             | 0FFE4h            | 18               |
|                                                                                                 |                                                            |                                                      | 0FFE2h            | 17               |
|                                                                                                 |                                                            |                                                      | 0FFE0h            | 16               |
| <sup>(5)</sup>                                                                                  |                                                            |                                                      | 0FFDEh            | 15               |
| <sup>(6)</sup>                                                                                  |                                                            |                                                      | 0FFDCh ... 0FFC0h | 14 ... 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address range.

(2) Multiple source flags

(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit disables an interrupt event.

(4) Interrupt flags are located in the module.

(5) This location is used as bootstrap loader security key (BSLSKEY). A 0AA55h at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.

(6) The interrupt vectors at addresses 0FFDCh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

## Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

### Interrupt Enable 1 and 2

| Address | 7 | 6 | 5      | 4     | 3 | 2 | 1    | 0     |
|---------|---|---|--------|-------|---|---|------|-------|
| 00h     |   |   | ACCVIE | NMIIE |   |   | OFIE | WDTIE |
|         |   |   | rw-0   | rw-0  |   |   | rw-0 | rw-0  |

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE: Oscillator fault enable

NMIIE: (Non)maskable interrupt enable

ACCVIE: Flash access violation interrupt enable

| Address | 7 | 6 | 5 | 4 | 3        | 2        | 1        | 0        |
|---------|---|---|---|---|----------|----------|----------|----------|
| 01h     |   |   |   |   | UCB0TXIE | UCB0RXIE | UCA0TXIE | UCA0RXIE |
|         |   |   |   |   | rw-0     | rw-0     | rw-0     | rw-0     |

UCA0RXIE USCI\_A0 receive-interrupt enable

UCA0TXIE USCI\_A0 transmit-interrupt enable

UCB0RXIE USCI\_B0 receive-interrupt enable

UCB0TXIE USCI\_B0 transmit-interrupt enable

### Interrupt Flag Register 1 and 2

| Address | 7 | 6 | 5 | 4      | 3      | 2      | 1     | 0      |
|---------|---|---|---|--------|--------|--------|-------|--------|
| 02h     |   |   |   | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
|         |   |   |   | rw-0   | rw-(0) | rw-(1) | rw-1  | rw-(0) |

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.  
Reset on  $V_{CC}$  power-up or a reset condition at  $\overline{RST}/NMI$  pin in reset mode.

OFIFG: Flag set on oscillator fault

RSTIFG: External reset interrupt flag. Set on a reset condition at  $\overline{RST}/NMI$  pin in reset mode. Reset on  $V_{CC}$  power up.

PORIFG: Power-On Reset interrupt flag. Set on  $V_{CC}$  power up.

NMIIFG: Set via  $\overline{RST}/NMI$ -pin

| Address | 7 | 6 | 5 | 4 | 3         | 2         | 1         | 0         |
|---------|---|---|---|---|-----------|-----------|-----------|-----------|
| 03h     |   |   |   |   | UCB0TXIFG | UCB0RXIFG | UCA0TXIFG | UCA0RXIFG |
|         |   |   |   |   | rw-1      | rw-0      | rw-1      | rw-0      |

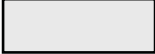
UCA0RXIFG USCI\_A0 receive-interrupt flag

UCA0TXIFG USCI\_A0 transmit-interrupt flag

UCB0RXIFG USCI\_B0 receive-interrupt flag

UCB0TXIFG USCI\_B0 transmit-interrupt flag

**Legend:**

|                                                                                   |                                                         |
|-----------------------------------------------------------------------------------|---------------------------------------------------------|
| rw:                                                                               | Bit can be read and written.                            |
| rw-0, 1:                                                                          | Bit can be read and written. It is Reset or Set by PUC. |
| rw-(0), (1):                                                                      | Bit can be read and written. It is Reset or Set by POR. |
|  | SFR bit is not present in device.                       |

**Memory Organization**

|                        |           | MSP430F223x   | MSP430F225x   | MSP430F227x   |
|------------------------|-----------|---------------|---------------|---------------|
| Memory                 | Size      | 8KB Flash     | 16KB Flash    | 32KB Flash    |
| Main: interrupt vector | Flash     | 0FFFFh–0FFC0h | 0FFFFh–0FFC0h | 0FFFFh–0FFC0h |
| Main: code memory      | Flash     | 0FFFFh–0E000h | 0FFFFh–0C000h | 0FFFFh–08000h |
| Information memory     | Size      | 256 Byte      | 256 Byte      | 256 Byte      |
|                        | Flash     | 010FFh–01000h | 010FFh–01000h | 010FFh–01000h |
| Boot memory            | Size      | 1KB           | 1KB           | 1KB           |
|                        | ROM       | 0FFFFh–0C00h  | 0FFFFh–0C00h  | 0FFFFh–0C00h  |
| RAM                    | Size      | 512 Byte      | 512 Byte      | 1KB           |
|                        |           | 03FFh–0200h   | 03FFh–0200h   | 05FFh–0200h   |
| Peripherals            | 16-bit    | 01FFh–0100h   | 01FFh–0100h   | 01FFh–0100h   |
|                        | 8-bit     | 0FFh–010h     | 0FFh–010h     | 0FFh–010h     |
|                        | 8-bit SFR | 0Fh–00h       | 0Fh–00h       | 0Fh–00h       |

**Bootstrap Loader (BSL)**

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report, *Features of the MSP430 Bootstrap Loader*, TI literature number SLAA089.

| BSL Function  | DA Package Pins | RHA Package Pins |
|---------------|-----------------|------------------|
| Data Transmit | 32 - P1.1       | 30 – P1.1        |
| Data Receive  | 10 - P2.2       | 8 – P2.2         |

**Flash Memory**

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0–n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

## Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x2xx Family User's Guide*.

## Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low power, low frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1  $\mu$ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator for  $-55^{\circ}\text{C}$  to  $105^{\circ}\text{C}$  operation. For  $> 105^{\circ}\text{C}$ , use external clock source.
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules

| DCO Calibration Data (provided from factory in flash info memory segment A) |                      |      |         |
|-----------------------------------------------------------------------------|----------------------|------|---------|
| DCO Frequency                                                               | Calibration Register | Size | Address |
| 1 MHz                                                                       | CALBC1_1MHZ          | byte | 010FFh  |
|                                                                             | CALDCO_1MHZ          | byte | 010FEh  |
| 8 MHz                                                                       | CALBC1_8MHZ          | byte | 010FDh  |
|                                                                             | CALDCO_8MHZ          | byte | 010FCh  |
| 12 MHz                                                                      | CALBC1_12MHZ         | byte | 010FBh  |
|                                                                             | CALDCO_12MHZ         | byte | 010FAh  |
| 16 MHz                                                                      | CALBC1_16MHZ         | byte | 010F9h  |
|                                                                             | CALDCO_16MHZ         | byte | 010F8h  |

## Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

## Digital I/O

There are four 8-bit I/O ports implemented – ports P1, P2, P3, and P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

## WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

## Timer\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_A3 Signal Connections |           |                     |                   |              |                      |                   |           |
|-----------------------------|-----------|---------------------|-------------------|--------------|----------------------|-------------------|-----------|
| Input Pin Number            |           | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |           |
| DA                          | RHA       |                     |                   |              |                      | DA                | RHA       |
| 31 - P1.0                   | 29 - P1.0 | TACLK               | TACLK             | Timer        | NA                   |                   |           |
|                             |           | ACLK                | ACLK              |              |                      |                   |           |
|                             |           | SMCLK               | SMCLK             |              |                      |                   |           |
| 9 - P2.1                    | 7 - P2.1  | TAINCLK             | INCLK             |              |                      |                   |           |
| 32 - P1.1                   | 30 - P1.1 | TA0                 | CCI0A             | CCR0         | TA0                  | 32 - P1.1         | 30 - P1.1 |
| 10 - P2.2                   | 8 - P2.2  | TA0                 | CCI0B             |              |                      | 10 - P2.2         | 8 - P2.2  |
|                             |           | V <sub>SS</sub>     | GND               |              |                      | 36 - P1.5         | 34 - P1.5 |
|                             |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |
| 33 - P1.2                   | 31 - P1.2 | TA1                 | CCI1A             | CCR1         | TA1                  | 33 - P1.2         | 31 - P1.2 |
| 29 - P2.3                   | 27 - P2.3 | TA1                 | CCI1B             |              |                      | 29 - P2.3         | 27 - P2.3 |
|                             |           | V <sub>SS</sub>     | GND               |              |                      | 37 - P1.6         | 35 - P1.6 |
|                             |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |
| 34 - P1.3                   | 32 - P1.3 | TA2                 | CCI2A             | CCR2         | TA2                  | 34 - P1.3         | 32 - P1.3 |
|                             |           | ACLK (internal)     | CCI2B             |              |                      | 30 - P2.4         | 28 - P2.4 |
|                             |           | V <sub>SS</sub>     | GND               |              |                      | 38 - P1.7         | 36 - P1.7 |
|                             |           | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |           |

## Timer\_B3

Timer\_B3 is a 16-bit timer/counter with three capture/compare registers. Timer\_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_B3 Signal Connections |           |                           |                   |              |                      |                   |           |
|-----------------------------|-----------|---------------------------|-------------------|--------------|----------------------|-------------------|-----------|
| Input Pin Number            |           | Device Input Signal       | Module Input Name | Module Block | Module Output Signal | Output Pin Number |           |
| DA                          | RHA       |                           |                   |              |                      | DA                | RHA       |
| 24 - P4.7                   | 22 - P4.7 | TBCLK                     | TBCLK             | Timer        | NA                   |                   |           |
|                             |           | ACLK                      | ACLK              |              |                      |                   |           |
|                             |           | SMCLK                     | SMCLK             |              |                      |                   |           |
| 24 - P4.7                   | 22 - P4.7 | $\overline{\text{TBCLK}}$ | INCLK             |              |                      |                   |           |
| 17 - P4.0                   | 15 - P4.0 | TB0                       | CCI0A             | CCR0         | TB0                  | 17 - P4.0         | 15 - P4.0 |
| 20 - P4.3                   | 18 - P4.3 | TB0                       | CCI0B             |              |                      | 20 - P4.3         | 18 - P4.3 |
|                             |           | V <sub>SS</sub>           | GND               |              |                      |                   |           |
|                             |           | V <sub>CC</sub>           | V <sub>CC</sub>   |              |                      |                   |           |
| 18 - P4.1                   | 16 - P4.1 | TB1                       | CCI1A             | CCR1         | TB1                  | 18 - P4.1         | 16 - P4.1 |
| 21 - P4.4                   | 19 - P4.4 | TB1                       | CCI1B             |              |                      | 21 - P4.4         | 19 - P4.4 |
|                             |           | V <sub>SS</sub>           | GND               |              |                      |                   |           |
|                             |           | V <sub>CC</sub>           | V <sub>CC</sub>   |              |                      |                   |           |
| 19 - P4.2                   | 17 - P4.2 | TB2                       | CCI2A             | CCR2         | TB2                  | 19 - P4.2         | 17 - P4.2 |
|                             |           | ACLK (internal)           | CCI2B             |              |                      | 22 - P4.5         | 20 - P4.5 |
|                             |           | V <sub>SS</sub>           | GND               |              |                      |                   |           |
|                             |           | V <sub>CC</sub>           | V <sub>CC</sub>   |              |                      |                   |           |

## USCI

The universal serial communication interface (USCI) module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baud-rate detection (LIN), and IrDA.

USCI\_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

USCI\_B0 provides support for SPI (3 or 4 pin) and I2C.

## ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

## Operational Amplifier (OA)

The MSP430F2274M has two configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

| OA0 Signal Connections     |          |                     |                   |
|----------------------------|----------|---------------------|-------------------|
| Analog Input<br>Pin Number |          | Device Input Signal | Module Input Name |
| DA                         | RHA      |                     |                   |
| 8 - A0                     | 6 - A0   | OA0I0               | OAxI0             |
| 10 - A2                    | 8 - A2   | OA0I1               | OA0I1             |
| 10 - A2                    | 8 - A2   | OA0I1               | OAxI1             |
| 27 - A6                    | 25 - A6  | OA0I2               | OAxIA             |
| 22 - A14                   | 20 - A14 | OA0I3               | OAxIB             |

| OA1 Signal Connections     |          |                     |                   |
|----------------------------|----------|---------------------|-------------------|
| Analog Input<br>Pin Number |          | Device Input Signal | Module Input Name |
| DA                         | RHA      |                     |                   |
| 30 - A4                    | 28 - A4  | OA0I0               | OAxI0             |
| 10 - A2                    | 8 - A2   | OA0I1               | OA0I1             |
| 29 - A3                    | 27 - A3  | OA0I1               | OAxI1             |
| 28 - A7                    | 26 - A7  | OA0I2               | OAxIA             |
| 23 - A15                   | 21 - A15 | OA0I3               | OAxIB             |

## Peripheral File Map

| PERIPHERALS WITH WORD ACCESS |                                                                                                                                                                                                                                      |                                                                                                 |                                                                               |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| <b>ADC10</b>                 | ADC data transfer start address<br>ADC memory<br>ADC control register 1<br>ADC control register 0<br>ADC analog enable 0<br>ADC analog enable 1<br>ADC data transfer control register 1<br>ADC data transfer control register 0      | ADC10SA<br>ADC10MEM<br>ADC10CTL1<br>ADC10CTL0<br>ADC10AE0<br>ADC10AE1<br>ADC10DTC1<br>ADC10DTC0 | 1BCh<br>1B4h<br>1B2h<br>1B0h<br>04Ah<br>04Bh<br>049h<br>048h                  |
| <b>Timer_B</b>               | Capture/compare register<br>Capture/compare register<br>Capture/compare register<br>Timer_B register<br>Capture/compare control<br>Capture/compare control<br>Capture/compare control<br>Timer_B control<br>Timer_B interrupt vector | TBCCR2<br>TBCCR1<br>TBCCR0<br>TBR<br>TBCCTL2<br>TBCCTL1<br>TBCCTL0<br>TBCTL<br>TBIV             | 0196h<br>0194h<br>0192h<br>0190h<br>0186h<br>0184h<br>0182h<br>0180h<br>011Eh |
| <b>Timer_A</b>               | Capture/compare register<br>Capture/compare register<br>Capture/compare register<br>Timer_A register<br>Capture/compare control<br>Capture/compare control<br>Capture/compare control<br>Timer_A control<br>Timer_A interrupt vector | TACCR2<br>TACCR1<br>TACCR0<br>TAR<br>TACCTL2<br>TACCTL1<br>TACCTL0<br>TACTL<br>TAIV             | 0176h<br>0174h<br>0172h<br>0170h<br>0166h<br>0164h<br>0162h<br>0160h<br>012Eh |
| <b>Flash Memory</b>          | Flash control 3<br>Flash control 2<br>Flash control 1                                                                                                                                                                                | FCTL3<br>FCTL2<br>FCTL1                                                                         | 012Ch<br>012Ah<br>0128h                                                       |
| <b>Watchdog Timer+</b>       | Watchdog/timer control                                                                                                                                                                                                               | WDTCTL                                                                                          | 0120h                                                                         |

| PERIPHERALS WITH BYTE ACCESS |                                                                                                                                                                                                                                                                                                              |                                                                                                                                       |                                                                                      |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| <b>OA1</b>                   | Operational Amplifier 1 control register 1<br>Operational Amplifier 1 control register 1                                                                                                                                                                                                                     | OA1CTL1<br>OA1CTL0                                                                                                                    | 0C3h<br>0C2h                                                                         |
| <b>OA0</b>                   | Operational Amplifier 0 control register 1<br>Operational Amplifier 0 control register 1                                                                                                                                                                                                                     | OA0CTL1<br>OA0CTL0                                                                                                                    | 0C1h<br>0C0h                                                                         |
| <b>USI_B0</b>                | USCI_B0 transmit buffer<br>USCI_B0 receive buffer<br>USCI_B0 status<br>USCI_B0 bit rate control 1<br>USCI_B0 bit rate control 0<br>USCI_B0 control 1<br>USCI_B0 control 0<br>USCI_B0 I2C slave address<br>USCI_B0 I2C own address                                                                            | UCB0TXBUF<br>UCB0RXBUF<br>UCB0STAT<br>UCB0BR1<br>UCB0BR0<br>UCB0CTL1<br>UCB0CTL0<br>UCB0SA<br>UCB0OA                                  | 06Fh<br>06Eh<br>06Dh<br>06Bh<br>06Ah<br>069h<br>068h<br>011Ah<br>0118h               |
| <b>USI_A0</b>                | USCI_A0 transmit buffer<br>USCI_A0 receive buffer<br>USCI_A0 status<br>USCI_A0 modulation control<br>USCI_A0 baud rate control 1<br>USCI_A0 baud rate control 0<br>USCI_A0 control 1<br>USCI_A0 control 0<br>USCI_A0 IrDA receive control<br>USCI_A0 IrDA transmit control<br>USCI_A0 auto baud rate control | UCA0TXBUF<br>UCA0RXBUF<br>UCA0STAT<br>UCA0MCTL<br>UCA0BR1<br>UCA0BR0<br>UCA0CTL1<br>UCA0CTL0<br>UCA0IRRCTL<br>UCA0IRTCTL<br>UCA0ABCTL | 067h<br>066h<br>065h<br>064h<br>063h<br>062h<br>061h<br>060h<br>05Fh<br>05Eh<br>05Dh |
| <b>Basic Clock System+</b>   | Basic clock system control 3<br>Basic clock system control 2<br>Basic clock system control 1<br>DCO clock frequency control                                                                                                                                                                                  | BCSCTL3<br>BCSCTL2<br>BCSCTL1<br>DCOCTL                                                                                               | 053h<br>058h<br>057h<br>056h                                                         |
| <b>Port P4</b>               | Port P4 resistor enable<br>Port P4 selection<br>Port P4 direction<br>Port P4 output<br>Port P4 input                                                                                                                                                                                                         | P4REN<br>P4SEL<br>P4DIR<br>P4OUT<br>P4IN                                                                                              | 011h<br>01Fh<br>01Eh<br>01Dh<br>01Ch                                                 |
| <b>Port P3</b>               | Port P3 resistor enable<br>Port P3 selection<br>Port P3 direction<br>Port P3 output<br>Port P3 input                                                                                                                                                                                                         | P3REN<br>P3SEL<br>P3DIR<br>P3OUT<br>P3IN                                                                                              | 010h<br>01Bh<br>01Ah<br>019h<br>018h                                                 |
| <b>Port P2</b>               | Port P2 resistor enable<br>Port P2 selection<br>Port P2 interrupt enable<br>Port P2 interrupt edge select<br>Port P2 interrupt flag<br>Port P2 direction<br>Port P2 output<br>Port P2 input                                                                                                                  | P2REN<br>P2SEL<br>P2IE<br>P2IES<br>P2IFG<br>P2DIR<br>P2OUT<br>P2IN                                                                    | 02Fh<br>02Eh<br>02Dh<br>02Ch<br>02Bh<br>02Ah<br>029h<br>028h                         |
| <b>Port P1</b>               | Port P1 resistor enable<br>Port P1 selection<br>Port P1 interrupt enable<br>Port P1 interrupt edge select<br>Port P1 interrupt flag<br>Port P1 direction<br>Port P1 output<br>Port P1 input                                                                                                                  | P1REN<br>P1SEL<br>P1IE<br>P1IES<br>P1IFG<br>P1DIR<br>P1OUT<br>P1IN                                                                    | 027h<br>026h<br>025h<br>024h<br>023h<br>022h<br>021h<br>020h                         |
| <b>Special Function</b>      | SFR interrupt flag 2<br>SFR interrupt flag 1<br>SFR interrupt enable 2<br>SFR interrupt enable 1                                                                                                                                                                                                             | IFG2<br>IFG1<br>IE2<br>IE1                                                                                                            | 003h<br>002h<br>001h<br>000h                                                         |

## Absolute Maximum Ratings<sup>(1)</sup>

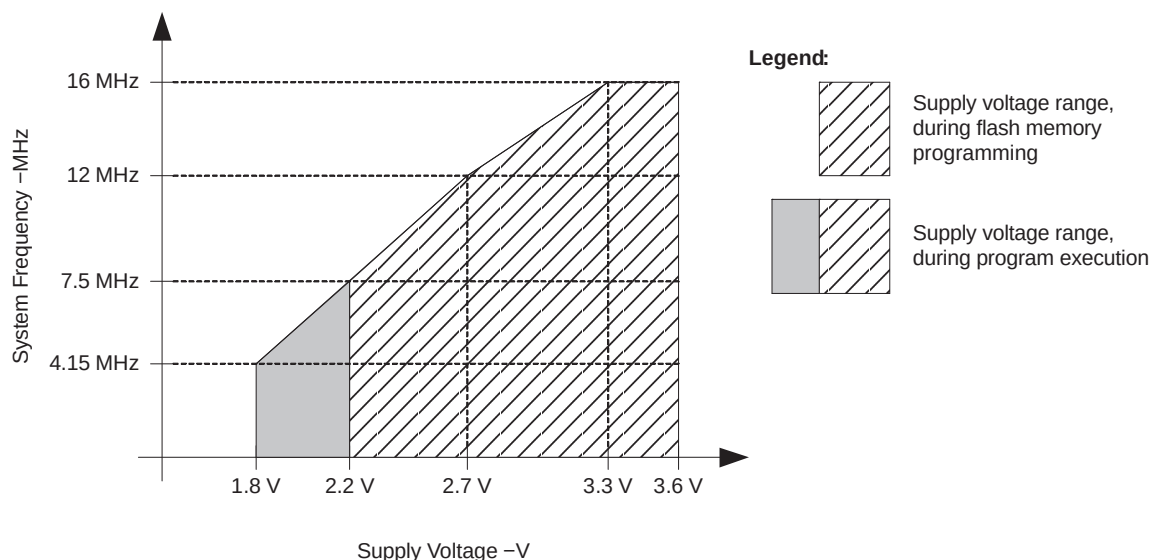
|                                                                      | VALUE                  | UNIT |
|----------------------------------------------------------------------|------------------------|------|
| Voltage applied at $V_{CC}$ to $V_{SS}$                              | –0.3 to 4.1            | V    |
| Voltage applied to any pin <sup>(2)</sup>                            | –0.3 to $V_{CC} + 0.3$ | V    |
| Diode current at any device terminal                                 | ±2                     | mA   |
| Storage temperature, $T_{stg}$ (unprogrammed device <sup>(3)</sup> ) | –55 to 150             | °C   |
| Storage temperature, $T_{stg}$ (programmed device <sup>(3)</sup> )   | –55 to 125             | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

**Recommended Operating Conditions<sup>(1) (2)</sup>**

|                                                                                                   |                                                          | MIN | NOM | MAX  | UNIT |
|---------------------------------------------------------------------------------------------------|----------------------------------------------------------|-----|-----|------|------|
| $V_{CC}$                                                                                          | Supply voltage during program execution                  | 1.8 |     | 3.6  | V    |
|                                                                                                   | Supply voltage during program/erase flash memory         | 2.2 |     | 3.6  | V    |
| $V_{SS}$                                                                                          | Supply voltage                                           |     | 0   |      | V    |
| $T_A$                                                                                             | Operating free-air temperature range                     | –55 |     | 125  | °C   |
| Processor frequency $f_{SYSTEM}$<br>(Maximum MCLK frequency) <sup>(1) (2)</sup><br>(see Figure 1) | $V_{CC} = 1.8\text{ V}$ , Duty Cycle = 50% $\pm 10\%$    | dc  |     | 4.15 | MHz  |
|                                                                                                   | $V_{CC} = 2.7\text{ V}$ , Duty Cycle = 50% $\pm 10\%$    | dc  |     | 12   |      |
|                                                                                                   | $V_{CC} \geq 3.3\text{ V}$ , Duty Cycle = 50% $\pm 10\%$ | dc  |     | 16   |      |

- (1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- (2) Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.2 V.

**Figure 1. Operating Area**

## Active-Mode Supply Current (Into $DV_{CC} + AV_{CC}$ ) Excluding External Current – Electrical Characteristics<sup>(1),(2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                           | TEST CONDITIONS                                                                                                                                                                                                                                   | $T_A$          | $V_{CC}$ | MIN | TYP | MAX | UNIT          |
|-----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------|-----|-----|-----|---------------|
| $I_{AM, 1MHz}$ Active-mode (AM) current (1 MHz)     | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1 \text{ MHz}$ ,<br>$f_{ACLK} = 32,768 \text{ Hz}$ ,<br>Program executes in flash,<br>BCSCTL1 = CALBC1_1 MHz,<br>DCOCTL = CALDCO_1 MHz,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0                        | –55°C to 125°C | 2.2 V    |     | 270 | 390 | $\mu\text{A}$ |
|                                                     |                                                                                                                                                                                                                                                   |                | 3 V      |     | 390 | 550 |               |
| $I_{AM, 1MHz}$ Active-mode (AM) current (1 MHz)     | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1 \text{ MHz}$ ,<br>$f_{ACLK} = 32,768 \text{ Hz}$ ,<br>Program executes in RAM,<br>BCSCTL1 = CALBC1_1 MHz,<br>DCOCTL = CALDCO_1 MHz,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0                          |                | 2.2 V    |     | 240 |     | $\mu\text{A}$ |
|                                                     |                                                                                                                                                                                                                                                   |                | 3 V      |     | 340 |     |               |
| $I_{AM, 4kHz}$ Active-mode (AM) current (4 kHz)     | $f_{MCLK} = f_{SMCLK} = f_{ACLK} = 32,768 \text{ Hz}/8 = 4,096 \text{ Hz}$ ,<br>$f_{DCO} = 0 \text{ Hz}$ ,<br>Program executes in flash,<br>SELMx = 11, SELS = 1,<br>DIVMx = DIVSx = DIVAx = 11,<br>CPUOFF = 0, SCG0 = 1, SCG1 = 0,<br>OSCOFF = 0 | –55°C to 85°C  | 2.2 V    |     | 5   | 9   | $\mu\text{A}$ |
|                                                     |                                                                                                                                                                                                                                                   | 125°C          |          |     |     | 18  |               |
|                                                     |                                                                                                                                                                                                                                                   | –55°C to 85°C  | 3 V      |     | 6   | 10  |               |
|                                                     |                                                                                                                                                                                                                                                   | 125°C          |          |     |     | 20  |               |
| $I_{AM, 100kHz}$ Active-mode (AM) current (100 kHz) | $f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \neq 100 \text{ kHz}$ ,<br>$f_{ACLK} = 0 \text{ Hz}$ ,<br>Program executes in flash,<br>RSELx = 0, DCOx = 0,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 1                                               | –55°C to 85°C  | 2.2 V    |     | 60  | 85  | $\mu\text{A}$ |
|                                                     |                                                                                                                                                                                                                                                   | 125°C          |          |     |     | 95  |               |
|                                                     |                                                                                                                                                                                                                                                   | –55°C to 85°C  | 3 V      |     | 72  | 95  |               |
|                                                     |                                                                                                                                                                                                                                                   | 125°C          |          |     |     | 125 |               |

(1) All inputs are tied to 0 V or  $V_{CC}$ . Outputs do not source or sink any current.

(2) For  $T_A < 105^\circ\text{C}$ , the currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.

The internal and external load capacitance is chosen to closely match the required 9 pF. For  $T_A > 105^\circ\text{C}$ , the currents are characterized using a 32-kHz external clock source for ACLK..

### Typical Characteristics – Active-Mode Supply Current (Into $DV_{CC} + AV_{CC}$ )

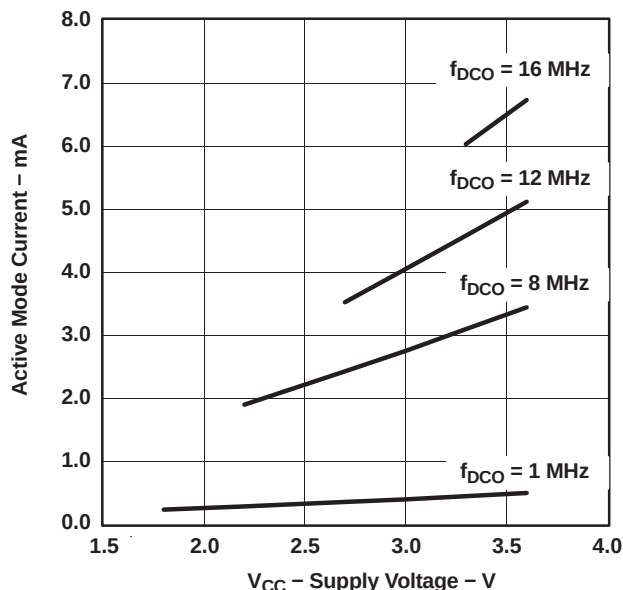


Figure 2. Active-Mode Current vs  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$

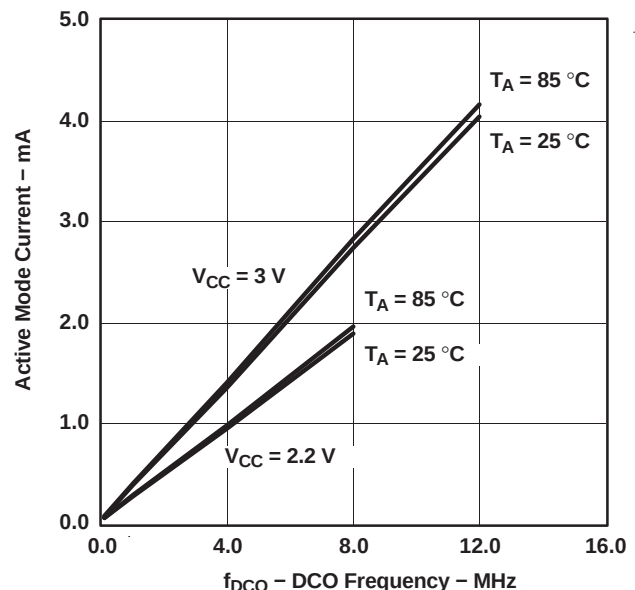


Figure 3. Active-Mode Current vs DCO Frequency

## Low-Power-Mode Supply Currents (Into $DV_{CC}$ + $AV_{CC}$ ) Excluding External Current – Electrical Characteristics<sup>(1) (2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                         | TEST CONDITIONS                                                                                                                                                                        | $T_A$          | $V_{CC}$      | MIN | TYP | MAX | UNIT    |
|-------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------|-----|-----|-----|---------|
| $I_{LPM0, 1MHz}$ Low-power mode 0 (LPM0) current <sup>(3)</sup>   | $f_{MCLK} = 0$ MHz,<br>$f_{SMCLK} = f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32,768$ Hz,<br>BCSCTL1 = CALBC1_1 MHz,<br>DCOCTL = CALDCO_1 MHz,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0 | –55°C to 125°C | 2.2 V         |     | 75  | 90  | $\mu A$ |
|                                                                   |                                                                                                                                                                                        |                | 3 V           |     | 90  | 120 |         |
| $I_{LPM0, 100kHz}$ Low-power mode 0 (LPM0) current <sup>(3)</sup> | $f_{MCLK} = 0$ MHz,<br>$f_{SMCLK} = f_{DCO(0, 0)} \neq 100$ kHz,<br>$f_{ACLK} = 0$ Hz,<br>RSELX = 0, DCOX = 0,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 1                        | –55°C to 125°C | 2.2 V         |     | 37  | 60  | $\mu A$ |
|                                                                   |                                                                                                                                                                                        |                | 3 V           |     | 41  | 75  |         |
| $I_{LPM2}$ Low-power mode 2 (LPM2) current <sup>(4)</sup>         | $f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32,768$ Hz,<br>BCSCTL1 = CALBC1_1 MHz,<br>DCOCTL = CALDCO_1 MHz,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 1,<br>OSCOFF = 0    | –55°C to 85°C  | 2.2 V         |     | 22  | 29  | $\mu A$ |
|                                                                   |                                                                                                                                                                                        | 125°C          |               |     |     | 40  |         |
|                                                                   |                                                                                                                                                                                        | –55°C to 85°C  | 3 V           |     | 25  | 32  |         |
|                                                                   |                                                                                                                                                                                        | 125°C          |               |     |     | 45  |         |
| $I_{LPM3, LFXT1}$ Low-power mode 3 (LPM3) current <sup>(4)</sup>  | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 32,768$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0                                                                  | –55°C          | 2.2 V         |     | 0.7 | 1.4 | $\mu A$ |
|                                                                   |                                                                                                                                                                                        | 25°C           |               |     | 0.7 | 1.4 |         |
|                                                                   |                                                                                                                                                                                        | 85°C           |               |     | 2.8 | 4.5 |         |
|                                                                   |                                                                                                                                                                                        | 125°C          |               |     | 6   | 18  |         |
|                                                                   |                                                                                                                                                                                        | –55°C          | 3 V           |     | 0.9 | 1.5 |         |
|                                                                   |                                                                                                                                                                                        | 25°C           |               |     | 0.9 | 1.5 |         |
|                                                                   |                                                                                                                                                                                        | 85°C           |               |     | 3.0 | 5.0 |         |
|                                                                   |                                                                                                                                                                                        | 125°C          |               |     | 6.5 | 19  |         |
| $I_{LPM3, VLO}$ Low-power mode 3 current, (LPM3) <sup>(4)</sup>   | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK}$ from internal LF oscillator (VLO),<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0                                            | –55°C          | 2.2 V         |     | 0.4 | 1.0 | $\mu A$ |
|                                                                   |                                                                                                                                                                                        | 25°C           |               |     | 0.5 | 1.0 |         |
|                                                                   |                                                                                                                                                                                        | 85°C           |               |     | 2.2 | 4.2 |         |
|                                                                   |                                                                                                                                                                                        | 125°C          |               |     | 5.7 | 18  |         |
|                                                                   |                                                                                                                                                                                        | –55°C          | 3 V           |     | 0.5 | 1.2 |         |
|                                                                   |                                                                                                                                                                                        | 25°C           |               |     | 0.6 | 1.2 |         |
|                                                                   |                                                                                                                                                                                        | 85°C           |               |     | 2.5 | 4.5 |         |
|                                                                   |                                                                                                                                                                                        | 125°C          |               |     | 6.0 | 19  |         |
| $I_{LPM4}$ Low-power mode 4 (LPM4) current <sup>(5)</sup>         | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 0$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 1                                                                       | –55°C          | 2.2 V/<br>3 V |     | 0.1 | 0.5 | $\mu A$ |
|                                                                   |                                                                                                                                                                                        | 25°C           |               |     | 0.1 | 0.5 |         |
|                                                                   |                                                                                                                                                                                        | 85°C           |               |     | 1.9 | 4.0 |         |
|                                                                   |                                                                                                                                                                                        | 125°C          |               |     | 5.5 | 16  |         |

(1) All inputs are tied to 0 V or  $V_{CC}$ . Outputs do not source or sink any current.

(2) For  $T_A < 105^\circ\text{C}$ , the currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF. For  $T_A > 105^\circ\text{C}$ , ACLK was sourced from an external clock source.

(3) Current for brownout and WDT clocked by SMCLK included.

(4) Current for brownout and WDT clocked by ACLK included.

(5) Current for brownout included.

## Schmitt-Trigger Inputs (Ports P1, P2, P3, P4, and RST/NMI<sup>(1)</sup>) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                        | TEST CONDITIONS                                                                                       | T <sub>A</sub> | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|----------------|-----------------|------|-----|------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                          |                                                                                                       | –55°C to 125°C | 2.2 V           | 1.00 |     | 1.65 | V    |
|                                                                                  |                                                                                                       |                | 3 V             | 1.35 |     | 2.25 |      |
| V <sub>IT–</sub> Negative-going input threshold voltage                          |                                                                                                       | –55°C to 125°C | 2.2 V           | .55  |     | 1.20 | V    |
|                                                                                  |                                                                                                       |                | 3 V             | .75  |     | 1.65 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                                                                                       | –55°C to 125°C | 2.2 V           | 0.2  |     | 1.0  | V    |
|                                                                                  |                                                                                                       |                | 3 V             | 0.3  |     | 1.0  |      |
| R <sub>Pull</sub> Pullup/pulldown resistor                                       | For pullup: V <sub>IN</sub> = V <sub>SS</sub> ;<br>For pulldown:<br>V <sub>IN</sub> = V <sub>CC</sub> | –55°C to 125°C |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I</sub> Input capacitance                                                 | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                                  |                |                 |      | 5   |      | pF   |

(1) RST/NMI limit values specified for –55°C to 125°C.

## Inputs (Ports P1 and P2) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS                                                                              | T <sub>A</sub> | V <sub>CC</sub> | MIN | MAX | UNIT |
|----------------------------------------------|----------------------------------------------------------------------------------------------|----------------|-----------------|-----|-----|------|
| t <sub>(int)</sub> External interrupt timing | Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag <sup>(1)</sup> | –55°C to 125°C | 2.2 V/3 V       | 20  |     | ns   |

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width t<sub>(int)</sub> is met. It may be set even with trigger signals shorter than t<sub>(int)</sub>.

## Leakage Current (Ports P1, P2, P3 and P4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                           | TEST CONDITIONS | T <sub>A</sub> | V <sub>CC</sub> | MIN | MAX  | UNIT |
|---------------------------------------------------------------------|-----------------|----------------|-----------------|-----|------|------|
| I <sub>lkg</sub> (P <sub>x.x</sub> ) High-impedance leakage current | (1)(2)          | –55°C to 125°C | 2.2 V/3 V       |     | ±100 | nA   |

(1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## Outputs (Ports P1, P2, P3, and P4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                               | T <sub>A</sub> | V <sub>CC</sub> | MIN                    | MAX                   | UNIT |
|-------------------------------------------|-----------------------------------------------|----------------|-----------------|------------------------|-----------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>OH(max)</sub> = –1.5 mA <sup>(1)</sup> | –55°C to 125°C | 2.2 V           | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>       | V    |
|                                           | I <sub>OH(max)</sub> = –6 mA <sup>(2)</sup>   | –55°C to 125°C |                 | V <sub>CC</sub> – 0.6  | V <sub>CC</sub>       |      |
|                                           | I <sub>OH(max)</sub> = –1.5 mA <sup>(1)</sup> | –55°C to 125°C | 3 V             | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>       |      |
|                                           | I <sub>OH(max)</sub> = –6 mA <sup>(2)</sup>   | –55°C to 125°C |                 | V <sub>CC</sub> – 0.6  | V <sub>CC</sub>       |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>OL(max)</sub> = 1.5 mA <sup>(1)</sup>  | –55°C to 125°C | 2.2 V           | V <sub>SS</sub>        | V <sub>SS</sub> +0.25 | V    |
|                                           | I <sub>OL(max)</sub> = 6 mA <sup>(2)</sup>    | –55°C to 125°C |                 | V <sub>SS</sub>        | V <sub>SS</sub> +0.6  |      |
|                                           | I <sub>OL(max)</sub> = 1.5 mA <sup>(1)</sup>  | –55°C to 125°C | 3 V             | V <sub>SS</sub>        | V <sub>SS</sub> +0.25 |      |
|                                           | I <sub>OL(max)</sub> = 6 mA <sup>(2)</sup>    | –55°C to 125°C |                 | V <sub>SS</sub>        | V <sub>SS</sub> +0.6  |      |

(1) The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.

(2) The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

## Output Frequency (Ports P1, P2, P3, and P4) – Electrical Characteristics

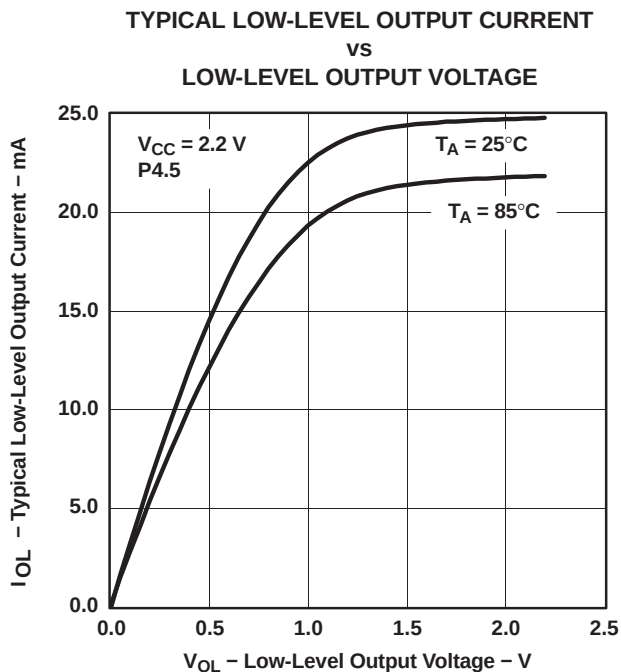
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                           | TEST CONDITIONS                                                                                                    | T <sub>A</sub> | V <sub>CC</sub> | MIN | MAX | UNIT |
|-----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|----------------|-----------------|-----|-----|------|
| f <sub>Px.y</sub> Port output frequency (with load) | P1.4/SMCLK, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ against V <sub>CC</sub> /2 <sup>(1)</sup> <sup>(2)</sup> | –55°C to 125°C | 2.2 V           |     | 10  | MHz  |
|                                                     |                                                                                                                    |                | 3 V             |     | 12  |      |
| f <sub>Port_CLK</sub> Clock output frequency        | P2.0/ACLK, P1.4/SMCLK, C <sub>L</sub> = 20 pF <sup>(2)</sup>                                                       | –55°C to 125°C | 2.2 V           |     | 12  | MHz  |
|                                                     |                                                                                                                    |                | 3 V             |     | 16  |      |

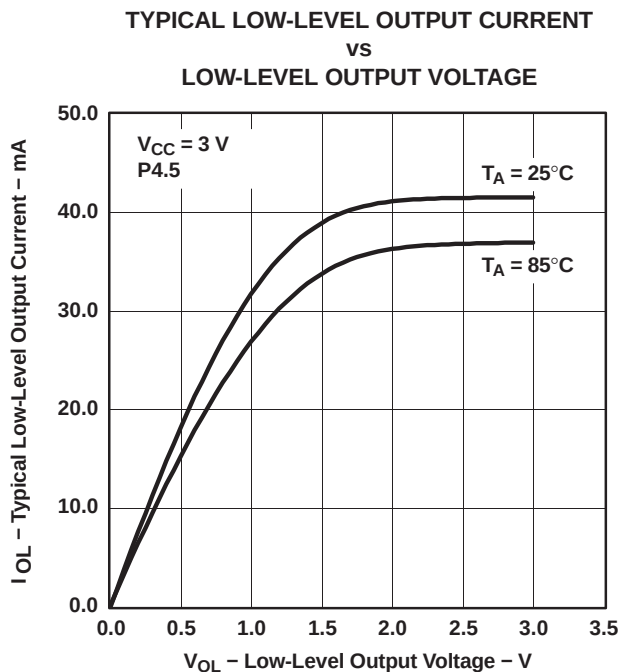
(1) A resistive divider with 2 times 0.5 kΩ between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

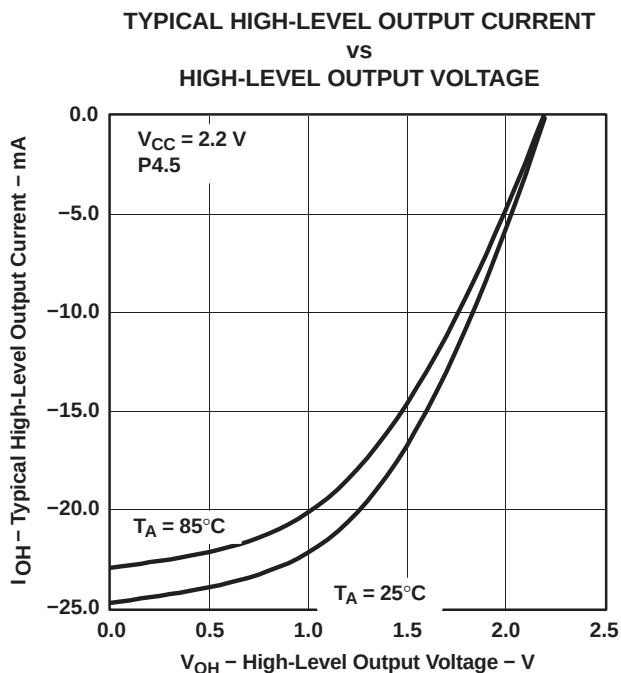
## Typical Characteristics – Outputs



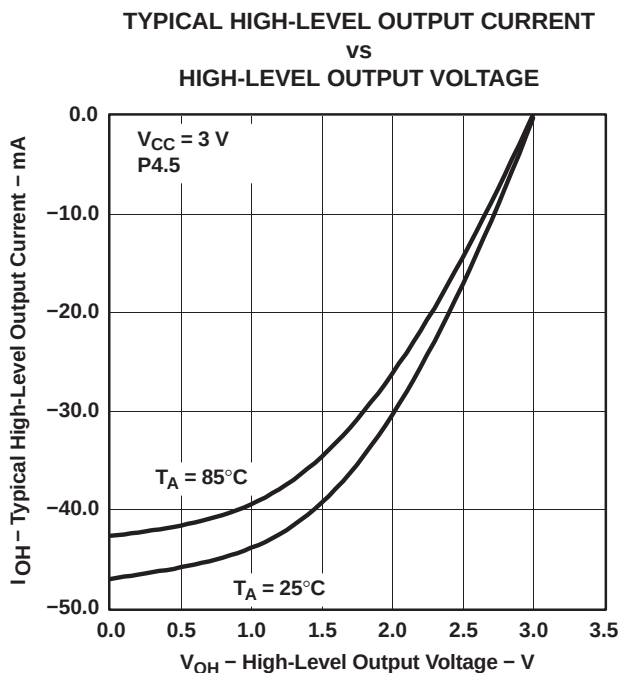
**Figure 4.**



**Figure 5.**



**Figure 6.**



**Figure 7.**

## POR/Brownout Reset (BOR) – Electrical Characteristics<sup>(1) (2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                                       | TEST CONDITIONS              | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP                        | MAX  | UNIT |
|-----------------------------------------------------------------------------------------------------------------|------------------------------|----------------|-----------------|-----|----------------------------|------|------|
| V <sub>CC(start)</sub> See Figure 8                                                                             | dV <sub>CC</sub> /dt ≤ 3 V/s |                |                 |     | 0.7 × V <sub>(B_IT-)</sub> |      | V    |
| V <sub>(B_IT-)</sub> See Figure 8 through Figure 10                                                             | dV <sub>CC</sub> /dt ≤ 3 V/s | –55°C to 125°C |                 |     |                            | 1.71 | V    |
| V <sub>hys(B_IT-)</sub> See Figure 8                                                                            | dV <sub>CC</sub> /dt ≤ 3 V/s | –55°C to 125°C |                 | 70  | 130                        | 210  | mV   |
| t <sub>d(BOR)</sub> See Figure 8                                                                                |                              | –55°C to 125°C |                 |     |                            | 2000 | μs   |
| t <sub>(reset)</sub> Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally |                              | –55°C to 125°C | 2.2 V/3 V       | 2   |                            |      | μs   |

- (1) The current consumption of the brownout module is already included in the I<sub>CC</sub> current consumption data. The voltage level V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub> is ≤ 1.8 V.
- (2) During power up, the CPU begins code execution following a period of t<sub>d(BOR)</sub> after V<sub>CC</sub> = V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub>. The default DCO settings must not be changed until V<sub>CC</sub> ≥ V<sub>CC(min)</sub>, where V<sub>CC(min)</sub> is the minimum supply voltage for the desired operating frequency.

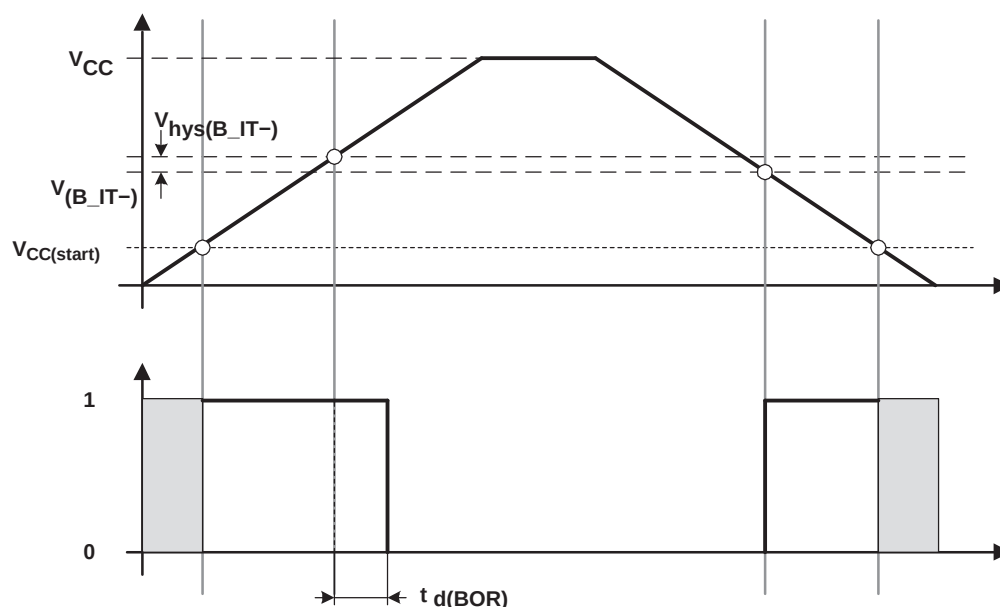


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

## Typical Characteristics - POR/Brownout Reset (BOR)

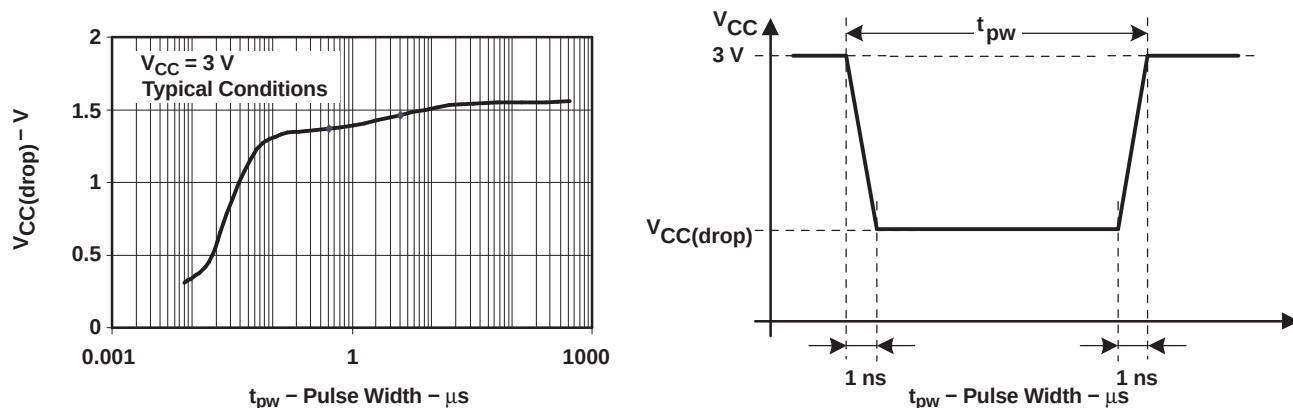


Figure 9.  $V_{CC(drop)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

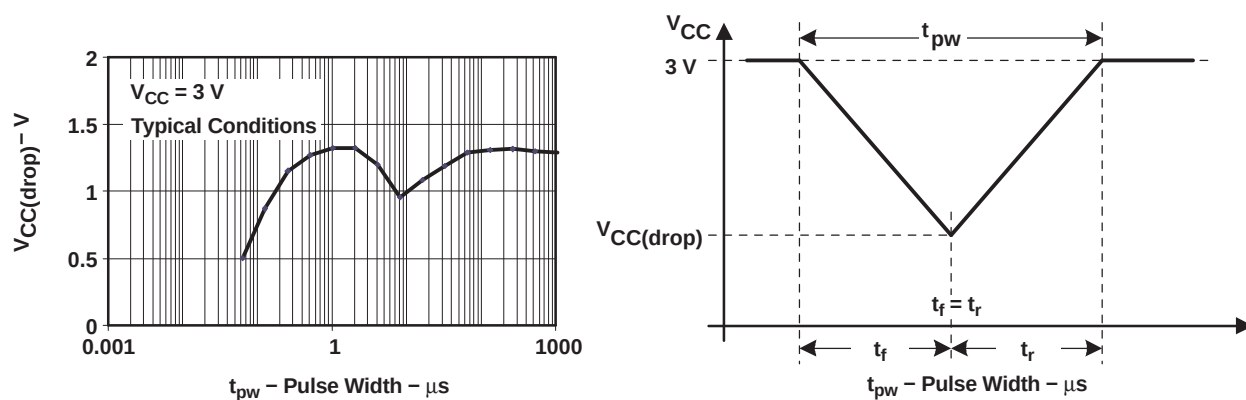


Figure 10.  $V_{CC(drop)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

## Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S<sub>DCO</sub>.
- Modulation control bits MODx select how often f<sub>DCO(RSEL,DCO+1)</sub> is used within the period of 32 DCOCLK cycles. The frequency f<sub>DCO(RSEL,DCO)</sub> is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{\text{DCO(RSEL,DCO)}} \times f_{\text{DCO(RSEL,DCO)} + 1}}{\text{MOD} \times f_{\text{DCO(RSEL,DCO)}} + (32 - \text{MOD}) \times f_{\text{DCO(RSEL,DCO)} + 1}}$$

## DCO Frequency – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                      | TEST CONDITIONS                                                              | T <sub>A</sub> | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT  |
|----------------------------------------------------------------|------------------------------------------------------------------------------|----------------|-----------------|------|-----|------|-------|
| V <sub>CC</sub> Supply voltage range                           | RSELx < 14                                                                   | –55°C to 125°C |                 | 1.8  |     | 3.6  | V     |
|                                                                | RSELx = 14                                                                   | –55°C to 125°C |                 | 2.2  |     | 3.6  |       |
|                                                                | RSELx = 15                                                                   | –55°C to 125°C |                 | 3.0  |     | 3.6  |       |
| f <sub>DCO(0,0)</sub> DCO frequency (0, 0)                     | RSELx = 0, DCOx = 0, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.06 |     | 0.14 | MHz   |
| f <sub>DCO(0,3)</sub> DCO frequency (0, 3)                     | RSELx = 0, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.07 |     | 0.17 | MHz   |
| f <sub>DCO(1,3)</sub> DCO frequency (1, 3)                     | RSELx = 1, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.10 |     | 0.20 | MHz   |
| f <sub>DCO(2,3)</sub> DCO frequency (2, 3)                     | RSELx = 2, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.14 |     | 0.28 | MHz   |
| f <sub>DCO(3,3)</sub> DCO frequency (3, 3)                     | RSELx = 3, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.20 |     | 0.40 | MHz   |
| f <sub>DCO(4,3)</sub> DCO frequency (4, 3)                     | RSELx = 4, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.28 |     | 0.54 | MHz   |
| f <sub>DCO(5,3)</sub> DCO frequency (5, 3)                     | RSELx = 5, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.39 |     | 0.77 | MHz   |
| f <sub>DCO(6,3)</sub> DCO frequency (6, 3)                     | RSELx = 6, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.54 |     | 1.06 | MHz   |
| f <sub>DCO(7,3)</sub> DCO frequency (7, 3)                     | RSELx = 7, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 0.80 |     | 1.50 | MHz   |
| f <sub>DCO(8,3)</sub> DCO frequency (8, 3)                     | RSELx = 8, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 1.10 |     | 2.10 | MHz   |
| f <sub>DCO(9,3)</sub> DCO frequency (9, 3)                     | RSELx = 9, DCOx = 3, MODx = 0                                                | –55°C to 125°C | 2.2 V/3 V       | 1.60 |     | 3.00 | MHz   |
| f <sub>DCO(10,3)</sub> DCO frequency (10, 3)                   | RSELx = 10, DCOx = 3, MODx = 0                                               | –55°C to 125°C | 2.2 V/3 V       | 2.50 |     | 4.30 | MHz   |
| f <sub>DCO(11,3)</sub> DCO frequency (11, 3)                   | RSELx = 11, DCOx = 3, MODx = 0                                               | –55°C to 125°C | 2.2 V/3 V       | 3.00 |     | 5.50 | MHz   |
| f <sub>DCO(12,3)</sub> DCO frequency (12, 3)                   | RSELx = 12, DCOx = 3, MODx = 0                                               | –55°C to 125°C | 2.2 V/3 V       | 4.30 |     | 7.30 | M Hz  |
| f <sub>DCO(13,3)</sub> DCO frequency (13, 3)                   | RSELx = 13, DCOx = 3, MODx = 0                                               | –55°C to 125°C | 2.2 V/3 V       | 6.00 |     | 9.60 | MHz   |
| f <sub>DCO(14,3)</sub> DCO frequency (14, 3)                   | RSELx = 14, DCOx = 3, MODx = 0                                               | –55°C to 125°C | 2.2 V/3 V       | 8.60 |     | 13.9 | MHz   |
| f <sub>DCO(15,3)</sub> DCO frequency (15, 3)                   | RSELx = 15, DCOx = 3, MODx = 0                                               | –55°C to 125°C | 3 V             | 12.0 |     | 18.5 | MHz   |
| f <sub>DCO(15,7)</sub> DCO frequency (15, 7)                   | RSELx = 15, DCOx = 7, MODx = 0                                               | –55°C to 125°C | 3 V             | 16.0 |     | 26.0 | MHz   |
| S <sub>RSEL</sub> Frequency step between range RSEL and RSEL+1 | S <sub>RSEL</sub> = f <sub>DCO(RSEL+1,DCO)</sub> /f <sub>DCO(RSEL,DCO)</sub> | –55°C to 125°C | 2.2 V/3 V       |      |     | 1.55 | ratio |

## DCO Frequency – Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        |                                                | TEST CONDITIONS                                                                | T <sub>A</sub> | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT  |
|------------------|------------------------------------------------|--------------------------------------------------------------------------------|----------------|-----------------|------|------|------|-------|
| S <sub>DCO</sub> | Frequency step<br>between tap DCO and<br>DCO+1 | S <sub>DCO</sub> =<br>f <sub>DCO(RSEL,DCO+1)</sub> /f <sub>DCO(RSEL,DCO)</sub> | –55°C to 125°C | 2.2 V/3 V       | 1.05 | 1.08 | 1.12 | ratio |
| Duty cycle       |                                                | Measured at P1.4/SMCLK                                                         | –55°C to 125°C | 2.2 V/3 V       | 40   | 50   | 60   | %     |

## Calibrated DCO Frequencies (Tolerance at Calibration) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                         | TEST CONDITIONS                                                        | T <sub>A</sub> | V <sub>CC</sub> | MIN   | TYP  | MAX   | UNIT |
|---------------------------------------------------|------------------------------------------------------------------------|----------------|-----------------|-------|------|-------|------|
| Frequency tolerance at calibration                |                                                                        | 25°C           | 3 V             | –1    | ±0.2 | 1     | %    |
| f <sub>CAL(1 MHz)</sub> 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | 25°C           | 3 V             | 0.990 | 1    | 1.010 | MHz  |
| f <sub>CAL(8 MHz)</sub> 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | 25°C           | 3 V             | 7.920 | 8    | 8.080 | MHz  |
| f <sub>CAL(12 MHz)</sub> 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | 25°C           | 3 V             | 11.88 | 12   | 12.12 | MHz  |
| f <sub>CAL(16 MHz)</sub> 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | 25°C           | 3 V             | 15.84 | 16   | 16.16 | MHz  |

## Calibrated DCO Frequencies (Tolerance Over Temperature) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                        | TEST CONDITIONS                                                        | T <sub>A</sub> | V <sub>CC</sub> | MIN   | TYP  | MAX   | UNIT |
|--------------------------------------------------|------------------------------------------------------------------------|----------------|-----------------|-------|------|-------|------|
| 1-MHz tolerance over temperature                 |                                                                        | –55°C to 125°C | 3 V             | –2.5  | ±0.5 | 2.5   | %    |
| 8-MHz tolerance over temperature                 |                                                                        | –55°C to 125°C | 3 V             | –2.5  | ±1.0 | 2.5   | %    |
| 12-MHz tolerance over temperature                |                                                                        | –55°C to 125°C | 3 V             | –2.5  | ±1.0 | 2.5   | %    |
| 16-MHz tolerance over temperature                |                                                                        | –55°C to 125°C | 3 V             | –3.0  | ±2.0 | 3.0   | %    |
| f <sub>CAL(1MHz)</sub> 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | –55°C to 125°C | 2.2 V           | 0.970 | 1    | 1.030 | MHz  |
|                                                  |                                                                        |                | 3 V             | 0.975 | 1    | 1.025 |      |
|                                                  |                                                                        |                | 3.6 V           | 0.970 | 1    | 1.030 |      |
| f <sub>CAL(8MHz)</sub> 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | –55°C to 125°C | 2.2 V           | 7.760 | 8    | 8.400 | MHz  |
|                                                  |                                                                        |                | 3 V             | 7.800 | 8    | 8.200 |      |
|                                                  |                                                                        |                | 3.6 V           | 7.600 | 8    | 8.240 |      |
| f <sub>CAL(12MHz)</sub> 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | –55°C to 125°C | 2.2 V           | 11.70 | 12   | 12.30 | MHz  |
|                                                  |                                                                        |                | 3 V             | 11.70 | 12   | 12.30 |      |
|                                                  |                                                                        |                | 3.6 V           | 11.70 | 12   | 12.30 |      |
| f <sub>CAL(16MHz)</sub> 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | –55°C to 125°C | 3 V             | 15.52 | 16   | 16.48 | MHz  |
|                                                  |                                                                        |                | 3.6 V           | 15.00 | 16   | 16.48 |      |

## Calibrated DCO Frequencies (Tolerance Over Supply Voltage $V_{CC}$ ) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                        | $T_A$ | $V_{CC}$       | MIN   | TYP | MAX   | UNIT |
|-------------------------------------------|------------------------------------------------------------------------|-------|----------------|-------|-----|-------|------|
| 1-MHz tolerance over $V_{CC}$             |                                                                        | 25°C  | 1.8 V to 3.6 V | –3    | ±2  | 3     | %    |
| 8-MHz tolerance over $V_{CC}$             |                                                                        | 25°C  | 1.8 V to 3.6 V | –3    | ±2  | 3     | %    |
| 12-MHz tolerance over $V_{CC}$            |                                                                        | 25°C  | 2.2 V to 3.6 V | –3    | ±2  | 3     | %    |
| 16-MHz tolerance over $V_{CC}$            |                                                                        | 25°C  | 3 V to 3.6 V   | –6    | ±2  | 3     | %    |
| $f_{CAL(1MHz)}$ 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | 25°C  | 1.8 V to 3.6 V | 0.970 | 1   | 1.030 | MHz  |
| $f_{CAL(8MHz)}$ 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | 25°C  | 1.8 V to 3.6 V | 7.760 | 8   | 8.240 | MHz  |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | 25°C  | 2.2 V to 3.6 V | 11.64 | 12  | 12.36 | MHz  |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | 25°C  | 3 V to 3.6 V   | 15.00 | 16  | 16.48 | MHz  |

## Calibrated DCO Frequencies (Overall Tolerance) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                        | $T_A$          | $V_{CC}$       | MIN   | TYP | MAX   | UNIT |
|-------------------------------------------|------------------------------------------------------------------------|----------------|----------------|-------|-----|-------|------|
| 1-MHz tolerance over temperature          |                                                                        | –55°C to 125°C | 1.8 V to 3.6 V | –5    | ±2  | +5    | %    |
| 8-MHz tolerance over temperature          |                                                                        | –55°C to 125°C | 1.8 V to 3.6 V | –5    | ±2  | +5    | %    |
| 12-MHz tolerance over temperature         |                                                                        | –55°C to 125°C | 2.2 V to 3.6 V | –5    | ±2  | +5    | %    |
| 16-MHz tolerance over temperature         |                                                                        | –55°C to 125°C | 3 V to 3.6 V   | –6    | ±3  | +6    | %    |
| $f_{CAL(1MHz)}$ 1-MHz calibration value   | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>Gating time: 5 ms   | –55°C to 125°C | 1.8 V to 3.6 V | .950  | 1   | 1.050 | MHz  |
| $f_{CAL(8MHz)}$ 8-MHz calibration value   | BCSCTL1 = CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>Gating time: 5 ms   | –55°C to 125°C | 1.8 V to 3.6 V | 7.6   | 8   | 8.4   | MHz  |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>Gating time: 5 ms | –55°C to 125°C | 2.2 V to 3.6 V | 11.4  | 12  | 12.6  | MHz  |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>Gating time: 2 ms | –55°C to 125°C | 3 V to 3.6 V   | 15.00 | 16  | 17.00 | MHz  |

## Typical Characteristics – Calibrated 1-MHz DCO Frequency

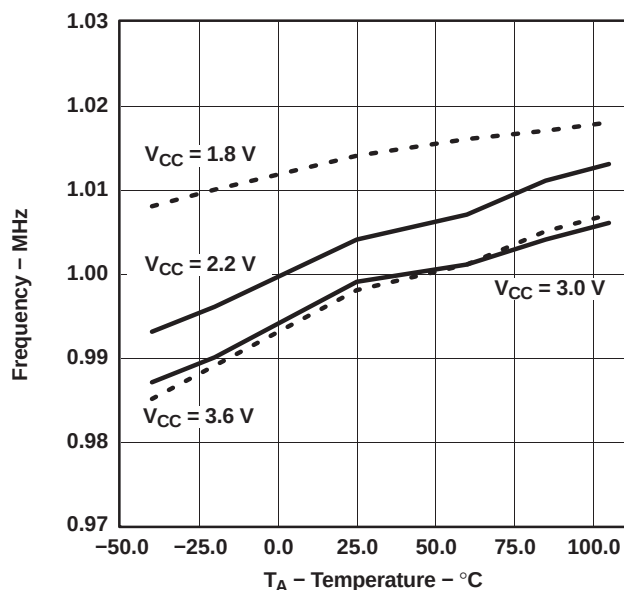


Figure 11. Calibrated 1-MHz Frequency vs Temperature

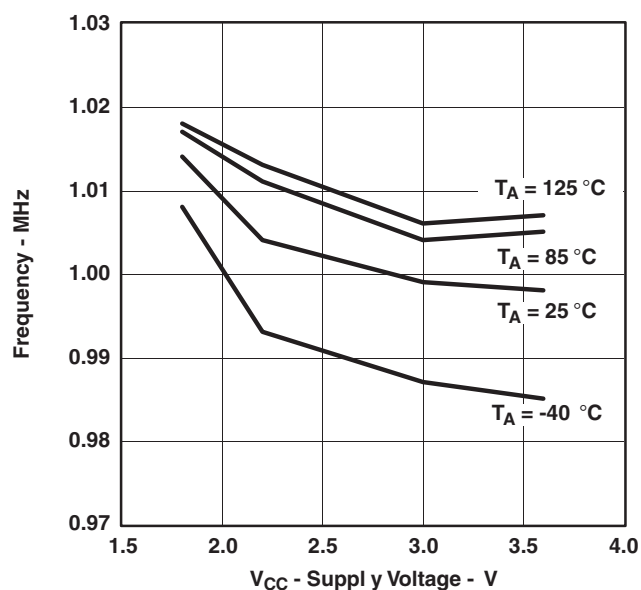


Figure 12. Calibrated 1-MHz Frequency vs V<sub>CC</sub>

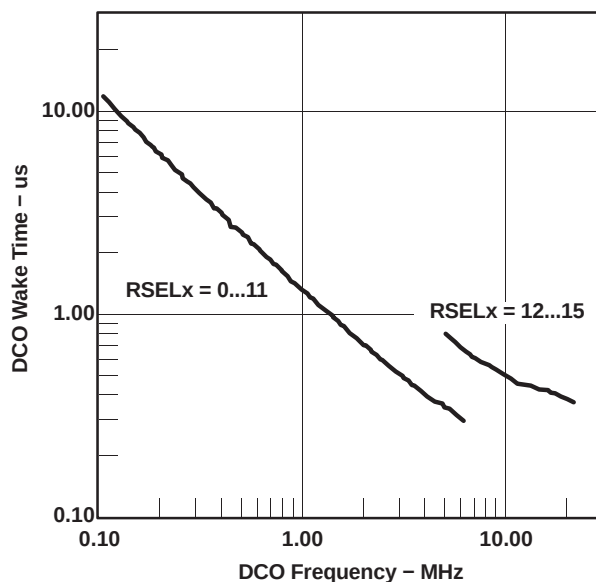
## Wake-Up From Lower-Power Modes (LPM3/4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                 | TEST CONDITIONS                                | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP                                              | MAX | UNIT |
|---------------------------------------------------------------------------|------------------------------------------------|----------------|-----------------|-----|--------------------------------------------------|-----|------|
| t <sub>DCO,LPM3/4</sub> DCO clock wake-up time from LPM3/4 <sup>(1)</sup> | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ,   | -55°C to 125°C | 2.2 V/3 V       |     |                                                  | 2   | μs   |
|                                                                           | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ,   | -55°C to 125°C | 2.2 V/3 V       |     |                                                  | 1.5 |      |
|                                                                           | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, | -55°C to 125°C | 3 V             |     |                                                  | 1   |      |
|                                                                           | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, | -55°C to 125°C | 3 V             |     |                                                  | 1   |      |
| t <sub>CPU,LPM3/4</sub> CPU wake-up time from LPM3/4 <sup>(2)</sup>       |                                                |                |                 |     | 1/f <sub>MCLK</sub> + t <sub>Clock,L</sub> PM3/4 |     |      |

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- (2) Parameter applicable only if DCOCLK is used for MCLK.

## Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4



**Figure 13. Clock Wake-Up Time From LPM3 vs DCO Frequency**

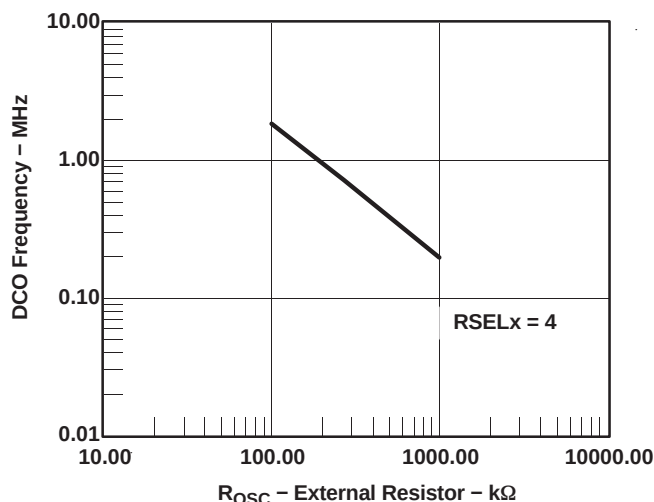
## DCO With External Resistor $R_{OSC}$ – Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

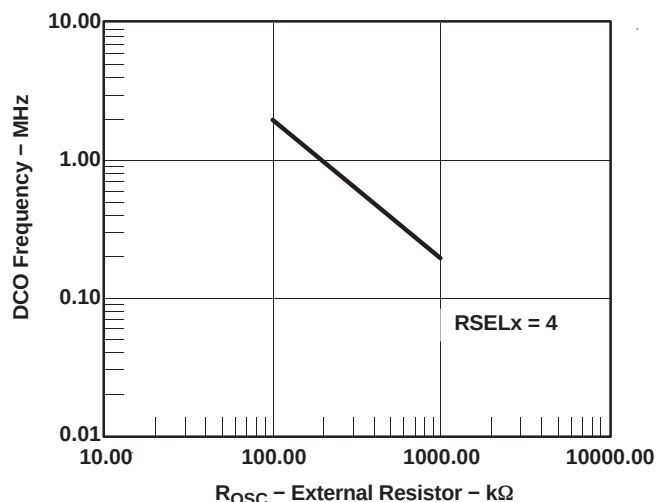
| PARAMETER      |                                     | TEST CONDITIONS                                                      | $V_{CC}$  | TYP       | UNIT                |
|----------------|-------------------------------------|----------------------------------------------------------------------|-----------|-----------|---------------------|
| $f_{DCO,ROSC}$ | DCO output frequency with $R_{OSC}$ | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0,<br>$T_A = 25^\circ\text{C}$ | 2.2 V     | 1.8       | MHz                 |
|                |                                     |                                                                      | 3 V       | 1.95      |                     |
| $D_t$          | Temperature drift                   | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0                              | 2.2 V/3 V | $\pm 0.1$ | %/ $^\circ\text{C}$ |
| $D_V$          | Drift with $V_{CC}$                 | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0                              | 2.2 V/3 V | 10        | %/V                 |

(1)  $R_{OSC} = 100\text{k}\Omega$ . Metal film resistor, type 0257. 0.6 watt with 1% tolerance and  $T_K = \pm 50\text{ppm}/^\circ\text{C}$

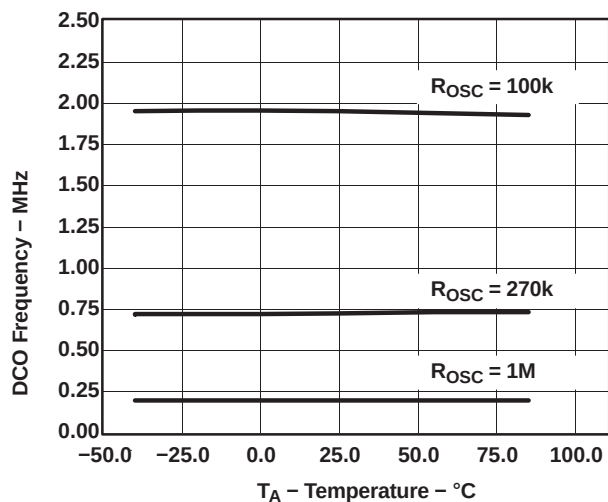
# **Typical Characteristics - DCO With External Resistor $R_{OSC}$**



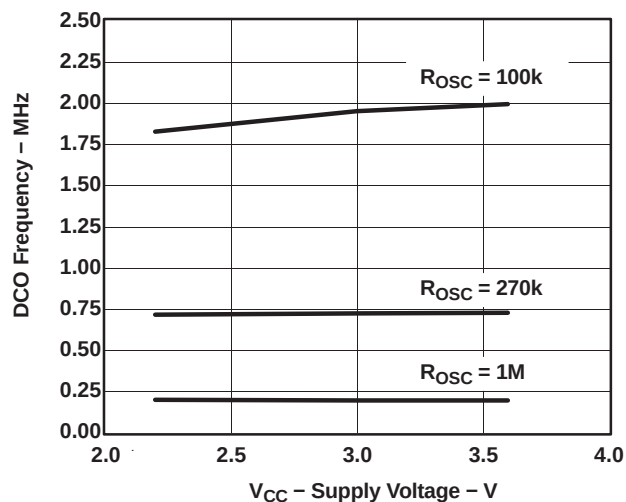
**Figure 14. DCO Frequency vs  $R_{OSC}$ ,  
 $V_{CC} = 2.2$  V,  $T_A = 25^\circ\text{C}$**



**Figure 15. DCO Frequency vs  $R_{OSC}$ ,  
 $V_{CC} = 3.0$  V,  $T_A = 25^\circ\text{C}$**



**Figure 16. DCO Frequency vs Temperature,  $V_{CC} = 3.0$  V**



**Figure 17. DCO Frequency vs  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**

## Crystal Oscillator (LFXT1) Low-Frequency Modes – Electrical Characteristics<sup>(1) (2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                     | TEST CONDITIONS                                                                      | T <sub>A</sub> | V <sub>CC</sub> | MIN    | TYP    | MAX    | UNIT |
|-----------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|----------------|-----------------|--------|--------|--------|------|
| f <sub>LFXT1,LF</sub> LFXT1 oscillator crystal frequency, LF mode 0, 1                        | XTS = 0, LFXT1Sx = 0 or 1                                                            | –55°C to 105°C | 1.8 V to 3.6 V  |        | 32,768 |        | Hz   |
| f <sub>LFXT1,LF,logic</sub> LFXT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, LFXT1Sx = 3                                                                 | –55°C to 125°C | 1.8 V to 3.6 V  | 10,000 | 32,768 | 50,000 | Hz   |
| OA <sub>LF</sub> Oscillation allowance for LF crystals                                        | XTS = 0, LFXT1Sx = 0; f <sub>LFXT1,LF</sub> = 32,768 kHz, C <sub>L,eff</sub> = 6 pF  | –55°C to 105°C |                 |        | 500    |        | kΩ   |
|                                                                                               | XTS = 0, LFXT1Sx = 0; f <sub>LFXT1,LF</sub> = 32,768 kHz, C <sub>L,eff</sub> = 12 pF | –55°C to 105°C |                 |        | 200    |        |      |
| C <sub>L,eff</sub> Integrated effective load capacitance, LF mode <sup>(3)</sup>              | XTS = 0                                                                              | –55°C to 105°C |                 |        | 1      |        | pF   |
|                                                                                               |                                                                                      |                |                 |        | 5.5    |        |      |
|                                                                                               |                                                                                      |                |                 |        | 8.5    |        |      |
|                                                                                               |                                                                                      |                |                 |        | 11     |        |      |
| Duty Cycle LF mode                                                                            | XTS = 0, Measured at P1.4/ACLK, f <sub>LFXT1,LF</sub> = 32,768 Hz                    | –55°C to 125°C | 2.2 V/3 V       | 30     | 50     | 70     | %    |
| f <sub>Fault,LF</sub> Oscillator fault frequency threshold, LF mode <sup>(4)</sup>            | XTS = 0, LFXT1Sx = 3 <sup>(5)</sup>                                                  | –55°C to 125°C | 2.2 V/3 V       | 10     |        | 10,000 | Hz   |

- (1) To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
  - (a) Keep as short of a trace as possible between the device and the crystal.
  - (b) Design a good ground plane around the oscillator pins.
  - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Use of the LFXT1 Crystal Oscillator with T<sub>A</sub> > 105°C is not guaranteed. It is recommended that an external digital clock source or the internal DCO is used to provide clocking.
- (3) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
- (4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (5) Measured with logic-level input frequency, but also applies to operation with crystals with T<sub>A</sub> < 105°C.

## Internal Very-Low-Power, Low-Frequency Oscillator (VLO) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                              | TEST CONDITIONS | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------|-----------------|----------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub> VLO frequency                                         |                 | –55°C to 85°C  | 2.2 V/3 V       | 4   | 12  | 20  | kHz  |
|                                                                        |                 | 125°C          | 2.2 V/3 V       |     |     | 22  |      |
| df <sub>VLO</sub> /dT VLO frequency temperature drift                  | <sup>(1)</sup>  | –55°C to 125°C | 2.2 V/3 V       | 0.5 |     |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> VLO frequency supply voltage drift | <sup>(2)</sup>  | 25°C           | 1.8 V – 3.6V    |     | 4   |     | %/V  |

- (1) Calculated using the box method:  
I Version: [MAX(–55...85°C) – MIN(–55...85°C)]/MIN(55...85°C)/[85°C – (–55°C)]  
T Version: [MAX(–55...125°C) – MIN(–55...125°C)]/MIN(–55...125°C)/[125°C – (–55°C)]
- (2) Calculated using the box method: [MAX(1.8...3.6 V) – MIN(1.8...3.6 V)]/MIN(1.8...3.6 V)/(3.6 V – 1.8 V)

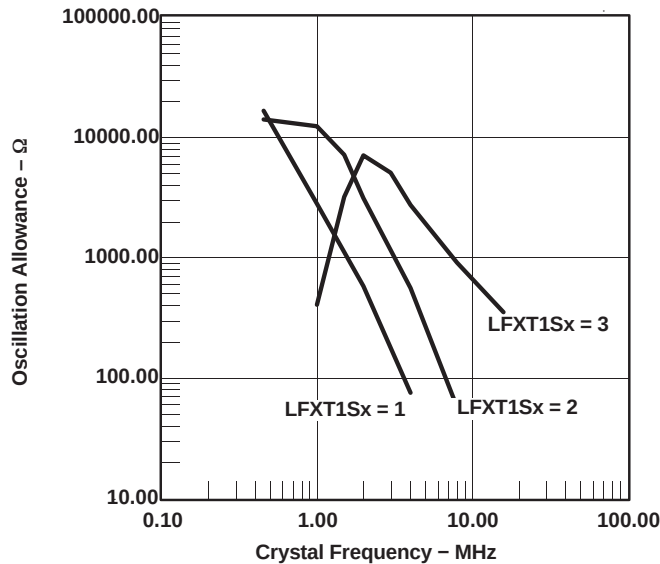
## Crystal Oscillator (LFXT1) High Frequency Modes – Electrical Characteristics<sup>(1) (2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

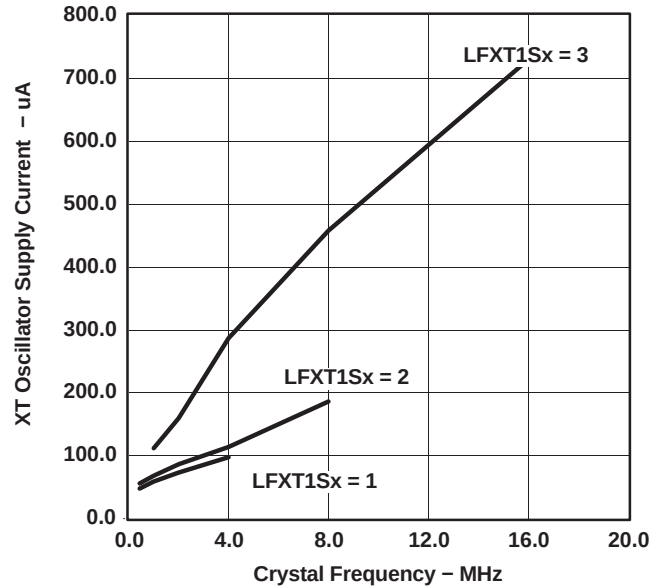
| PARAMETER                    |                                                                     | TEST CONDITIONS                                                                   | T <sub>A</sub> | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT |
|------------------------------|---------------------------------------------------------------------|-----------------------------------------------------------------------------------|----------------|-----------------|------|-----|-----|------|
| f <sub>LFXT1, HF0</sub>      | LFXT1 oscillator crystal frequency, HF mode 0                       | XTS = 1, LFXT1Sx = 0                                                              | –55°C to 125°C | 1.8 V to 3.6 V  | 0.4  |     | 1   | MHz  |
| f <sub>LFXT1, HF1</sub>      | LFXT1 oscillator crystal frequency, HF mode 1                       | XTS = 1, LFXT1Sx = 1                                                              | –55°C to 125°C | 1.8 V to 3.6 V  | 1    |     | 4   | MHz  |
| f <sub>LFXT1, HF2</sub>      | LFXT1 oscillator crystal frequency, HF mode 2                       | XTS = 1, LFXT1Sx = 2                                                              | –55°C to 125°C | 1.8 V to 3.6 V  | 2    |     | 10  | MHz  |
|                              |                                                                     |                                                                                   |                | 2.2 V to 3.6 V  | 2    |     | 12  |      |
|                              |                                                                     |                                                                                   |                | 3 V to 3.6 V    | 2    |     | 16  |      |
| f <sub>LFXT1, HF,logic</sub> | LFXT1 oscillator logic-level square-wave input frequency, HF mode   | XTS = 1, LFXT1Sx = 3                                                              | –55°C to 125°C | 1.8 V to 3.6 V  | 0.4  |     | 10  | MHz  |
|                              |                                                                     |                                                                                   |                | 2.2 V to 3.6 V  | 0.4  |     | 12  |      |
|                              |                                                                     |                                                                                   |                | 3 V to 3.6 V    | 0.4  |     | 16  |      |
| OA <sub>HF</sub>             | Oscillation allowance for HF crystals (see Figure 18 and Figure 19) | XTS = 0, LFXT1Sx = 0; f <sub>LFXT1, HF</sub> = 1 MHz, C <sub>L, eff</sub> = 15 pF | –55°C to 125°C |                 | 2700 |     |     | Ω    |
|                              |                                                                     | XTS = 0, LFXT1Sx = 1 f <sub>LFXT1, HF</sub> = 4 MHz, C <sub>L, eff</sub> = 15 pF  |                |                 | 800  |     |     |      |
|                              |                                                                     | XTS = 0, LFXT1Sx = 2 f <sub>LFXT1, HF</sub> = 16 MHz, C <sub>L, eff</sub> = 15 pF |                |                 | 300  |     |     |      |
| C <sub>L, eff</sub>          | Integrated effective load capacitance, HF mode <sup>(3)</sup>       | XTS = 1 <sup>(4)</sup>                                                            | –55°C to 125°C |                 | 1    |     |     | pF   |
| Duty Cycle                   | HF mode                                                             | XTS = 1, Measured at P1.4/ACLK, f <sub>LFXT1, HF</sub> = 10 MHz                   | –55°C to 125°C | 2.2 V/3 V       | 40   | 50  | 60  | %    |
|                              |                                                                     | XTS = 1, Measured at P1.4/ACLK, f <sub>LFXT1, HF</sub> = 16 MHz                   | –55°C to 125°C |                 | 40   | 50  | 60  |      |
| f <sub>Fault, HF</sub>       | Oscillator fault frequency, HF mode <sup>(5)</sup>                  | XTS = 1, LFXT1Sx = 3 <sup>(6)</sup>                                               | –55°C to 125°C | 2.2 V/3 V       | 30   |     | 300 | kHz  |

- (1) To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
  - (a) Keep as short of a trace as possible between the device and the crystal.
  - (b) Design a good ground plane around the oscillator pins.
  - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Use of the LFXT1 Crystal Oscillator with T<sub>A</sub> > 105°C is not guaranteed. It is recommended that an external digital clock source or the internal DCO is used to provide clocking.
- (3) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
- (4) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (5) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (6) Measured with logic-level input frequency, but also applies to operation with crystals

## Typical Characteristics – LFXT1 Oscillator in HF Mode (XTS = 1)



**Figure 18. Oscillation Allowance vs Crystal Frequency,  $C_{L,eff} = 15$  pF,  $T_A = 25^\circ\text{C}$**



**Figure 19. XT Oscillator Supply Current vs Crystal Frequency,  $C_{L,eff} = 15$  pF,  $T_A = 25^\circ\text{C}$**

## Timer\_A – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                            | TEST CONDITIONS                                                                 | $T_A$                                      | $V_{CC}$  | MIN | MAX | UNIT |
|--------------------------------------|---------------------------------------------------------------------------------|--------------------------------------------|-----------|-----|-----|------|
| $f_{TA}$ Timer_A clock frequency     | Internal: SMCLK, ACLK,<br>External: TACLK, INCLK,<br>Duty cycle = 50% $\pm$ 10% | $-55^\circ\text{C}$ to $125^\circ\text{C}$ | 2.2 V     |     | 10  | MHz  |
|                                      |                                                                                 |                                            | 3 V       |     | 16  |      |
| $t_{TA,cap}$ Timer_A, capture timing | TA0, TA1, TA2                                                                   | $-55^\circ\text{C}$ to $125^\circ\text{C}$ | 2.2 V/3 V | 20  |     | ns   |

## Timer\_B – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                            | TEST CONDITIONS                                                          | $T_A$                                      | $V_{CC}$  | MIN | MAX | UNIT |
|--------------------------------------|--------------------------------------------------------------------------|--------------------------------------------|-----------|-----|-----|------|
| $f_{TB}$ Timer_B clock frequency     | Internal: SMCLK, ACLK,<br>External: TBCLK,<br>Duty Cycle = 50% $\pm$ 10% | $-55^\circ\text{C}$ to $125^\circ\text{C}$ | 2.2 V     |     | 10  | MHz  |
|                                      |                                                                          |                                            | 3 V       |     | 16  |      |
| $t_{TB,cap}$ Timer_B, capture timing | TB0, TB1, TB2                                                            | $-55^\circ\text{C}$ to $125^\circ\text{C}$ | 2.2 V/3 V | 20  |     | ns   |

## USCI (UART Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                 | TEST CONDITIONS                                                     | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX                 | UNIT |
|---------------------------------------------------------------------------|---------------------------------------------------------------------|----------------|-----------------|-----|-----|---------------------|------|
| f <sub>USCI</sub> USCI input clock frequency                              | Internal: SMCLK, ACLK,<br>External: UCLK;<br>Duty cycle = 50% ± 10% | –55°C to 125°C |                 |     |     | f <sub>SYSTEM</sub> | MHz  |
| f <sub>BITCLK</sub> BITCLK clock frequency<br>(equals baud rate in MBaud) |                                                                     | –55°C to 125°C | 2.2 V/3 V       |     |     | 1                   | MHz  |
| t <sub>r</sub> UART receive deglitch time <sup>(1)</sup>                  |                                                                     | –55°C to 125°C | 2.2 V           | 50  | 150 | 600                 | ns   |
|                                                                           |                                                                     |                | 3 V             | 50  | 150 | 600                 |      |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their width should exceed the maximum specification of the deglitch time.

## USCI (SPI Master Mode) – Electrical Characteristics

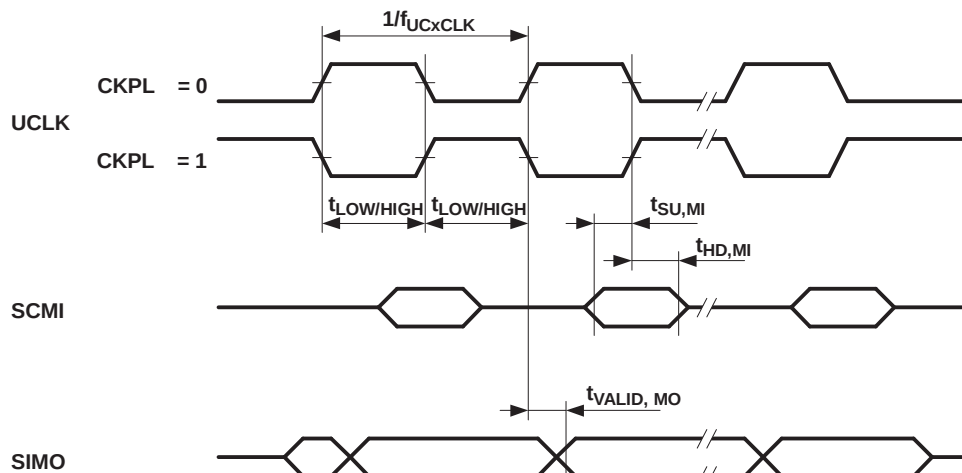
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 20](#) and [Figure 21](#))

| PARAMETER                                         | TEST CONDITIONS                                    | T <sub>A</sub> | V <sub>CC</sub> | MIN | MAX                 | UNIT |
|---------------------------------------------------|----------------------------------------------------|----------------|-----------------|-----|---------------------|------|
| f <sub>USCI</sub> USCI input clock frequency      | SMCLK, ACLK,<br>Duty cycle = 50% ± 10%             | –55°C to 125°C |                 |     | f <sub>SYSTEM</sub> | MHz  |
| t <sub>SU,MI</sub> SOMI input data setup time     |                                                    | –55°C to 125°C | 2.2 V           | 110 |                     | ns   |
|                                                   |                                                    |                | 3 V             | 75  |                     |      |
| t <sub>HD,MI</sub> SOMI input data hold time      |                                                    | –55°C to 125°C | 2.2 V           | 0   |                     | ns   |
|                                                   |                                                    |                | 3 V             | 0   |                     |      |
| t <sub>VALID,MO</sub> SIMO output data valid time | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF | –55°C to 125°C | 2.2 V           |     | 30                  | ns   |
|                                                   |                                                    |                | 3 V             |     | 20                  |      |

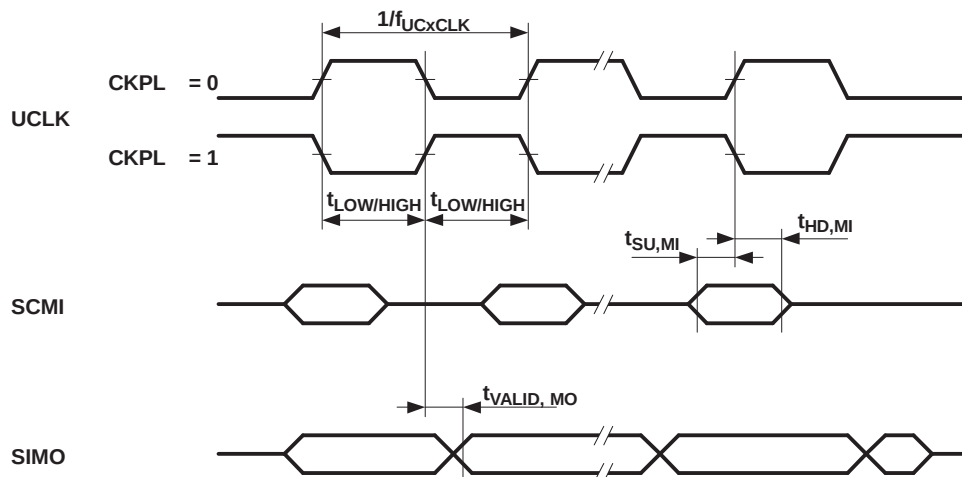
## USCI (SPI Slave Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 22](#) and [Figure 23](#))

| PARAMETER                                                                    | TEST CONDITIONS                                    | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------------|----------------------------------------------------|----------------|-----------------|-----|-----|-----|------|
| t <sub>STE,LEAD</sub> STE lead time,<br>STE low to clock                     |                                                    |                | 2.2 V/3 V       | 50  |     |     | ns   |
| t <sub>STE,LAG</sub> STE lag time,<br>Last clock to STE high                 |                                                    | –55°C to 125°C | 2.2 V/3 V       | 10  |     |     | ns   |
| t <sub>STE,ACC</sub> STE access time,<br>STE low to SOMI data out            |                                                    |                | 2.2 V/3 V       | 50  |     |     | ns   |
| t <sub>STE,DIS</sub> STE disable time,<br>STE high to SOMI high<br>impedance |                                                    |                | 2.2 V/3 V       | 50  |     |     | ns   |
| t <sub>SU,SI</sub> SIMO input data setup time                                |                                                    | –55°C to 125°C | 2.2 V           | 20  |     |     | ns   |
|                                                                              |                                                    |                | 3 V             | 15  |     |     |      |
| t <sub>HD,SI</sub> SIMO input data hold time                                 |                                                    | –55°C to 125°C | 2.2 V           | 10  |     |     | ns   |
|                                                                              |                                                    |                | 3 V             | 10  |     |     |      |
| t <sub>VALID,SO</sub> SOMI output data valid time                            | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF | –55°C to 125°C | 2.2 V           | 75  | 110 |     | ns   |
|                                                                              |                                                    |                | 3 V             | 50  | 75  |     |      |



**Figure 20. SPI Master Mode, CKPH = 0**



**Figure 21. SPI Master Mode, CKPH = 1**

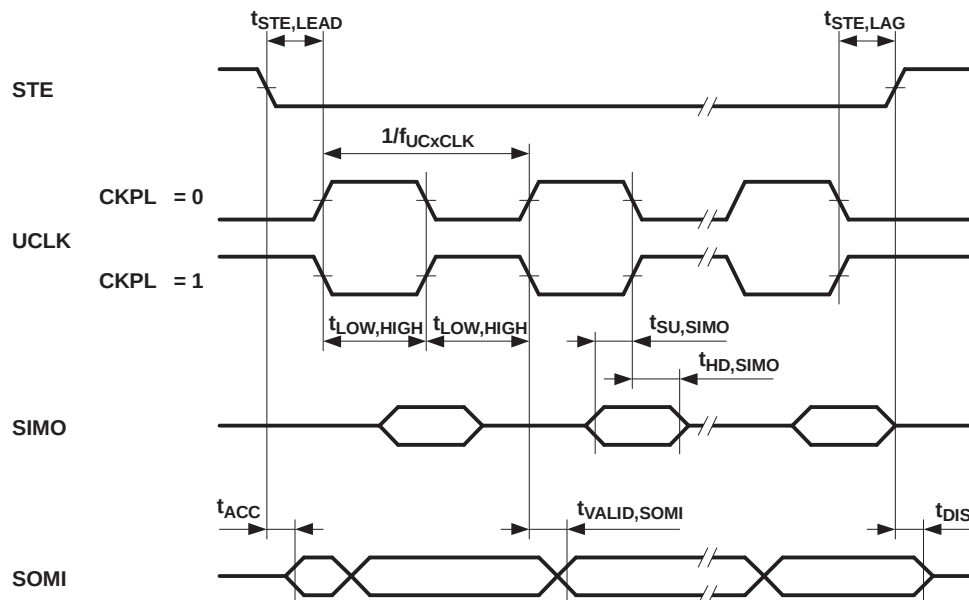


Figure 22. SPI Slave Mode, CKPH = 0

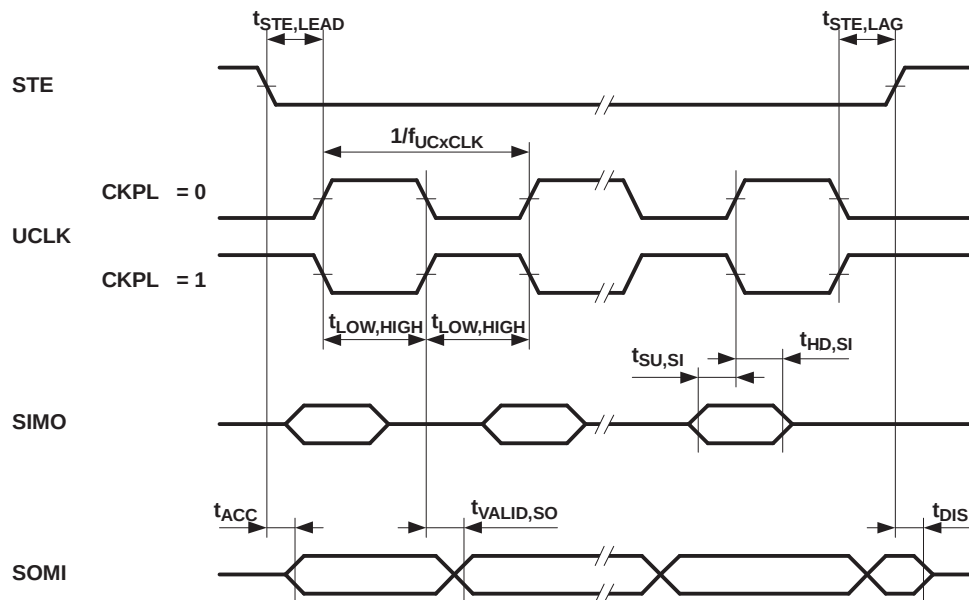
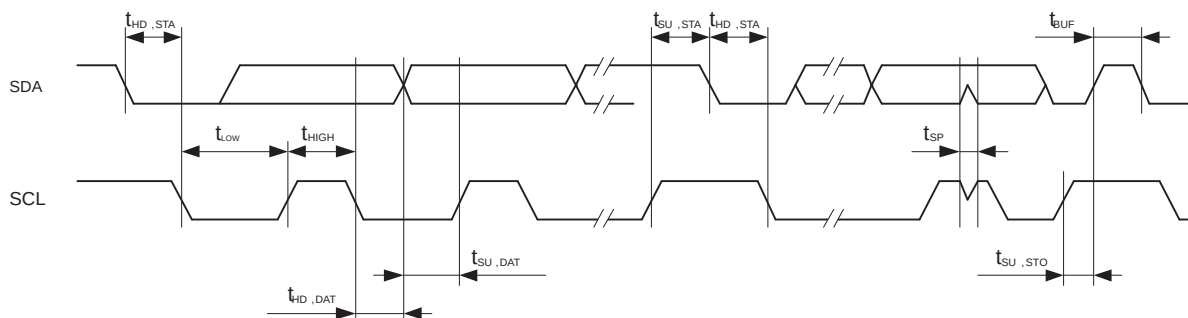


Figure 23. SPI Slave Mode, CKPH = 1

## USCI (I2C Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 24](#))

| PARAMETER                                                        | TEST CONDITIONS                                                     | T <sub>A</sub> | V <sub>CC</sub> | MIN                 | TYP | MAX | UNIT |
|------------------------------------------------------------------|---------------------------------------------------------------------|----------------|-----------------|---------------------|-----|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                     | Internal: SMCLK, ACLK,<br>External: UCLK,<br>Duty cycle = 50% ± 10% |                |                 | f <sub>SYSTEM</sub> |     |     | MHz  |
| f <sub>SCL</sub> SCL clock frequency                             |                                                                     | –55°C to 125°C | 2.2 V/3 V       | 0                   |     | 400 | kHz  |
| t <sub>HD,STA</sub> Hold time (repeated) START                   | f <sub>SCL</sub> ≤ 100 kHz                                          | –55°C to 125°C | 2.2 V/3 V       | 4.0                 |     |     | μs   |
|                                                                  | f <sub>SCL</sub> > 100 kHz                                          | –55°C to 125°C |                 | 0.6                 |     |     |      |
| t <sub>SU,STA</sub> Set-up time for a repeated START             | f <sub>SCL</sub> ≤ 100 kHz                                          | –55°C to 125°C | 2.2 V/3 V       | 4.7                 |     |     | μs   |
|                                                                  | f <sub>SCL</sub> > 100 kHz                                          | –55°C to 125°C |                 | 0.6                 |     |     |      |
| t <sub>HD,DAT</sub> Data hold time                               |                                                                     | –55°C to 125°C | 2.2 V/3 V       | 0                   |     |     | ns   |
| t <sub>SU,DAT</sub> Data set-up time                             |                                                                     | –55°C to 125°C | 2.2 V/3 V       | 250                 |     |     | ns   |
| t <sub>SU,STO</sub> Set-up time for STOP                         |                                                                     | –55°C to 125°C | 2.2 V/3 V       | 4.0                 |     |     | μs   |
| t <sub>SP</sub> Pulse width of spikes suppressed by input filter |                                                                     | –55°C to 125°C | 2.2 V           | 50                  | 150 | 600 | ns   |
|                                                                  |                                                                     |                | 3 V             | 50                  | 100 | 600 |      |



**Figure 24. I2C Mode Timing**

## 10-Bit ADC, Power-Supply and Input Range Conditions – Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                                                                       | TEST CONDITIONS                                                                                                 | T <sub>A</sub>  | V <sub>CC</sub> | MIN | TYP  | MAX             | UNIT |
|---------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|-----------------|-----------------|-----|------|-----------------|------|
| V <sub>CC</sub>     | Analog supply voltage range                                           | V <sub>SS</sub> = 0 V                                                                                           | –55°C to 125 °C |                 | 2.2 |      | 3.6             | V    |
| V <sub>AX</sub>     | Analog input voltage range <sup>(2)</sup>                             | All Ax terminals,<br>Analog inputs selected in<br>ADC10AE register                                              | –55°C to 125°C  |                 | 0   |      | V <sub>CC</sub> | V    |
| I <sub>ADC10</sub>  | ADC10 supply current <sup>(3)</sup>                                   | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 1, REFON = 0,<br>ADC10SHT0 = 1,<br>ADC10SHT1 = 0,<br>ADC10DIV = 0 | –55°C to 125°C  | 2.2 V           |     | 0.52 | 1.05            | mA   |
|                     |                                                                       |                                                                                                                 |                 | 3 V             |     | 0.6  | 1.2             |      |
| I <sub>REF+</sub>   | Reference supply current,<br>reference buffer disabled <sup>(4)</sup> | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REF2_5V = 0,<br>REFON = 1, REFOUT = 0                          | –55°C to 125°C  | 2.2 V/3 V       |     | 0.25 | .4              | mA   |
|                     |                                                                       | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REF2_5V = 1,<br>REFON = 1, REFOUT = 0                          | –55°C to 125°C  | 3 V             |     |      |                 |      |
| I <sub>REFB,0</sub> | Reference buffer supply current<br>with ADC10SR = 0 <sup>(4)</sup>    | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REFON = 1,<br>REF2_5V = 0, REFOUT = 1, ADC10SR = 0             | –55°C to 85°C   | 2.2 V/3 V       |     | 1.1  | 1.4             | mA   |
|                     |                                                                       |                                                                                                                 | 125°C           | 2.2 V/3 V       |     |      | 1.8             |      |
| I <sub>REFB,1</sub> | Reference buffer supply current<br>with ADC10SR = 1 <sup>(4)</sup>    | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REFON = 1,<br>REF2_5V = 0, REFOUT = 1,<br>ADC10SR = 1          | –55°C to 85°C   | 2.2 V/3 V       |     | 0.5  | .7              | mA   |
|                     |                                                                       |                                                                                                                 | 125°C           | 2.2 V/3 V       |     |      | .8              | mA   |
| C <sub>I</sub>      | Input capacitance                                                     | Only one terminal Ax selected at<br>a time                                                                      |                 |                 |     | 27   |                 | pF   |
| R <sub>I</sub>      | Input MUX ON resistance                                               | 0 V ≤ V <sub>AX</sub> ≤ V <sub>CC</sub>                                                                         |                 | 2.2 V/3 V       |     | 2000 |                 | Ω    |

(1) The leakage current is defined in the leakage current table with Px.x/Ax parameter.

(2) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R–</sub> for valid conversion results.

(3) The internal reference supply current is not included in current consumption parameter I<sub>ADC10</sub>.

(4) The internal reference current is supplied via terminal V<sub>CC</sub>. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

## 10-Bit ADC, Built-In Voltage Reference – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                       |                                                             | TEST CONDITIONS                                                                                                    |             | T <sub>A</sub> | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT   |
|-------------------------------------------------|-------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|-------------|----------------|-----------------|------|-----|------|--------|
| V <sub>CC,REF+</sub>                            | Positive built-in reference analog supply voltage range     | I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 0                                                                             |             | –55°C to 125°C |                 | 2.2  |     |      | V      |
|                                                 |                                                             | I <sub>VREF+</sub> ≤ 0.5 mA, REF2_5V = 1                                                                           |             | –55°C to 125°C |                 | 2.8  |     |      |        |
|                                                 |                                                             | I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 1                                                                             |             | –55°C to 125°C |                 | 2.9  |     |      |        |
| V <sub>REF+</sub>                               | Positive built-in reference voltage                         | I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> max, REF2_5V = 0                                                           |             | –55°C to 125°C | 2.2 V/3 V       | 1.41 | 1.5 | 1.59 | V      |
|                                                 |                                                             | I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> max, REF2_5V = 1                                                           |             | –55°C to 125°C | 3 V             | 2.35 | 2.5 | 2.65 |        |
| I <sub>LD,VREF+</sub>                           | Maximum V <sub>REF+</sub> load current                      |                                                                                                                    |             | –55°C to 125°C | 2.2 V           | ±0.5 |     |      | mA     |
|                                                 |                                                             |                                                                                                                    |             |                | 3 V             | ±1   |     |      |        |
| V <sub>REF+</sub> load regulation               |                                                             | I <sub>VREF+</sub> = 500 μA ± 100 μA, Analog input voltage V <sub>AX</sub> ≠ 0.75 V, REF2_5V = 0                   |             | –55°C to 125°C | 2.2 V/3 V       | ±2   |     |      | LSB    |
|                                                 |                                                             | I <sub>VREF+</sub> = 500 μA ± 100 μA, Analog input voltage V <sub>AX</sub> ≠ 1.25 V, REF2_5V = 1                   |             | –55°C to 125°C | 3 V             | ±2   |     |      |        |
| V <sub>REF+</sub> load regulation response time |                                                             | I <sub>VREF+</sub> = 100 μA→900 μA, V <sub>AX</sub> ≠ 0.5 × V <sub>REF+</sub> , Error of conversion result ≤ 1 LSB | ADC10SR = 0 | –55°C to 125°C | 3 V             | 400  |     |      | ns     |
|                                                 |                                                             |                                                                                                                    | ADC10SR = 1 | –55°C to 125°C |                 | 2000 |     |      |        |
| C <sub>VREF+</sub>                              | Maximum capacitance at pin V <sub>REF+</sub> <sup>(1)</sup> | I <sub>VREF+</sub> ≤ 1 mA, REFON = 1, REFOUT = 1                                                                   |             | –55°C to 125°C | 2.2 V/3 V       | 100  |     |      | pF     |
| TC <sub>REF+</sub>                              | Temperature coefficient                                     | I <sub>VREF+</sub> = const. with 0 mA ≤ I <sub>VREF+</sub> ≤ 1 mA                                                  |             | –55°C to 125°C | 2.2 V/3 V       | ±100 |     |      | ppm/°C |
| t <sub>REFON</sub>                              | Settling time of internal reference voltage <sup>(2)</sup>  | I <sub>VREF+</sub> = 0.5 mA, REF2_5V = 0<br>REFON = 0 → 1                                                          |             | –55°C to 125°C | 3.6 V           | 30   |     |      | μs     |
| t <sub>REFBURST</sub>                           | Settling time of reference buffer <sup>(2)</sup>            | I <sub>VREF+</sub> = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1                                                  | ADC10SR = 0 | –55°C to 125°C | 2.2 V           | 1    |     |      | μs     |
|                                                 |                                                             |                                                                                                                    | ADC10SR = 1 | –55°C to 125°C |                 | 2.5  |     |      |        |
|                                                 |                                                             | I <sub>VREF+</sub> = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1                                                  | ADC10SR = 0 | –55°C to 125°C | 3 V             | 2    |     |      |        |
|                                                 |                                                             |                                                                                                                    | ADC10SR = 1 | –55°C to 125°C |                 | 4.5  |     |      |        |

(1) The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA2/A4/V<sub>REF+</sub>/V<sub>eREF+</sub> (REFOUT = 1), must be limited; the reference buffer may become unstable otherwise.

(2) The condition is that the error in a conversion started after t<sub>REFON</sub> or t<sub>RefBuf</sub> is less than ±0.5 LSB.

## 10-Bit ADC, External Reference – Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                                                                                                                      | TEST CONDITIONS                                                                                            | T <sub>A</sub> | V <sub>CC</sub> | MIN | MAX             | UNIT |
|---------------------|----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|----------------|-----------------|-----|-----------------|------|
| V <sub>eREF+</sub>  | Positive external reference input voltage range <sup>(2)</sup>                                                       | V <sub>eREF+</sub> > V <sub>eREF−</sub> ,<br>SREF1 = 1, SREF0 = 0                                          | −55°C to 125°C |                 | 1.4 | V <sub>CC</sub> | V    |
|                     |                                                                                                                      | V <sub>eREF−</sub> ≤ V <sub>eREF+</sub> ≤ V <sub>CC</sub> − 0.15 V,<br>SREF1 = 1, SREF0 = 1 <sup>(3)</sup> | −55°C to 125°C |                 | 1.4 | 3.0             |      |
| V <sub>eREF−</sub>  | Negative external reference input voltage range <sup>(4)</sup>                                                       | V <sub>eREF+</sub> > V <sub>eREF−</sub>                                                                    | −55°C to 125°C |                 | 0   | 1.2             | V    |
| ΔV <sub>eREF</sub>  | Differential external reference input voltage range,<br>ΔV <sub>eREF</sub> = V <sub>eREF+</sub> − V <sub>eREF−</sub> | V <sub>eREF+</sub> > V <sub>eREF−</sub> <sup>(5)</sup>                                                     | −55°C to 125°C |                 | 1.4 | V <sub>CC</sub> | V    |
| I <sub>VeREF+</sub> | Static input current into V <sub>eREF+</sub>                                                                         | 0 V ≤ V <sub>eREF+</sub> ≤ V <sub>CC</sub> ,<br>SREF1 = 1, SREF0 = 0                                       | −55°C to 125°C | 2.2 V/3 V       |     | ±1              | μA   |
|                     |                                                                                                                      | 0 V ≤ V <sub>eREF+</sub> ≤ V <sub>CC</sub> − 0.15 V ≤ 3 V,<br>SREF1 = 1, SREF0 = 1 <sup>(3)</sup>          | −55°C to 125°C | 2.2 V/3 V       |     | 0               |      |
| I <sub>VeREF−</sub> | Static input current into V <sub>eREF−</sub>                                                                         | 0 V ≤ V <sub>eREF−</sub> ≤ V <sub>CC</sub>                                                                 | −55°C to 125°C | 2.2 V/3 V       |     | ±1              | μA   |

- (1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C<sub>i</sub>, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I<sub>REFB</sub>. The current consumption can be limited to the sample and conversion period with REBURST = 1.
- (4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

## 10-Bit ADC, Timing Parameters – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                 | TEST CONDITIONS                                                                          | T <sub>A</sub>                | V <sub>CC</sub> | MIN                                    | TYP  | MAX  | UNIT |
|-----------------------------------------------------------|------------------------------------------------------------------------------------------|-------------------------------|-----------------|----------------------------------------|------|------|------|
| f <sub>ADC10CLK</sub> ADC10 input clock frequency         | For specified performance of ADC10 linearity parameters                                  | ADC10SR=0                     | −55°C to 125°C  | 2.2 V/3 V                              | 0.45 | 6.5  | MHz  |
|                                                           |                                                                                          | ADC10SR=1                     | −55°C to 125°C  | 2.2 V/3 V                              | 0.45 | 1.5  |      |
| f <sub>ADC10OSC</sub> ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0, f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub>             | −55°C to 125°C                | 2.2 V/3 V       | 3.25                                   |      | 6.45 | MHz  |
| t <sub>CONVERT</sub> Conversion time                      | ADC10 built-in oscillator, ADC10SSELx = 0, f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub> | −55°C to 125°C                | 2.2 V/3 V       | 2.06                                   |      | 3.51 | μs   |
|                                                           | f <sub>ADC10CLK</sub> from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0                          | −55°C to 125°C                |                 | 13 = ADC10DIVx / f <sub>ADC10CLK</sub> |      |      |      |
| t <sub>ADC10ON</sub> Turn-on settling time of the ADC     |                                                                                          | <sup>(1)</sup> −55°C to 125°C |                 |                                        |      | 100  | ns   |

- (1) The condition is that the error in a conversion started after t<sub>ADC10ON</sub> is less than ±0.5 LSB. The reference and input signal are already settled.

## 10-Bit ADC, Linearity Parameters – Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER      |                              | TEST CONDITIONS                                                                      | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|----------------|------------------------------|--------------------------------------------------------------------------------------|----------------|-----------------|-----|------|-----|------|
| E <sub>I</sub> | Integral linearity error     |                                                                                      | –55°C to 125°C | 2.2 V/3 V       |     |      | ±1  | LSB  |
| E <sub>D</sub> | Differential linearity error |                                                                                      | –55°C to 125°C | 2.2 V/3 V       |     |      | ±1  | LSB  |
| E <sub>O</sub> | Offset error                 | Source impedance R <sub>S</sub> < 100 Ω                                              | –55°C to 125°C | 2.2 V/3 V       |     |      | ±1  | LSB  |
| E <sub>G</sub> | Gain error                   | SREFx = 010, un-buffered external reference, V <sub>eREF+</sub> = 1.5 V              | –55°C to 125°C | 2.2 V           |     | ±1.1 | ±2  | LSB  |
|                |                              | SREFx = 010; un-buffered external reference, V <sub>eREF+</sub> = 2.5 V              | –55°C to 125°C | 3 V             |     | ±1.1 | ±2  |      |
|                |                              | SREFx = 011, buffered external reference <sup>(2)</sup> , V <sub>eREF+</sub> = 1.5 V | –55°C to 125°C | 2.2 V           |     | ±1.1 | ±4  |      |
|                |                              | SREFx = 011, buffered external reference <sup>(2)</sup> , V <sub>eREF+</sub> = 2.5 V | –55°C to 125°C | 3 V             |     | ±1.1 | ±3  |      |
| E <sub>T</sub> | Total unadjusted error       | SREFx = 010, unbuffered external reference, V <sub>eREF+</sub> = 1.5 V               | –55°C to 125°C | 2.2 V           |     | ±2   | ±5  | LSB  |
|                |                              | SREFx = 010, unbuffered external reference, V <sub>eREF+</sub> = 2.5 V               | –55°C to 125°C | 3 V             |     | ±2   | ±5  |      |
|                |                              | SREFx = 011, buffered external reference <sup>(2)</sup> , V <sub>eREF+</sub> = 1.5 V | –55°C to 125°C | 2.2 V           |     | ±2   | ±7  |      |
|                |                              | SREFx = 011, buffered external reference <sup>(2)</sup> , V <sub>eREF+</sub> = 2.5 V | –55°C to 125°C | 3 V             |     | ±2   | ±6  |      |

(1) 2.2V Not Production Tested.

(2) The reference buffer's offset adds to the gain and total unadjusted error.

## 10-Bit ADC, Temperature Sensor and Built-In V<sub>MID</sub> – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   |                                                               | TEST CONDITIONS                                                       | T <sub>A</sub> | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT  |
|-----------------------------|---------------------------------------------------------------|-----------------------------------------------------------------------|----------------|-----------------|------|------|------|-------|
| I <sub>SENSOR</sub>         | Temperature sensor supply current <sup>(1)</sup>              | REFON = 0, INCHx = 0Ah, T <sub>A</sub> = 25°C                         | –55°C to 125°C | 2.2 V           |      | 40   | 120  | μA    |
|                             |                                                               |                                                                       |                | 3 V             |      | 60   | 160  |       |
| TC <sub>SENSOR</sub>        |                                                               | ADC10ON = 1, INCHx = 0Ah <sup>(2)</sup>                               | –55°C to 125°C | 2.2 V/3 V       | 3.44 | 3.55 | 3.66 | mV/°C |
| V <sub>Offset,Sensor</sub>  | Sensor offset voltage                                         | ADC10ON = 1, INCHx = 0Ah <sup>(2)</sup>                               | –55°C to 125°C |                 | -100 |      | 100  | mV    |
| V <sub>SENSOR</sub>         | Sensor output voltage <sup>(3)</sup>                          | Temperature sensor voltage at T <sub>A</sub> = 125°C (T version only) | –55°C to 125°C | 2.2 V/3 V       | 1265 | 1365 | 1465 | mV    |
|                             |                                                               | Temperature sensor voltage at T <sub>A</sub> = 85°C                   | –55°C to 125°C |                 | 1195 | 1295 | 1395 |       |
|                             |                                                               | Temperature sensor voltage at T <sub>A</sub> = 25°C                   | –55°C to 125°C |                 | 985  | 1085 | 1185 |       |
|                             |                                                               | Temperature sensor voltage at T <sub>A</sub> = 0°C                    | –55°C to 125°C |                 | 895  | 995  | 1095 |       |
| t <sub>Sensor(sample)</sub> | Sample time required if channel 10 is selected <sup>(4)</sup> | ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB          | –55°C to 125°C | 2.2 V/3 V       | 30   |      |      | μs    |
| I <sub>VMID</sub>           | Current into divider at channel 11 <sup>(5)</sup>             | ADC10ON = 1, INCHx = 0Bh                                              | –55°C to 125°C | 2.2 V           |      |      | NA   | μA    |
|                             |                                                               |                                                                       |                | 3 V             |      |      | NA   |       |
| V <sub>MID</sub>            | V <sub>CC</sub> divider at channel 11                         | ADC10ON = 1, INCHx = 0Bh, V <sub>MID</sub> is ≠ 0.5 × V <sub>CC</sub> | –55°C to 125°C | 2.2 V           | 1.06 | 1.1  | 1.14 | V     |
|                             |                                                               |                                                                       |                | 3 V             | 1.46 | 1.5  | 1.54 |       |
| t <sub>VMID(sample)</sub>   | Sample time required if channel 11 is selected <sup>(6)</sup> | ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB          | –55°C to 125°C | 2.2 V           | 1400 |      |      | ns    |
|                             |                                                               |                                                                       |                | 3 V             | 1220 |      |      |       |

- (1) The sensor current I<sub>SENSOR</sub> is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I<sub>SENSOR</sub> is included in I<sub>REF+</sub>. When REFON = 0, I<sub>SENSOR</sub> applies during conversion of the temperature sensor input (INCH = 0Ah).
- (2) The following formula can be used to calculate the temperature sensor output voltage:  

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}]$$
or  

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} T [^{\circ}\text{C}] + V_{\text{Sensor}}(T_A = 0^{\circ}\text{C}) [\text{mV}]$$
- (3) Results based on characterization and/or production test, not TC<sub>Sensor</sub> or V<sub>Offset,sensor</sub>.
- (4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t<sub>SENSOR(on)</sub>.
- (5) No additional current is needed. The V<sub>MID</sub> is used during sampling.
- (6) The on-time t<sub>VMID(on)</sub> is included in the sampling time t<sub>VMID(sample)</sub>; no additional on time is needed.

## Operational Amplifier (OA) Supply Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER       |                               | TEST CONDITIONS | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------|-------------------------------|-----------------|----------------|-----------------|-----|-----|-----|------|
| V <sub>CC</sub> | Supply voltage range          |                 | –55°C to 125°C |                 | 2.2 |     | 3.6 | V    |
| I <sub>CC</sub> | Supply current <sup>(1)</sup> | Fast Mode       | –55°C to 125°C | 2.2 V/3 V       |     | 180 | 290 | μA   |
|                 |                               | Medium Mode     | –55°C to 125°C |                 |     | 110 | 190 |      |
|                 |                               | Slow Mode       | –55°C to 125°C |                 |     | 50  | 80  |      |
| PSSR            | Power-supply rejection ratio  | Noninverting    |                | 2.2 V/3 V       |     | 70  |     | dB   |

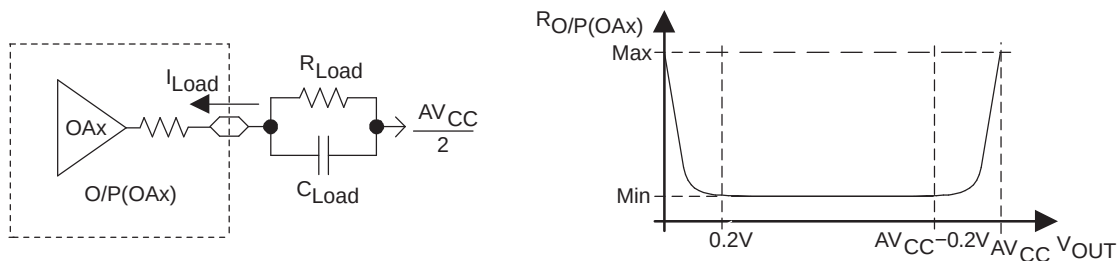
- (1) Corresponding pins configured as OA inputs and outputs, respectively.

## Operational Amplifier (OA) Input/Output Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                                                   | TEST CONDITIONS                                                                                              |                              | T <sub>A</sub> | V <sub>CC</sub> | MIN                   | TYP  | MAX                   | UNIT   |
|-----------------------|-------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|------------------------------|----------------|-----------------|-----------------------|------|-----------------------|--------|
| V <sub>I/P</sub>      | Input voltage range                                               |                                                                                                              |                              | –55°C to 125°C |                 | –0.1                  |      | V <sub>CC</sub> – 1.2 | V      |
| I <sub>lkg</sub>      | Input leakage current <sup>(1) (2)</sup>                          |                                                                                                              |                              | –55°C to 55°C  | 2.2 V/3 V       | –15                   | ±0.5 | 15                    | nA     |
|                       |                                                                   |                                                                                                              |                              | 55°C to 85°C   |                 | –20                   | ±5   | 20                    |        |
|                       |                                                                   |                                                                                                              |                              | 85°C to 125°C  |                 | –100                  |      | 100                   |        |
| V <sub>n</sub>        | Voltage noise density, I/P                                        | Fast Mode                                                                                                    | f <sub>V(I/P)</sub> = 1 kHz  |                |                 | 50                    |      |                       | nV/√Hz |
|                       |                                                                   | Medium Mode                                                                                                  |                              |                |                 | 80                    |      |                       |        |
|                       |                                                                   | Slow Mode                                                                                                    |                              |                |                 | 140                   |      |                       |        |
|                       |                                                                   | Fast Mode                                                                                                    | f <sub>V(I/P)</sub> = 10 kHz |                |                 | 30                    |      |                       |        |
|                       |                                                                   | Medium Mode                                                                                                  |                              |                |                 | 50                    |      |                       |        |
|                       |                                                                   | Slow Mode                                                                                                    |                              |                |                 | 65                    |      |                       |        |
| V <sub>IO</sub>       | Offset voltage, I/P                                               |                                                                                                              |                              | –55°C to 125°C | 2.2 V/3 V       | ±10                   |      |                       | mV     |
|                       | Offset temperature drift, I/P                                     | See <sup>(3)</sup>                                                                                           |                              |                | 2.2 V/3 V       | ±10                   |      |                       | μV/°C  |
|                       | Offset voltage drift with supply, I/P                             | 0.3 V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> – 1.0 V<br>ΔV <sub>CC</sub> ≤ ±10%, T <sub>A</sub> = 25°C          |                              | –55°C to 125°C | 2.2 V/3 V       | ±1.5                  |      |                       | mV/V   |
| V <sub>OH</sub>       | High-level output voltage, O/P                                    | Fast Mode, I <sub>SOURCE</sub> ≤ –500 μA                                                                     |                              | –55°C to 125°C | 2.2 V/3 V       | V <sub>CC</sub> – 0.2 |      |                       | V      |
|                       |                                                                   | Slow Mode, I <sub>SOURCE</sub> ≤ –150 μA                                                                     |                              | –55°C to 125°C |                 | V <sub>CC</sub> – 0.1 |      |                       |        |
| V <sub>OL</sub>       | Low-level output voltage, O/P                                     | Fast Mode, I <sub>SOURCE</sub> ≤ 500 μA                                                                      |                              | –55°C to 125°C | 2.2 V/3 V       | V <sub>SS</sub>       |      |                       | V      |
|                       |                                                                   | Slow Mode, I <sub>SOURCE</sub> ≤ 150 μA                                                                      |                              | –55°C to 125°C |                 | V <sub>SS</sub>       |      |                       |        |
| R <sub>O/P(OAx)</sub> | Output resistance <sup>(4)</sup> (see <a href="#">Figure 25</a> ) | R <sub>Load</sub> = 3 kΩ, C <sub>Load</sub> = 50 pF, V <sub>O/P(OAx)</sub> < 0.2 V                           |                              |                | 2.2 V/3 V       | 150                   |      |                       | Ω      |
|                       |                                                                   | R <sub>Load</sub> = 3 kΩ, C <sub>Load</sub> = 50 pF, V <sub>O/P(OAx)</sub> > V <sub>CC</sub> – 1.2 V         |                              |                |                 | 150                   |      |                       |        |
|                       |                                                                   | R <sub>Load</sub> = 3 kΩ, C <sub>Load</sub> = 50 pF, 0.2 V ≤ V <sub>O/P(OAx)</sub> ≤ V <sub>CC</sub> – 0.2 V |                              |                |                 | 0.1                   |      |                       |        |
| CMRR                  | Common-mode rejection ratio                                       | Noninverting                                                                                                 |                              |                | 2.2 V/3 V       | 70                    |      |                       | dB     |

- (1) ESD damage can degrade input current leakage.
- (2) The input bias current is overridden by the input leakage current.
- (3) Calculated using the box method
- (4) Specification valid for voltage-follower OAx configuration



**Figure 25. OAx Output Resistance Tests**

## Operational Amplifier (OA) Dynamic Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                         | TEST CONDITIONS                                                               | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|----------------------|---------------------------------------------------------|-------------------------------------------------------------------------------|----------------|-----------------|-----|-----|-----|------|
| SR                   | Slew rate                                               | Fast Mode                                                                     |                |                 |     | 1.2 |     | V/μs |
|                      |                                                         | Medium Mode                                                                   |                |                 |     | 0.8 |     |      |
|                      |                                                         | Slow Mode                                                                     |                |                 |     | 0.3 |     |      |
|                      | Open-loop voltage gain                                  |                                                                               |                |                 |     | 100 |     | dB   |
| φ <sub>m</sub>       | Phase margin                                            | C <sub>L</sub> = 50 pF                                                        |                |                 |     | 60  |     | deg  |
|                      | Gain margin                                             | C <sub>L</sub> = 50 pF                                                        |                |                 |     | 20  |     | dB   |
| GBW                  | Gain-bandwidth product<br>(see Figure 26 and Figure 27) | Noninverting, Fast Mode,<br>R <sub>L</sub> = 47 kΩ, C <sub>L</sub> = 50 pF    |                | 2.2 V/3 V       |     | 2.2 |     | MHz  |
|                      |                                                         | Noninverting, Medium Mode,<br>R <sub>L</sub> = 300 kΩ, C <sub>L</sub> = 50 pF |                |                 |     | 1.4 |     |      |
|                      |                                                         | Noninverting, Slow Mode,<br>R <sub>L</sub> = 300 kΩ, C <sub>L</sub> = 50 pF   |                |                 |     | 0.5 |     |      |
| t <sub>en(on)</sub>  | Enable time on                                          | t <sub>on</sub> , noninverting, Gain = 1                                      | –55°C to 125°C | 2.2 V/3 V       |     | 10  | 20  | μs   |
| t <sub>en(off)</sub> | Enable time off                                         |                                                                               | –55°C to 125°C | 2.2 V/3 V       |     |     | 1   | μs   |

TYPICAL OPEN-LOOP GAIN vs FREQUENCY

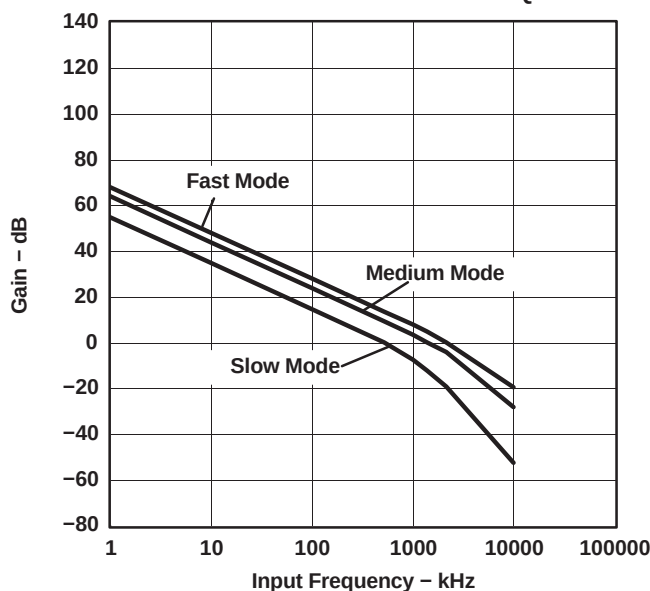


Figure 26.

TYPICAL PHASE vs FREQUENCY

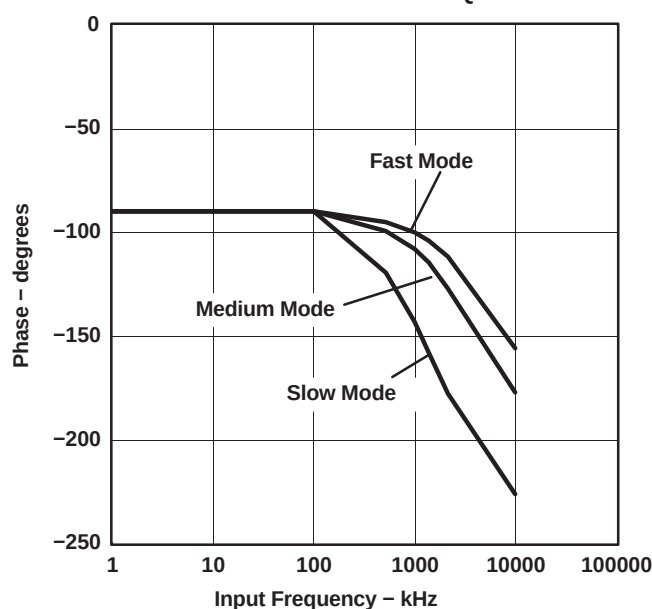


Figure 27.

## Operational Amplifier OA Feedback Network, Resistor Network – Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER          |                                                 | TEST CONDITIONS | T <sub>A</sub> | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------------------------|-----------------|----------------|-----|-----|-----|------|
| R <sub>total</sub> | Total resistance of resistor string             |                 |                |     | 96  |     | kΩ   |
| R <sub>unit</sub>  | Unit resistor of resistor string <sup>(2)</sup> |                 |                |     | 6   |     | kΩ   |

(1) A single resistor string is composed of 4 R<sub>unit</sub> + 4 R<sub>unit</sub> + 2 R<sub>unit</sub> + 2 R<sub>unit</sub> + 1 R<sub>unit</sub> + 1 R<sub>unit</sub> + 1 R<sub>unit</sub> + 1 R<sub>unit</sub> = 16 R<sub>unit</sub> = R<sub>total</sub>.

(2) For the matching (i.e., the relative accuracy) of the unit resistors on a device, refer to the gain and level specifications of the respective configurations.

## Operational Amplifier (OA) Feedback Network, Comparator Mode (OAFc<sub>x</sub> = 3) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                        | TEST CONDITIONS                    | T <sub>A</sub> | V <sub>CC</sub> | MIN                | TYP  | MAX   | UNIT            |
|----------------------------------------------------------------------------------|------------------------------------|----------------|-----------------|--------------------|------|-------|-----------------|
| V <sub>Level</sub> Comparator level                                              | OAFBR <sub>x</sub> = 1, OARRIP = 0 | –55°C to 125°C | 2.2 V/3 V       | 0.242              | 1/4  | 0.262 | V <sub>CC</sub> |
|                                                                                  | OAFBR <sub>x</sub> = 2, OARRIP = 0 | –55°C to 125°C |                 | 0.492              | ½    | 0.512 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 3, OARRIP = 0 | –55°C to 125°C |                 | 0.619              | 5/8  | 0.639 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 4, OARRIP = 0 |                |                 | N/A <sup>(1)</sup> |      |       |                 |
|                                                                                  | OAFBR <sub>x</sub> = 5, OARRIP = 0 |                |                 | N/A <sup>(1)</sup> |      |       |                 |
|                                                                                  | OAFBR <sub>x</sub> = 6, OARRIP = 0 |                |                 | N/A <sup>(1)</sup> |      |       |                 |
|                                                                                  | OAFBR <sub>x</sub> = 7, OARRIP = 0 |                |                 | N/A <sup>(1)</sup> |      |       |                 |
|                                                                                  | OAFBR <sub>x</sub> = 1, OARRIP = 1 | –55°C to 125°C |                 | 0.057              | 1/16 | 0.071 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 2, OARRIP = 1 | –55°C to 125°C |                 | 0.122              | 1/8  | 0.128 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 3, OARRIP = 1 | –55°C to 125°C |                 | 0.182              | 3/16 | 0.197 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 4, OARRIP = 1 | –55°C to 125°C |                 | 0.242              | 1/4  | 0.262 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 5, OARRIP = 1 | –55°C to 125°C |                 | 0.367              | 3/8  | 0.383 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 6, OARRIP = 1 | –55°C to 125°C |                 | 0.492              | ½    | 0.512 |                 |
|                                                                                  | OAFBR <sub>x</sub> = 7, OARRIP = 1 |                |                 | N/A <sup>(1)</sup> |      |       |                 |
| t <sub>PLH</sub> , t <sub>PHL</sub> Propagation delay<br>(low-high and high-low) | Fast Mode, Overdrive 10 mV         |                | 2.2 V/3 V       |                    | 40   |       | µs              |
|                                                                                  | Fast Mode, Overdrive 100 mV        |                |                 |                    | 4    |       |                 |
|                                                                                  | Fast Mode, Overdrive 500 mV        |                |                 |                    | 3    |       |                 |
|                                                                                  | Medium Mode, Overdrive 10 mV       |                |                 |                    | 60   |       |                 |
|                                                                                  | Medium Mode, Overdrive 100 mV      |                |                 |                    | 6    |       |                 |
|                                                                                  | Medium Mode, Overdrive 500 mV      |                |                 |                    | 5    |       |                 |
|                                                                                  | Slow Mode, Overdrive 10 mV         |                |                 |                    | 160  |       |                 |
|                                                                                  | Slow Mode, Overdrive 100 mV        |                |                 |                    | 20   |       |                 |
|                                                                                  | Slow Mode, Overdrive 500 mV        |                |                 |                    | 15   |       |                 |

(1) The level is not available due to the analog input voltage range of the operational amplifier.

## Operational Amplifier (OA) Feedback Network, Noninverting Amplifier Mode (OAFc<sub>x</sub> = 4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                        | TEST CONDITIONS        | T <sub>A</sub> | V <sub>CC</sub> | MIN   | TYP   | MAX   | UNIT |
|--------------------------------------------------|------------------------|----------------|-----------------|-------|-------|-------|------|
| G      Gain                                      | OAFBR <sub>x</sub> = 0 | –55°C to 125°C | 2.2 V/3 V       | 0.970 | 1.00  | 1.035 |      |
|                                                  | OAFBR <sub>x</sub> = 1 | –55°C to 125°C |                 | 1.325 | 1.334 | 1.345 |      |
|                                                  | OAFBR <sub>x</sub> = 2 | –55°C to 125°C |                 | 1.985 | 2.001 | 2.017 |      |
|                                                  | OAFBR <sub>x</sub> = 3 | –55°C to 125°C |                 | 2.638 | 2.667 | 2.696 |      |
|                                                  | OAFBR <sub>x</sub> = 4 | –55°C to 125°C |                 | 3.94  | 4.00  | 4.06  |      |
|                                                  | OAFBR <sub>x</sub> = 5 | –55°C to 125°C |                 | 5.22  | 5.33  | 5.44  |      |
|                                                  | OAFBR <sub>x</sub> = 6 | –55°C to 125°C |                 | 7.76  | 7.97  | 8.18  |      |
|                                                  | OAFBR <sub>x</sub> = 7 | –55°C to 125°C |                 | 15.0  | 15.8  | 16.7  |      |
| THD      Total harmonic distortion/nonlinearity  | All gains              |                | 2.2 V           |       | –60   |       | dB   |
|                                                  |                        |                | 3 V             |       | –70   |       |      |
| t <sub>Settle</sub> Settling time <sup>(1)</sup> | All power modes        | –55°C to 125°C | 2.2 V/3 V       |       | 7     | 12    | µs   |

(1) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

## Operational Amplifier (OA) Feedback Network, Inverting Amplifier Mode (OAFcx = 6) – Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| For recommended ranges of supply voltage and operating free air temperature (unless otherwise noted) |                                        |                 |                |                 |        |        |        |      |
|------------------------------------------------------------------------------------------------------|----------------------------------------|-----------------|----------------|-----------------|--------|--------|--------|------|
| PARAMETER                                                                                            |                                        | TEST CONDITIONS | T <sub>A</sub> | V <sub>CC</sub> | MIN    | TYP    | MAX    | UNIT |
| G                                                                                                    | Gain                                   | OAFBRx = 1      | –55°C to 125°C | 2.2 V/3 V       | –0.385 | –0.335 | –0.305 |      |
|                                                                                                      |                                        | OAFBRx = 2      | –55°C to 125°C |                 | –1.023 | –1.002 | –0.979 |      |
|                                                                                                      |                                        | OAFBRx = 3      | –55°C to 125°C |                 | –1.712 | –1.668 | –1.624 |      |
|                                                                                                      |                                        | OAFBRx = 4      | –55°C to 125°C |                 | –3.10  | –3.00  | –2.90  |      |
|                                                                                                      |                                        | OAFBRx = 5      | –55°C to 125°C |                 | –4.51  | –4.33  | –4.15  |      |
|                                                                                                      |                                        | OAFBRx = 6      | –55°C to 125°C |                 | –7.37  | –6.97  | –6.57  |      |
|                                                                                                      |                                        | OAFBRx = 7      | –55°C to 125°C |                 | –16.6  | –14.8  | –13.1  |      |
| THD                                                                                                  | Total harmonic distortion/nonlinearity | All gains       |                | 2.2 V           | –60    |        |        | dB   |
|                                                                                                      |                                        |                 |                | 3 V             | –70    |        |        |      |
| t <sub>settle</sub>                                                                                  | Settling time <sup>(2)</sup>           | All power modes | –55°C to 125°C | 2.2 V/3 V       | 7 12   |        |        | μs   |

(1) This includes the 2 OA configuration "inverting amplifier with input buffer". Both OA needs to be set to the same power mode OAPMx.

(2) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

## Flash Memory – Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                    | TEST CONDITIONS       | T <sub>A</sub> | V <sub>CC</sub> | MIN             | TYP             | MAX  | UNIT             |
|------------------------------------------------------------------------------|-----------------------|----------------|-----------------|-----------------|-----------------|------|------------------|
| V <sub>CC(PGM/ERASE)</sub> Program and erase supply voltage                  |                       | –55°C to 125°C |                 | 2.2             |                 | 3.6  | V                |
| f <sub>FTG</sub> Flash timing generator frequency                            |                       | –55°C to 125°C |                 | 257             |                 | 476  | kHz              |
| I <sub>PGM</sub> Supply current from V <sub>CC</sub> during program          |                       | –55°C to 125°C | 2.2 V/3.6 V     |                 | 1               | 5    | mA               |
| I <sub>ERASE</sub> Supply current from V <sub>CC</sub> during erase          |                       | –55°C to 125°C | 2.2 V/3.6 V     |                 | 1               | 10.5 | mA               |
| t <sub>CPT</sub> Cumulative program time <sup>(2)</sup>                      |                       | –55°C to 125°C | 2.2 V/3.6 V     |                 |                 | 10   | ms               |
| t <sub>CMErase</sub> Cumulative mass erase time                              |                       | –55°C to 125°C | 2.2 V/3.6 V     | 20              |                 |      | ms               |
| Program/Erase endurance                                                      |                       | –55°C to 125°C |                 | 10 <sup>4</sup> | 10 <sup>5</sup> |      | cycles           |
| t <sub>Retention</sub> Data retention duration <sup>(3)</sup>                | T <sub>J</sub> = 25°C |                |                 | 100             |                 |      | years            |
| t <sub>Word</sub> Word or byte program time                                  | (4)                   |                |                 |                 | 30              |      | t <sub>FTG</sub> |
| t <sub>Block, 0</sub> Block program time for 1 <sup>st</sup> byte or word    | (4)                   |                |                 |                 | 25              |      | t <sub>FTG</sub> |
| t <sub>Block, 1-63</sub> Block program time for each additional byte or word | (4)                   |                |                 |                 | 18              |      | t <sub>FTG</sub> |
| t <sub>Block, End</sub> Block program end-sequence wait time                 | (4)                   |                |                 |                 | 6               |      | t <sub>FTG</sub> |
| t <sub>Mass Erase</sub> Mass erase time                                      | (4)                   |                |                 |                 | 1059<br>3       |      | t <sub>FTG</sub> |
| t <sub>Seg Erase</sub> Segment erase time                                    | (4)                   |                |                 |                 | 4819            |      | t <sub>FTG</sub> |

(1) Additional Flash retention documentation located in application report (SLAA392).

(2) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.

(3) To test the flash data retention at various temperatures we make use of accelerated tests on the flash with **500-Hours Baking Time at 250°C**. These tests are wholly based on Arrhenius law and equation.

(4) These values are hardwired into the Flash Controller's state machine (t<sub>FTG</sub> = 1/f<sub>FTG</sub>).

## RAM – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                       | TEST CONDITIONS | T <sub>A</sub> | MIN | MAX | UNIT |
|-----------------------------------------------------------------|-----------------|----------------|-----|-----|------|
| V <sub>(RAMh)</sub> RAM retention supply voltage <sup>(1)</sup> | CPU halted      | –55°C to 125°C | 1.6 |     | V    |

(1) This parameter defines the minimum supply voltage V<sub>CC</sub> when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

## JTAG and Spy-Bi-Wire Interface – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                                 | TEST CONDITIONS | T <sub>A</sub> | V <sub>CC</sub> | MIN       | TYP | MAX | UNIT |
|-----------------------------------------------------------------------------------------------------------|-----------------|----------------|-----------------|-----------|-----|-----|------|
| f <sub>SBW</sub> Spy-Bi-Wire input frequency                                                              |                 | –55°C to 125°C | 2.2 V/3 V       | 0         |     | 20  | MHz  |
| t <sub>SBW,Low</sub> Spy-Bi-Wire low clock pulse length                                                   |                 | –55°C to 125°C | 2.2 V/3 V       | 0.02<br>5 |     | 15  | µs   |
| t <sub>SBW,En</sub> Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge <sup>(1)</sup> ) |                 | –55°C to 125°C | 2.2 V/3 V       |           |     | 1   | µs   |
| t <sub>SBW,Ret</sub> Spy-Bi-Wire return to normal operation time                                          |                 | –55°C to 125°C | 2.2 V/3 V       | 15        |     | 100 | µs   |
| f <sub>TCK</sub> TCK input frequency <sup>(2)</sup>                                                       |                 | –55°C to 125°C | 2.2 V           | 0         |     | 5   | MHz  |
|                                                                                                           |                 |                | 3 V             | 0         |     | 10  | MHz  |
| R <sub>Internal</sub> Internal pulldown resistance on TEST                                                |                 | –55°C to 125°C | 2.2 V/3 V       | 25        | 60  | 90  | kΩ   |

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum t<sub>SBW,En</sub> time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.

(2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.

## JTAG Fuse<sup>(1)</sup> – Electrical Characteristics

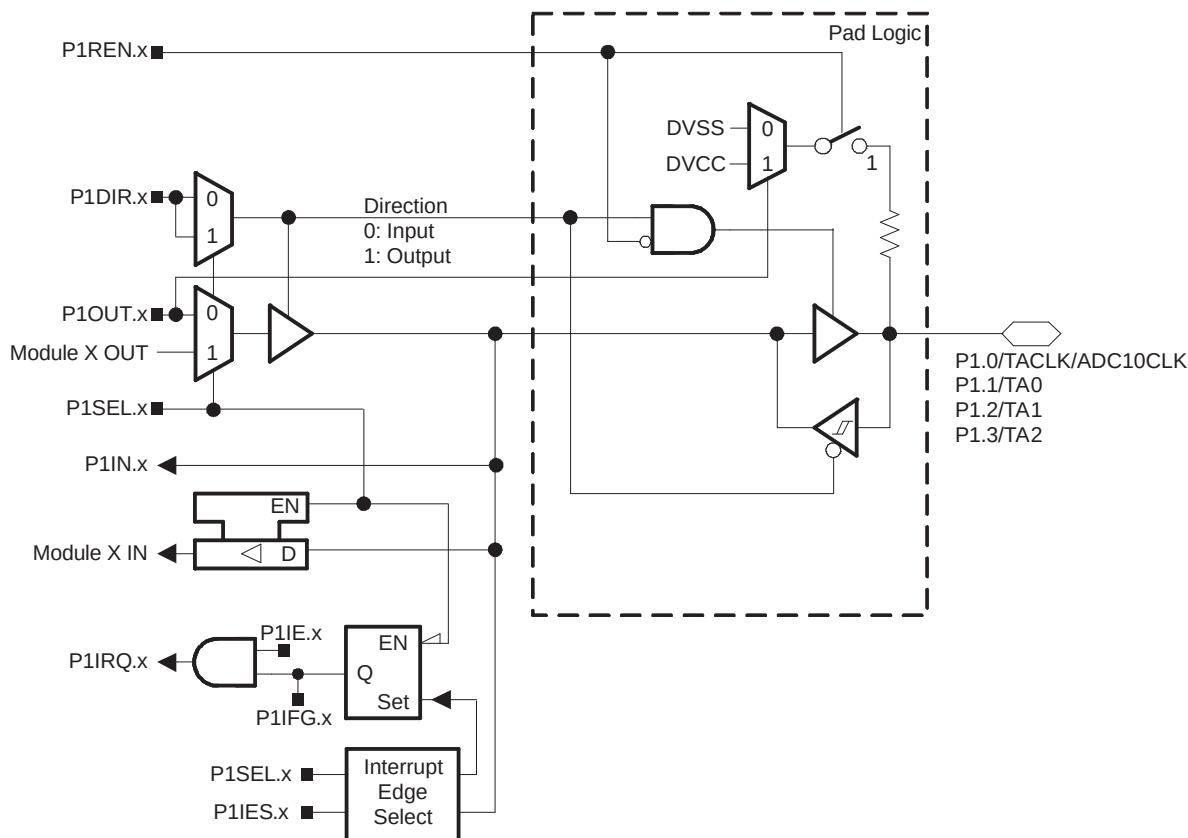
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                     | TEST CONDITIONS | T <sub>A</sub>        | MIN | MAX | UNIT |
|---------------------------------------------------------------|-----------------|-----------------------|-----|-----|------|
| V <sub>CC(FB)</sub> Supply voltage during fuse-blow condition |                 | T <sub>A</sub> = 25°C | 2.5 |     | V    |
| V <sub>FB</sub> Voltage level on TEST for fuse blow           |                 | –55°C to 125°C        | 6   | 7   | V    |
| I <sub>FB</sub> Supply current into TEST during fuse blow     |                 | –55°C to 125°C        |     | 100 | mA   |
| t <sub>FB</sub> Time to blow fuse                             |                 | –55°C to 125°C        |     | 1   | ms   |

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

## APPLICATION INFORMATION

### Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger



### Port P1 (P1.0 to P1.3) Pin Functions

| PIN NAME (P1.X)     | X | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |
|---------------------|---|---------------------------|-------------------------------------|---------|
|                     |   |                           | P1DIR.x                             | P1SEL.x |
| P1.0/TACLK/ADC10CLK | 0 | P1.0 <sup>(3)</sup>       | I: 0; O: 1                          | 0       |
|                     |   | Timer_A3.TACLK            | 0                                   | 1       |
|                     |   | ADC10CLK                  | 1                                   | 1       |
| P1.1/TA0            | 1 | P1.1 <sup>(4)</sup> (I/O) | I: 0; O: 1                          | 0       |
|                     |   | Timer_A3.CCI0A            | 0                                   | 1       |
|                     |   | Timer_A3.TA0              | 1                                   | 1       |
| P1.2/TA1            | 2 | P1.2 <sup>(4)</sup> (I/O) | I: 0; O: 1                          | 0       |
|                     |   | Timer_A3.CCI0A            | 0                                   | 1       |
|                     |   | Timer_A3.TA0              | 1                                   | 1       |
| P1.3/TA2            | 3 | P1.3 <sup>(4)</sup> I/O   | I: 0; O: 1                          | 0       |
|                     |   | Timer_A3.CCI0A            | 0                                   | 1       |
|                     |   | Timer_A3.TA0              | 1                                   | 1       |

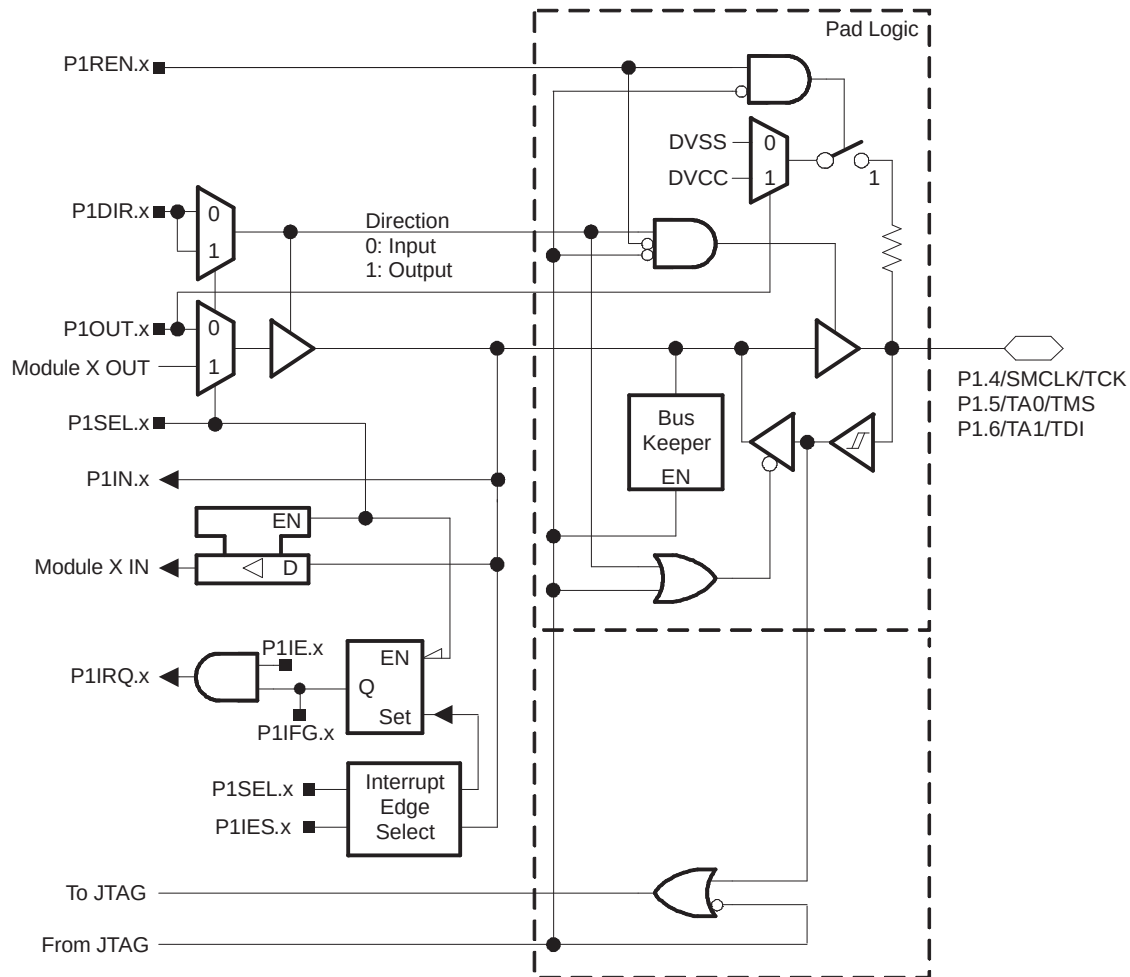
(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Default after reset (PUC/POR)

## Port P1 Pin Schematic: P1.4 to P1.6, Input/Output With Schmitt Trigger and In-System Access Features



## Port P1 (P1.4 to P1.6) Pin Functions

| PIN NAME (P1.X)   | X | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |             |
|-------------------|---|---------------------------|-------------------------------------|---------|-------------|
|                   |   |                           | P1DIR.x                             | P1SEL.x | 4-Wire JTAG |
| P1.4/SMCLK/TCK    | 4 | P1.4 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0           |
|                   |   | SMCLK                     | 1                                   | 1       | 0           |
|                   |   | TCK                       | X                                   | X       | 1           |
| P1.5/TA0/TMS      | 5 | P1.5 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0           |
|                   |   | Timer_A3.TA0              | 1                                   | 1       | 0           |
|                   |   | TMS                       | X                                   | X       | 1           |
| P1.6/TA1/TDI/TCLK | 6 | P1.6 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0           |
|                   |   | Timer_A3.TA1              | 1                                   | 1       | 0           |
|                   |   | TDI/TCLK <sup>(4)</sup>   | X                                   | X       | 1           |

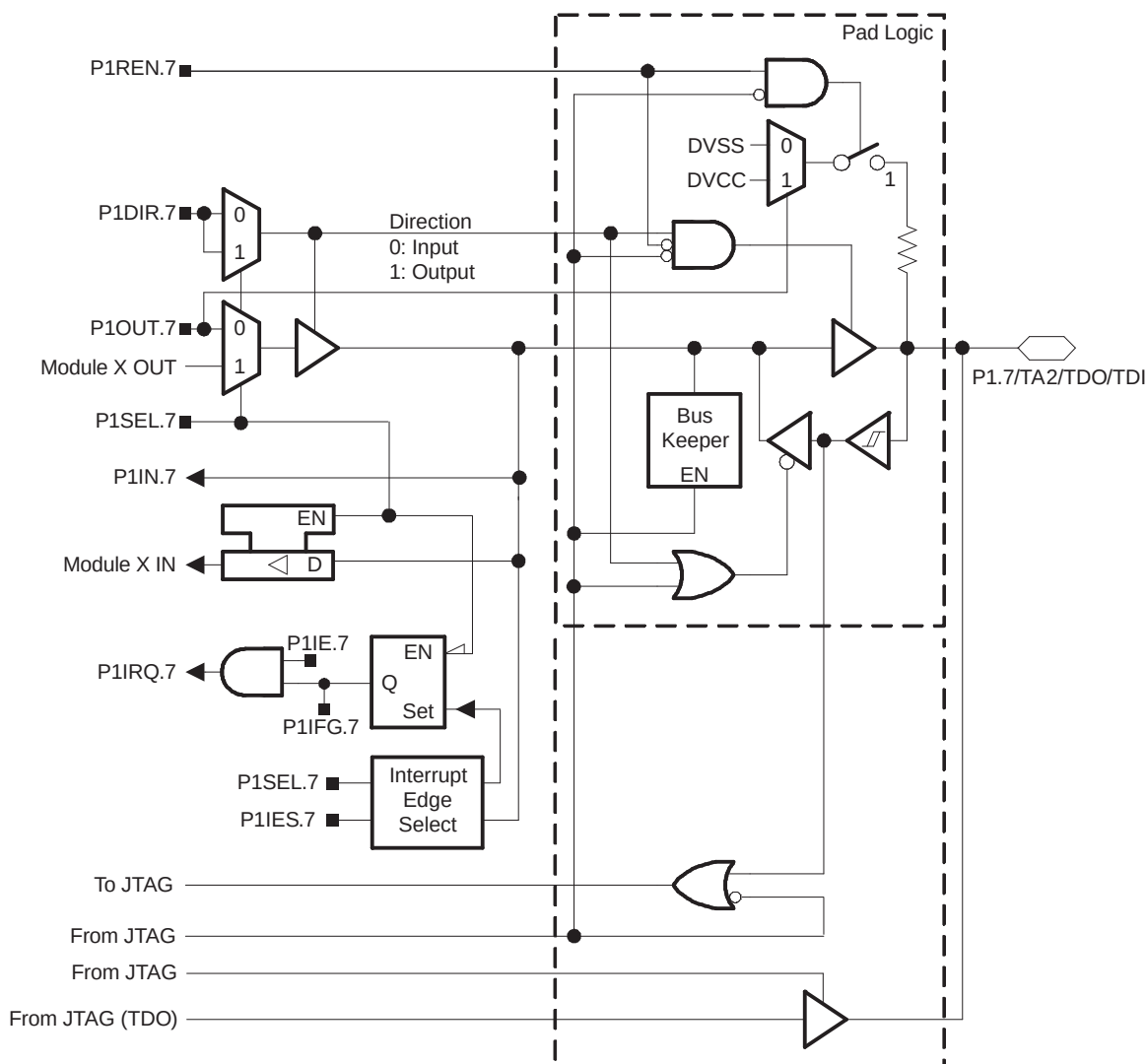
(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Function controlled by JTAG

## Port P1 Pin Schematic: P1.7, Input/Output With Schmitt Trigger and In-System Access Features



## Port P1 (P1.7) Pin Functions

| PIN NAME (P1.X)  | X | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |             |
|------------------|---|---------------------------|-------------------------------------|---------|-------------|
|                  |   |                           | P1DIR.x                             | P1SEL.x | 4-Wire JTAG |
| P1.7/TA2/TDO/TDI | 7 | P1.7 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0           |
|                  |   | Timer_A3.TA2              | 1                                   | 1       | 0           |
|                  |   | TDO/TDI <sup>(4)</sup>    | X                                   | X       | 1           |

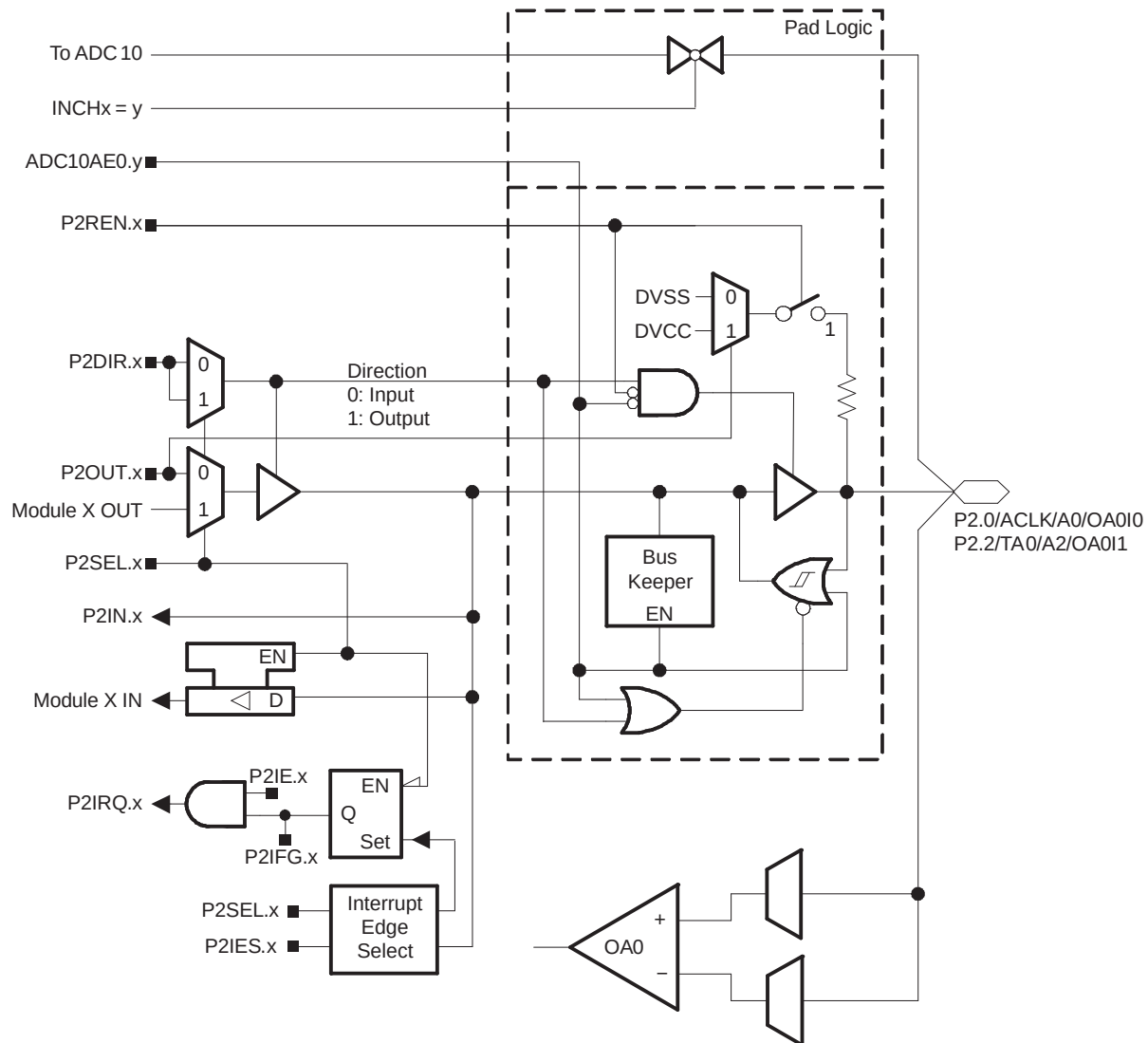
(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Function controlled by JTAG

## Port P2 Pin Schematic: P2.0, P2.2, Input/Output With Schmitt Trigger



## Port P2 (P2.0, P2.2) Pin Functions

| Pin Name (P2.X)    | X | Y | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|--------------------|---|---|---------------------------|-------------------------------------|---------|------------|
|                    |   |   |                           | P2DIR.x                             | P2SEL.x | ADC10AE0.y |
| P2.0/ACLK/A0/OA0I0 | 0 | 0 | P2.0 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0          |
|                    |   |   | ACLK                      | 1                                   | 1       | 0          |
|                    |   |   | A0/OA0I0 <sup>(4)</sup>   | X                                   | X       | 1          |
| P2.2/TA0/A2/OA0I1  | 2 | 2 | P2.2 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0          |
|                    |   |   | Timer_A3.CCI0B            | 0                                   | 1       | 0          |
|                    |   |   | Timer_A3.TA0              | 1                                   | 1       | 0          |
|                    |   |   | A2/OA0I1 <sup>(4)</sup>   | X                                   | X       | 1          |

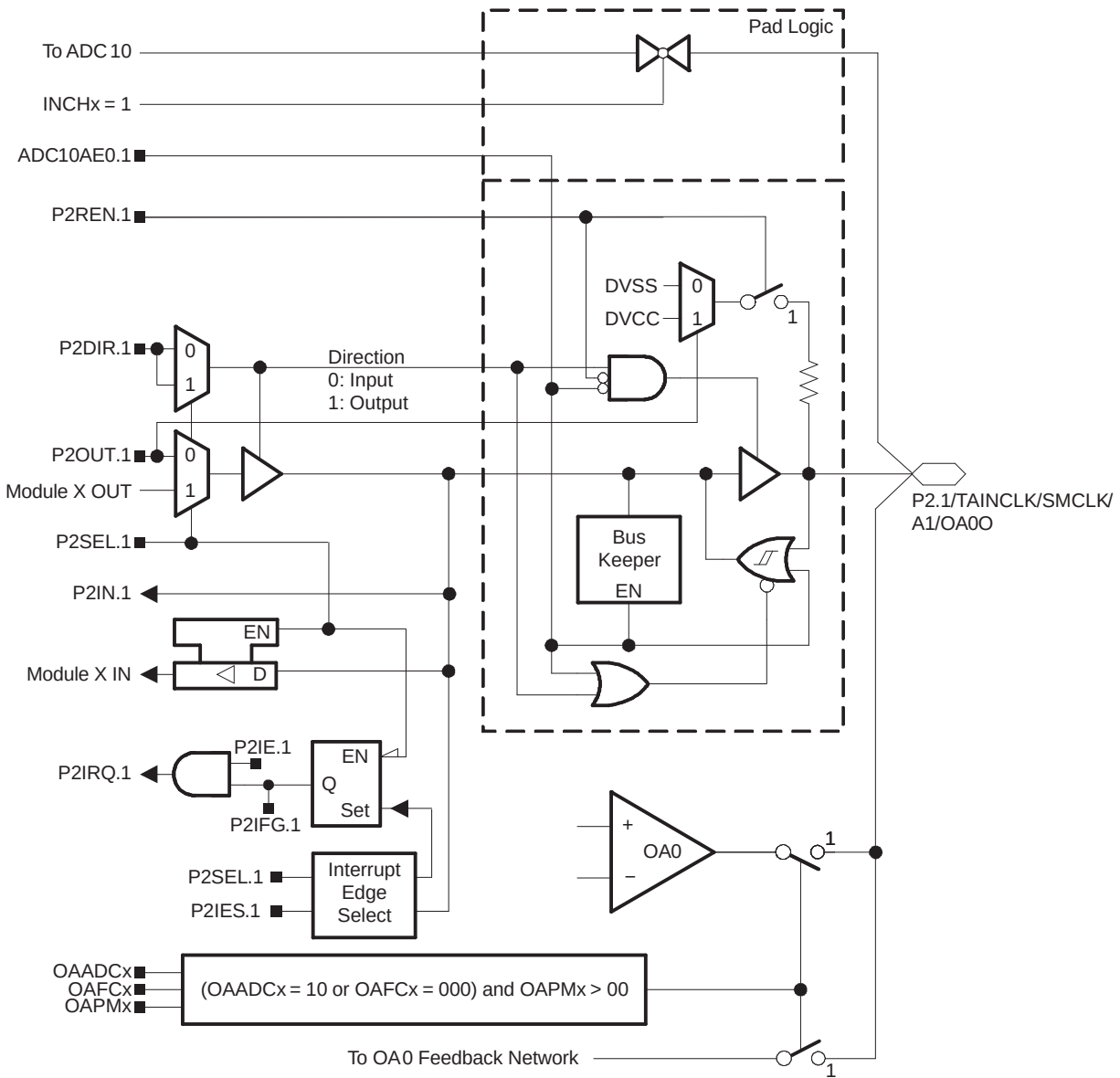
(1) N/A: Not available or not applicable

(2) X: Don't care

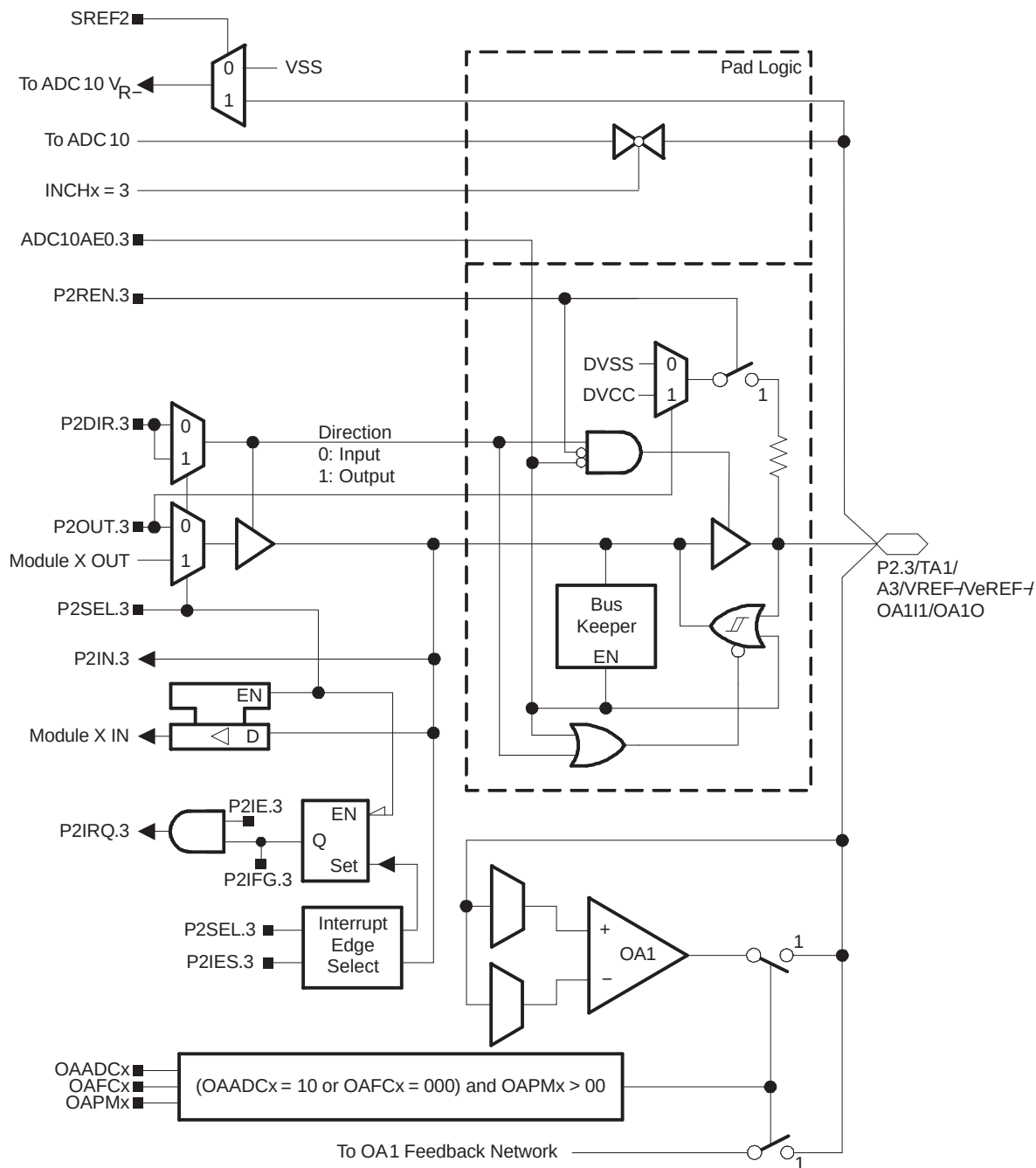
(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

## Port P2 Pin Schematic: P2.1, Input/Output With Schmitt Trigger



## Port P2 Pin Schematic: P2.3, Input/Output With Schmitt Trigger



## Port P2 (P2.1) Pin Functions

| PIN NAME (P2.X)            | X | Y | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|----------------------------|---|---|---------------------------|-------------------------------------|---------|------------|
|                            |   |   |                           | P2DIR.x                             | P2SEL.x | ADC10AE0.y |
| P2.1/TAINCLK/SMCLK/A1/OA00 | 1 | 1 | P2.1 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0          |
|                            |   |   | Timer_A3.INCLK            | 0                                   | 1       | 0          |
|                            |   |   | SMCLK                     | 1                                   | 1       | 0          |
|                            |   |   | A1/OA00 <sup>(4)</sup>    | X                                   | X       | 1          |

(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

## Port P2 (P2.3) Pin Functions

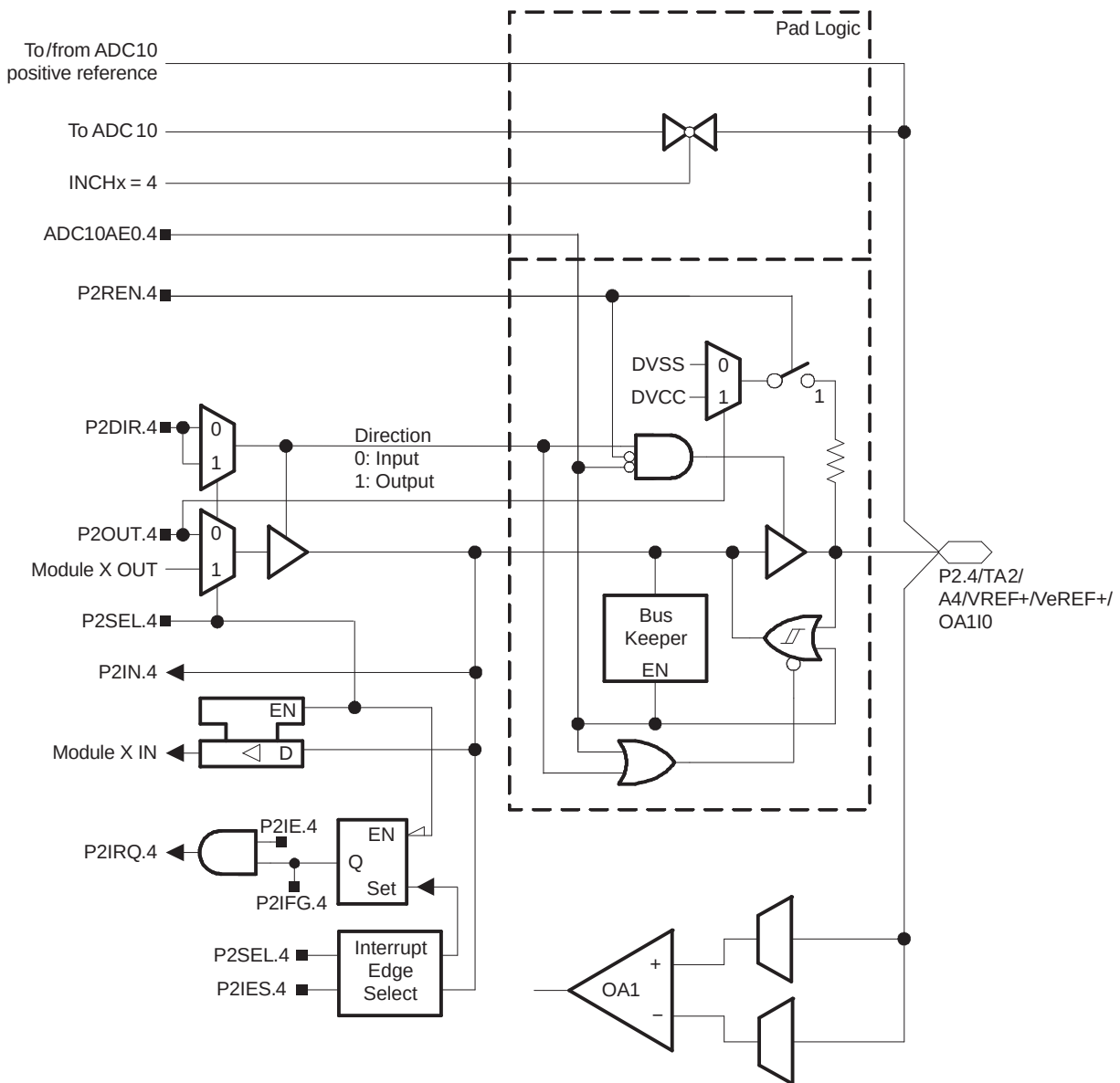
| PIN NAME (P2.X)                                               | X | Y | FUNCTION <sup>(1)</sup>                                             | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|---------------------------------------------------------------|---|---|---------------------------------------------------------------------|-------------------------------------|---------|------------|
|                                                               |   |   |                                                                     | P2DIR.x                             | P2SEL.x | ADC10AE0.y |
| P2.3/TA1/A3/V <sub>REF-</sub> /V <sub>eREF-</sub> /OA1I1/OA1O | 3 | 3 | P2.3 <sup>(3)</sup> (I/O)                                           | I: 0; O: 1                          | 0       | 0          |
|                                                               |   |   | Timer_A3.CCI1B                                                      | 0                                   | 1       | 0          |
|                                                               |   |   | Timer_A3.TA1                                                        | 1                                   | 1       | 0          |
|                                                               |   |   | A3/V <sub>REF-</sub> /V <sub>eREF-</sub> /OA1I1/OA1O <sup>(4)</sup> | X                                   | X       | 1          |

(1) N/A: Not available or not applicable

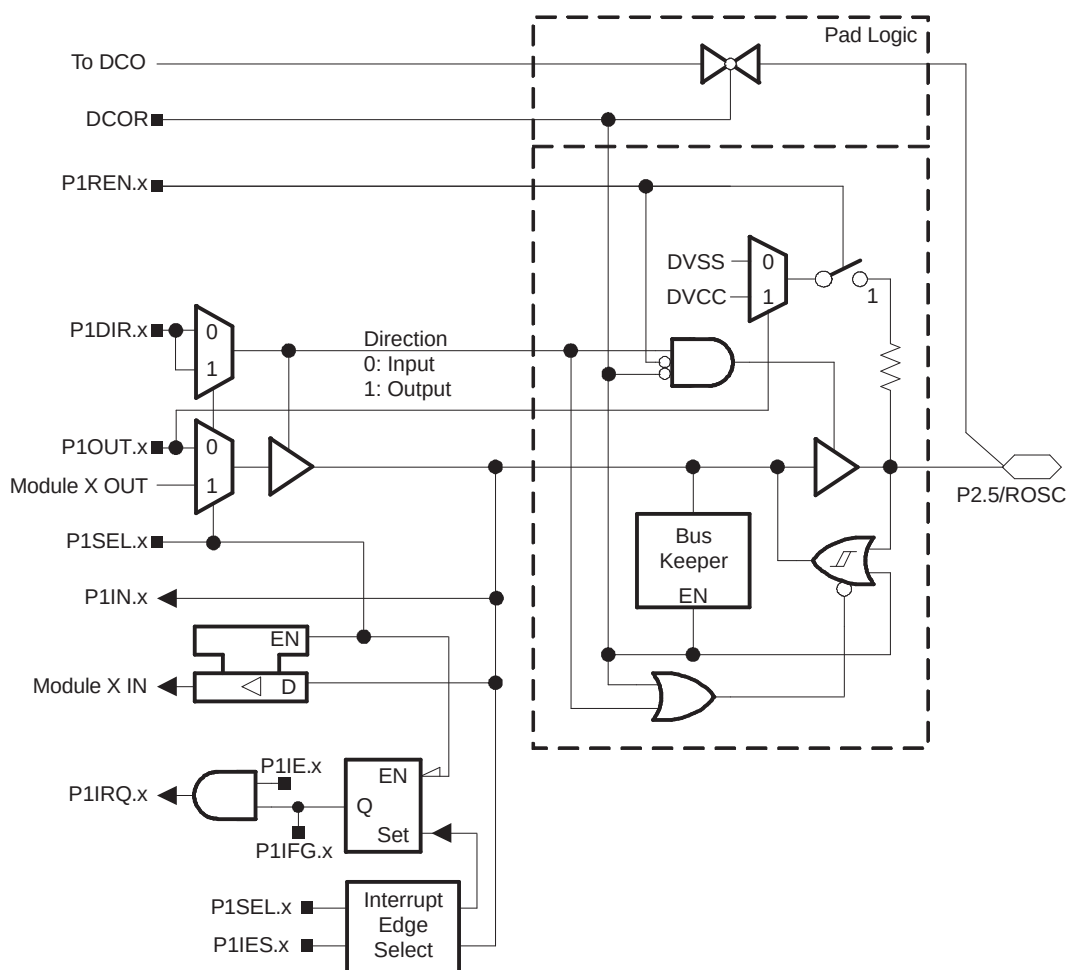
(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.



| PIN NAME (P2.X)                                         | X | Y | FUNCTION <sup>(1)</sup>                                       | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|---------------------------------------------------------|---|---|---------------------------------------------------------------|-------------------------------------|---------|------------|
|                                                         |   |   |                                                               | P2DIR.x                             | P2SEL.x | ADC10AE0.y |
| P2.4/TA2/A4/V <sub>REF+</sub> /V <sub>REF+</sub> /OA1I0 | 4 | 4 | P2.4 <sup>(3)</sup> (I/O)                                     | I: 0; O: 1                          | 0       | 0          |
|                                                         |   |   | Timer_A3.TA2                                                  | 1                                   | 1       | 0          |
|                                                         |   |   | A4/V <sub>REF+</sub> /V <sub>REF+</sub> /OA1I0 <sup>(4)</sup> | X                                   | X       | 1          |

**Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger and External R<sub>OSC</sub> for DCO**

**Port P2 (P2.5) Pin Functions**

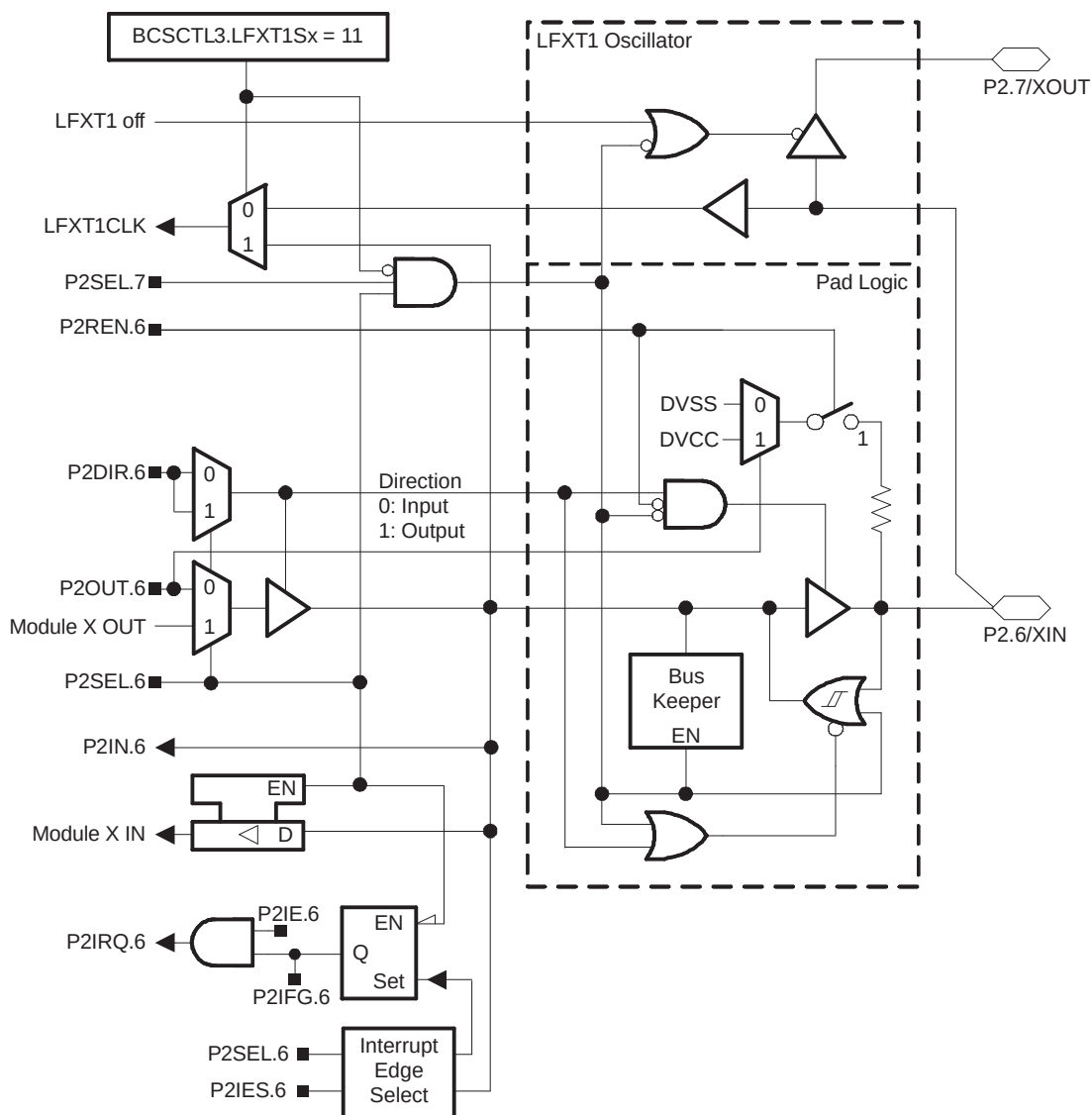
| PIN NAME (P2.X)       | X | FUNCTION                  | CONTROL BITS/SIGNALS <sup>(1)</sup> |         |      |
|-----------------------|---|---------------------------|-------------------------------------|---------|------|
|                       |   |                           | P2DIR.x                             | P2SEL.x | DCOR |
| P2.5/R <sub>OSC</sub> | 5 | P2.5 <sup>(2)</sup> (I/O) | 0/1                                 | 0       | 0    |
|                       |   | N/A <sup>(3)</sup>        | 0                                   | 1       | 0    |
|                       |   | DV <sub>SS</sub>          | 1                                   | 1       | 0    |
|                       |   | R <sub>OSC</sub>          | X                                   | X       | 1    |

(1) X: Don't care

(2) Default after reset (PUC/POR)

(3) N/A: Not available or not applicable

## Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger and Crystal Oscillator Input



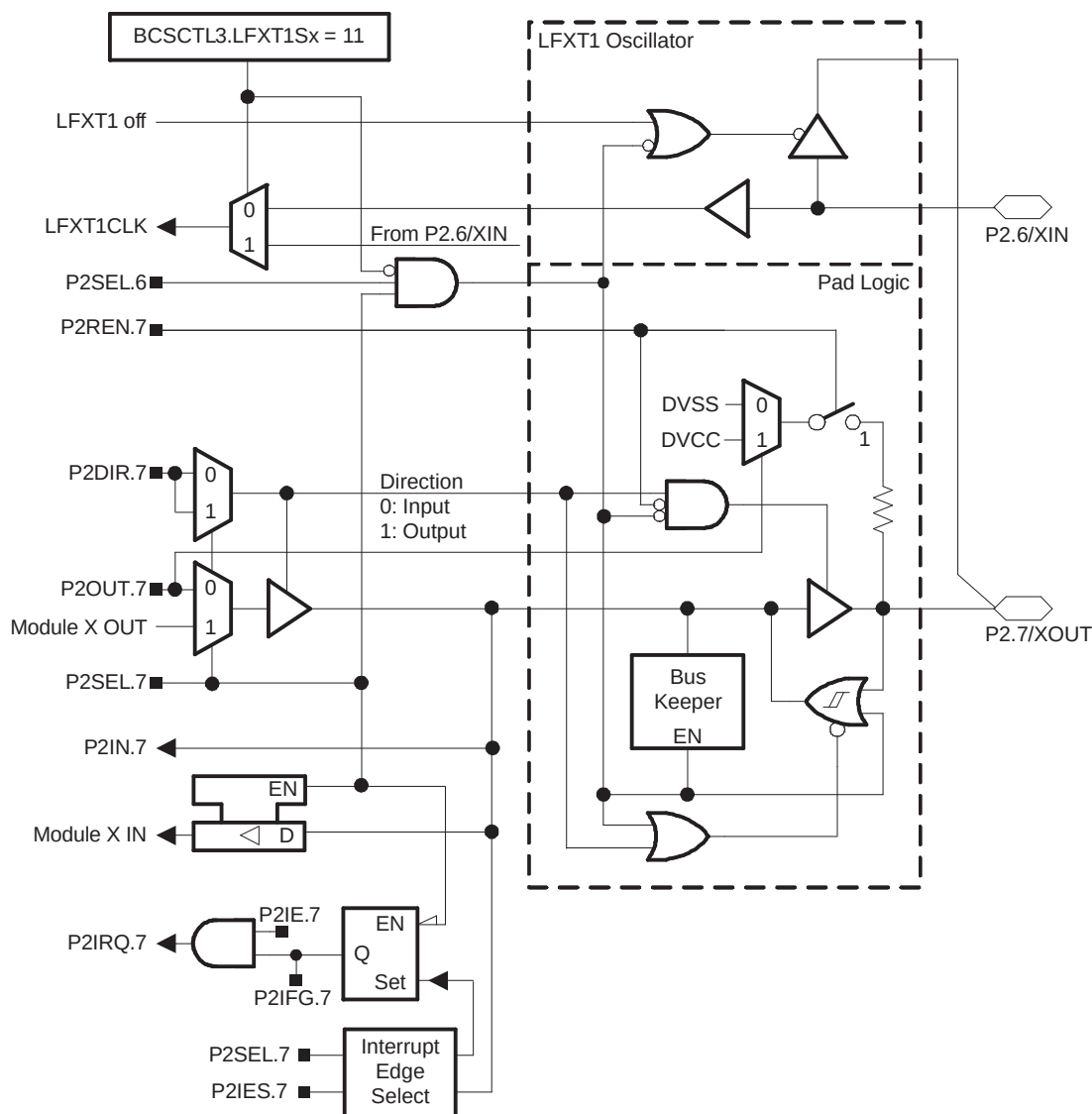
## Port P2 (P2.6) Pin Functions

| PIN NAME (P2.X) | X | FUNCTION <sup>(1)</sup> | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |
|-----------------|---|-------------------------|-------------------------------------|---------|
|                 |   |                         | P2DIR.x                             | P2SEL.x |
| P2.6/XIN        | 6 | P2.6 (I/O)              | I: 0; O: 1                          | 0       |
|                 |   | XIN <sup>(3)</sup>      | X                                   | 1       |

(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

**Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger and Crystal Oscillator Output**

**Port P2 (P2.7) Pin Functions**

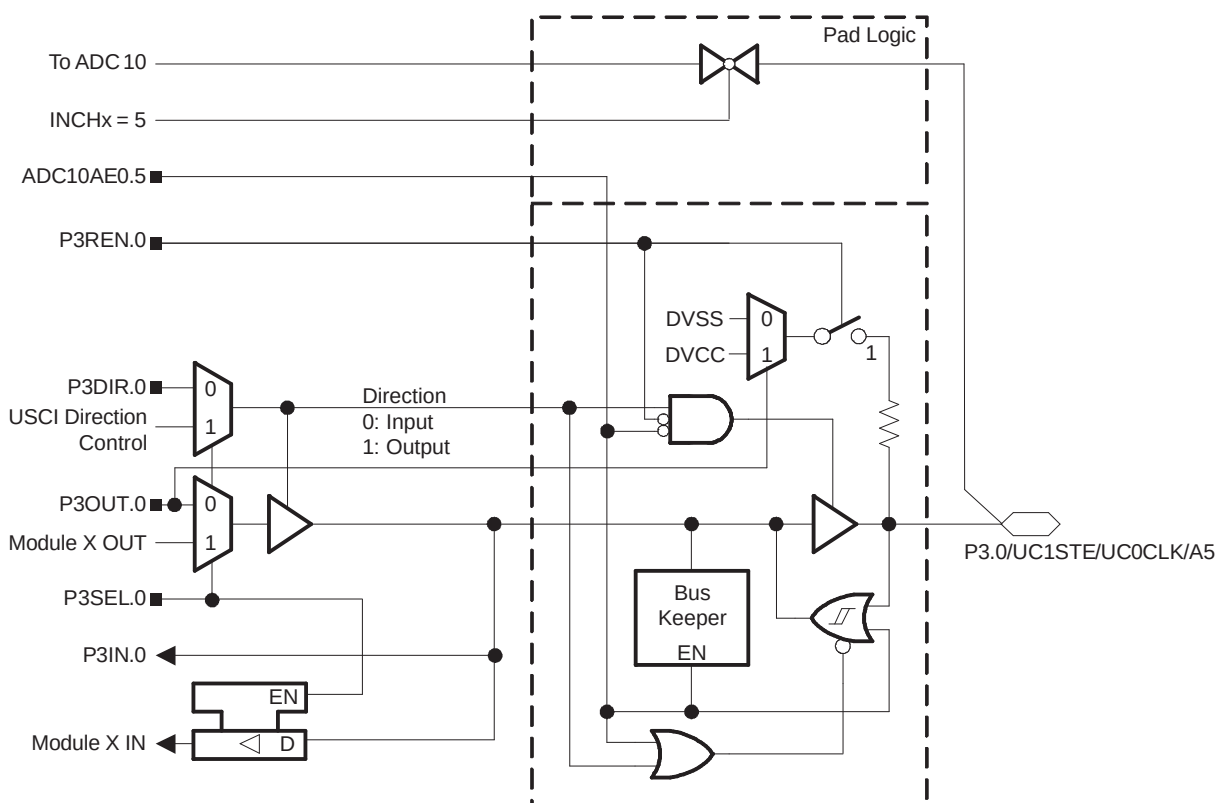
| PIN NAME (P2.X) | X | FUNCTION <sup>(1)</sup> | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |
|-----------------|---|-------------------------|-------------------------------------|---------|
|                 |   |                         | P2DIR.x                             | P2SEL.x |
| XOUT/P2.7       | 6 | P2.7 (I/O)              | I: 0; O: 1                          | 0       |
|                 |   | XOUT <sup>(3) (4)</sup> | X                                   | 1       |

(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

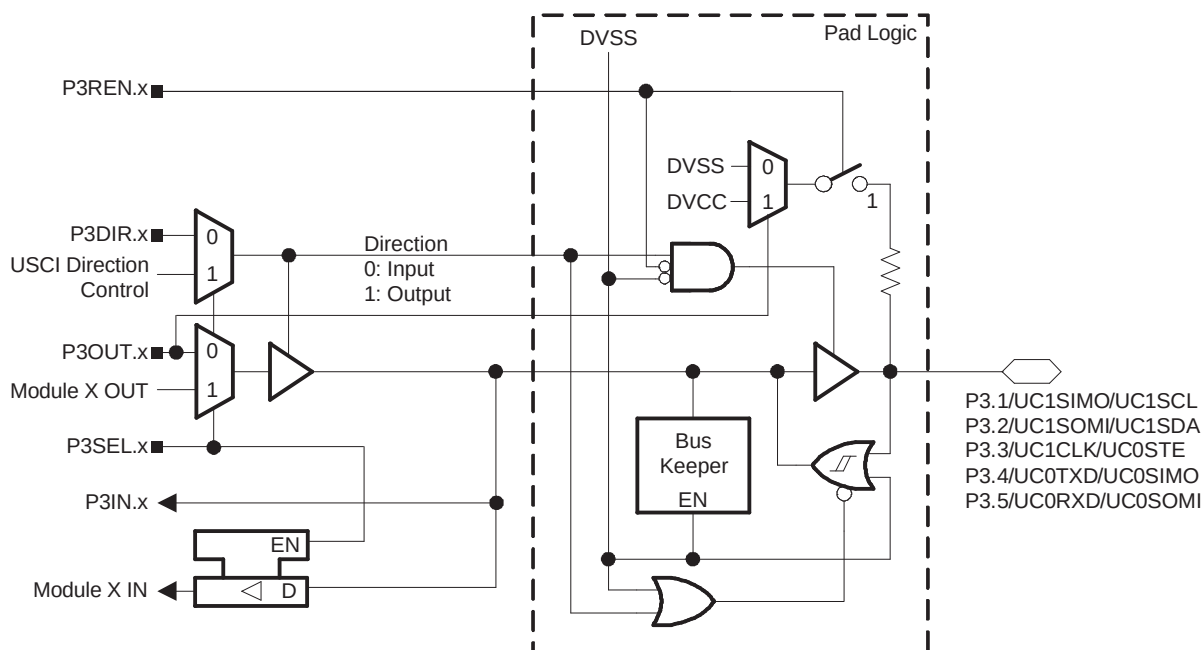
(4) If the pin XOUT/P2.7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.



| PIN NAME (P1.X)       | X | Y | FUNCTION <sup>(1)</sup>                     | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|-----------------------|---|---|---------------------------------------------|-------------------------------------|---------|------------|
|                       |   |   |                                             | P3DIR.x                             | P3SEL.x | ADC10AE0.y |
| P3.0/UC1STE/UC0CLK/A5 | 0 | 5 | P3.0 <sup>(3)</sup> (I/O)                   | I: 0; O: 1                          | 0       | 0          |
|                       |   |   | UC1STE/UC0CLK <sup>(4)</sup> <sup>(5)</sup> | X                                   | 1       | 0          |
|                       |   |   | A5 <sup>(6)</sup>                           | X                                   | X       | 1          |

- (1) N/A: Not available or not applicable
- (2) X: Don't care
- (3) Default after reset (PUC/POR)
- (4) The pin direction is controlled by the USCI module.
- (5) UC0CLK function takes precedence over UC1STE function. If the pin is required as UC0CLK input or output USCI1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
- (6) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

## Port P3 Pin Schematic: P3.1 to P3.5, Input/Output With Schmitt Trigger



## Port P3 (P3.1 to P3.5) Pin Functions

| PIN NAME (P3.X)     | X | FUNCTION <sup>(1)</sup>          | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |
|---------------------|---|----------------------------------|-------------------------------------|---------|
|                     |   |                                  | P3DIR.x                             | P3SEL.x |
| P3.1/UC1SIMO/UC1SDA | 1 | P3.1 <sup>(3)</sup> (I/O)        | I: 0; O: 1                          | 0       |
|                     |   | UC1SIMO/UC1SDA <sup>(4)</sup>    | X                                   | 1       |
| P3.2/UC1SOMI/UC1SCL | 1 | P3.2 <sup>(5)</sup> (I/O)        | I: 0; O: 1                          | 0       |
|                     |   | UC1SOMI/UC1SCL <sup>(6)</sup>    | X                                   | 1       |
| P3.3/UC1CLK/UC0STE  | 1 | P3.3 <sup>(5)</sup> (I/O)        | I: 0; O: 1                          | 0       |
|                     |   | UC1CLK/UC0STE <sup>(6) (7)</sup> | X                                   | 1       |
| P3.4/UC0TXD/UC0SIMO | 1 | P3.4 <sup>(5)</sup> (I/O)        | I: 0; O: 1                          | 0       |
|                     |   | UC0TXD/UC0SIMO <sup>(6)</sup>    | X                                   | 1       |
| P3.5/UC0RXD/UC0SOMI | 1 | P3.5 <sup>(5)</sup> (I/O)        | I: 0; O: 1                          | 0       |
|                     |   | UC0RXD/UC0SOMI <sup>(6)</sup>    | X                                   | 1       |

(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

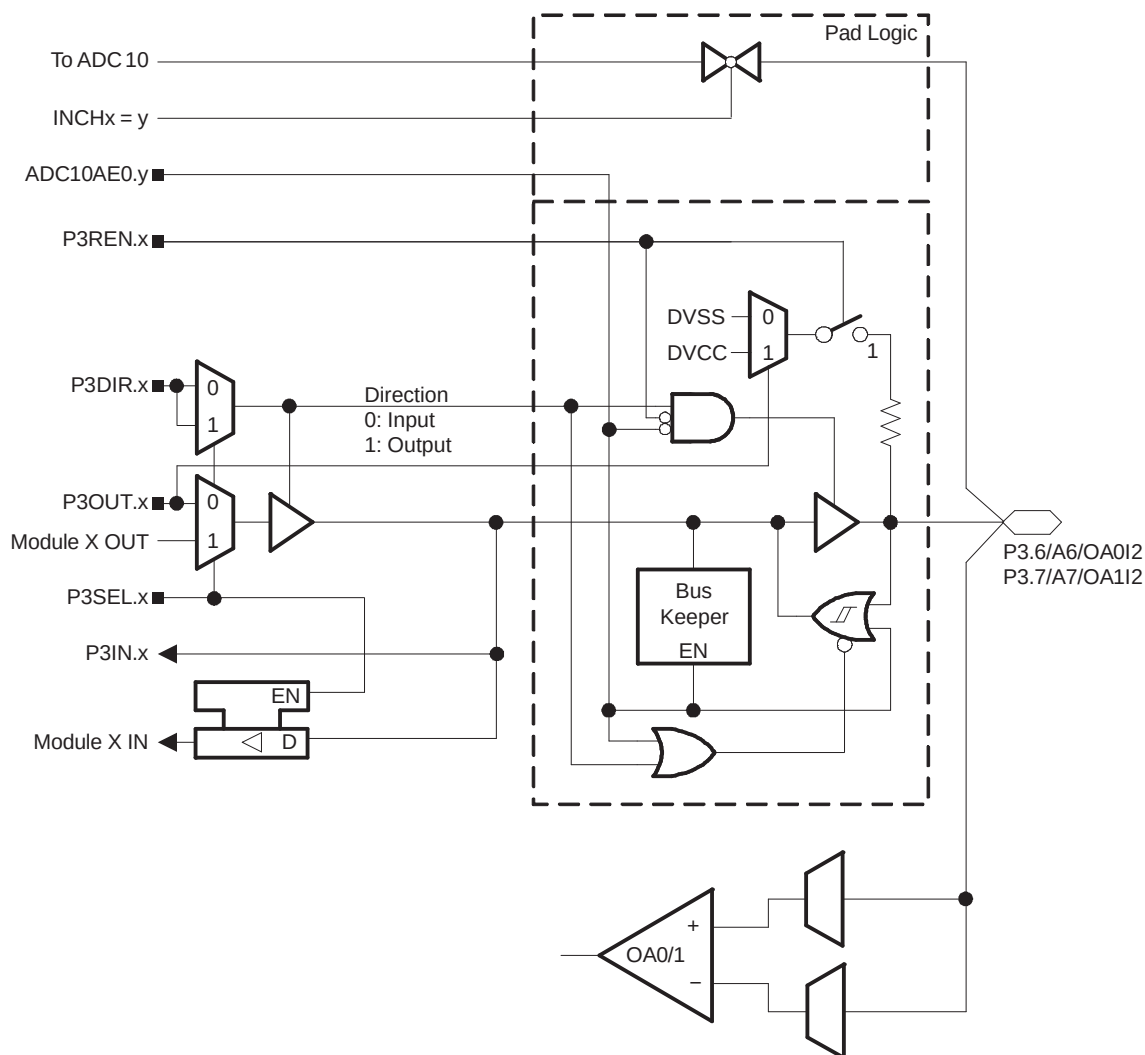
(4) The pin direction is controlled by the USC1 module.

(5) Default after reset (PUC/POR)

(6) The pin direction is controlled by the USC1 module.

(7) UC1CLK function takes precedence over UC0STE function. If the pin is required as UC1CLK input or output, USC10 is forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

## Port P3 Pin Schematic: P3.6 to P3.7, Input/Output With Schmitt Trigger



## Port P3 (P3.6, P3.7) Pin Functions

| PIN NAME (P3.X) | X | Y | FUNCTION <sup>(1) (2)</sup> | CONTROL BITS/SIGNALS <sup>(3)</sup> |         |            |
|-----------------|---|---|-----------------------------|-------------------------------------|---------|------------|
|                 |   |   |                             | P3DIR.x                             | P3SEL.x | ADC10AE0.y |
| P3.6/A6/OA0I2   | 6 | 6 | P3.6 <sup>(4)</sup> (I/O)   | I: 0; O: 1                          | 0       | 0          |
|                 |   |   | A6/OA0I2 <sup>(5)</sup>     | X                                   | X       | 1          |
| P3.7/A7/OA1I2   | 7 | 7 | P3.7 <sup>(4)</sup> (I/O)   | I: 0; O: 1                          | 0       | 0          |
|                 |   |   | A7/OA1I2 <sup>(5)</sup>     | X                                   | X       | 1          |

(1) N/A: Not available or not applicable

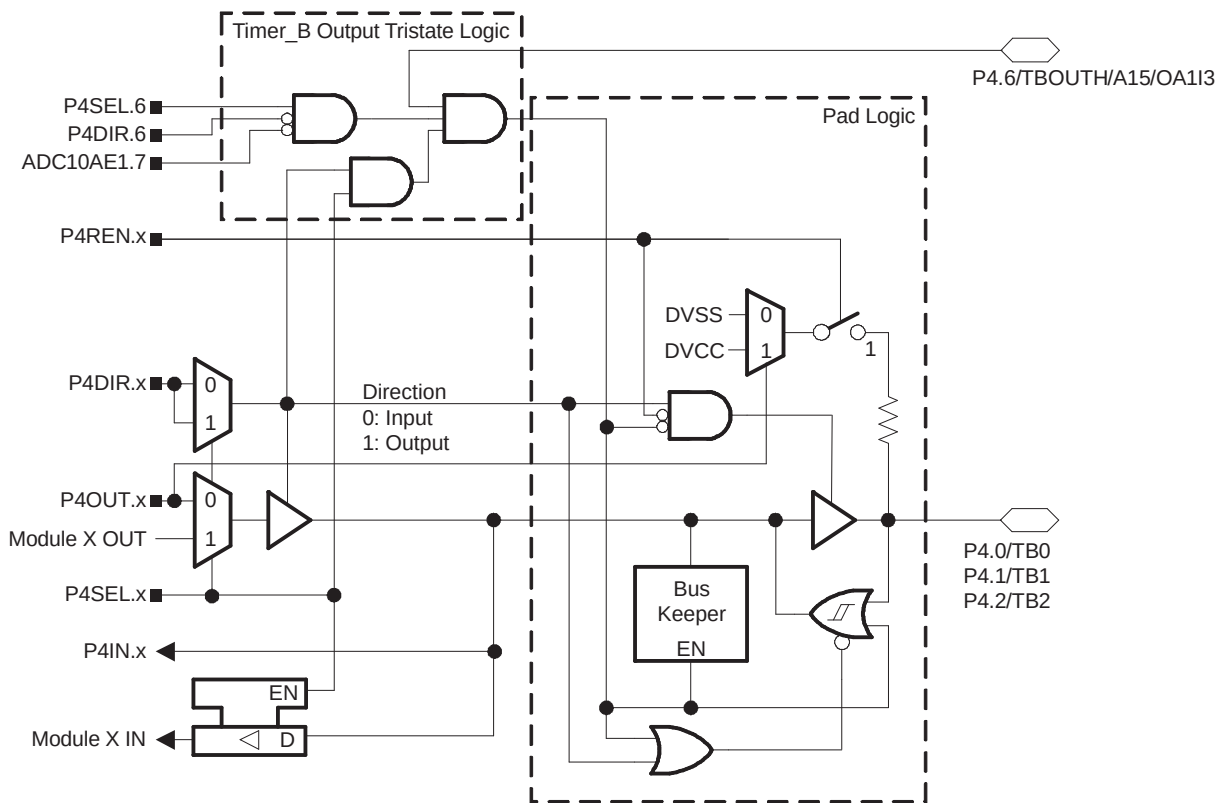
(2) UC0CLK function takes precedence over UC0STE function. If the pin is required as UC1CLK input or output, USC10 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

(3) X: Don't care

(4) Default after reset (PUC/POR)

(5) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

**Port P4 Pin Schematic: P4.0 to P4.2, Input/Output With Schmitt Trigger**

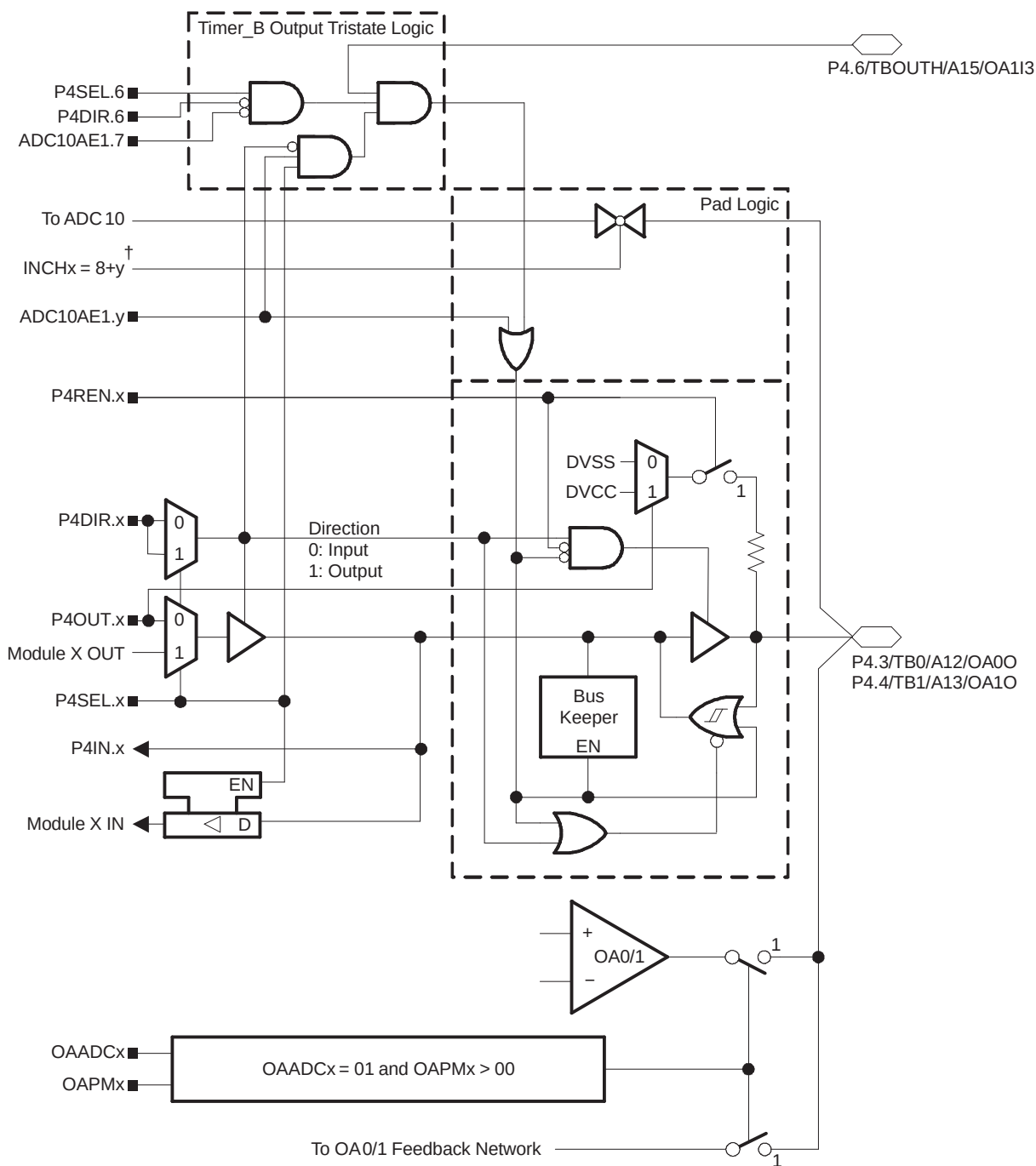


**Port P4 (P4.0 to P4.2) Pin Functions**

| PIN NAME (P4.X) | X | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS |         |
|-----------------|---|---------------------------|----------------------|---------|
|                 |   |                           | P4DIR.x              | P4SEL.x |
| P4.0/TB0        | 0 | P4.0 <sup>(2)</sup> (I/O) | I: 0; O: 1           | 0       |
|                 |   | Timer_B3.CCI0A            | 0                    | 1       |
|                 |   | Timer_B3.TB0              | 1                    | 1       |
| P4.1/TB1        | 1 | P4.1 <sup>(2)</sup> (I/O) | I: 0; O: 1           | 0       |
|                 |   | Timer_B3.CCI1A            | 0                    | 1       |
|                 |   | Timer_B3.TB1              | 1                    | 1       |
| P4.2/TB2        | 2 | P4.2 <sup>(2)</sup> (I/O) | I: 0; O: 1           | 0       |
|                 |   | Timer_B3.CCI2A            | 0                    | 1       |
|                 |   | Timer_B3.TB2              | 1                    | 1       |

(1) N/A: Not available or not applicable.  
(2) Default after reset (PUC/POR)

## Port P4 Pin Schematic: P4.3 to P4.4, Input/Output With Schmitt Trigger



†If OAADCx = 11 and not OAFcx = 000, the ADC input A12 or A13 is internally connected to the OA0 or OA1 output, respectively, and the connections from the ADC and the operational amplifiers to the pad are disabled.

**Port P4 (P4.3 to P4.4) Pin Functions**

| PIN NAME (P4.X)   | X | Y | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|-------------------|---|---|---------------------------|-------------------------------------|---------|------------|
|                   |   |   |                           | P4DIR.x                             | P4SEL.x | ADC10AE1.y |
| P4.3/TB0/A12/OA0O | 3 | 4 | P4.3 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0          |
|                   |   |   | Timer_B3.CCI0B            | 0                                   | 1       | 0          |
|                   |   |   | Timer_B3.TB0              | 1                                   | 1       | 0          |
|                   |   |   | A12/OA0O <sup>(4)</sup>   | X                                   | X       | 1          |
| P4.4/TB1/A13/OA1O | 4 | 5 | P4.4 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0          |
|                   |   |   | Timer_B3.CCI1B            | 0                                   | 1       | 0          |
|                   |   |   | Timer_B3.TB1              | 1                                   | 1       | 0          |
|                   |   |   | A13/OA1O <sup>(4)</sup>   | X                                   | X       | 1          |

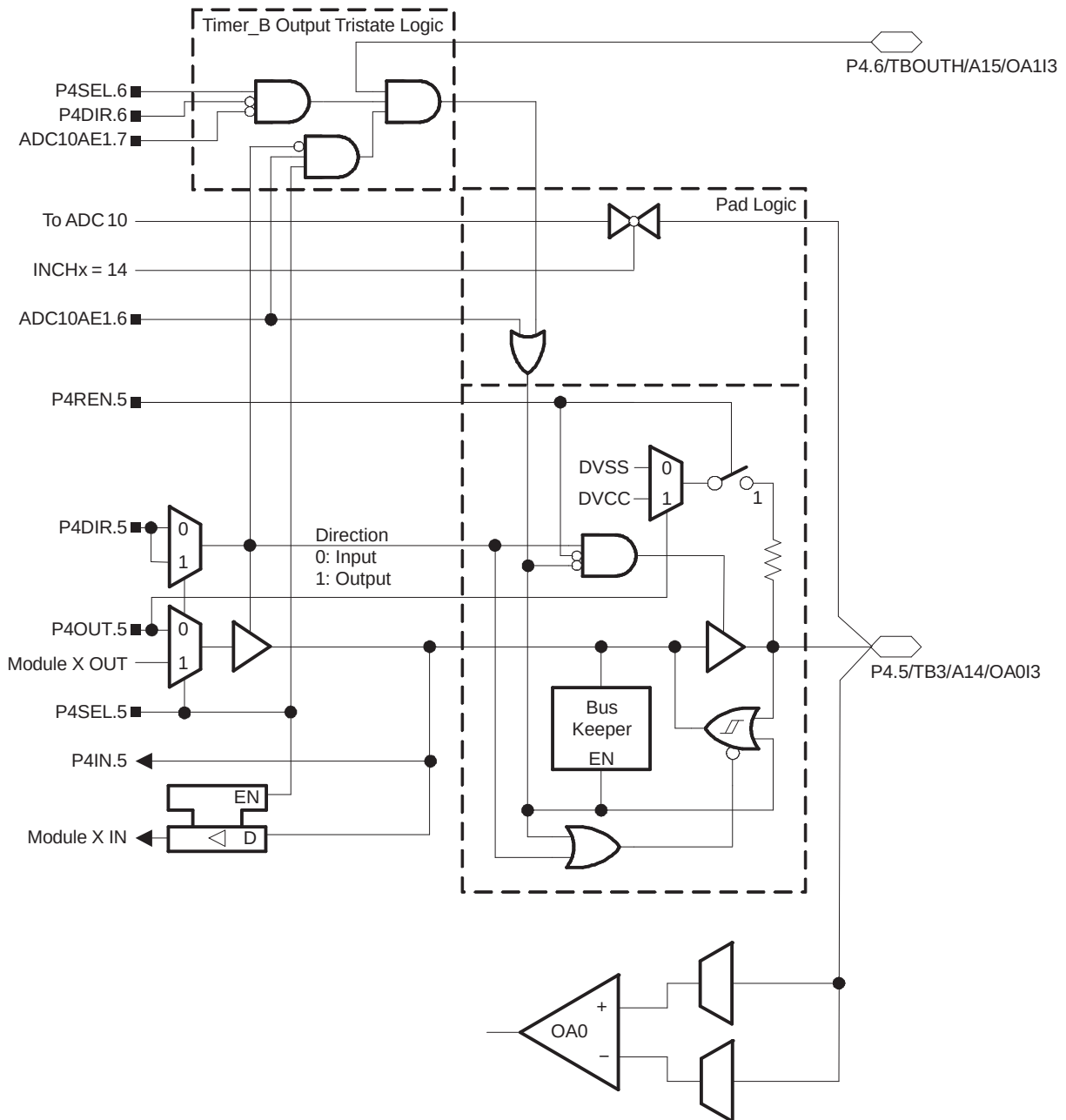
(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

## Port P4 Pin Schematic: P4.5, Input/Output With Schmitt Trigger



## Port P4 (P4.5) Pin Functions

| PIN NAME (P4.X)    | X | Y | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|--------------------|---|---|---------------------------|-------------------------------------|---------|------------|
|                    |   |   |                           | P4DIR.x                             | P4SEL.x | ADC10AE1.y |
| P4.5/TB3/A14/OA0I3 | 5 | 6 | P4.5 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0          |
|                    |   |   | Timer_B3.TB2              | 1                                   | 1       | 0          |
|                    |   |   | A14/OA0I3 <sup>(4)</sup>  | X                                   | X       | 1          |

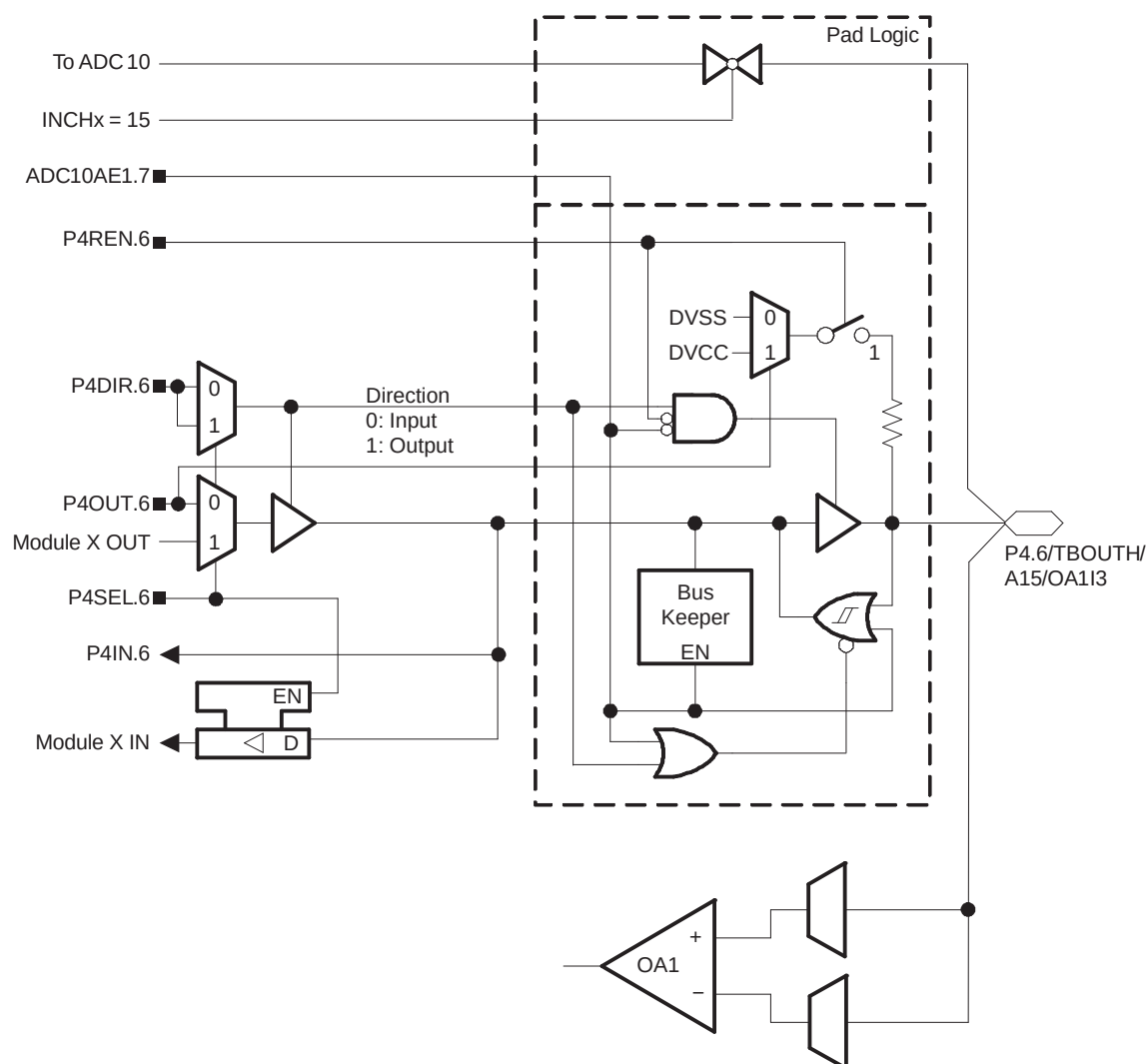
(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

## Port P4 Pin Schematic: P4.6, Input/Output With Schmitt Trigger



## Port P4 (P4.6) Pin Functions

| PIN NAME (P4.X)       | X | Y | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS <sup>(2)</sup> |         |            |
|-----------------------|---|---|---------------------------|-------------------------------------|---------|------------|
|                       |   |   |                           | P4DIR.x                             | P4SEL.x | ADC10AE1.y |
| P4.6/TBOUTH/A15/OA1I3 | 6 | 7 | P4.6 <sup>(3)</sup> (I/O) | I: 0; O: 1                          | 0       | 0          |
|                       |   |   | TBOUTH                    | 0                                   | 1       | 0          |
|                       |   |   | DV <sub>SS</sub>          | 1                                   | 1       | 0          |
|                       |   |   | A15/OA1I3 <sup>(4)</sup>  | X                                   | X       | 1          |

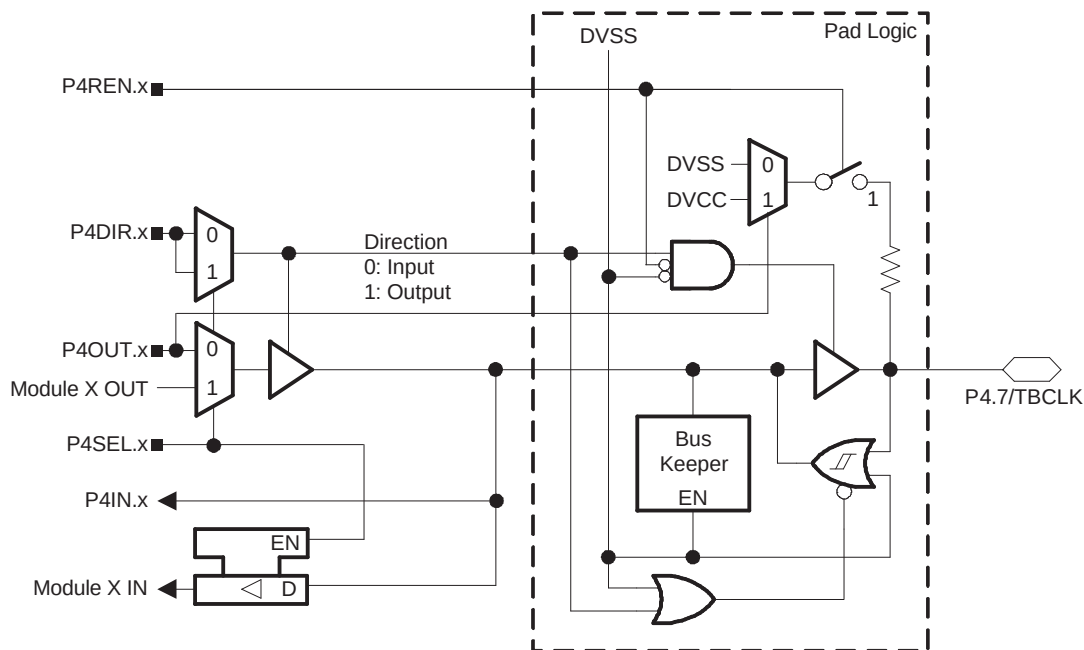
(1) N/A: Not available or not applicable

(2) X: Don't care

(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

## Port P4 Pin Schematic: P4.7, Input/Output With Schmitt Trigger



## Port P4 (Pr.7) Pin Functions

| PIN NAME (P4.X) | X | FUNCTION <sup>(1)</sup>   | CONTROL BITS/SIGNALS |         |
|-----------------|---|---------------------------|----------------------|---------|
|                 |   |                           | P4DIR.x              | P4SEL.x |
| P4.7/TBCLK      | 7 | P4.7 <sup>(2)</sup> (I/O) | I: 0; O: 1           | 0       |
|                 |   | Timer_B3.TBCLK            | 0                    | 1       |
|                 |   | DV <sub>SS</sub>          | 1                    | 1       |

(1) N/A: Not available or not applicable

(2) Default after reset (PUC/POR)

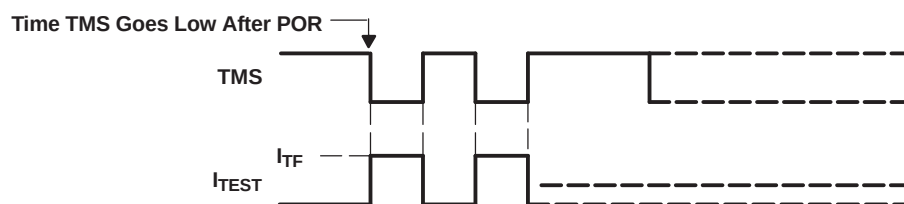
## JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current,  $I_{TF}$ , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see [Figure 28](#)). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).



**Figure 28. Fuse Check Mode Current, MSP430F22xx**

### NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the Bootstrap Loader section for more information.

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430F2274MDATEP</a>  | Active        | Production           | TSSOP (DA)   38 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -55 to 125   | M430F2274MEP        |
| <a href="#">MSP430F2274MRHATEP</a> | Active        | Production           | VQFN (RHA)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -55 to 125   | M4F2274<br>MRHATEP  |
| <a href="#">V62/08631-01XE</a>     | Active        | Production           | VQFN (RHA)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -55 to 125   | M4F2274<br>MRHATEP  |
| <a href="#">V62/08631-01YE</a>     | Active        | Production           | TSSOP (DA)   38 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -55 to 125   | M430F2274MEP        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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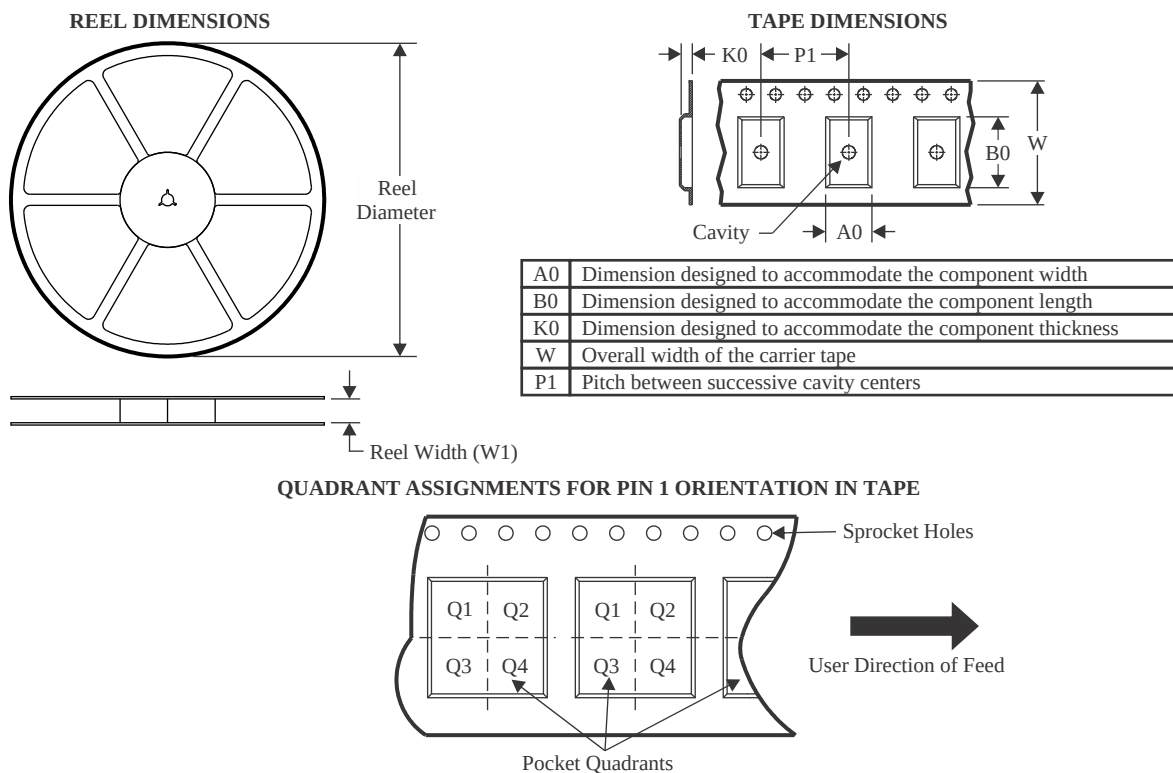
**OTHER QUALIFIED VERSIONS OF MSP430F2274-EP :**

- Catalog : [MSP430F2274](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

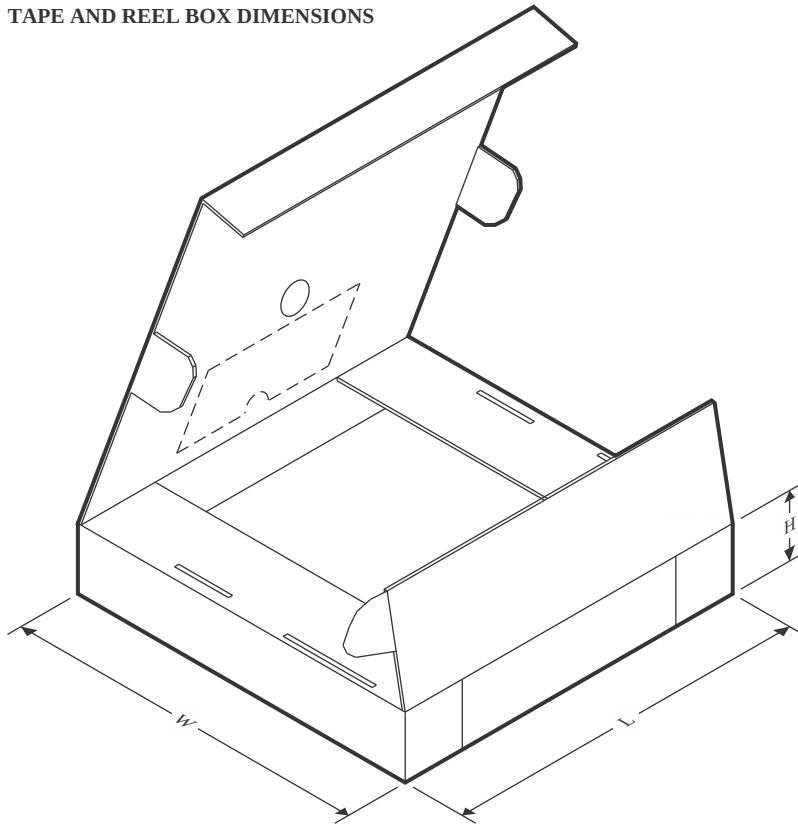
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F2274MRHATEP | VQFN         | RHA             | 40   | 250 | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



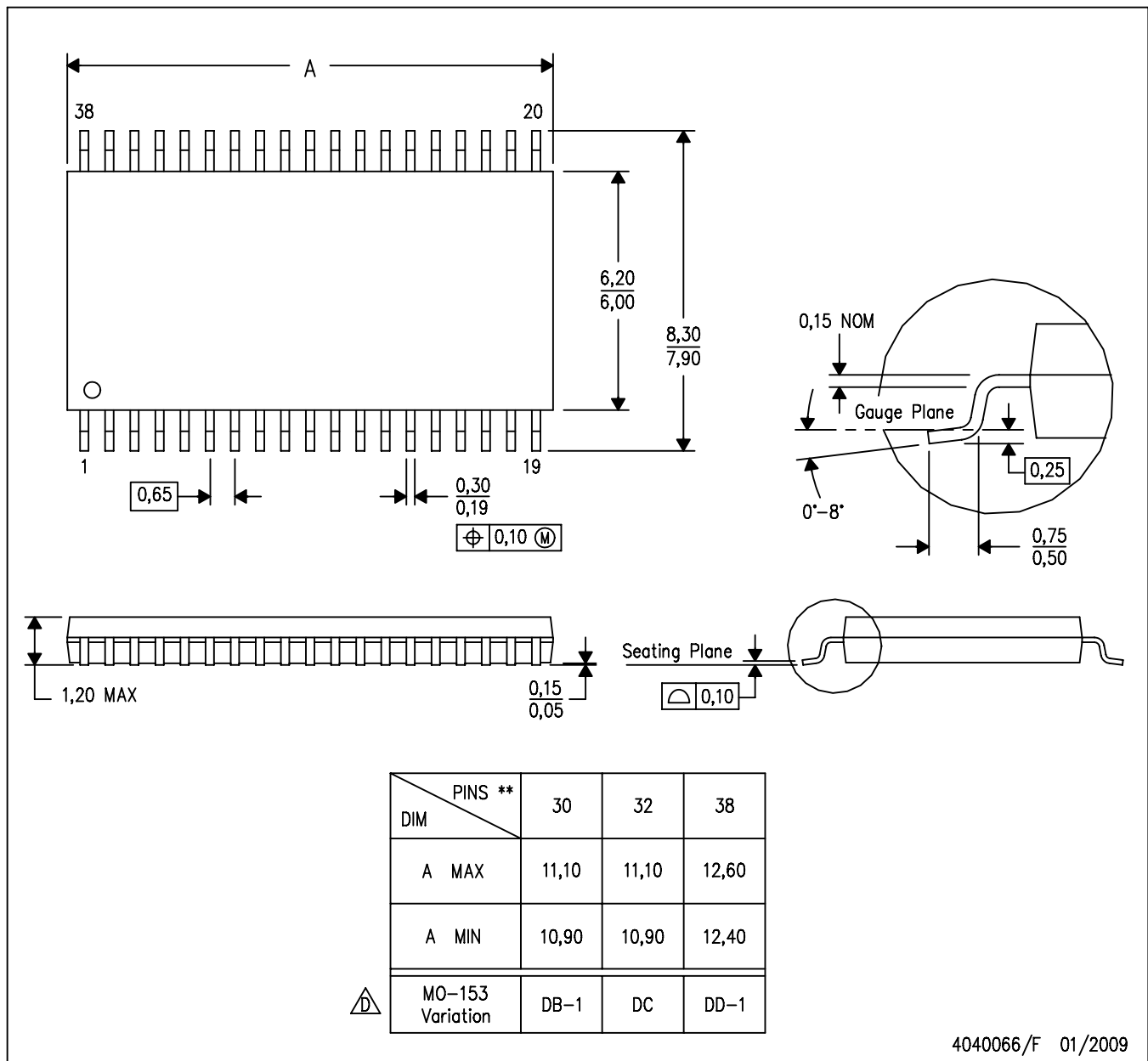
\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| MSP430F2274MRHATEP | VQFN         | RHA             | 40   | 250 | 213.0       | 191.0      | 35.0        |

DA (R-PDSO-G\*\*)

38 PIN SHOWN

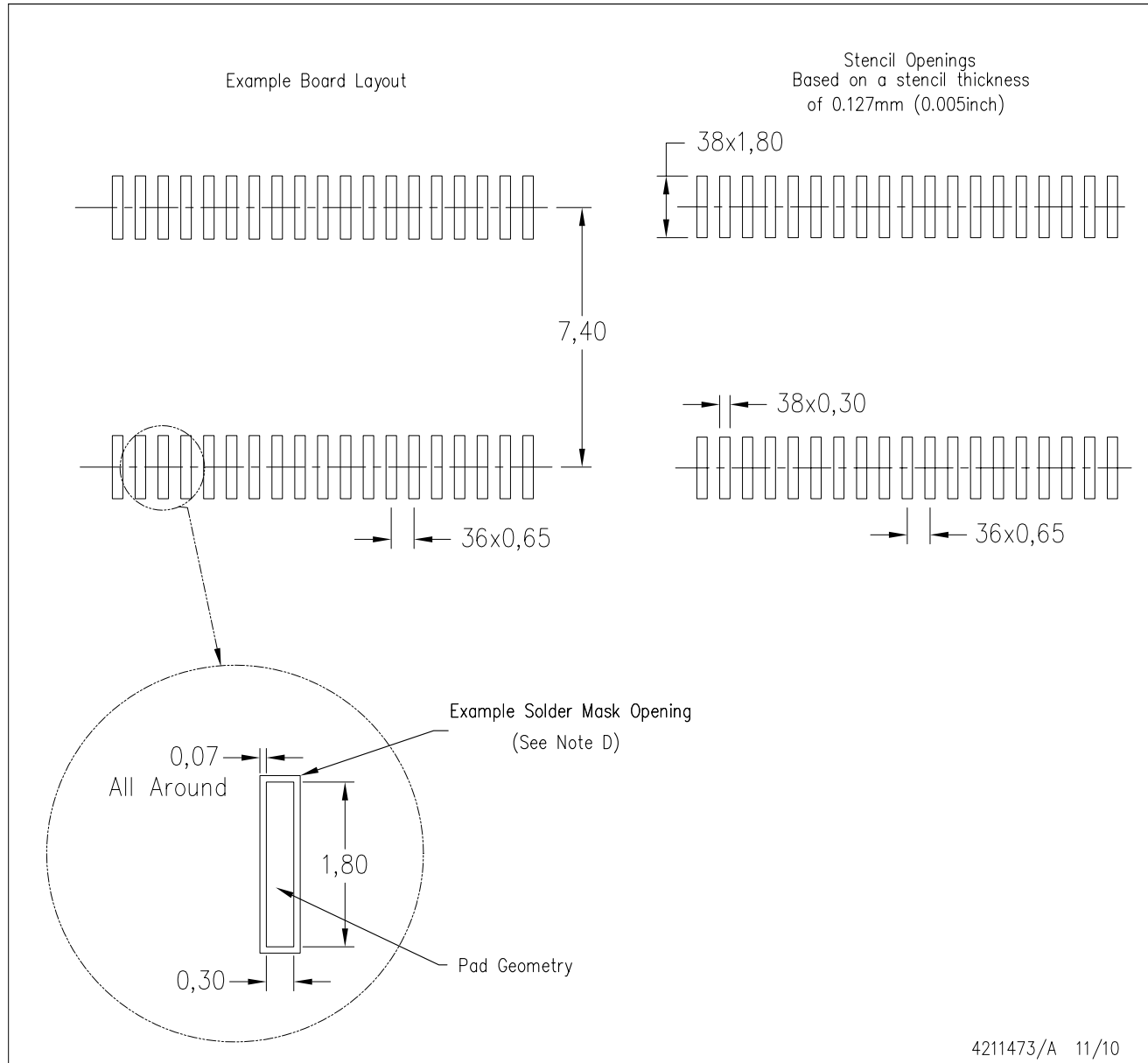
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-153, except 30 pin body length.

DA (R-PDSO-G38)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - D. Contact the board fabrication site for recommended soldermask tolerances.

## GENERIC PACKAGE VIEW

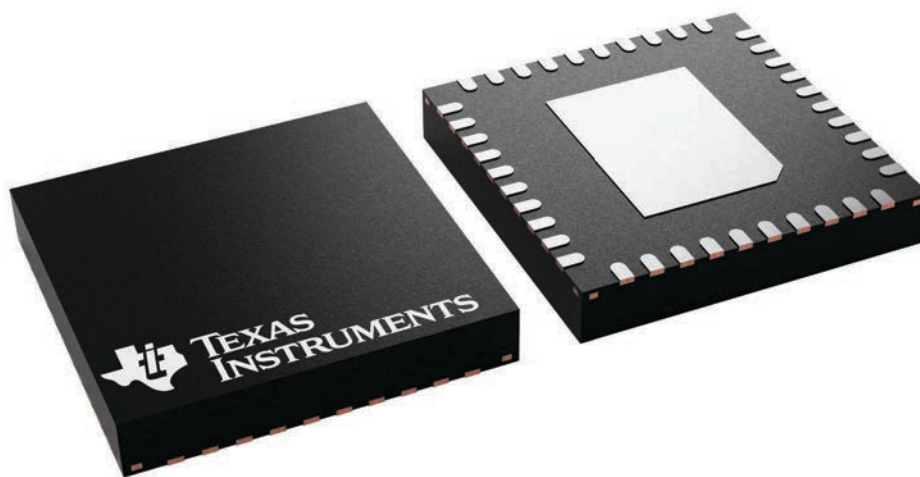
**RHA 40**

**VQFN - 1 mm max height**

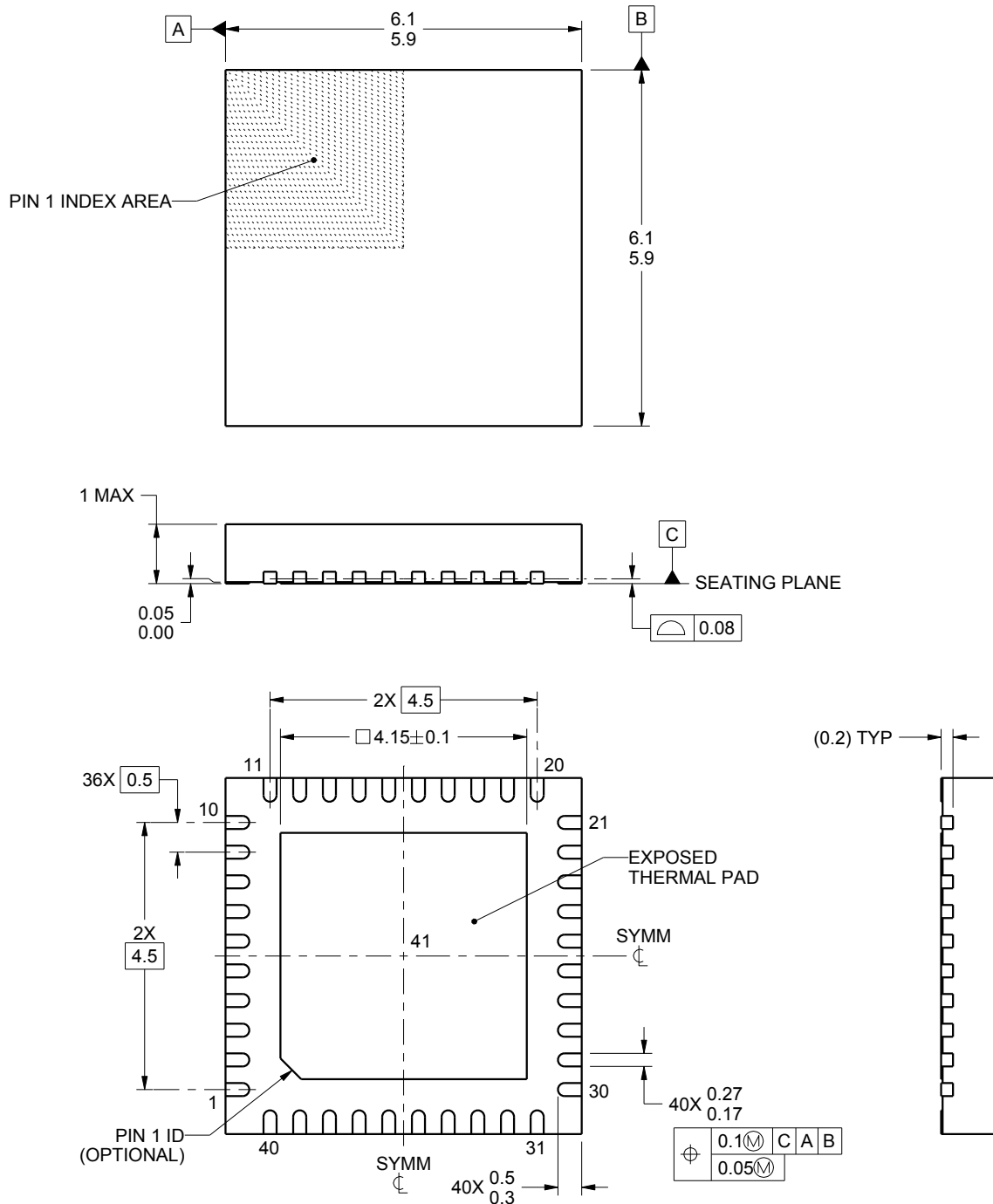
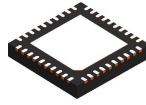
6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225870/A



4219052/A 06/2016

## NOTES:

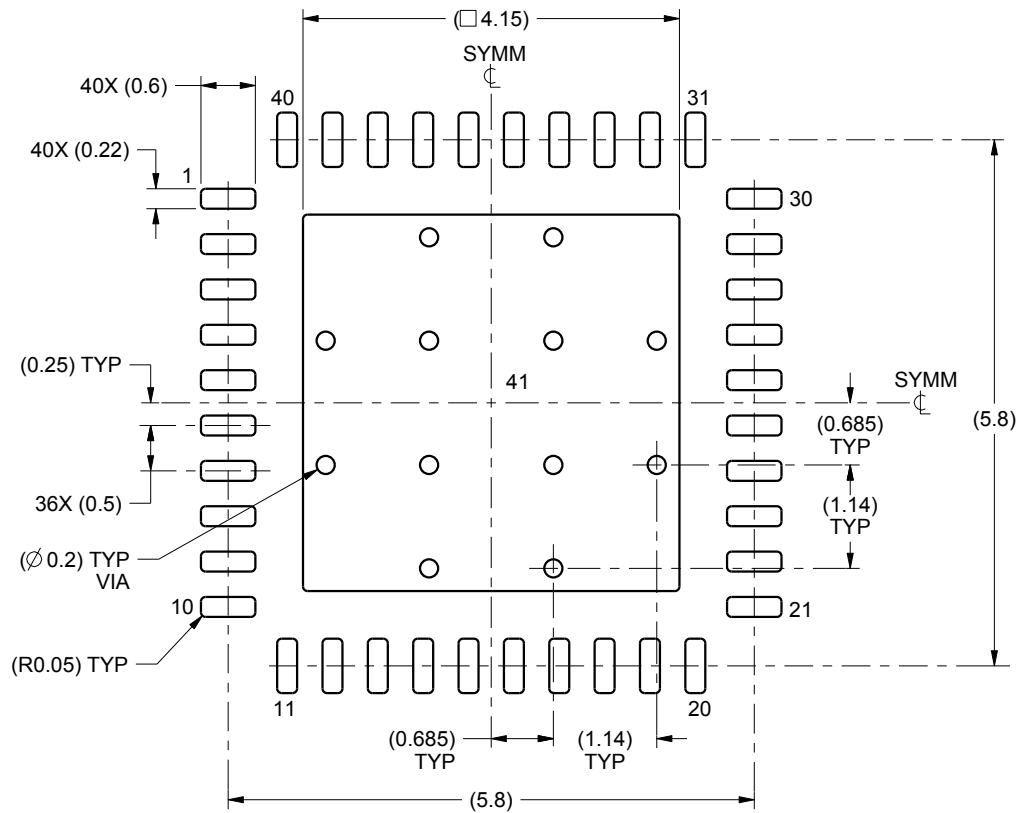
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

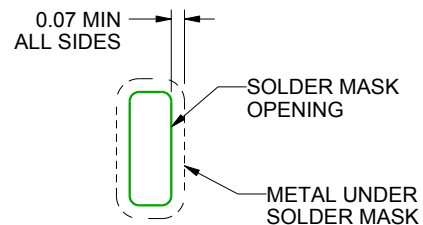
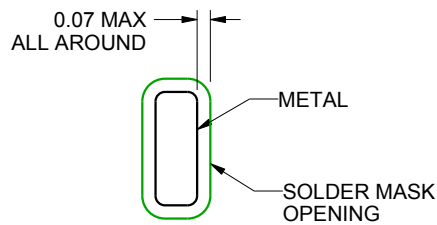
RHA0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:12X



SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

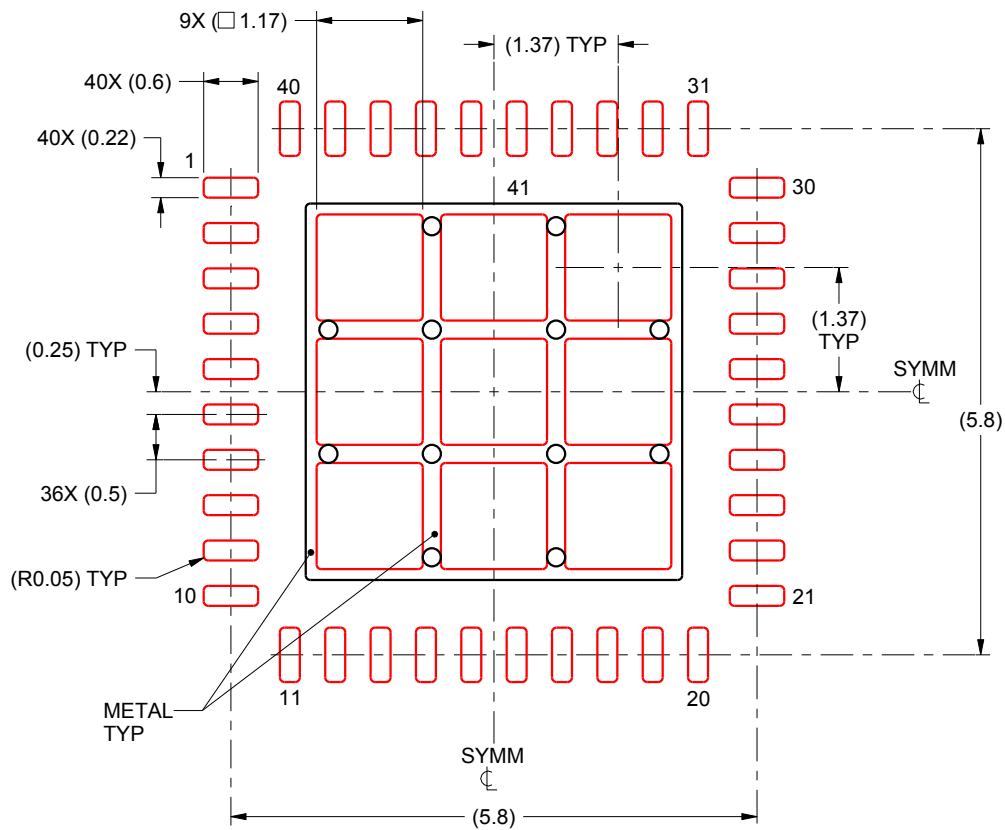
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

RHA0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:  
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:12X

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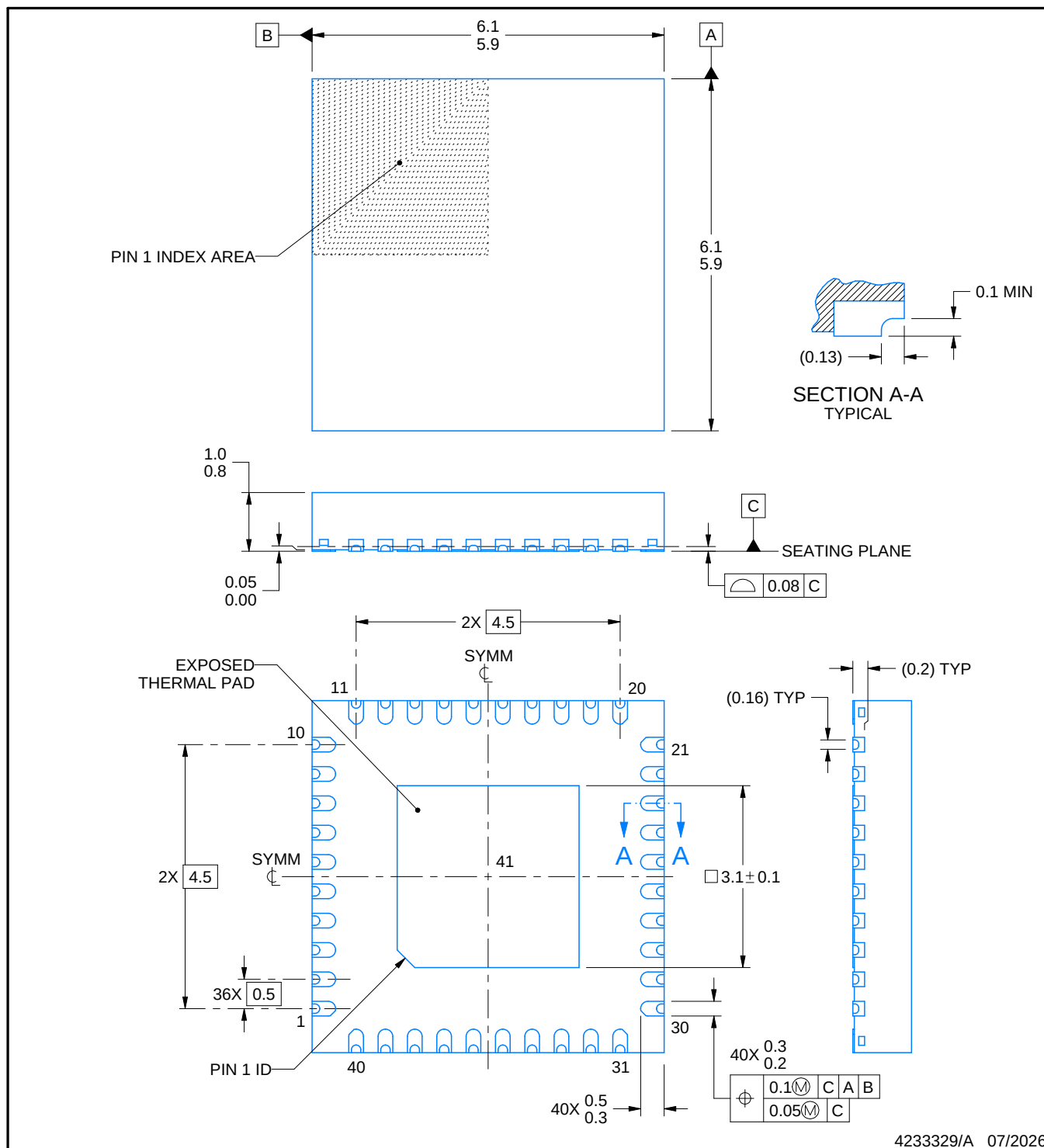
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



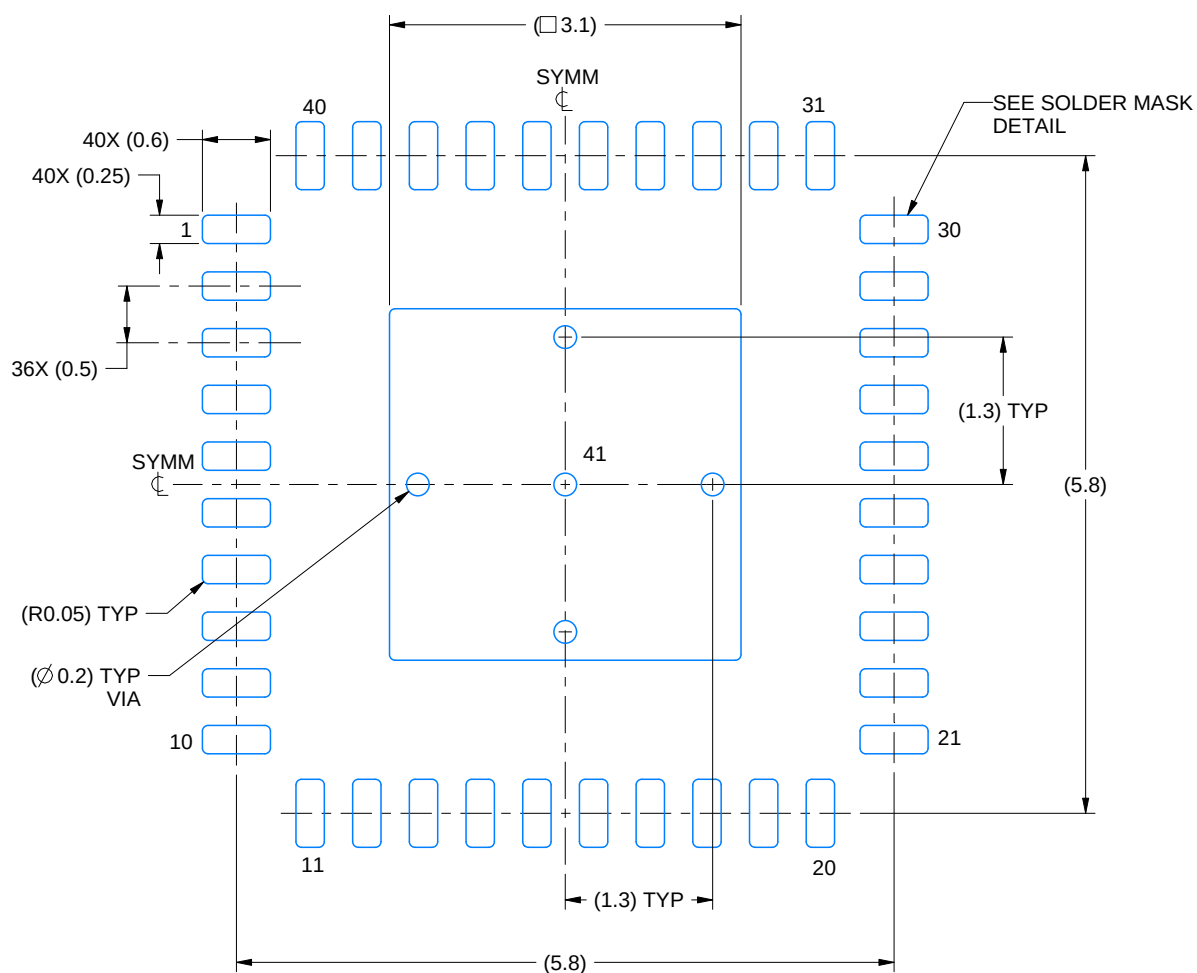
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**RHA0040Y**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4233329/A 07/2026

NOTES: (continued)

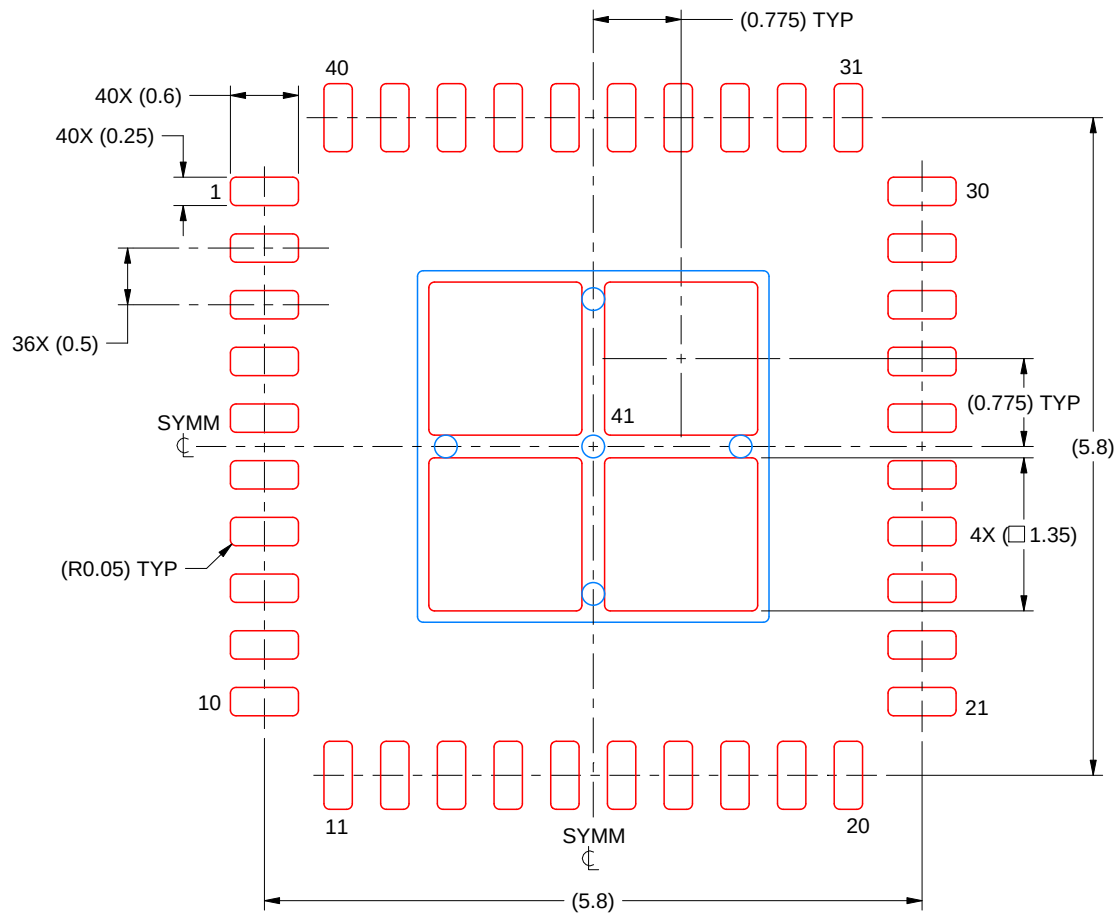
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHA0040Y

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



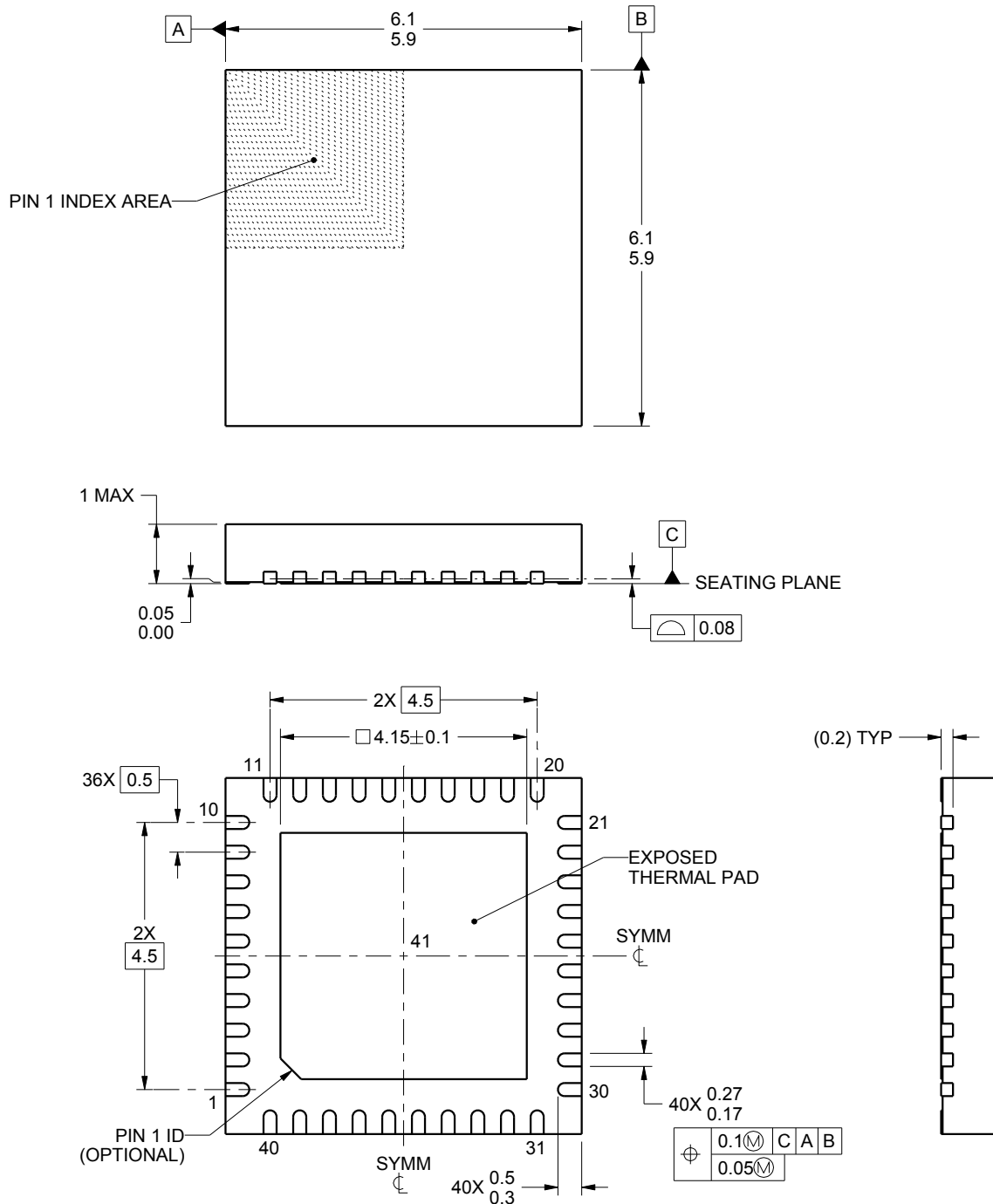
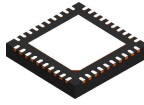
SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 15X

EXPOSED PAD 41  
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4233329/A 07/2026

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4219052/A 06/2016

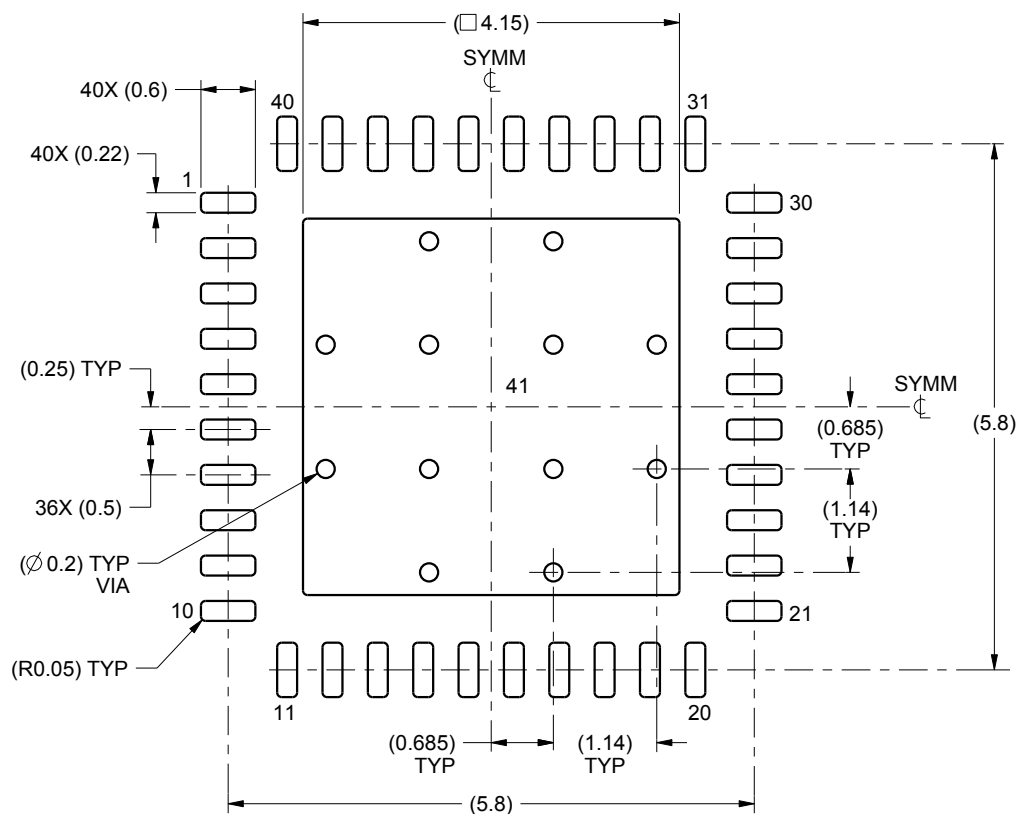
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

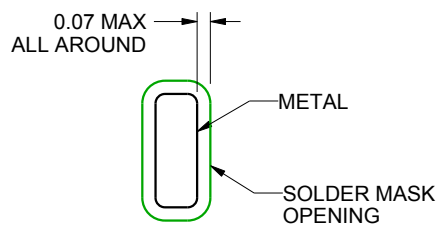
**RHA0040B**

### VQFN - 1 mm max height

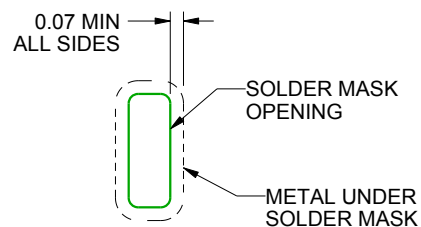
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:12X



NON SOLDER MASK  
DEFINED  
(PREFERRED)



SOLDER MASK  
DEFINED

## SOLDER MASK DETAILS

4219052/A 06/2016

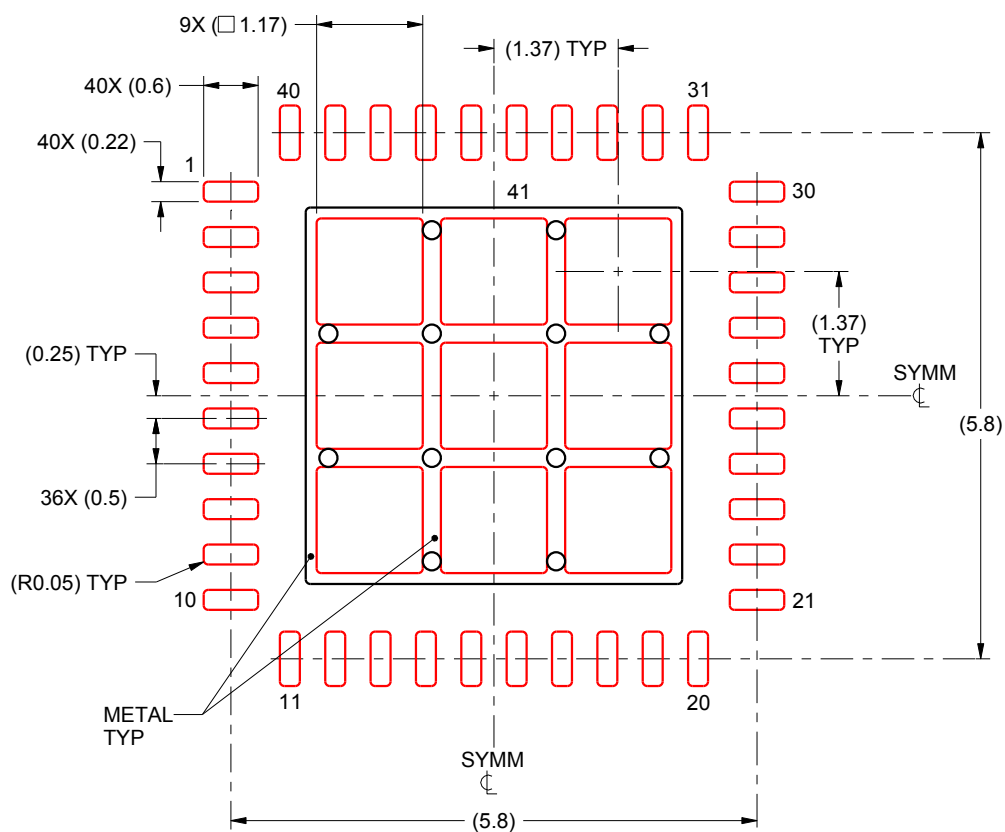
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

**RHA0040B**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:  
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025