MSPM0H321x Mixed-Signal Microcontrollers

1 Features

- Core
  - Arm® 32-bit Cortex®-M0+ CPU, frequency up to 32MHz
- Operating characteristics
  - Extended temperature: –40°C to 125°C
  - Supply voltage range: 4.5V to 5.5V
- Memories
  - Up to 64KB of flash
  - 8KB of SRAM
- High-performance analog peripherals
  - One analog-to-digital converter (ADC) with up to 27 total external channels, 1.6-Msps@12-bit
  - 4.05V internal ADC voltage reference (VREF)
  - Integrated temperature sensor
  - Integrated supply monitor
- Optimized low-power modes
  - RUN: 126µA/MHz (CoreMark)
  - SLEEP: 2516uA at 32MHz
  - STOP: 1442µA at 4MHz and 674uA at 32kHz
  - STANDBY: 3.8µA with SRAM retention
- Intelligent digital peripherals
  - 3-channel DMA controller
  - Five timers supporting up to 18 PWM channels
    - One 16-bit advanced timers with deadband support up to 8 PWM channels
    - One 16-bit general purpose timer with 4 capture/compares
    - Two 16-bit general purpose timers with 2 capture/compares
    - One 16-bit general purpose timer with 2 capture/compares and QEI
  - Windowed watchdog timer (WWDT)
  - Independent watch dog timer (IWDT)
  - RTC with alarm and calendar mode
  - BEEPER generating 1/2/4/8kHz square wave to drive an external beeper
- Enhanced communication interfaces
  - Three UART interfaces supporting low-power operation in STANDBY mode
    - One advanced UART instance supporting LIN, IrDA, DALI, Smart Card, & Manchester coding
  - Two I^2C interfaces supporting FM+ (1Mbit/s), SMBus/PMBus, and wakeup from STOP mode,
  - One SPI supporting up to 16Mbit/s
- Clock system
  - Internal 32MHz oscillator with -2.1% to 1.6% accuracy (SYSOSC)
  - Internal 32kHz low-frequency oscillator (LFOSC) with up to ±3% accuracy
  - External 4MHz to 32MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator (LFXT)
  - External Low Frequency (LF) and High Frequency (HF) digital clock inputs
- Data integrity
  - Flexible firewalls for protecting code and data
  - Cyclic redundancy checker (CRC-16)
- Flexible I/O features
  - Up to 45 GPIOs
  - True 5V IOs
- Development support
  - 2-pin serial wire debug (SWD)
- Package options
  - 48-pin LQFP (PT), VQFN (RGZ)
  - 32-pin VQFN (RHB)
  - 28-pin VSSOP (DGS28)
  - 24-pin VQFN (RGE)
  - 20-pin VSSOP (DGS20), WQFN (RUK)
- Family members (also see *Device Comparison*)
  - MSPM0H3216: 64KB of flash, 8KB of RAM
  - MSPM0H3215: 32KB of flash, 8KB of RAM
- Development kits and software (also see *Tools and Software*)
  - LP-MSPM0H3216 LaunchPad™ development kit
  - MSP Software Development Kit (SDK)

2 Applications

- Appliances
- Battery charging and management
- Power supplies and power delivery
- Personal electronics
- Building security and fire safety
- Connected peripherals and printers
- Factory Automation Control
- Smart metering
- Communication modules
- Medical and healthcare
- Lighting

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

3 Description

MSPM0H321x microcontrollers (MCUs) are part of the MSP highly-integrated 5V power supply and 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ core platform operating at up to 32MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 4.5V.

The MSPM0H321x devices provide up to 64KB embedded flash program memory with 8KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy of -2.1% to 1.6%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.6Msps ADC with VDD as the voltage reference, and an on-chip temperature sensor. These devices offer intelligent digital peripherals such as one 16-bit advanced timer, four 16-bit general purpose timer, one windowed watchdog timer, one independent watchdog timer, and a real-time clock (RTC). These devices also offer a variety of communication peripherals including three UART, one SPI, and two I^2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration enabling customers to find the MCU that meets their project needs. The architecture combined with extensive low-power modes is optimized to achieve extended battery life in portable measurement applications.

MSPM0H321x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad™ kit available for purchase and design files for a target-socket board. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0H-Series 32MHz Microcontrollers Technical Reference Manual*.

Table 3-1. Package Information

PART NUMBER (1) (3)	PACKAGE	PACKAGE SIZE(2)
MSPM0H3216SPTR	PT (LQFP, 48)	9mm × 9mm
MSPM0H3215SPTR	PT (LQFP, 48)	9mm × 9mm
MSPM0H3216SRGZR	RGZ (VQFN, 48)	7mm × 7mm
MSPM0H3215SRGZR	RGZ (VQFN, 48)	7mm × 7mm
MSPM0H3216SRHBR	RHB (VQFN, 32)	5mm × 5mm
MSPM0H3215SRHBR	RHB (VQFN, 32)	5mm x 5mm
MSPM0H3216SDGS28R	DGS28 (VSSOP, 28)	7.1mm × 4.9mm
MSPM0H3215SDGS28R	DGS28 (VSSOP, 28)	7.1mm × 4.9mm
MSPM0H3216SRGER	RGE (VQFN, 24)	4mm x 4mm
MSPM0H3215SRGER	RGE (VQFN, 24)	4mm x 4mm
MSPM0H3216SDGS20R	DGS20 (VSSOP, 20)	5.1mm × 4.9mm
MSPM0H3215SDGS20R	DGS20 (VSSOP, 20)	5.1mm × 4.9mm
MSPM0H3216SRUKR	RUK (WQFN, 20)	3mm x 3mm
MSPM0H3215SRUKR	RUK (WQFN, 20)	3mm x 3mm

1. For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI web site.
2. The package size (length × width) is a nominal value and includes pins, where applicable. For package dimensions with tolerances, see the *Mechanical Data* in Section 12.

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3. For more information about the device name, see Section 10.1.

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4 Functional Block Diagram

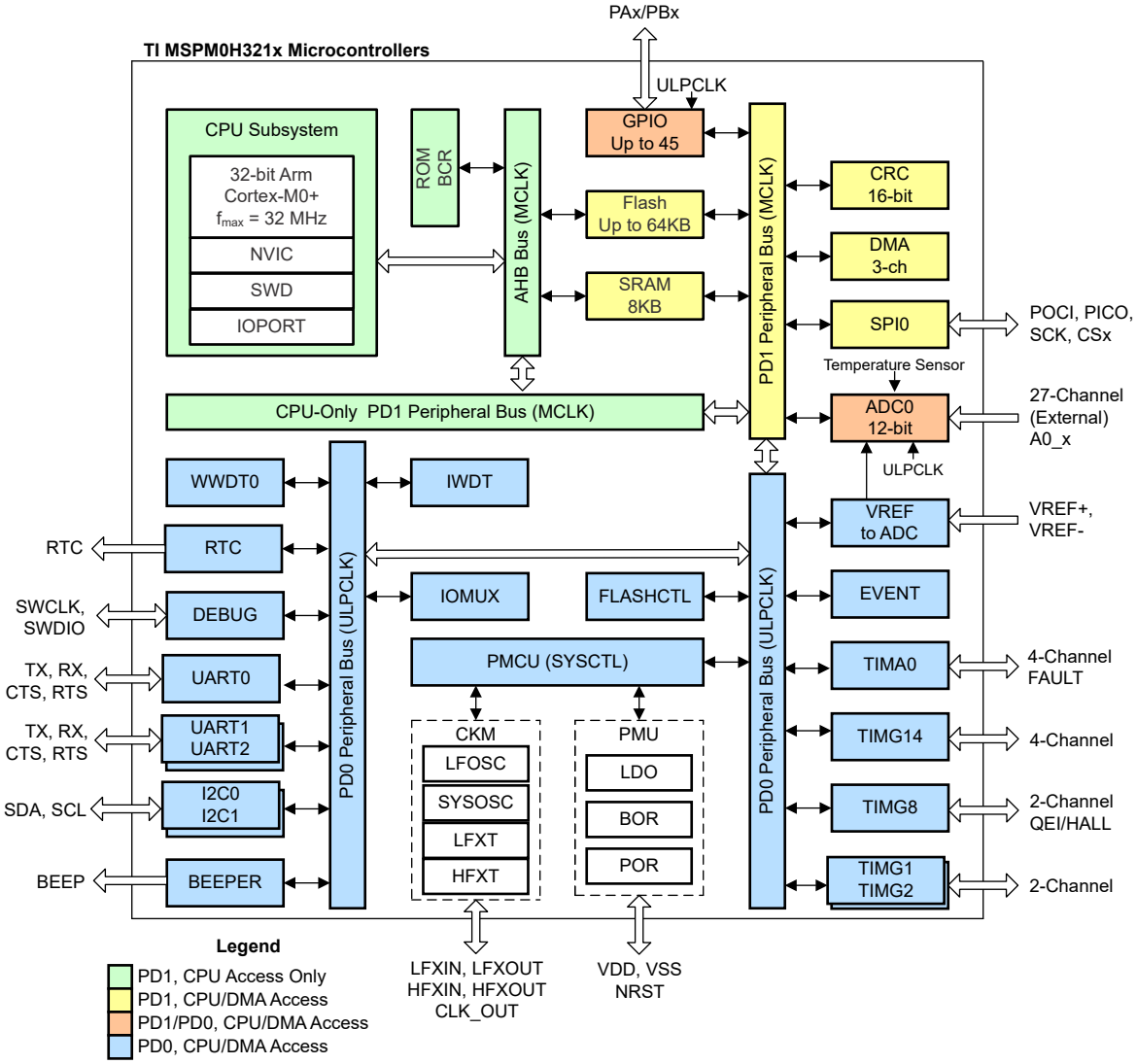

Figure 4-1. MSPM0H321x Functional Block Diagram

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Table of Contents

1 Features....1
2 Applications....1
3 Description....2
4 Functional Block Diagram....4
5 Device Comparison....6
6 Pin Configuration and Functions....7
6.1 Pin Diagrams....7
6.2 Pin Attributes....11
6.3 Signal Descriptions....24
6.4 Connections for Unused Pins....31
7 Specifications....33
7.1 Absolute Maximum Ratings....33
7.2 ESD Ratings....33
7.3 Recommended Operating Conditions....33
7.4 Thermal Information....34
7.5 Supply Current Characteristics....35
7.6 Power Supply Sequencing....35
7.7 Flash Memory Characteristics....36
7.8 Timing Characteristics....37
7.9 Clock Specifications....38
7.10 Digital IO....40
7.11 ADC....40
7.12 Temperature Sensor....42
7.13 VREF....43
7.14 I2C....43
7.15 SPI....44
7.16 UART....46
7.17 TIMx....46
7.18 Emulation and Debug....46
8 Detailed Description....47
8.1 Overview....48
8.2 CPU....48
8.3 Operating Modes....48
8.4 Power Management Unit (PMU)....50
8.5 Clock Module (CKM)....50
8.6 DMA_B....51
8.7 Events....52
8.8 Memory....52
8.9 Flash Memory....55
8.10 SRAM....55
8.11 GPIO....56
8.12 IOMUX....56
8.13 ADC....56
8.14 Temperature Sensor....57
8.15 VREF....57
8.16 Security....58
8.17 CRC....58
8.18 UART....58
8.19 SPI....59
8.20 I2C....59
8.21 Low-Frequency Sub System (LFSS)....59
8.22 RTC_B....60
8.23 IWDT_B....61
8.24 WWDT....61
8.25 Timers (TIMx)....61
8.26 Device Analog Connections....63
8.27 Input/Output Diagrams....64
8.28 Serial Wire Debug Interface....64
8.29 DEBUGSS....65
8.30 Device Factory Constants....65
8.31 Identification....66
9 Applications, Implementation, and Layout....67
9.1 Typical Application....67
10 Device and Documentation Support....68
10.1 Device Nomenclature....68
10.2 Tools and Software....69
10.3 Documentation Support....69
10.4 Support Resources....70
10.5 Trademarks....70
10.6 Electrostatic Discharge Caution....70
10.7 Glossary....70
11 Revision History....70
12 Mechanical, Packaging, and Orderable Information....71

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5 Device Comparison

Table 5-1. Device Comparison

DEVICE NAME (1) (3)	FLASH / SRAM (KB)	ADC CHANNELS	UART / I2C / SPI	TIMG	TIMA	GPIOs	PACKAGE (PACKAGE SIZE)(2)
MSPM0H3216SPTR	64 / 8	27	3 / 2 / 1	4	1	45	48 LQFP (9mm × 9mm)
MSPM0H3215SPTR	32 / 8						
MSPM0H3216SRGZR	64 / 8	27	3 / 2 / 1	4	1	45	48 VQFN (7mm × 7mm)
MSPM0H3215SRGZR	32 / 8						
MSPM0H3216SRHBR	64 / 8	18	3 / 2 / 1	4	1	29	32 VQFN (5mm × 5mm)
MSPM0H3215SRHBR	32 / 8						
MSPM0H3216SDGS28R	64 / 8	15	3 / 2 / 1	4	1	25	28 VSSOP (7.1mm × 4.9mm)
MSPM0H3215SDGS28R	32 / 8						
MSPM0H3216SRGER	64 / 8	13	3 / 2 / 1	4	1	21	24 VQFN (4mm × 4mm)
MSPM0H3215SRGER	32 / 8						
MSPM0H3216SDGS20R	64 / 8	12	3 / 2 / 1	4	1	17	20 VSSOP (5.1mm × 4.9mm)
MSPM0H3215SDGS20R	32 / 8						
MSPM0H3216SRUKR	64 / 8	12	3 / 2 / 1	4	1	17	20 WQFN (3mm × 3mm)
MSPM0H3215SRUKR	32 / 8						

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI web site.
(2) The package size (length × width) is a nominal value and includes pins, where applicable. For package dimensions with tolerances, see the *Mechanical Data* in Section 12.
(3) For more information about the device name, see Section 10.1.

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6 Pin Configuration and Functions

6.1 Pin Diagrams

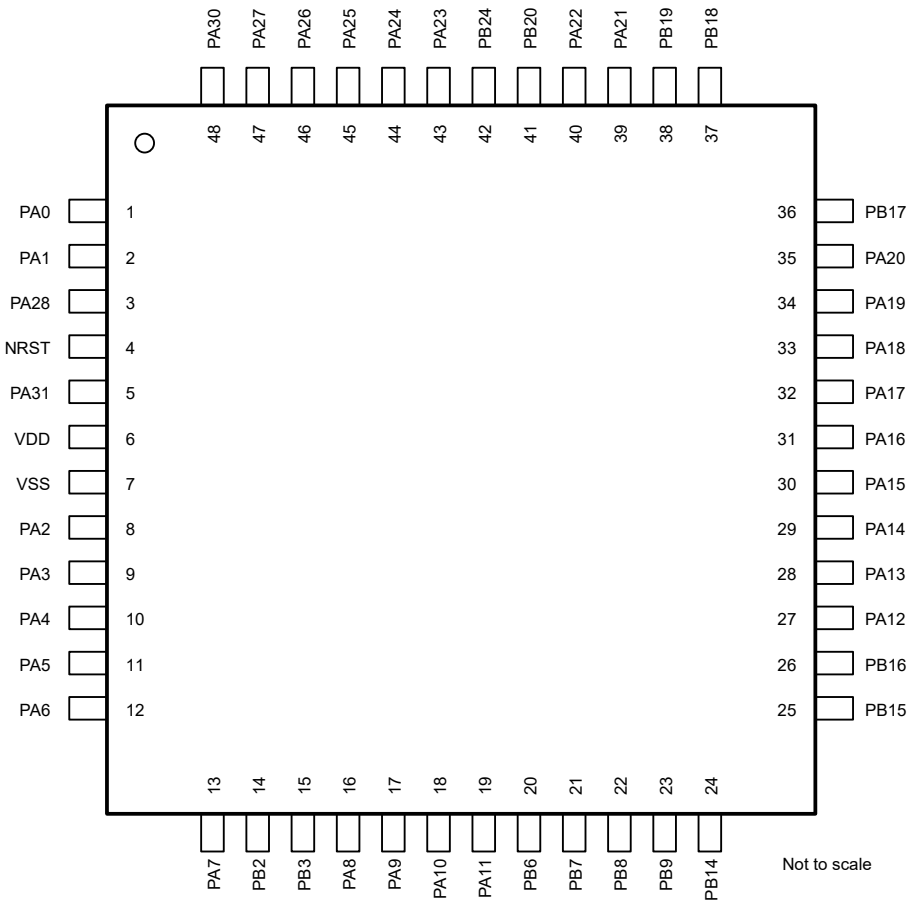

Figure 6-1. 48-Pin PT (LQFP) (Top View)

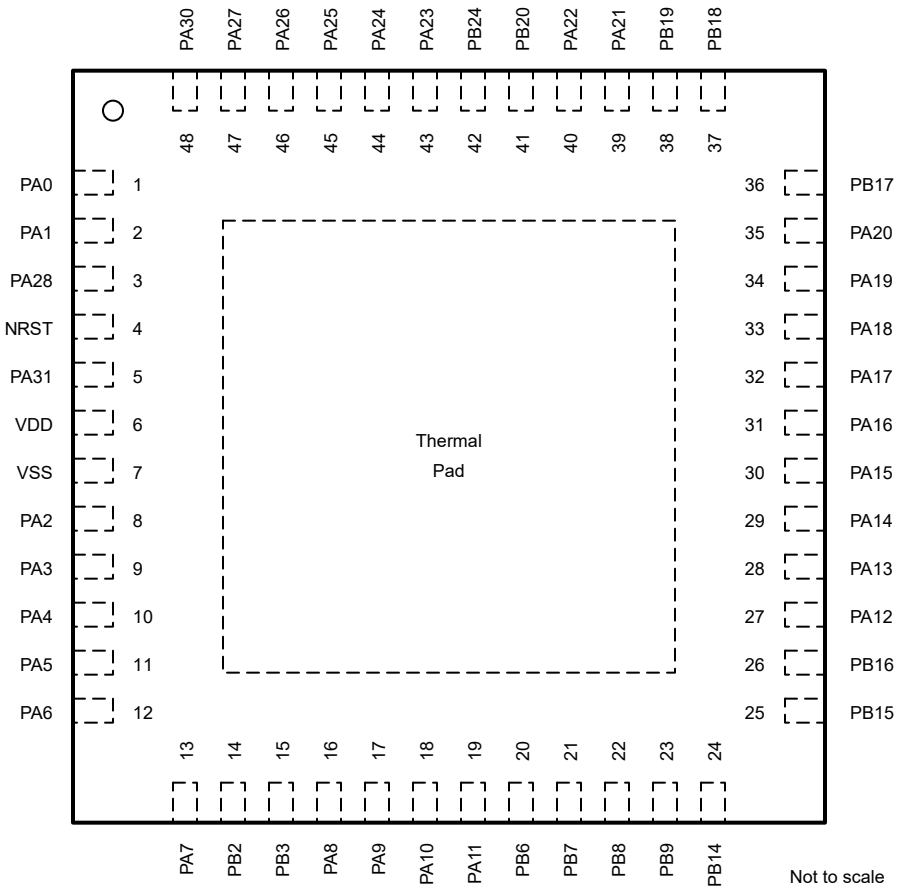

Figure 6-2. 48-Pin RGZ (VQFN) (Top View)

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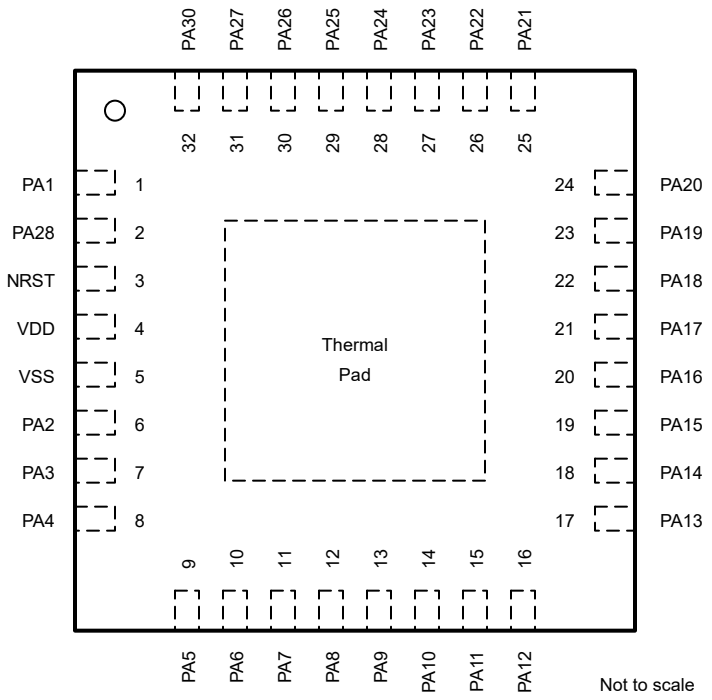

Figure 6-3. 32-Pin RHB (VQFN) (Top View)

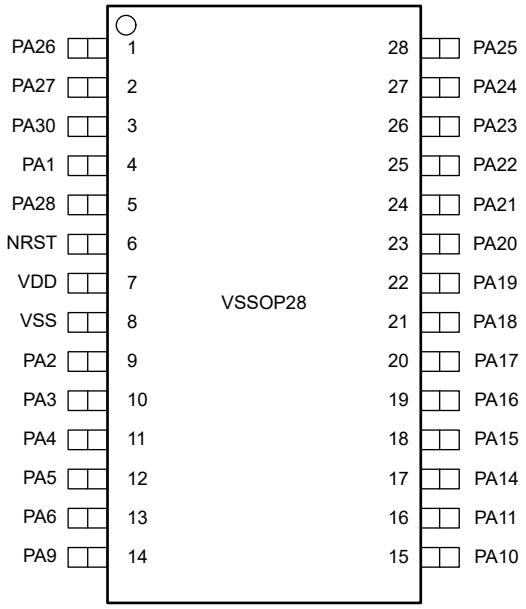

Figure 6-4. 28-Pin DGS28 (VSSOP) (Top View)

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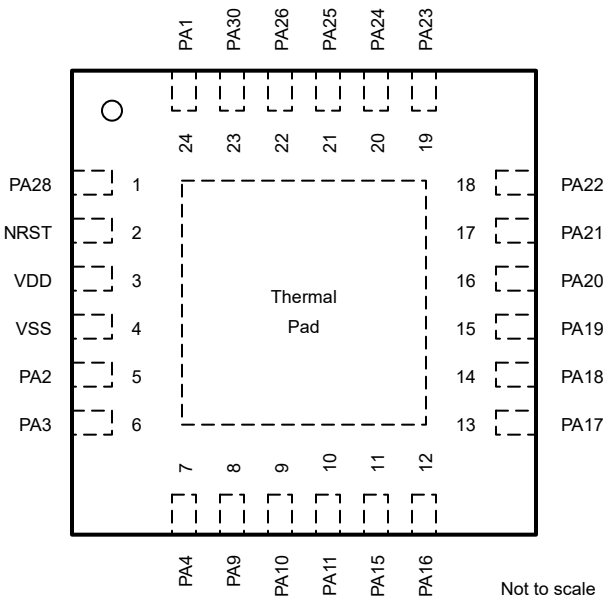

Figure 6-5. 24-Pin RGE (VQFN) (Top View)

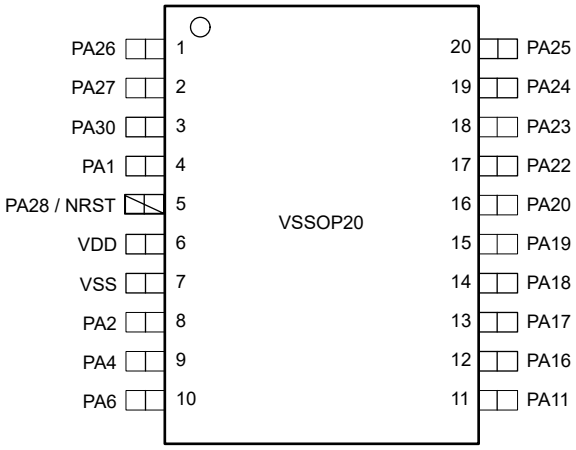

Figure 6-6. 20-Pin DGS20 (VSSOP) (Top View)

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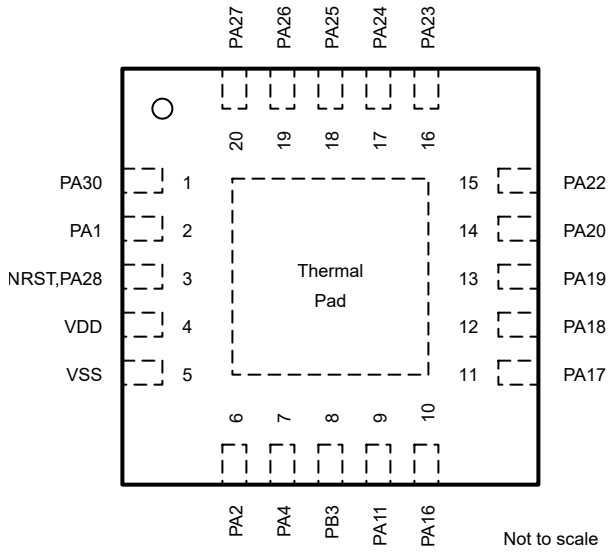

Figure 6-7. 20-Pin RUK (WQFN) (Top View)

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
SDIO (standard drive)	Y			Y		
HSIO (High speed)	Y	Y		Y		

Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
4	3	4	3	6	2	5	NRST	NRST	(Non-IOMUX 1) 0	RESET	RESET

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
1		1					PA0 PINCM1 0x40428000	PA0	1	IO	SDIO (standard)
								UART0_TX	2	O	
								I2C0_SDA	3	IOD	
								TIMA0_C0	4	IO	
								TIMA_FAL1	5	I	
								FCC_IN	6	I	
								TIMG8_C1	7	IO	
								BEEP	8	O	
								TIMG14_C0	9	IO	
								SPI0_CS1_MISO1	10	IO	
								RTC_OUT	12	O	
2	2	2	1	4	24	4	PA1 PINCM2 0x40428004	PA1	1	IO	SDIO (standard)
								UART0_RX	2	IO	
								I2C0_SCL	3	IOD	
								TIMA0_C1	4	IO	
								TIMA_FAL2	5	I	
								TIMG8_IDX	6	I	
								TIMG8_C0	7	IO	
								TIMG14_C1	9	IO	
								SPI0_CS3_CD_MISO3	10	IO	
								HFCLKIN	11	I	
								UART0_TX	12	O	
								UART1_RTS	13	O	
								I2C0_SDA	14	IOD	
								HFXOUT	(Non-IOMUX 1) 0	A	
8	6	8	6	9	5	8	PA2 PINCM5 0x40428010	PA2	1	IO	HSIO (high-speed)
								TIMG8_C1	2	IO	
								SPI0_CS0	3	IO	
								TIMG2_C1	4	IO	
								TIMG8_IDX	5	I	
								TIMA0_C3N	6	O	
								TIMA0_C2N	7	O	
								TIMA_FAL0	8	I	
								TIMA_FAL1	9	I	
								TIMA0_C0	11	IO	
								I2C0_SCL	12	IOD	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
9		9	7	10	6		PA3 PINCM6 0x40428014	PA3	1	IO	HSIO (high-speed)
								TIMG8_C0	2	IO	
								SPI0_CS1_MISO1	3	IO	
								I2C1_SDA	4	IOD	
								TIMA0_C1	5	IO	
								TIMG2_C0	7	IO	
								TIMA0_C2	8	IO	
								UART2_CTS	9	I	
								UART1_TX	10	O	
								SPI0_CS3_CD_MISO3	11	IO	
								I2C0_SDA	12	IOD	
								LFXIN 1	(Non-IOMUX 1) 0	A	
10	7	10	8	11	7	9	PA4 PINCM7 0x40428018	PA4	1	IO	HSIO (high-speed)
								TIMG8_C1	2	IO	
								SPI0_POCI	3	IO	
								I2C1_SCL	4	IOD	
								TIMA0_C1N	5	O	
								TIMG2_C1	7	IO	
								TIMA0_C3	8	IO	
								UART2_RTS	9	O	
								UART1_RX	10	I	
								SPI0_CS0	11	IO	
								TIMA0_C0N	12	O	
								HFCLKIN	13	I	
								LFXOUT 1	(Non-IOMUX 1) 0	A	
11		11	9	12			PA5 PINCM8 0x4042801c	PA5	1	IO	HSIO (high-speed)
								TIMG8_C0	2	IO	
								SPI0_PICO	3	IO	
								I2C1_SDA	4	IOD	
								TIMG14_C0	5	IO	
								FCC_IN	6	I	
								TIMG1_C0	7	IO	
								TIMA_FAL1	8	I	
								UART0_CTS	9	I	
								UART1_TX	11	O	
								TIMA0_C1	12	IO	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
12		12	10	13		10	PA6 PINCM9 0x40428020	PA6	1	IO	HSIO (high-speed)
								TIMG8_C1	2	IO	
								SPI0_SCLK	3	IOD	
								I2C1_SCL	4	IOD	
								TIMG14_C1	5	IO	
								HFCLKIN	6	I	
								TIMG1_C1	7	IO	
								TIMA_FAL0	8	I	
								UART0_RTS	9	O	
								TIMA0_C2N	10	O	
								UART1_RX	11	I	
								TIMA0_C2	12	IO	
								I2C0_SDA	13	IOD	
								BEEP	14	O	
13		13	11				PA7 PINCM10 0x40428024	PA7	1	IO	HSIO (high-speed)
								CLK_OUT	2	O	
								TIMG8_C0	3	IO	
								TIMA0_C2	4	IO	
								TIMG8_IDX	5	I	
								TIMG2_C1	6	IO	
								TIMA0_C1	7	IO	
								SPI0_CS2_MISO2	8	IO	
								FCC_IN	9	I	
								SPI0_POCI	10	IO	
								SPI0_PICO	11	IO	
								UART1_TX	12	O	
								TIMG1_C0	13	IO	
16		16	12				PA8 PINCM13 0x40428030	PA8	1	IO	HSIO (high-speed)
								UART1_TX	2	O	
								SPI0_CS0	3	IO	
								I2C0_SDA	4	IOD	
								TIMA0_C0	5	IO	
								TIMA_FAL2	6	I	
								TIMA_FAL0	7	I	
								SPI0_CS3_CD_MISO3	8	IO	
								TIMG2_C1	9	IO	
								HFCLKIN	10	I	
								UART0_RTS	11	O	
								SPI0_SCLK	12	IOD	
								UART1_RX	13	I	
								TIMA0_C3N	14	O	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
17		17	13	14	8		PA9 PINCM14 0x40428034	PA9	1	IO	HSIO (high-speed)
								UART1_RX	2	I	
								SPI0_PICO	3	IO	
								I2C0_SCL	4	IOD	
								TIMA0_C0N	5	O	
								CLK_OUT	6	O	
								TIMA0_C1	7	IO	
								RTC_OUT	8	O	
								TIMG2_C0	9	IO	
								SPI0_POCI	10	IO	
								UART0_CTS	11	I	
								TIMA_FAL1	12	I	
								TIMG1_C1	13	IO	
18		18	14	15	9		PA10 PINCM15 0x40428038	PA10	1	IO	SDIO (standard)
								UART0_TX	2	O	
								SPI0_POCI	3	IO	
								I2C0_SDA	4	IOD	
								TIMA0_C2	5	IO	
								CLK_OUT	6	O	
								TIMG14_C0	7	IO	
								I2C1_SDA	8	IOD	
								TIMA_FAL1	10	I	
								TIMA0_C1N	12	O	
								TIMG8_C1	13	IO	
								SPI0_PICO	14	IO	
19	9	19	15	16	10	11	PA11 PINCM16 0x4042803c	PA11	1	IO	HSIO (high-speed)
								UART0_RX	2	IO	
								SPI0_SCLK	3	IOD	
								I2C0_SCL	4	IOD	
								TIMA0_C2N	5	O	
								UART1_RX	6	I	
								TIMG14_C1	7	IO	
								I2C1_SCL	8	IOD	
								TIMA_FAL0	10	I	
								SPI0_CS0	12	IO	
								BSL_invoke	13	I	
								ADC0_25	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
27		27	16				PA12 PINCM24 0x4042805c	PA12	1	IO	SDIO (standard)
								SPI0_SCLK	2	IOD	
								TIMA0_C3	4	IO	
								FCC_IN	5	I	
								TIMG14_C0	6	IO	
								SPI0_CS1_MISO1	8	IO	
								UART2_CTS	9	I	
								UART1_CTS	10	I	
								TIMA0_C3N	11	O	
								I2C1_SCL	12	IOD	
								TIMG2_C1	13	IO	
								ADC0_18	(Non-IOMUX 1) 0	A	
28		28	17				PA13 PINCM25 0x40428060	PA13	1	IO	SDIO (standard)
								SPI0_POCI	3	IO	
								TIMA0_C2N	4	O	
								TIMA0_C3N	5	O	
								RTC_OUT	6	O	
								TIMG14_C1	7	IO	
								TIMG14_C3	8	IO	
								SPI0_CS3_CD_MISO3	9	IO	
								UART2_TX	10	O	
								UART1_RTS	11	O	
								SPI0_CS0	12	IO	
								TIMG8_C1	13	IO	
								TIMA0_C1	14	IO	
								ADC0_17	(Non-IOMUX 1) 0	A	
29		29	18	17			PA14 PINCM26 0x40428064	PA14	1	IO	SDIO (standard)
								UART0_CTS	2	I	
								SPI0_PICO	3	IO	
								TIMG1_C0	4	IO	
								CLK_OUT	6	O	
								SPI0_CS2_MISO2	9	IO	
								UART2_RX	10	I	
								I2C0_SCL	12	IOD	
								UART0_TX	13	O	
								TIMA0_C2	14	IO	
								ADC0_16	(Non-IOMUX 1) 0	A	
30		30	19	18	11		PA15 PINCM27 0x40428068	PA15	1	IO	SDIO (standard)
								UART0_RTS	2	O	
								SPI0_CS2_MISO2	3	IO	
								I2C1_SCL	4	IOD	
								TIMA0_C2	5	IO	
								TIMG8_IDX	7	I	
								UART2_RTS	10	O	
								ADC0_15	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
31	10	31	20	19	12	12	PA16 PINCM28 0x4042806c	PA16	1	IO	SDIO (standard)
								SPI0_POCI	3	IO	
								I2C1_SDA	4	IOD	
								TIMA0_C2N	5	O	
								FCC_IN	7	I	
								UART2_CTS	10	I	
								TIMG14_C2	12	IO	
								ADC0_14	(Non-IOMUX 1) 0	A	
32	11	32	21	20	13	13	PA17 PINCM29 0x40428070	PA17	1	IO	HSIO (high-speed)
								UART1_TX	2	O	
								TIMA0_C2	3	IO	
								I2C1_SCL	4	IOD	
								TIMA0_C3	5	IO	
								TIMG2_C0	6	IO	
								TIMG8_C0	7	IO	
								TIMA0_C0N	8	O	
								SPI0_CS1_MISO1	9	IO	
								SPI0_SCLK	10	IOD	
								UART0_RX	12	IO	
								ADC0_13	(Non-IOMUX 1) 0	A	
33	12	33	22	21	14	14	PA18 PINCM30 0x40428074	PA18	1	IO	SDIO (standard)
								UART1_RX	2	I	
								UART1_RTS	3	O	
								I2C1_SDA	4	IOD	
								TIMA0_C3N	5	O	
								TIMG2_C1	6	IO	
								TIMG8_C1	7	IO	
								SPI0_PICO	8	IO	
								SPI0_CS0	9	IO	
								UART0_CTS	10	I	
								TIMA0_C0	11	IO	
								SPI0_POCI	12	IO	
								TIMA_FAL2	13	I	
								CLK_OUT	14	O	
								ADC0_12	(Non-IOMUX 1) 0	A	
34	13	34	23	22	15	15	PA19 PINCM31 0x40428078	PA19	1	IO	HSIO (high-speed)
								SWDIO	2	IO	
								SPI0_SCLK	3	IOD	
								I2C1_SDA	4	IOD	
								TIMA0_C2	5	IO	
								TIMG14_C0	6	IO	
								SPI0_POCI	7	IO	
								UART0_CTS	8	I	
								UART0_RTS	12	O	
								SPI0_PICO	13	IO	
								ADC0_22	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
35	14	35	24	23	16	16	PA20 PINCM32 0x4042807c	PA20	1	IO	HSIO (high-speed)
								SWCLK	2	I	
								TIMA_FAL1	3	I	
								I2C1_SCL	4	IOD	
								TIMA0_C2N	5	O	
								TIMG14_C1	6	IO	
								SPI0_PICO	7	IO	
								TIMA0_C0	8	IO	
								UART0_RTS	9	O	
								UART1_RX	13	I	
								ADC0_4	(Non-IOMUX 1) 0	A	
39		39	25	24	17		PA21 PINCM36 0x4042808c	PA21	1	IO	SDIO (standard)
								UART2_TX	2	O	
								SPI0_CS3_CD_MISO3	3	IO	
								UART1_CTS	4	I	
								TIMA0_C0	5	IO	
								TIMG1_C0	6	IO	
								UART2_CTS	8	I	
								TIMG8_C0	10	IO	
								TIMA0_C0N	12	O	
								UART2_RX	13	I	
								ADC0_8	(Non-IOMUX 1) 0	A	
40	15	40	26	25	18	17	PA22 PINCM37 0x40428090	PA22	1	IO	SDIO (standard)
								UART2_RX	2	I	
								SPI0_CS2_MISO2	3	IO	
								UART1_RTS	4	O	
								TIMA0_C0N	5	O	
								TIMG1_C1	6	IO	
								TIMA0_C1	7	IO	
								CLK_OUT	8	O	
								I2C0_SCL	9	IOD	
								TIMG8_C1	10	IO	
								UART1_RX	11	I	
								SPI0_POCI	12	IO	
								UART2_TX	13	O	
								ADC0_7	(Non-IOMUX 1) 0	A	
								ADC0_VREF-	(Non-IOMUX 2) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
43	16	43	27	26	19	18	PA23 PINCM40 0x4042809c	PA23	1	IO	HSIO (high-speed)
								UART2_TX	2	O	
								SPI0_CS3_CD_MISO3	3	IO	
								TIMA0_C3	5	IO	
								TIMG8_C0	6	IO	
								TIMG2_C0	7	IO	
								UART0_TX	8	O	
								TIMG14_C0	9	IO	
								SPI0_POCI	12	IO	
								UART0_CTS	13	I	
								ADC0_26	(Non-IOMUX 1) 0	A	
								ADC0_VREF+	(Non-IOMUX 2) 0	A	
44	17	44	28	27	20	19	PA24 PINCM41 0x404280a0	PA24	1	IO	SDIO (standard)
								UART2_RX	2	I	
								SPI0_CS2_MISO2	3	IO	
								UART0_RTS	4	O	
								TIMA0_C3N	5	O	
								TIMG8_C1	6	IO	
								TIMG2_C1	7	IO	
								UART1_RX	8	I	
								TIMG14_C1	9	IO	
								SPI0_PICO	12	IO	
								I2C0_SDA	13	IOD	
								ADC0_3	(Non-IOMUX 1) 0	A	
45	18	45	29	28	21	20	PA25 PINCM42 0x404280a4	PA25	1	IO	SDIO (standard)
								SPI0_PICO	2	IO	
								SPI0_POCI	3	IO	
								SPI0_SCLK	4	IOD	
								TIMA0_C3	5	IO	
								TIMA0_C1N	6	O	
								TIMA0_C2	7	IO	
								UART2_CTS	8	I	
								TIMG14_C0	9	IO	
								TIMG1_C0	10	IO	
								I2C0_SDA	11	IOD	
								UART0_TX	12	O	
								UART0_RTS	13	O	
								I2C0_SCL	14	IOD	
								ADC0_2	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
46	19	46	30	1	22	1	PA26 PINCM43 0x404280a8	PA26	1	IO	HSIO (high-speed)
								BEEP	2	O	
								SPI0_POCI	3	IO	
								TIMG8_C0	4	IO	
								TIMA_FAL0	5	I	
								TIMA0_C3N	6	O	
								TIMG2_C0	7	IO	
								UART2_RTS	8	O	
								I2C0_SCL	9	IOD	
								TIMG1_C1	10	IO	
								UART0_RX	11	IO	
								TIMA0_C0	12	IO	
								I2C0_SDA	13	IOD	
								UART1_CTS	14	I	
								ADC0_1	(Non-IOMUX 1) 0	A	
								LFXOUT 2	(Non-IOMUX 2) 0	A	
47	20	47	31	2		2	PA27 PINCM44 0x404280ac	PA27	1	IO	HSIO (high-speed)
								SPI0_CS3_CD_MISO3	2	IO	
								TIMA0_C0N	3	O	
								TIMG8_C1	4	IO	
								TIMA_FAL2	5	I	
								CLK_OUT	6	O	
								TIMG2_C1	7	IO	
								RTC_OUT	8	O	
								UART1_CTS	9	I	
								I2C0_SCL	10	IOD	
								UART0_TX	11	O	
								SPI0_POCI	12	IO	
								LFCLKIN	14	I	
								ADC0_0	(Non-IOMUX 1) 0	A	
								LFXIN 2	(Non-IOMUX 2) 0	A	
3	3	3	2	5	1	5	PA28 PINCM3 0x40428008	PA28	1	IO	SDIO (standard)
								UART0_TX	2	O	
								I2C0_SDA	3	IOD	
								TIMA0_C3	4	IO	
								TIMA_FAL0	5	I	
								TIMG2_C0	6	IO	
								TIMA0_C1	7	IO	
								HFXIN	(Non-IOMUX 1) 0	A	
48	1	48	32	3	23	3	PA30 PINCM45 0x404280b0	PA30	1	IO	SDIO (standard)
								UART0_RX	4	IO	
								TIMG8_IDX	5	I	
								TIMA0_C0	6	IO	
								UART1_RTS	9	O	
								TIMG2_C1	10	IO	
								TIMG14_C2	11	IO	
								I2C0_SDA	12	IOD	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
5		5					PA31 PINCM4 0x4042800c	PA31	1	IO	SDIO (standard)
								UART0_RX	2	IO	
								I2C0_SCL	3	IOD	
								TIMA0_C3N	4	O	
								CLK_OUT	6	O	
14		14					PB2 PINCM11 0x40428028	PB2	1	IO	HSIO (high-speed)
								UART2_CTS	3	I	
								I2C1_SCL	4	IOD	
								TIMA0_C3	5	IO	
								UART1_CTS	6	I	
								TIMG1_C0	7	IO	
								UART2_TX	8	O	
								HFCLKIN	10	I	
								SPI0_PICO	11	IO	
								UART1_RX	12	I	
								TIMA0_C1N	13	O	
15	8	15					PB3 PINCM12 0x4042802c	PB3	1	IO	HSIO (high-speed)
								TIMA_FAL0	2	I	
								UART2_RTS	3	O	
								I2C1_SDA	4	IOD	
								TIMA0_C3N	5	O	
								UART1_RTS	6	O	
								TIMG1_C1	7	IO	
								UART2_RX	8	I	
								TIMG2_C1	9	IO	
								TIMA0_C0	10	IO	
								SPI0_SCLK	11	IOD	
								SPI0_CS0	12	IO	
								UART1_TX	13	O	
								RTC_OUT	14	O	
20		20					PB6 PINCM17 0x40428040	PB6	1	IO	SDIO (standard)
								UART1_TX	2	O	
								TIMG8_C0	5	IO	
								UART2_CTS	6	I	
								TIMG1_C0	7	IO	
								TIMA_FAL2	8	I	
								SPI0_CS1_MISO1	9	IO	
								TIMA0_C3N	11	O	
								TIMG8_C1	12	IO	
								TIMA0_C2N	13	O	
								UART0_TX	14	O	
								ADC0_24	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
21		21					PB7 PINCM18 0x40428044	PB7	1	IO	SDIO (standard)
								UART1_RX	2	I	
								TIMG8_C1	5	IO	
								UART2_RTS	6	O	
								TIMG1_C1	7	IO	
								SPI0_CS2_MISO2	9	IO	
								BEEP	12	O	
								SPI0_SCLK	13	IOD	
								UART0_RX	14	IO	
								ADC0_23	(Non-IOMUX 1) 0	A	
22		22					PB8 PINCM19 0x40428048	PB8	1	IO	SDIO (standard)
								UART1_CTS	2	I	
								TIMA0_C0	5	IO	
								TIMG1_C0	7	IO	
								SPI0_SCLK	9	IOD	
								BEEP	10	O	
								TIMG8_C0	11	IO	
								UART0_RX	12	IO	
								SPI0_POCI	13	IO	
								I2C0_SCL	14	IOD	
23		23					PB9 PINCM20 0x4042804c	PB9	1	IO	SDIO (standard)
								UART1_RTS	2	O	
								TIMA0_C0N	5	O	
								TIMA0_C1	6	IO	
								TIMG1_C1	7	IO	
								TIMG2_C0	8	IO	
								SPI0_POCI	10	IO	
								UART0_RX	11	IO	
								I2C0_SCL	12	IOD	
								UART0_TX	13	O	
								I2C0_SDA	14	IOD	
24		24					PB14 PINCM21 0x40428050	PB14	1	IO	SDIO (standard)
								TIMA0_C0	5	IO	
								TIMG8_IDX	6	I	
								SPI0_CS3_CD_MISO3	7	IO	
								TIMG2_C1	8	IO	
								I2C0_SDA	9	IOD	
								SPI0_PICO	10	IO	
								UART0_TX	11	O	
								TIMA_FAL2	12	I	
								TIMA_FAL0	13	I	
								TIMG14_C2	14	IO	
								ADC0_21	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
25		25					PB15 PINCM22 0x40428054	PB15	1	IO	SDIO (standard)
								UART2_TX	2	O	
								TIMG8_C0	5	IO	
								TIMG2_C0	6	IO	
								TIMA0_C1N	12	O	
								UART1_TX	13	O	
								TIMG2_C1	14	IO	
								ADC0_20	(Non-IOMUX 1) 0	A	
26		26					PB16 PINCM23 0x40428058	PB16	1	IO	SDIO (standard)
								UART2_RX	2	I	
								TIMG8_C1	5	IO	
								TIMG2_C1	6	IO	
								TIMA0_C2N	12	O	
								UART1_RX	13	I	
								I2C1_SDA	14	IOD	
								ADC0_19	(Non-IOMUX 1) 0	A	
36		36					PB17 PINCM33 0x40428080	PB17	1	IO	SDIO (standard)
								UART2_TX	2	O	
								SPI0_PICO	3	IO	
								I2C0_SCL	4	IOD	
								TIMA0_C2	5	IO	
								TIMG14_C0	6	IO	
								TIMG1_C0	9	IO	
								SPI0_CS0	10	IO	
								UART1_RX	11	I	
								UART1_TX	13	O	
								UART0_RTS	14	O	
								ADC0_11	(Non-IOMUX 1) 0	A	
37		37					PB18 PINCM34 0x40428084	PB18	1	IO	SDIO (standard)
								UART2_RX	2	I	
								SPI0_SCLK	3	IOD	
								I2C0_SDA	4	IOD	
								TIMA0_C2N	5	O	
								TIMG14_C1	6	IO	
								SPI0_CS0	7	IO	
								TIMG1_C1	9	IO	
								TIMA0_C1	12	IO	
								UART0_RTS	13	O	
								ADC0_10	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PT, RUK, RGZ, RHB, DGS28, RGE, DGS20 Packages) (continued)

PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
38		38					PB19 PINCM35 0x40428088	PB19	1	IO	SDIO (standard)
								SPI0_POCI	3	IO	
								TIMG8_C1	4	IO	
								UART0_CTS	5	I	
								TIMG2_C1	6	IO	
								TIMG8_IDX	7	I	
								UART2_CTS	8	I	
								TIMA0_C1N	12	O	
								UART2_RX	13	I	
								ADC0_9	(Non-IOMUX 1) 0	A	
41		41					PB20 PINCM38 0x40428094	PB20	1	IO	SDIO (standard)
								SPI0_CS2_MISO2	2	IO	
								TIMA0_C2	5	IO	
								TIMA_FAL1	6	I	
								TIMA0_C1	7	IO	
								UART2_RTS	8	O	
								I2C0_SDA	9	IOD	
								UART1_CTS	12	I	
								TIMA0_C2N	13	O	
								TIMG8_C1	14	IO	
								ADC0_6	(Non-IOMUX 1) 0	A	
42		42					PB24 PINCM39 0x40428098	PB24	1	IO	SDIO (standard)
								SPI0_CS3_CD_MISO3	2	IO	
								SPI0_CS1_MISO1	3	IO	
								TIMA0_C3	5	IO	
								TIMA0_C1N	6	O	
								UART2_RTS	8	O	
								SPI0_SCLK	12	IOD	
								TIMG14_C2	13	IO	
								UART0_RTS	14	O	
								ADC0_5	(Non-IOMUX 1) 0	A	
6	4	6	4	7	3	6	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
7	5	7	5	8	4	7	VSS	VSS	(Non-IOMUX 1) 0	PWR	PWR

1. RUK and DGS20 do not support LFXIN/LFXOUT on pins PA3/PA4 respectively.
2. DGS28, RGE, RHB, RGZ, and PT do not support LFXOUT/LFXIN on pins PA26/PA27 respectively

6.3 Signal Descriptions

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
ADC0_VREF+	A	ADC0 voltage reference (VREF) power supply	43	16	43	27	26	19	18
ADC0_VREF-	A	ADC0 voltage reference (VREF) ground supply	40	15	40	26	25	18	17
ADC0_0	A	ADC0 analog input channel 0	47	20	47	31	2		2
ADC0_1	A	ADC0 analog input channel 1	46	19	46	30	1	22	1

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Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
ADC0_2	A	ADC0 analog input channel 2	45	18	45	29	28	21	20
ADC0_3	A	ADC0 analog input channel 3	44	17	44	28	27	20	19
ADC0_4	A	ADC0 analog input channel 4	35	14	35	24	23	16	16
ADC0_5	A	ADC0 analog input channel 5	42		42				
ADC0_6	A	ADC0 analog input channel 6	41		41				
ADC0_7	A	ADC0 analog input channel 7	40	15	40	26	25	18	17
ADC0_8	A	ADC0 analog input channel 8	39		39	25	24	17	
ADC0_9	A	ADC0 analog input channel 9	38		38				
ADC0_10	A	ADC0 analog input channel 10	37		37				
ADC0_11	A	ADC0 analog input channel 11	36		36				
ADC0_12	A	ADC0 analog input channel 12	33	12	33	22	21	14	14
ADC0_13	A	ADC0 analog input channel 13	32	11	32	21	20	13	13
ADC0_14	A	ADC0 analog input channel 14	31	10	31	20	19	12	12
ADC0_15	A	ADC0 analog input channel 15	30		30	19	18	11	
ADC0_16	A	ADC0 analog input channel 16	29		29	18	17		
ADC0_17	A	ADC0 analog input channel 17	28		28	17			
ADC0_18	A	ADC0 analog input channel 18	27		27	16			
ADC0_19	A	ADC0 analog input channel 19	26		26				
ADC0_20	A	ADC0 analog input channel 20	25		25				
ADC0_21	A	ADC0 analog input channel 21	24		24				
ADC0_22	A	ADC0 analog input channel 22	34	13	34	23	22	15	15
ADC0_23	A	ADC0 analog input channel 23	21		21				
ADC0_24	A	ADC0 analog input channel 24	20		20				
ADC0_25	A	ADC0 analog input channel 25	19	9	19	15	16	10	11
ADC0_26	A	ADC0 analog input channel 26	43	16	43	27	26	19	18

Table 6-4. Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
BSL_invoke	I	Default Flash BSL invoke signal	19	9	19	15	16	10	11

Table 6-5. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
CLK_OUT	O	CLK_OUT digital clock output from the PMCU	13, 17, 18, 29, 33, 40, 47, 5	12, 15, 20	13, 17, 18, 29, 33, 40, 47, 5	11, 13, 14, 18, 22, 26, 31	14, 15, 17, 2, 21, 25	14, 18, 8, 9	14, 17, 2
FCC_IN	I	Frequency clock counter (FCC) input signal	1, 11, 13, 27, 31	10	1, 11, 13, 27, 31	11, 16, 20, 9	12, 19	12	12
HFCLKIN	I	High frequency clock digital clock input signal	10, 12, 14, 16, 2	2, 7	10, 12, 14, 16, 2	1, 10, 12, 8	11, 13, 4	24, 7	10, 4, 9
HFXIN	A	High frequency crystal oscillator (HFXT) signal	3	3	3	2	5	1	5
HFXOUT	A	High frequency crystal oscillator (HFXT) signal	2	2	2	1	4	24	4

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Table 6-5. Clock Module (CKM) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
LFCLKIN	I	Low frequency clock digital clock input signal	47	20	47	31	2		2
LFXIN	A	Low frequency crystal oscillator (LFXT) signal	47, 9	20	47	31	2	6	2
LFXOUT	A	Low frequency crystal oscillator (LFXT) signal	10, 46	19, 7	10, 46	30, 8	1, 11	22, 7	1, 9

Table 6-6. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
PA0	IO	GPIO port A input/output 0	1		1				
PA1	IO	GPIO port A input/output 1	2	2	2	1	4	24	4
PA2	IO	GPIO port A input/output 2	8	6	8	6	9	5	8
PA3	IO	GPIO port A input/output 3	9		9	7	10	6	
PA4	IO	GPIO port A input/output 4	10	7	10	8	11	7	9
PA5	IO	GPIO port A input/output 5	11		11	9	12		
PA6	IO	GPIO port A input/output 6	12		12	10	13		10
PA7	IO	GPIO port A input/output 7	13		13	11			
PA8	IO	GPIO port A input/output 8	16		16	12			
PA9	IO	GPIO port A input/output 9	17		17	13	14	8	
PA10	IO	GPIO port A input/output 10	18		18	14	15	9	
PA11	IO	GPIO port A input/output 11	19	9	19	15	16	10	11
PA12	IO	GPIO port A input/output 12	27		27	16			
PA13	IO	GPIO port A input/output 13	28		28	17			
PA14	IO	GPIO port A input/output 14	29		29	18	17		
PA15	IO	GPIO port A input/output 15	30		30	19	18	11	
PA16	IO	GPIO port A input/output 16	31	10	31	20	19	12	12
PA17	IO	GPIO port A input/output 17	32	11	32	21	20	13	13
PA18	IO	GPIO port A input/output 18	33	12	33	22	21	14	14
PA19	IO	GPIO port A input/output 19	34	13	34	23	22	15	15
PA20	IO	GPIO port A input/output 20	35	14	35	24	23	16	16
PA21	IO	GPIO port A input/output 21	39		39	25	24	17	
PA22	IO	GPIO port A input/output 22	40	15	40	26	25	18	17
PA23	IO	GPIO port A input/output 23	43	16	43	27	26	19	18
PA24	IO	GPIO port A input/output 24	44	17	44	28	27	20	19
PA25	IO	GPIO port A input/output 25	45	18	45	29	28	21	20
PA26	IO	GPIO port A input/output 26	46	19	46	30	1	22	1
PA27	IO	GPIO port A input/output 27	47	20	47	31	2		2
PA28	IO	GPIO port A input/output 28	3	3	3	2	5	1	5
PA30	IO	GPIO port A input/output 30	48	1	48	32	3	23	3
PA31	IO	GPIO port A input/output 31	5		5				
PB2	IO	GPIO port B input/output 2	14		14				
PB3	IO	GPIO port B input/output 3	15	8	15				
PB6	IO	GPIO port B input/output 6	20		20				
PB7	IO	GPIO port B input/output 7	21		21				
PB8	IO	GPIO port B input/output 8	22		22				

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Table 6-6. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
PB9	IO	GPIO port B input/output 9	23		23				
PB14	IO	GPIO port B input/output 14	24		24				
PB15	IO	GPIO port B input/output 15	25		25				
PB16	IO	GPIO port B input/output 16	26		26				
PB17	IO	GPIO port B input/output 17	36		36				
PB18	IO	GPIO port B input/output 18	37		37				
PB19	IO	GPIO port B input/output 19	38		38				
PB20	IO	GPIO port B input/output 20	41		41				
PB24	IO	GPIO port B input/output 24	42		42				

Table 6-7. I2C Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
I2C0_SCL	IOD	I2C0 serial clock signal (SCL)	17, 19, 2, 22, 23, 29, 36, 40, 45, 46, 47, 5, 8	15, 18, 19, 2, 20, 6, 9	17, 19, 2, 22, 23, 29, 36, 40, 45, 46, 47, 5, 8	1, 13, 15, 18, 26, 29, 30, 31, 6	1, 14, 16, 17, 2, 25, 28, 4, 9	10, 18, 21, 22, 24, 5, 8	1, 11, 17, 2, 20, 4, 8
I2C0_SDA	IOD	I2C0 serial data signal (SDA)	1, 12, 16, 18, 2, 23, 24, 3, 37, 41, 44, 45, 46, 48, 9	1, 17, 18, 19, 2, 3	1, 12, 16, 18, 2, 23, 24, 3, 37, 41, 44, 45, 46, 48, 9	1, 10, 12, 14, 2, 28, 29, 30, 32, 7	1, 10, 13, 15, 27, 28, 3, 4, 5	1, 20, 21, 22, 23, 24, 6, 9	1, 10, 19, 20, 3, 4, 5
I2C1_SCL	IOD	I2C1 serial clock signal (SCL)	10, 12, 14, 19, 27, 30, 32, 35	11, 14, 7, 9	10, 12, 14, 19, 27, 30, 32, 35	10, 15, 16, 19, 21, 24, 8	11, 13, 16, 18, 20, 23	10, 11, 13, 16, 7	10, 11, 13, 16, 9
I2C1_SDA	IOD	I2C1 serial data signal (SDA)	11, 15, 18, 26, 31, 33, 34, 9	10, 12, 13, 8	11, 15, 18, 26, 31, 33, 34, 9	14, 20, 22, 23, 7, 9	10, 12, 15, 19, 21, 22	12, 14, 15, 6, 9	12, 14, 15

Table 6-8. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
RTC_OUT	O	Real-time clock output signal	1, 15, 17, 28, 47	20, 8	1, 15, 17, 28, 47	13, 17, 31	14, 2	8	2

Table 6-9. Serial Peripheral Interface (SPI) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
SPI0_PICO	IO	SPI0 peripheral in controller out signal	11, 13, 14, 17, 18, 24, 29, 33, 34, 35, 36, 44, 45	12, 13, 14, 17, 18	11, 13, 14, 17, 18, 24, 29, 33, 34, 35, 36, 44, 45	11, 13, 14, 18, 22, 23, 24, 28, 29, 9	12, 14, 15, 17, 21, 22, 23, 27, 28	14, 15, 16, 20, 21, 8, 9	14, 15, 16, 19, 20

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Table 6-9. Serial Peripheral Interface (SPI) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
SPI0_POCI	IO	SPI0 peripheral out controller in signal	10, 13, 17, 18, 22, 23, 28, 31, 33, 34, 38, 40, 43, 45, 46, 47	10, 12, 13, 15, 16, 18, 19, 20, 7	10, 13, 17, 18, 22, 23, 28, 31, 33, 34, 38, 40, 43, 45, 46, 47	11, 13, 14, 17, 20, 22, 23, 26, 27, 29, 30, 31, 8	1, 11, 14, 15, 19, 2, 21, 22, 25, 26, 28	12, 14, 15, 18, 19, 21, 22, 7, 8, 9	1, 12, 14, 15, 17, 18, 2, 20, 9
SPI0_SCLK	IOD	SPI0 serial clock	12, 15, 16, 19, 21, 22, 27, 32, 34, 37, 42, 45	11, 13, 18, 8, 9	12, 15, 16, 19, 21, 22, 27, 32, 34, 37, 42, 45	10, 12, 15, 16, 21, 23, 29	13, 16, 20, 22, 28	10, 13, 15, 21	10, 11, 13, 15, 20
SPI0_CS0	IO	SPI0 chip-select 0 signal	10, 15, 16, 19, 28, 33, 36, 37, 8	12, 6, 7, 8, 9	10, 15, 16, 19, 28, 33, 36, 37, 8	12, 15, 17, 22, 6, 8	11, 16, 21, 9	10, 14, 5, 7	11, 14, 8, 9
SPI0_CS1_MISO1	IO		1, 20, 27, 32, 42, 9	11	1, 20, 27, 32, 42, 9	16, 21, 7	10, 20	13, 6	13
SPI0_CS2_MISO2	IO		13, 21, 29, 30, 40, 41, 44	15, 17	13, 21, 29, 30, 40, 41, 44	11, 18, 19, 26, 28	17, 18, 25, 27	11, 18, 20	17, 19
SPI0_CS3_CD_MISO3	IO		16, 2, 24, 28, 39, 42, 43, 47, 9	16, 2, 20	16, 2, 24, 28, 39, 42, 43, 47, 9	1, 12, 17, 25, 27, 31, 7	10, 2, 24, 26, 4	17, 19, 24, 6	18, 2, 4

Table 6-10. Serial Wire Debug (SWD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
SWCLK	I	Serial wire debug interface clock input signal	35	14	35	24	23	16	16
SWDIO	IO	Serial wire debug interface data input/output signal	34	13	34	23	22	15	15

Table 6-11. System Controller (SYSCTL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
BEEP	O	Beep output	1, 12, 21, 22, 46	19	1, 12, 21, 22, 46	10, 30	1, 13	22	1, 10
NRST	RESET	Active-low reset signal (must be logic high for the device to start)	4	3	4	3	6	2	5
VDD	PWR	VDD supply	6	4	6	4	7	3	6
VSS	PWR	VSS (ground)	7	5	7	5	8	4	7

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Table 6-12. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
TIMA0_C0	IO	TIMA0 capture/compare 0 signal	1, 15, 16, 22, 24, 33, 35, 39, 46, 48, 8	1, 12, 14, 19, 6, 8	1, 15, 16, 22, 24, 33, 35, 39, 46, 48, 8	12, 22, 24, 25, 30, 32, 6	1, 21, 23, 24, 3, 9	14, 16, 17, 22, 23, 5	1, 14, 16, 3, 8
TIMA0_C1	IO	TIMA0 capture/compare 1 signal	11, 13, 17, 2, 23, 28, 3, 37, 40, 41, 9	15, 2, 3	11, 13, 17, 2, 23, 28, 3, 37, 40, 41, 9	1, 11, 13, 17, 2, 26, 7, 9	10, 12, 14, 25, 4, 5	1, 18, 24, 6, 8	17, 4, 5
TIMA0_C2	IO	TIMA0 capture/compare 2 signal	12, 13, 18, 29, 30, 32, 34, 36, 41, 45, 9	11, 13, 18	12, 13, 18, 29, 30, 32, 34, 36, 41, 45, 9	10, 11, 14, 18, 19, 21, 23, 29, 7	10, 13, 15, 17, 18, 20, 22, 28	11, 13, 15, 21, 6, 9	10, 13, 15, 20
TIMA0_C3	IO	TIMA0 capture/compare 3 signal	10, 14, 27, 3, 32, 42, 43, 45	11, 16, 18, 3, 7	10, 14, 27, 3, 32, 42, 43, 45	16, 2, 21, 27, 29, 8	11, 20, 26, 28, 5	1, 13, 19, 21, 7	13, 18, 20, 5, 9
TIMA0_C0N	O	TIMA0 capture/compare 0 complementary output	10, 17, 23, 32, 39, 40, 47	11, 15, 20, 7	10, 17, 23, 32, 39, 40, 47	13, 21, 25, 26, 31, 8	11, 14, 2, 20, 24, 25	13, 17, 18, 7, 8	13, 17, 2, 9
TIMA0_C1N	O	TIMA0 capture/compare 1 complementary output	10, 14, 18, 25, 38, 42, 45	18, 7	10, 14, 18, 25, 38, 42, 45	14, 29, 8	11, 15, 28	21, 7, 9	20, 9
TIMA0_C2N	O	TIMA0 capture/compare 2 complementary output	12, 19, 20, 26, 28, 31, 35, 37, 41, 8	10, 14, 6, 9	12, 19, 20, 26, 28, 31, 35, 37, 41, 8	10, 15, 17, 20, 24, 6	13, 16, 19, 23, 9	10, 12, 16, 5	10, 11, 12, 16, 8
TIMA0_C3N	O	TIMA0 capture/compare 3 complementary output	15, 16, 20, 27, 28, 33, 44, 46, 5, 8	12, 17, 19, 6, 8	15, 16, 20, 27, 28, 33, 44, 46, 5, 8	12, 16, 17, 22, 28, 30, 6	1, 21, 27, 9	14, 20, 22, 5	1, 14, 19, 8
TIMA_FAL0	I	TIMA fault input 0	12, 15, 16, 19, 24, 3, 46, 8	19, 3, 6, 8, 9	12, 15, 16, 19, 24, 3, 46, 8	10, 12, 15, 2, 30, 6	1, 13, 16, 5, 9	1, 10, 22, 5	1, 10, 11, 5, 8
TIMA_FAL1	I	TIMA fault input 1	1, 11, 17, 18, 35, 41, 8	14, 6	1, 11, 17, 18, 35, 41, 8	13, 14, 24, 6, 9	12, 14, 15, 23, 9	16, 5, 8, 9	16, 8
TIMA_FAL2	I	TIMA fault input 2	16, 2, 20, 24, 33, 47	12, 2, 20	16, 2, 20, 24, 33, 47	1, 12, 22, 31	2, 21, 4	14, 24	14, 2, 4
TIMG8_IDX	I	TIMG8 quadrature encoder index pulse signal	13, 2, 24, 30, 38, 48, 8	1, 2, 6	13, 2, 24, 30, 38, 48, 8	1, 11, 19, 32, 6	18, 3, 4, 9	11, 23, 24, 5	3, 4, 8
TIMG14_C0	IO	TIMG14 capture/compare 0 signal	1, 11, 18, 27, 34, 36, 43, 45	13, 16, 18	1, 11, 18, 27, 34, 36, 43, 45	14, 16, 23, 27, 29, 9	12, 15, 22, 26, 28	15, 19, 21, 9	15, 18, 20

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Table 6-12. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
TIMG14_C1	IO	TIMG14 capture/compare 1 signal	12, 19, 2, 28, 35, 37, 44	14, 17, 2, 9	12, 19, 2, 28, 35, 37, 44	1, 10, 15, 17, 24, 28	13, 16, 23, 27, 4	10, 16, 20, 24	10, 11, 16, 19, 4
TIMG14_C2	IO	TIMG14 capture/compare 2 signal	24, 31, 42, 48	1, 10	24, 31, 42, 48	20, 32	19, 3	12, 23	12, 3
TIMG14_C3	IO	TIMG14 capture/compare 3 signal	28		28	17			
TIMG1_C0	IO	TIMG1 capture/compare 0 signal	11, 13, 14, 20, 22, 29, 36, 39, 45	18	11, 13, 14, 20, 22, 29, 36, 39, 45	11, 18, 25, 29, 9	12, 17, 24, 28	17, 21	20
TIMG1_C1	IO	TIMG1 capture/compare 1 signal	12, 15, 17, 21, 23, 37, 40, 46	15, 19, 8	12, 15, 17, 21, 23, 37, 40, 46	10, 13, 26, 30	1, 13, 14, 25	18, 22, 8	1, 10, 17
TIMG2_C0	IO	TIMG2 capture/compare 0 signal	17, 23, 25, 3, 32, 43, 46, 9	11, 16, 19, 3	17, 23, 25, 3, 32, 43, 46, 9	13, 2, 21, 27, 30, 7	1, 10, 14, 20, 26, 5	1, 13, 19, 22, 6, 8	1, 13, 18, 5
TIMG2_C1	IO	TIMG2 capture/compare 1 signal	10, 13, 15, 16, 24, 25, 26, 27, 33, 38, 44, 47, 48, 8	1, 12, 17, 20, 6, 7, 8	10, 13, 15, 16, 24, 25, 26, 27, 33, 38, 44, 47, 48, 8	11, 12, 16, 22, 28, 31, 32, 6, 8	11, 2, 21, 27, 3, 9	14, 20, 23, 5, 7	14, 19, 2, 3, 8, 9
TIMG8_C0	IO	TIMG8 capture/compare 0 signal	11, 13, 2, 20, 22, 25, 32, 39, 43, 46, 9	11, 16, 19, 2	11, 13, 2, 20, 22, 25, 32, 39, 43, 46, 9	1, 11, 21, 25, 27, 30, 7, 9	1, 10, 12, 20, 24, 26, 4	13, 17, 19, 22, 24, 6	1, 13, 18, 4
TIMG8_C1	IO	TIMG8 capture/compare 1 signal	1, 10, 12, 18, 20, 21, 26, 28, 33, 38, 40, 41, 44, 47, 8	12, 15, 17, 20, 6, 7	1, 10, 12, 18, 20, 21, 26, 28, 33, 38, 40, 41, 44, 47, 8	10, 14, 17, 22, 26, 28, 31, 6, 8	11, 13, 15, 2, 21, 25, 27, 9	14, 18, 20, 5, 7, 9	10, 14, 17, 19, 2, 8, 9

Table 6-13. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
UART0_CTS	I	UART0 clear to send signal	11, 17, 29, 33, 34, 38, 43	12, 13, 16	11, 17, 29, 33, 34, 38, 43	13, 18, 22, 23, 27, 9	12, 14, 17, 21, 22, 26	14, 15, 19, 8	14, 15, 18
UART0_RTS	O	UART0 ready to send signal	12, 16, 30, 34, 35, 36, 37, 42, 44, 45	13, 14, 17, 18	12, 16, 30, 34, 35, 36, 37, 42, 44, 45	10, 12, 19, 23, 24, 28, 29	13, 18, 22, 23, 27, 28	11, 15, 16, 20, 21	10, 15, 16, 19, 20

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Table 6-13. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PT PIN	RUK PIN	RGZ PIN	RHB PIN	DGS28 PIN	RGE PIN	DGS20 PIN
UART0_RX	IO	UART0 receive signal (RXD)	19, 2, 21, 22, 23, 32, 46, 48, 5	1, 11, 19, 2, 9	19, 2, 21, 22, 23, 32, 46, 48, 5	1, 15, 21, 30, 32	1, 16, 20, 3, 4	10, 13, 22, 23, 24	1, 11, 13, 3, 4
UART0_TX	O	UART0 transmit signal (TXD)	1, 18, 2, 20, 23, 24, 29, 3, 43, 45, 47	16, 18, 2, 20, 3	1, 18, 2, 20, 23, 24, 29, 3, 43, 45, 47	1, 14, 18, 2, 27, 29, 31	15, 17, 2, 26, 28, 4, 5	1, 19, 21, 24, 9	18, 2, 20, 4, 5
UART1_CTS	I	UART1 clear to send signal	14, 22, 27, 39, 41, 46, 47	19, 20	14, 22, 27, 39, 41, 46, 47	16, 25, 30, 31	1, 2, 24	17, 22	1, 2
UART1_RTS	O	UART1 ready to send signal	15, 2, 23, 28, 33, 40, 48	1, 12, 15, 2, 8	15, 2, 23, 28, 33, 40, 48	1, 17, 22, 26, 32	21, 25, 3, 4	14, 18, 23, 24	14, 17, 3, 4
UART1_RX	I	UART1 receive signal (RXD)	10, 12, 14, 16, 17, 19, 21, 26, 33, 35, 36, 40, 44	12, 14, 15, 17, 7, 9	10, 12, 14, 16, 17, 19, 21, 26, 33, 35, 36, 40, 44	10, 12, 13, 15, 22, 24, 26, 28, 8	11, 13, 14, 16, 21, 23, 25, 27	10, 14, 16, 18, 20, 7, 8	10, 11, 14, 16, 17, 19, 9
UART1_TX	O	UART1 transmit signal (TXD)	11, 13, 15, 16, 20, 25, 32, 36, 9	11, 8	11, 13, 15, 16, 20, 25, 32, 36, 9	11, 12, 21, 7, 9	10, 12, 20	13, 6	13
UART2_CTS	I	UART2 clear to send signal	14, 20, 27, 31, 38, 39, 45, 9	10, 18	14, 20, 27, 31, 38, 39, 45, 9	16, 20, 25, 29, 7	10, 19, 24, 28	12, 17, 21, 6	12, 20
UART2_RTS	O	UART2 ready to send signal	10, 15, 21, 30, 41, 42, 46	19, 7, 8	10, 15, 21, 30, 41, 42, 46	19, 30, 8	1, 11, 18	11, 22, 7	1, 9
UART2_RX	I	UART2 receive signal (RXD)	15, 26, 29, 37, 38, 39, 40, 44	15, 17, 8	15, 26, 29, 37, 38, 39, 40, 44	18, 25, 26, 28	17, 24, 25, 27	17, 18, 20	17, 19
UART2_TX	O	UART2 transmit signal (TXD)	14, 25, 28, 36, 39, 40, 43	15, 16	14, 25, 28, 36, 39, 40, 43	17, 25, 26, 27	24, 25, 26	17, 18, 19	17, 18

6.4 Connections for Unused Pins

Table 6-14 lists the correct termination of unused pins.

Table 6-14. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.

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Table 6-14. Connection of Unused Pins (continued)

PIN (1)	POTENTIAL	COMMENT
NRST	VCC	NRST is an active-low reset signal. Pull high to VCC or the device cannot start. For more information, see Section 9.1.

(1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAx" unused pin connection guidelines.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	-0.3	6.5	V
V_I	Input voltage	Applied to any common tolerance pins	-0.3	V_{DD} + 0.3 (6.5 MAX)	V
I_{VDD}	Current of VDD pin	Current into VDD pin (source)		80	mA
I_{VSS}	Current of VSS pin	Current out of VSS pin (sink)		80	mA
I_{IO}	Current for SDIO pin	Current sunk or sourced by SDIO pin		3	mA
I_{IO}	Current for SDIO pin	Current sunk or sourced by HSIO pin		6	mA
I_D	Supported diode current	Diode current at any device pin		±2	mA
T_A		Ambient Temperature	–40	125	°C
Tj		Junction temperature	–40	130	°C
T_{stg}		Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage (2)	4.5 (4)		5.5	V
C_{VDD}	Capacitor placed between VDD and VSS (1)		10		uF
T_A	Ambient temperature	–40		125	°C
T_J	Max junction temperature			130	°C
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state (3)			32	MHz
	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait state (3)			24	MHz

(1) Connect C_{VDD} between VDD/VSS, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}.
(2) There is no dependency on MCLK frequency with respect to VDD recommended operating range.
(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software.
(4) Functionality is guaranteed down to VBOR0-(min).

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7.4 Thermal Information

THERMAL METRIC[1]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT)	77.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		34.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		49.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		49.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ)	30.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		23.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		16.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		16.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		7.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	36.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		17.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		17.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		7.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-28 (DGS28)	79.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		38.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		41.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		40.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-24 (RGE)	45.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		22.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		8.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-20 (DGS20)	91.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		48.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		47.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	WQFN-20 (RUK)	48.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		47.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		22.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		22.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		8.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=5V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	3.9		4.0		4.0		4.0		4.1		mA
IDD_{RUN}, per MHz	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	123		126		127		127		127		uA/Mhz
	MCLK=SYSOSC, While(1), execute from flash	32MHz	89	100	91	101	92	102	92	102	93	102	
SLEEP Mode													
IDD_{SLEEP}	MCLK=SYSOSC, CPU is halted	32MHz	2452	2647	2516	2693	2558	2723	2575	2740	2595	2760	uA
IDD_{SLEEP}	MCLK=LFCLK, CPU is halted	32kHz	828	930	873	959	926	1011	943	1028	967	1128	uA

7.5.2 STOP/STANDBY Modes

VDD=5V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, DISABLESTOP=0	4MHz	1390	1512	1442	1547	1479	1575	1493	1589	1510	1628	uA
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	631	720	674	749	714	783	729	798	748	869	
STANDBY Mode													
IDD_{STBY0}	LFCLK=LFOSC, STOPCLKSTBY=0, TIMG8 enabled	32kHz	4.0	5.5	4.3	5.5	12	23	17	27	24	79	uA
	LFCLK=LFXT, STOPCLKSTBY=0, TIMG8 enabled	32kHz	4.0	5.5	4.3	5.5	12	24	17	29	24	86	
IDD_{STBY1}	LFCLK=LFOSC, STOPCLKSTBY=1, TIMG8 enabled	32kHz	3.5	4.4	3.8	4.8	12	22	16	26	24	78	uA
	LFCLK=LFOSC, STOPCLKSTBY=1, GPIOA enabled	32kHz	3.5	4.4	3.8	4.8	12	22	16	26	24	78	
	LFCLK=LFXT, STOPCLKSTBY=1, TIMG8 enabled	32kHz	3.5	4.4	3.8	4.8	12	23	16	28	24	85	
	LFCLK=LFXT, STOPCLKSTBY=1, GPIOA enabled	32kHz	3.5	4.4	3.8	4.8	12	23	16	28	24	85	

7.6 Power Supply Sequencing

7.6.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (1)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising	2.5	3.33	4.2	V
V_{POR-}		Falling	2.4	3.25	4.1	V

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS, POR}$	POR hysteresis		10	80	170	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	Cold start, rising	3.9	4.2	4.5	V
V_{BOR0+}		Rising	4.26	4.4	4.5	
V_{BOR0-}		Falling	4.24	4.38	4.48	
$V_{BOR0, STBY}$	Brown-out reset voltage level 0 (default level)	STANDBY mode	4	4.27	4.5	V
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0		14	23	mV
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
		STANDBY mode			100	us

(1) Device operating in RUN, SLEEP, or STOP mode.

7.6.2 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

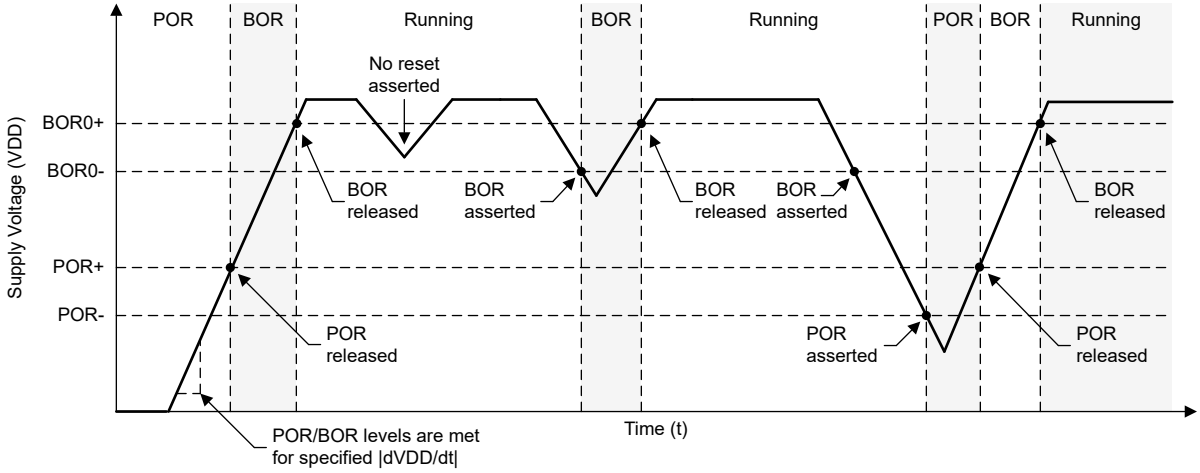

Figure 7-1. Power Cycle POR/BOR Conditions

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
$NWEC_{(LOWER)}$	Erase/program cycle endurance (lower 32kB flash) (1)		100			k cycles
$NWEC_{(UPPER)}$	Erase/program cycle endurance (remaining flash) (1)		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C ≤T_j ≤ 85°C	60			years

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RET_105}	Flash memory data retention	-40°C ≤T_j ≤ 105°C	11.4			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 64)}$	Program time for flash word (4) (6)			50	275	µs
$t_{PROG\ (SEC,\ 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤2k erase/program cycles, T_j≥25°C		4	20	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles, T_j≥25°C		20	150	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles		20	200	ms
$t_{ERASE\ (BANK)}$	Bank erase time	≤10k erase/program cycles		22	220	ms

(1) The lower 32kB flash address space supports higher erase/program endurance to enable EEPROM emulation applications. On devices with <=32kB flash memory, the entire flash memory supports $NWEC_{(LOWER)}$ erase/program cycles.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=5V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE,\ SLEEP}$	Wakeup time from SLEEP0 to RUN			2		cycles
$t_{WAKE,\ SLEEP}$	Wakeup time from SLEEP1 to RUN			1.7		us
$t_{WAKE,\ SLEEP}$	Wakeup time from SLEEP2 to RUN			2.3		us
$t_{WAKE,\ STOP}$	Wakeup time from STOP0 to RUN (SYSOSC enabled)			8.1		us
	Wakeup time from STOP2 to RUN (SYSOSC disabled)			8.8		us
$t_{WAKE,\ STBY}$	Wakeup time from STANDBY0 to RUN			12.8		us
$t_{WAKE,\ STBY}$	Wakeup time from STANDBY1 to RUN			12.8		us
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP1		0.3		us
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2		0.9		us
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP0		0.9		us
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP2		0.9		us
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY0		5.0		us

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VDD=5V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1		5.0		us
Startup Timing						
$t_{START, RESET}$	Device cold start-up time from reset/ power-up (1)	Fast boot enabled		252		us
$t_{START, RESET}$	Device cold start-up time from reset/ power-up (1)	Fast boot disabled		292		us
NRST Timing						
$t_{RST, BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK=SYSOSC		2		us
		ULPCLK=LFOSC		100		us
$t_{RST, POR}$	Pulse length on NRST pin to generate POR			1		s

(1) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used (1)	SETUSEFCL=1, T_a = 25 ℃	0		1	%
		SETUSEFCL=1 -40 ℃ ≤ T_a ≤ 125 ℃	-2.1		1.6	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	-2.6		1.8	%
$t_{settle, SYSOSC}$	Settling time to target accuracy (2)	SETUSEFCL=1			36	us

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.

(2) When SYSOSC is enabled from a disabled state, the SYSOSC output will be released to the device within the time specified by $t_{start, SYSOSC}$. Once the output is released, the SYSOSC worst-case accuracy is specified by f_{settle}, SYSOSC. After the time specified by $t_{settle, SYSSOSC}$, the SYSOSC will have settled to the target f_{SYSOSC} accuracy.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
f_{LFOSC}	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 125 ℃	–5		5	%
f_{LFOSC}	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 85 ℃	-3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1		ms

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7.9.3 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
f_{HFXT}	HFXT frequency	HFXTRSEL=01	8.01		16	MHz
f_{HFXT}	HFXT frequency	HFXTRSEL=10	16.01		32	MHz
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=01	40		60	%
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=10	40		60	%
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance (1)			1		pF
$t_{start, HFXT}$	HFXT start-up time(2)	HFXTRSEL=11, 32MHz crystal		0.5		ms
I_{HFXT}	HFXT current consumption(2)	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		100		uA
I_{HFXT}	HFXT current consumption(2)	f_{HFXT}=32MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		uA
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency (3)	USEEXTHFCLK =1	4		32	MHz
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK =1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{HFXIN} \times C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT})$, where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM0 H-Series 32-MHz Microcontrollers Technical Reference Manual.Current consumption increases with higher RSEL and start up time is decreases with higher RSEL.
(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.9.4 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, LFXT}$	LFXT start-up time (2)			200		ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=0, LOWCAP=1		300		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency (3)	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle (3)	SETUSEEXLF=1	40		60	%

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LFCLK Monitor						
$f_{FAULTLF}$	LFCLK monitor fault frequency (4)	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The user must ensure that the crystal is properly rated to support the start-up drive load (e.g. 0.1uW)
(3) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(4) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage		VDD≥4.5V	0.7*VDD		VDD	V
V_{IL}	Low level input voltage		VDD≥4.5V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis			0.1*VDD			V
I_{lkg}	High-Z leakage current	HSIO(1)	VDD = 5.5V			0.79(4)	uA
	High-Z leakage current (all pins except PA1, PA28)	SDIO(2) (3)	VDD = 5.5V			0.42(4)	
	High-Z leakage current (PA1, PA28)	SDIO(2) (3)	VDD = 5.5V			2.0	
R_{PU}	Pull up resistance		VIN = VSS		40		kΩ
C_I	Input capacitance		VDD = 5V		20		pF
V_{OH}	High level output voltage	HSIO	VDD≥4.5V, $\|I_{IO}\|_{,max}$=6mA	VDD-0.4			V
	High level output voltage	SDIO	VDD ≥ 4.5V, $\|I_{IO}\|_{,max}$ = 3mA	VDD-0.4			
V_{OL}	Low level output voltage	HSIO	VDD≥4.5V, $\|I_{IO}\|_{,max}$=6mA			0.4	V
	Low level output voltage	SDIO	VDD ≥ 4.5V,$\|I_{IO}\|_{,max}$ = 3mA			0.4	

(1) I/O Types: SDIO = Standard-Drive (8-MHz), HSIO = High-Speed (16-MHz)
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(4) This value is for IOs not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be higher.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO (1)	VDD ≥ 4.5V, C_L= 20pF			8	MHz
f_{max}	Port output frequency	HSIO	VDD ≥ 2.7V, DRV = 1, CL= 20pF 40			16	MHz
t_r,t_f	Output rise/fall time	All output ports	VDD ≥ 4.5V			0.3/f_{max}	s

(1) I/O Types: SDIO = Standard-Drive , HSIO = High-Speed

7.11 ADC

7.11.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V

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over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from internal reference (VREF)		4.05		V
V_{R-}	Negative ADC reference voltage			0		V
Fs	ADC sampling frequency	RES = 0x0 (12-bit mode), External Reference			1.6	Msps
		RES = 0x1 (10-bit mode), External Reference			1.77	
		RES = 0x2 (8-bit mode), External Reference			2	
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), Internal Reference			0.9	Msps
		RES = 0x1 (10-bit mode), Internal Reference			1	
		RES = 0x2 (8-bit mode), Internal Reference			1.2	
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 1.6MSPS, V_{R+} = VDD		350		µA
		F_S = 0.9MSPS,V_{R+} = VREF = 4.05V (VREF power consumption included)		400		
$C_{S/H}$	ADC sample-and-hold capacitance			0.22		pF
Rin	ADC switch resistance			15		kΩ
$ENOB_{AC}$	Effective number of bits, AC	Internal reference, V_{R+} = VREF = 4.05V, f_{in} = 5kHz	9.2	10.2		bit
		External reference(2), f_{in} = 5kHz	10.0	10.7		
		External reference with over sampling, f_{in} = 1kHz		11.4		
SNR	Signal-to-noise ratio	External reference (2)		68		dB
		External reference with over sampling		74		
		Internal reference, V_{R+} = VREF = 4.05V		64		
$PSRR_{DC}$	Power supply rejection ratio, DC	VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 4.05V		60		dB
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference (4), VDD = $VDD_{(min)}$ to $VDD_{(max)}$		64		dB
$PSRR_{AC}$	Power supply rejection ratio, AC	ΔVDD = 0.1 V at 1 kHz Internal reference, V_{R+} = VREF = 4.05V		48.6		dB
$PSRR_{AC}$	Power supply rejection ratio, AC	ΔVDD = 0.1 V at 1 kHz External reference, V_{R+} = VREF = 4.05V		61		dB
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor (3)	-1.5		+1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		16		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 5V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin
(3) Analog power supply monitor. Analog input on channel 31 is disconnected and is internally connected to the voltage divider which is VDD/3.

7.11.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency		4		32	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample_step}	Sampling time for step input	12-bit mode, R_S = 50Ω, C_{pext} = 10pF, V_{step}=4V	0.188			µs
t_{Sample_step}	Sampling time for step input	12-bit mode, R_S = 50Ω, C_{pext} = 10pF, V_{step}=5V	0.400			µs
t_{Sample_VREF}	Sample time with internal VREF input	ADC CHANNEL=29, 12-bit mode, VDD as reference	10			µs
$t_{Sample_SupplyMon}$	Sample time with Supply Monitor (VDD/3)		3			µs

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7.11.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL)	External reference, 12-bit (2)	-2.5		+2.5	LSB
E_D	Differential linearity error (DNL)	External reference, 12-bit (2)	-1		+1.5	LSB
	Differential linearity error (DNL)	External reference, 10-bit (2)	-1		+0.4	
E_O	Offset error	External reference, 12-bit (2)	-5		5	mV
E_G	Gain error	External reference, 12-bit (2)	-6		6	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 5V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin

7.11.4 Typical Connection Diagram

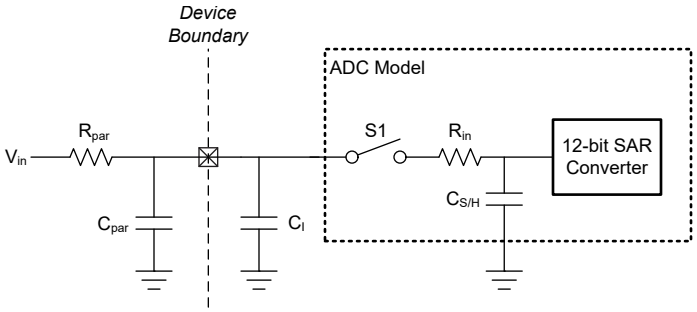

Figure 7-2. ADC Input Network

1. Refer to Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to Electrical Characteristics for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. Tau = $(R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_I)$
2. K= $\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (minimum sampling time) = K × Tau

7.12 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)		27	30	33	°C
TS_c	Temperature coefficient		-2.05	-1.9	-1.75	mV/°C
$t_{SET, TS}$	Temperature sensor settling time (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=4h (VREF+=4.05V,VREF-=0), ADC CHANNEL=28		5	10	us

(1) Higher absolute accuracy may be achieved through user calibration.
(2) This is the minimum required ADC sampling time when measuring the temperature sensor.

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7.13 VREF

7.13.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation		4.5	5	5.5	V
VREF	Voltage reference output voltage		3.98	4.05	4.12	V

7.13.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current(this spec is an estimation and will be more reliable once the IP is further in the design phase)	No load	No load		150	200	µA
TC_{VREF}	Temperature coefficient of VREF (1)					80	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, T = 25℃	Time = 1000 hours, T = 25℃			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD 4.5 to VDDmax, BUFCONFIG = 1		49	60		dB
$T_{startup}$	VREF startup time	VDD = 5 V	VDD = 5 V			30	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.14 I2C

7.14.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0		32		32		32	MHz
f_{SCL}	SCL clock frequency			100		400		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

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7.14.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.14.3 I²C Timing Diagram

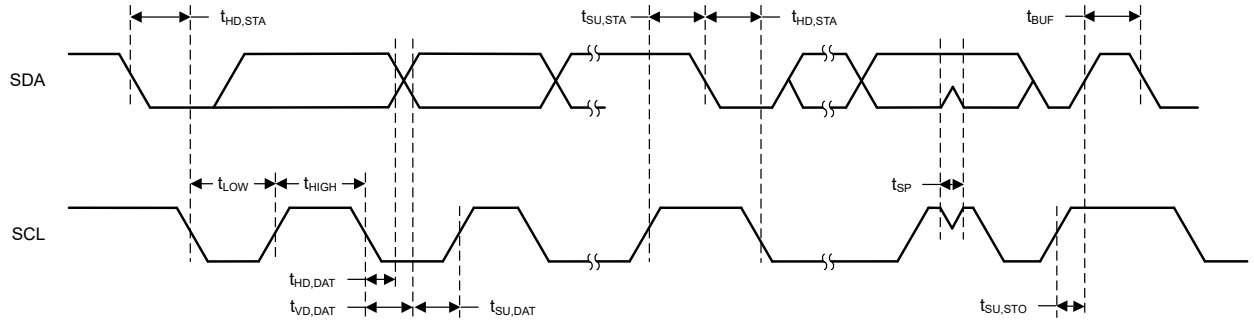

Figure 7-3. I2C Timing Diagram

7.15 SPI

7.15.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	MCLK = 32MHz 4.5 < VDD < 5.5V Peripheral or Controller mode			16[4]	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=0	1 SPI CLOCK			ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=1	1/2 SPI CLOCK			
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	SPH=0	1/2 SPI CLOCK			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	SPH=1	1 SPI CLOCK			
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI CLOCK	ns
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1 SPI CLOCK	ns
$t_{SU.CI}$	POCI input data setup time [1]	delayed sampling enabled	3			ns
$t_{SU.CI}$	POCI input data setup time [1]	no delayed sampling	34			ns
$t_{HD.CI}$	POCI input data hold time	delayed sampling enabled	23			ns
$t_{HD.CI}$	POCI input data hold time	no delayed sampling	0			ns
$t_{VALID.CO}$	PICO output data valid time [2]				10	ns

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over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HD.CO}$	PICO output data hold time (3)		0			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		15			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				45	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance				45	ns
$t_{SU.PI}$	PICO input data setup time		15			ns
$t_{HD.PI}$	PICO input data hold time		3			ns
$t_{VALID.PO}$	POCI output data valid time(2)				33	ns
$t_{HD.PO}$	POCI output data hold time(3)		7			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge
(4) fSPIclk = 1/2tLO/HI with tLO/HI = max(tVALID,CO + tSU,PI, tSU,CI + tVALID,PO).

7.15.2 SPI Timing Diagram

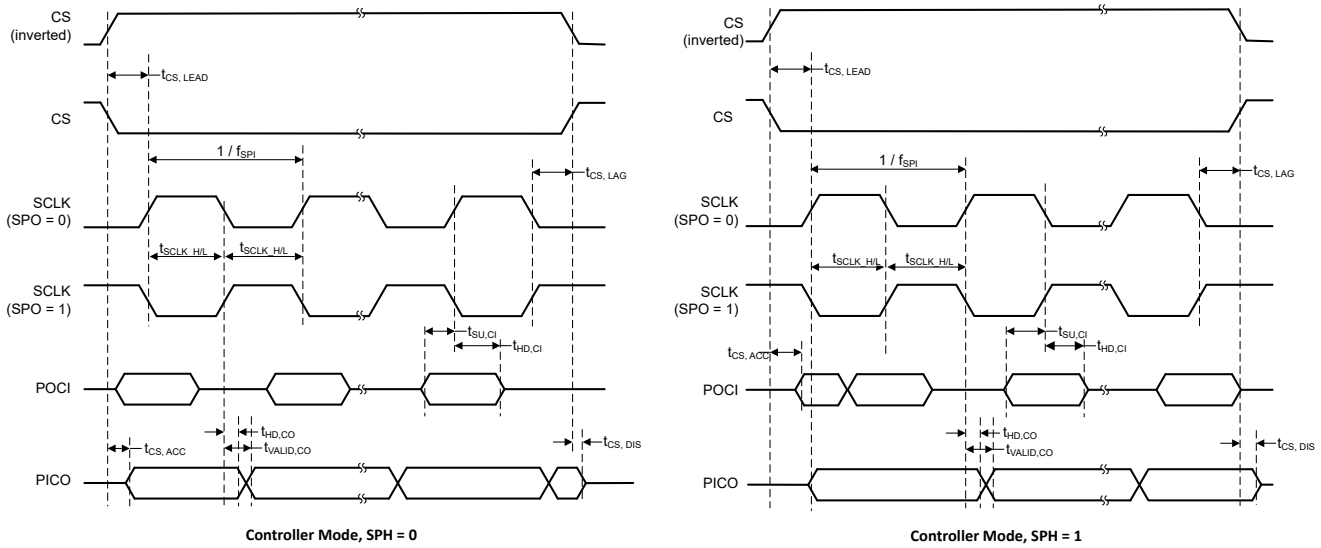

Figure 7-4. SPI timing diagram - Controller Mode

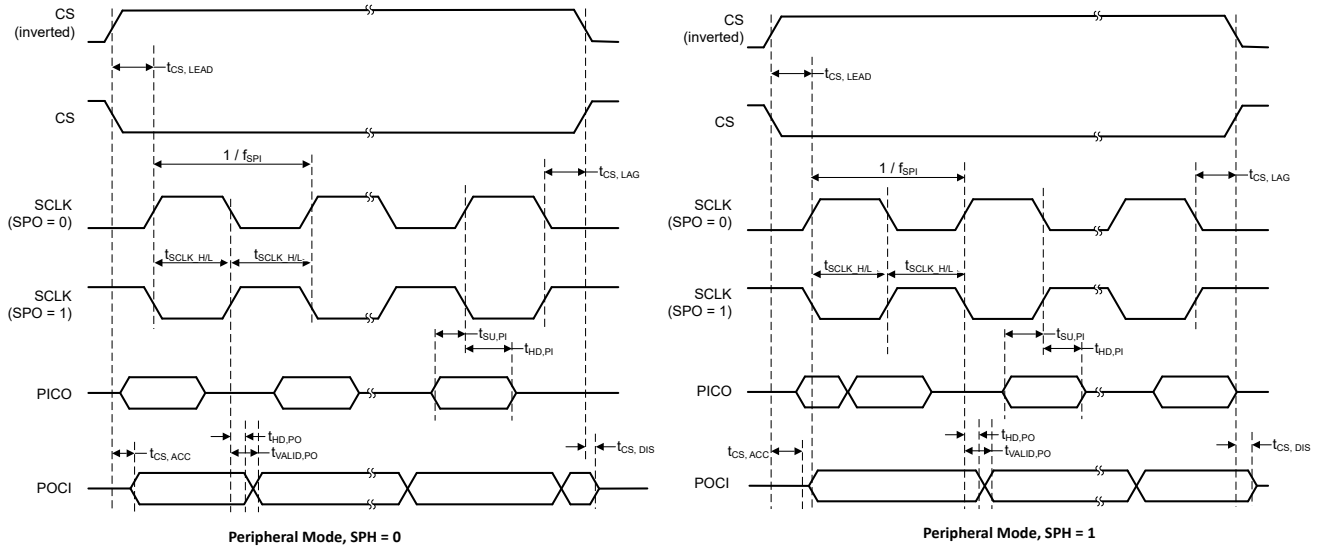

Figure 7-5. SPI timing diagram - Peripheral Mode

7.16 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency				32	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				4	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.17 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 64MHz (1)	15.625			ns
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 32MHz	31.25			ns
			1			$t_{TIMxCLK}$
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 64MHz(1)	0.01563		1024	us
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 32MHz	0.03125		2048	us
			1		65536	$t_{TIMxCLK}$

(1) $f_{TIMxCLK}$ = 64MHz only applies to TIMA0 with clock doubler configured

7.18 Emulation and Debug

7.18.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

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8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

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8.1 Overview

MSPM0H321x microcontrollers (MCUs) are part of the MSP highly-integrated 5V power supply and 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ core platform operating at up to 32MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 4.5V.

The MSPM0H321x devices provide up to 64KB embedded flash program memory with 8KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy up to -2.1 to 1.6%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.6-Msps ADC with VDD as the voltage reference, and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as one 16-bit advanced timer, four 16-bit general purpose timer, one windowed watchdog timer, one independent watchdog timer, a real-time clock (RTC) and a variety of communication peripherals including three UART, one SPI, and two I^2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration enabling customers to find the MCU that meets their project needs. The architecture combined with extensive low-power modes is optimized to achieve extended battery life in portable measurement applications.

MSPM0H321x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad™ kit available for purchase and design files for a target-socket board. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0H-Series 32MHz Microcontrollers Technical Reference Manual*.

8.2 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized 32-bit CPU that delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supports clock frequencies from 32kHz to 32MHz
  - ARMv6-M Thumb instruction set (little endian) with 32-cycle 32x32 fast multiply instruction
- Prefetch logic to improve sequential code execution, and I-cache with 2 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail chaining

8.3 Operating Modes

MSPM0H MCUs provide four main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP and STANDBY. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode.

To further balance performance and power consumption, MSPM0H devices implement two power domains: PD1 (for the CPU, memories, and high performance peripherals), and PD0 (for low speed, low power peripherals). PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes.

8.3.1 Functionality by Operating Mode (MSPM0H321x)

Table 8-1 lists the supported functionality in each operating mode.

Functional key:

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- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but it is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained.

Table 8-1. Supported Functionality by Operating Mode

Operating Mode		RUN			SLEEP			STOP		STANDBY	
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT[1]	DIS	DIS	DIS
	LFOSC	EN									
Clocks	CPUCLK	32M	32k	32k	DIS						
	MCLK to PD1	32M	32k	32k	32M	32k	32k	DIS			
	ULPCLK to PD0	32M	32k	32k	32M	32k	32k	4M[1]	32k		DIS
	ULPCLK to TIMG14, TIMG8	32M	32k	32k	32M	32k	32k	4M[1]	32k		
	MFCLK	OPT	DIS		OPT	DIS		OPT	DIS		
	LFCLK	32k									DIS
	LFCLK to TIMG14, TIMG1,TIMG2,TIMG8, TIMA0	32k									
	MCLK Monitor	OPT									DIS
	LFCLK Monitor	OPT									
PMU	POR Monitor	EN									
	BOR Monitor	EN									
	Core Regulator	Full drive								Low drive	
Core Functions	CPU	EN			DIS						
	DMA	OPT						NS (triggers supported)			
	Flash	EN						OPT		DIS	
	SRAM	EN						OPT		DIS	
PD1 Peripherals	SPI0	OPT						DIS			
	CRC	OPT						DIS			
PD0 Peripherals	TIMG14	OPT									
	TIMG1	OPT									DIS
	TIMG2	OPT									DIS
	TIMG8	OPT									DIS
	TIMA0	OPT									DIS
	UART0	OPT									DIS
	UART1	OPT									DIS
	UART2	OPT									DIS
	I2C0	OPT									DIS
	I2C1	OPT									DIS
	GPIOA	OPT									OPT[2]
	GPIOB	OPT									OPT[2]
	WWDT0	OPT									OPT[2]

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Table 8-1. Supported Functionality by Operating Mode (continued)

Operating Mode		RUN			SLEEP			STOP		STANDBY	
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1
Analog	ADC0	OPT							NS (triggers supported)		
	VREF	OPT							NS		
	Temperature Sensor	OPT								OFF	
IOMUX and IO Wakeup		EN									
Wake Sources		N/A			ANY IRQ			PD0 IRQ			

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32kHz as it was in RUN2.
(2) When using the STANDBY1 policy for STANDBY, only TIMG14 is clocked. These PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

8.4 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.5 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32kHz)
- **SYSOSC**: Internal high-frequency oscillator (32MHz)
- **LFXT**: Low frequency, low power crystal oscillator (32kHz typical frequency)
- **HFXT**: High frequency crystal oscillator (4-32MHz typical frequency)
- **LFCKIN** : low-frequency digital clock input (32KHz)
- **HFCKIN**: high-frequency digital clock input (4 to 32MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC or LFCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **HFCLK**: High frequency external clock
- **HSCLK**: High speed clock derived from HFCLK, available in RUN and SLEEP mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **RTCCLK**: Fixed 32kHz clock direct to RTC

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- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes

For more details, see the CKM chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.6 DMA_B

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA_B in these devices support the following key features:

- 3 DMA transfer channel
  - 2 full-feature channels, supporting repeated transfer modes
  - 1 basic channel, supporting single transfer mode
- Configurable DMA channel priorities
- Direct peripheral to DMA trigger is supported from ADC, UART, SPI or timer triggers.
- Byte (8-bit), short word (16-bit) and word (32-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications
- Gather mode

DMA_B Channel Features shows the DMA features that are supported and the corresponding DMA channel numbers.

Table 8-2. DMA_B Channel Features

DMA Feature	DMA_B	
	Full-Feature Channel	Basic Channel
Channel Number	0, 1	2
Repeated mode	✓	–
Table & fill mode	✓	–
Gather mode	✓	–
Early IRQ notification	✓	–
Auto enable	✓	✓
Long long (128-bit) transfer	✓	✓
Stride mode	✓	✓
Cascading channel support	✓	✓

DMA Trigger Mapping lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-3. DMA Trigger Mapping

DMACTL.DMATSEL	TRIGGER SOURCE
0	Software
1	Generic Subscriber 0 (FSUB_0)
2	Generic Subscriber 0 (FSUB_1)
9	UART0 PUBLISHER 1
10	UART0 PUBLISHER 2
13	UART2 PUBLISHER 1
14	UART2 PUBLISHER 2

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Table 8-3. DMA Trigger Mapping (continued)

DMACTL.DMATSEL	TRIGGER SOURCE
7	SPI0 PUBLISHER 1
8	SPI0 PUBLISHER 2
5	I2C1 PUBLISHER 1
6	I2C1 PUBLISHER 2
3	I2C0 PUBLISHER 1
4	I2C0 PUBLISHER 2
15	ADC0 EVT g
11	UART1 PUBLISHER 1
12	UART1 PUBLISHER 2

8.7 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) that are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: GPIO interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: ADC trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the Event chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

Table 8-4. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish the event to another entity (or entities, in the case of a splitter route). An entity can be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
5	Generic event channel 5 selected	1 : 1
6	Generic event channel 6 selected	1 : 2 (splitter)
7	Generic event channel 6 selected	1 : 2 (splitter)

8.8 Memory

8.8.1 Memory Organization

Table 8-5 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

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Table 8-5. Memory Organization

Memory Region	Subregion	MSPM0C1105	MSPM0C1106
Code (Flash)	Flash	32KB(1) 0x0000.0000 to 0x0000.7FFF	64KB(1) 0x0000.0000 to 0x0000.FFFF
SRAM (SRAM)	SRAM	8KB 0x2000.0000 to 0x2000.1FFF	8KB 0x2000.0000 to 0x2000.1FFF
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	Flash	0x0040.0000 to 0x0040.7FFF	0x0040.0000 to 0x0040.FFFF
	NONMAIN (2)	512 bytes 0x41C0.0000 to 0x41C0.07FF	512 bytes 0x41C0.0000 to 0x41C0.07FF
	FACTORY	0x41C4.0000 to 0x41C4.03FF	0x41C4.0000 to 0x41C4.03FF
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

(1) First 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program/erase cycles.
(2) Modifying the NONMAIN configuration region can result in permanent device lockout if the region is not reprogrammed with a valid configuration. Valid configurations must include accurate CRC values and appropriate debug policies in order to maintain device access.

8.8.2 Peripheral File Map

Table 8-6 lists the available peripherals and the register base address for each.

Table 8-6. Peripherals Summary

Peripheral name	Base Address	Size
VREF	0x40030000	0x00001F00
WWDT0	0x40080000	0x00001500
TIMG14	0x40084000	0x00001F00
TIMG1	0x40086000	0x00001F00
TIMG2	0x40088000	0x00001F00
TIMG8	0x40090000	0x00001F00
LFSS	0x40094000	0x00001600
RTC_B	0x40094000	0x00001600
IWDT	0x40094000	0x00001600
GPIOA	0x400A0000	0x00001F00
GPIOB	0x400A2000	0x00001F00
SYSCTL	0x400AF000	0x00003100
DEBUGSS	0x400C7000	0x00001F00
EVENTLP	0x400C9000	0x00003000
FLASHCTL	0x400CD000	0x00002000
I2C0	0x400F0000	0x00001F00
I2C1	0x400F2000	0x00001F00
UART1	0x40100000	0x00001F00
UART2	0x40102000	0x00001F00
UART0	0x40108000	0x00001F00
CPUSS	0x40400000	0x00001F00
WUC	0x40424000	0x00000500
IOMUX	0x40428000	0x00002000
DMA	0x4042A000	0x00001F00
CRC	0x40440000	0x00002000
SPI0	0x40468000	0x00001F00

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Table 8-6. Peripherals Summary (continued)

Peripheral name	Base Address	Size
ADC0	0x4055A000	0x00001000
TIMA0	0x40860000	0x00001F00

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8.8.3 Peripheral Interrupt Vector

Interrupt Vector Number shows the IRQ number for each peripheral.

Table 8-7. Interrupt Vector Number

Peripheral name	NVIC IRQ
SYSCTL	0
DEBUGSS	1
TIMG8	2
UART1	3
ADC0	4
UART2	8
SPI0	9
UART0	15
TIMG14	16
TIMG2	17
TIMA0	18
TIMG1	19
GPIOA	22
GPIOB	23
I2C0	24
I2C1	25
FLASHCTL	27
WWDT0	29
LFSS	30
RTC_B	30
IWDT	30
DMA	31

8.9 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 100,000 program/erase cycles on 32 selected sectors of the flash memory, with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32kB support 100,000 cycles on the entire flash memory)

For a complete description of the flash memory, see the NVM chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

8.10 SRAM

MSPM0Hxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY operating modes. A write protection mechanism is provided to allow the application to dynamically write protect the SRAM memory with 1KB resolution. Write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

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8.11 GPIO

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A and Port B GPIO peripheral, these devices support up to 45 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set, clear, or toggle multiple bits without the need of a read-modify-write construct in software
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

8.12 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO pad configuration registers allow for programmable drive strength, speed, pullup, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

8.13 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.6-Msps with greater than 10-bit ENOB
- Up to 27 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- Software selectable reference:
  - Configurable internal dedicated ADC reference voltage of 4.05V (VREF)
  - MCU supply voltage (VDD)
  - Support for bringing in an external reference on VREF+/- device pins
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-8. ADC0 Channel Mapping

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME
0	A0	16	A16
1	A1	17	A17
2	A2	18	A18
3	A3	19	A19
4	A4	20	A20
5	A5	21	A21
6	A6	22	A22
7	A7	23	A23
8	A8	24	A24
9	A9	25	A25
10	A10	26	A26
11	A11	27	Reserved

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Table 8-8. ADC0 Channel Mapping (continued)

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME
12	A12	28	*Temperature Sensor*
13	A13	29	VREF
14	A14	30	Reserved
15	A15	31	*Supply/Battery Monitor*

Italicized signal names are internal to the SoC. These signals are used for internal peripheral interconnections.

For more details, see the ADC chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

8.14 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 4.05V internal VREF at the factory trim temperature (TS_{TRIM}). This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual for guidance on estimating the device temperature with the factory trim value.

8.15 VREF

The voltage reference module (VREF) in these devices contains a configurable voltage reference buffer dedicated for the on-board ADC.

VREF features include:

- 4.05V internal reference
- Internal reference supports ADC operation up to 0.9Msps at 12-bit mode

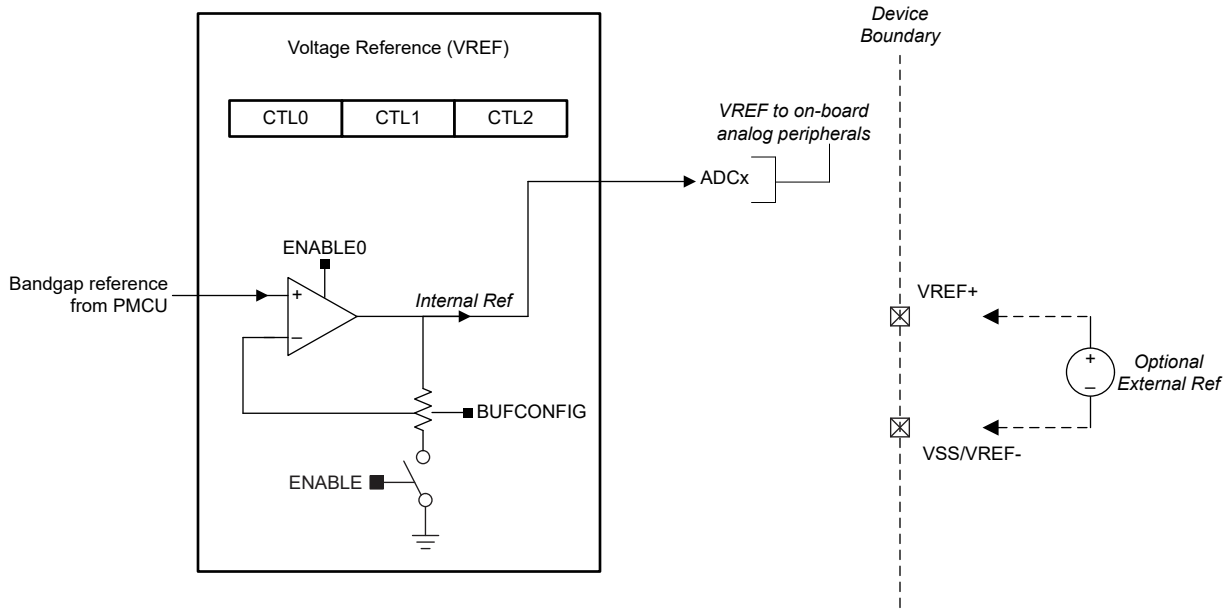

Figure 8-1. VREF module

For more details, see the VREF chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.16 Security

This device offers several security features, including:

- Debug security
- Unique Die ID
- Flexible firewalls for protecting code and data
  - Flash write-erase protection
  - Flash read-execute protection
  - Flash IP protection
  - SRAM write-execute mutual exclusion
- Secure boot
- Secure firmware update
- Customer secure code
- Cyclic redundancy checker (CRC-16) with support for custom polynomial

For more details, see the Security chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*

8.17 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for bit reversal

For more details, see the CRC chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.18 UART

The UART peripherals provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8, or 3
  - Local Interconnect Network (LIN) mode support
- Separated 4-entry transmit and receive FIFOs
- Support transmit and receive loopback mode operation
- See Table 8-9 for detail information on supported protocols

Table 8-9. UART Features

UART FEATURES	UART0 (ADV)	UART1 (MAIN)	UART2 (MAIN)
Active in stop and standby modes	Yes	Yes	Yes
Separate transmit and receive FIFOs	Yes	Yes	Yes
Support hardware flow control	Yes	Yes	Yes

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Table 8-9. UART Features (continued)

UART FEATURES	UART0 (ADV)	UART1 (MAIN)	UART2 (MAIN)
Support 9-bit configuration	Yes	Yes	Yes
Support LIN mode	Yes	No	No
Support DALI	Yes	No	No
Support IrDA	Yes	No	No
Support ISO7816 Smart Card	Yes	No	No
Support Manchester coding	Yes	No	No

For more details, see the UART chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.19 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 16 Mbits/s in both controller and peripheral modes
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode)
- Programmable data frame size from 7 bits to 16 bits (peripheral mode)
- Separated 4-entry transmit and receive FIFOs
- Supports TI mode, Motorola mode, and National Microwire format

For more details, see the SPI chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.20 I2C

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
- Separated 8-entry transmit and receive FIFOs
- Support SMBus 3.0 with PEC, ARP, timeout detection, and host support
- Support analog and digital glitch filter for input signal glitch suppression

For more details, see the I2C chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.21 Low-Frequency Sub System (LFSS)

The Low-Frequency Sub-System (LFSS) is a sub-system which combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low frequency clock (LFCLK) or need to be active during low power modes. The LFCLK has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS in this device contains following components:

- *Real Time Clock* with additional prescalar extension and timestamp captures

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- An asynchronous *IWDT*

For more details, see the LFSS chapter of the *MSPM0 C-Series Microcontrollers Technical Reference Manual*.

8.22 RTC_B

The RTC_B instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. The RTC_B provides common key features in relation to the Low-Frequency Sub System (LFSS).

Common key features of the RTC_B include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128 Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5 Hz
- Calibration for crystal offset error (up to +/- 240ppm)
- Compensation for temperature drift (up to +/- 240ppm)
- RTC clock output to pin for calibration

RTC_B Key Features #none# shows the RTC features supported in this device.

Table 8-10. RTC_B Key Features

RTC Features	RTC_B
Power enable register	-
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes
Selectable binary or binary-coded decimal (BCD) format	Yes
Leap-year correction (valid for year 1901 through 2099)	Yes
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes
Calibration for crystal offset error and crystal temperature drift (up to ±240 ppm total)	Yes
RTC clock output to pin for calibration (GPIO)	Yes
RTC clock output to pin for calibration (TIO)	-
Three -bit prescaler for heartbeat function with interrupt generation	-
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	-
RTC time stamp capture upon detection of a timer stamp event, including: • TIO event • VDD fail event	-
RTC counter lock function	-

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For more details, see the RTC chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.23 IWDT_B

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods (2ms to 2hr)

For more details, see the IWDT chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

8.24 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual

8.25 Timers (TIMx)

The timer peripherals in these devices support the following key features. For specific configuration, see Table 8-11.

Specific features for the **general-purpose timer (TIMGx)** include:

- 16-bit down, up/down, or up counter with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Support quadrature encoder interface (QEI) for positioning and movement sensing
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Cross-trigger event logic for Hall sensor inputs

Specific features for the **advanced timer (TIMAx)** include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Clock doubler to provide 2x clock source for improved timer resolution

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- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow register for load and CC register available
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to keep the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-11. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEAD-BAND	FAULT	QEI
TIMG14	PD0	16 bit	8 bit	–	4	–	–	–	–	–	–
TIMG1	PD0	16 bit	8 bit	–	2	–	–	–	–	–	–
TIMG2	PD0	16 bit	8 bit	–	2	–	–	–	–	–	–
TIMG8	PD0	16 bit	8 bit	–	2	–	–	–	–	–	Yes
TIMA0	PD0	16 bit	8 bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	–

For more details, see the timer chapters of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

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8.26 Device Analog Connections

Figure 8-2 shows the internal analog connection of the device.

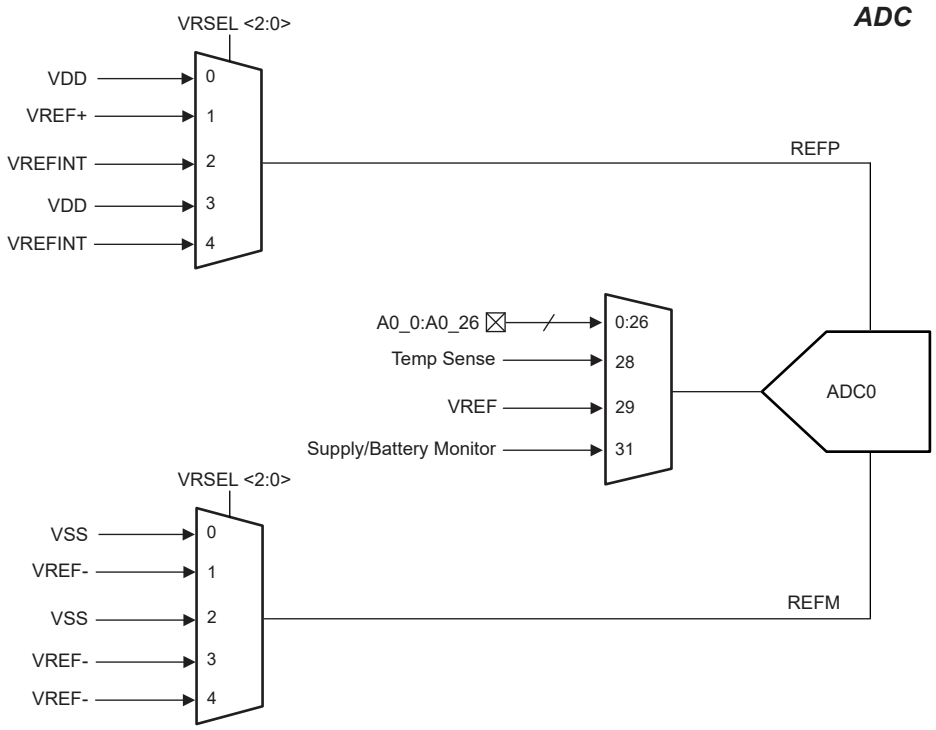

Figure 8-2. Analog Connections

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8.27 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO and provides the controls for the output driver and input path. For more information, see the IOMUX section of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-3. Not all pins have analog functions, drive strength control, and pullup resistors available. See Section 6.2 for detailed information on the features that are supported for a specific pin.

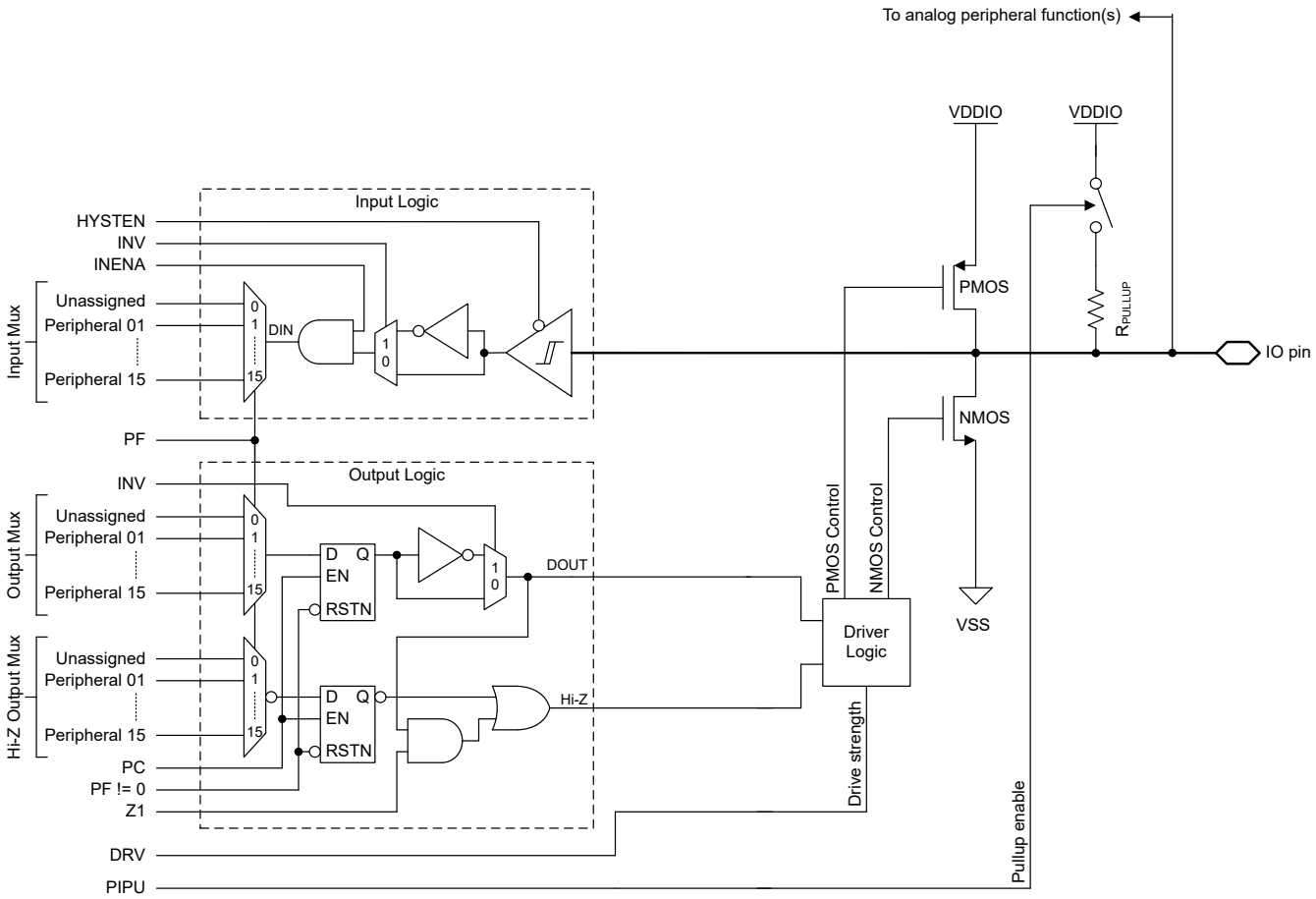

Figure 8-3. Superset Input/Output Diagram

8.28 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the debug chapter of the technical reference manual.

Table 8-12. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

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8.29 DEBUGSS

The debug subsystem (DEBUGSS) interfaces the ARM Serial Wire Debug (SWD) two-wire physical interface to multiple debug functions within the device. MSPM0 devices support debugging of processor execution and the device state. The DEBUGSS also provides a mailbox system for communicating with software through SWD.

Key features provided by the debug subsystem include:

- The ARM Serial Wire Debug (SWD) two-wire (SWDIO, SWCLK) debug interface, compatible with both TI and 3rd party debug probes
  - On-chip pullup and pulldown resistors for SWDIO and SWCLK, respectively, enabled by default
  - Support for disabling SWD functions to use SWD pins as general-purpose input/output pins
  - Support for debug on all low power modes
- Debug of the processor
  - Run, halt, and step debug support
  - 2 hardware breakpoints (BPU)
  - 1 hardware watchpoints (DWT)
  - Supporting software breakpoints
- Software-configurable peripheral behavior during processor debug
  - Ability to free run select peripherals through debug halt
  - Ability to halt select peripherals on a debug halt
  - Ability to request reset and mode changes to the PMCU
- Mailbox (DSSM) for passing data and control signals between the SWD interface and boot ROM (as well as application software)
- Support for various security features, including SWD lockout and password authenticated debugging

For more details, see the DEBUGSS chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

8.30 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. See the *Factory Constants* section of the MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual.

Table 8-13. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	DEVICEID.PARTNUM	DEVICEID.MANUFACTURER
MSPM0H3215	0x0BBA	0x17
MSPM0H3216	0x0BBA	0x17

Table 8-14. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	PART	VARIANT	Device	PART	VARIANT
MSPM0H3216SPTR	1D79	10	MSPM0H3215SPTR	1346	1A
MSPM0H3216SRGZR	1D79	12	MSPM0H3215SRGZR	1346	1C
MSPM0H3216SDGS28R	1D79	15	MSPM0H3215SDGS28R	1346	1F
MSPM0H3216SDGS20R	1D79	16	MSPM0H3215SDGS20R	1346	20

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Table 8-14. USERID (continued)

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	PART	VARIANT	Device	PART	VARIANT
MSPM0H3216SRHBR	1D79	17	MSPM0H3215SRHBR	1346	21
MSPM0H3216SRGER	1D79	18	MSPM0H3215SRGER	1346	22
MSPM0H3216SRUKR	1D79	19	MSPM0H3215SRUKR	1346	23

8.31 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region (see the Device Factory Constants section) which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. For more information, see the *Factory Constants* chapter of the *MSPM0 H-Series 32MHz Microcontrollers Technical Reference Manual*.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata describes these markings.

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9 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 Schematic

TI recommends connecting a combination of a 10-µF and a 0.1-µF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used but can affect the supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins (within a few millimeters).

The NRST reset pin must connect an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor.

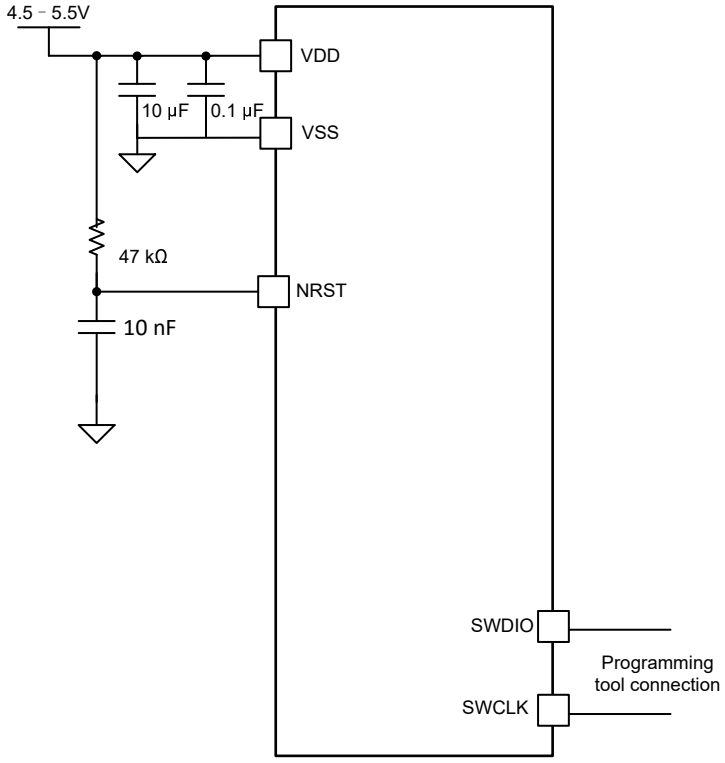

Figure 9-1. Typical Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

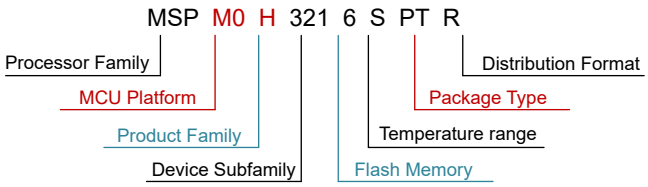

Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M0 = Arm-based 32-bit M0+
Product Family	H = 5V
Device Subfamily	321 = 32MHz frequency, ADC, RTC
Flash Memory	5 = 32KB 6 = 64KB
Temperature Range	S = –40°C to 125°C
Package Type	See Table 5-1 and www.ti.com/packaging
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

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10.2 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0H3216	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming, debugging, and EnergyTrace™ technology. The LP ecosystem includes dozens of BoosterPack™ stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Cloud Tools	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler tool chains

Code Composer Studio™ (CCS)	Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.
IAR Embedded Workbench® IDE	
Keil® MDK IDE	
GNU Arm Embedded Tool Chain	

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 H-Series 32-MHz Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the MSPM0H family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different

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devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

Errata

MSPM0H321x Mixed-Signal Microcontrollers Errata	This document describes the known exceptions to the functional specifications (advisories).

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

LaunchPad™, Code Composer Studio™, TI E2E™, EnergyTrace™, and BoosterPack™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 31, 2025 to March 31, 2026 (from Revision A (December 2025) to Revision B (March 2026)) **Page**

- Removed VSSOP32 package from datasheet..... 1
- Added table note 2 regarding proper NONMAIN configuration policy..... 52

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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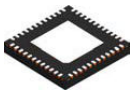
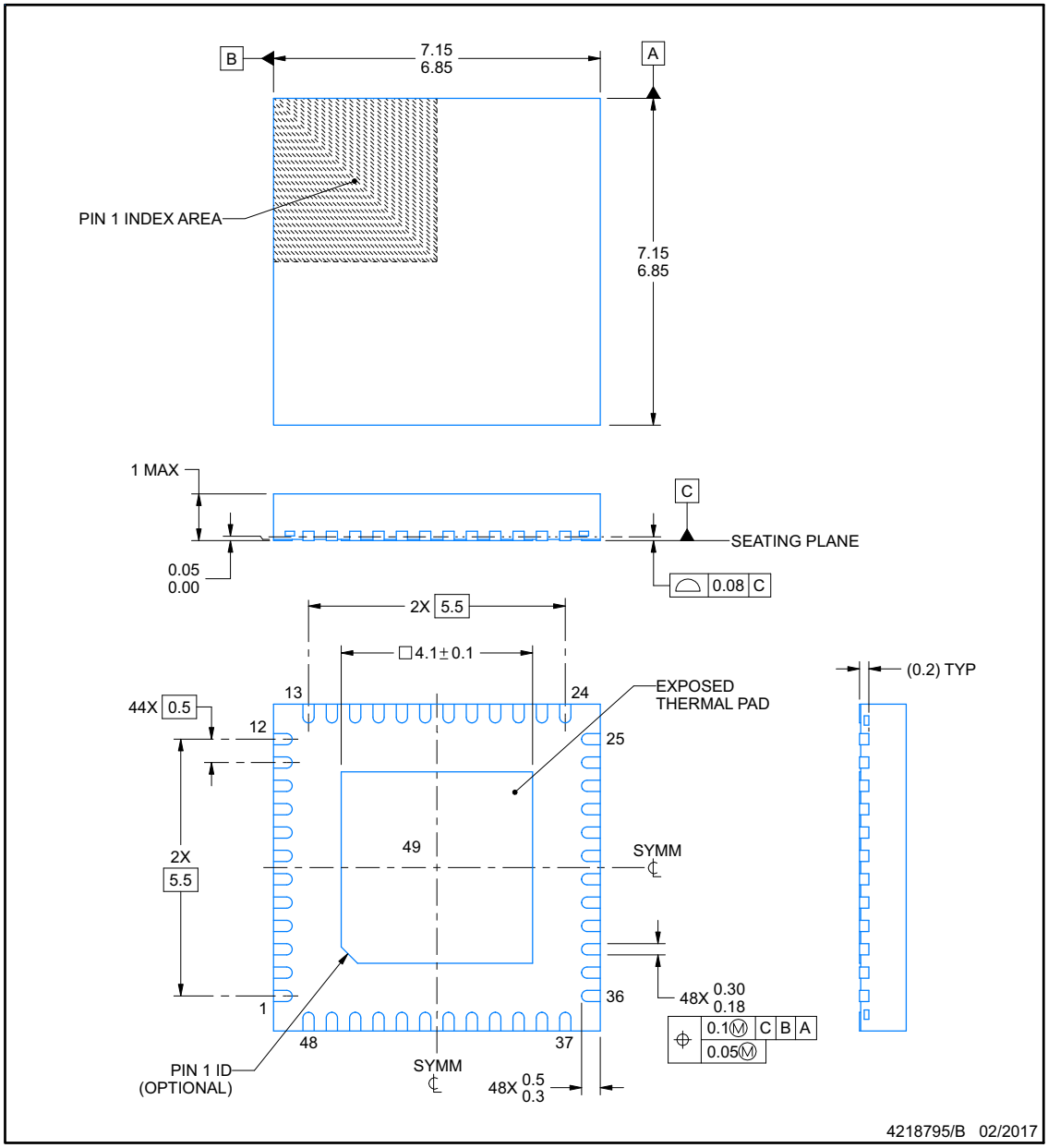
PACKAGE OUTLINE

RGZ0048B



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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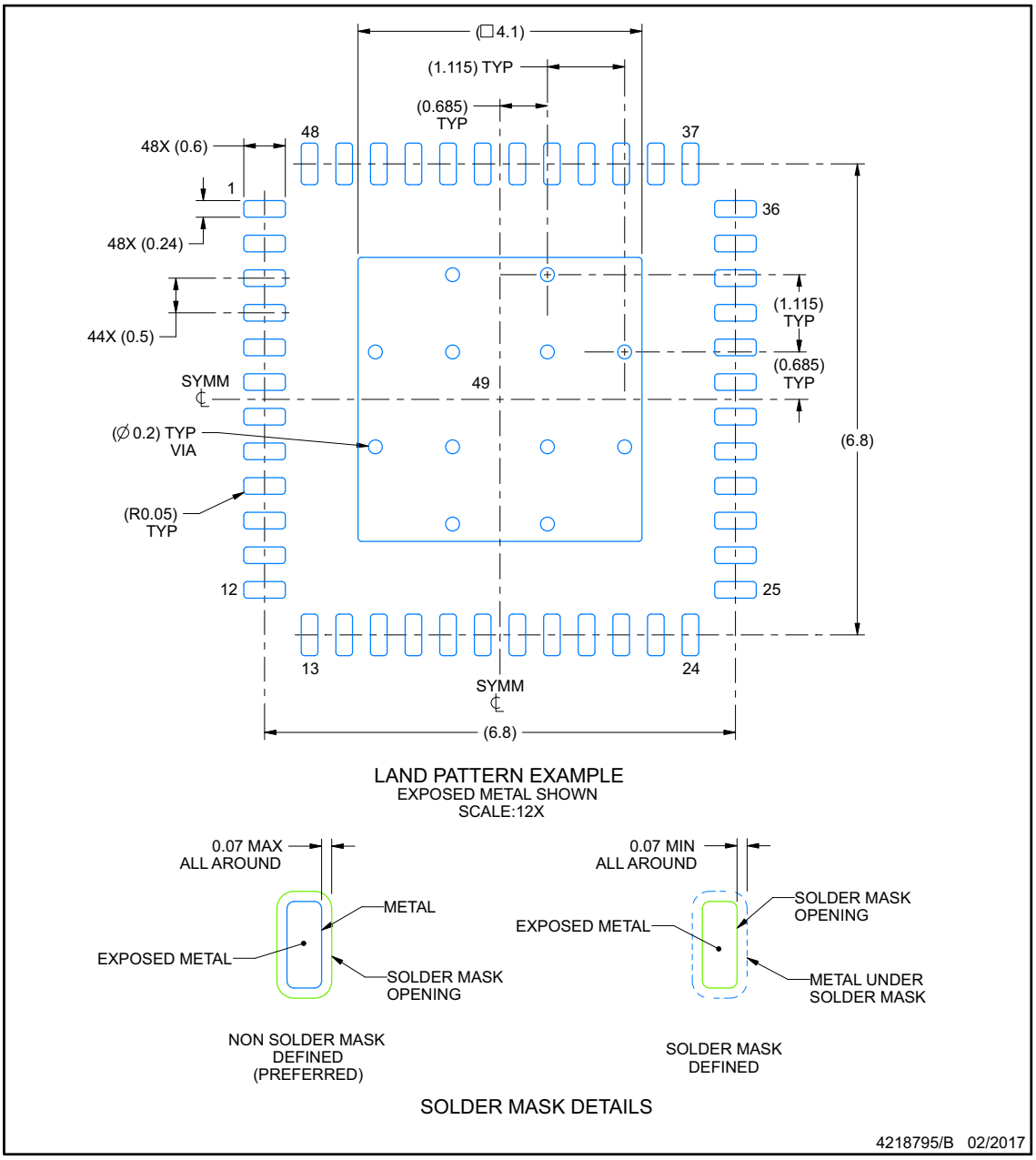
EXAMPLE BOARD LAYOUT

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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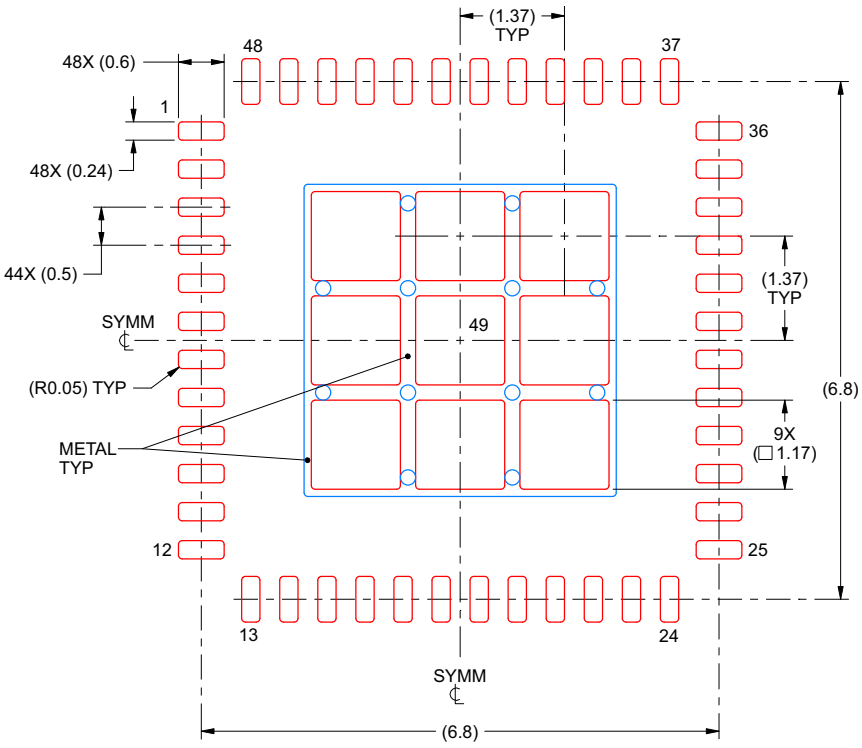
EXAMPLE STENCIL DESIGN

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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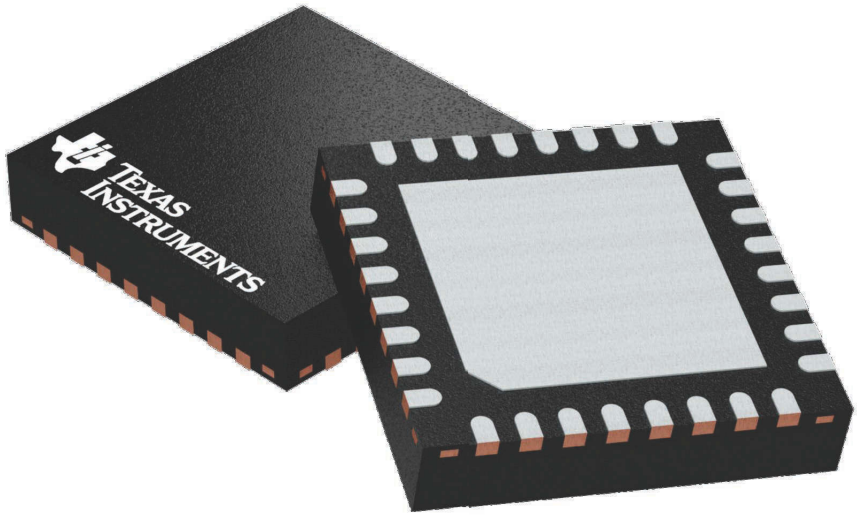
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

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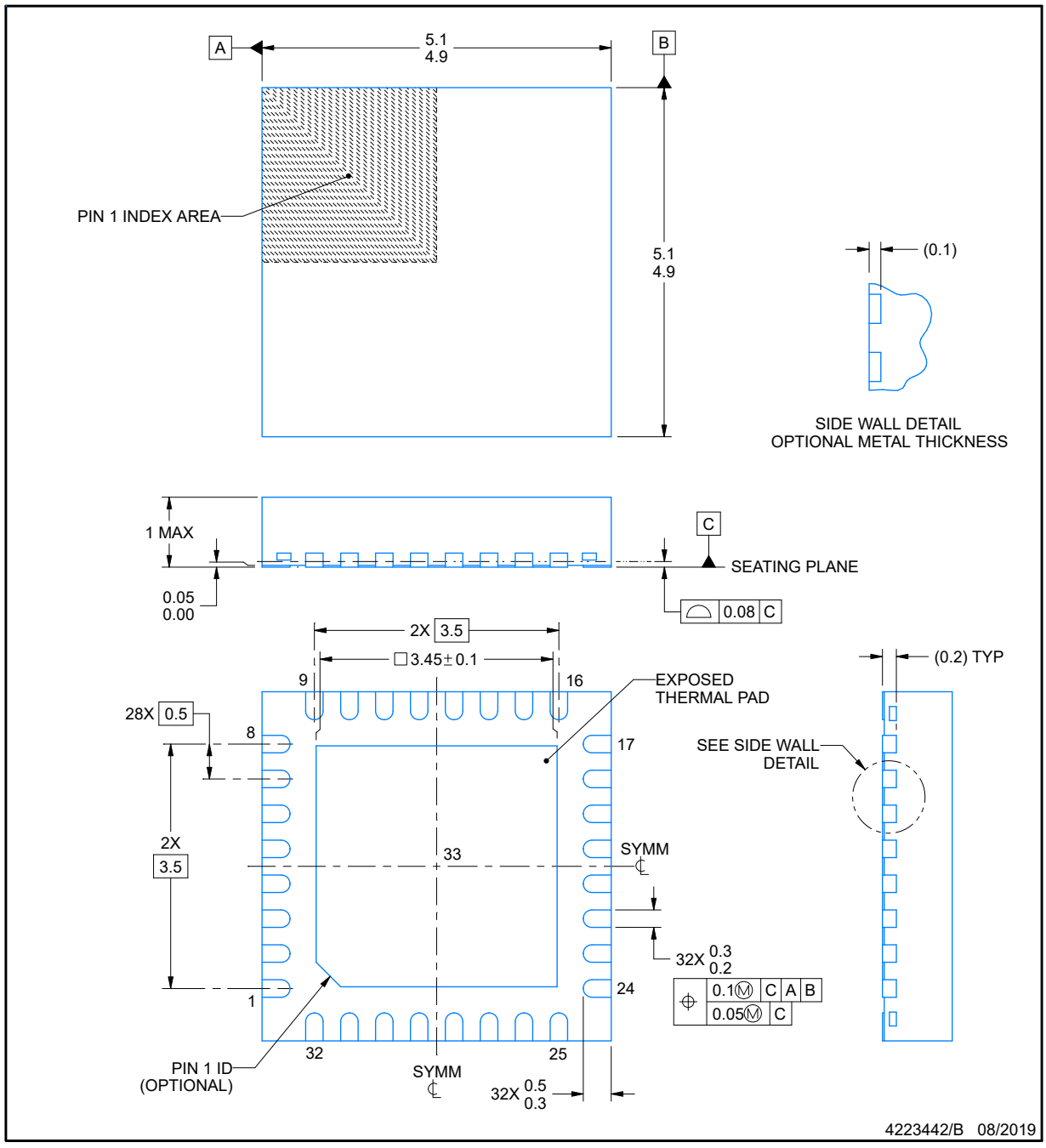
PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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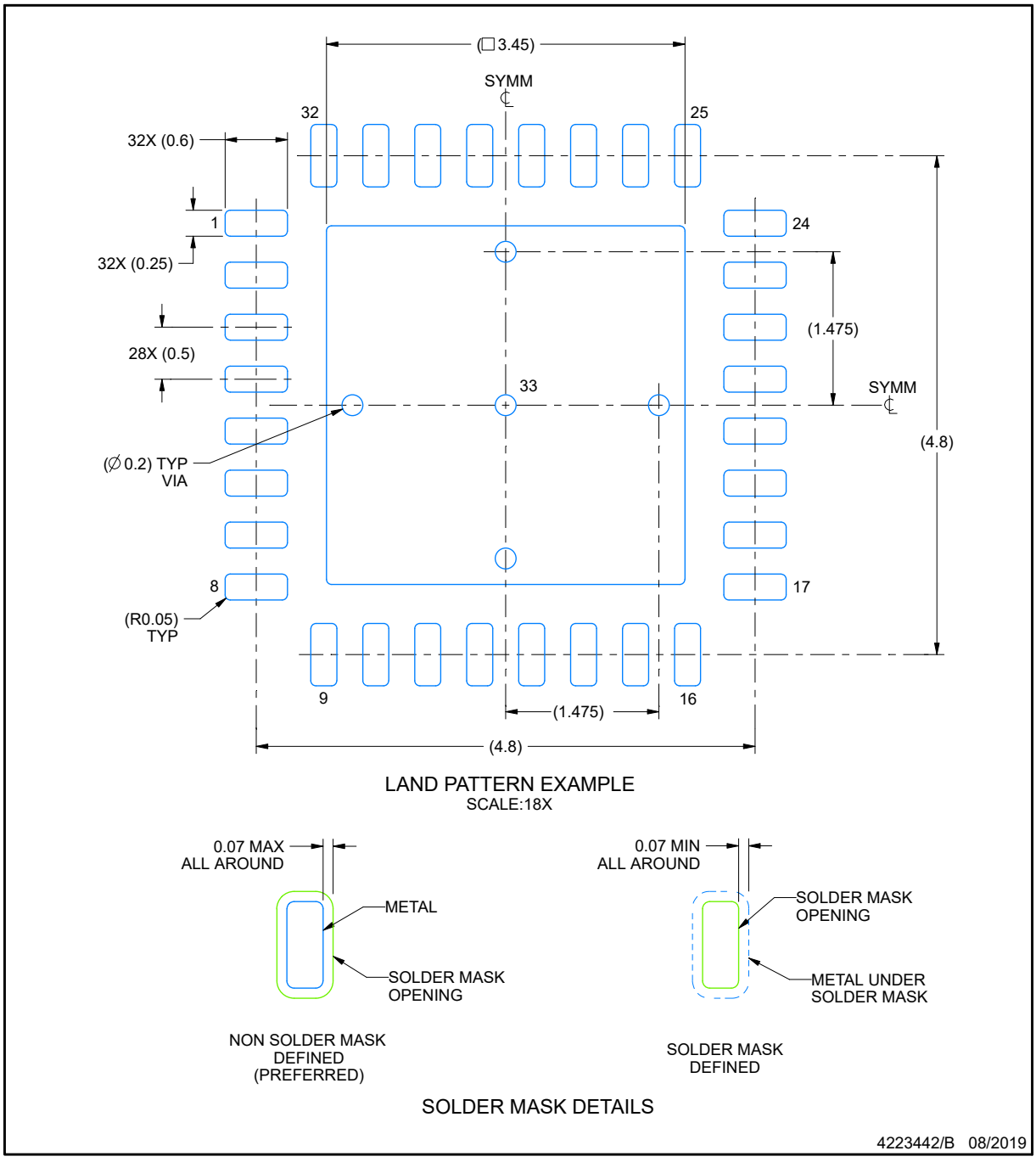
EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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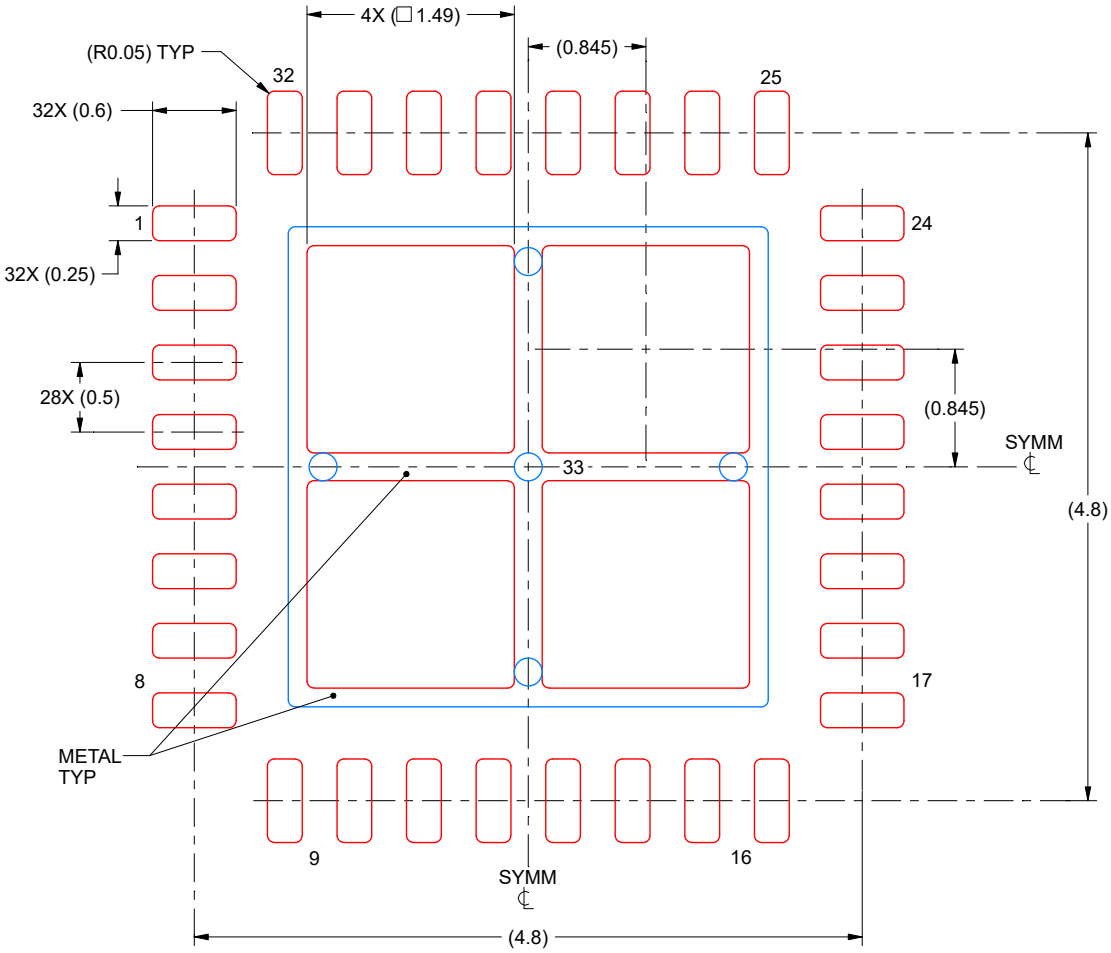
EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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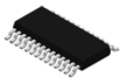
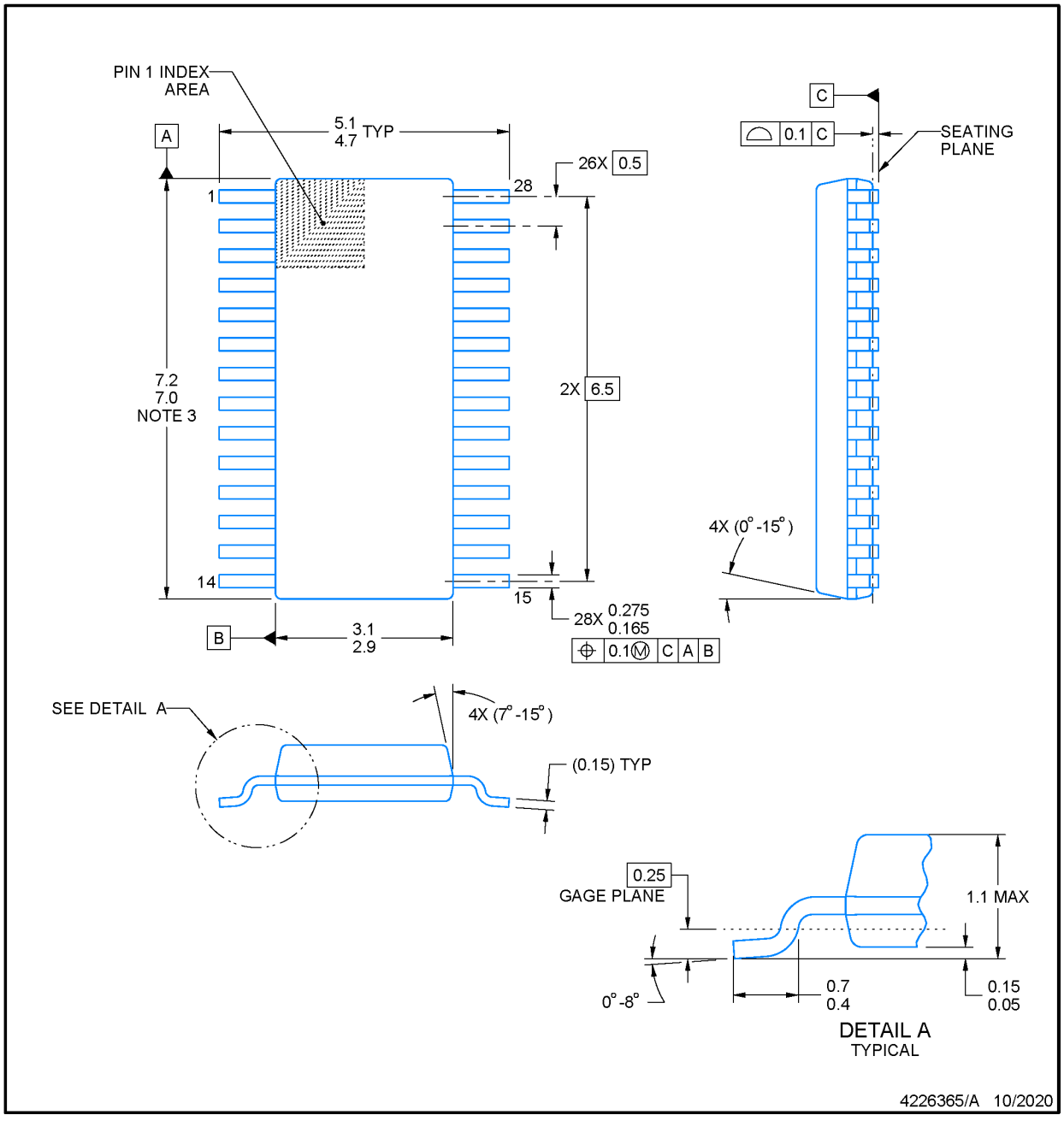
PACKAGE OUTLINE



DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

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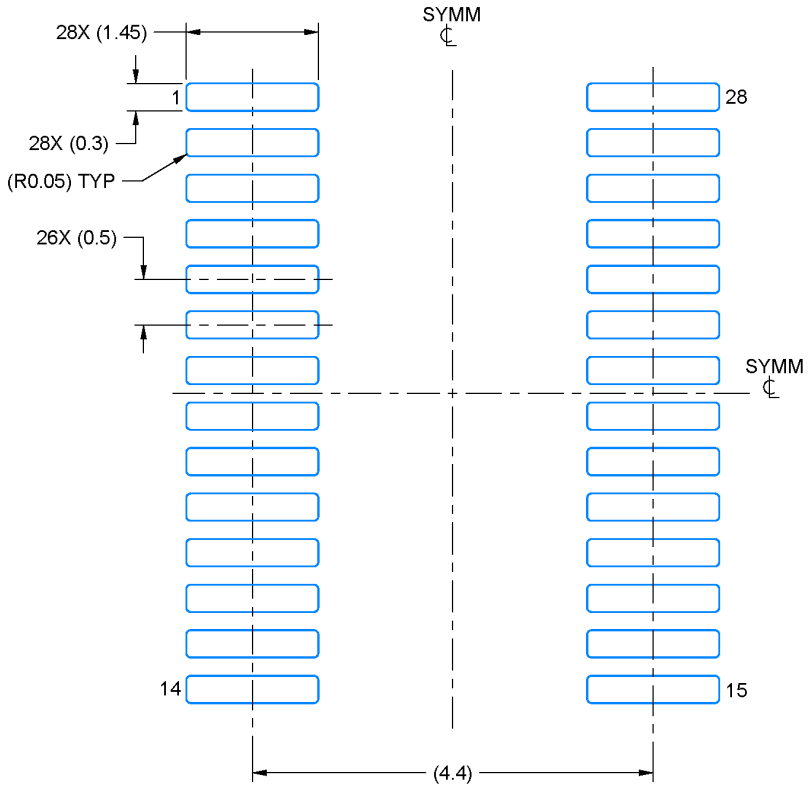
EXAMPLE BOARD LAYOUT

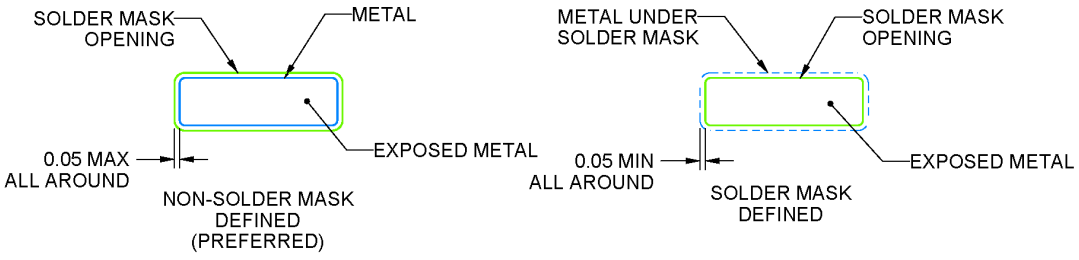
DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE: 13X



SOLDER MASK DETAILS

4226365/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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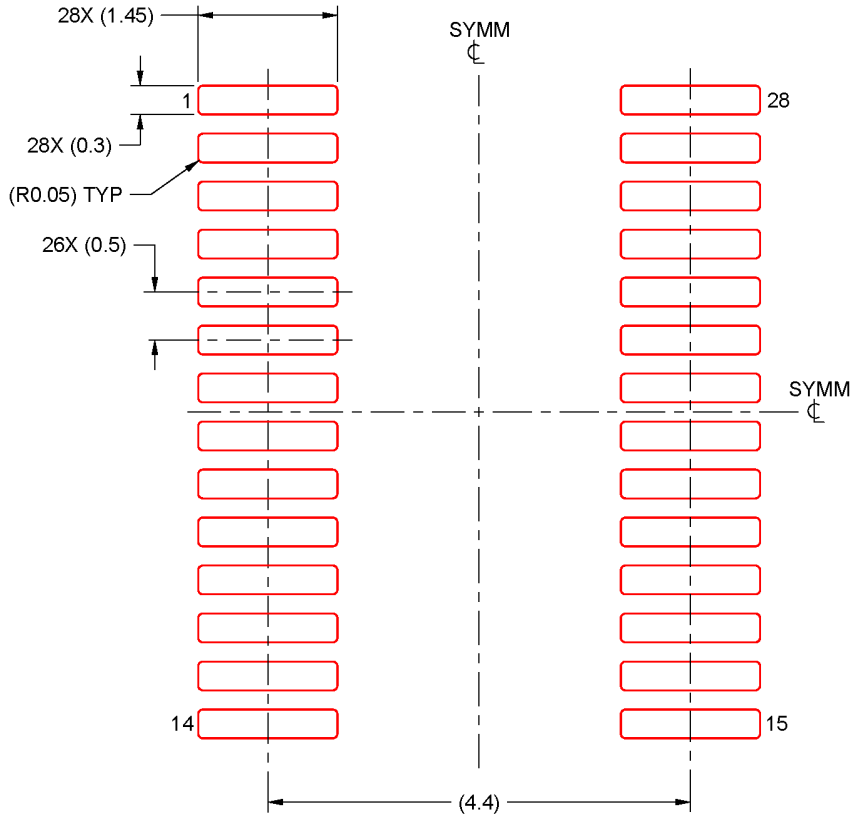
EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 13X

4226365/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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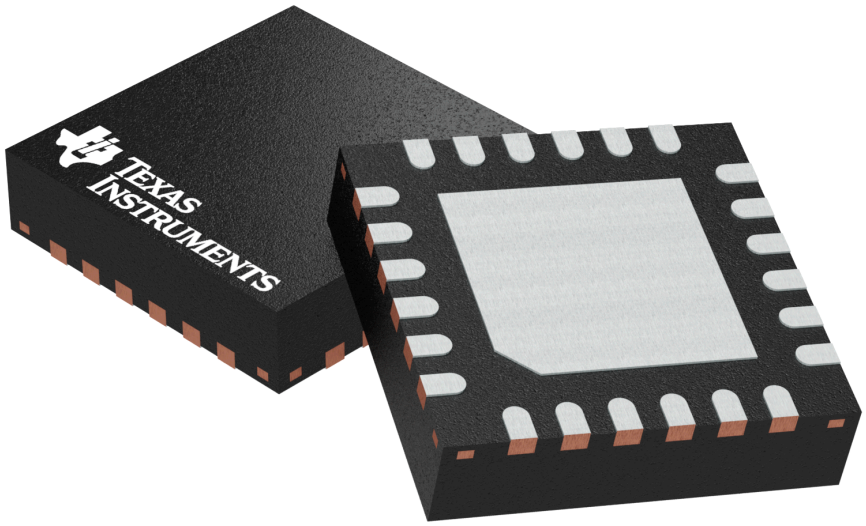
GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

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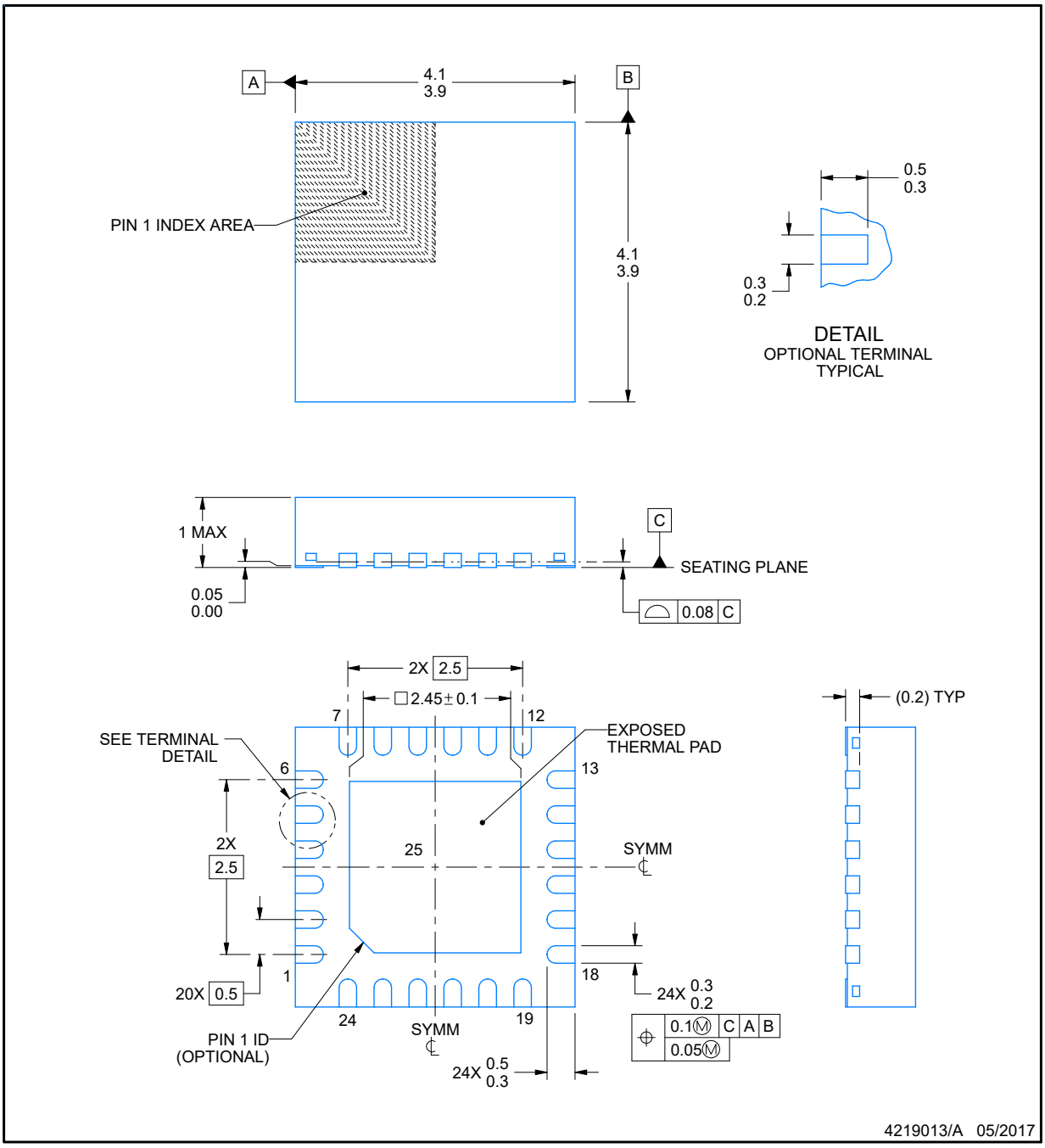
PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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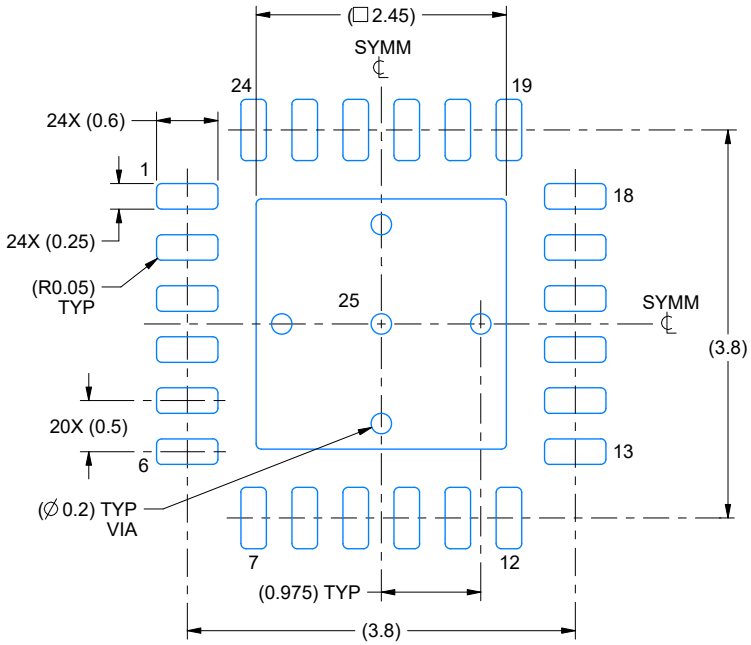
EXAMPLE BOARD LAYOUT

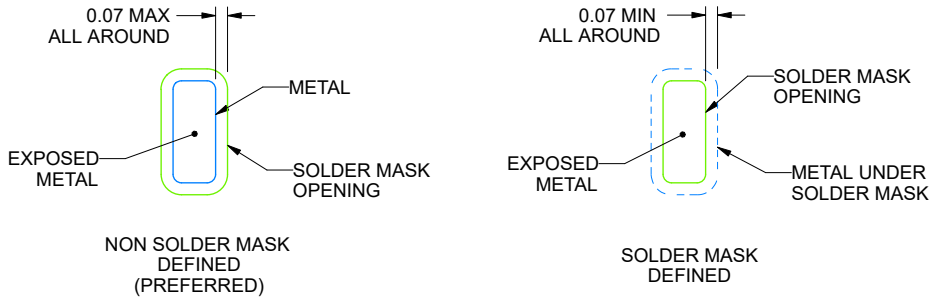
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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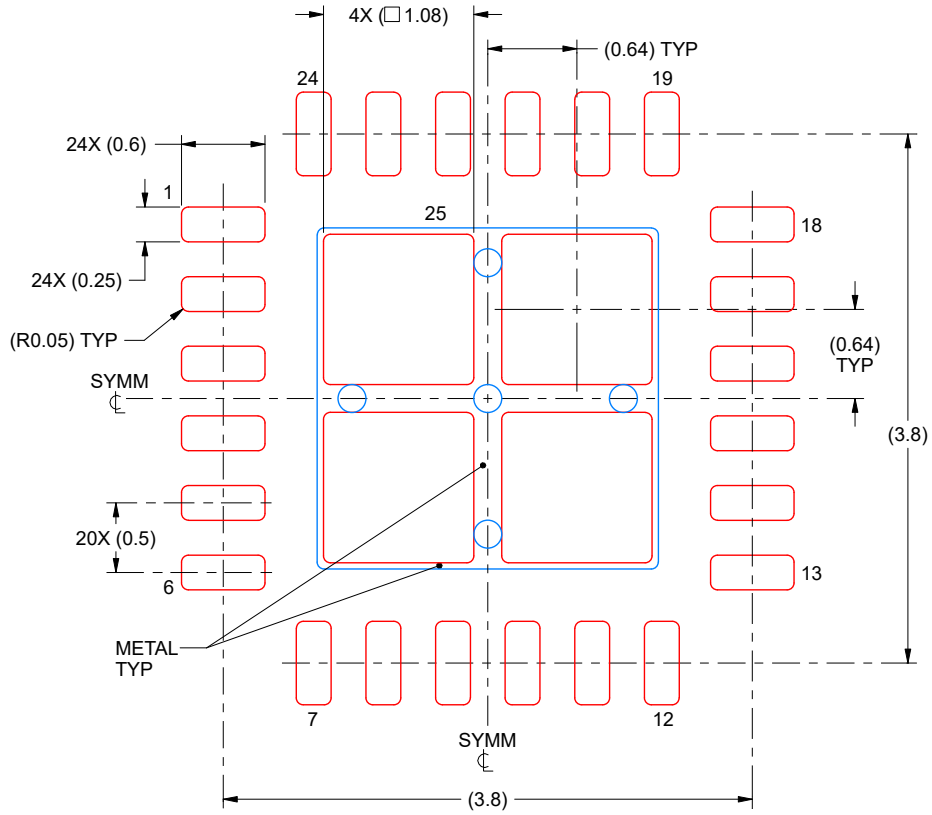
EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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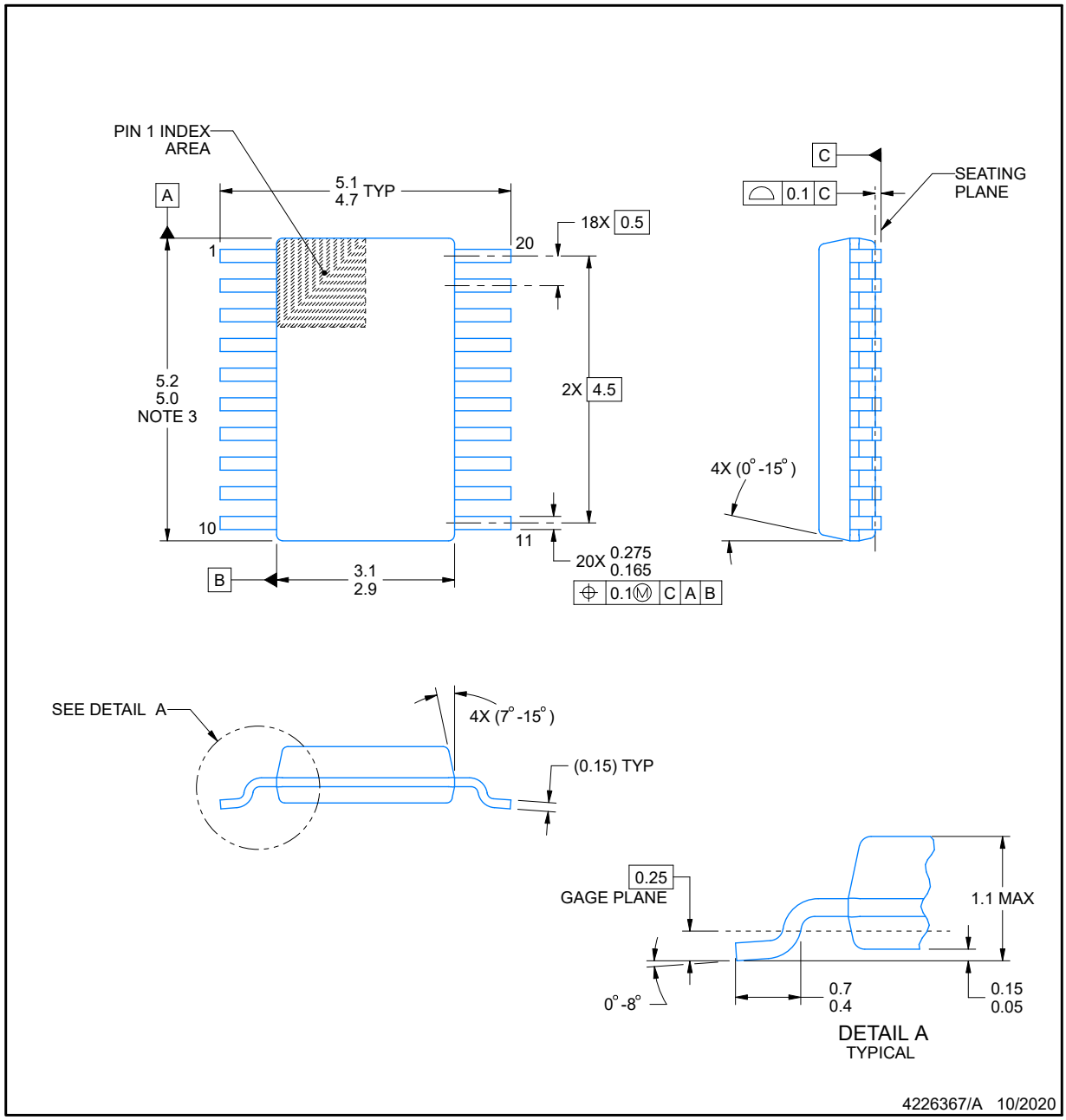
PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

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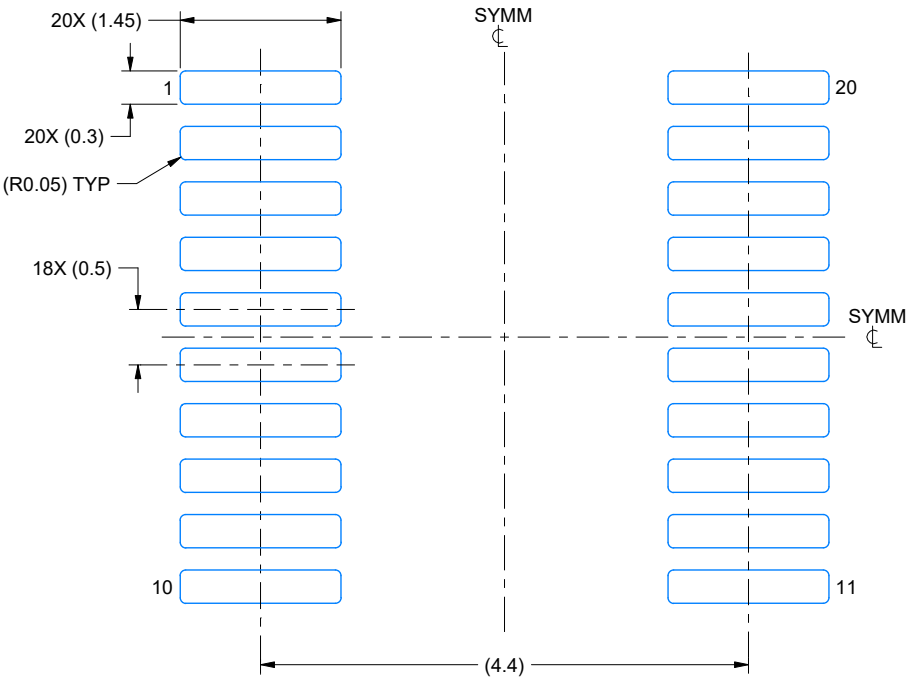
EXAMPLE BOARD LAYOUT

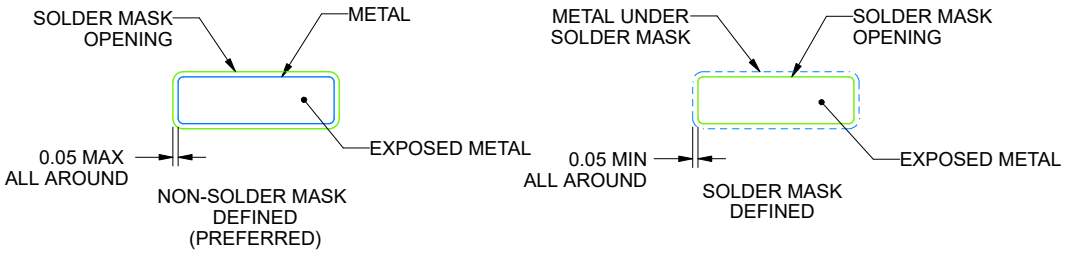
DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE: 16X



SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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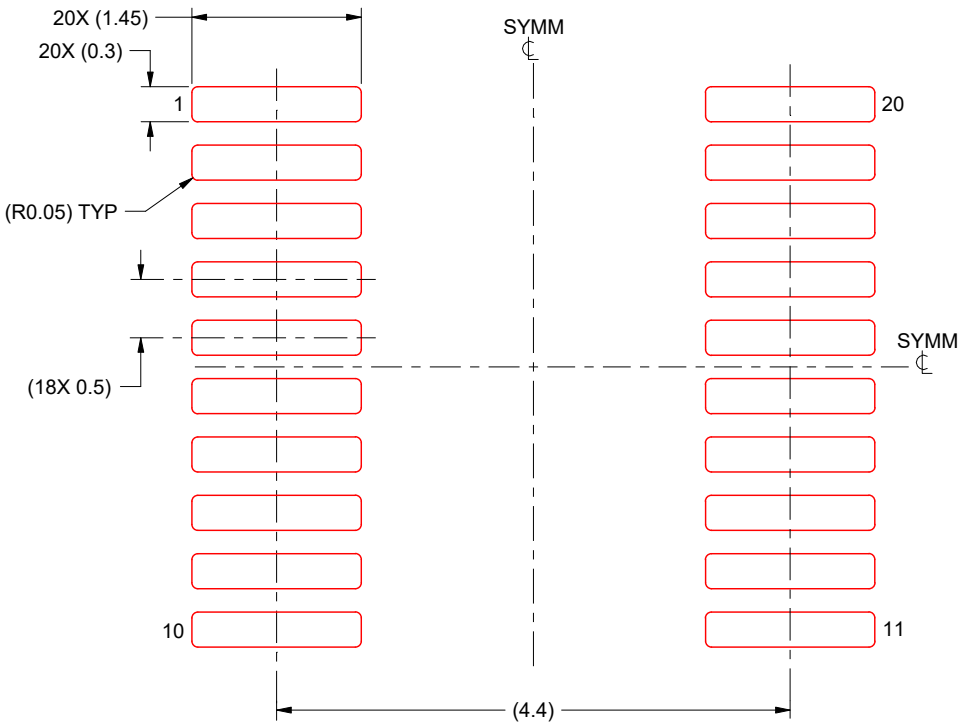
EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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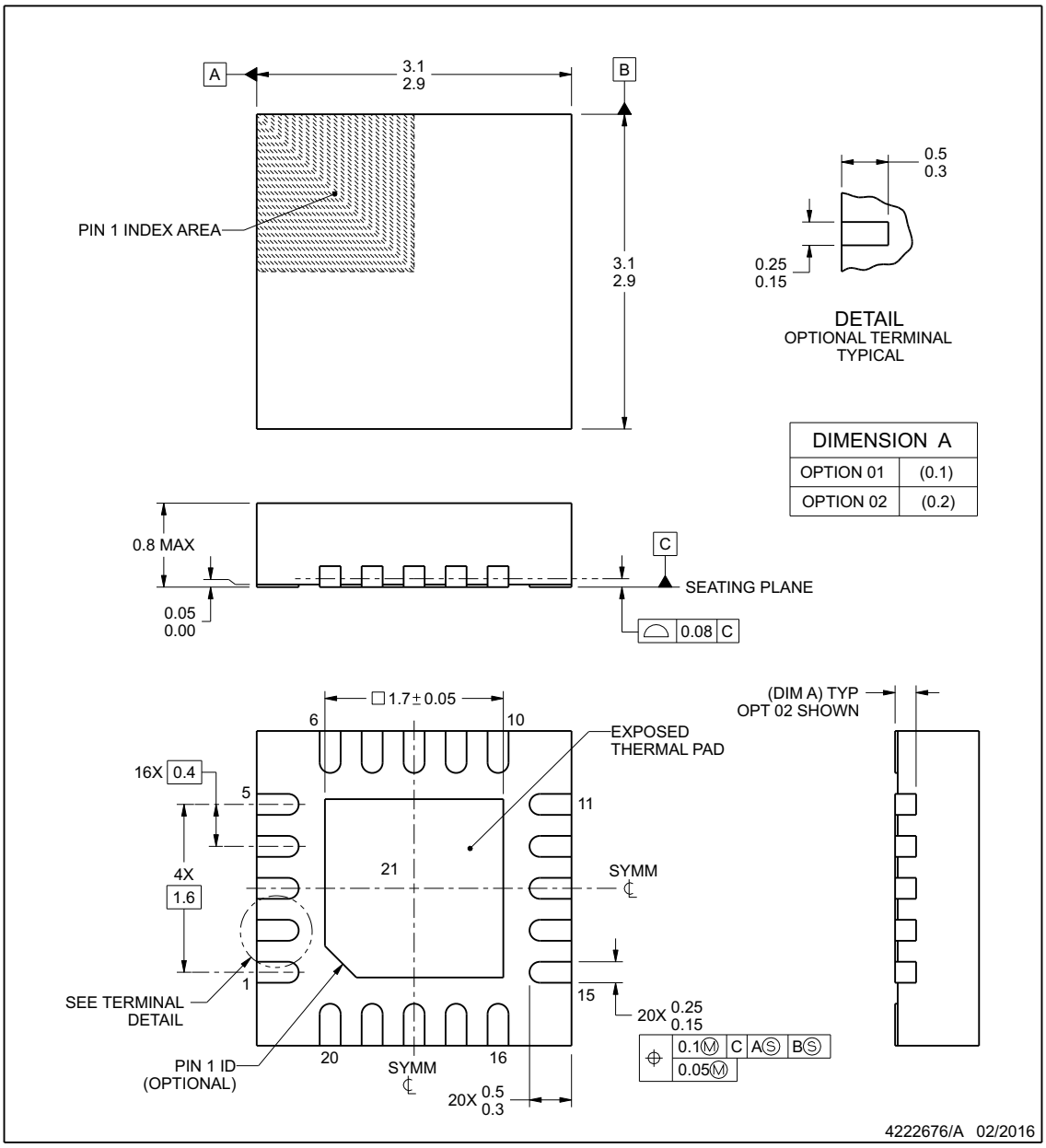
PACKAGE OUTLINE

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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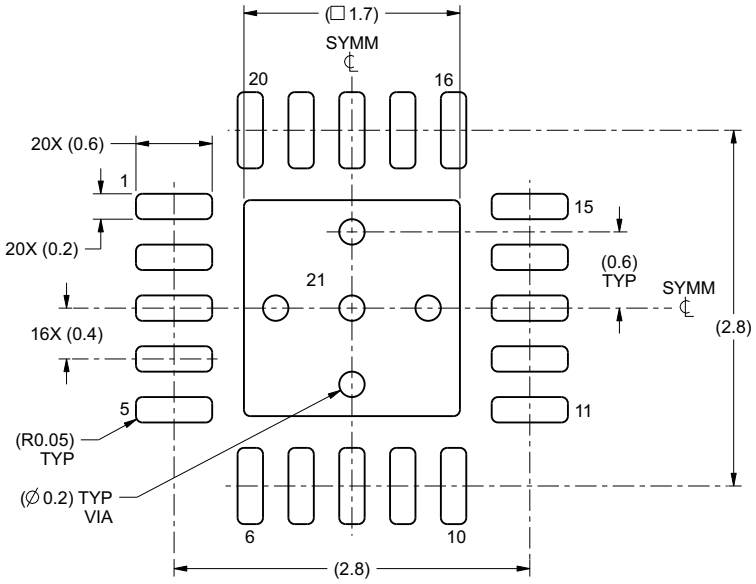
EXAMPLE BOARD LAYOUT

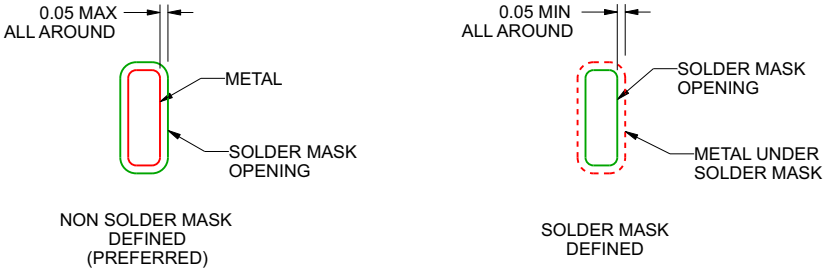
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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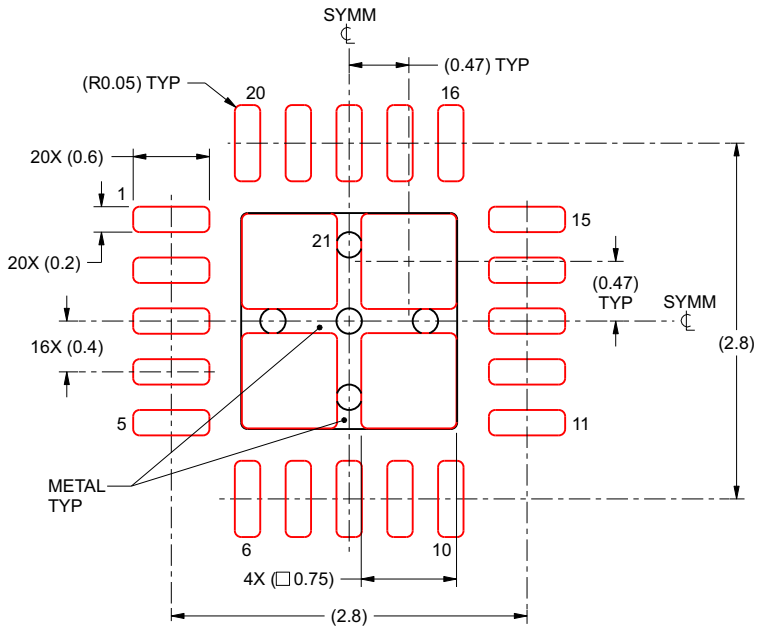
EXAMPLE STENCIL DESIGN

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSPM0H3215SPTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0H3215S
MSPM0H3215SRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MSPM0 H3215S
MSPM0H3215SRGZR	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 H3215S
MSPM0H3215SRHBR	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 H3215S
MSPM0H3215SRUKR	Active	Production	WQFN (RUK) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H3215S
MSPM0H3216SPTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0H3216S
MSPM0H3216SRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MSPM0 H3216S
MSPM0H3216SRHBR	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 H3216S
MSPM0H3216SRUKR	Active	Production	WQFN (RUK) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H3216S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSPM0H3215, MSPM0H3216 :

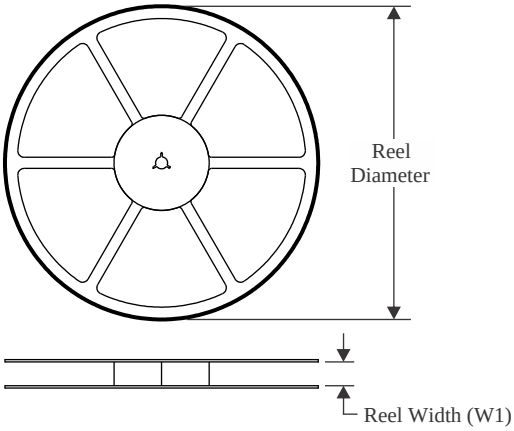
- Automotive : MSPM0H3215-Q1, MSPM0H3216-Q1

NOTE: Qualified Version Definitions:

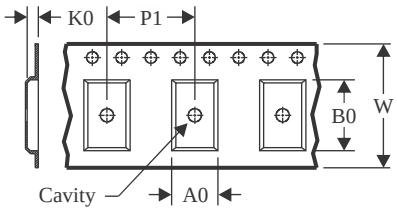
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

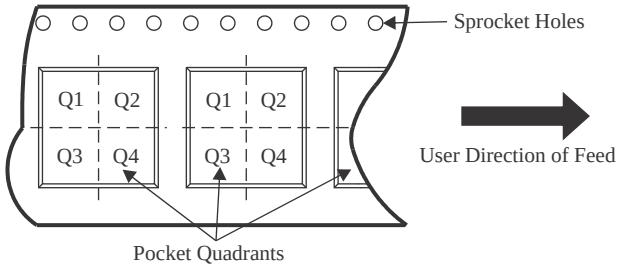


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

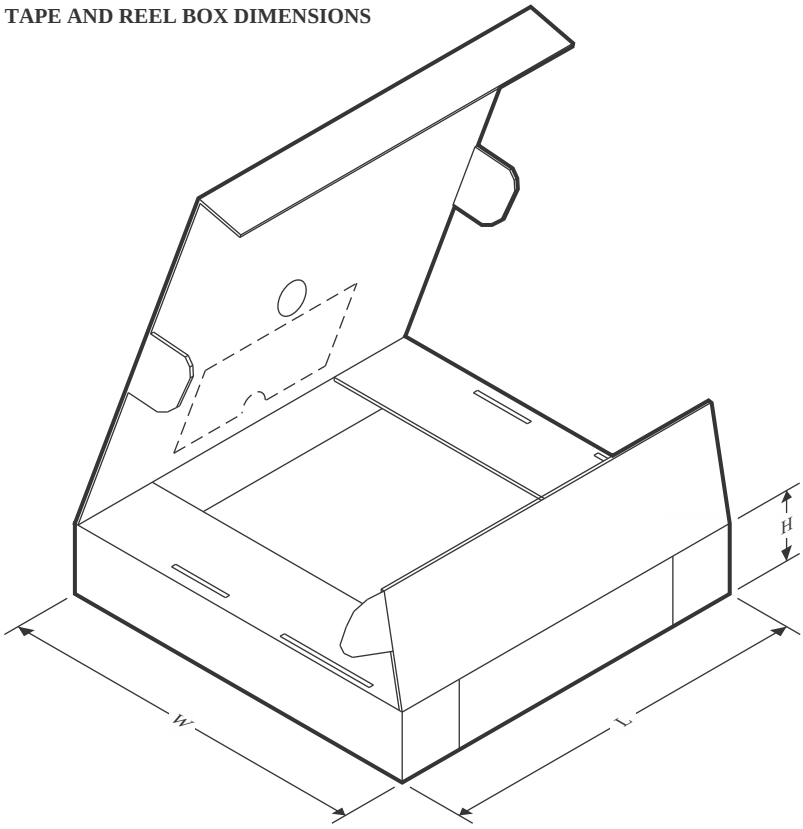
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSPM0H3215SPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSPM0H3215SRGER	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0H3215SRGZR	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSPM0H3215SRHBR	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0H3215SRUKR	WQFN	RUK	20	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSPM0H3216SPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSPM0H3216SRGER	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0H3216SRHBR	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0H3216SRUKR	WQFN	RUK	20	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



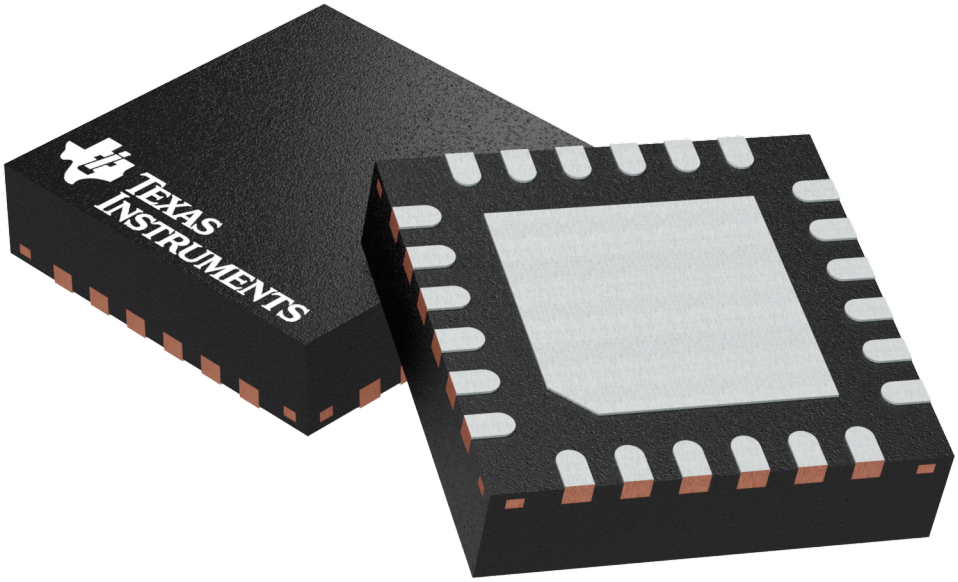
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSPM0H3215SPTR	LQFP	PT	48	1000	336.6	336.6	31.8
MSPM0H3215SRGER	VQFN	RGE	24	5000	360.0	360.0	36.0
MSPM0H3215SRGZR	VQFN	RGZ	48	4000	360.0	360.0	36.0
MSPM0H3215SRHBR	VQFN	RHB	32	5000	360.0	360.0	36.0
MSPM0H3215SRUKR	WQFN	RUK	20	5000	360.0	360.0	36.0
MSPM0H3216SPTR	LQFP	PT	48	1000	336.6	336.6	31.8
MSPM0H3216SRGER	VQFN	RGE	24	5000	360.0	360.0	36.0
MSPM0H3216SRHBR	VQFN	RHB	32	5000	360.0	360.0	36.0
MSPM0H3216SRUKR	WQFN	RUK	20	5000	360.0	360.0	36.0

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



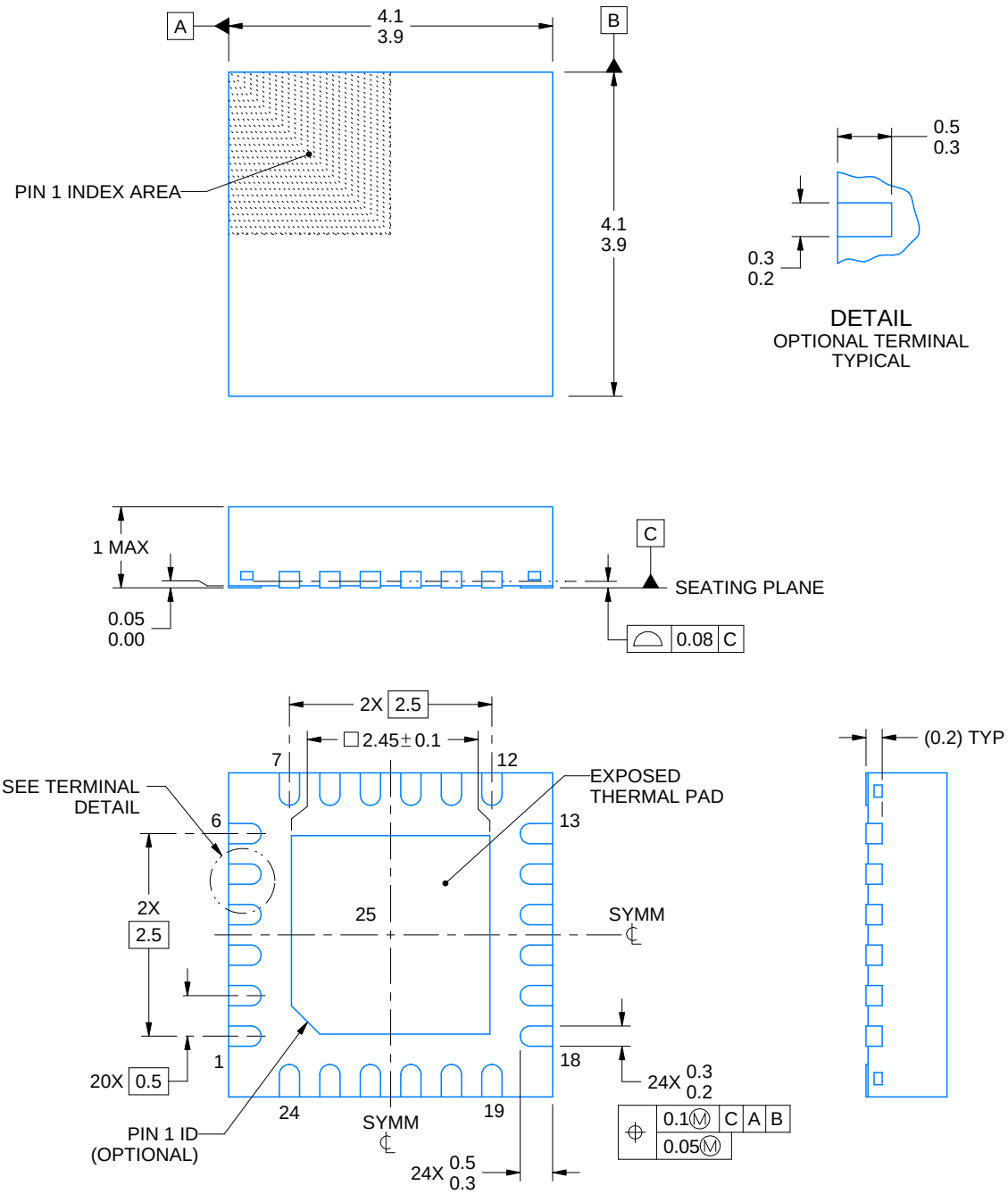
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024B

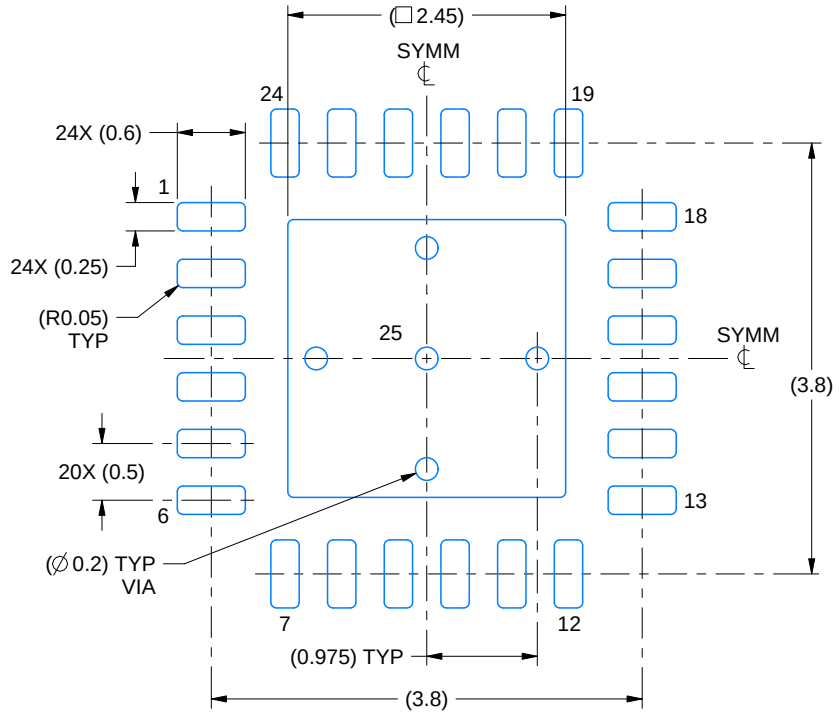
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

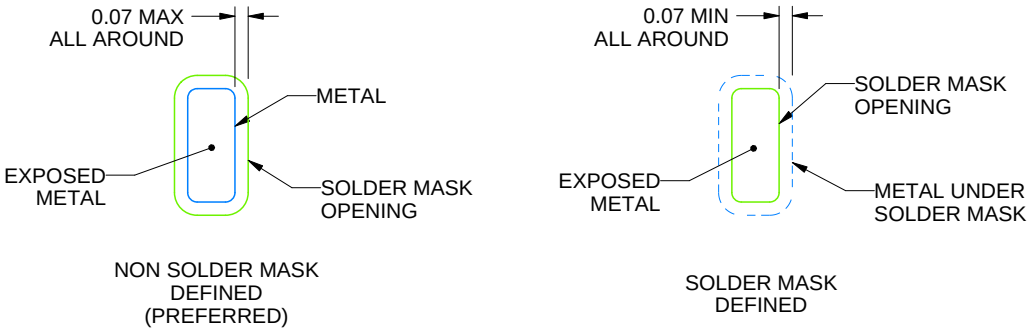


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

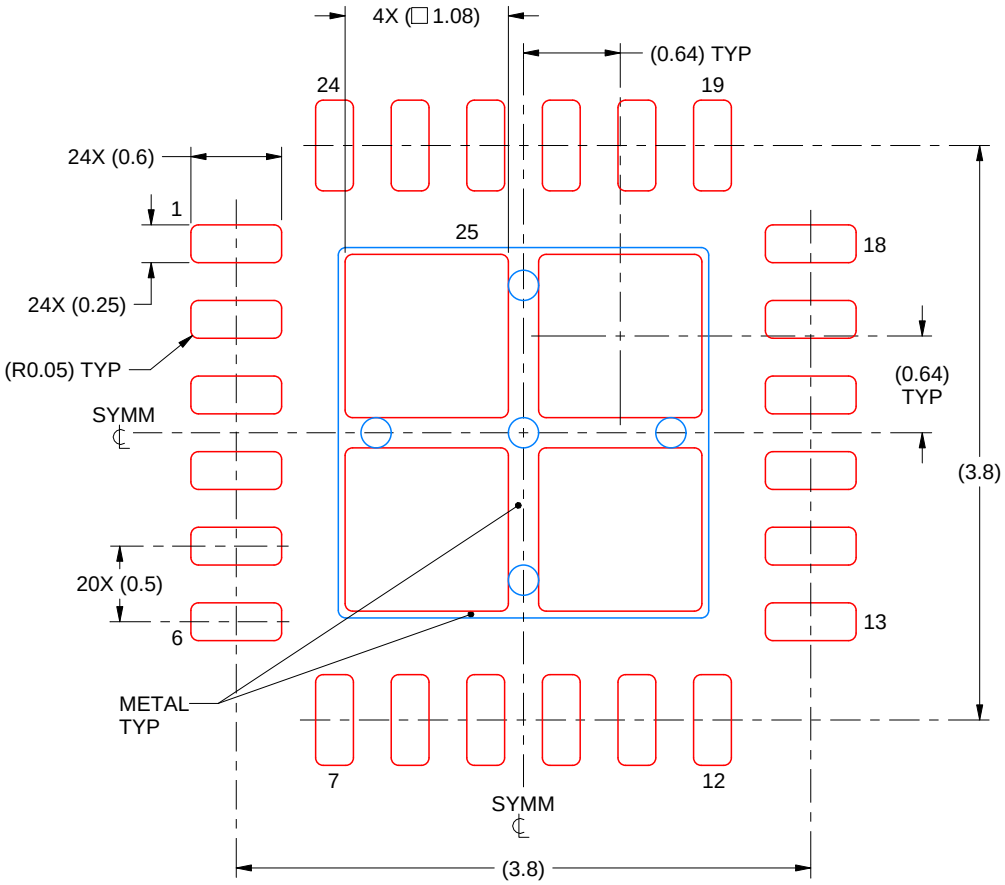


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

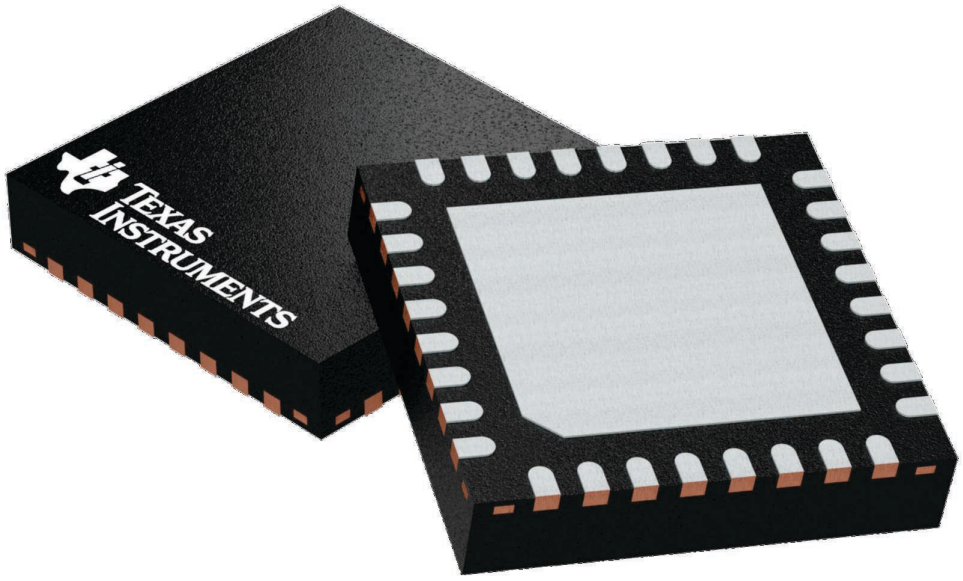
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

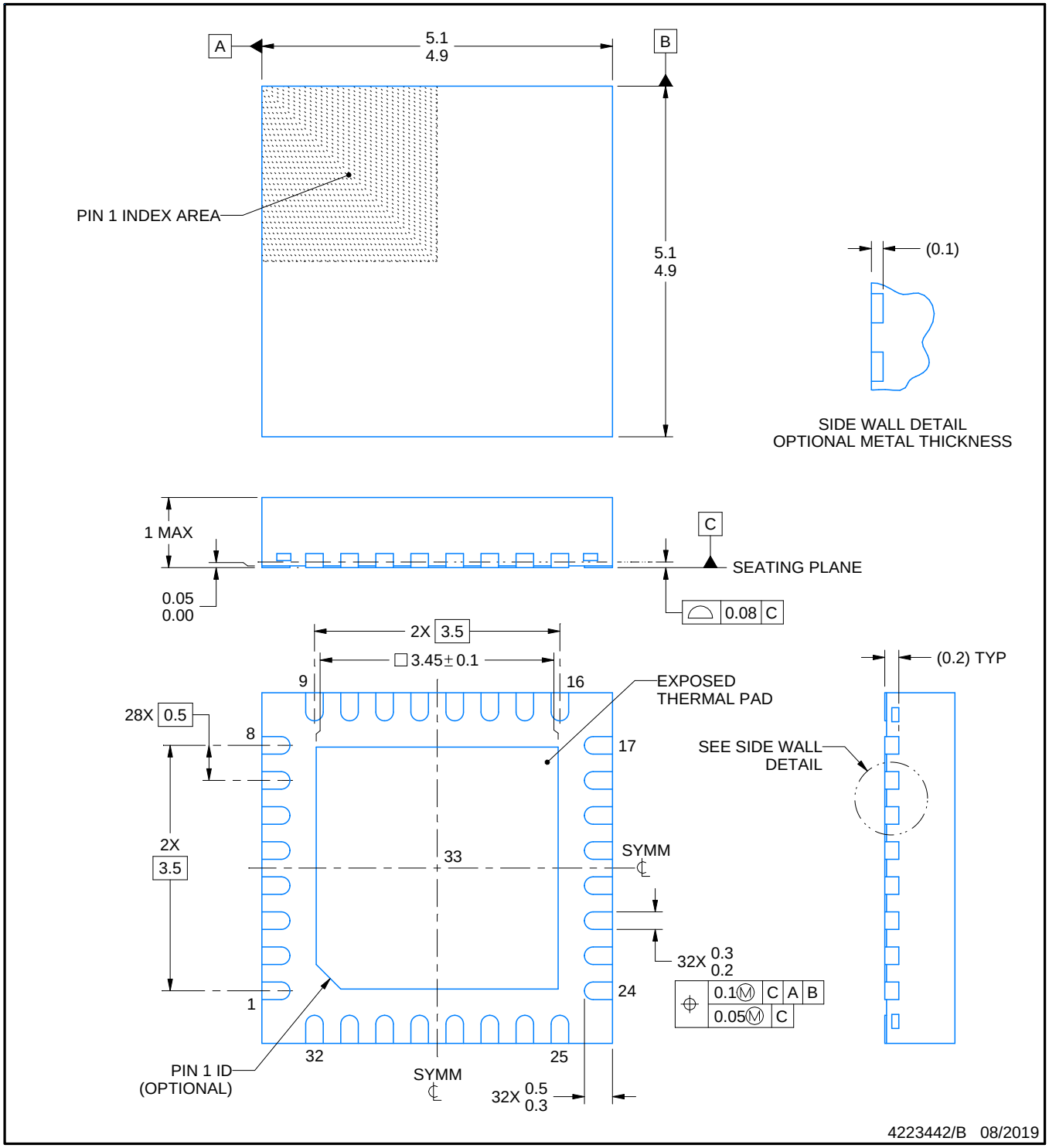
4224745/A

RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

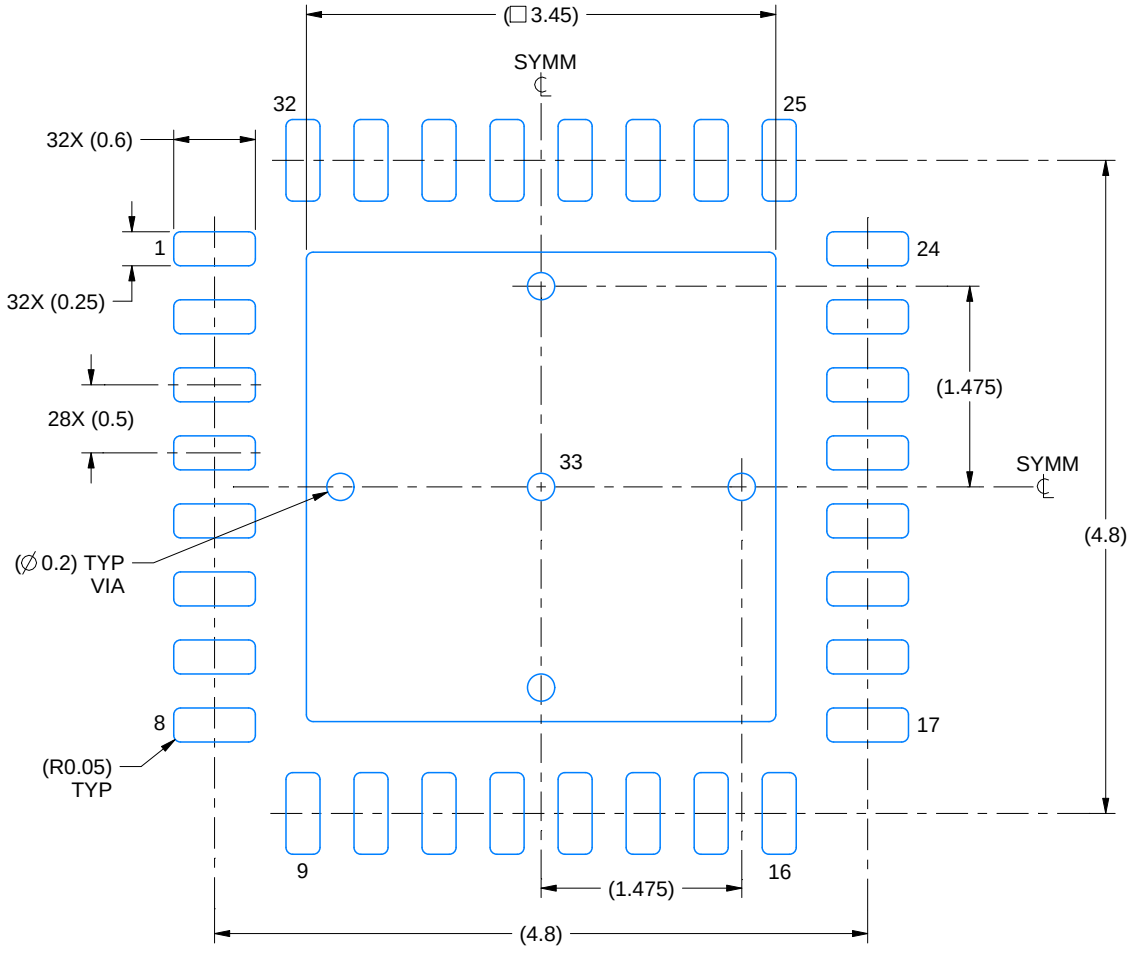
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

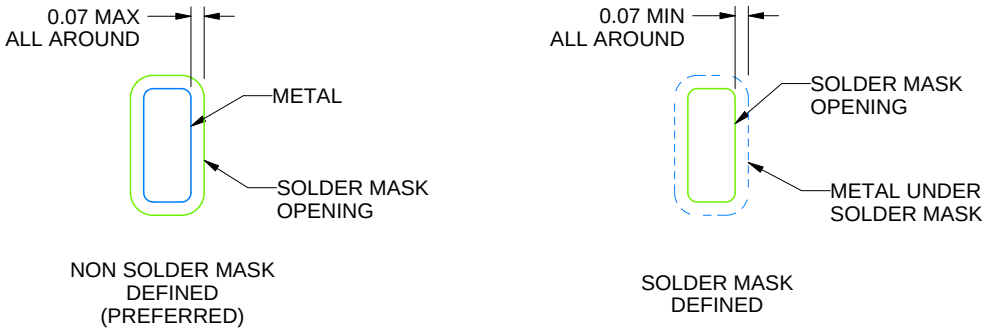
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X

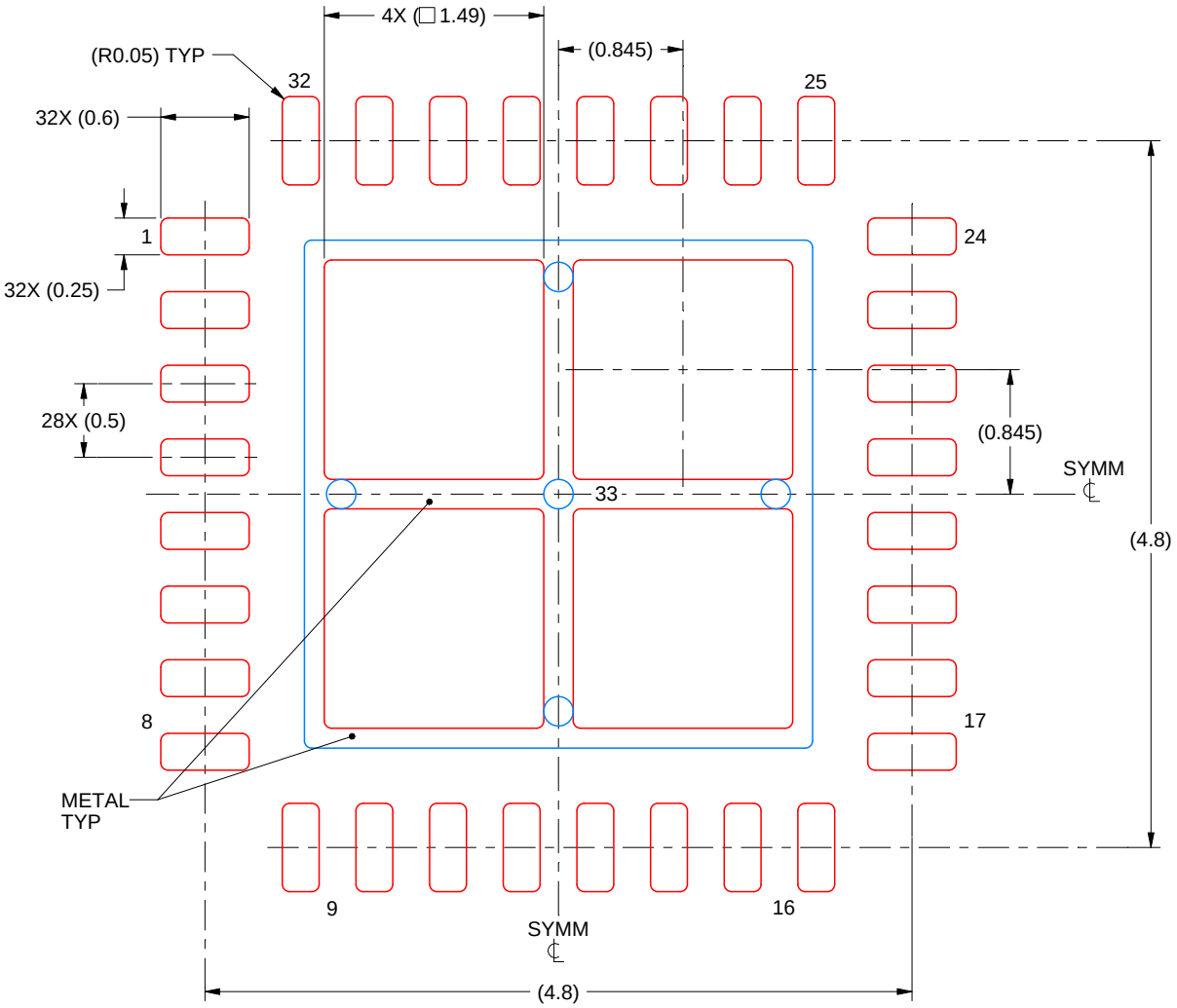


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

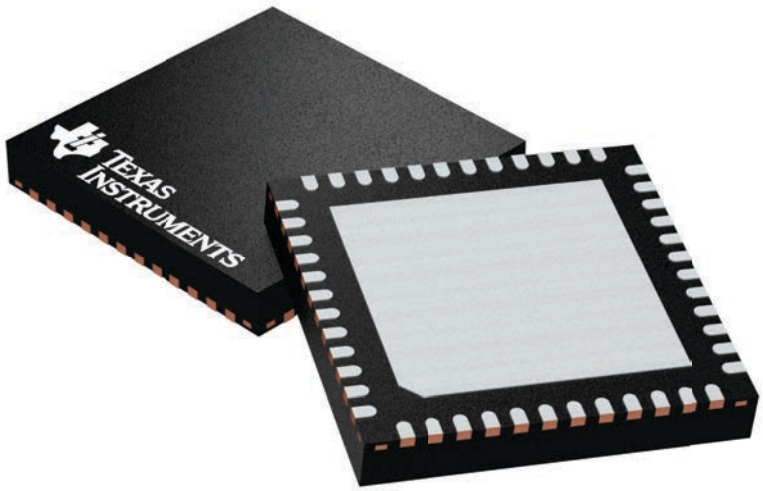
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

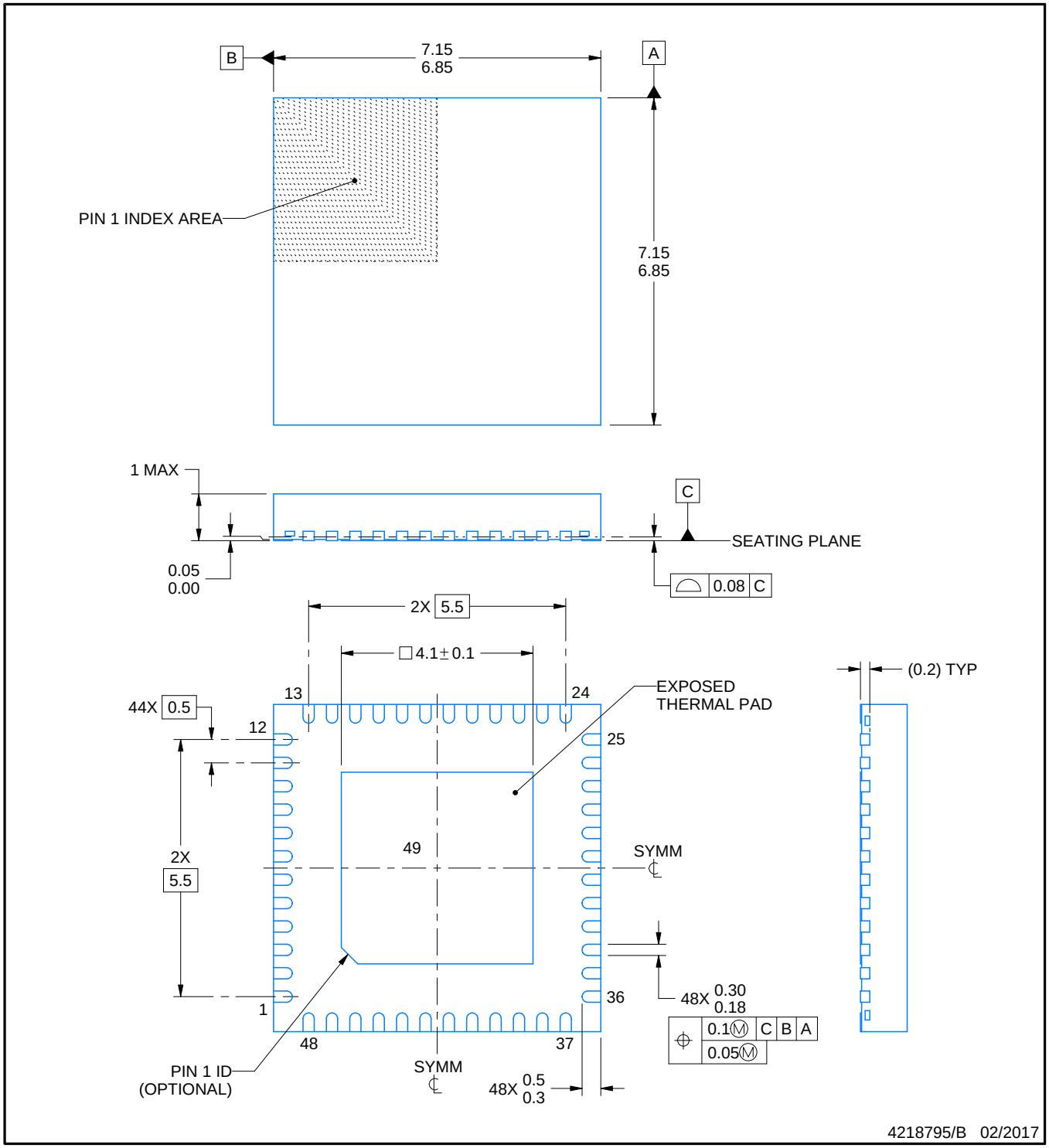
4224671/A

RGZ0048B

PACKAGE OUTLINE

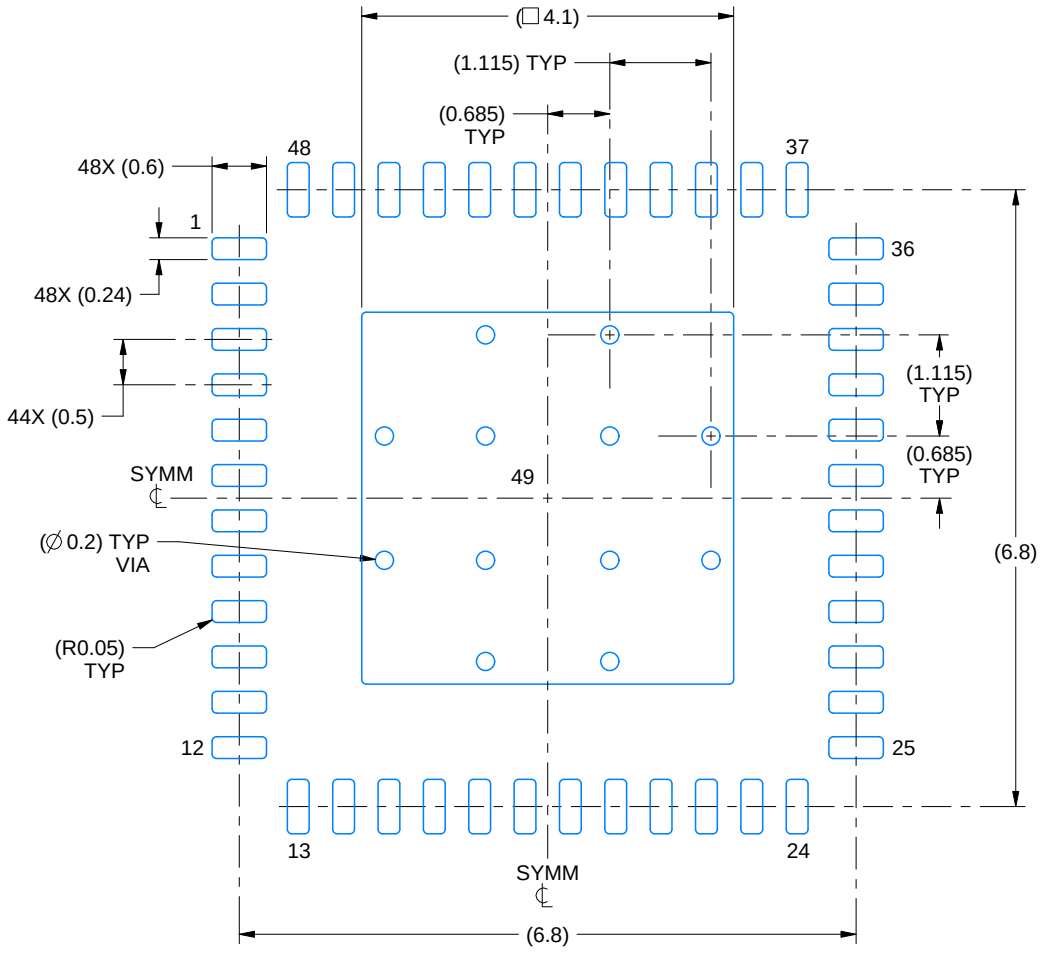
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

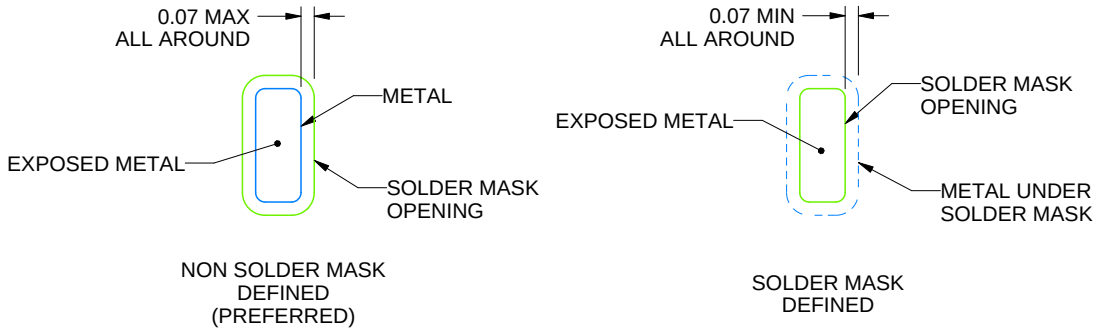


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

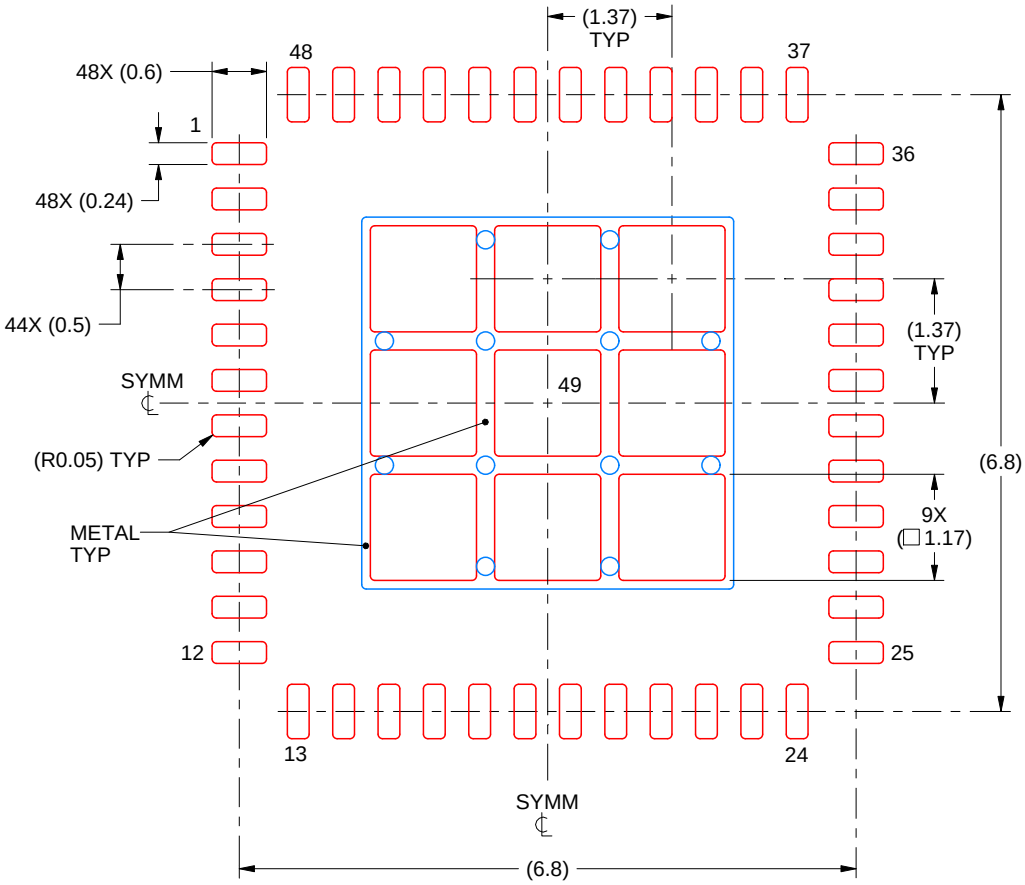


SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

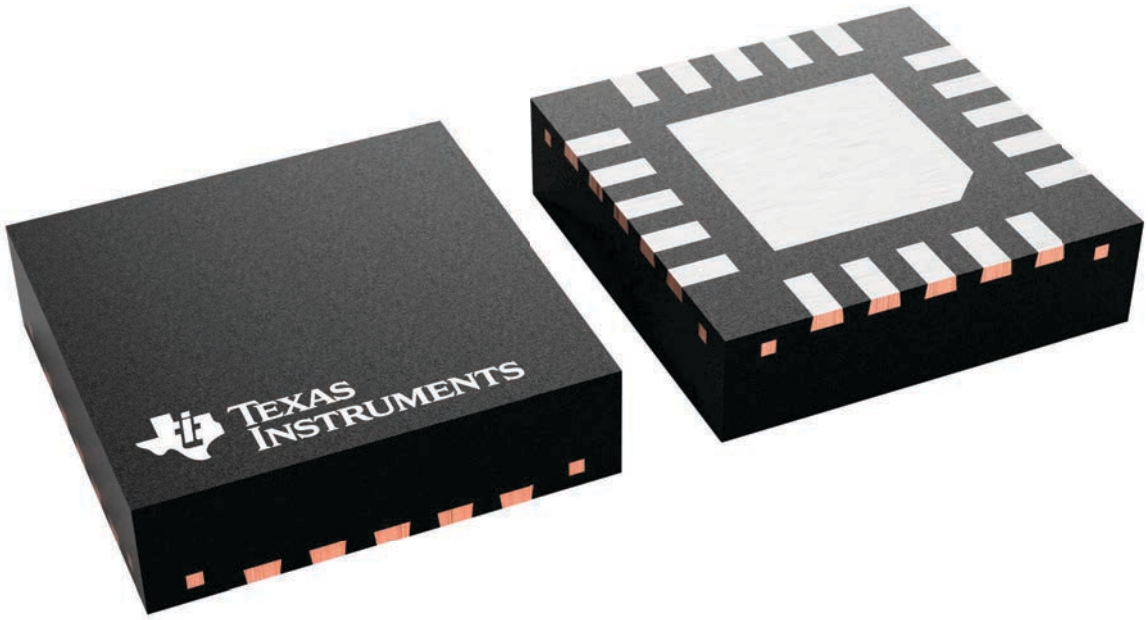
RUK 20

WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



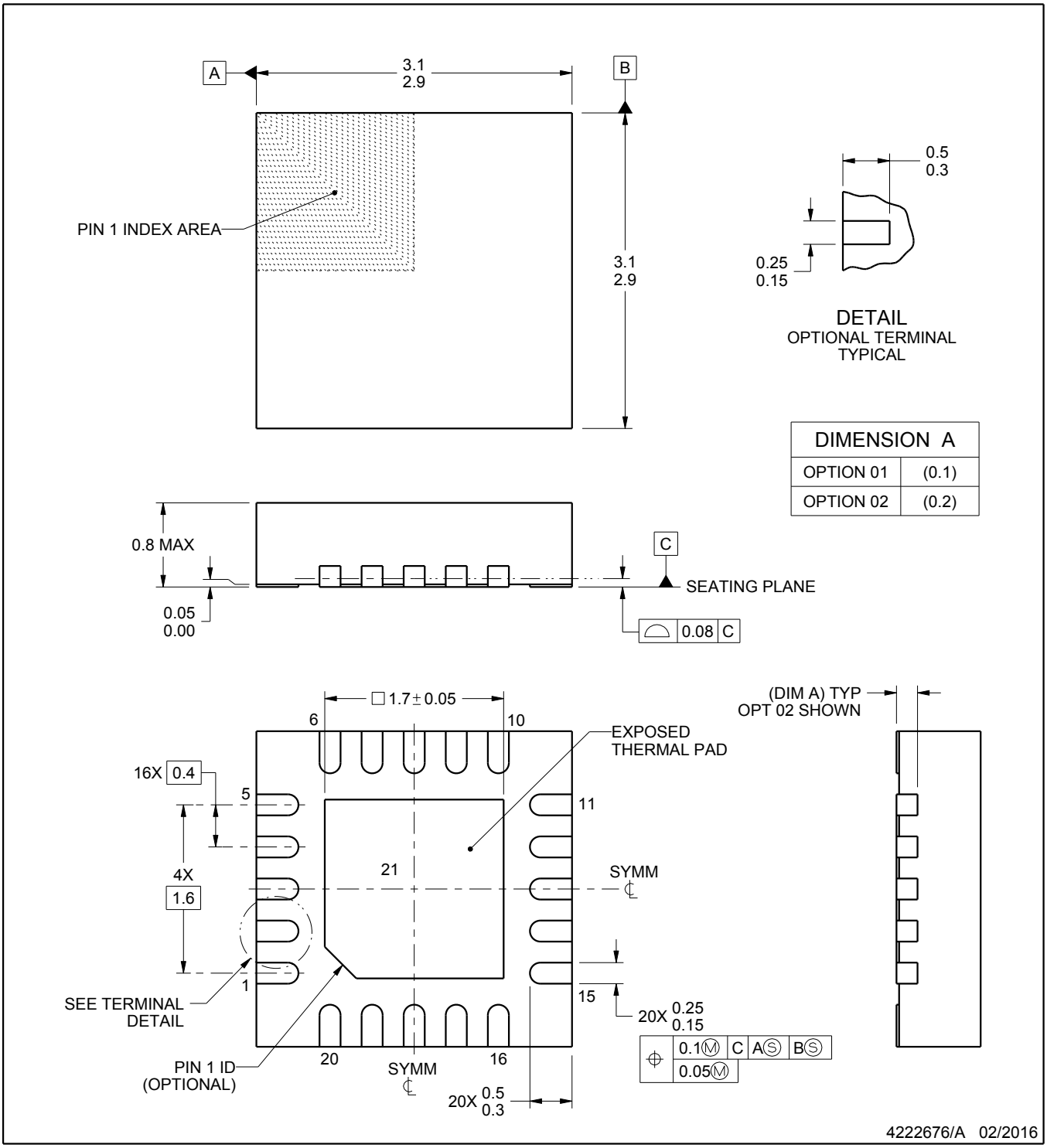
4229651/A

PACKAGE OUTLINE

RUK0020B

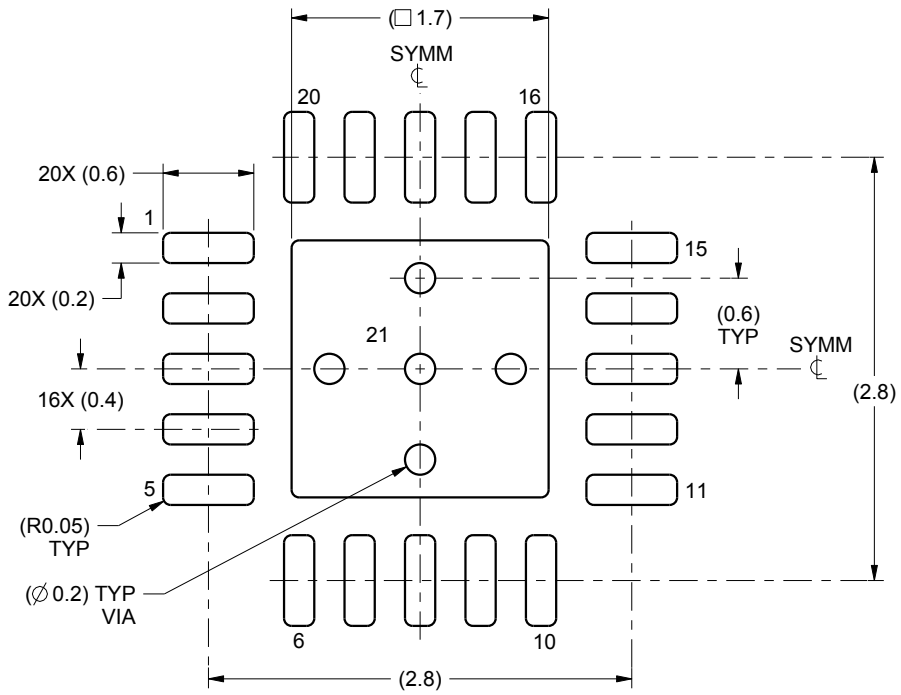
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

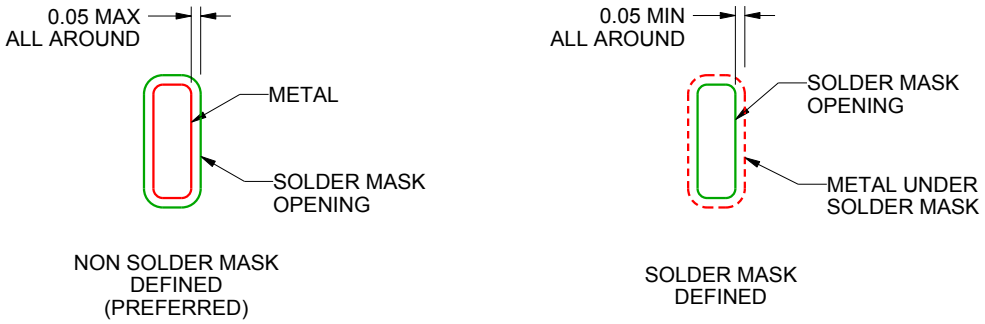


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

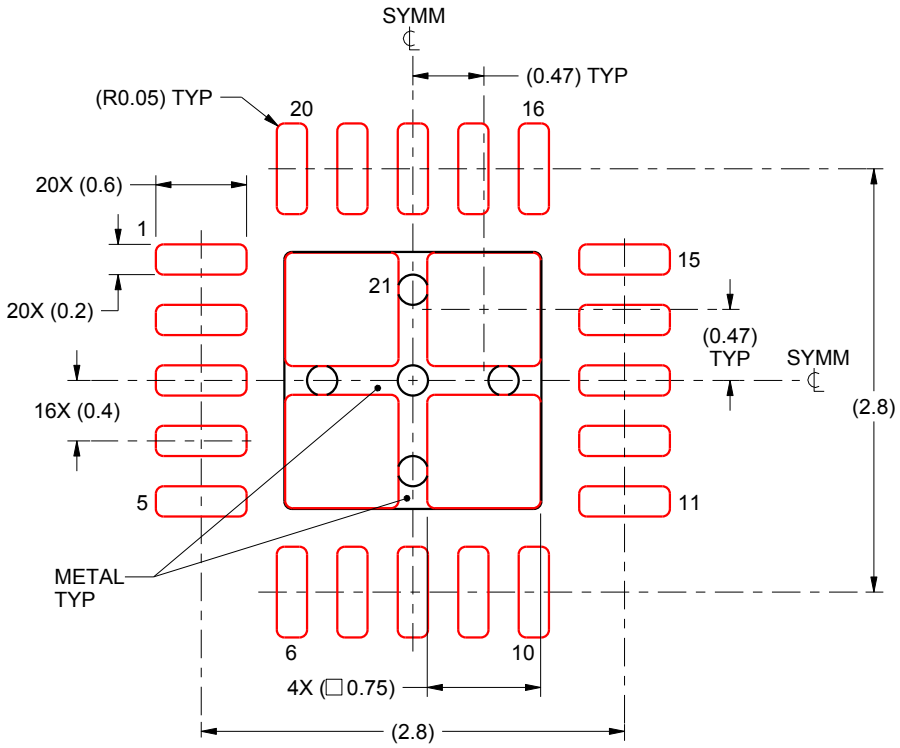


SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

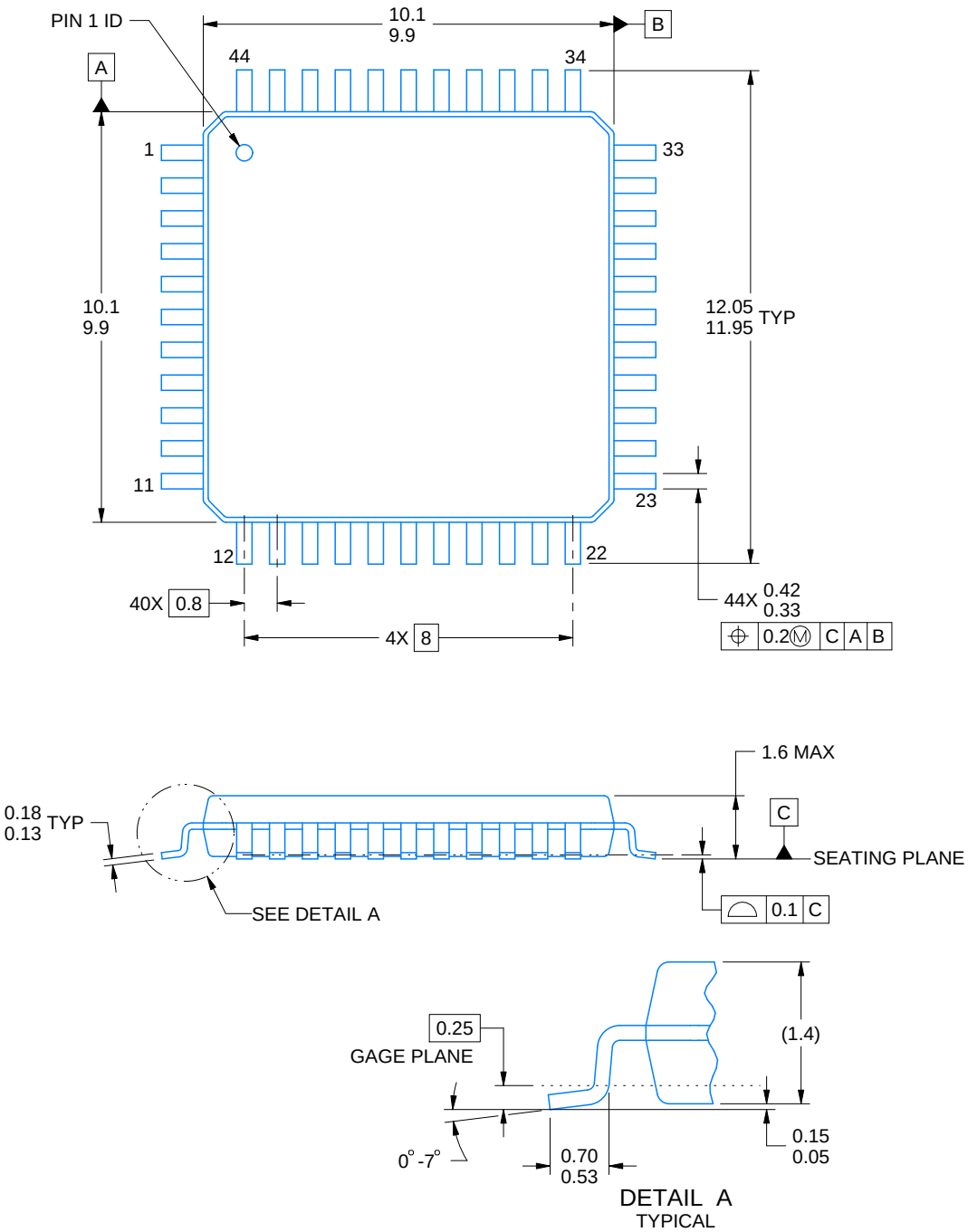
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

NNA0044A

LQFP - 1.6 mm max height

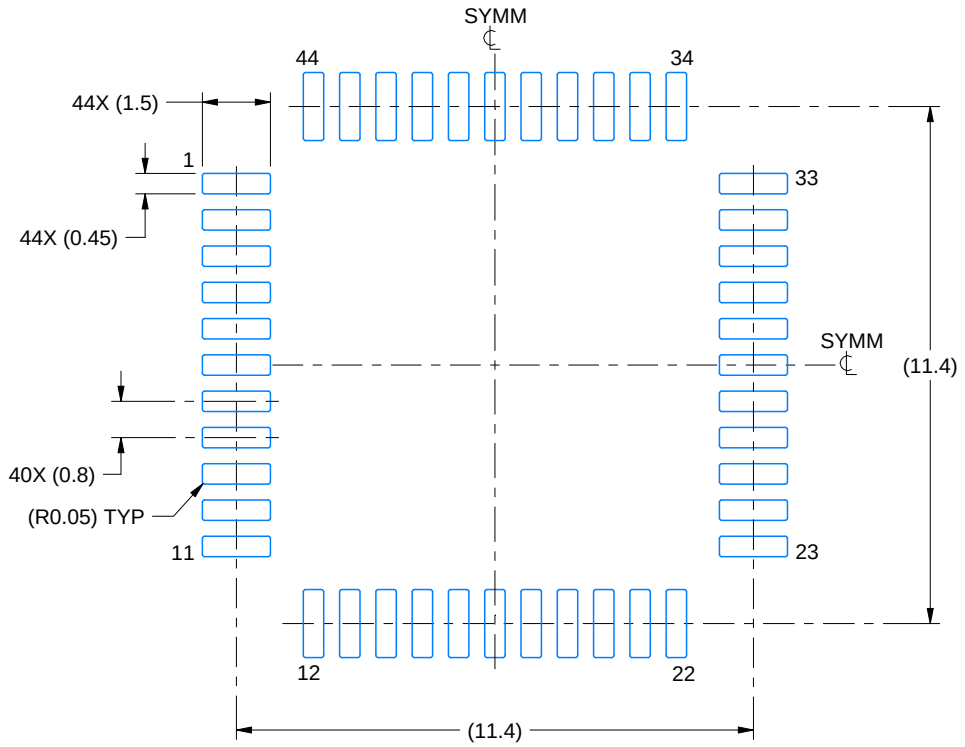
PLASTIC QUAD FLATPACK



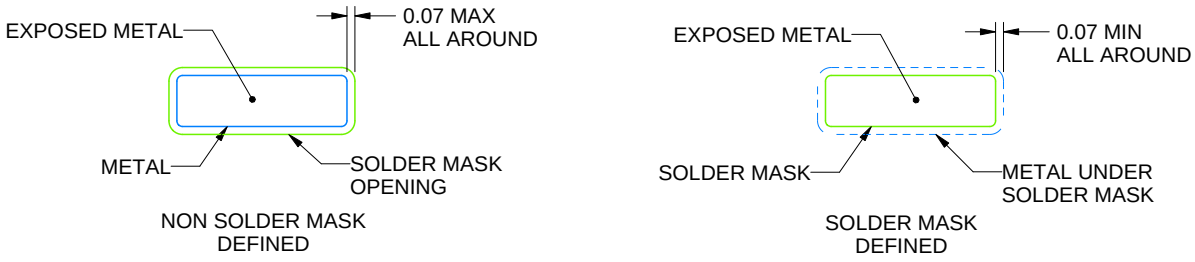
4215163/B 05/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

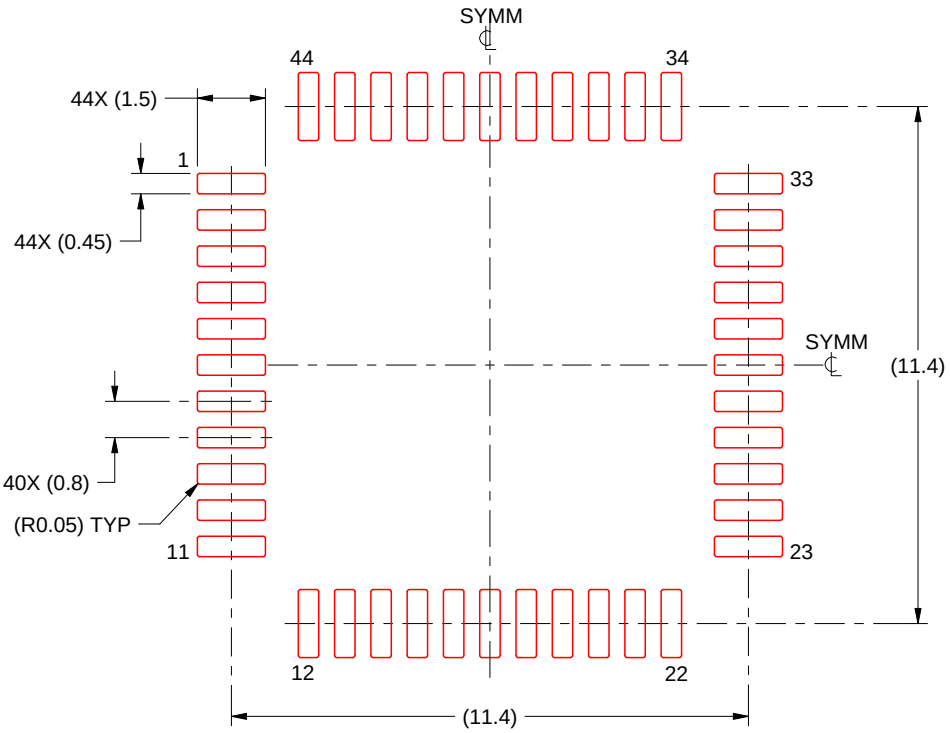


SOLDER MASK DETAILS

4215163/B 05/2025

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



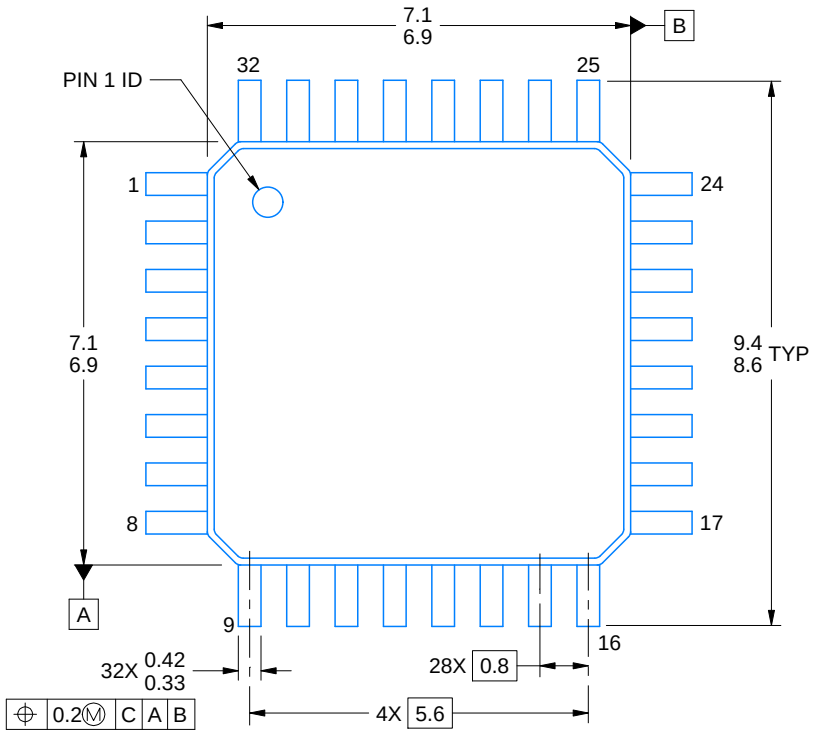
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

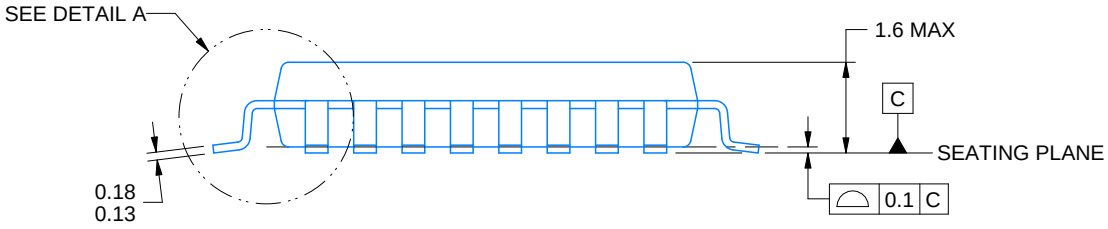
4215163/B 05/2025

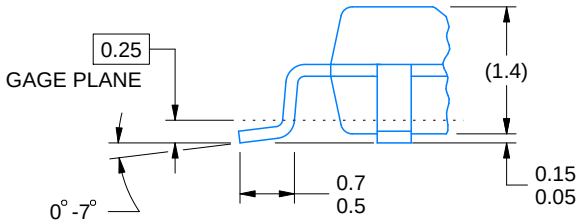
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PLASTIC QUAD FLATPACK





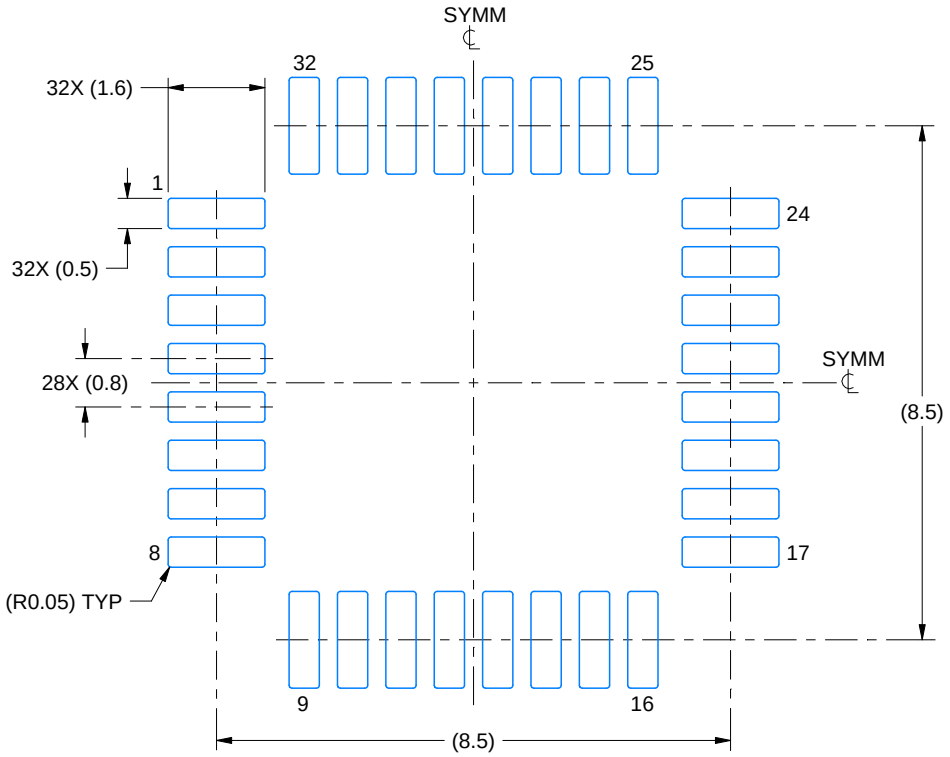


DETAIL A
TYPICAL

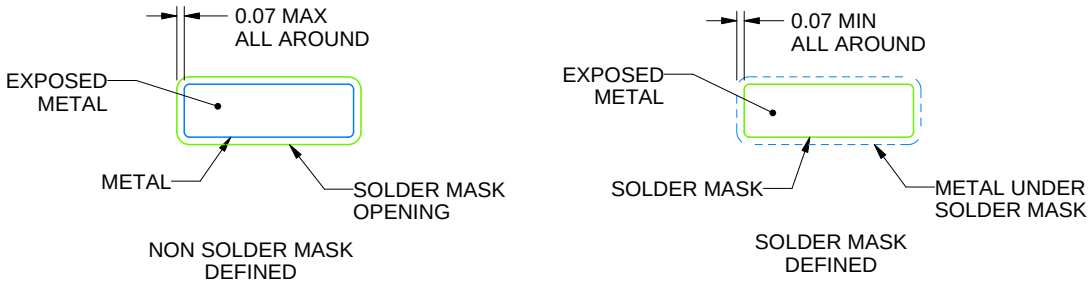
4229978/A 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

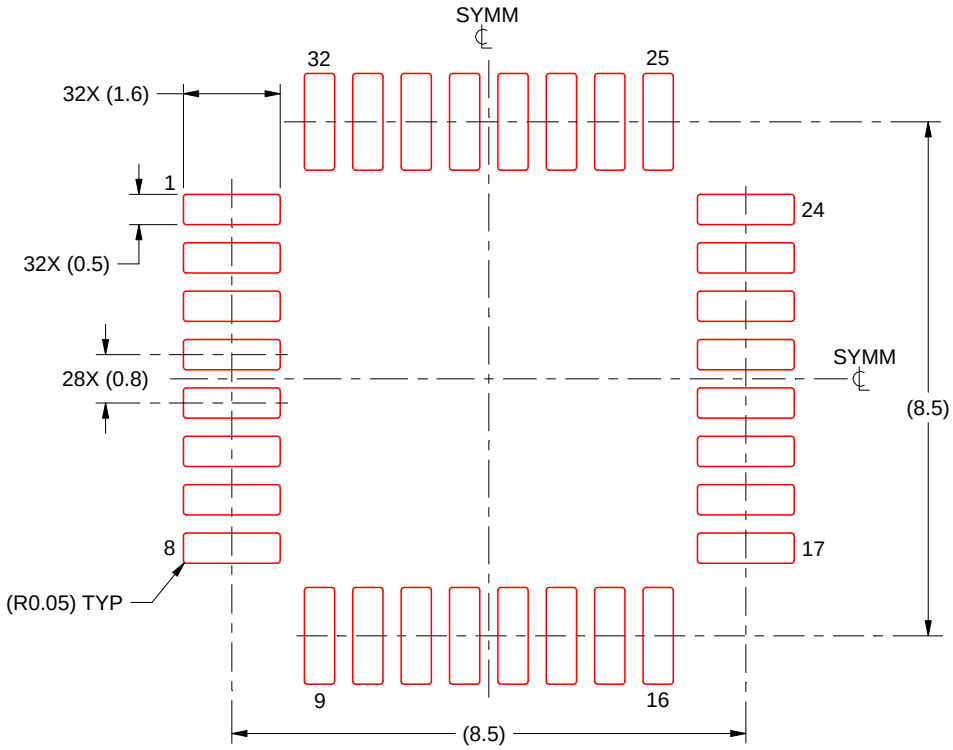


SOLDER MASK DETAILS

4229978/A 09/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE 8X

4229978/A 09/2023

NOTES: (continued)

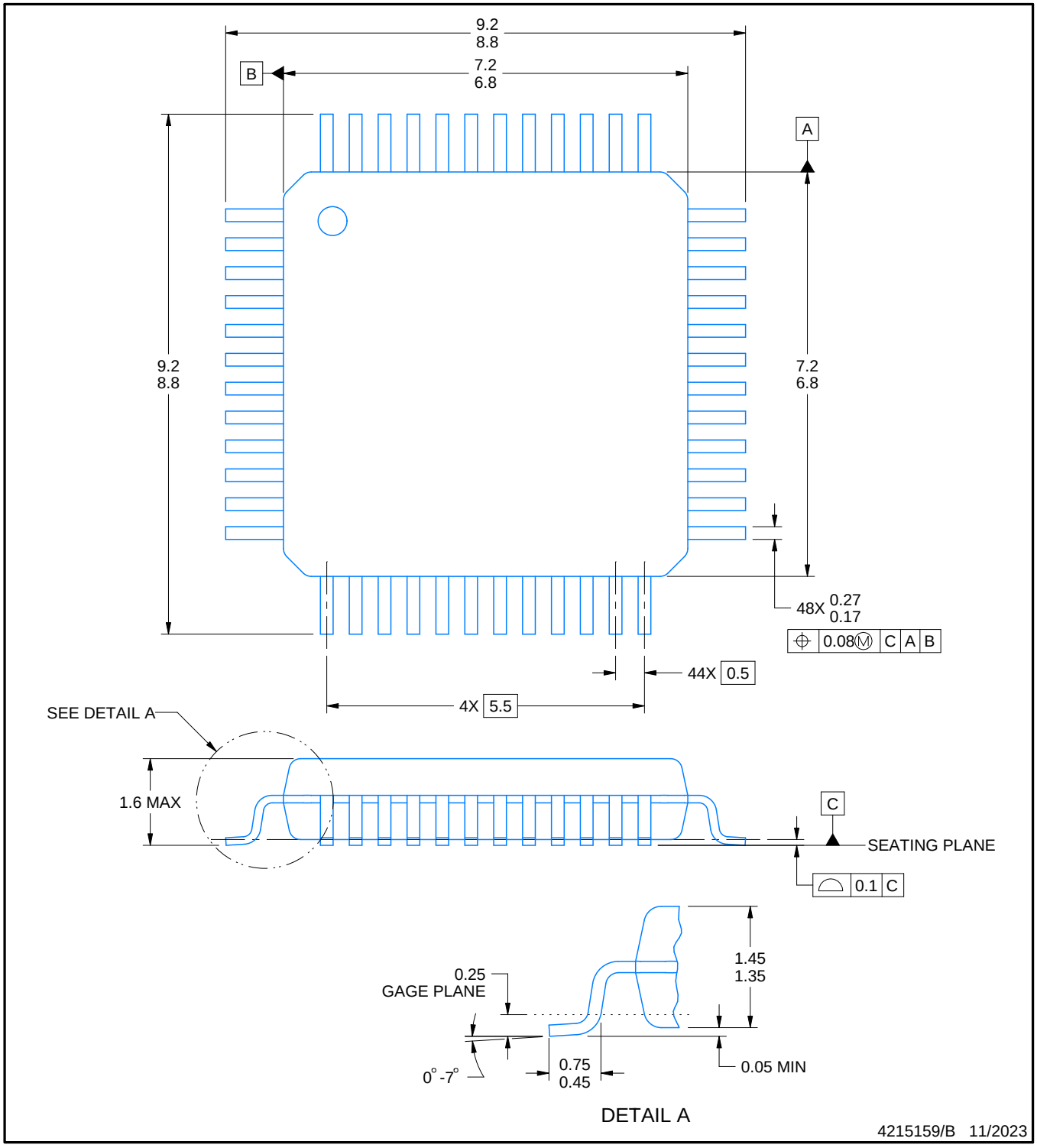
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PT0048A

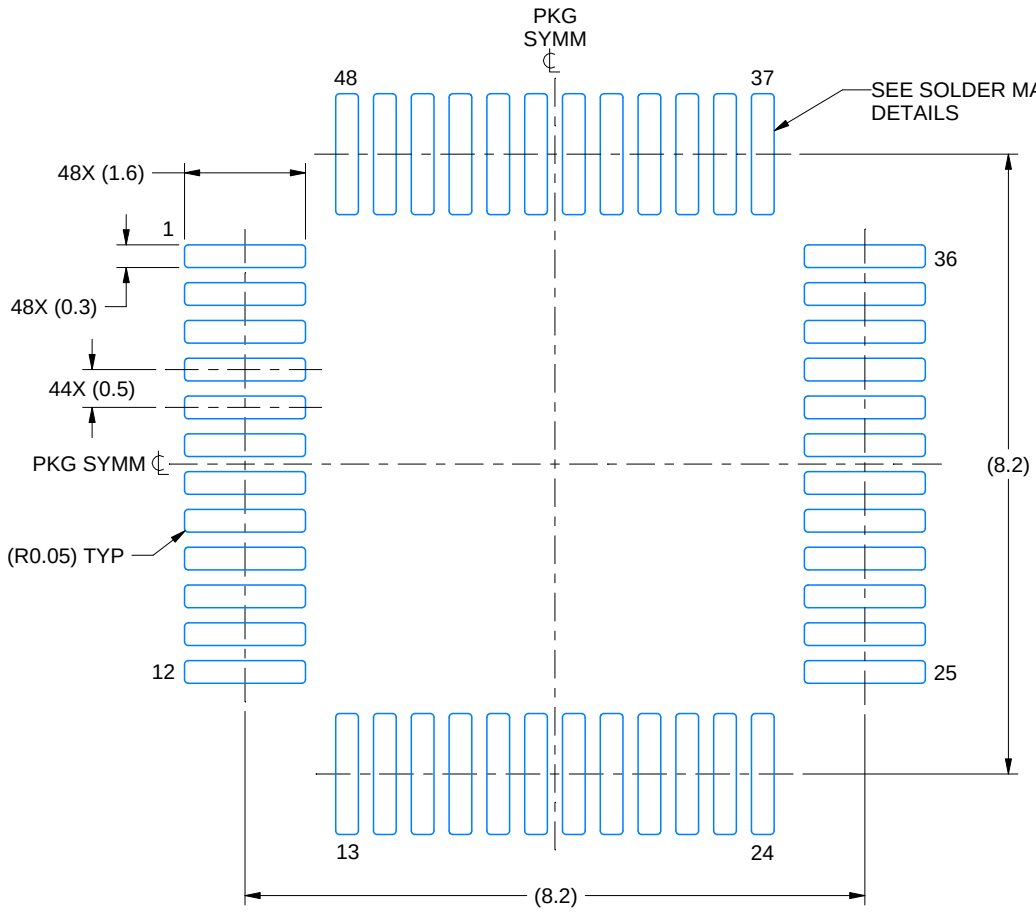
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

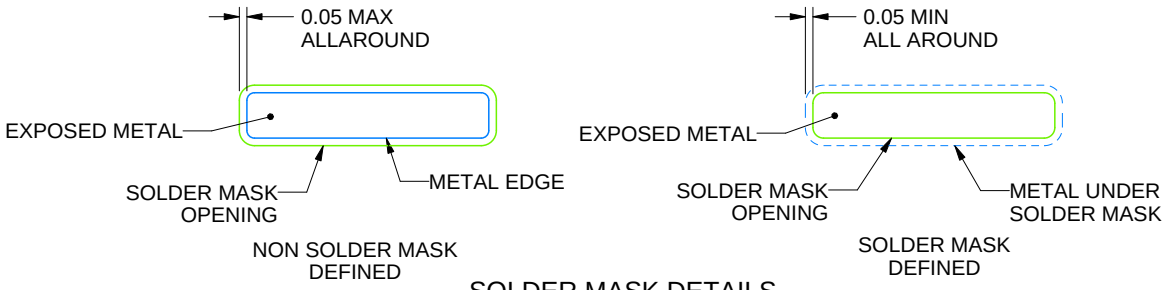


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

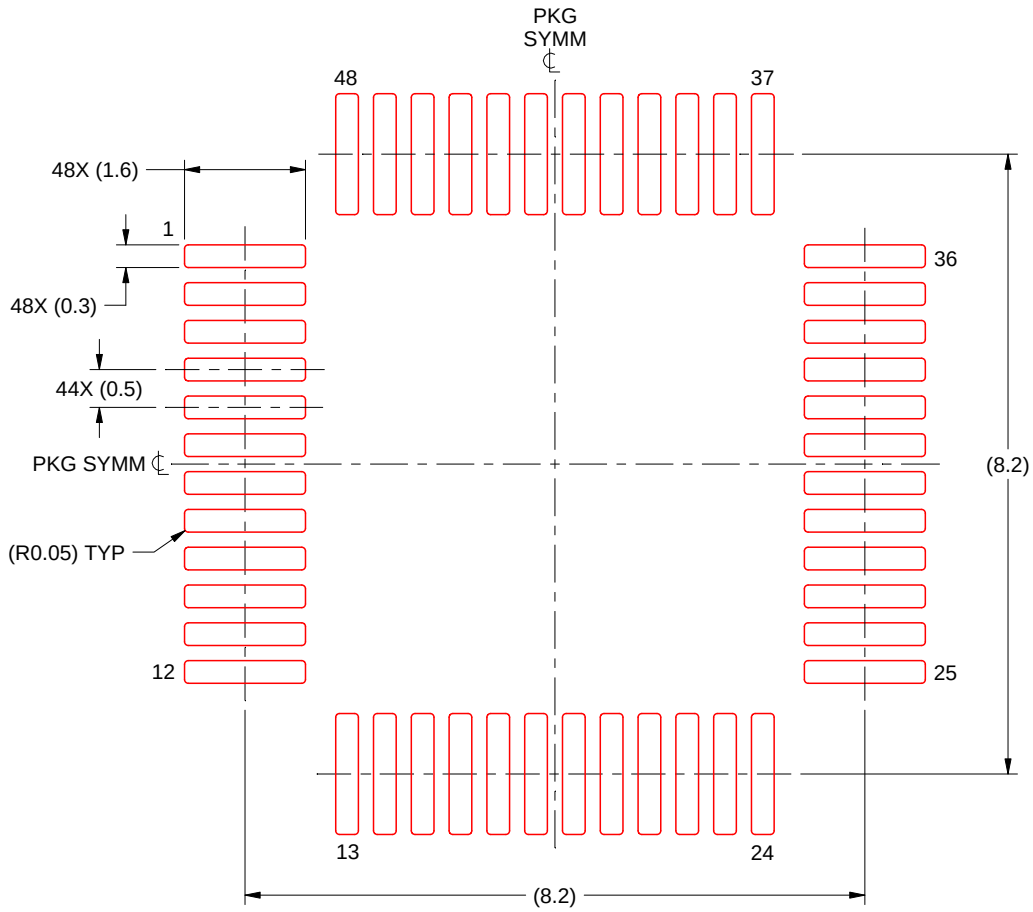


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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