MSPM0L222x-Q1, MSPM0L122x-Q1 Automotive Mixed-Signal Microcontrollers

1 Features

- AEC-Q100 Grade 1 qualified for automotive applications
- **Support for FuSa**
  - ISO26262 ASIL B
- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU with memory protection unit, frequency up to 32MHz
- PSA-L1 Certified
- **Operating characteristics**
  - Extended temperature: –40°C up to 125°C
  - Wide supply voltage range: 1.62V to 3.6V
- **Memories**
  - Up to 256KB of flash memory with ECC
    - Dual-bank with address swap with OTA updates
  - 32KB of SRAM with ECC or parity
  - 32B backup memory[1]
- **High-performance analog peripherals**
  - 12-bit 1.68Msps analog-to-digital converter (ADC), up to 26 external channels
  - Configurable 1.4V or 2.5V internal shared voltage reference (VREF)
  - Comparator (COMP) with 8-bit reference DAC
  - Integrated temperature sensor
- **User interface**
  - Ultra-low power segmented LCD controller supporting up to 8×51 and 4×55 LCD displays[2]
- **Optimized low-power modes**
  - RUN:106µA/MHz (CoreMark)
  - STOP: 54µA at 32kHz
  - $STANDBY_1$ 1.2µA (VDD), 1.1µA (VBAT) with 32kHz, LFXT, RTC, and SRAM and registers fully retained
  - SHUTDOWN: 80nA (VDD), 1.1µA (VBAT) with 32kHz, LFXT, RTC, and I/O wake-up capability
- **Intelligent digital peripherals**
  - 7-channel DMA controller
  - 15-channel event fabric signaling system
  - Six timers supporting up to 18 PWM outputs, all operational down to STANDBY mode
    - One 16-bit advanced timer with deadband
    - One 32-bit general-purpose timer
    - Four 16-bit general-purpose timers
  - Window-watchdog timer (WWDT)
  - Independent watchdog timer (IWDT) residing in the VBAT island
- **Communication interfaces**
  - Five UART modules, with two supporting LIN, IrDA, DALI, smart card, Manchester
  - Three I^2C modules supporting SMBus/PMBus and wakeup from STOP mode, with two supporting up to FM+ (1Mbps)
  - Two SPI modules supporting up to 16Mbps
- **Clock system**
  - Internal 4MHz to 32MHz oscillator with up to ±1.2% accuracy (SYSOSC)
  - Internal 32kHz oscillator (LFOSC) with ±3% accuracy [1]
  - External 4MHz to 32MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator (LFXT) [1]
  - External LF [1] and HF digital clock inputs
  - Digital clock output
- **Data integrity and encryption**
  - AES accelerator with support for GCM/GMAC, CCM/CBC-MAC, CBC, CTR
  - Secure Key Storage for up to four AES keys
  - Flexible firewalls for protecting code and data
  - True random number generator (TRNG)
  - Cyclic redundancy checker (CRC-16, CRC-32)
- **VBAT island (auxiliary supply)** [1]
  - Independent supply with dedicated VBAT pin
  - Internal super-capacitor charger
  - Real-time clock (RTC)
  - Tamper detection with timestamp
  - Independent watchdog timer (IWDT)
  - Scratch Pad Memory (SPM)
- **Flexible I/O features**
  - Up to 73 total GPIOs
  - Up to 5 GPIOs supplied by VBAT pin [1]
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**
  - 80-pin LQFP
  - 64-pin LQFP
  - 48-pin LQFP, VQFN[3]
  - 32-pin VQFN [3]
  - 24-pin VQFN [3]
- **Family members** (also see *Device Comparison*)
  - MSPM0L2228: 256KB flash, LCD
  - MSPM0L2227: 128KB flash, LCD
  - MSPM0L1228: 256KB flash
  - MSPM0L1227: 128KB flash
- **Development kits and software** (also see *Tools and Software*)

[1] Part of the LFSS (Low Frequency Subsystem) supplied by the VBAT pin residing in the VBAT island
[2] MSPM0L222x devices only
[3] VQFN packages have wettable flanks.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

  - LP-MSPM0L2228 LaunchPad™ development kit
  - MSP Software Development Kit (SDK)

2 Applications

- Automotive body electronics and Lighting
- Automotive Gateway
- Steering Wheel Systems
- Automotive Motor Control
- DC to AC Inverters
- Automotive Interior Lighting
- Door handle modules
- Kick to open modules
- Vehicle Occupancy Detection
- Seat Comfort Module

3 Description

MSPM0Lx22x microcontrollers (MCUs) are part of the highly integrated, ultra-low-power 32-bit MSPM0 MCU family based on the Arm® Cortex®-M0+ 32-bit core platform, operating at up to 32MHz frequency. These MCUs offer a blend of cost optimization and design flexibility for applications requiring 128KB to 256KB of flash memory in small packages (down to 4mm x 4mm) or high pin count packages (up to 80 pins). These devices include a VBAT backup island, an optional segmented LCD controller (on MSPM0L222x), cybersecurity enablers, and high-performance integrated analog, and provide excellent low-power performance across the operating temperature range.

Up to 256KB of embedded flash program memory with built-in error correction code (ECC) and up to 32KB SRAM with ECC and parity protection is provided. The flash memory is organized into two main banks to support field firmware updates, with address swap support provided between the two main banks. An additional 32-byte backup memory is provided in the VBAT island, supplied by the VBAT pin and retained even when the main supply (VDD) is lost.

The VBAT island provides a fully independent auxiliary power domain (separate from the main supply) which supplies low frequency modules from an alternate supply such as a battery, supercapacitor, or alternate voltage level (1.62V to 3.6V). The VBAT island includes the low-frequency clock system (LFOSC, LFXT), the real-time clock, the tamper detection, and timestamp logic, an independent watchdog timer, and a 32-byte backup memory. Up to five digital IOs are powered from the VBAT supply. A charging mode is provided to optionally trickle charge a supercapacitor on the VBAT pin from the primary (VDD) supply when VDD is greater than VBAT.

An ultra-low power segmented LCD controller (on MSPM0L2228 and MSPM0L2227 devices) supports driving LCD glass with up to 59 pins in a variety of mux and bias configurations, enabling low cost displays.

Flexible cybersecurity enablers can be used to support secure boot, secure in-field firmware updates, IP protection (execute-only memory), key storage, and more. Hardware acceleration is provided for a variety of AES symmetric cipher modes, as well as a TRNG entropy source. The cybersecurity architecture is Arm® PSA Level 1 certified.

A set of high-performance analog modules is provided, including a 12-bit 1.68Msps SAR ADC supporting up to 26 external channels. An analog comparator is provided to support low power or low latency monitoring of analog signals. An on-chip voltage reference (1.4V or 2.5V) can be used to provide a stable reference voltage to the ADC and comparator. Environmental monitoring of the die temperature using the internal temperature sensor, VDD voltage, and VBAT voltage is supported.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0Lx22x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

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For complete module descriptions, see the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM0 MCUs.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
MSPM0L2228SPN	PN (LQFP, 80)	14mm x 14mm
MSPM0L2227SPN		
MSPM0L1228SPN		
MSPM0L1227SPN		
MSPM0L2228SPM	PM (LQFP, 64)	12 mm x 12 mm
MSPM0L2227SPM		
MSPM0L1228SPM		
MSPM0L1227SPM		
MSPM0L2228SPT	PT (LQFP, 48)	9mm x 9mm
MSPM0L2227SPT		
MSPM0L1228SPT		
MSPM0L1227SPT		
MSPM0L2228SRGZ	RGZ (VQFN, 48)	7mm x 7mm
MSPM0L2227SRGZ		
MSPM0L1228SRGZ		
MSPM0L1227SRGZ		
MSPM0L1228SRHB	RHB (VQFN, 32)	5mm x 5mm
MSPM0L1227SRHB		
MSPM0L1228SRGE	RGE (VQFN, 24)	4mm x 4mm
MSPM0L1227SRGE		

(1) For more information, see Section 12.
(2) The package size (length x width) is a nominal value and includes pins, where applicable

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4 Functional Block Diagram

Figure 4-1 shows the functional block diagram.

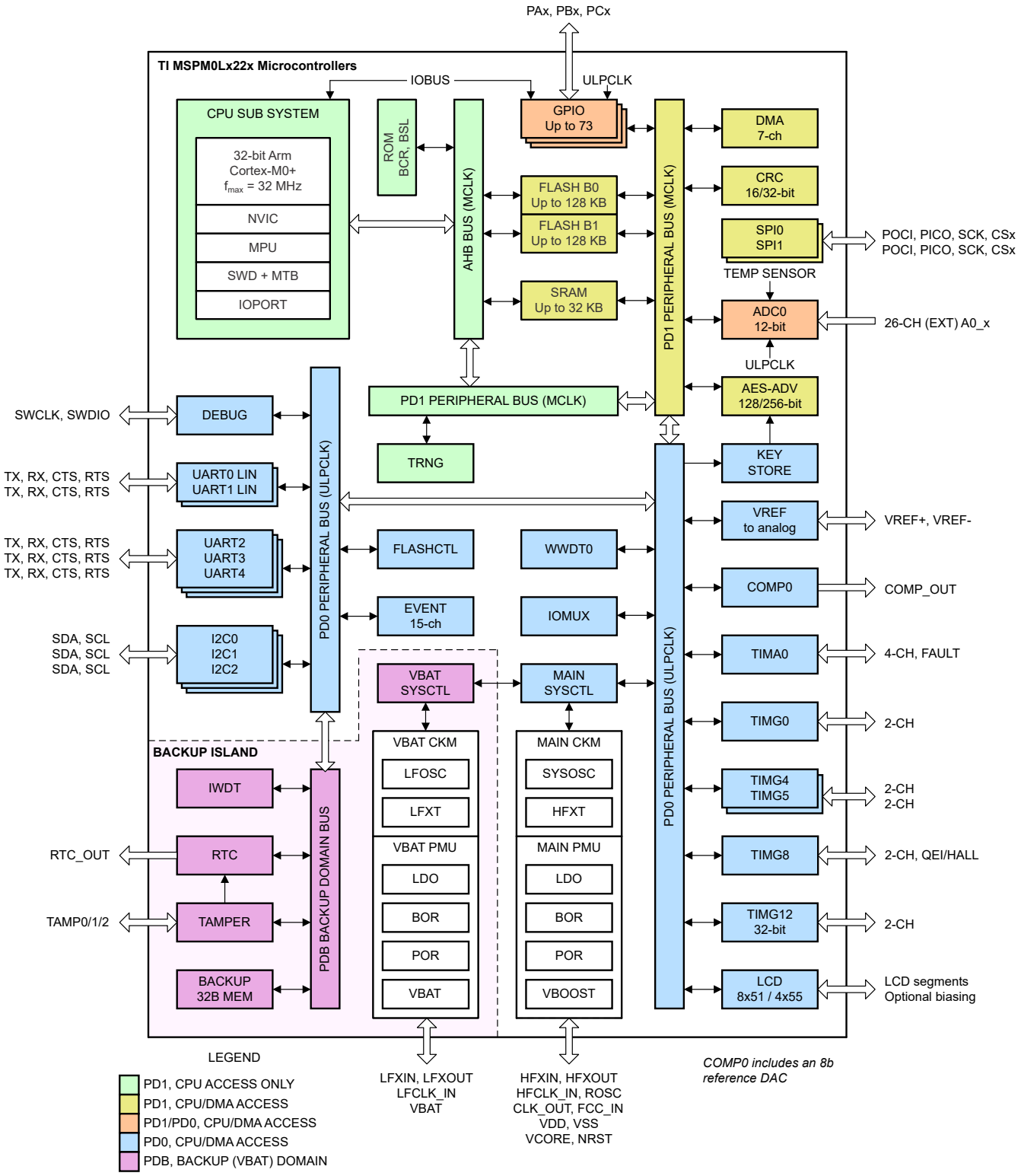


Figure 4-1. MSPM0Lx22x Functional Block Diagram

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5 Device Comparison

Table 5-1. Device Comparison Table

DEVICE NAME	FLASH / SRAM (KB)	QUAL	LCD	UART/I2C/ SPI	VBAT(1)	ADC CHANNEL	GPIO	PACKAGE
M0L2228QPNQ1	256 / 32	Q	Yes	5/3/2	Yes	26	73	80 LQFP [14mm x 14mm]
M0L2227QPNQ1	128 / 32	Q	Yes	5/3/2	Yes	26	73	
M0L1228QPNQ1	256 / 32	Q	-	5/3/2	Yes	26	73	
M0L1227QPNQ1	128 / 32	Q	-	5/3/2	Yes	26	73	
M0L2228QPMQ1	256 / 32	Q	Yes	5/3/2	Yes	26	59	64 LQFP [12mm x 12mm]
M0L2227QPMQ1	128 / 32	Q	Yes	5/3/2	Yes	26	59	
M0L1228QPMQ1	256 / 32	Q	-	5/3/2	Yes	26	59	
M0L1227QPMQ1	128 / 32	Q	-	5/3/2	Yes	26	59	
M0L2228QPTQ1	256 / 32	Q	Yes	5/3/2	Yes	21	43	48 LQFP [9mm x 9mm]
M0L2227QPTQ1	128 / 32	Q	Yes	5/3/2	Yes	21	43	
M0L1228QPTQ1	256 / 32	Q	-	5/3/2	Yes	21	43	
M0L1227QPTQ1	128 / 32	Q	-	5/3/2	Yes	21	43	
M0L1228QRGZQ1	256 / 32	Q	-	5/3/2	Yes	21	43	48 VQFN [7mm x 7mm](2)
M0L1227QRGZQ1	128 / 32	Q	-	5/3/2	Yes	21	43	
M0L1228QRHBQ1	256 / 32	Q	-	4/3/2	-	13	28	32 VQFN [5mm x 5mm](2)
M0L1227QRHBQ1	128 / 32	Q	-	4/3/2	-	13	28	
M0L1228QRGEQ1	256 / 32	Q	-	4/3/2	-	9	20	24 VQFN [4mm x 4mm](2)
M0L1227QRGEQ1	128 / 32	Q	-	4/3/2	-	9	20	

(1) The VBAT pin for backup power domain is available in packages with 48 or more pins.
(2) 24-pin, 32-pin, and 48-pin VQFN packages are available with wettable flanks.

5.1 Device Comparison Chart

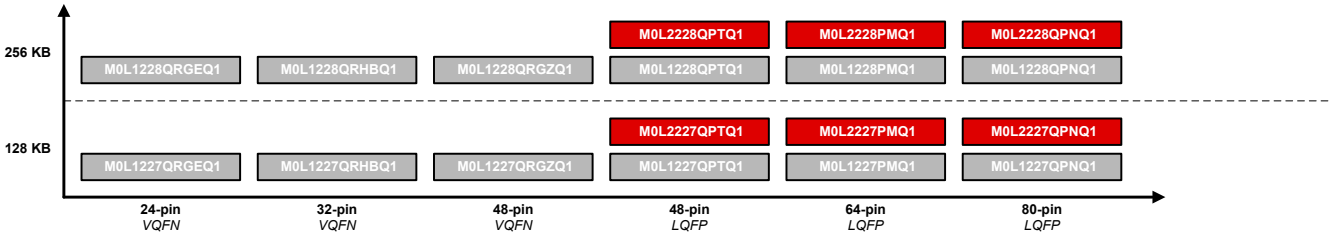


Figure 5-1. Device Comparison Chart

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6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The pin diagrams shown in the data sheet show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout.

For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

Note

For full pin configuration and functions for each package option, refer to Section 6.2.1 and Signal Descriptions.

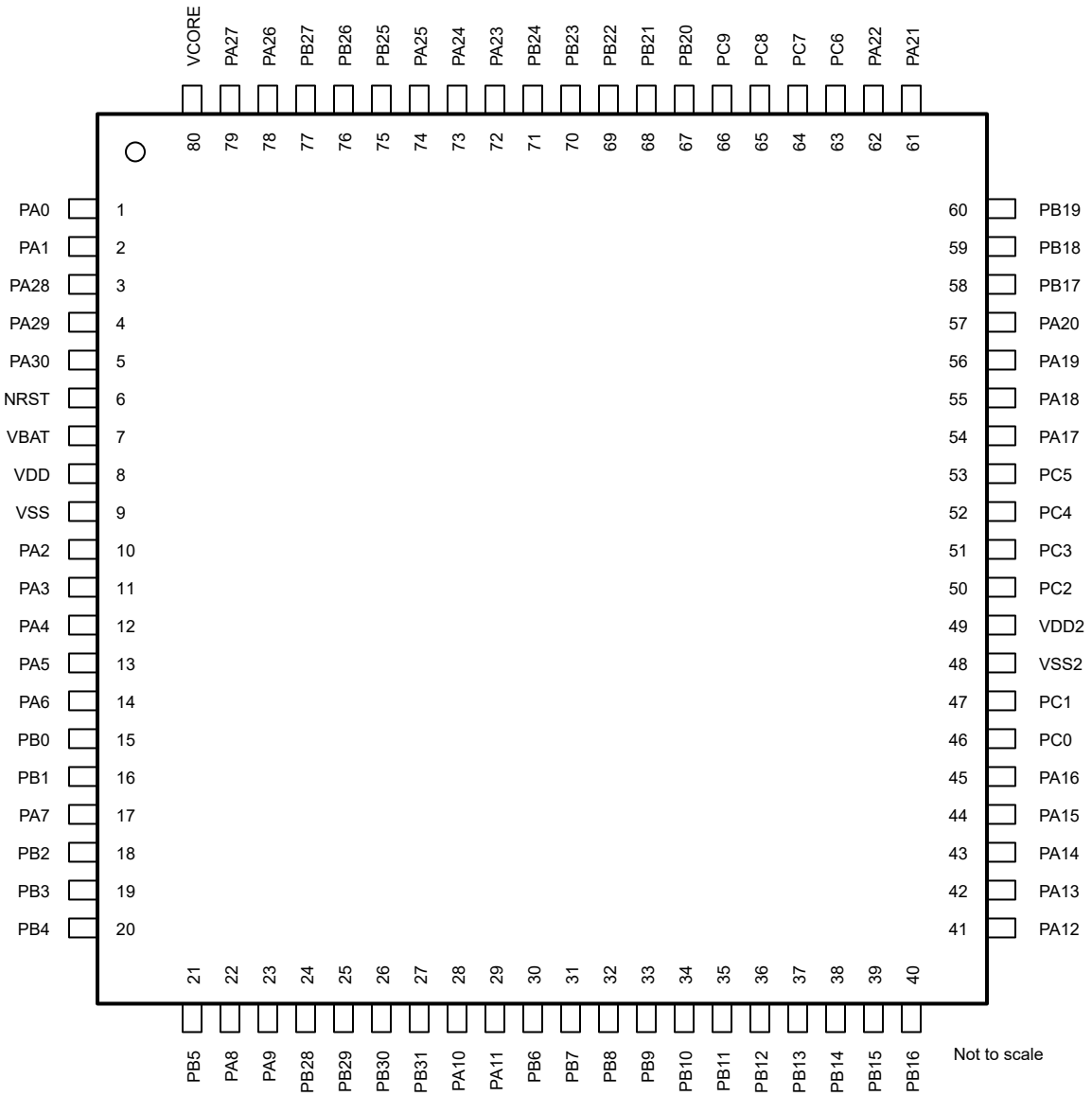


Figure 6-1. 80-pin PN (0.5mm) (LQFP) Package

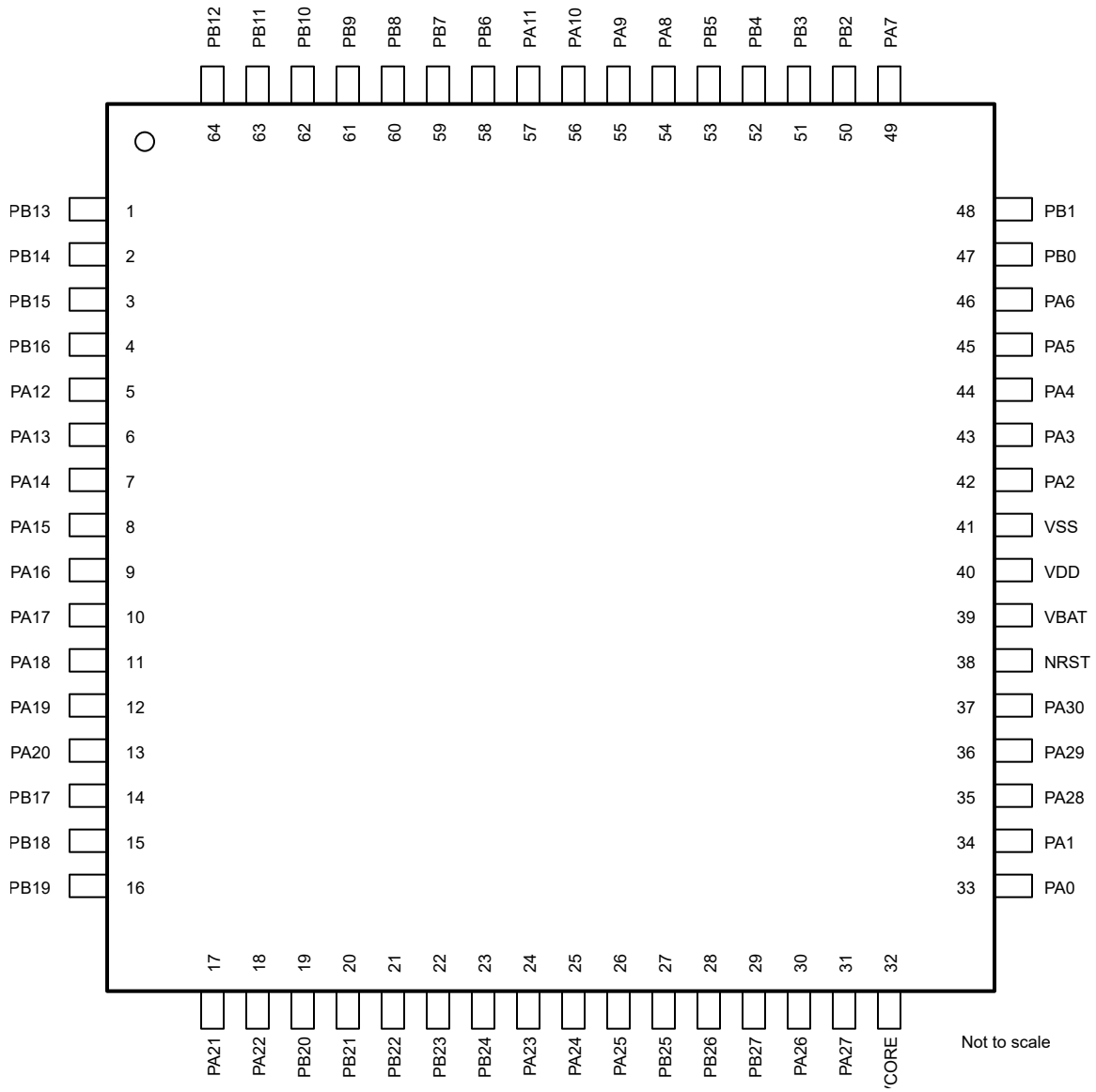


Figure 6-2. 64-pin PM (LQFP) Package

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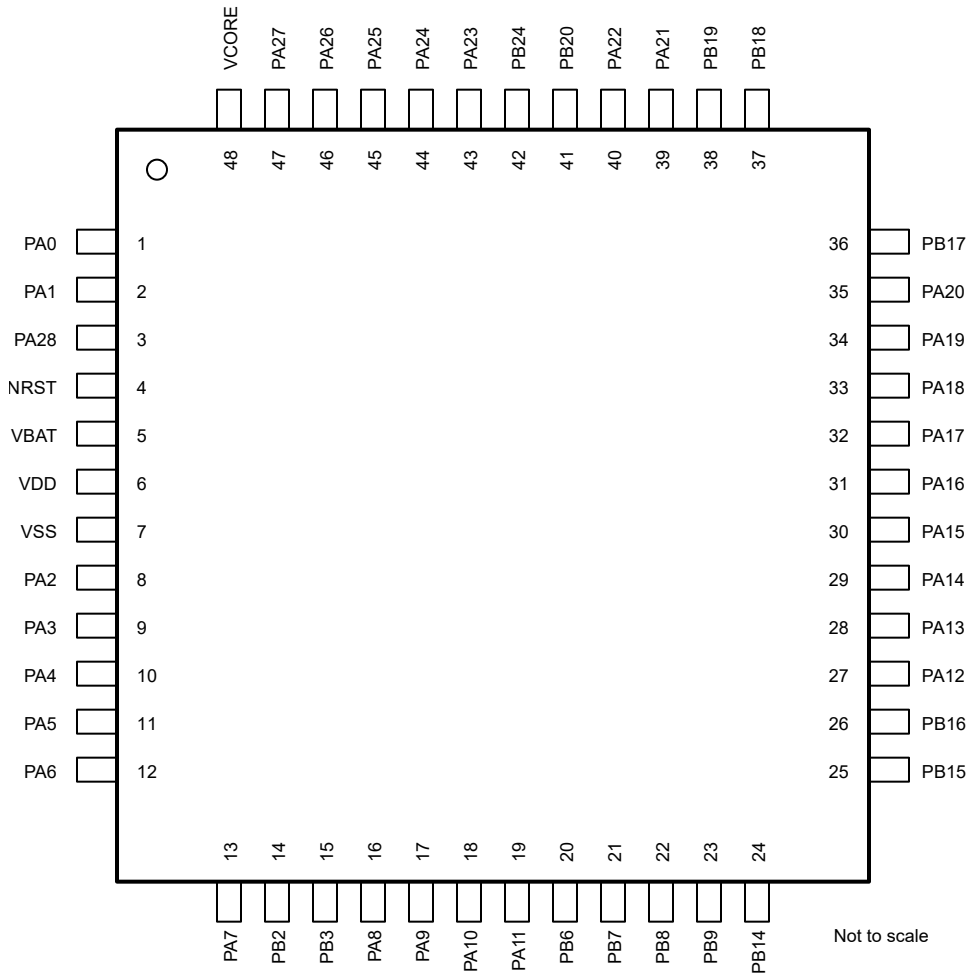


Figure 6-3. 48-pin PT (LQFP) Package

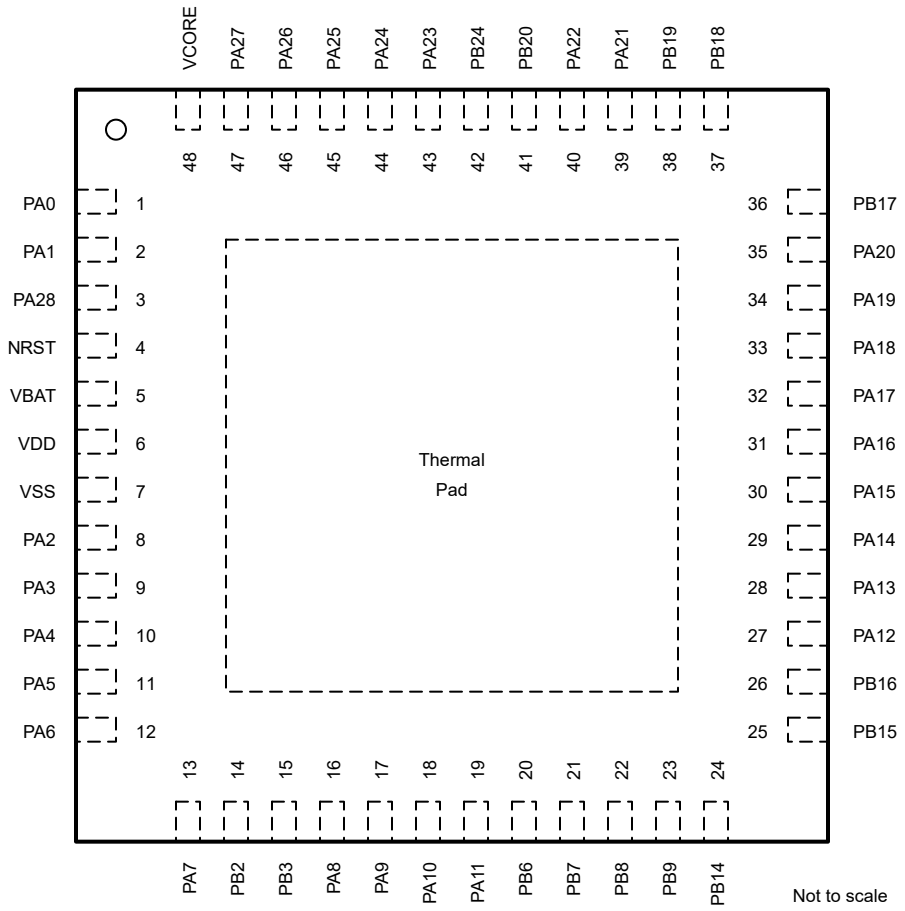
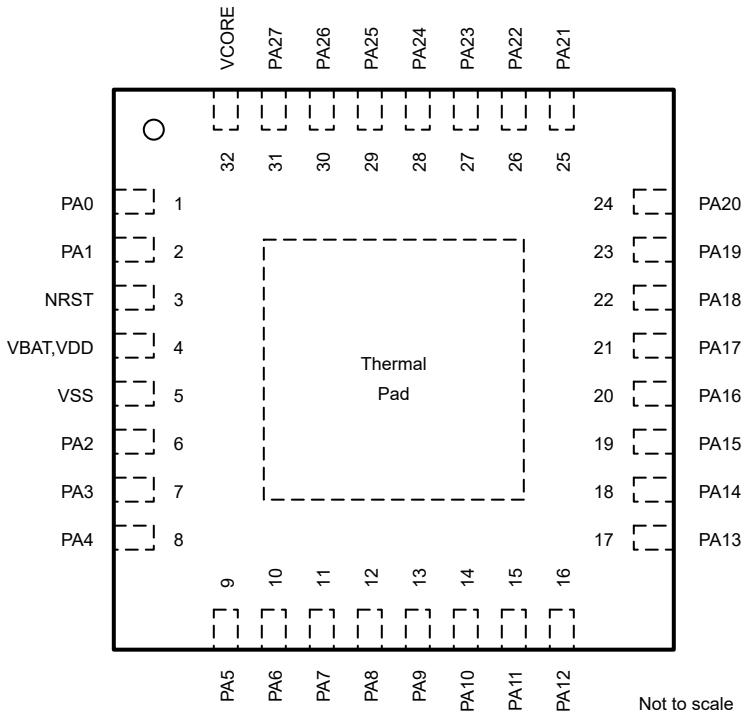


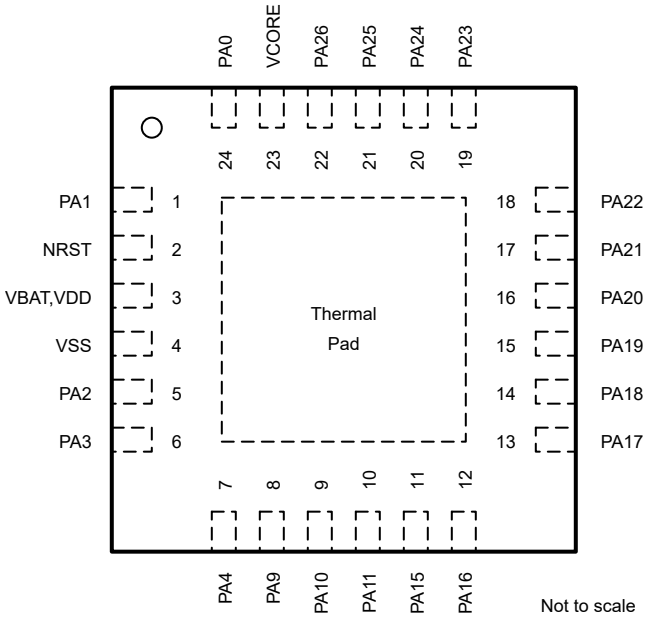
Figure 6-4. 48-pin RGZ (VQFN) Package

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VBAT is internally shorted to VDD on 24 and 32 pin packages.

Figure 6-5. 32-pin RHB (VQFN) Package



VBAT is internally shorted to VDD on 24 and 32 pin packages.

Figure 6-6. 24-pin RGE (VQFN) Package

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in IOMUX are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC	Power Domain
SDIO (standard drive)	Y			Y	Y		VDD
SDIO (standard drive) with wake	Y			Y	Y	Y	VDD
HDIO (High drive)	Y	Y		Y	Y	Y	VDD
ODIO (5V-tolerant open drain)	Y		Y		Y	Y	VDD
LFSSIO	Y			Y	Y		VBAT

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
2	3	4	4	38	6	NRST	NRST	(Non-IOMUX 1) 0	I	RESET
							WAKE	(Non-IOMUX 2) 0	I	
24	1	1	1	33	1	PA0 PINCM1 0x40428000	PA0	1	IO	ODIO (5V-tol)
							UART0_TX	2	O	
							I2C0_SDA	3	IOD	
							TIMA0_C0	4	IO	
							TIMA_FAL1	5	I	
							FCC_IN	6	I	
							TIMG8_C1	7	IO	
							TIMG12_C0	8	IO	
							TIMG0_C0	9	IO	
							BSLSDA	(Non-IOMUX 1) 0	IOD	
							WAKE	(Non-IOMUX 2) 0	I	
1	2	2	2	34	2	PA1 PINCM2 0x40428004	PA1	1	IO	ODIO (5V-tol)
							UART0_RX	2	I	
							I2C0_SCL	3	IOD	
							TIMA0_C1	4	IO	
							TIMA_FAL2	5	I	
							TIMG8_IDX	6	I	
							TIMG8_C0	7	IO	
							TIMG12_C1	8	IO	
							TIMG0_C1	9	IO	
							SPI0_CS3	10	IO	
							BSLSCL	(Non-IOMUX 1) 0	IOD	
							WAKE	(Non-IOMUX 2) 0	I	
5	6	8	8	42	10	PA2 PINCM7 0x40428018	PA2	1	IO	SDIO (standard)
							TIMG8_C1	2	IO	
							SPI0_CS0	3	IO	
							TIMG5_C1	4	IO	
							SPI1_CS0	5	IO	
							TIMA0_C3N	6	O	
							TIMA0_C2N	7	O	
							TIMA_FAL0	8	I	
							TIMA_FAL1	9	I	
							UART4_CTS	10	I	
							TIMA0_C0	11	IO	
							ROSC	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
6	7	9	9	43	11	PA3 PINCM8 0x4042801c	PA3	1	IO	LFSSIO (standard)
							TIMG8_C0	2	IO	
							SPI0_CS1	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C1	5	IO	
							COMP0_OUT	6	O	
							TIMG5_C0	7	IO	
							TIMA0_C2	8	IO	
							UART2_CTS	9	I	
							UART1_TX	10	O	
							SPI0_CS3	11	IO	
							LFXIN	(Non-IOMUX 1) 0	A	
7	8	10	10	44	12	PA4 PINCM9 0x40428020	PA4	1	IO	LFSSIO (standard)
							TIMG8_C1	2	IO	
							SPI0_POCI	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C1N	5	O	
							LFCLK_IN	6	I	
							TIMG5_C1	7	IO	
							TIMA0_C3	8	IO	
							UART2_RTS	9	O	
							UART1_RX	10	I	
							SPI0_CS0	11	IO	
							LFXOUT	(Non-IOMUX 1) 0	A	
	9	11	11	45	13	PA5 PINCM10 0x40428024	PA5	1	IO	SDIO (standard)
							TIMG8_C0	2	IO	
							SPI0_PICO	3	IO	
							I2C1_SDA	4	IOD	
							TIMG0_C0	5	IO	
							FCC_IN	6	I	
							TIMG4_C0	7	IO	
							TIMA_FAL1	8	I	
							UART0_CTS	9	I	
							UART4_RTS	10	O	
							UART1_TX	11	O	
							HFXIN	(Non-IOMUX 1) 0	A	
	10	12	12	46	14	PA6 PINCM11 0x40428028	PA6	1	IO	SDIO (standard)
							TIMG8_C1	2	IO	
							SPI0_SCK	3	IO	
							I2C1_SCL	4	IOD	
							TIMG0_C1	5	IO	
							HFCLK_IN	6	I	
							TIMG4_C1	7	IO	
							TIMA_FAL0	8	I	
							UART0_RTS	9	O	
							TIMA0_C2N	10	O	
							UART1_RX	11	I	
							HFXOUT	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
	11	13	13	49	17	PA7 PINCM14 0x40428034	PA7	1	IO	LFSSIO (standard)
							COMP0_OUT	2	O	
							CLK_OUT	3	O	
							TIMG8_C0	4	IO	
							TIMA0_C2	5	IO	
							TIMG8_IDX	6	I	
							TIMG5_C1	7	IO	
							TIMA0_C1	8	IO	
							SPI0_CS2	9	IO	
							FCC_IN	10	I	
							SPI0_POCI	11	IO	
							TIO0	(Non-IOMUX 1) 0	I	
	12	16	16	54	22	PA8 PINCM19 0x40428048	PA8	1	IO	SDIO (standard)
							UART1_TX	2	O	
							SPI0_CS0	3	IO	
							I2C0_SDA	4	IOD	
							TIMA0_C0	5	IO	
							TIMA_FAL2	6	I	
							TIMA_FAL0	7	I	
							SPI0_CS3	8	IO	
							TIMG5_C1	9	IO	
							HFCLK_IN	10	I	
							UART0_RTS	11	O	
							LCD0	(Non-IOMUX 1) 0	A	
8	13	17	17	55	23	PA9 PINCM20 0x4042804c	PA9	1	IO	SDIO (standard)
							UART1_RX	2	I	
							SPI0_PICO	3	IO	
							I2C0_SCL	4	IOD	
							TIMA0_C0N	5	O	
							CLK_OUT	6	O	
							TIMA0_C1	7	IO	
							RTC_OUT	8	O	
							TIMG5_C0	9	IO	
							UART4_RTS	10	O	
							UART0_CTS	11	I	
							LCD1	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
9	14	18	18	56	28	PA10 PINCM25 0x40428060	PA10	1	IO	HDIO (high drive)
							UART0_TX	2	O	
							SPI0_POCI	3	IO	
							I2C0_SDA	4	IOD	
							TIMA0_C2	5	IO	
							CLK_OUT	6	O	
							TIMG0_C0	7	IO	
							I2C1_SDA	8	IOD	
							TIMG12_C0	9	IO	
							TIMA_FAL1	10	I	
							BSLTX	(Non-IOMUX 1) 0	O	
							WAKE	(Non-IOMUX 2) 0	I	
							LCD2	(Non-IOMUX 3) 0	A	
10	15	19	19	57	29	PA11 PINCM26 0x40428064	PA11	1	IO	HDIO (high drive)
							UART0_RX	2	I	
							SPI0_SCK	3	IO	
							I2C0_SCL	4	IOD	
							TIMA0_C2N	5	O	
							COMP0_OUT	6	O	
							TIMG0_C1	7	IO	
							I2C1_SCL	8	IOD	
							TIMG12_C1	9	IO	
							TIMA_FAL0	10	I	
							BSLRX	(Non-IOMUX 1) 0	I	
							WAKE	(Non-IOMUX 2) 0	I	
							LCD3	(Non-IOMUX 3) 0	A	
	16	27	27	5	41	PA12 PINCM38 0x40428094	PA12	1	IO	SDIO (standard)
							UART3_CTS	2	I	
							SPI0_SCK	3	IO	
							COMP0_OUT	4	O	
							TIMA0_C3	5	IO	
							FCC_IN	6	I	
							TIMG0_C0	7	IO	
							SPI1_CS1	8	IO	
							SPI0_CS1	9	IO	
							UART2_CTS	10	I	
							UART1_CTS	11	I	
							LCD11	(Non-IOMUX 1) 0	A	
							R33	(Non-IOMUX 2) 0	A	
							A_18	(Non-IOMUX 3) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
	17	28	28	6	42	PA13 PINCM39 0x40428098	PA13	1	IO	SDIO (standard)
							UART3_RTS	2	O	
							SPI0_POCI	3	IO	
							UART3_RX	4	I	
							TIMA0_C3N	5	O	
							RTC_OUT	6	O	
							TIMG0_C1	7	IO	
							SPI1_CS0	8	IO	
							SPI0_CS3	9	IO	
							UART2_TX	10	O	
							UART1_RTS	11	O	
							LCD12	(Non-IOMUX 1) 0	A	
							LCDCAP0	(Non-IOMUX 2) 0	A	
							A_17	(Non-IOMUX 3) 0	A	
							COMP0_IN2-	(Non-IOMUX 4) 0	A	
	18	29	29	7	43	PA14 PINCM40 0x4042809c	PA14	1	IO	SDIO (standard)
							UART0_CTS	2	I	
							SPI0_PICO	3	IO	
							UART3_TX	4	O	
							TIMG12_C0	5	IO	
							CLK_OUT	6	O	
							TIMG12_C1	7	IO	
							SPI1_CS2	8	IO	
							SPI0_CS2	9	IO	
							UART2_RX	10	I	
							LCD13	(Non-IOMUX 1) 0	A	
							LCDCAP1	(Non-IOMUX 2) 0	A	
							A_16	(Non-IOMUX 3) 0	A	
							COMP0_IN2+	(Non-IOMUX 4) 0	A	
11	19	30	30	8	44	PA15 PINCM41 0x404280a0	PA15	1	IO	SDIO (standard)
							UART0_RTS	2	O	
							SPI1_CS2	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C2	5	IO	
							I2C2_SCL	6	IOD	
							TIMG8_IDX	7	I	
							TIMG12_C0	8	IO	
							LCDEN	9	A	
							UART2_RTS	10	O	
							LCD14	(Non-IOMUX 1) 0	A	
							A_15	(Non-IOMUX 2) 0	A	
							COMP0_IN3+	(Non-IOMUX 3) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
12	20	31	31	9	45	PA16 PINCM42 0x404280a4	PA16	1	IO	SDIO (standard)
							COMP0_OUT	2	O	
							SPI1_POCI	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C2N	5	O	
							I2C2_SDA	6	IOD	
							FCC_IN	7	I	
							TIMG12_C1	8	IO	
							LCDSON	9	IO	
							UART2_CTS	10	I	
							LCD15	(Non-IOMUX 1) 0	A	
							A_14	(Non-IOMUX 2) 0	A	
13	21	32	32	10	54	PA17 PINCM49 0x404280c0	PA17	1	IO	SDIO (standard with wake)
							UART1_TX	2	O	
							SPI1_SCK	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C3	5	IO	
							TIMG5_C0	6	IO	
							TIMG8_C0	7	IO	
							TIMG12_C0	8	IO	
							SPI0_CS1	9	IO	
							LCDLFCLK	10	IO	
							WAKE	(Non-IOMUX 1) 0	I	
							LCD16	(Non-IOMUX 2) 0	A	
							A_13	(Non-IOMUX 3) 0	A	
							COMP0_IN1-	(Non-IOMUX 4) 0	A	
14	22	33	33	11	55	PA18 PINCM50 0x404280c4	PA18	1	IO	SDIO (standard with wake)
							UART1_RX	2	I	
							SPI1_PICO	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C3N	5	O	
							TIMG5_C1	6	IO	
							TIMG8_C1	7	IO	
							TIMG12_C1	8	IO	
							SPI0_CS0	9	IO	
							LCDEN	10	A	
							BSL_invoke	(Non-IOMUX 1) 0	I	
							WAKE	(Non-IOMUX 2) 0	I	
							LCD17	(Non-IOMUX 3) 0	A	
							A_12	(Non-IOMUX 4) 0	A	
							COMP0_IN1+	(Non-IOMUX 5) 0	A	
15	23	34	34	12	56	PA19 PINCM51 0x404280c8	PA19	1	IO	SDIO (standard)
							SWDIO	2	IO	
							SPI1_POCI	3	IO	
							I2C1_SDA	4	IOD	
							TIMA0_C2	5	IO	
							TIMG0_C0	6	IO	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
16	24	35	35	13	57	PA20 PINCM52 0x404280cc	PA20	1	IO	SDIO (standard)
							SWCLK	2	I	
							SPI1_SCK	3	IO	
							I2C1_SCL	4	IOD	
							TIMA0_C2N	5	O	
							TIMG0_C1	6	IO	
17	25	39	39	17	61	PA21 PINCM56 0x404280dc	PA21	1	IO	SDIO (standard)
							UART2_TX	2	O	
							SPI0_CS3	3	IO	
							UART1_CTS	4	I	
							TIMA0_C0	5	IO	
							TIMG4_C0	6	IO	
							SPI1_CS1	7	IO	
							UART2_CTS	8	I	
							UART4_RTS	9	O	
							TIMG8_C0	10	IO	
							LCD21	(Non-IOMUX 1) 0	A	
							A_8	(Non-IOMUX 2) 0	A	
							VREF-	(Non-IOMUX 3) 0	A	
18	26	40	40	18	62	PA22 PINCM57 0x404280e0	PA22	1	IO	SDIO (standard)
							UART2_RX	2	I	
							SPI0_CS2	3	IO	
							UART1_RTS	4	O	
							TIMA0_C0N	5	O	
							TIMG4_C1	6	IO	
							TIMA0_C1	7	IO	
							CLK_OUT	8	O	
							I2C0_SCL	9	IOD	
							TIMG8_C1	10	IO	
							LCD22	(Non-IOMUX 1) 0	A	
							A_7	(Non-IOMUX 2) 0	A	
19	27	43	43	24	72	PA23 PINCM67 0x40428108	PA23	1	IO	SDIO (standard)
							UART2_TX	2	O	
							SPI0_CS3	3	IO	
							I2C2_SCL	4	IOD	
							TIMA0_C3	5	IO	
							TIMG8_C0	6	IO	
							TIMG5_C0	7	IO	
							UART3_CTS	8	I	
							TIMG0_C0	9	IO	
							SPI1_CS1	10	IO	
							LCD25	(Non-IOMUX 1) 0	A	
							VREF+	(Non-IOMUX 2) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
20	28	44	44	25	73	PA24 PINCM68 0x4042810c	PA24	1	IO	SDIO (standard)
							UART2_RX	2	I	
							SPI0_CS2	3	IO	
							I2C2_SDA	4	IOD	
							TIMA0_C3N	5	O	
							TIMG8_C1	6	IO	
							TIMG5_C1	7	IO	
							UART3_RTS	8	O	
							TIMG0_C1	9	IO	
							SPI1_CS2	10	IO	
							LCD26	(Non-IOMUX 1) 0	A	
							A_3	(Non-IOMUX 2) 0	A	
21	29	45	45	26	74	PA25 PINCM69 0x40428110	PA25	1	IO	SDIO (standard)
							UART3_RX	2	I	
							SPI1_CS3	3	IO	
							TIMG12_C1	4	IO	
							TIMA0_C3	5	IO	
							TIMA0_C1N	6	O	
							COMP0_OUT	7	O	
							UART2_CTS	8	I	
							UART3_TX	9	O	
							TIMG4_C0	10	IO	
							LCD27	(Non-IOMUX 1) 0	A	
							A_2	(Non-IOMUX 2) 0	A	
22	30	46	46	30	78	PA26 PINCM73 0x40428120	PA26	1	IO	SDIO (standard)
							UART3_TX	2	O	
							SPI1_CS0	3	IO	
							TIMG8_C0	4	IO	
							TIMA_FAL0	5	I	
							TIMA0_C3N	6	O	
							TIMG5_C0	7	IO	
							UART2_RTS	8	O	
							UART3_RX	9	I	
							TIMG4_C1	10	IO	
							LCD28	(Non-IOMUX 1) 0	A	
							A_1	(Non-IOMUX 2) 0	A	
							COMP0_IN0+	(Non-IOMUX 3) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
	31	47	47	31	79	PA27 PINCM74 0x40428124	PA27	1	IO	SDIO (standard)
							UART3_RX	2	I	
							SPI1_CS1	3	IO	
							TIMG8_C1	4	IO	
							TIMA_FAL2	5	I	
							CLK_OUT	6	O	
							TIMG5_C1	7	IO	
							RTC_OUT	8	O	
							COMP0_OUT	9	O	
							LCD29	(Non-IOMUX 1) 0	A	
							A_0	(Non-IOMUX 2) 0	A	
							COMP0_IN0-	(Non-IOMUX 3) 0	A	
		3	3	35	3	PA28 PINCM3 0x40428008	PA28	1	IO	HDIO (high drive)
							UART0_TX	2	O	
							I2C0_SDA	3	IOD	
							TIMA0_C3	4	IO	
							TIMA_FAL0	5	I	
							TIMG5_C0	6	IO	
							TIMA0_C1	7	IO	
							WAKE	(Non-IOMUX 1) 0	I	
							LCD30	(Non-IOMUX 2) 0	A	
				36	4	PA29 PINCM4 0x4042800c	PA29	1	IO	SDIO (standard)
							I2C1_SCL	2	IOD	
							UART2_RTS	3	O	
							TIMG8_C0	4	IO	
							TIMG4_C0	5	IO	
							I2C2_SCL	6	IOD	
							UART0_CTS	7	I	
							SPI0_CS3	8	IO	
							LCD31	(Non-IOMUX 1) 0	A	
				37	5	PA30 PINCM5 0x40428010	PA30	1	IO	SDIO (standard)
							I2C1_SDA	2	IOD	
							UART2_CTS	3	I	
							TIMG8_C1	4	IO	
							TIMG4_C1	5	IO	
							I2C2_SDA	6	IOD	
							UART0_RTS	7	O	
							SPI0_CS2	8	IO	
							LCD32	(Non-IOMUX 1) 0	A	
				47	15	PB0 PINCM12 0x4042802c	PB0	1	IO	SDIO (standard)
							UART0_TX	2	O	
							SPI1_CS2	3	IO	
							I2C0_SCL	4	IOD	
							TIMA0_C2	5	IO	
							TIMG0_C0	6	IO	
							SPI0_CS3	7	IO	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
				48	16	PB1 PINCM13 0x40428030	PB1	1	IO	SDIO (standard)
							UART0_RX	2	I	
							SPI1_CS3	3	IO	
							I2C0_SDA	4	IOD	
							TIMA0_C2N	5	O	
							TIMG0_C1	6	IO	
							SPI0_CS2	7	IO	
		14	14	50	18	PB2 PINCM15 0x40428038	PB2	1	IO	LFSSIO (standard)
							UART3_TX	2	O	
							UART2_CTS	3	I	
							I2C1_SCL	4	IOD	
							TIMA0_C3	5	IO	
							UART1_CTS	6	I	
							TIMG4_C0	7	IO	
							UART2_TX	8	O	
							TIMG12_C0	9	IO	
							HFCLK_IN	10	I	
							SPI0_PICO	11	IO	
							TIO1	(Non-IOMUX 1) 0	I	
		15	15	51	19	PB3 PINCM16 0x4042803c	PB3	1	IO	LFSSIO (standard)
							UART3_RX	2	I	
							UART2_RTS	3	O	
							I2C1_SDA	4	IOD	
							TIMA0_C3N	5	O	
							UART1_RTS	6	O	
							TIMG4_C1	7	IO	
							UART2_RX	8	I	
							TIMG12_C1	9	IO	
							TIMA0_C0	10	IO	
							SPI0_SCK	11	IO	
							TIO2	(Non-IOMUX 1) 0	I	
				52	20	PB4 PINCM17 0x40428040	PB4	1	IO	SDIO (standard)
							UART1_TX	2	O	
							UART3_CTS	3	I	
							TIMA0_C1	4	IO	
							TIMA0_C2	5	IO	
							TIMG0_C0	6	IO	
							TIMG4_C0	7	IO	
							LCD33	(Non-IOMUX 1) 0	A	
				53	21	PB5 PINCM18 0x40428044	PB5	1	IO	SDIO (standard)
							UART1_RX	2	I	
							UART3_RTS	3	O	
							TIMA0_C1N	4	O	
							TIMA0_C2N	5	O	
							TIMG0_C1	6	IO	
							TIMG4_C1	7	IO	
							LCD34	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
		20	20	58	30	PB6 PINCM27 0x40428068	PB6	1	IO	SDIO (standard)
							UART1_TX	2	O	
							SPI1_CS0	3	IO	
							I2C2_SCL	4	IOD	
							TIMG8_C0	5	IO	
							UART2_CTS	6	I	
							TIMG4_C0	7	IO	
							TIMA_FAL2	8	I	
							SPI0_CS1	9	IO	
							TIMG12_C0	10	IO	
							LCD4	(Non-IOMUX 1) 0	A	
		21	21	59	31	PB7 PINCM28 0x4042806c	PB7	1	IO	SDIO (standard)
							UART1_RX	2	I	
							SPI1_POCI	3	IO	
							I2C2_SDA	4	IOD	
							TIMG8_C1	5	IO	
							UART2_RTS	6	O	
							TIMG4_C1	7	IO	
							LCDLFCLK	8	IO	
							SPI0_CS2	9	IO	
							TIMG12_C1	10	IO	
							LCD5	(Non-IOMUX 1) 0	A	
		22	22	60	32	PB8 PINCM29 0x40428070	PB8	1	IO	SDIO (standard)
							UART1_CTS	2	I	
							SPI1_PICO	3	IO	
							I2C2_SCL	4	IOD	
							TIMA0_C0	5	IO	
							COMP0_OUT	6	O	
							TIMG4_C0	7	IO	
							LCDSON	8	IO	
							LCD6	(Non-IOMUX 1) 0	A	
		23	23	61	33	PB9 PINCM30 0x40428074	PB9	1	IO	SDIO (standard)
							UART1_RTS	2	O	
							SPI1_SCK	3	IO	
							I2C2_SDA	4	IOD	
							TIMA0_C0N	5	O	
							TIMA0_C1	6	IO	
							TIMG4_C1	7	IO	
							LCDEN	8	A	
							LCD7	(Non-IOMUX 1) 0	A	
				62	34	PB10 PINCM31 0x40428078	PB10	1	IO	SDIO (standard)
							TIMG0_C0	2	IO	
							TIMG8_C0	3	IO	
							COMP0_OUT	4	O	
							TIMG4_C0	5	IO	
							UART4_TX	6	O	
							SPI1_CS3	7	IO	
							LCD35	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
				63	35	PB11 PINCM32 0x4042807c	PB11	1	IO	SDIO (standard)
							TIMG0_C1	2	IO	
							TIMG8_C1	3	IO	
							CLK_OUT	4	O	
							TIMG4_C1	5	IO	
							UART4_RX	6	I	
							SPI1_CS2	7	IO	
							LCD36	(Non-IOMUX 1) 0	A	
				64	36	PB12 PINCM33 0x40428080	PB12	1	IO	SDIO (standard)
							UART3_TX	2	O	
							TIMA0_C2	3	IO	
							TIMA_FAL1	4	I	
							TIMA0_C1	5	IO	
							UART4_CTS	6	I	
							SPI1_CS1	7	IO	
							LCD37	(Non-IOMUX 1) 0	A	
				1	37	PB13 PINCM34 0x40428084	PB13	1	IO	SDIO (standard)
							UART3_RX	2	I	
							TIMA0_C3	3	IO	
							TIMG12_C0	4	IO	
							TIMA0_C1N	5	O	
							UART4_RTS	6	O	
							SPI1_CS0	7	IO	
							LCD38	(Non-IOMUX 1) 0	A	
		24	24	2	38	PB14 PINCM35 0x40428088	PB14	1	IO	SDIO (standard)
							SPI1_CS3	2	IO	
							SPI1_POCI	3	IO	
							TIMG12_C1	4	IO	
							TIMA0_C0	5	IO	
							TIMG8_IDX	6	I	
							SPI0_CS3	7	IO	
							LCD8	(Non-IOMUX 1) 0	A	
							R13	(Non-IOMUX 2) 0	A	
							A_21	(Non-IOMUX 3) 0	A	
		25	25	3	39	PB15 PINCM36 0x4042808c	PB15	1	IO	SDIO (standard)
							UART2_TX	2	O	
							SPI1_PICO	3	IO	
							UART3_CTS	4	I	
							TIMG8_C0	5	IO	
							TIMG5_C0	6	IO	
							I2C2_SCL	7	IOD	
							LCD9	(Non-IOMUX 1) 0	A	
							R24	(Non-IOMUX 2) 0	A	
							A_20	(Non-IOMUX 3) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
		26	26	4	40	PB16 PINCM37 0x40428090	PB16	1	IO	SDIO (standard)
							UART2_RX	2	I	
							SPI1_SCK	3	IO	
							UART3_RTS	4	O	
							TIMG8_C1	5	IO	
							TIMG5_C1	6	IO	
							I2C2_SDA	7	IOD	
							LCD10	(Non-IOMUX 1) 0	A	
							R23	(Non-IOMUX 2) 0	A	
							A_19	(Non-IOMUX 3) 0	A	
		36	36	14	58	PB17 PINCM53 0x404280d0	PB17	1	IO	SDIO (standard)
							UART2_TX	2	O	
							SPI0_PICO	3	IO	
							I2C0_SCL	4	IOD	
							TIMA0_C2	5	IO	
							TIMG0_C0	6	IO	
							SPI1_CS1	7	IO	
							UART4_TX	8	O	
							TIMG4_C0	9	IO	
							LCDSON	10	IO	
							LCD18	(Non-IOMUX 1) 0	A	
							A_11	(Non-IOMUX 2) 0	A	
		37	37	15	59	PB18 PINCM54 0x404280d4	PB18	1	IO	SDIO (standard)
							UART2_RX	2	I	
							SPI0_SCK	3	IO	
							I2C0_SDA	4	IOD	
							TIMA0_C2N	5	O	
							TIMG0_C1	6	IO	
							SPI1_CS2	7	IO	
							UART4_RX	8	I	
							TIMG4_C1	9	IO	
							LCDLFCLK	10	IO	
							LCD19	(Non-IOMUX 1) 0	A	
							A_10	(Non-IOMUX 2) 0	A	
		38	38	16	60	PB19 PINCM55 0x404280d8	PB19	1	IO	SDIO (standard)
							COMP0_OUT	2	O	
							SPI0_POCI	3	IO	
							TIMG8_C1	4	IO	
							UART0_CTS	5	I	
							TIMG5_C1	6	IO	
							TIMG8_IDX	7	I	
							UART2_CTS	8	I	
							UART4_CTS	9	I	
							SPI1_CS3	10	IO	
							LCD20	(Non-IOMUX 1) 0	A	
							A_9	(Non-IOMUX 2) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
		41	41	19	67	PB20 PINCM62 0x404280f4	PB20	1	IO	SDIO (standard)
							SPI0_CS2	2	IO	
							SPI1_CS0	3	IO	
							TIMG12_C0	4	IO	
							TIMA0_C2	5	IO	
							TIMA_FAL1	6	I	
							TIMA0_C1	7	IO	
							UART2_RTS	8	O	
							I2C0_SDA	9	IOD	
							LCD23	(Non-IOMUX 1) 0	A	
							A_6	(Non-IOMUX 2) 0	A	
				20	68	PB21 PINCM63 0x404280f8	PB21	1	IO	SDIO (standard)
							UART4_TX	2	O	
							SPI1_POCI	3	IO	
							I2C0_SCL	4	IOD	
							TIMG8_C0	5	IO	
							UART1_TX	6	O	
							LCD39	(Non-IOMUX 1) 0	A	
							A_25	(Non-IOMUX 2) 0	A	
				21	69	PB22 PINCM64 0x404280fc	PB22	1	IO	SDIO (standard)
							UART4_RX	2	I	
							SPI1_PICO	3	IO	
							I2C0_SDA	4	IOD	
							TIMG8_C1	5	IO	
							UART1_RX	6	I	
							LCD40	(Non-IOMUX 1) 0	A	
							A_24	(Non-IOMUX 2) 0	A	
				22	70	PB23 PINCM65 0x40428100	PB23	1	IO	SDIO (standard)
							UART1_CTS	2	I	
							SPI1_SCK	3	IO	
							TIMA_FAL0	4	I	
							COMP0_OUT	5	O	
							LCD41	(Non-IOMUX 1) 0	A	
		42	42	23	71	PB24 PINCM66 0x40428104	PB24	1	IO	SDIO (standard)
							SPI0_CS3	2	IO	
							SPI0_CS1	3	IO	
							TIMG12_C1	4	IO	
							TIMA0_C3	5	IO	
							TIMA0_C1N	6	O	
							SPI1_CS1	7	IO	
							UART2_RTS	8	O	
							LCD24	(Non-IOMUX 1) 0	A	
							A_5	(Non-IOMUX 2) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
				27	75	PB25 PINCM70 0x40428114	PB25	1	IO	SDIO (standard)
							UART0_CTS	2	I	
							SPI0_CS0	3	IO	
							TIMA_FAL0	4	I	
							TIMA_FAL1	5	I	
							TIMA_FAL2	6	I	
							COMP0_OUT	7	O	
							FCC_IN	8	I	
							LCD42	(Non-IOMUX 1) 0	A	
							A_4	(Non-IOMUX 2) 0	A	
				28	76	PB26 PINCM71 0x40428118	PB26	1	IO	SDIO (standard)
							UART0_RTS	2	O	
							SPI0_CS1	3	IO	
							TIMA0_C0	4	IO	
							TIMA0_C3	5	IO	
							TIMG4_C0	6	IO	
							COMP0_OUT	7	O	
							FCC_IN	8	I	
							LCD43	(Non-IOMUX 1) 0	A	
							A_23	(Non-IOMUX 2) 0	A	
				29	77	PB27 PINCM72 0x4042811c	PB27	1	IO	SDIO (standard)
							COMP0_OUT	2	O	
							SPI1_CS1	3	IO	
							TIMA0_C0N	4	O	
							TIMA0_C3N	5	O	
							TIMG4_C1	6	IO	
							LCD44	(Non-IOMUX 1) 0	A	
							A_22	(Non-IOMUX 2) 0	A	
					24	PB28 PINCM21 0x40428050	PB28	1	IO	SDIO (standard)
							I2C2_SCL	2	IOD	
							SPI1_CS0	3	IO	
							TIMA_FAL0	4	I	
							TIMA0_C0	5	IO	
							TIMG0_C0	6	IO	
							LCD45	(Non-IOMUX 1) 0	A	
					25	PB29 PINCM22 0x40428054	PB29	1	IO	SDIO (standard)
							I2C2_SDA	2	IOD	
							SPI1_POCI	3	IO	
							TIMA_FAL1	4	I	
							TIMA0_C0N	5	O	
							TIMG0_C1	6	IO	
							LCD46	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
					26	PB30 PINCM23 0x40428058	PB30	1	IO	SDIO (standard)
							UART1_CTS	2	I	
							SPI1_PICO	3	IO	
							TIMA_FAL2	4	I	
							TIMA0_C1	5	IO	
							TIMG4_C0	6	IO	
							LCD47	(Non-IOMUX 1) 0	A	
					27	PB31 PINCM24 0x4042805c	PB31	1	IO	SDIO (standard)
							UART1_RTS	2	O	
							SPI1_SCK	3	IO	
							TIMG8_IDX	4	I	
							TIMA0_C1N	5	O	
							TIMG4_C1	6	IO	
							LCD48	(Non-IOMUX 1) 0	A	
					46	PC0 PINCM43 0x404280a8	PC0	1	IO	SDIO (standard)
							UART1_TX	2	O	
							SPI1_CS3	3	IO	
							TIMG8_C0	4	IO	
							TIMA0_C2	5	IO	
							LCD49	(Non-IOMUX 1) 0	A	
					47	PC1 PINCM44 0x404280ac	PC1	1	IO	SDIO (standard)
							UART1_RX	2	I	
							SPI1_CS2	3	IO	
							TIMG8_C1	4	IO	
							TIMA0_C2N	5	O	
							LCD50	(Non-IOMUX 1) 0	A	
					50	PC2 PINCM45 0x404280b0	PC2	1	IO	SDIO (standard)
							I2C2_SCL	2	IOD	
							SPI1_CS0	3	IO	
							TIMA_FAL0	4	I	
							TIMA0_C0	5	IO	
							TIMG0_C0	6	IO	
							LCD51	(Non-IOMUX 1) 0	A	
					51	PC3 PINCM46 0x404280b4	PC3	1	IO	SDIO (standard)
							I2C2_SDA	2	IOD	
							SPI1_CS1	3	IO	
							TIMA_FAL1	4	I	
							TIMA0_C0N	5	O	
							TIMG0_C1	6	IO	
							LCD52	(Non-IOMUX 1) 0	A	
					52	PC4 PINCM47 0x404280b8	PC4	1	IO	SDIO (standard)
							UART3_CTS	2	I	
							SPI1_CS2	3	IO	
							TIMA_FAL2	4	I	
							TIMA0_C1	5	IO	
							TIMG4_C0	6	IO	
							LCD53	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (RGE, PM, PN, RHB, PT, RGZ Packages) (continued)

RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
					53	PC5 PINCM48 0x404280bc	PC5	1	IO	SDIO (standard)
							UART3_RTS	2	O	
							SPI1_CS3	3	IO	
							TIMG8_IDX	4	I	
							TIMA0_C1N	5	O	
							TIMG4_C1	6	IO	
							LCD54	(Non-IOMUX 1) 0	A	
					63	PC6 PINCM58 0x404280e4	PC6	1	IO	SDIO (standard)
							UART3_TX	2	O	
							SPI0_CS1	3	IO	
							TIMG8_C0	4	IO	
							TIMA0_C0	5	IO	
							LCD55	(Non-IOMUX 1) 0	A	
					64	PC7 PINCM59 0x404280e8	PC7	1	IO	SDIO (standard)
							UART3_RX	2	I	
							SPI0_CS0	3	IO	
							TIMG8_C1	4	IO	
							TIMA0_C0N	5	O	
							LCD56	(Non-IOMUX 1) 0	A	
					65	PC8 PINCM60 0x404280ec	PC8	1	IO	SDIO (standard)
							UART3_CTS	2	I	
							SPI1_CS2	3	IO	
							TIMG5_C0	4	IO	
							TIMA0_C1	5	IO	
							LCD57	(Non-IOMUX 1) 0	A	
					66	PC9 PINCM61 0x404280f0	PC9	1	IO	SDIO (standard)
							UART3_RTS	2	O	
							SPI1_CS1	3	IO	
							TIMG5_C1	4	IO	
							TIMA0_C1N	5	O	
							LCD58	(Non-IOMUX 1) 0	A	
3	4	5	5	39	7	VBAT	VBAT	(Non-IOMUX 1) 0	PWR	PWR
23	32	48	48	32	80	VCORE	VCORE	(Non-IOMUX 1) 0	PWR	PWR
3	4	6	6	40	8	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
					49	VDD2	VDD2	(Non-IOMUX 1) 0	PWR	PWR
4	5	7	7	41	9	VSS	VSS	(Non-IOMUX 1) 0	PWR	PWR
					48	VSS2	VSS2	(Non-IOMUX 1) 0	PWR	PWR

6.3 Signal Descriptions

Many MSPM0 signals are made available on multiple device pins. The following list describes the column headers:

1. **SIGNAL NAME**: The name of the signal which can be connected to one of the specified pins.
2. **PIN TYPE**: The signal direction and signal type:
   - I = Input
   - O = Output
   - IO = Input, output, or simultaneous input and output
   - ID = Input with open-drain behavior

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- OD = Output with open-drain behavior
- IOD = Input, output, or simultaneous input and output with open-drain behavior
- A = Analog
- PWR = Power function

3. **DESCRIPTION**: A description of the signal.
4. **PIN**: Associated pin number.

For additional information on the pin multiplexing scheme, refer to the IOMUX chapter of the .

Note

The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
A_0	A	ADC analog input channel 0		31	47	47	31	79
A_1	A	ADC analog input channel 1	22	30	46	46	30	78
A_2	A	ADC analog input channel 2	21	29	45	45	26	74
A_3	A	ADC analog input channel 3	20	28	44	44	25	73
A_4	A	ADC analog input channel 4					27	75
A_5	A	ADC analog input channel 5			42	42	23	71
A_6	A	ADC analog input channel 6			41	41	19	67
A_7	A	ADC analog input channel 7	18	26	40	40	18	62
A_8	A	ADC analog input channel 8	17	25	39	39	17	61
A_9	A	ADC analog input channel 9			38	38	16	60
A_10	A	ADC analog input channel 10			37	37	15	59
A_11	A	ADC analog input channel 11			36	36	14	58
A_12	A	ADC analog input channel 12	14	22	33	33	11	55
A_13	A	ADC analog input channel 13	13	21	32	32	10	54
A_14	A	ADC analog input channel 14	12	20	31	31	9	45
A_15	A	ADC analog input channel 15	11	19	30	30	8	44
A_16	A	ADC analog input channel 16		18	29	29	7	43
A_17	A	ADC analog input channel 17		17	28	28	6	42
A_18	A	ADC analog input channel 18		16	27	27	5	41
A_19	A	ADC analog input channel 19			26	26	4	40
A_20	A	ADC analog input channel 20			25	25	3	39
A_21	A	ADC analog input channel 21			24	24	2	38
A_22	A	ADC analog input channel 22					29	77
A_23	A	ADC analog input channel 23					28	76
A_24	A	ADC analog input channel 24					21	69
A_25	A	ADC analog input channel 25					20	68

Table 6-4. Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
BSLRX	I	BSL UART receive signal (RXD)	10	15	19	19	57	29

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Table 6-4. Bootstrap Loader (BSL) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
BSLSCL	IOD	BSL I2C clock signal (SCL)	1	2	2	2	34	2
BSLSDA	IOD	BSL I2C data signal (SDA)	24	1	1	1	33	1
BSLTX	O	BSL UART transmit signal (TXD)	9	14	18	18	56	28
BSL_invoke	I	BSL invoke signal (if BSL is enabled, must be HIGH during BOOTRST for a BSL entry, and LOW during BOOTRST to prevent BSL entry)	14	22	33	33	11	55

Table 6-5. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
CLK_OUT	O	CLK_OUT digital clock output from the PMCU	18, 8, 9	11, 13, 14, 18, 26, 31	13, 17, 18, 29, 40, 47	13, 17, 18, 29, 40, 47	18, 31, 49, 55, 56, 63, 7	17, 23, 28, 35, 43, 62, 79
FCC_IN	I	Frequency clock counter (FCC) input signal	12, 24	1, 11, 16, 20, 9	1, 11, 13, 27, 31	1, 11, 13, 27, 31	27, 28, 33, 45, 49, 5, 9	1, 13, 17, 41, 45, 75, 76
HFCLK_IN	I	High frequency clock digital clock input signal		10, 12	12, 14, 16	12, 14, 16	46, 50, 54	14, 18, 22
HFXIN	A	High frequency crystal oscillator (HFXT) signal		9	11	11	45	13
HFXOUT	A	High frequency crystal oscillator (HFXT) signal		10	12	12	46	14
LFCLK_IN	I	Low frequency clock digital clock input signal	7	8	10	10	44	12
LFXIN	A	Low frequency crystal oscillator (LFXT) signal	6	7	9	9	43	11
LFXOUT	A	Low frequency crystal oscillator (LFXT) signal	7	8	10	10	44	12
ROSC	A	SYSOSC frequency correction loop (FCL) external resistor signal	5	6	8	8	42	10

Table 6-6. Comparator (COMP) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PNA PIN
COMP0_OUT	O	COMP0 digital output signal	10, 12, 21, 6	11, 15, 16, 20, 29, 31, 7	13, 19, 22, 27, 31, 38, 45, 47, 9	13, 19, 22, 27, 31, 38, 45, 47, 9	16, 22, 26, 27, 28, 29, 31, 43, 49, 5, 57, 60, 62, 9	11, 17, 29, 32, 34, 41, 45, 60, 70, 74, 75, 76, 77, 79	11, 17, 29, 32, 34, 41, 45, 60, 70, 74, 75, 76, 77, 79
COMP0_IN0+	A	COMP0 non-inverting input channel 0	22	30	46	46	30	78	78
COMP0_IN0-	A	COMP0 inverting input channel 0		31	47	47	31	79	79
COMP0_IN1+	A	COMP0 non-inverting input channel 1	14	22	33	33	11	55	55
COMP0_IN1-	A	COMP0 inverting input channel 1	13	21	32	32	10	54	54
COMP0_IN2+	A	COMP0 non-inverting input channel 2		18	29	29	7	43	43
COMP0_IN2-	A	COMP0 inverting input channel 2		17	28	28	6	42	42

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Table 6-6. Comparator (COMP) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN	PNA PIN
COMP0_IN3+	A	COMP0 non-inverting input channel 3	11	19	30	30	8	44	44

Table 6-7. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
PA0	IO	GPIO port A input/output 0	24	1	1	1	33	1
PA1	IO	GPIO port A input/output 1	1	2	2	2	34	2
PA2	IO	GPIO port A input/output 2	5	6	8	8	42	10
PA3	IO	GPIO port A input/output 3	6	7	9	9	43	11
PA4	IO	GPIO port A input/output 4	7	8	10	10	44	12
PA5	IO	GPIO port A input/output 5		9	11	11	45	13
PA6	IO	GPIO port A input/output 6		10	12	12	46	14
PA7	IO	GPIO port A input/output 7		11	13	13	49	17
PA8	IO	GPIO port A input/output 8		12	16	16	54	22
PA9	IO	GPIO port A input/output 9	8	13	17	17	55	23
PA10	IO	GPIO port A input/output 10	9	14	18	18	56	28
PA11	IO	GPIO port A input/output 11	10	15	19	19	57	29
PA12	IO	GPIO port A input/output 12		16	27	27	5	41
PA13	IO	GPIO port A input/output 13		17	28	28	6	42
PA14	IO	GPIO port A input/output 14		18	29	29	7	43
PA15	IO	GPIO port A input/output 15	11	19	30	30	8	44
PA16	IO	GPIO port A input/output 16	12	20	31	31	9	45
PA17	IO	GPIO port A input/output 17	13	21	32	32	10	54
PA18	IO	GPIO port A input/output 18	14	22	33	33	11	55
PA19	IO	GPIO port A input/output 19	15	23	34	34	12	56
PA20	IO	GPIO port A input/output 20	16	24	35	35	13	57
PA21	IO	GPIO port A input/output 21	17	25	39	39	17	61
PA22	IO	GPIO port A input/output 22	18	26	40	40	18	62
PA23	IO	GPIO port A input/output 23	19	27	43	43	24	72
PA24	IO	GPIO port A input/output 24	20	28	44	44	25	73
PA25	IO	GPIO port A input/output 25	21	29	45	45	26	74
PA26	IO	GPIO port A input/output 26	22	30	46	46	30	78
PA27	IO	GPIO port A input/output 27		31	47	47	31	79
PA28	IO	GPIO port A input/output 28			3	3	35	3
PA29	IO	GPIO port A input/output 29					36	4
PA30	IO	GPIO port A input/output 30					37	5
PB0	IO	GPIO port B input/output 0					47	15
PB1	IO	GPIO port B input/output 1					48	16
PB2	IO	GPIO port B input/output 2			14	14	50	18
PB3	IO	GPIO port B input/output 3			15	15	51	19
PB4	IO	GPIO port B input/output 4					52	20
PB5	IO	GPIO port B input/output 5					53	21
PB6	IO	GPIO port B input/output 6			20	20	58	30
PB7	IO	GPIO port B input/output 7			21	21	59	31

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Table 6-7. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
PB8	IO	GPIO port B input/output 8			22	22	60	32
PB9	IO	GPIO port B input/output 9			23	23	61	33
PB10	IO	GPIO port B input/output 10					62	34
PB11	IO	GPIO port B input/output 11					63	35
PB12	IO	GPIO port B input/output 12					64	36
PB13	IO	GPIO port B input/output 13					1	37
PB14	IO	GPIO port B input/output 14			24	24	2	38
PB15	IO	GPIO port B input/output 15			25	25	3	39
PB16	IO	GPIO port B input/output 16			26	26	4	40
PB17	IO	GPIO port B input/output 17			36	36	14	58
PB18	IO	GPIO port B input/output 18			37	37	15	59
PB19	IO	GPIO port B input/output 19			38	38	16	60
PB20	IO	GPIO port B input/output 20			41	41	19	67
PB21	IO	GPIO port B input/output 21					20	68
PB22	IO	GPIO port B input/output 22					21	69
PB23	IO	GPIO port B input/output 23					22	70
PB24	IO	GPIO port B input/output 24			42	42	23	71
PB25	IO	GPIO port B input/output 25					27	75
PB26	IO	GPIO port B input/output 26					28	76
PB27	IO	GPIO port B input/output 27					29	77
PB28	IO	GPIO port B input/output 28						24
PB29	IO	GPIO port B input/output 29						25
PB30	IO	GPIO port B input/output 30						26
PB31	IO	GPIO port B input/output 31						27
PC0	IO	GPIO port C input/output 0						46
PC1	IO	GPIO port C input/output 1						47
PC2	IO	GPIO port C input/output 2						50
PC3	IO	GPIO port C input/output 3						51
PC4	IO	GPIO port C input/output 4						52
PC5	IO	GPIO port C input/output 5						53
PC6	IO	GPIO port C input/output 6						63
PC7	IO	GPIO port C input/output 7						64
PC8	IO	GPIO port C input/output 8						65
PC9	IO	GPIO port C input/output 9						66

Table 6-8. I2C Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
I2C0_SCL	IOD	I2C0 serial clock signal (SCL)	1, 10, 18, 8	13, 15, 2, 26	17, 19, 2, 36, 40	17, 19, 2, 36, 40	14, 18, 34, 47, 55, 57	15, 2, 23, 29, 58, 62
I2C0_SDA	IOD	I2C0 serial data signal (SDA)	24, 9	1, 12, 14	1, 16, 18, 3, 37, 41	1, 16, 18, 3, 37, 41	15, 19, 33, 35, 48, 54, 56	1, 16, 22, 28, 3, 59, 67

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Table 6-8. I2C Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
I2C1_SCL	IOD	I2C1 serial clock signal (SCL)	10, 11, 13, 16, 7	10, 15, 19, 21, 24, 8	10, 12, 14, 19, 30, 32, 35	10, 12, 14, 19, 30, 32, 35	10, 13, 36, 44, 50, 57, 8	12, 18, 29, 4, 44, 54, 57
I2C1_SDA	IOD	I2C1 serial data signal (SDA)	12, 14, 15, 6, 9	14, 20, 22, 23, 7, 9	11, 15, 18, 31, 33, 34, 9	11, 15, 18, 31, 33, 34, 9	11, 12, 37, 43, 45, 51, 56, 9	11, 13, 19, 28, 45, 5, 55, 56
I2C2_SCL	IOD	I2C2 serial clock signal (SCL)	11, 19	19, 27	20, 22, 25, 30, 43	20, 22, 25, 30, 43	24, 3, 36, 58, 60, 8	24, 30, 32, 39, 4, 44, 50, 72
I2C2_SDA	IOD	I2C2 serial data signal (SDA)	12, 20	20, 28	21, 23, 26, 31, 44	21, 23, 26, 31, 44	25, 37, 4, 59, 61, 9	25, 31, 33, 40, 45, 5, 51, 73

Table 6-9. IOMUX Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
WAKE	I	Input signal to wake the device from SHUTDOWN mode	1, 10, 13, 14, 2, 24, 9	1, 14, 15, 2, 21, 22, 3	1, 18, 19, 2, 3, 32, 33, 4	1, 18, 19, 2, 3, 32, 33, 4	10, 11, 33, 34, 35, 38, 56, 57	1, 2, 28, 29, 3, 54, 55, 6

Table 6-10. Liquid Crystal Display (LCD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
LCD0	A	LCD segment 0		12	16	16	54	22
LCD1	A	LCD segment 1	8	13	17	17	55	23
LCD2	A	LCD segment 2	9	14	18	18	56	28
LCD3	A	LCD segment 3	10	15	19	19	57	29
LCD4	A	LCD segment 4			20	20	58	30
LCD5	A	LCD segment 5			21	21	59	31
LCD6	A	LCD segment 6			22	22	60	32
LCD7	A	LCD segment 7			23	23	61	33
LCD8	A	LCD segment 8			24	24	2	38
LCD9	A	LCD segment 9			25	25	3	39
LCD10	A	LCD segment 10			26	26	4	40
LCD11	A	LCD segment 11		16	27	27	5	41
LCD12	A	LCD segment 12		17	28	28	6	42
LCD13	A	LCD segment 13		18	29	29	7	43
LCD14	A	LCD segment 14	11	19	30	30	8	44
LCD15	A	LCD segment 15	12	20	31	31	9	45
LCD16	A	LCD segment 16	13	21	32	32	10	54
LCD17	A	LCD segment 17	14	22	33	33	11	55
LCD18	A	LCD segment 18			36	36	14	58
LCD19	A	LCD segment 19			37	37	15	59
LCD20	A	LCD segment 20			38	38	16	60
LCD21	A	LCD segment 21	17	25	39	39	17	61

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Table 6-10. Liquid Crystal Display (LCD) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
LCD22	A	LCD segment 22	18	26	40	40	18	62
LCD23	A	LCD segment 23			41	41	19	67
LCD24	A	LCD segment 24			42	42	23	71
LCD25	A	LCD segment 25	19	27	43	43	24	72
LCD26	A	LCD segment 26	20	28	44	44	25	73
LCD27	A	LCD segment 27	21	29	45	45	26	74
LCD28	A	LCD segment 28	22	30	46	46	30	78
LCD29	A	LCD segment 29		31	47	47	31	79
LCD30	A	LCD segment 30			3	3	35	3
LCD31	A	LCD segment 31					36	4
LCD32	A	LCD segment 32					37	5
LCD33	A	LCD segment 33					52	20
LCD34	A	LCD segment 34					53	21
LCD35	A	LCD segment 35					62	34
LCD36	A	LCD segment 36					63	35
LCD37	A	LCD segment 37					64	36
LCD38	A	LCD segment 38					1	37
LCD39	A	LCD segment 39					20	68
LCD40	A	LCD segment 40					21	69
LCD41	A	LCD segment 41					22	70
LCD42	A	LCD segment 42					27	75
LCD43	A	LCD segment 43					28	76
LCD44	A	LCD segment 44					29	77
LCD45	A	LCD segment 45						24
LCD46	A	LCD segment 46						25
LCD47	A	LCD segment 47						26
LCD48	A	LCD segment 48						27
LCD49	A	LCD segment 49						46
LCD50	A	LCD segment 50						47
LCD51	A	LCD segment 51						50
LCD52	A	LCD segment 52						51
LCD53	A	LCD segment 53						52
LCD54	A	LCD segment 54						53
LCD55	A	LCD segment 55						63
LCD56	A	LCD segment 56						64
LCD57	A	LCD segment 57						65
LCD58	A	LCD segment 58						66
LCDCAP0	A	LCD capacitor pin 0		17	28	28	6	42
LCDCAP1	A	LCD capacitor pin 1		18	29	29	7	43
LCDEN	A	LCD enable pin	11, 14	19, 22	23, 30, 33	23, 30, 33	11, 61, 8	33, 44, 55
LCDLFCLK	IO	LCD LFCLK signal	13	21	21, 32, 37	21, 32, 37	10, 15, 59	31, 54, 59
LCDSON	IO	LCD SON signal	12	20	22, 31, 36	22, 31, 36	14, 60, 9	32, 45, 58

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Table 6-10. Liquid Crystal Display (LCD) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
R13	A	LCD R13 signal			24	24	2	38
R23	A	LCD R23 signal			26	26	4	40
R24	A	LCD R24 signal			25	25	3	39
R33	A	LCD R33 signal		16	27	27	5	41

Table 6-11. Power Management Unit (PMU) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
VBAT	PWR	VBAT (backup island) supply	3	4	5	5	39	7
VCORE	PWR	VCORE capacitor connection	23	32	48	48	32	80
VDD	PWR	VDD supply	3	4	6	6	40	8
VDD2	PWR	VDD2 supply						49
VSS	PWR	VSS (ground)	4	5	7	7	41	9
VSS2	PWR	VSS (ground)						48

Table 6-12. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
RTC_OUT	O	Real-time clock output signal	8	13, 17, 31	17, 28, 47	17, 28, 47	31, 55, 6	23, 42, 79

Table 6-13. Serial Peripheral Interface (SPI) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
SPI0_PICO	IO	SPI0 peripheral in controller out signal	8	13, 18, 9	11, 14, 17, 29, 36	11, 14, 17, 29, 36	14, 45, 50, 55, 7	13, 18, 23, 43, 58
SPI0_POCI	IO	SPI0 peripheral out controller in signal	7, 9	11, 14, 17, 8	10, 13, 18, 28, 38	10, 13, 18, 28, 38	16, 44, 49, 56, 6	12, 17, 28, 42, 60
SPI0_SCK	IO	SPI0 serial clock	10	10, 15, 16	12, 15, 19, 27, 37	12, 15, 19, 27, 37	15, 46, 5, 51, 57	14, 19, 29, 41, 59
SPI1_PICO	IO	SPI1 peripheral in controller out signal	14	22	22, 25, 33	22, 25, 33	11, 21, 3, 60	26, 32, 39, 55, 69
SPI1_POCI	IO	SPI1 peripheral out controller in signal	12, 15	20, 23	21, 24, 31, 34	21, 24, 31, 34	12, 2, 20, 59, 9	25, 31, 38, 45, 56, 68
SPI1_SCK	IO	SPI1 serial clock	13, 16	21, 24	23, 26, 32, 35	23, 26, 32, 35	10, 13, 22, 4, 61	27, 33, 40, 54, 57, 70
SPI0_CS0	IO	SPI0 chip select 0 signal	14, 5, 7	12, 22, 6, 8	10, 16, 33, 8	10, 16, 33, 8	11, 27, 42, 44, 54	10, 12, 22, 55, 64, 75
SPI0_CS1	IO	SPI0 chip select 1 signal	13, 6	16, 21, 7	20, 27, 32, 42, 9	20, 27, 32, 42, 9	10, 23, 28, 43, 5, 58	11, 30, 41, 54, 63, 71, 76

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Table 6-13. Serial Peripheral Interface (SPI) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
SPI0_CS2	IO	SPI0 chip select 2 signal	18, 20	11, 18, 26, 28	13, 21, 29, 40, 41, 44	13, 21, 29, 40, 41, 44	18, 19, 25, 37, 48, 49, 59, 7	16, 17, 31, 43, 5, 62, 67, 73
SPI0_CS3	IO	SPI0 chip select 3 signal	1, 17, 19, 6	12, 17, 2, 25, 27, 7	16, 2, 24, 28, 39, 42, 43, 9	16, 2, 24, 28, 39, 42, 43, 9	17, 2, 23, 24, 34, 36, 43, 47, 54, 6	11, 15, 2, 22, 38, 4, 42, 61, 71, 72
SPI1_CS0	IO	SPI1 chip select 0 signal	22, 5	17, 30, 6	20, 28, 41, 46, 8	20, 28, 41, 46, 8	1, 19, 30, 42, 58, 6	10, 24, 30, 37, 42, 50, 67, 78
SPI1_CS1	IO	SPI1 chip select 1 signal	17, 19	16, 25, 27, 31	27, 36, 39, 42, 43, 47	27, 36, 39, 42, 43, 47	14, 17, 23, 24, 29, 31, 5, 64	36, 41, 51, 58, 61, 66, 71, 72, 77, 79
SPI1_CS2	IO	SPI1 chip select 2 signal	11, 20	18, 19, 28	29, 30, 37, 44	29, 30, 37, 44	15, 25, 47, 63, 7, 8	15, 35, 43, 44, 47, 52, 59, 65, 73
SPI1_CS3	IO	SPI1 chip select 3 signal	21	29	24, 38, 45	24, 38, 45	16, 2, 26, 48, 62	16, 34, 38, 46, 53, 60, 74

Table 6-14. Serial Wire Debug (SWD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
SWCLK	I	Serial wire debug interface clock input signal	16	24	35	35	13	57
SWDIO	IO	Serial wire debug interface data input/ output signal	15	23	34	34	12	56

Table 6-15. System Controller (SYSCTL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
NRST	I	Active-low reset signal (must be logic high for the device to start)	2	3	4	4	38	6

Table 6-16. Tamper IO (TIO) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
TIO0	I	Passive tamper detection signal 0		11	13	13	49	17
TIO1	I	Passive tamper detection signal 1			14	14	50	18
TIO2	I	Passive tamper detection signal 2			15	15	51	19

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Table 6-17. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
TIMA0_C0	IO	TIMA0 capture/compare 0 signal	17, 24, 5	1, 12, 25, 6	1, 15, 16, 22, 24, 39, 8	1, 15, 16, 22, 24, 39, 8	17, 2, 28, 33, 42, 51, 54, 60	1, 10, 19, 22, 24, 32, 38, 50, 61, 63, 76
TIMA0_C1	IO	TIMA0 capture/compare 1 signal	1, 18, 6, 8	11, 13, 2, 26, 7	13, 17, 2, 23, 3, 40, 41, 9	13, 17, 2, 23, 3, 40, 41, 9	18, 19, 34, 35, 43, 49, 52, 55, 61, 64	11, 17, 2, 20, 23, 26, 3, 33, 36, 52, 62, 65, 67
TIMA0_C2	IO	TIMA0 capture/compare 2 signal	11, 15, 6, 9	11, 14, 19, 23, 7	13, 18, 30, 34, 36, 41, 9	13, 18, 30, 34, 36, 41, 9	12, 14, 19, 43, 47, 49, 52, 56, 64, 8	11, 15, 17, 20, 28, 36, 44, 46, 56, 58, 67
TIMA0_C3	IO	TIMA0 capture/compare 3 signal	13, 19, 21, 7	16, 21, 27, 29, 8	10, 14, 27, 3, 32, 42, 43, 45	10, 14, 27, 3, 32, 42, 43, 45	1, 10, 23, 24, 26, 28, 35, 44, 5, 50	12, 18, 3, 37, 41, 54, 71, 72, 74, 76
TIMA0_C0N	O	TIMA0 capture/compare 0 complementary output	18, 8	13, 26	17, 23, 40	17, 23, 40	18, 29, 55, 61	23, 25, 33, 51, 62, 64, 77
TIMA0_C1N	O	TIMA0 capture/compare 1 complementary output	21, 7	29, 8	10, 42, 45	10, 42, 45	1, 23, 26, 44, 53	12, 21, 27, 37, 53, 66, 71, 74
TIMA0_C2N	O	TIMA0 capture/compare 2 complementary output	10, 12, 16, 5	10, 15, 20, 24, 6	12, 19, 31, 35, 37, 8	12, 19, 31, 35, 37, 8	13, 15, 42, 46, 48, 53, 57, 9	10, 14, 16, 21, 29, 45, 47, 57, 59
TIMA0_C3N	O	TIMA0 capture/compare 3 complementary output	14, 20, 22, 5	17, 22, 28, 30, 6	15, 28, 33, 44, 46, 8	15, 28, 33, 44, 46, 8	11, 25, 29, 30, 42, 51, 6	10, 19, 42, 55, 73, 77, 78
TIMA_FAL0	I	Timer fault input 0	10, 22, 5	10, 12, 15, 30, 6	12, 16, 19, 3, 46, 8	12, 16, 19, 3, 46, 8	22, 27, 30, 35, 42, 46, 54, 57	10, 14, 22, 24, 29, 3, 50, 70, 75, 78
TIMA_FAL1	I	Timer fault input 1	24, 5, 9	1, 14, 6, 9	1, 11, 18, 41, 8	1, 11, 18, 41, 8	19, 27, 33, 42, 45, 56, 64	1, 10, 13, 25, 28, 36, 51, 67, 75
TIMA_FAL2	I	Timer fault input 2	1	12, 2, 31	16, 2, 20, 47	16, 2, 20, 47	27, 31, 34, 54, 58	2, 22, 26, 30, 52, 75, 79
TIMG8_IDX	I	TIMG8 quadrature encoder index pulse signal	1, 11	11, 19, 2	13, 2, 24, 30, 38	13, 2, 24, 30, 38	16, 2, 34, 49, 8	17, 2, 27, 38, 44, 53, 60

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Table 6-17. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
TIMG0_C0	IO	TIMG0 capture/compare 0 signal	15, 19, 24, 9	1, 14, 16, 23, 27, 9	1, 11, 18, 27, 34, 36, 43	1, 11, 18, 27, 34, 36, 43	12, 14, 24, 33, 45, 47, 5, 52, 56, 62	1, 13, 15, 20, 24, 28, 34, 41, 50, 56, 58, 72
TIMG0_C1	IO	TIMG0 capture/compare 1 signal	1, 10, 16, 20	10, 15, 17, 2, 24, 28	12, 19, 2, 28, 35, 37, 44	12, 19, 2, 28, 35, 37, 44	13, 15, 25, 34, 46, 48, 53, 57, 6, 63	14, 16, 2, 21, 25, 29, 35, 42, 51, 57, 59, 73
TIMG12_C0	IO	TIMG12 capture/compare 0 signal	11, 13, 24, 9	1, 14, 18, 19, 21	1, 14, 18, 20, 29, 30, 32, 41	1, 14, 18, 20, 29, 30, 32, 41	1, 10, 19, 33, 50, 56, 58, 7, 8	1, 18, 28, 30, 37, 43, 44, 54, 67
TIMG12_C1	IO	TIMG12 capture/compare 1 signal	1, 10, 12, 14, 21	15, 18, 2, 20, 22, 29	15, 19, 2, 21, 24, 29, 31, 33, 42, 45	15, 19, 2, 21, 24, 29, 31, 33, 42, 45	11, 2, 23, 26, 34, 51, 57, 59, 7, 9	19, 2, 29, 31, 38, 43, 45, 55, 71, 74
TIMG4_C0	IO	TIMG4 capture/compare 0 signal	17, 21	25, 29, 9	11, 14, 20, 22, 36, 39, 45	11, 14, 20, 22, 36, 39, 45	14, 17, 26, 28, 36, 45, 50, 52, 58, 60, 62	13, 18, 20, 26, 30, 32, 34, 4, 52, 58, 61, 74, 76
TIMG4_C1	IO	TIMG4 capture/compare 1 signal	18, 22	10, 26, 30	12, 15, 21, 23, 37, 40, 46	12, 15, 21, 23, 37, 40, 46	15, 18, 29, 30, 37, 46, 51, 53, 59, 61, 63	14, 19, 21, 27, 31, 33, 35, 5, 53, 59, 62, 77, 78
TIMG5_C0	IO	TIMG5 capture/compare 0 signal	13, 19, 22, 6, 8	13, 21, 27, 30, 7	17, 25, 3, 32, 43, 46, 9	17, 25, 3, 32, 43, 46, 9	10, 24, 3, 30, 35, 43, 55	11, 23, 3, 39, 54, 65, 72, 78
TIMG5_C1	IO	TIMG5 capture/compare 1 signal	14, 20, 5, 7	11, 12, 22, 28, 31, 6, 8	10, 13, 16, 26, 33, 38, 44, 47, 8	10, 13, 16, 26, 33, 38, 44, 47, 8	11, 16, 25, 31, 4, 42, 44, 49, 54	10, 12, 17, 22, 40, 55, 60, 66, 73, 79
TIMG8_C0	IO	TIMG8 capture/compare 0 signal	1, 13, 17, 19, 22, 6	11, 2, 21, 25, 27, 30, 7, 9	11, 13, 2, 20, 25, 32, 39, 43, 46, 9	11, 13, 2, 20, 25, 32, 39, 43, 46, 9	10, 17, 20, 24, 3, 30, 34, 36, 43, 45, 49, 58, 62	11, 13, 17, 2, 30, 34, 39, 4, 46, 54, 61, 63, 68, 72, 78

Table 6-17. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
TIMG8_C1	IO	TIMG8 capture/compare 1 signal	14, 18, 20, 24, 5, 7	1, 10, 22, 26, 28, 31, 6, 8	1, 10, 12, 21, 26, 33, 38, 40, 44, 47, 8	1, 10, 12, 21, 26, 33, 38, 40, 44, 47, 8	11, 16, 18, 21, 25, 31, 33, 37, 4, 42, 44, 46, 59, 63	1, 10, 12, 14, 31, 35, 40, 47, 5, 55, 60, 62, 64, 69, 73, 79

Table 6-18. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
UART0_CTS	I	UART0 clear to send signal	8	13, 18, 9	11, 17, 29, 38	11, 17, 29, 38	16, 27, 36, 45, 55, 7	13, 23, 4, 43, 60, 75
UART0_RTS	O	UART0 ready to send signal	11	10, 12, 19	12, 16, 30	12, 16, 30	28, 37, 46, 54, 8	14, 22, 44, 5, 76
UART0_RX	I	UART0 receive signal (RXD)	1, 10	15, 2	19, 2	19, 2	34, 48, 57	16, 2, 29
UART0_TX	O	UART0 transmit signal (TXD)	24, 9	1, 14	1, 18, 3	1, 18, 3	33, 35, 47, 56	1, 15, 28, 3
UART1_CTS	I	UART1 clear to send signal	17	16, 25	14, 22, 27, 39	14, 22, 27, 39	17, 22, 5, 50, 60	18, 26, 32, 41, 61, 70
UART1_RTS	O	UART1 ready to send signal	18	17, 26	15, 23, 28, 40	15, 23, 28, 40	18, 51, 6, 61	19, 27, 33, 42, 62
UART1_RX	I	UART1 receive signal (RXD)	14, 7, 8	10, 13, 22, 8	10, 12, 17, 21, 33	10, 12, 17, 21, 33	11, 21, 44, 46, 53, 55, 59	12, 14, 21, 23, 31, 47, 55, 69
UART1_TX	O	UART1 transmit signal (TXD)	13, 6	12, 21, 7, 9	11, 16, 20, 32, 9	11, 16, 20, 32, 9	10, 20, 43, 45, 52, 54, 58	11, 13, 20, 22, 30, 46, 54, 68
UART2_CTS	I	UART2 clear to send signal	12, 17, 21, 6	16, 20, 25, 29, 7	14, 20, 27, 31, 38, 39, 45, 9	14, 20, 27, 31, 38, 39, 45, 9	16, 17, 26, 37, 43, 5, 50, 58, 9	11, 18, 30, 41, 45, 5, 60, 61, 74
UART2_RTS	O	UART2 ready to send signal	11, 22, 7	19, 30, 8	10, 15, 21, 30, 41, 42, 46	10, 15, 21, 30, 41, 42, 46	19, 23, 30, 36, 44, 51, 59, 8	12, 19, 31, 4, 44, 67, 71, 78
UART2_RX	I	UART2 receive signal (RXD)	18, 20	18, 26, 28	15, 26, 29, 37, 40, 44	15, 26, 29, 37, 40, 44	15, 18, 25, 4, 51, 7	19, 40, 43, 59, 62, 73
UART2_TX	O	UART2 transmit signal (TXD)	17, 19	17, 25, 27	14, 25, 28, 36, 39, 43	14, 25, 28, 36, 39, 43	14, 17, 24, 3, 50, 6	18, 39, 42, 58, 61, 72
UART3_CTS	I	UART3 clear to send signal	19	16, 27	25, 27, 43	25, 27, 43	24, 3, 5, 52	20, 39, 41, 52, 65, 72
UART3_RTS	O	UART3 ready to send signal	20	17, 28	26, 28, 44	26, 28, 44	25, 4, 53, 6	21, 40, 42, 53, 66, 73

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Table 6-18. Universal Asynchronous Receiver Transmitter (UART) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
UART3_RX	I	UART3 receive signal (RXD)	21, 22	17, 29, 30, 31	15, 28, 45, 46, 47	15, 28, 45, 46, 47	1, 26, 30, 31, 51, 6	19, 37, 42, 64, 74, 78, 79
UART3_TX	O	UART3 transmit signal (TXD)	21, 22	18, 29, 30	14, 29, 45, 46	14, 29, 45, 46	26, 30, 50, 64, 7	18, 36, 43, 63, 74, 78
UART4_CTS	I	UART4 clear to send signal	5	6	38, 8	38, 8	16, 42, 64	10, 36, 60
UART4_RTS	O	UART4 ready to send signal	17, 8	13, 25, 9	11, 17, 39	11, 17, 39	1, 17, 45, 55	13, 23, 37, 61
UART4_RX	I	UART4 receive signal (RXD)			37	37	15, 21, 63	35, 59, 69
UART4_TX	O	UART4 transmit signal (TXD)			36	36	14, 20, 62	34, 58, 68

Table 6-19. Voltage Reference Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	RGE PIN	RHB PIN	RGZ PIN	PT PIN	PM PIN	PN PIN
VREF+	A	Voltage reference positive input	19	27	43	43	24	72
VREF-	A	Voltage reference negative input	17	25	39	39	17	61

6.4 Connections for Unused Pins

Table 6-20 lists the correct termination of unused pins.

Table 6-20. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx , PBx, and PCx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup/ pulldown resistor.
NRST	VCC	NRST is an active-low reset signal; it must be pulled high to VCC or the device will not start, for more information refer to Section 9.1

(1) Any unused pin with a function that is shared with general-purpose I/O should follow the "PAx, PBx, and PCx" unused pin connection guidelines.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
VBAT	Battery Backup Supply	At VBAT pin, with respect to VSS	–0.3	4.1	V
V_I	Input voltage	Applied to any 5-V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current of VDD pin	Current into VDD pin (source), VDD >= 2.7V		80	mA
I_{VBAT}	Current of VBAT pin	Current into VBAT pin (source), VBAT >= 2.7V		20	mA
I_{VSS}	Current of VSS pin	Current out of VSS pin (sink), VDD, VBAT>=2.7V		80	mA
I_{IO}	Current of SD IO pin	Current sunk or sourced by SD IO pin, VDD>=2.7V		6	mA
I_{IO}	Current of HS IO pin	Current sunk or sourced by HS IO pin, VDD >=2.7V		6	mA
I_{IO}	Current of HD IO pin	Current sunk or sourced by HD IO pin		20	mA
I_{IO}	Current of OD IO pin	Current sunk by OD IO pin		20	mA
I_D	Supported diode current	Diode current on pin supporting LCD function	-2	0.4	mA
I_D	Supported diode current	Diode current on pin not supporting LCD function (excluding Open Drain IO)	-2	0.05	mA
T_J		Junction temperature	-40	130	°C
T_{stg}		Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD (4)	Supply voltage	1.62(5)		3.6	V
VBAT	At VBAT pin, with respect to VSS	1.62(5)		3.6	V
VCORE	Voltage on VCORE pin (2)		1.35		V
C_{VDD}	Capacitor connected betwen VDD and VSS (1)		10		uF
C_{VBAT}	Capacitor connected between VBAT and VSS		1		µF
C_{VCORE}	Capacitor connected between VCORE and VSS (1) (2)		470		nF
T_A	Ambient temperature	–40		125	°C
T_J	Max junction temperature			130	°C

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7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state (3)			32	MHz
	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states (3)			24	

(1) Connect C_{VDD} ,C_{VBAT} and C_{VCORE} between VDD/VSS , VBAT/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} ,C_{VBAT} and C_{VCORE}.
(2) The VCORE pin must only be connected to C_{VCORE}. Do not supply any voltage or apply any external load to the VCORE pin.
(3) Wait states are managed automatically by the system controller (SYSCTL), and do not need to be configured by application software unless MCLK is sourced from a high speed clock source (HSCLK sourced from HFCLK)
(4) There is no dependency on MCLK frequency with respect to VDD recommended operating range.
(5) Functionality is guaranteed down to $V_{BOR0-(min)}$.

7.4 Thermal Information

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-80 (PN)	59.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		19.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		39.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-64 (PM)	63.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		40.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		39.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ)	29.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		20.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		11.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		3.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT)	72.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		44.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		44.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	33.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		13.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		13.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		3.5	°C/W

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7.4 Thermal Information (continued)

THERMAL METRIC[1]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-24 (RGE)	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		32.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		18.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		18.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	3.3		3.4		3.4		3.5		3.5		mA
		4MHz	0.6		0.7		0.7		0.8		0.8		
	MCLK=SYSOSC, CoreMark, execute from SRAM	32MHz	2.9		3.0		3.0		3.1		3.1		
		4MHz	0.6		0.6		0.7		0.7		0.7		
IDD_{RUN}, per MHz	MCLK=SYSOSC, While(1), execute from flash	32MHz	57	62	57	65	58	68	60	70	61	75	uA/Mhz
	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	103		106		106		109		109		
	MCLK=SYSOSC, CoreMark, execute from flash	4MHz	150		175		175		200		200		
SLEEP Mode													
IDD_{SLEEP}	MCLK=LFCLK, CPU is halted	32KHz	252	310	259	320	284	370	317	585	370	800	uA
IDD_{SLEEP}	MCLK=SYSOSC, CPU is halted	32MHz	1240	1312	1255	1328	1275	1405	1305	1552	1350	1699	uA
		4MHz	408	461	416	474	438	589	477	737	517	885	

7.5.2 STOP/STANDBY Modes

VDD=3.3V, VBAT=3.3V. All inputs in VDD Island tied to 0V or VDD, All inputs in VBAT Island tied to 0V or VBAT. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0	4MHz	342	359	347	362	352	367	361	380	369	392	uA
IDD_{STOP1}	SYSOSC=4MHz, USE4MHZSTOP=1, DISABLESTOP=0		180	192	186	197	191	203	200	217	209	230	
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	51	55	54	58	58	64	66	79	74	93	
STANDBY Mode													
VDD Island IDD_{STBY0}	STOPCLKSTBY=0, TIMG0 enabled	32kHz	1.5	2.2	1.6	2.3	4.0	7	12	22	20	36	uA
VDD Island IDD_{STBY1}	STOPCLKSTBY=1, TIMG0 enabled		1	2	1.2	2	3.5	6.5	11	21	19	35	
VDD Island IDD_{STBY1}	STOPCLKSTBY=1, GPIOA enabled		1	2	1.2	2	3.5	6.5	11	21	19	35	
VBAT Island IDD_{STBY1}	LF-XT and RTC is running	32kHz	1.1	1.6	1.1	1.7	1.2	1.8	1.8	2.7	2.0	3.6	uA
VBAT Island IDD_{STBY1}	LFOSC and IWDG is running		1.1	1.6	1.1	1.7	1.2	1.8	1.8	2.7	2.0	3.6	
IDD_{STBY0}	Idd_Q ($_{VBAT}$) + Idd_Q (SoC)		2.6	3.8	2.7	4	5.2	9	14	25	22	40	

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7.5.3 SHUTDOWN Mode

VDD=3.3V, VBAT=3.3V. All inputs in VDD Island tied to 0V or VDD, All inputs in VBAT Island tied to 0V or VBAT. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
VDD Island IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	40		80		700		2600		4500		nA
VBAT Island IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	1.1	1.6	1.1	1.7	1.2	1.8	1.8	2.7	2.0	3.6	uA

7.6 Power Supply Sequencing

7.6.1 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

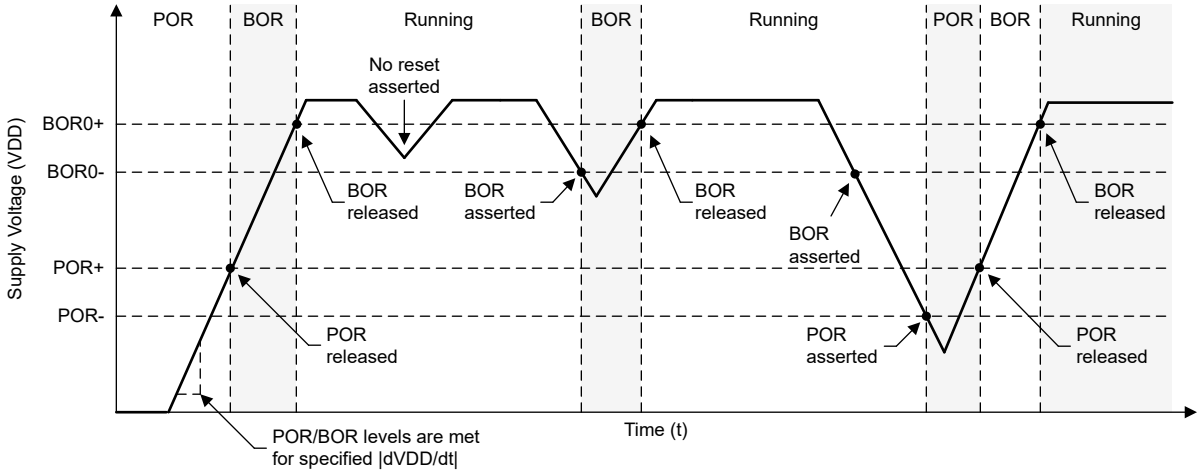


Figure 7-1. Power Cycle POR/BOR Conditions - VDD

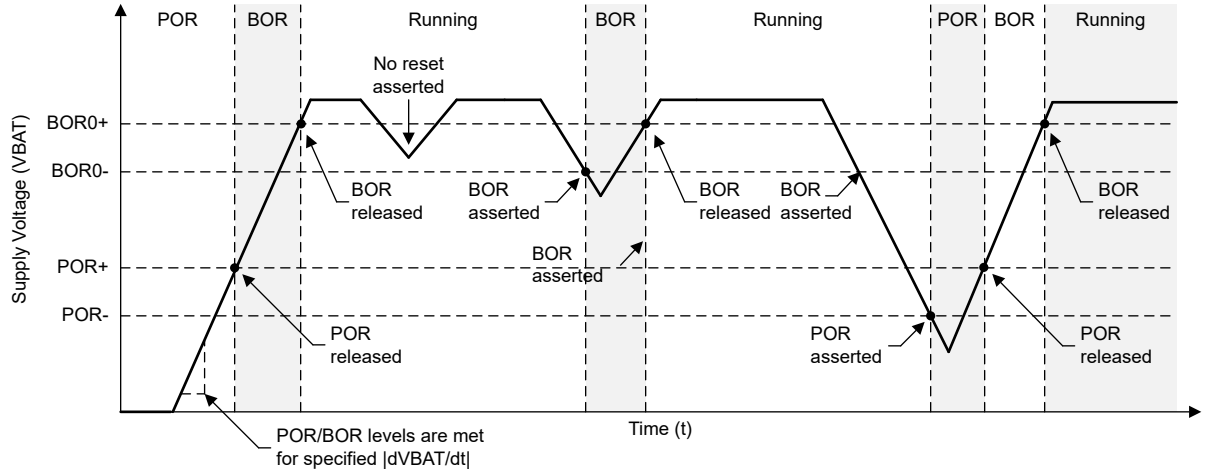


Figure 7-2. Power Cycle POR/BOR Conditions - VBAT

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7.6.2 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Power supply range		1.62		3.6	V
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling (2)			0.01	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising (1)	0.95	1.30	1.56	V
V_{POR-}	Power-on reset voltage level	Falling (1)	0.9	1.25	1.53	V
$V_{HYS, POR}$	POR hysteresis		25	45	70	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	-40℃ ≤ Tj ≤ 30℃ Cold start, rising (1)	1.45	1.54	1.62	V
$V_{BOR0+, COLD}$		30℃ ≤ Tj ≤ 85℃ Cold start, rising (1)	1.48	1.56	1.64	V
$V_{BOR0+, COLD}$		85℃ ≤ Tj ≤ 130℃ Cold start, rising (1)	1.48	1.57	1.66	V
V_{BOR0+}	Brown-out reset voltage level 0 (default level)	Rising (1) (2)	1.56	1.59	1.62	V
V_{BOR0-}	Brown-out reset voltage level 0 (default level)	Falling (1) (2)	1.55	1.58	1.61	V
$V_{BOR0, STBY}$	Brown-out reset voltage level 0 (default level)	STANDBY mode (1)	1.51	1.56	1.61	V
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1) (2)	2.13	2.17	2.21	V
V_{BOR1-}	Brown-out-reset voltage level 1	Falling (1) (2)	2.10	2.14	2.18	V
$V_{BOR1, STBY}$	Brown-out-reset voltage level 1	STANDBY mode (1)	2.06	2.13	2.20	V
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1) (2)	2.73	2.77	2.82	V
V_{BOR2-}	Brown-out-reset voltage level 2	Falling (1) (2)	2.7	2.74	2.79	V
$V_{BOR2, STBY}$	Brown-out-reset voltage level 2	STANDBY mode (1)	2.62	2.71	2.8	V
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1) (2)	2.88	2.96	3.04	V
V_{BOR3-}	Brown-out-reset voltage level 3	Falling (1) (2)	2.85	2.93	3.01	V
$V_{BOR3, STBY}$	Brown-out-reset voltage level 3	STANDBY mode (1)	2.82	2.92	3.02	V
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (1)		15	21	mV
$V_{HYS,BOR}$	Brown-out reset hysteresis	Levels 1-3 (1)		34	40	mV
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
$T_{PD, BOR}$	BOR propagation delay	STANDBY mode			100	us

(1) |dVDD/dt| ≤ 3V/s
(2) Device operating in RUN, SLEEP, or STOP mode.

7.7 VBat Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBAT	Power supply range		1.62		3.6	V
dVBAT/dt	VBAT (supply voltage) slew rate	Rising			0.1	V/us
dVBAT/dt	VBAT (supply voltage) slew rate	Falling,standby			0.1	V/ms
$V_{POR+ (VBAT)}$	Power-on reset voltage level	Rising (1)	0.95	1.3	1.55	V
$V_{POR- (VBAT)}$	Power-on reset voltage level	Falling (1)	0.9	1.25	1.52	V
$V_{HYS, POR(VBAT)}$	POR hysteresis		25	45	70	mV

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7.7 VBat Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR0+, COLD(VBAT)}$	Brown-out reset voltage level	Cold start, rising (1)	1.48	1.54	1.62	V
$V_{BOR0+ (VBAT)}$	Brown-out reset voltage level	Rising (1)	1.56	1.58	1.62	V
$V_{BOR0- (VBAT)}$	Brown-out reset voltage level	Falling (1)	1.51	1.56	1.61	V
$T_{PU(VBAT)}$	Cold power up time			1.2		ms
Icharge	Charging peak current	VDD=3.3, VBAT=0V		1.7		mA
Rswitch	Internal switch resistance between VBAT and VDD		0.9	1.4	2.7	kΩ
I(trip)	Min current for internal comparator to detect reverse current from VBAT to VDD	VDD sinking , 1.6<VBAT<3.3	100			µA
$VBAT_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (1)		15	21	mV

(1) |dVBAT/dt| ≤ 3V/s

7.8 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
NWEC(HI_ENDURANCE)	Erase/program cycle endurance for any 32 sectors of flash (1)		100			k cycles per sector
NWEC (NORMAL_ENDURANCE)	Erase/program cycle endurance (Flash not used for HI_ENDURANCE) (1)		10			k cycles per sector
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C <= Tj <= 105°C	11.4			years
Program and Erase Timing						
$t_{PROG (WORD, 64)}$	Program time for flash word (4) (6)			50	275	µs
$t_{PROG (SEC, 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE (SEC)}$	Sector erase time	<10k erase/program cycles		20	200	ms
$t_{ERASE (BANK)}$	Bank erase time	<10k erase/program cycles		22	220	ms

(1) Up to 32 application-chosen sectors from the main flash bank(s) or data bank can be used as high endurance sectors. This enables applications that frequently update flash data such as EEPROM emulation.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.

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(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.9 Timing Characteristics

VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE, SLEEP}$	Wakeup time from SLEEP0 to RUN (1)			1.5		us
	Wakeup time from SLEEP1 to RUN (1)			2.1		
	Wakeup time from SLEEP2 to RUN (1)			2.5		
$t_{WAKE, STOP}$	Wakeup time from STOP0 to RUN (SYSOSC enabled) (1)			12.5		us
	Wakeup time from STOP1 to RUN (SYSOSC enabled) (1)			14.6		
	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)			13.5		
$t_{WAKE, STBY}$	Wakeup time from STANDBY0 to RUN (1)			15.7		us
	Wakeup time from STANDBY1 to RUN (1)			15.7		
$t_{WAKEUP, SHDN}$	Wakeup time from SHUTDOWN to RUN (2)	Fast boot enabled		300		us
		Fast boot disabled		322		us
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2		0.9		us
		Mode is STOP1		2.4		
		Mode is STOP2		0.9		
		Mode is STANDBY1		3.2		
Startup Timing						
$t_{START, RESET}$	Device cold startup time from reset/ power-up (3)	Fast boot enabled		304		us
		Fast boot disabled		370		
NRST Timing						
$t_{RST, BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		1.5		us
		ULPCLK=32kHz		80		
$t_{RST, POR}$	Pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external wake-up signal (GPIO wake-up event) to the time that the first instruction of the user program is executed, with glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1) .
(2) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.
(3) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

7.10 Clock Specifications

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7.10.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
f_{SYSOSC}		SYSOSCCFG.FREQ=01		4		
f_{SYSOSC}	User trimmed SYSOSC frequency	SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=10		24		
f_{SYSOSC}		SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=01		16		
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled and an ideal ROSC resistor is assumed (1) (2)	SETUSEFCL=1, T_a = 25 ℃	-0.41		0.58	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃	-0.8		0.93	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃	-0.8		1.1	
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-0.8		1.3	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is enabled with ROSC resistor put at ROSC pin, for factory trimmed frequencies (1)	SETUSEFCL=1, ±0.1% 25ppm R_{OSC}, T_a = 25 ℃	-0.5		0.7	%
		SETUSEFCL=1, ±0.1% 25ppm R_{OSC}, -40 ℃ ≤ T_a ≤ 85 ℃	-1.1		1.2	
		SETUSEFCL=1, ±0.1% 25ppm R_{OSC}, -40 ℃ ≤ T_a ≤ 105 ℃	-1.1		1.4	
		SETUSEFCL=1, ±0.1% 25ppm R_{OSC}, -40 ℃ ≤ T_a ≤ 125 ℃	-1.5		1.4	
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used (4)	SETUSEFCL=1 -40 ℃ ≤ Ta ≤ 125 ℃	-2		1.4	%
f_{SYSOSC}	SYSOSC raw accuracy with FCL disabled, 32MHz	SETUSEFCL=0,SYSOSCCFG.FREQ=00 -40 ℃ ≤ T_a ≤ 125 ℃	-2.6		1.8	%
f_{SYSOSC}	SYSOSC raw accuracy with FCL disabled, 4MHz	SETUSEFCL=0,SYSOSCCFG.FREQ=01 -40 ℃ ≤ T_a ≤ 125 ℃	-2.7		2.3	%
R_{OSC}	External resistor between ROSC pin and VSS (1)	SETUSEFCL=1		100		kΩ
$t_{settle, SYSOSC}$	Settling time to target accuracy (3)	SETUSEFCL=1, ±0.1% 25ppm R_{OSC} (1)			30	us
$f_{settle, SYSOSC}$	f_{SYSOSC} accuracy during t_{settle} (3)	SETUSEFCL=1 (1), ±0.1% 25ppm R_{OSC}	-11			%

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an external reference resistor (ROSC) which must be connected between the device ROSC pin and VSS when using the FCL. Accuracies are shown for a ±0.1% ±25ppm ROSC; relaxed tolerance resistors may also be used (with reduced SYSOSC accuracy). See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy for various ROSC accuracies. ROSC does not need to be populated if the FCL is not enabled.

(2) Represents the device accuracy only. The tolerance and temperature drift of the ROSC resistor used must be combined with this spec to determine final accuracy. Performance for a ±0.1% ±25ppm ROSC is given as a reference point.

(3) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency fSYSOSC by an additional error of up to fsettle,SYSOSC for the time tsettle,SYSOSC, after which the target accuracy is achieved.

(4) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.

7.10.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 125 ℃	–5		5	%
		-40 ℃ ≤ T_a ≤ 85 ℃	–3		3	%

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7.10.2 Low Frequency Oscillator (LFOSC) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1.7		ms

7.10.3 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, LFXT}$	LFXT start-up time			483	640	ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=0, LOWCAP=1		200		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency (2)	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle (2)	SETUSEEXLF=1	40		60	%
LFCLK Monitor						
$f_{FAULTLF}$	LFCLK monitor fault frequency (3)	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(3) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.10.4 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
		HFXTRSEL=01	8.01		16	
		HFXTRSEL=10	16.01		32	
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
		HFXTRSEL=01	40		60	
		HFXTRSEL=10	40		60	
		HFXTRSEL=11	40		60	
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, HFXT}$	HFXT start-up time (2)	HFXTRSEL=11, 32MHz crystal		0.5		ms
I_{HFXT}	HFXT current consumption	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		100		uA
		f_{HFXT}=32MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency (3)	USEEXTHFCLK=1	4		32	MHz

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7.10.4 High Frequency Crystal/Clock (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{HFXIN} \times C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT})$, where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual.
(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.11 *Digital IO*

7.11.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). All specifications for SDIO in VDD Power Domain are also applicable to LFSSIO in the VBAT Power Domain.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO (1)	VDD≥1.62V	0.7*VDD		5.5	V
			VDD≥2.7V	2		5.5	V
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	V
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
			VDD≥2.7V	-0.3		0.8	V
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			V
I_{lkg}	High-Z leakage current	non-LCD pins SDIO(2) (3)				50	nA
I_{lkg}	High-Z leakage current	All LCD pins except PA12 SDIO(2) (3)				100	nA
I_{lkg}	High-Z leakage current	PA12 LCD pin SDIO(2) (3)				300	nA
R_{PU}	Pull up resistance	All I/O except ODIO			40		kΩ
R_{PD}	Pull down resistance				40		kΩ
C_I	Input capacitance				5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA T_j≤85 °C	VDD-0.4			V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA T_j>85 °C	VDD-0.45			V
		HDIO	VDD≥2.7V, DRV=1, |IIO|,max=20mAVDD≥1.71V, DRV=1, |IIO|,max=10mA	VDD-0.4			V
			VDD≥2.7V, DRV=0, |IIO|,max=6mAVDD≥1.71V, DRV=0, |IIO|,max=2mA	VDD-0.45			V

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7.11.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). All specifications for SDIO in VDD Power Domain are also applicable to LFSSIO in the VBAT Power Domain.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA T_j≤85 °C			0.4	V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA T_j>85 °C			0.45	
		HDIO	VDD≥2.7V, DRV=1, | IIO|,max=20mAVDD≥1.71V, DRV=1, |IIO|,max=10mA VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=6mAVDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA T_j≤85 °C			0.4	
			VDD≥2.7V, DRV=1, | IIO|,max=20mAVDD≥1.71V, DRV=1, |IIO|,max=10mA VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=6mAVDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA T_j>85 °C			0.45	
		ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA T_j≤85 °C			0.4	
			VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA T_j>85 °C			0.45	

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HDIO = High-Drive
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

7.11.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).All specifications for SDIO in VDD Power Domain are also applicable to LFSSIO in the VBAT Power Domain.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO (1)	VDD ≥ 1.71V, C_L= 20pF			16	MHz
f_{max}	Port output frequency	SDIO (1)	VDD ≥ 2.7V, CL= 20pF			32	
f_{max}	Port output frequency	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF - 100pF			1	
t_r,t_f	Output rise/fall time	All output ports except ODIO	VDD ≥ 1.71V			0.3*f_{max}	s
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF-100pF	20*VDD/5.5		120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed , HDIO = High-Drive

7.12 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz		10.6		uA
$t_{START,VBST}$	VBOOST startup time			12	20	us

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7.13 *ADC*

7.13.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from external reference pin (VREF+)	1.4		VDD	V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), External Reference			1.68	Msps
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), Internal Reference			200	ksps
$I_{(ADC)}$ (2)	Operating supply current into VDD terminal	F_S = 1.68MSPS, Internal reference OFF, V_{R+} = VDD		570		µA
		F_S = 200ksps, Internal reference ON, V_{R+} = VREF = 2.5V		320	435	
Rin	ADC input resistance			0.5		kΩ
$C_{S/H}$	ADC sample-and-hold capacitance			4.3		pF
ENOB	Effective number of bits	Fin = 10kHz, External reference (3)	11.0	11.1		bit
		Fin = 10kHz, Internal reference, V_{R+} = VREF = 2.5V	10	10.2		
SNR	Signal-to-noise ratio	Fin = 10kHz, External reference (3)	68	71		dB
		Fin = 10kHz, Internal reference, V_{R+} = VREF = 2.5V	63	65		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference (3), VDD = $VDD_{(min)}$ to $VDD_{(max)}$	63	68		dB
		VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 2.5V	50	68		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference (3), ΔVDD = 0.1 V at 1 kHz		61		dB
		ΔVDD = 0.1 V at 1 kHz Internal reference, V_{R+} = VREF = 2.5V		55		
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor (4)	-1.5		+1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA
$V_{VBATmon}$	VBAT Monitor voltage divider (VBAT/3) accuracy	ADC input channel: VBAT Monitor (4)	-1.5		+1.5	%
$I_{VBATmon}$	VBAT Monitor voltage divider current consumption	ADC input channel: VBAT Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to $V_{R–}$ for valid conversion results.
(2) The internal reference (VREF) supply current is not included in current consumption parameter $I_{(ADC)}$.
(3) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin
(4) Analog power supply monitor. Analog input on channel 31 for VDD monitor and channel 30 for VBAT monitor is disconnected and is internally connected to the voltage divider which is VDD/3. Both the supply monitors are measured with external reference

7.13.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency		4		32	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample}	Sampling time	12-bit mode, R_S = 50Ω, C_{pext} = 10pF	156			ns
t_{Sample_VREF}	Sample time with VREF	ADC Channel = 28, 12-bit mode, VDD as reference	4			µs
$t_{Sample_SupplyMon(VDD)}$	Sample time with Supply Monitor (VDD/3) (1)		5			µs

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7.13.2 Switching Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Sample_SupplyMon(VBAT)}$	Sample time with Supply Monitor (VBAT/3)(1)		5			µs

(1) Analog power supply monitor. Analog input on channel 31 for VDD monitor and channel 30 for VBAT monitor is disconnected and is internally connected to the voltage divider which is VDD/3.

7.13.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Ej	Integral linearity error (INL)	External reference (2)	External reference (2)	-2.0		+2.0	LSB
Ek	Differential linearity error (DNL) Guaranteed no missing codes	External reference (2)	External reference (2)	-1.0		+1.0	LSB
E_O	Offset error	External reference (2)		-3.5		3.5	mV
E_G	Gain error	External reference (2)		-4		4	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate

(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD and V_{R-} = VSS = 0V, external 1uF cap on VREF+ Pin and HW Averaging feature will only be supported since PG2.0.

7.13.4 Typical Connection Diagram

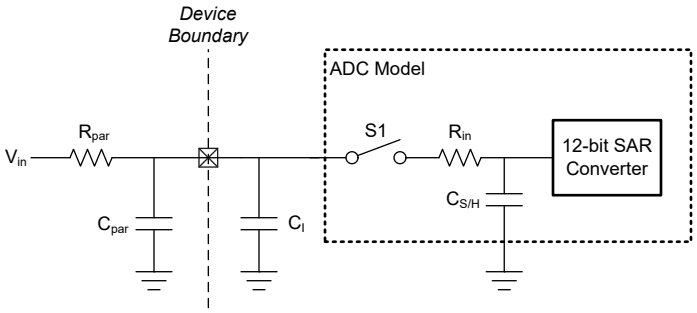


Figure 7-3. ADC Input Network

1. Refer to ADC Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to Digital IO Electrical Characteristics for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. Tau = $(R_{par} + R_{in})* C_{S/H} + R_{par}*(C_{par} + C_I)$
2. K= $\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (Min sampling time) = K*Tau

7.14 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL= 2h (VREF = 1.4V), ADC t_{sample} = 12.5uS	27	30	33	℃
TS_c	Temperature coefficient	-40℃ ≤ T_j ≤ 130℃	-1.9	-1.8	-1.7	mV/℃

7.14 Temperature Sensor (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SET, TS}$	Temperature sensor settling time (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (VREF=1.4V), ADC CHANNEL=29			12.5	us

(1) Higher absolute accuracy may be achieved through user calibration. Please refer to temperature sensor chapter in detailed description section.
(2) This is the minimum required ADC sampling time when measuring the temperature sensor.

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7.15 VREF

7.15.1 Electrical Characteristics ADC

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load	BUFCONFIG = {0, 1}, No load		80	100	µA
TC_{VREF}	Temperature coefficient of VREF (1)	BUFCONFIG = {0, 1}	BUFCONFIG = {0, 1}			75	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	60	70		dB
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 2.7 V to VDDmax, BUFCONFIG = 0	VDD = 2.7 V to VDDmax, BUFCONFIG = 0	50	60		dB
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFFCONFIG = 1	BUFFCONFIG = 1		500		µVrms
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFFCONFIG = 0	BUFFCONFIG = 0		750		µVrms
ADC F_S	Max supported ADC sampling frequency	Using VREF as ADC reference	Using VREF as ADC reference			200	ksps
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8 V	BUFCONFIG = {0, 1} , VDD = 2.8 V			15	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.15.2 Electrical Characteristics (Comparator)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load	BUFCONFIG = {0, 1}, No load		80	100	µA
TC_{VREF}	Temperature coefficient of VREF (1)	BUFCONFIG = {0, 1}	BUFCONFIG = {0, 1}			75	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	VDD = 1.7 V to VDDmax, BUFCONFIG = 1		69		dB
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 2.7 V to VDDmax, BUFCONFIG = 0	VDD = 2.7 V to VDDmax, BUFCONFIG = 0		60		dB
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFFCONFIG = 1	BUFFCONFIG = 1		500		µVrms
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFFCONFIG = 0	BUFFCONFIG = 0		750		µVrms

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7.15.2 Electrical Characteristics (Comparator) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8 V	BUFCONFIG = {0, 1} , VDD = 2.8 V			15	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.15.3 Voltage Characterisitcs (ADC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 0	2.7			V
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
VREF	Voltage reference output voltage	BUFCONFIG = 0	2.46	2.5	2.54	V
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.38	1.4	1.42	V

7.15.4 Voltage Characterisitcs (Comparator)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 0	2.7			V
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
VREF	Voltage reference output voltage	BUFCONFIG = 0	2.46	2.5	2.54	V
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.38	1.4	1.42	V

7.16 *Comparator (COMP)*

7.16.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage				±20	mV
V_{hys}	DC input hysteresis	HYST = 00h		0.4		mV
		HYST = 01h		10		
		HYST = 02h		20		
		HYST = 03h		30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode			5	µs
		Startup time to reach propagation delay specification, Low Power Mode			10	µs

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7.16.1 Comparator Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA
I_{comp}	Comparator +VREF current consumption in low power	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, Internal VREF is reference for DAC, Low Power Mode		1.5		uA
8-bit DAC Electrical Characteristics						
V_{dac}	DAC output range		0		VDD	V
$V_{dac-code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		µs

7.17 LCD

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LCD Electrical Characteristics						
$V_{CC, LCD, CP en, 3.6}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.6 V	LCDCPEN = 1, 0000 < VLCDx ≤ 1111, LCDREFEN = 1 (charge pump enabled, VLCD ≤ 3.6 V)	1.62		3.6	V
Delta VLCD	1/4 bias mode	LCDCPEN = 1, 0000 < VLCDx ≤ 1111, LCDREFEN = 1 (charge pump enabled, VLCD ≤ 3.6 V)		60		mV
Delta VLCD	1/3 bias mode	LCDCPEN = 1, 0000 < VLCDx ≤ 1111, LCDREFEN = 1 (charge pump enabled, VLCD ≤ 3.6 V)		75		mV
$V_{CC, LCD, ext. bias}$	Supply voltage range, external biasing, charge pump enabled	LCDCPEN = 1, LCDREFEN = 0	1.62		3.6	V
$V_{CC, LCD, VLCDEXT}$	Supply voltage range, external LCD voltage, external biasing, charge pump disabled	LCDCPEN = 0, LCDSELVDD = 0	1.62		3.6	V
V_{R33}	External LCD voltage at R33, external biasing, charge pump disabled	LCDCPEN = 0, LCDSELVDD = 0	1.62		3.6	V
V_{R33}	LCD voltage at R33, internal biasing, charge pump enabled	LCDCPEN=1, LCDSELCDD=0, LCDREFEN=1	2.4		3.8	V
C_{LCDCAP}		+/=20% tolerance is recommended, ceramic caps X5R (Between LCDCAP0 and LCDCAP1)		0.47		µF
C_{R33}		+/=20% tolerance is recommended, ceramic caps X5R		0.47		µF

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7.17 LCD (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{R23}		+/=20% tolerance is recommended, ceramic caps X5R		0.47		µF
C_{R24}		+/=20% tolerance is recommended, ceramic caps X5R		0.47		µF
C_{R13}		+/=20% tolerance is recommended, ceramic caps X5R		0.47		µF
f_{Frame}	LCD frame frequency range	f_{LCD} = 2 × mux × f_{FRAME} with mux = 1 (static), 2, 3, 4, 8	16	32	64	Hz
$f_{LFCLK, in}$	LFCLK input frequency range	+/-10% accurate		32.768		kHz
C_{Panel}	Panel capacitance	32-Hz frame frequency			20	nF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	1.6		3.6	V
$V_{R23, 1/3bias}$	Analog input voltage at R23 with 1/3 biasing	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	1.1		2.4	V
$V_{R23, 1/4bias}$	Analog input voltage at R23 with 1/4 biasing	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	1.2		2.7	V
$V_{R24, 1/4bias}$	Analog input voltage at R24 with 1/4 biasing	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	0.8		1.8	V
$V_{R13, 1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	0		1.2	V
$V_{R14, 1/4bias}$	Analog input voltage at R14 with 1/4 biasing	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	0		0.9	V
$V_{LCDREF/R13}$	External LCD reference voltage applied at LCDREF/R13 for 1/4 bias mode	LCDCPEN = 1, LCDSELVDD = 0, LCDREFEN = 0	0.6		0.9	V
$V_{LCDREF/R13}$	External LCD reference voltage applied at LCDREF/R13 for 1/3 bias mode	LCDCPEN = 1, LCDSELVDD = 0, LCDREFEN = 0	0.8		1.2	V
Tamb	Operating Temperature Range		-40	25	125	deg C
IDD LCD	Stand by power - External Biasing (Mode 0), Vboost = OFF. External resistor ladder. 5% matched tolerance and less than 1% individual tolerance	Vdd>=2.4V,LCDCPEN =0, LCDSELVDD=0,LCDSEL_VDD_R33=0,LCD INTBIASEN=0,LVDVERFEN=0, Vboost= OFF, External Supply on		100		nA
IDD LCD	Stand by power - External Biasing (Mode 0), Vboost = ON, External resistor ladder. Current through resistor ladder is not accounted in spec. 5% matched tolerance and less than 1% individual tolerance	Vdd<2.4V,LCDCPEN =0, LCDSELVDD=0,LCDSEL_VDD_R33=0,LCD INTBIASEN=0,LVDVERFEN=0, Vboost= ON, External Supply on		150		nA
IDD LCD	Stand by power - Internal Biasing (Mode 1). Enable VDD connection to R33 pin and add external resistor ladder.Current through resistor ladder is not accounted in spec	LCDCPEN =0, LCDSELVDD=1,LCDSEL_VDD_R33=0,LCD INTBIASEN=0, LCDVREFEN =0(Internal reference disabled),Vboost= OFF, External Supply Off		54		uA
IDD LCD	Stand by power - External Biasing (Mode 2). Check for LCD_HP_LP=0/1 and LCDBIASSEL=0/1	LCDCPEN =0, LCDSELVDD=0,LCDSEL_VDD_R33=0,LCD INTBIASEN=1, LCDVREFEN =0(Internal reference disabled),Vboost= OFF, External Supply on		100		nA

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7.17 LCD (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD LCD	Stand by power - Internal Biasing (Mode 3). Check for LCD_HP_LP=0/1 and LCDBIASSEL=0/1. AVDD connected to internal ladder used to generate voltages	LCDCPEN =0, LCDSELVDD=0,LCDSEL_VDD_R33=1,LCD INTBIASEN=1, LCDVREFEN =0(Internal reference disabled),Vboost= OFF, External Supply off		57		uA
IDD LCD	Stand by power - External Biasing (Mode 4). Check for LCDBIASSEL=0/1. Vext connected to R33. CP used to generate voltage fractions	LCDCPEN =1, LCDSELVDD=0,LCDSEL_VDD_R33=0,LCD INTBIASEN=0, LCDVREFEN =0(Internal reference disabled),Vboost= OFF, External Supply on		200		nA
IDD LCD	Stand by power - Internal Biasing (Mode 5). Check for LCDBIASSEL=0/1.AVDD connected to R33. CP used to generate voltage fractions. LOADCAP0/1 are connected	LCDCPEN =1,LCDCPFSELx=0x2 LCDSELVDD=1,LCDSEL_VDD_R33=1,LCD INTBIASEN=0, LCDVREFEN =0(Internal reference disabled),Vboost= OFF, External Supply off		300		nA
IDD LCD	Stand by power - External Biasing (Mode 6). CP used to generate 1/3 and 1/4 voltage fractions. Vext connected to R13. LOADCAP0/1 are connected	LCDCPEN =1, LCDSELVDD=0,LCDSEL_VDD_R33=1,LCD INTBIASEN=0, LCDVREFEN =0(Internal reference disabled),Vboost= OFF, External Supply on		200		nA
IDD LCD	Stand by power - Internal Biasing (Mode 7). CP used to generate 1/3 and 1/4 voltage fractions. LOADCAP0/1 are connected. Vboost = OFF	LCDCPEN =1,LCDCPFSELx=0x2,VLCDx=3V LCDSELVDD=0,LCDSEL_VDD_R33=1,LCD INTBIASEN=0, LCDVREFEN =1(Internal reference enabled),LCDREFMODE =0/1		1.2		µA
IDD LCD	Stand by power - Internal Biasing (Mode 7). CP used to generate 1/3 and 1/4 voltage fractions. LOADCAP0/1 are connected. Vboost = ON	LCDCPEN =1,LCDCPFSELx=0x2,VLCDx=3V LCDSELVDD=0,LCDSEL_VDD_R33=1,LCD INTBIASEN=0, LCDVREFEN =1(Internal reference enabled),LCDREFMODE =0/1		1.5		µA

7.18 *I2C*

7.18.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency		2	32	8	32	20	32	MHz
f_{SCL}	SCL clock frequency		0.025	0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us

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7.18.1 I2C Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

7.18.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.18.3 *I²C Timing Diagram*

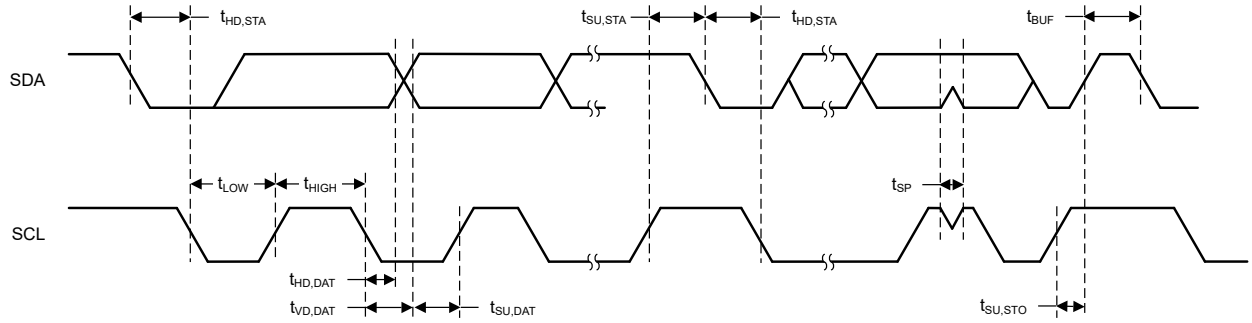


Figure 7-4. I2C Timing Diagram

7.19 *SPI*

7.19.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.62 < VDD < 3.6V Controller mode			16	MHz
f_{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.62 < VDD < 3.6V Peripheral mode			16	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=0	1 SPI Clock			ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=1	1/2 SPI Clock			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1 SPI Clock			ns
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI Clock	ns

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7.19.1 SPI (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance				1 SPI Clock	ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, delayed sampling enabled	1			ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	29			ns
$t_{SU.CI}$	POCI input data setup time (1)	1.62 < VDD < 2.7V, no delayed sampling	37			ns
$t_{HD.CI}$	POCI input data hold time	delayed sampling enabled	24			ns
$t_{HD.CI}$	POCI input data hold time	no delayed sampling enabled	0			ns
$t_{VALID.CO}$	PICO output data valid time (2)				10	ns
$t_{HD.CO}$	PICO output data hold time (3)		6			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		11			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				26	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance				26	ns
$t_{SU.PI}$	PICO input data setup time		7			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(2)	2.7 < VDD < 3.6V			25	ns
$t_{VALID.PO}$	POCI output data valid time(2)	1.62 < VDD < 2.7V			31	ns
$t_{HD.PO}$	POCI output data hold time(3)		5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.19.2 SPI Timing Diagram

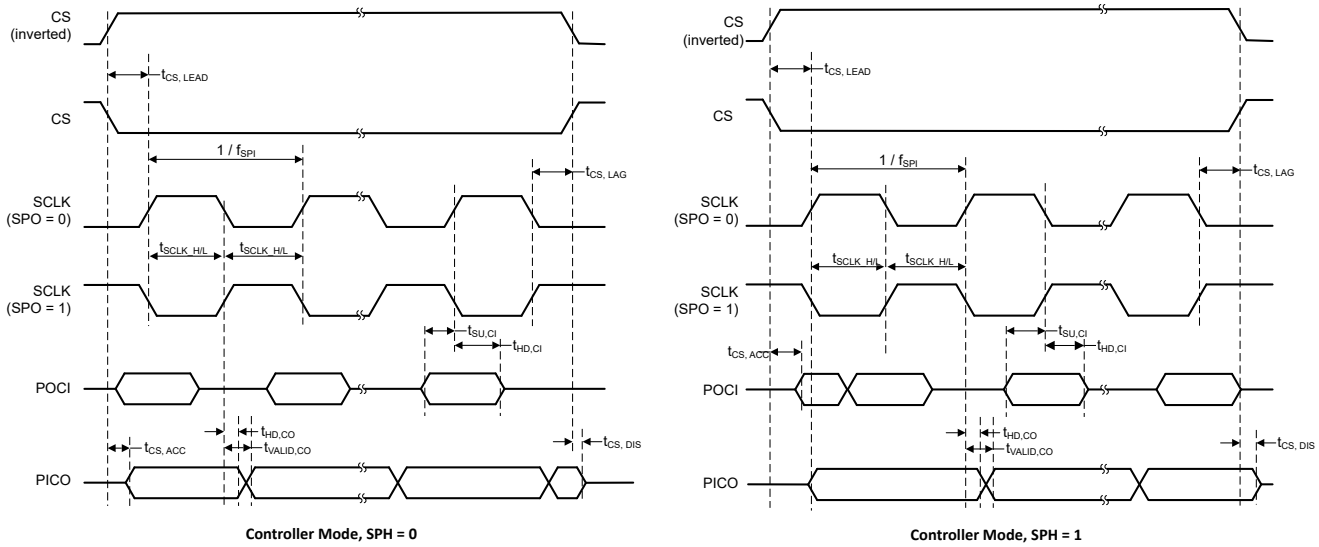


Figure 7-5. SPI Timing Diagram - Controller Mode

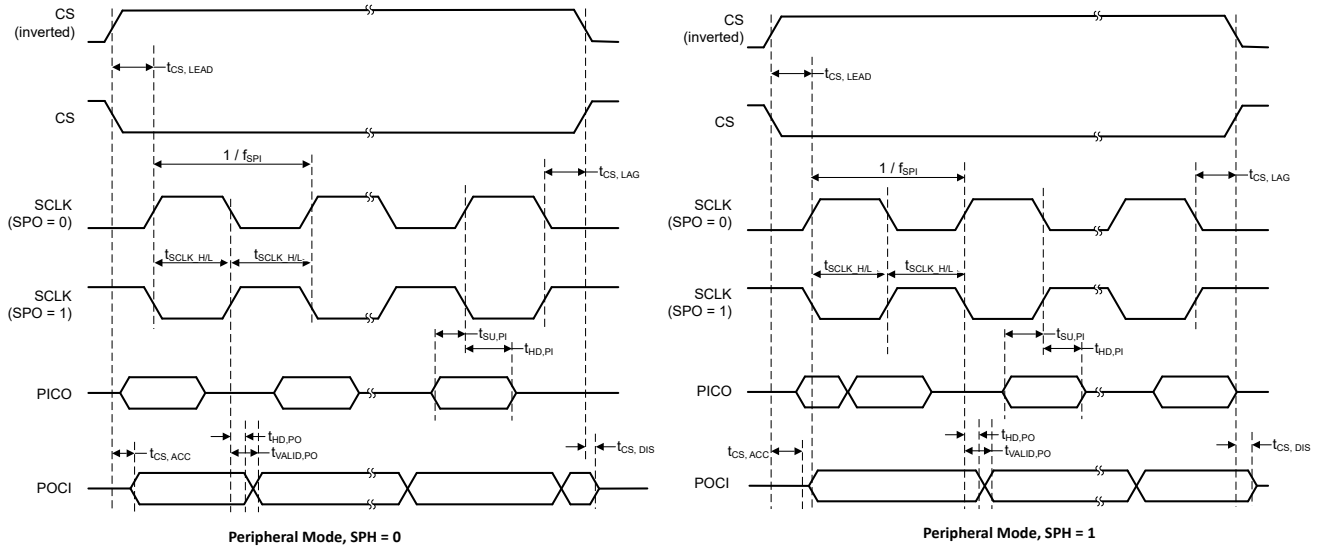


Figure 7-6. SPI Timing Diagram - Peripheral Mode

7.20 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency				32	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				4	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 1		14	35	ns
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 2		22	60	ns
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 3		35	90	ns

7.21 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 32MHz	31.25			ns
			1			$t_{TIMxCLK}$
t_{res}	Timer resolution time	TIMx with 16bit counter			16	bit
t_{res}	Timer resolution time	TIMx with 32bit counter			32	bit
$t_{COUNTER}$	32-bit counter clock period	$f_{TIMxCLK}$ = 32MHz	0.03125		134.21	s
			1		4294967296	$t_{TIMxCLK}$
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 32MHz	0.03125		2048	us
			1		65536	$t_{TIMxCLK}$

7.22 *TRNG*

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7.22.1 TRNG Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNG_{IACT}$	TRNG active current	TRNG clock = 20MHz		115		µA

7.22.2 TRNG Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TRNGCLK_F$	TRNG input clock frequency		9.5	10	25	MHz
$TRNG_{STARTUP}$	TRNG startup time			520		µs
$TRNG_{LAT32}$	Latency to generate 32 random bits	Decimation ratio = 4, TRNG clock = 20MHz		6.4		µs
$TRNG_{LAT256}$	Latency to generate 256 random bits	Decimation ratio = 4, TRNG clock = 20MHz		51.2		µs

7.23 Emulation and Debug

7.23.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

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8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.1 Functional Block Diagram

Figure 8-1 shows the functional block diagram.

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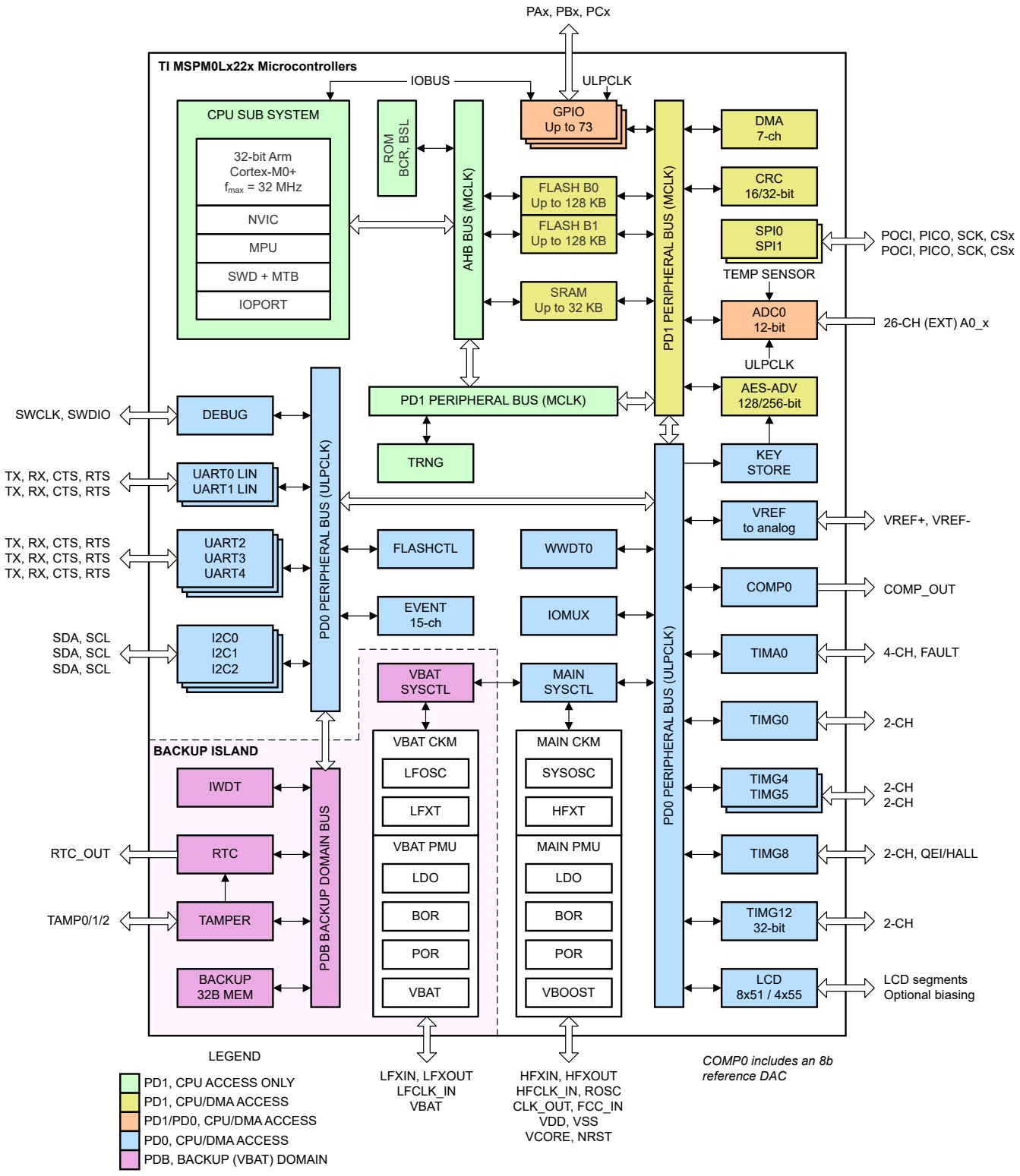


Figure 8-1. MSPM0Lx22x Functional Block Diagram

8.2 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction pre-fetch/cache, a system timer, a memory protection unit, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized,

32-bit CPU which delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supporting clock frequencies up to 32kHz
  - ARMv6-M Thumb instruction set (little endian) with single-cycle 32×32 multiply instruction
  - Single-cycle access to GPIO registers through Arm single-cycle IO port
- Pre-fetch logic to improve sequential code execution, and I-cache with four 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Memory protection unit (MPU) with 8 programmable regions
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining
- Interrupt groups for expanding the total interrupt sources, with jump index for low interrupt latency

8.3 Operating Modes

MSPM0 MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0 devices implement two power domains: **PD1** (for the CPU, memories, and high performance peripherals), and **PD0** (for low speed, low power peripherals).

- **PD1** is always powered in RUN and SLEEP modes, but is disabled in all other modes.
- **PD0** is always powered in RUN, SLEEP, STOP, and STANDBY modes.
- PD1 and PD0 are both disabled in SHUTDOWN mode.
- PDB (for VBAT island) is operational irrespective of mode.

8.3.1 Functionality by Operating Mode (MSPM0Lx22x)

Supported functionality in each operating mode is given in Table 8-1.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode but is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Mode

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT(1)	EN	DIS	DIS	DIS	OFF
	LFOSC or LFXT	EN (LFOSC or LFXT)											EN
	HFXT	OPT	DIS	DIS	OPT	DIS	DIS	DIS	DIS	DIS	DIS	DIS	OFF

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Table 8-1. Supported Functionality by Operating Mode (continued)

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Clocks	CPUCLK	32MHz	32kHz	32kHz	DIS								OFF
	MCLK to PD1	32MHz	32kHz	32kHz	32MHz	32kHz	32kHz	DIS					OFF
	ULPCLK to PD0	32MHz	32kHz	32kHz	32MHz	32kHz	32kHz	4MHz[1]	4MHz	32kHz		DIS	OFF
	ULPCLK to TIMG0, TIMG4, TIMG5, TIMG8, TIMG12, TIMA0	32MHz	32kHz	32kHz	32MHz	32kHz	32kHz	4MHz[1]	4MHz	32kHz			OFF
	MFCLK	OPT	DIS		OPT	DIS		OPT		DIS			OFF
	MFPCLK	OPT	DIS		OPT	DIS		OPT		DIS			OFF
	LFCLK	32kHz										DIS	OFF
	LFCLK to TIMG0, TIMG4, TIMG5, TIMG8, TIMG12, TIMA0	32kHz											OFF
	LFCLK Monitor	OPT											OFF
	MCLK Monitor	OPT										DIS	OFF
PMU	POR monitor	EN											
	BOR monitor	EN											OFF
	Core regulator	FULL DRIVE						REDUCED DRIVE			LOW DRIVE		OFF
VBAT	POR monitor	EN											
	BOR monitor	EN											
	Core regulator	EN											
Core Functions	CPU	EN			DIS								OFF
	DMA	OPT						DIS (triggers supported)					OFF
	Flash	EN						DIS					OFF
	SRAM	EN						DIS					OFF
PD1 Peripherals	CRC	OPT											OFF
	SPI0, SPI1	OPT											OFF
	AESADV	OPT											OFF

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Table 8-1. Supported Functionality by Operating Mode (continued)

OPERATING MODE		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
PD0 Peripherals	Keystore	OPT											OFF
	UART0, UART1, UART2, UART3, UART4	OPT										OPT[2]	OFF
	I2C0, I2C1	OPT										OPT[2]	OFF
	TIMG0, TIMG4, TIMG5, TIMG8, TIMG12	OPT											OFF
	TIMA0	OPT											OFF
	COMP0	OPT											OFF
	LCD	OPT											OFF
	GPIOA, GPIOB, GPIOC[3]	OPT										OPT[2]	OFF
	WWDT0	OPT										DIS	OFF
LFSS Peripherals	IWDT	OPT											OPT
	RTC_A	OPT											OPT
	Tamper I/O, SPM	OPT											OPT
Analog	TRNG	OPT											OFF
	ADC0 [3]	OPT								NS (triggers supported)			OFF
	COMP0	OPT	OPT (ULP)		OPT	OPT (ULP)		OPT		OPT (ULP)			OFF
	Temperature Sensor	OPT									OFF		OFF
IOMUX and IO Wakeup		EN											DIS w/ WAKE
Wake Sources		N/A			ANY IRQ			PD0 IRQ					IOMUX, NRST, SWD

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as in RUN1, and ULPCLK remains at 32kHz as in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as in RUN2, and ULPCLK remains at 32kHz as in RUN2.
(2) When using the STANDBY1 policy for STANDBY, all TIMx instances and the RTC are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.
(3) For ADCx and GPIO Ports A, B and C, the digital logic is in PD0 and the register interface is in PD1. These peripherals support fast single-cycle register access when PD1 is active and also support basic operation down to STANDBY mode where PD0 is still active.

8.4 Security

This PSA-L1 certified device offers several security features, including:

- Debug security
- Device identify
- Crypto acceleration
- True random number generation
- Flash write-erase protection
- Flash read-execute protection
- Flash IP protection
- SRAM write-execute mutual exclusion
- Secure boot
- Secure firmware update

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- Secure key storage
- Customer secure code
- Hardware monotonic counter

For more details, see the Security chapter of the .

8.5 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY mode to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.6 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32kHz)
- **SYSOSC**: Internal high-frequency oscillator (4MHz or 32MHz with factory trim, 16MHz or 24MHz with user trim)
- **LFXT/LFCKIN** : low-frequency external crystal oscillator or digital clock input (32kHz)
- **HFXT/HFCKIN**: high-frequency external crystal oscillator or digital clock input (4MHz to 32MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **MFPCLK**: 4MHz fixed mid-frequency precision clock, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode

For more details, see the CKM chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.7 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 7 independent DMA transfer channels
- Configurable DMA channel priorities

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- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications

Table 8-2 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-2. DMA Trigger Mapping

DMACTL.DMATSEL	TRIGGER SOURCE	DMACTL.DMATSEL	TRIGGER SOURCE
0	Software	13	SPI1 Publisher 1
1	Generic Subscriber 0 (FSUB_0)	14	SPI1 Publisher 2
2	Generic Subscriber 0 (FSUB_1)	15	UART0 Publisher 1
3	AES Publisher 1	16	UART0 Publisher 2
4	AES Publisher 1	17	UART1 Publisher 1
5	I2C0 Publisher 1	18	UART1 Publisher 2
6	I2C0 Publisher 2	19	UART2 Publisher 1
7	I2C1 Publisher 1	20	UART2 Publisher 2
8	I2C1 Publisher 2	21	UART3 Publisher 1
9	I2C2 Publisher 1	22	UART3 Publisher 2
10	I2C2 Publisher 2	23	UART4 Publisher 1
11	SPI0 Publisher 1	24	UART4 Publisher 2
12	SPI1 Publisher 2	25	ADC0 Publisher 2

For more details, see the DMA chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.8 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events which are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the EVENT chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

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Table 8-3. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
5	Generic event channel 5 selected	1 : 1
6	Generic event channel 6 selected	1 : 1
7	Generic event channel 7 selected	1 : 1
8	Generic event channel 8 selected	1 : 1
9	Generic event channel 9 selected	1 : 1
10	Generic event channel 10 selected	1 : 1
11	Generic event channel 11 selected	1 : 1
12	Generic event channel 12 selected	1 : 2 (splitter)
13	Generic event channel 13 selected	1 : 2 (splitter)
14	Generic event channel 14 selected	1 : 2 (splitter)
15	Generic event channel 15 selected	1 : 2 (splitter)

8.9 Memory

8.9.1 Memory Organization

Table 8-4 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 Lx22x-Series 32MHz Microcontrollers Technical Reference Manual* .

Table 8-4. Memory Organization

MEMORY REGION	SUBREGION	MSP0L1227, MSPM0L2227	MSPM0L1228, MSPM0L2228
Code (Flash Bank 0)	MAIN ECC Corrected	64KB[1] 0x0000.0000 to 0x0000.FFFF	128KB[1] 0x0000.0000 to 0x0001.FFFF
	MAIN ECC Uncorrected	0x0040.0000 to 0x0040.FFFF	0x0040.0000 to 0x0041.FFFF
	Flash ECC code	0x0080.0000 to 0x0080.FFFF	0x0080.0000 to 0x0081.FFFF
Code (Flash Bank 1)	MAIN ECC Corrected	64KB[1] 0x0001.0000 to 0x0001.FFFF	128KB[1] 0x0002.0000 to 0x0003.FFFF
	MAIN ECC Uncorrected	0x0041.0000 to 0x0041.FFFF	0x0042.0000 to 0x0043.FFFF
	Flash ECC code	0x0081.0000 to 0x0081.FFFF	0x0082.0000 to 0x0083.FFFF
SRAM (SRAM)	SRAM "ECC Checked"	32KB 0x2000.0000 to 0x2000.7FFF	32KB 0x2000.0000 to 0x2000.7FFF
	Parity checked	0x2010.0000 to 0x2010.7FFF	0x2010.0000 to 0x2010.7FFF
	Un-checked	0x2020.0000 to 0x2020.7FFF	0x2020.0000 to 0x2020.7FFF
	ECC/parity code	0x2030.0000 to 0x2030.7FFF	0x2030.0000 to 0x2030.7FFF

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Table 8-4. Memory Organization (continued)

MEMORY REGION	SUBREGION	MSP0L1227, MSPM0L2227	MSPM0L1228, MSPM0L2228
Peripheral	Peripherals	0x4000.4000 to 0x4087.1FFF	0x4000.4000 to 0x4087.1FFF
	Configuration NVM (NONMAIN) Corrected	0x41C0.0000 to 0x41C0.03FF	0x41C0.0000 to 0x41C0.03FF
	Configuration NVM (NONMAIN) Uncorrected	0x41C1.0000 to 0x41C1.03FF	0x41C1.0000 to 0x41C1.03FF
	Configuration NVM (NONMAIN) ECC code	0x41C2.0000 to 0x41C2.03FF	0x41C2.0000 to 0x41C2.03FF
	FACTORY Corrected	0x41C4.0000 to 0x41C4.01FF	0x41C4.0000 to 0x41C4.01FF
	FACTORY Uncorrected	0x41C5.0000 to 0x41C5.01FF	0x41C5.0000 to 0x41C5.01FF
	FACTORY ECC code	0x41C6.0000 to 0x41C6.01FF	0x41C6.0000 to 0x41C6.01FF
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

(1) First 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program/erase cycles.

8.9.2 Peripheral File Map

Table 8-5 lists the available peripherals and the register base address for each.

Table 8-5. Peripherals Summary

PERIPHERAL NAME	BASE ADDRESS	SIZE
ADC0	0x40004000	0x2000
COMP0	0x40008000	0x2000
VREF	0x40030000	0x2000
LCD	0x40070000	0x2000
WWDT0	0x40080000	0x2000
TIMG0	0x40084000	0x2000
TIMG4	0x4008C000	0x2000
TIMG5	0x4008E000	0x2000
TIMG8	0x40090000	0x2000
LFSS (RTC_A, TIO, IWDT, SPM)	0x40094000	0x2000
RTC_A	0x40095100	0x100
TIO	0x40095200	0x100
IWDT	0x40095300	0x100
SPM	0x040095400	0x100
GPIOA	0x400A0000	0x2000
GPIOB	0x400A2000	0x2000
GPIOC	0x400A4000	0x2000
KEYSTORE	0x400AC000	0x2000
SYSCTL	0x400AF000	0x4000
DEBUGSS	0x400C7000	0x2000
EVENT	0x400C9000	0x3000
NVM	0x400CD000	0x2000
I2C0	0x400F0000	0x2000
I2C1	0x400F2000	0x2000
I2C2	0x400F4000	0x2000
UART2	0x40100000	0x2000
UART3	0x40102000	0x2000
UART4	0x40104000	0x2000

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Table 8-5. Peripherals Summary (continued)

PERIPHERAL NAME	BASE ADDRESS	SIZE
UART0	0x40108000	0x2000
UART1	0x4010A000	0x2000
MCPUSS	0x40400000	0x2000
WUC	0x40424000	0x2000
IOMUX	0x40428000	0x2000
DMA	0x4042A000	0x2000
CRC	0x40440000	0x2000
AESADV	0x40442000	0x2000
TRNG	0x40444000	0x2000
SPI0	0x40468000	0x2000
SPI1	0x4046A000	0x2000
ADC0(1)	0x4055A000	0x2000
TIMA0	0x40860000	0x2000
TIMG12	0x40870000	0x2000

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8.9.3 Peripheral Interrupt Vector

Table 8-6 shows the IRQ number and the interrupt group number for each peripheral in this device.

Table 8-6. Interrupt vector number

Peripheral Name	NVIC IRQ	Group IIDX
WWDT0	0	0
DEBUGSS	0	2
FLASHCTL	0	3
EVENT SUB PORT 0	0	4
EVENT SUB PORT 1	0	5
SYSCTL	0	6
GPIOA	1	0
GPIOB	1	1
COMP0	1	2
TRNG	1	5
GPIOC	1	6
TIMG12	2	-
UART4	3	-
ADC0	4	-
SPI0	9	-
SPI1	10	-
UART2	13	-
UART3	14	-
UART0	15	-
UART1	16	-
TIMA0	18	-
TIMG8	20	-
TIMG0	21	-
TIMG4	22	-
TIMG5	23	-
I2C0	24	-
I2C1	25	-
I2C2	26	-
AESADV	28	-
LCD0	29	-
LFSS	30	-
DMA0	31	-

8.10 Flash Memory

A dual bank of nonvolatile flash memory (up to 128KB or 256KB total) is provided for storing executable program code and application data.

Key features of the flash include:

- Hardware ECC protection (encode and decode) with single bit error correction and double-bit error detection
- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)

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- Up to 100,000 program/erase cycles on the 32 selected sectors of the flash memory, with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32kB support 100,000 cycles on the entire flash memory)

For more details, see the NVM chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.11 SRAM

MSPM0 MCUs include a low power, high performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. MSPM0 MCUs also provide up to 128KB of ECC protected SRAM with hardware parity. SRAM memory may be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY modes and is lost in shutdown mode.

A write-execute mutual exclusion mechanism is provided to allow the application to partition the SRAM into two sections: a read-write (RW) partition and a read-execute (RX) partition. The RX partition occupies the upper portion of the SRAM address space. Write protection is useful when placing executable code into SRAM as it provides a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.12 GPIO

The general purpose input/output (GPIO) peripheral provides the user with a means to write data out and read data in to and from the device pins. Through the use of the Port A, Port B and Port C GPIO peripherals, these devices support up to 60 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

For more details, see the GPIO chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.13 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.14 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.68Msps with greater than 11-bit ENOB
- Hardware averaging enables 14-bit conversion resolution at 105ksps
- Up to 26 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- Software selectable reference:

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  - Configurable internal dedicated ADC reference voltage of 1.4V and 2.5V (VREF)
  - MCU supply voltage (VDD)
  - External reference supplied to the ADC through the VREF+ and VREF- pins
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-7. ADC Channel Mapping

Channel [0:15]	Signal Name (ADC0)(1) (2)	Channel [16:31]	Signal Name (ADC0)(1) (2)
0	A0_0	16	A0_16
1	A0_1	17	A0_17
2	A0_2	18	A0_18
3	A0_3	19	A0_19
4	A0_4	20	A0_20
5	A0_5	21	A0_21
6	A0_6	22	A0_22
7	A0_7	23	A0_23
8	A0_8	24	A0_24
9	A0_9	25	A0_25
10	A0_10	26	-
11	A0_11	27	-
12	A0_12	28	*VREF*
13	A0_13	29	*Temperature Sensor*
14	A0_14	30	*VBAT Monitor*
15	A0_15	31	*Supply/Battery Monitor*

(1) *Italicized* signal names are purely internal to the device. These signals are used for internal peripheral interconnections.
(2) For more information about device analog connections, refer to Section 8.31

For more details, see the ADC chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.15 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4V internal VREF at the factory trim temperature (TS_{TRIM}). This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.16 LFSS

The Low-Frequency Subsystem (LFSS) combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low-frequency clock (LFCLK) or need to be active during low-power modes. In this device, LFSS is powered by a separate battery backup domain called VBAT. The low-frequency clock has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS in this device contains following components:

- A dedicated battery backup domain supply and dedicated pin (VBAT)
- Real-time clock (RTC_A) with additional prescalar extension and timestamp captures
- An asynchronous Independent Watchdog Timer (IWDT)
- Tamper detection input / output (TIO) module

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- Tamper detection with timestamp
- A small scratchpad memory storage (SPM)
- Heartbeat generator

For more details, see the LFSS chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.17 VREF

VREF for ADC

The voltage reference module (VREF) contains a configurable voltage reference buffer dedicated for the on-board ADC. The devices also support connection of an external reference for applications in which higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references. Same reference voltage will be selected for ADC and COMP
- Internal reference supports ADC operation at 200ksps
- Support for bringing in an external reference on VREF+ and VREF- device pins
- Requires a decoupling capacitor placed on VREF+ pin and VREF- pins for proper operation. See VREF specification section for more details

VREF for COMP

The voltage reference module (VREF) contains a configurable voltage reference buffer dedicated for the on-board COMP. The devices also support connection of an external reference for applications in which higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal reference for COMP. Same reference voltage will be selected for ADC and COMP.
- Supports low power mode operation of COMP+VREF in standby mode.
- Support for bringing in an external reference on VREF+ and VREF- device pins.
- Requires a decoupling capacitor placed on VREF+ pin and VREF- pins for proper operation. See VREF specification section for more details.

For more details, see the VREF chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.18 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
  - External reference voltage (VREF IO)
  - Dedicated Internal reference voltage (1.4V, 2.5V) available in RUN/SLEEP/STOP/STANDBY modes.
  - Integrated 8-bit reference DAC
- Configurable operation modes:
  - High speed mode
  - Lower power mode
- Programmable output glitch filter delay
- Support output wake up device from all low power modes
- Output connected to advanced timer fault handling mechanism
- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins or from internal analog modules.

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Table 8-8. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x3	COMP0_IN3+	-
0x5	-	Temp Sensor output

For more information about device analog connections, refer to Section 8.31.

For more details, see the COMP chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.19 TRNG

The true random number generator (TRNG) utilizes an internal circuit to generate 32-bit random numbers. The TRNG is intended to be used as a source to a deterministic random number generator (DRNG) to build a FIPS-140-2 compliant system. Key features of the TRNG include:

- Generation of 32-bit random numbers
- A new 32-bit number can be generated every 32 × 4 = 128 TRNG clock cycles
- Built-in health tests
- Available in RUN and SLEEP modes

For more details, see the TRNG chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.20 AESADV

The AES advanced (AESADV) accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware according to the advanced encryption standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AESADV accelerator features include:

- AES operation with 128-bit and 256-bit keys
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- AES-CCM
- AES-GCM
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AESADV ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the *Operating Modes* section of the device technical reference manual)

For more details, see the AESADV chapter of the .

8.21 Keystore

The Keystore controller provides secure management of the Advanced Encryption Engine (AES) keys. The use-model of the keystore controller is to securely deposit keys into it during the execution of customer secure code, and have the AES engine access them subsequently in a secure manner without leaking any key data to observers. Both 128 and 256-bit keys can be stored in the keystore's key slots. The keystore and its interaction with the AES engine are designed for secure operation including thwarting partial key modification attacks.

For more details, see the KEYSTORE chapter of the .

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8.22 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal
- Support for custom polynomials

For more details, see the CRC chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.23 UART

The UART peripherals (UART0, UART1, UART2, UART3, UART4) provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DMA data transfer
- Support transmit and receive loopback mode operation
- See Table 8-9 for detail information on supported protocols.

Table 8-9. UART Features

UART Features	UART0, UART1 (Extend)	UART2, UART3, UART4 (Main)
Active in Stop and Standby Mode	Yes	Yes
Separate transmit and receive FIFOs	Yes	Yes
Support hardware flow control	Yes	Yes
Support 9-bit configuration	Yes	Yes
Support LIN mode	Yes	-
Support DALI	Yes	-
Support IrDA	Yes	-
Support ISO7816 Smart Card	Yes	-
Support Manchester coding	Yes	-

For more details, see the UART chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.24 I2C

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100kbps
- Support Fast-mode (Fm), with a bit rate up to 400kbps
- Support Fast-mode Plus (Fm+), with a bit rate up to 1Mbps
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support

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- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression

For more details, see the I2C chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.25 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to Mbits/s in both controller and peripheral mode
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode)
- Programmable data frame size from 7 bits to 16 bits (peripheral mode)
- Separated transmit and receive FIFOs support DMA data transfer
- Supports TI mode, Motorola mode, and National Microwire format

For more details, see the SPI chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.26 IWDT

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent power and clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods (2ms to 2hr)

For more details, see the IWDT chapter of the .

8.27 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.28 RTC_A

The RTC_A instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. RTC_A provides common key features in relation to the Low-Frequency Subsystem (LFSS).

Common key features of RTC_A include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format

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- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz
- Calibration for crystal offset error (up to ±240ppm)
- Compensation for temperature drift (up to ±240ppm)
- RTC clock output to pin for calibration
- Three bit prescaler for heartbeat function with interrupt generation
- RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz, or 1Hz
- RTC time stamp capture upon detection of a timer stamp event, including tamper (TIO) event and VDD fail event
- RTC counter lock function

Table 8-10 shows the RTC features supported in this device.

Table 8-10. RTC Instances and Key Features

RTC Features	RTC_A
Power enable register	-
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes
Selectable binary or binary-coded decimal (BCD) format	Yes
Leap-year correction (valid for year 1901 through 2099)	Yes
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes
Calibration for crystal offset error and crystal temperature drift (up to ±240ppm total)	Yes
RTC clock output to pin for calibration (GPIO)	Yes
RTC clock output to pin for calibration (TIO)	Yes
Three bit prescaler for heartbeat function with interrupt generation	Yes
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	Yes
RTC time stamp capture upon detection of a timer stamp event, including: • TIO event • VDD fail event	Yes
RTC counter lock function	Yes

For more details, see the RTC chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.29 Timers (TIMx)

There are two timer peripherals in these devices support that following key features: TIMGx (general-purpose timer) and TIMAx (advanced timer). TIMGx is a subset of TIMAx, which means these timers share many common features that are compatible in software. For specific configuration, see Table 8-11:

Specific features for the general-purpose timer **(TIMGx)** include:

- 16-bit and 32-bit timers with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent CC channels for
  - Output compare
  - Input capture

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  - PWM output
  - One-shot mode
- Support quadrature encoder interface (QEI) for positioning and movement sensing available in TIMG8
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Cross trigger event logic for Hall sensor inputs (TIMG8)

Specific features for the advanced timer **(TIMAx)** include:

- 16-bit timer with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Two additional capture/compare channels for internal events (CC4/CC5)
- Shadow register for load and CC register available in TIMA0
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to ensure the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt and DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-11. TIMx Instance Configuration

Instance	Power Domain	Counter Resolution	Prescaler	Repeat Counter	CCP Channels (External/ Internal)	External PWM Channels	Phase Load	Shadow Load	Shadow CCs	Deadband	Fault Handler	QEI / Hall Input Mode
TIMG0	PD0	16-bit	8-bit	-	2	2	-	-	-	-	-	-
TIMG4	PD0	16-bit	8-bit	-	2	2	-	Yes	Yes	-	-	-
TIMG5	PD0	16-bit	8-bit	-	2	2	-	Yes	Yes	-	-	-
TIMG8	PD0	16-bit	8-bit	-	2	2	-	-	-	-	-	Yes
TIMG12	PD0	32-bit	-	-	2	2	-	-	Yes	-	-	-
TIMA0	PD0	16-bit	8-bit	Yes	4/2	8	Yes	Yes	Yes	Yes	Yes	-

Table 8-12. TIMx Cross Trigger Map (PD0)

TSEL.ETSEL Selection	TIMA0	TIMG0	TIMG4	TIMG5	TIMG8	TIMG12
0	TIMA0.TRIGO	TIMA0.TRIGO	TIMA0.TRIGO	TIMA0.TRIGO	TIMA0.TRIGO	TIMA0.TRIGO
1	TIMG0.TRIGO	TIMG0.TRIGO	TIMG0.TRIGO	TIMG0.TRIGO	TIMG0.TRIGO	TIMG0.TRIGO
2	TIMG4.TRIGO	TIMG4.TRIGO	TIMG4.TRIGO	TIMG4.TRIGO	TIMG4.TRIGO	TIMG4.TRIGO
3	TIMG5.TRIGO	TIMG5.TRIGO	TIMG5.TRIGO	TIMG5.TRIGO	TIMG5.TRIGO	TIMG5.TRIGO
4	TIMG8.TRIGO	TIMG8.TRIGO	TIMG8.TRIGO	TIMG8.TRIGO	TIMG8.TRIGO	TIMG8.TRIGO
5	TIMG12.TRIGO	TIMG12.TRIGO	TIMG12.TRIGO	TIMG12.TRIGO	TIMG12.TRIGO	TIMG12.TRIGO
6 to 15	Reserved					
16	Event Subscriber Port 0 (FSUB0)					
17	Event Subscriber Port 1 (FSUB1)					
18-31	Reserved					

The following tests can be applied as functional safety mechanisms for this module (to provide diagnostic coverage on a specific function):

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Table 8-13. Timers Safety Mechanisms

Safety Mechanism	Description	Faults/Failure modes
TIM1	Test for PWM generation	Targeted towards PWM generation logic, including the counters, compare registers, clocking logic, output generation logic etc.
TIM2	Periodic Software Read Back of IP Static Configuration Registers	Targets the static configuration registers in Timer.
TIM3(latent fault coverage)	Test for fault generation	This test is a test for diagnostic, which checks the functioning of fault detection logic in timer. **Note** This test is applicable only to TIMAx.
TIM4	Fault detection to take the PWMs to safe state	This safety mechanism can be used to detect faults which result in system level failures like over/under voltages/currents. The external faults can be monitored using the fault pins or the analog comparators. The faults which can be covered include the faults in the PWM generation logic, faults in external drivers etc. **Note** This test is applicable only to TIMAx.
TIM5	Input capture on two or more timer instances	This test is used to cover the faults in the capture mode logic. The faults could be in clocking, capture logic, counter logic etc.
TIM6	Timer period monitoring.	This test is a run time check in which the duration between two interrupts can be measured (using another timer). This is useful in detecting faults which result in the counter taking more or less time than expected and can also cover the clocking related faults.
WDT	Windowed watchdog event	Targeted towards faults which result in missing interrupts (periodic interrupts) affecting the program sequence of the CPU. These could be faults in the interrupt logic or the logic which sets the interrupt flags or the logic which generated hardware triggers for other IPs (ADC for example) etc.

8.30 LCD

The Liquid Crystal Display (LCD) controller directly drives LCD displays through the segment (SEG) and common (COM) voltage signals. The controller can support 2-mux to 8-mux LCD glasses. The main features of the LCD controller are:

- Display memory

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- Standby mode support
- Configurable SEG and COM pins
- Automatic signal generation
- Configurable frame frequency
- Blinking of individual segments with separate blinking memory for static and 2-4 mux LCD
- Blinking of complete display for 5-8 mux LCDs
- Regulated charge pump up to 3.6V (typical)
- Internal resistor divider for generating bias voltages
- Internal charge pump for generating bias voltages
- Contrast control by software
- Ability to use LCD IOs as GPIOs or analog signals when pins are not used for LCD operation
- Supports static, 1/3 and 1/4 bias modes. 1/2 bias mode is not supported.

For more details, see the LCD chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

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8.31 Device Analog Connections

Figure 8-2 shows the internal analog connection of the device.

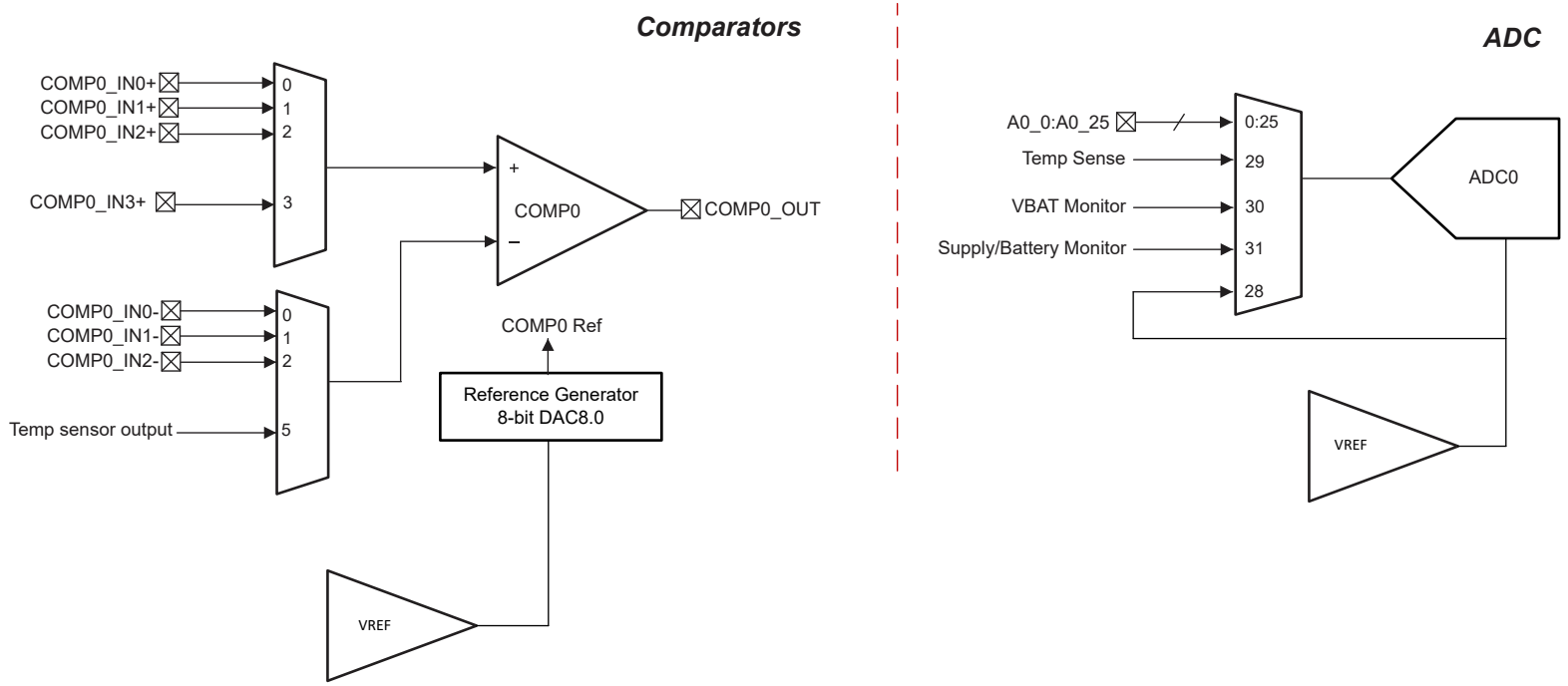


Figure 8-2. Device Analog Connection

8.32 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-3. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

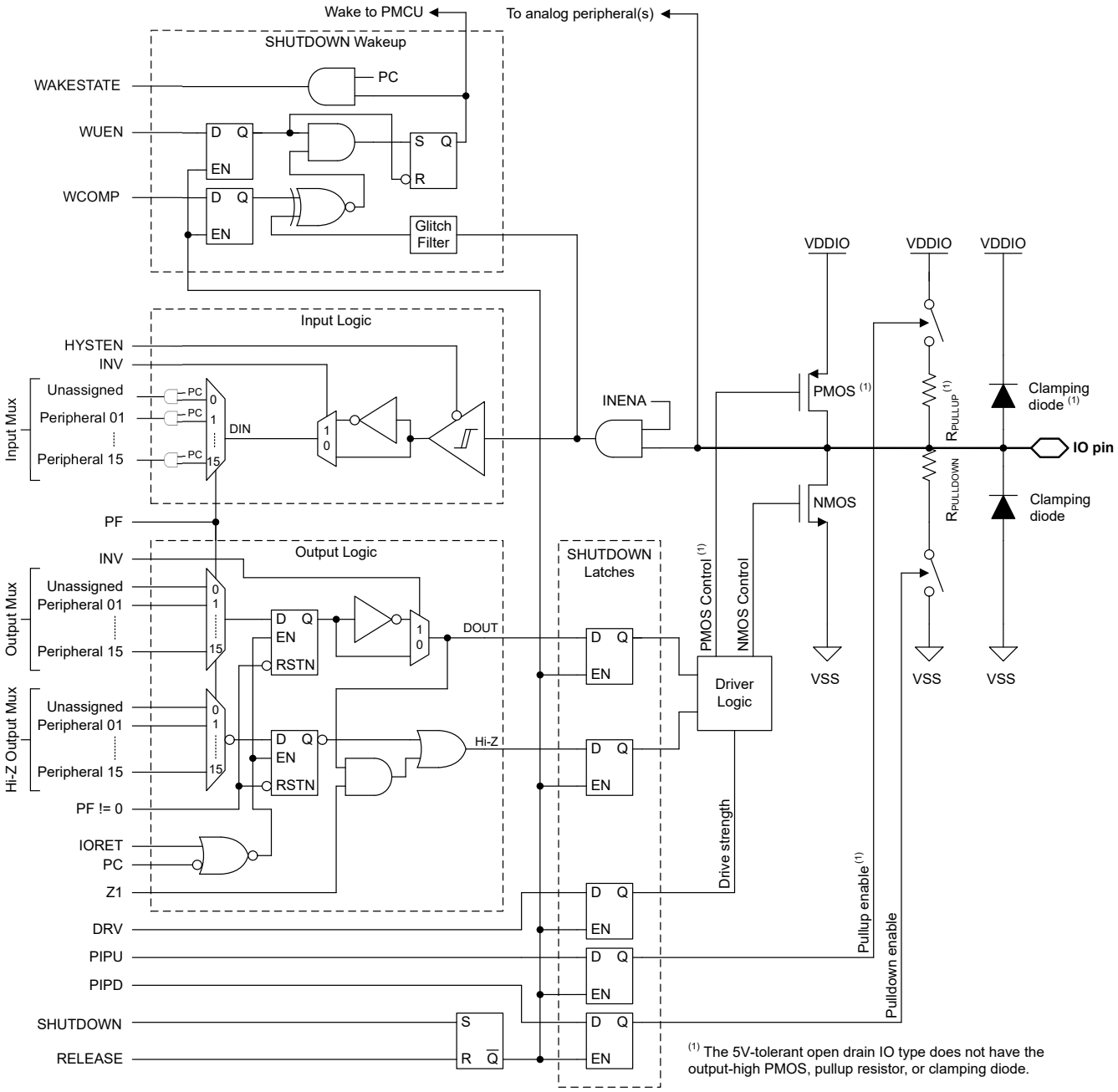


Figure 8-3. Superset Input/Output Diagram

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8.33 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device.

Table 8-14. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

For a complete description of the debug functionality offered on MSPM0 devices, see the Debug chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.34 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BSLSDA signals (for I^2C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-15. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSLRX	Required for UART	UART receive signal (RXD), an input
BSLTX	Required for UART	UART transmit signal (TXD) an output
BSLSCL	Required for I2C	I^2C BSL clock signal (SCL)
BSLSDA	Required for I2C	I^2C BSL data signal (SDA)
BSL_invoke	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the MSPM0 boot strap loader user's guide.

8.35 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please

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refer to Factory Constants chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual* for more information.

Table 8-16. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER
MSPM0L1227, MSPM0L2227	0xBB9F	0x17
MSPM0L1228, MSPM0L2228	0xBB9F	0x17

Table 8-17. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	Part	Variant
M0L1227QRGERQ1	0xDDE7	0x1B
M0L1227QRHBRQ1	0xDDE7	0xF2
M0L1227QRGZRQ1	0xDDE7	0x86
M0L1227QPTRQ1	0xDDE7	0x78
M0L1227QPMRQ1	0xDDE7	0x2
M0L1227QPNRQ1	0xDDE7	0xD1
M0L1228QRGERQ1	0xB371	0x50
M0L1228QRHBRQ1	0xB371	0x9C
M0L1228QRGZRQ1	0xB371	0x19
M0L1228QPTRQ1	0xB371	0xF1
M0L1228QPMRQ1	0xB371	0xE9
M0L1228QPNRQ1	0xB371	0xB2
M0L2227QPTRQ1	0x6BC	0xD1
M0L2227QPMRQ1	0x6BC	0x87
M0L2227QPNRQ1	0x6BC	0xFF
M0L2228QPTRQ1	0xBE7B	0x3E
M0L2228QPMRQ1	0xBE7B	0xFD
M0L2228QPNRQ1	0xBE7B	0xFC

8.36 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to the Factory Constants chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual* for more information.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4).

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9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10µF and a 0.1µF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

The NRST reset pin is required to connect an external 47kΩ pullup resistor with a 10nF pulldown capacitor.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100kΩ resistor, populated between the ROSC pin and VSS, to stabilize the SYSOSC frequency by providing a precision reference current for the SYSOSC. This resistor needs to be 0.1% accurate and is not required if the SYSOSC FCL is not enabled.

For devices supporting external crystals, external bypass capacitors for the crystal oscillator pins are required. Refer to *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual* which explains how to calculate the capacitor value.

A 0.47µF tank capacitor is required for the VCORE pin and needs to be placed close to the device with minimum distance to the device ground.

For 5V-tolerant open drain IOs (ODIO), a pullup resistor is required to output a logic high signal. This is required for I^2C and UART functions if the ODIO are used.

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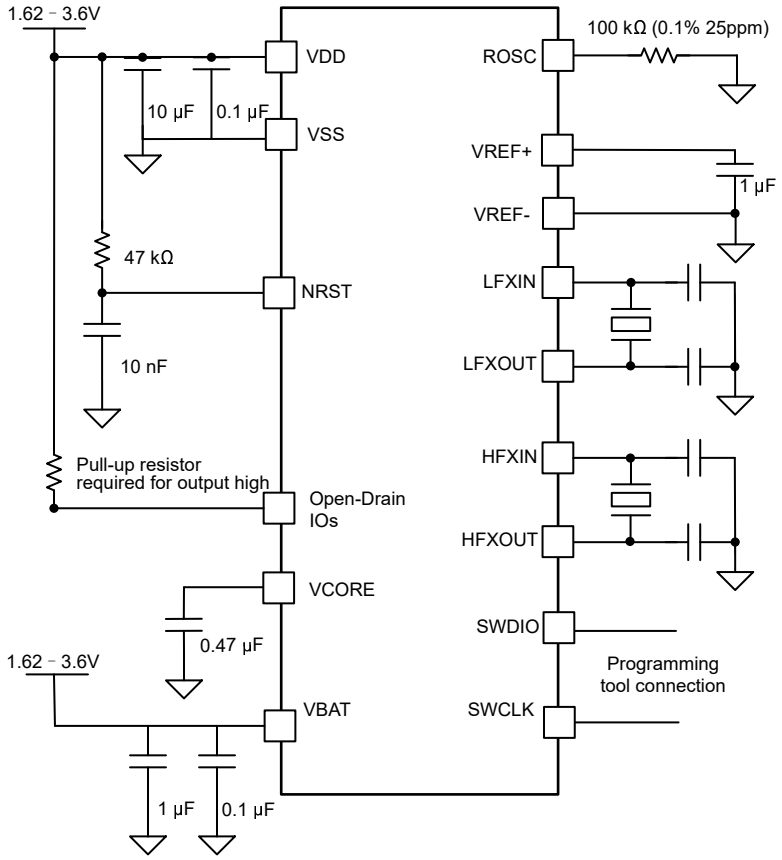


Figure 9-1. Typical Application Schematic

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M0+ MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

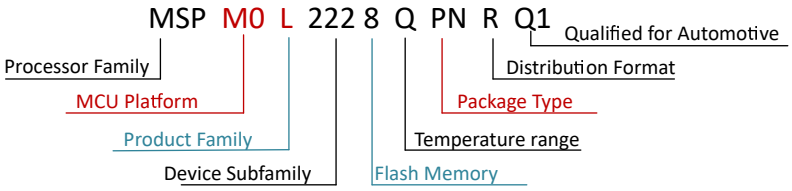


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M0 = Arm based 32-bit M0+
Product Family	L = 32MHz frequency
Device Subfamily	1227 = ADC, CMP, VBAT 222x = ADC, CMP, VBAT, LCD
Flash Memory	7 = 128KB 8 = 256KB
Temperature Range	Q = –40°C to 125°C, AEC-Q100 qualified
Package Type	See the *Device Comparison* section and https://www.ti.com/packaging
Distribution Format	R = Large reel No marking = Tube or tray

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For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0L2228	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/EnergyTrace. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Cloud Tools	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™ (CCS)	Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.
IAR Embedded Workbench® IDE	
Keil® MDK IDE	
GNU Arm Embedded Toolchain	

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 L-Series 32MHz Microcontrollers	This manual describes the modules and peripherals of the family of devices. Each description presents the module or peripheral in a general sense. Not all features

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Technical Reference Manual	and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

LaunchPad™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 20, 2024 to November 30, 2024 (from Revision * (May 2024) to Revision A (November2024)) **Page**

- Added column to specifiy number of communications interfaces for each part number ... 6
- Removed unavailable OPNs ... 6
- Corrected pin attributes and descriptions ... 7
- Added VBAT specifications for SHUTDOWN mode ... 46
- Updated NWEC specification name to reflect what type of endurance is being defined ... 48
- Changed specification to reflect that the user can choose up to 32 sectors from any area of the flash ... 48
- Updated endurance specification units to indicate number of cycles per sector ... 48
- Updated NWEC specification name to reflect what type of endurance is being defined ... 48
- Updated endurance specification units to indicate number of cycles per sector ... 48
- Updated current from 75uA to 100uA ... 51
- Updated spec from 460uA to 570uA, and removed max spec ... 54
- Changed sample-and-hold capacitance from 3.3pF to 4.3pF ... 54
- Changed DC PSRR from 60 to 68 ... 54
- Changed AC PSRR from 49 to 55 ... 54
- Removed I2C PD0 test condition because I2C is only in PD0 ... 61
- Split out register base addresses for TIO and SPM, and made corrections to the sizes ... 73
- Added "Support for custom polynomials" to CRC feature list ... 81

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

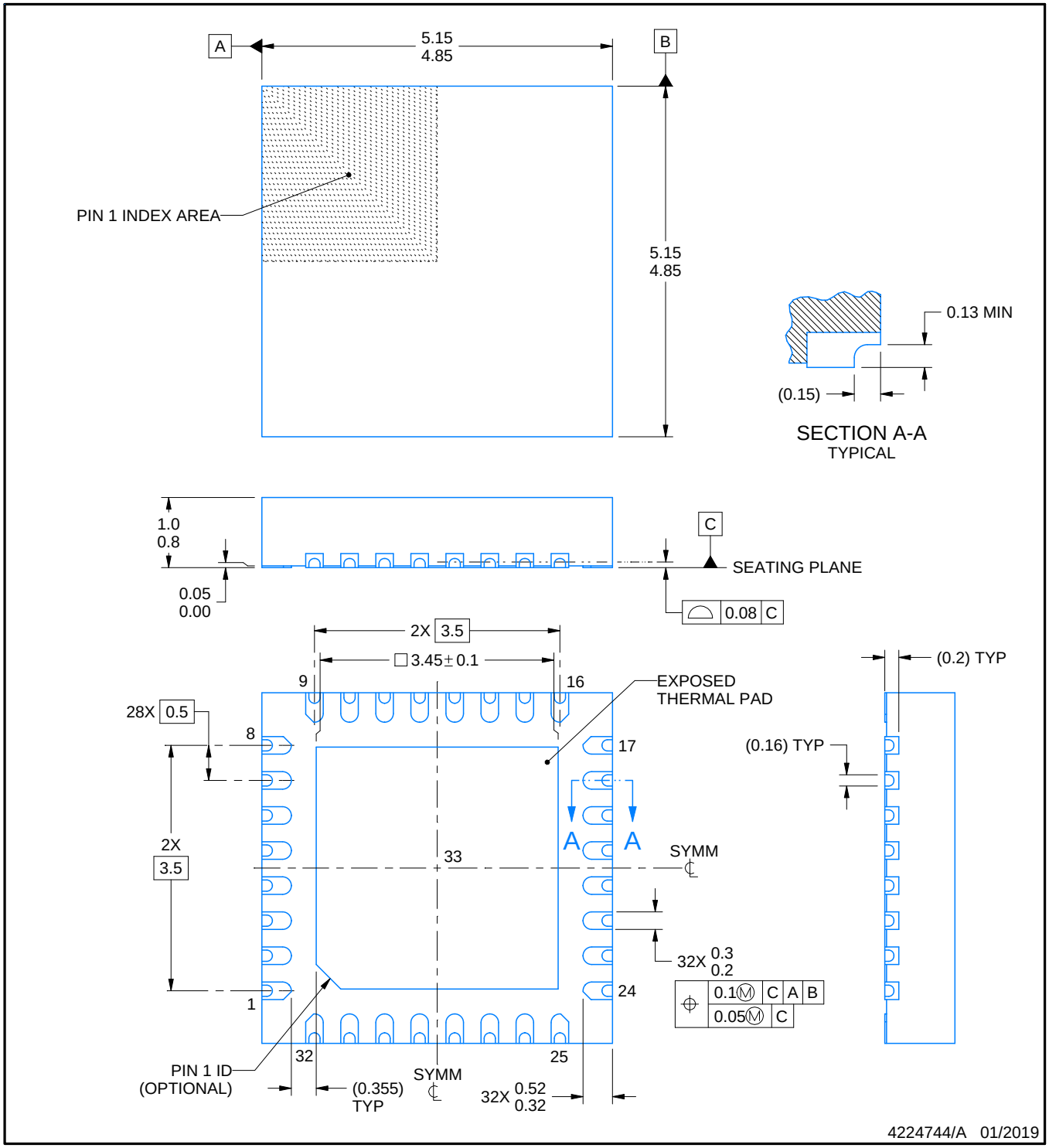
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RHB0032T

PACKAGE OUTLINE

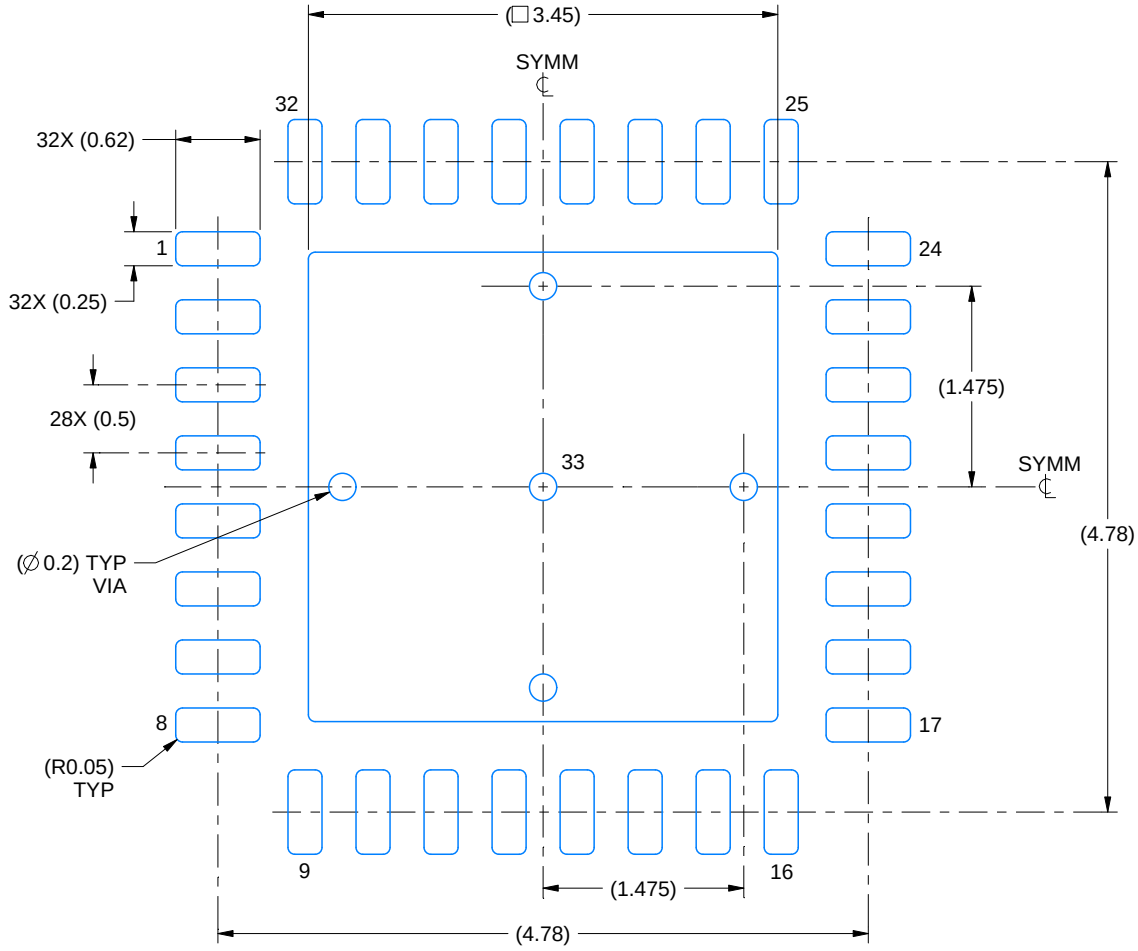
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

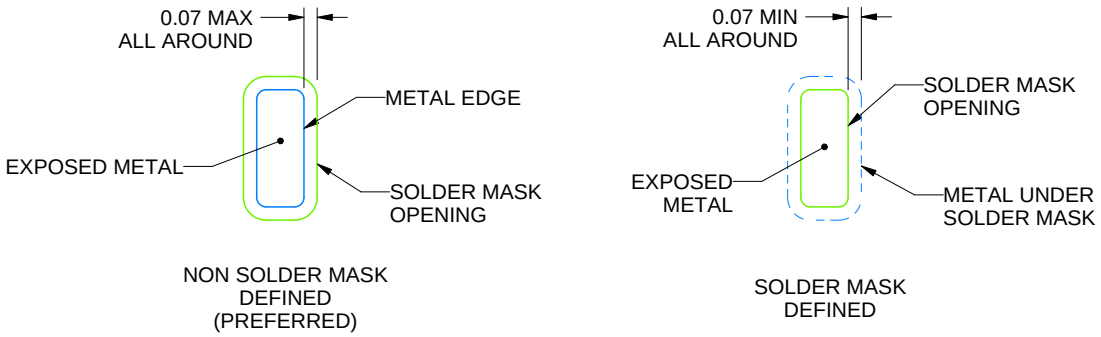
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:18X

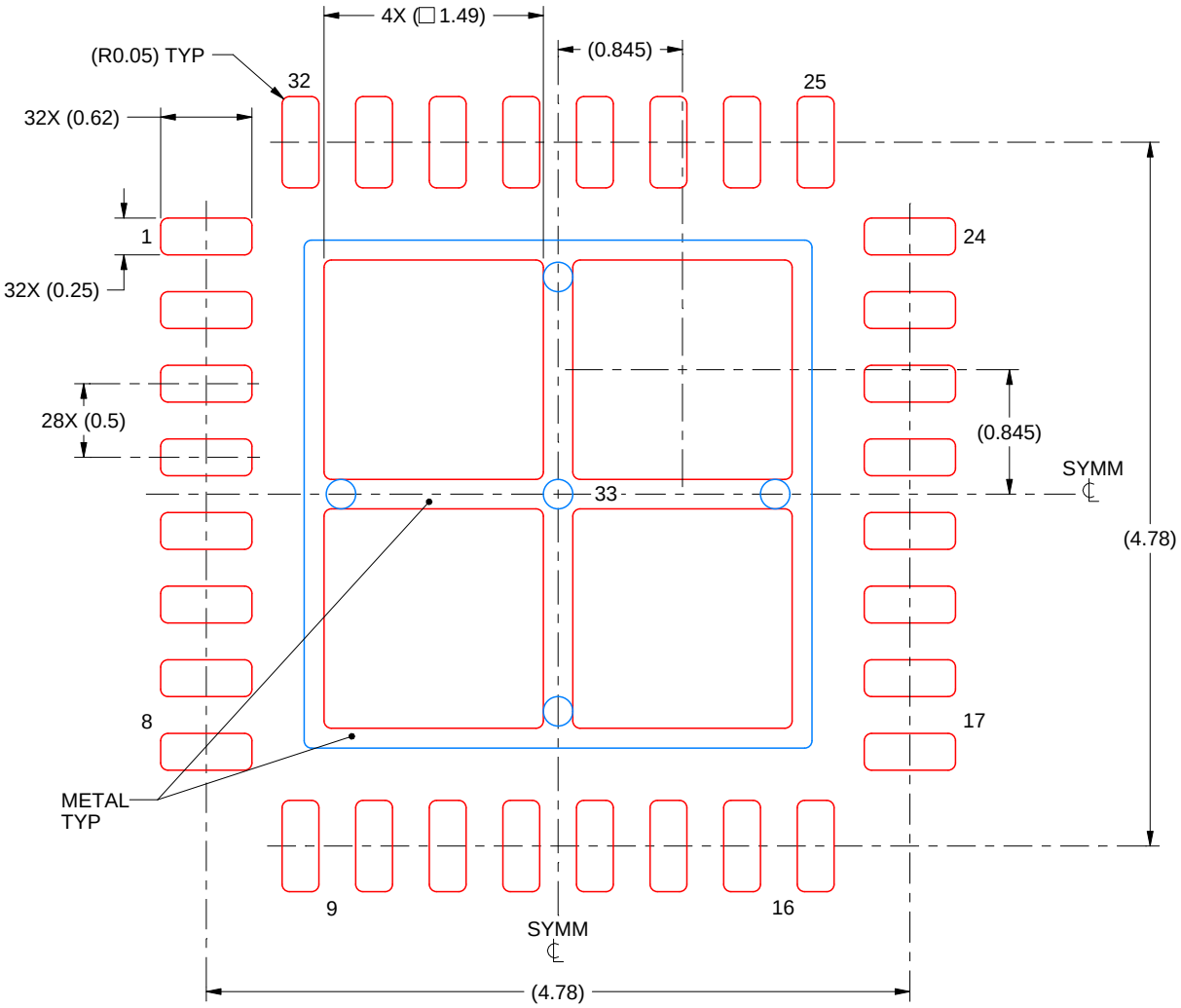


SOLDER MASK DETAILS

4224744/A 01/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224744/A 01/2019

NOTES: (continued)

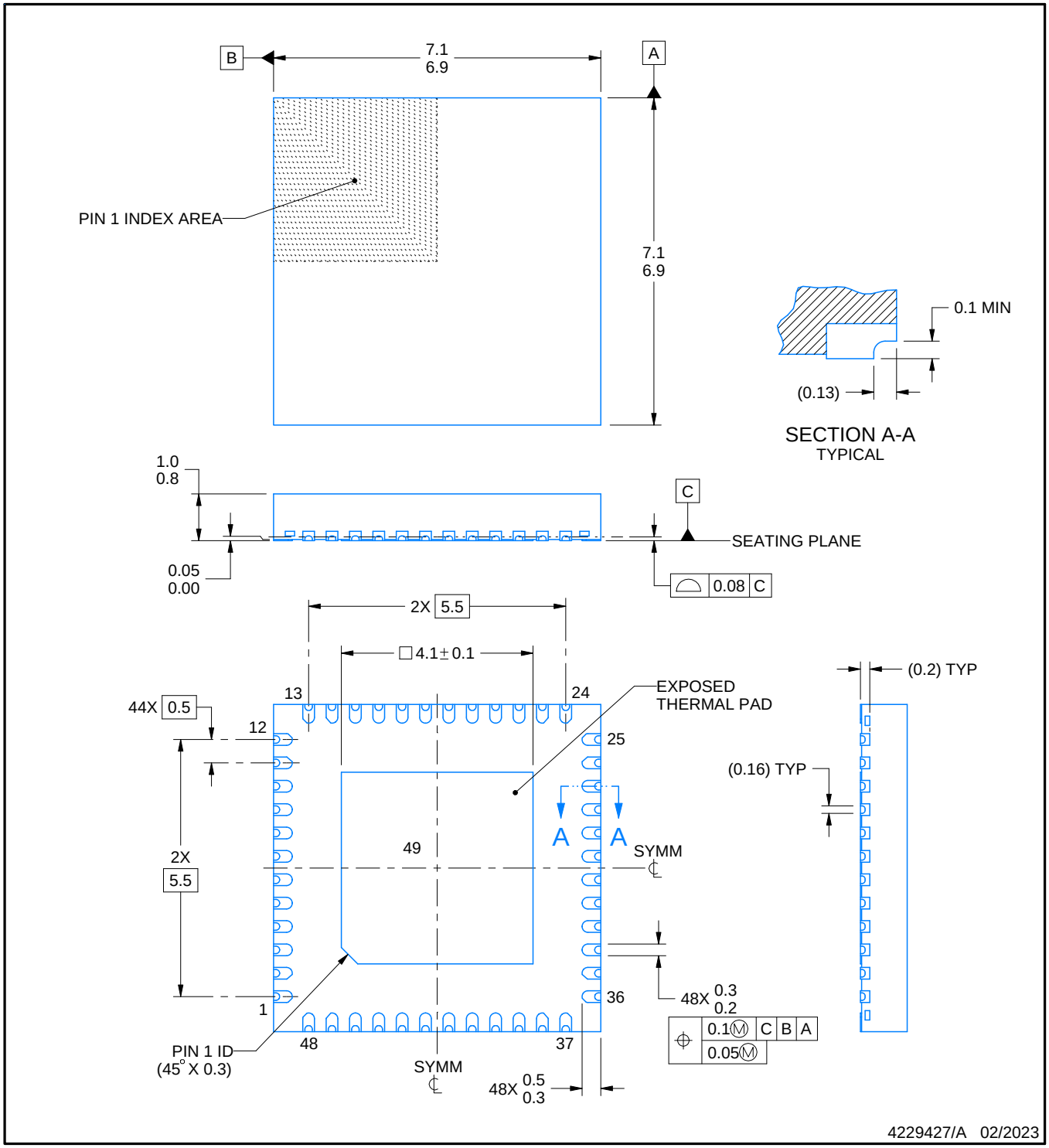
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGZ0048F

PACKAGE OUTLINE

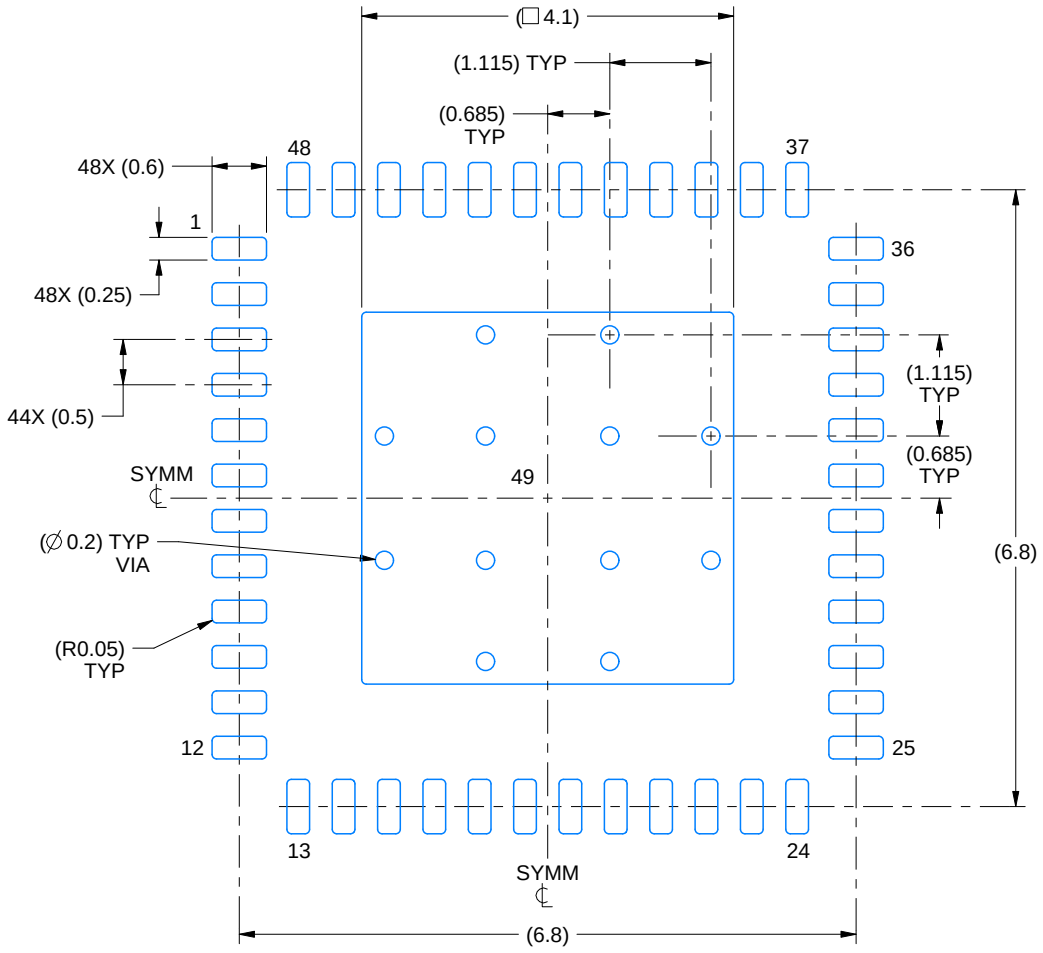
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

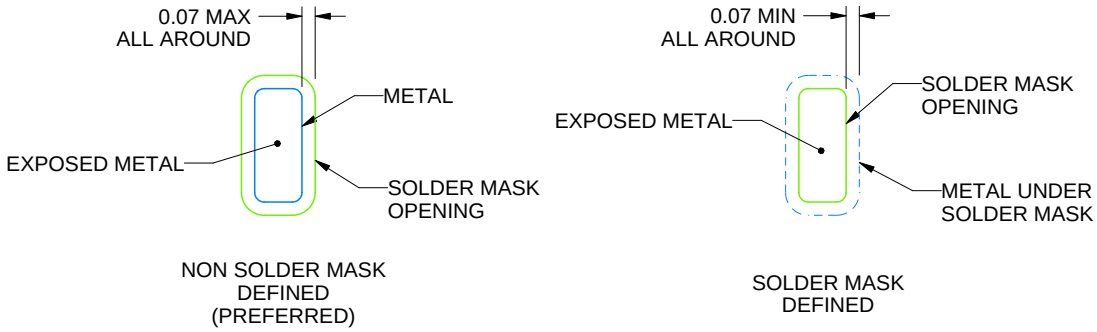


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

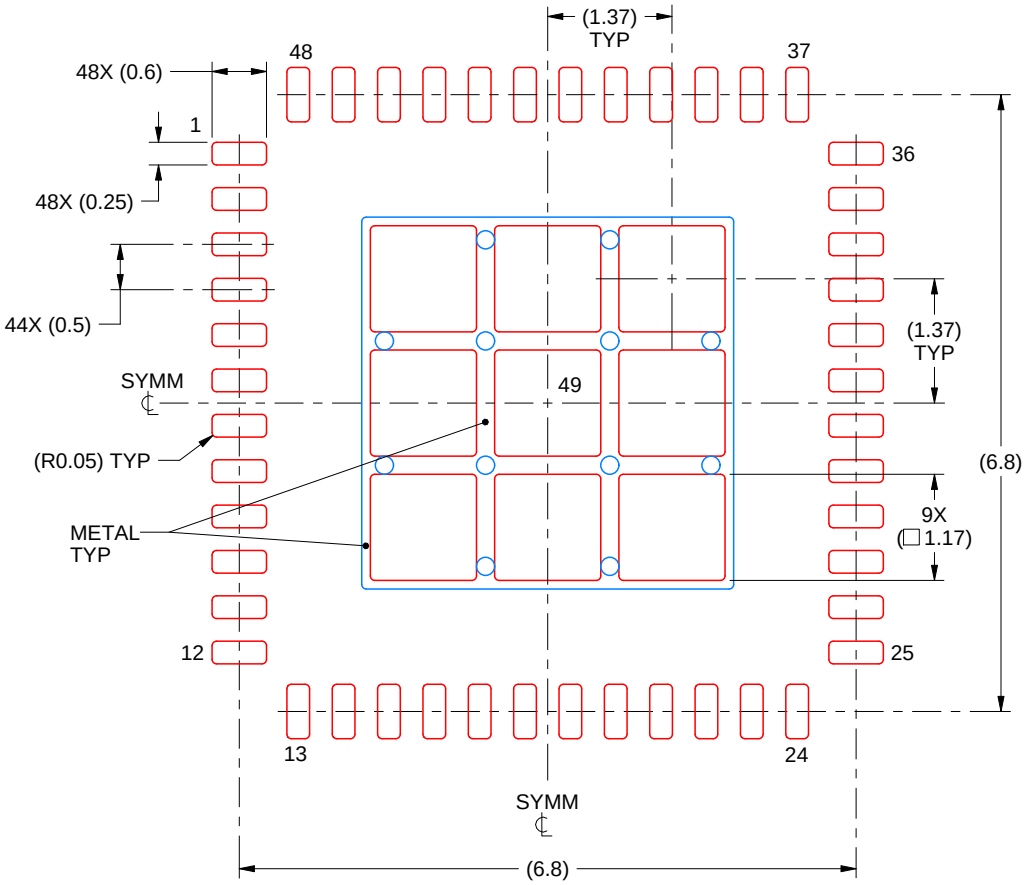


SOLDER MASK DETAILS

4229427/A 02/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



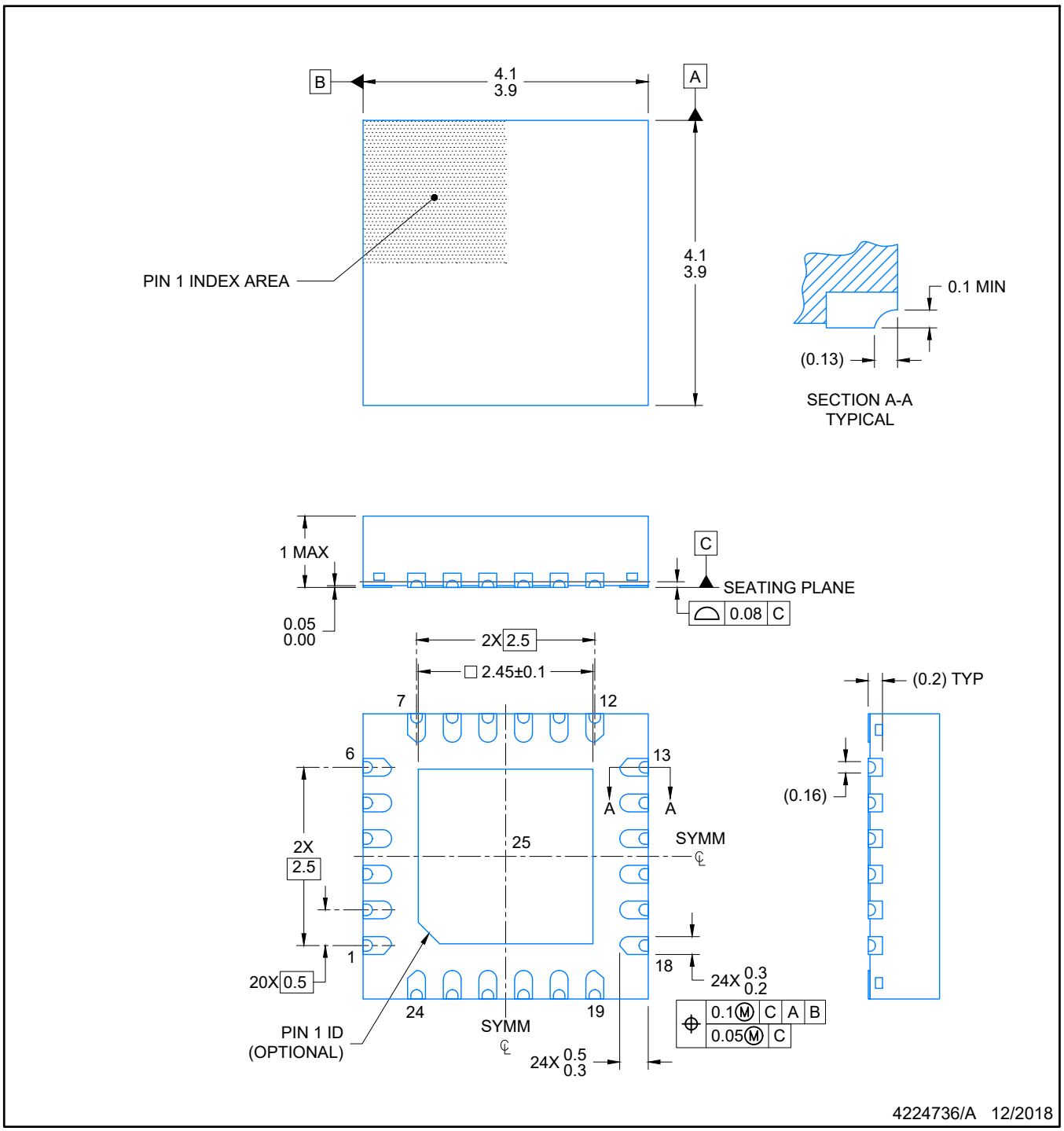
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4229427/A 02/2023

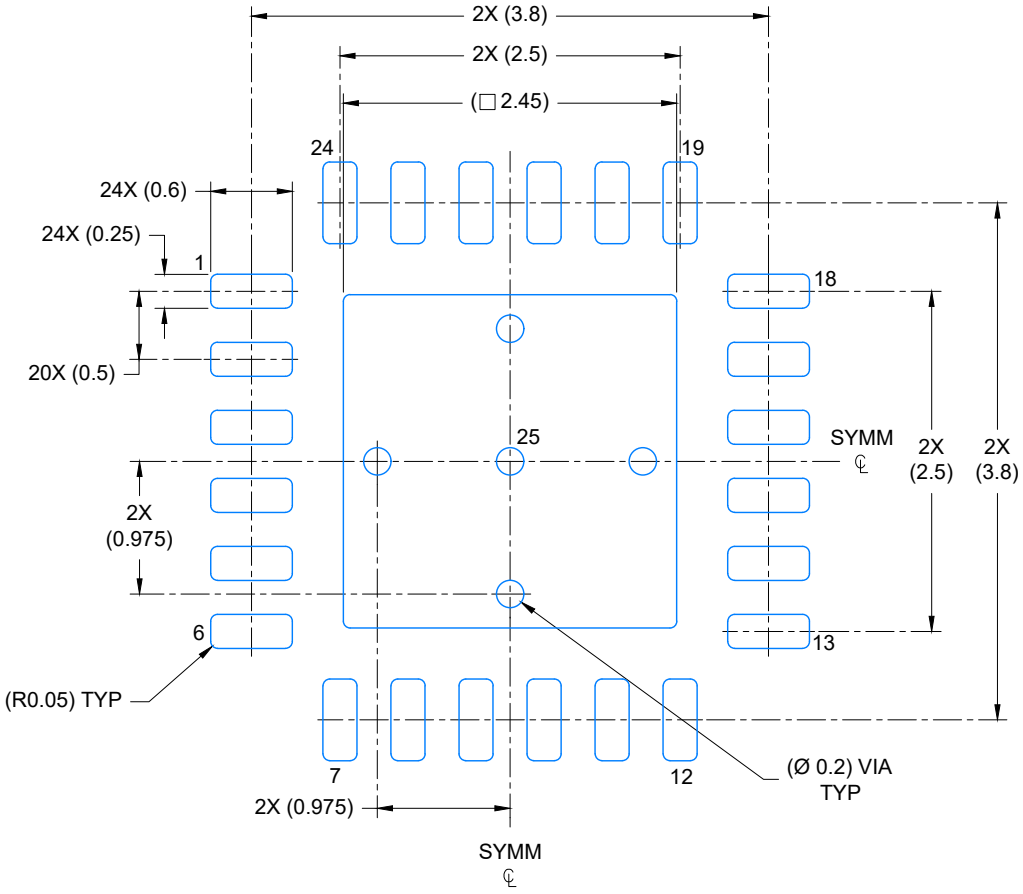
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

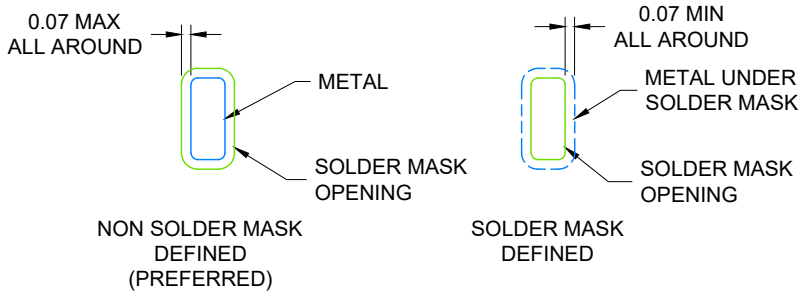


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

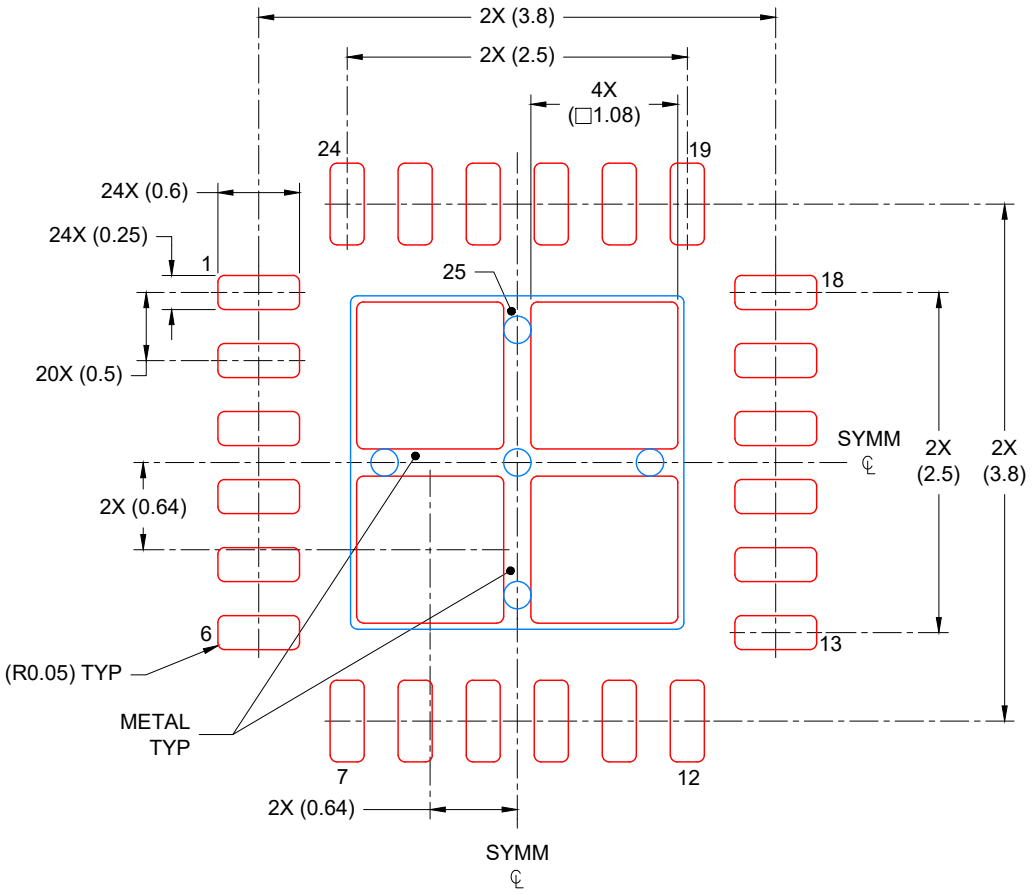


SOLDER MASK DETAILS

4224736/A 12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

4224736/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M0L1227QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1227Q
M0L1227QPMRQ1.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1227Q
M0L1227QPMRQ1.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1227Q
M0L1227QPNRQ1	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L1227Q
M0L1227QPNRQ1.A	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L1227Q
M0L1227QPNRQ1.B	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L1227Q
M0L1227QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1227Q
M0L1227QPTRQ1.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1227Q
M0L1227QPTRQ1.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1227Q
M0L1227QRGERQ1	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRGERQ1.A	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRGERQ1.B	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRGZRQ1	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRGZRQ1.A	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRGZRQ1.B	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRHBRQ1.A	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1227QRHBRQ1.B	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1227Q
M0L1228QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1228Q
M0L1228QPMRQ1.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1228Q
M0L1228QPMRQ1.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1228Q
M0L1228QPNRQ1	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L1228Q

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M0L1228QPNRQ1.A	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L1228Q
M0L1228QPNRQ1.B	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L1228Q
M0L1228QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1228Q
M0L1228QPTRQ1.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1228Q
M0L1228QPTRQ1.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1228Q
M0L1228QRGERQ1	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRGERQ1.A	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRGERQ1.B	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRGZRQ1	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRGZRQ1.A	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRGZRQ1.B	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRHBRQ1.A	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L1228QRHBRQ1.B	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1228Q
M0L2227QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2227Q
M0L2227QPMRQ1.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2227Q
M0L2227QPMRQ1.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2227Q
M0L2227QPNRQ1	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L2227Q
M0L2227QPNRQ1.A	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L2227Q
M0L2227QPNRQ1.B	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L2227Q
M0L2227QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2227Q
M0L2227QPTRQ1.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2227Q
M0L2227QPTRQ1.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2227Q
M0L2228QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2228Q

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M0L2228QPMRQ1.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2228Q
M0L2228QPMRQ1.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2228Q
M0L2228QPNRQ1	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L2228Q
M0L2228QPNRQ1.A	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L2228Q
M0L2228QPNRQ1.B	Active	Production	LQFP (PN) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	M0L2228Q
M0L2228QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2228Q
M0L2228QPTRQ1.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2228Q
M0L2228QPTRQ1.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L2228Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSPM0L1227-Q1, MSPM0L1228-Q1, MSPM0L2227-Q1, MSPM0L2228-Q1 :

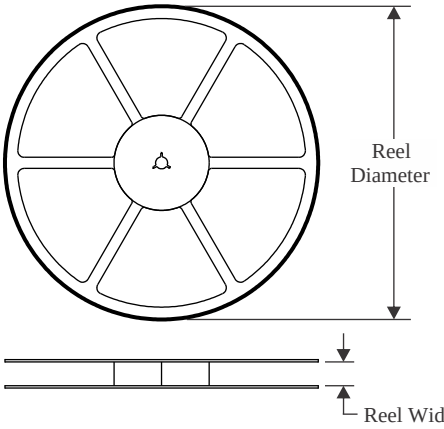
- Catalog : MSPM0L1227, MSPM0L1228, MSPM0L2227, MSPM0L2228

NOTE: Qualified Version Definitions:

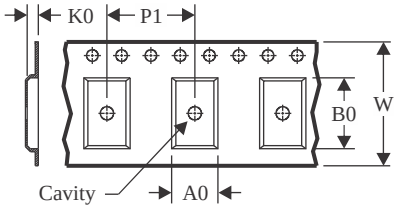
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

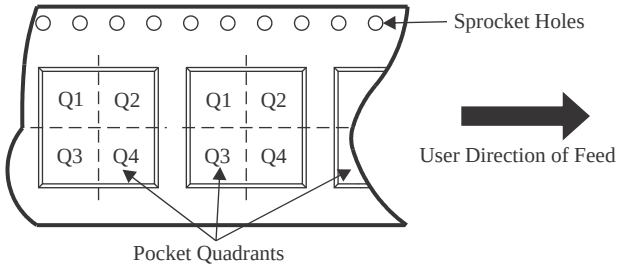


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

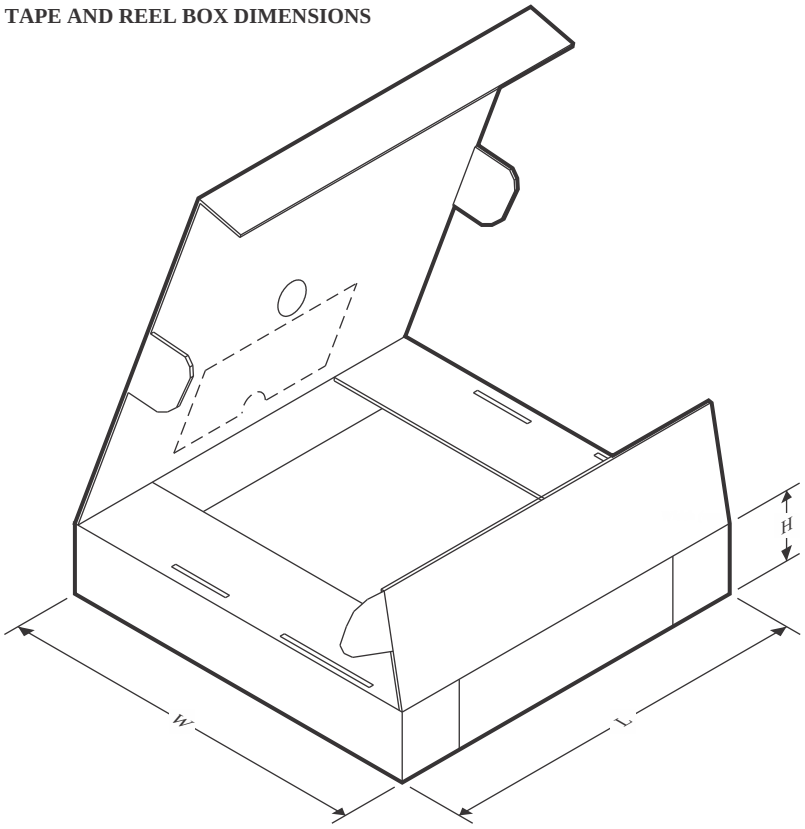


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
M0L1227QPMRQ1	LQFP	PM	64	1000	330.0	24.4	12.5	12.5	2.2	16.0	24.0	Q2
M0L1227QPNRQ1	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
M0L1227QPTRQ1	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
M0L1227QRGERQ1	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
M0L1227QRGZRQ1	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
M0L1227QRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
M0L1228QPMRQ1	LQFP	PM	64	1000	330.0	24.4	12.5	12.5	2.2	16.0	24.0	Q2
M0L1228QPNRQ1	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
M0L1228QPTRQ1	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
M0L1228QRGERQ1	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
M0L1228QRGZRQ1	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
M0L1228QRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
M0L2227QPMRQ1	LQFP	PM	64	1000	330.0	24.4	12.5	12.5	2.2	16.0	24.0	Q2
M0L2227QPNRQ1	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
M0L2227QPTRQ1	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
M0L2228QPMRQ1	LQFP	PM	64	1000	330.0	24.4	12.5	12.5	2.2	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
M0L2228QPNRQ1	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2
M0L2228QPTRQ1	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



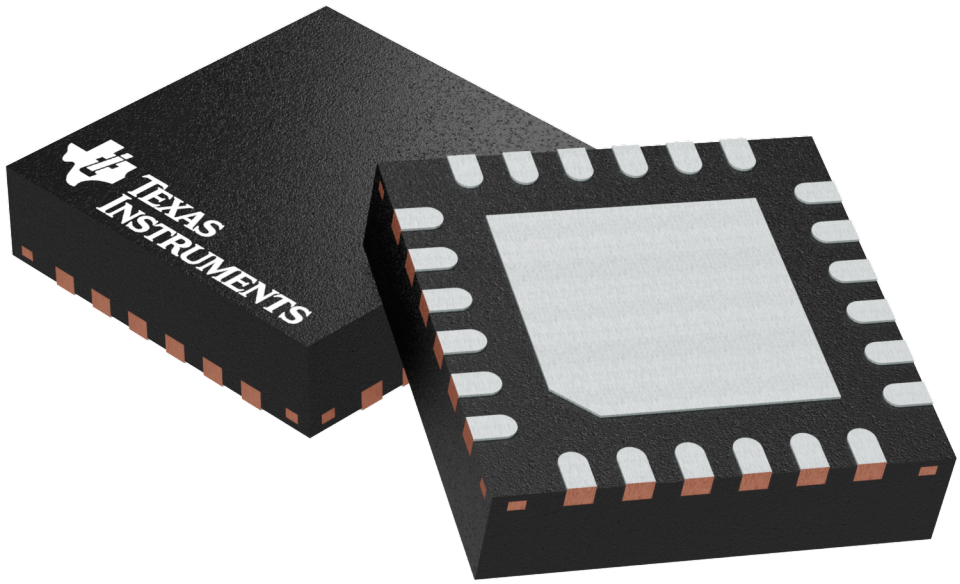
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
M0L1227QPMRQ1	LQFP	PM	64	1000	336.6	336.6	41.3
M0L1227QPNRQ1	LQFP	PN	80	1000	367.0	367.0	55.0
M0L1227QPTRQ1	LQFP	PT	48	1000	336.6	336.6	31.8
M0L1227QRGERQ1	VQFN	RGE	24	5000	367.0	367.0	35.0
M0L1227QRGZRQ1	VQFN	RGZ	48	4000	367.0	367.0	35.0
M0L1227QRHBRQ1	VQFN	RHB	32	5000	367.0	367.0	35.0
M0L1228QPMRQ1	LQFP	PM	64	1000	336.6	336.6	41.3
M0L1228QPNRQ1	LQFP	PN	80	1000	367.0	367.0	55.0
M0L1228QPTRQ1	LQFP	PT	48	1000	336.6	336.6	31.8
M0L1228QRGERQ1	VQFN	RGE	24	5000	367.0	367.0	35.0
M0L1228QRGZRQ1	VQFN	RGZ	48	4000	367.0	367.0	35.0
M0L1228QRHBRQ1	VQFN	RHB	32	5000	367.0	367.0	35.0
M0L2227QPMRQ1	LQFP	PM	64	1000	336.6	336.6	41.3
M0L2227QPNRQ1	LQFP	PN	80	1000	367.0	367.0	55.0
M0L2227QPTRQ1	LQFP	PT	48	1000	336.6	336.6	31.8
M0L2228QPMRQ1	LQFP	PM	64	1000	336.6	336.6	41.3
M0L2228QPNRQ1	LQFP	PN	80	1000	367.0	367.0	55.0
M0L2228QPTRQ1	LQFP	PT	48	1000	336.6	336.6	31.8

GENERIC PACKAGE VIEW

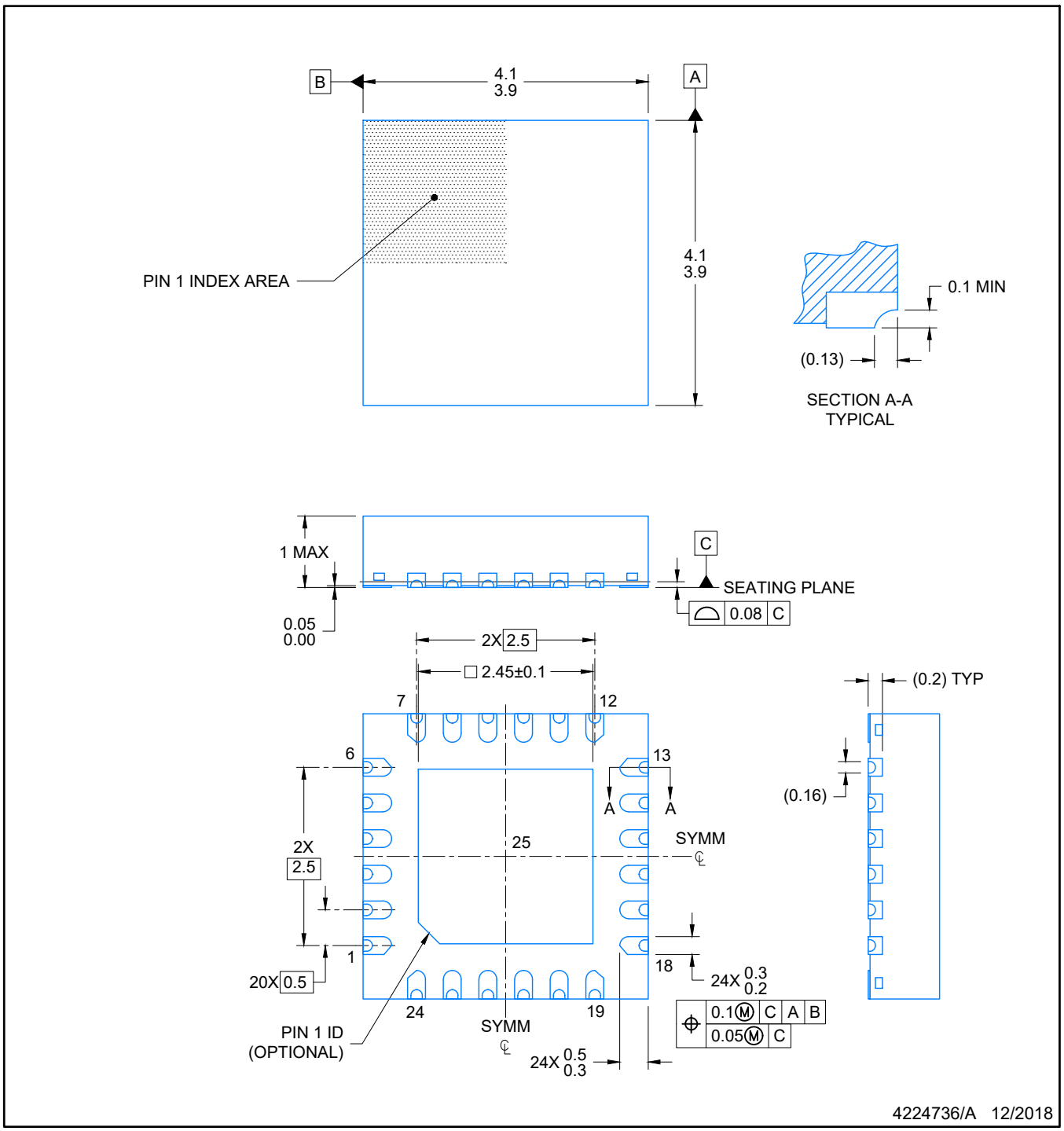
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



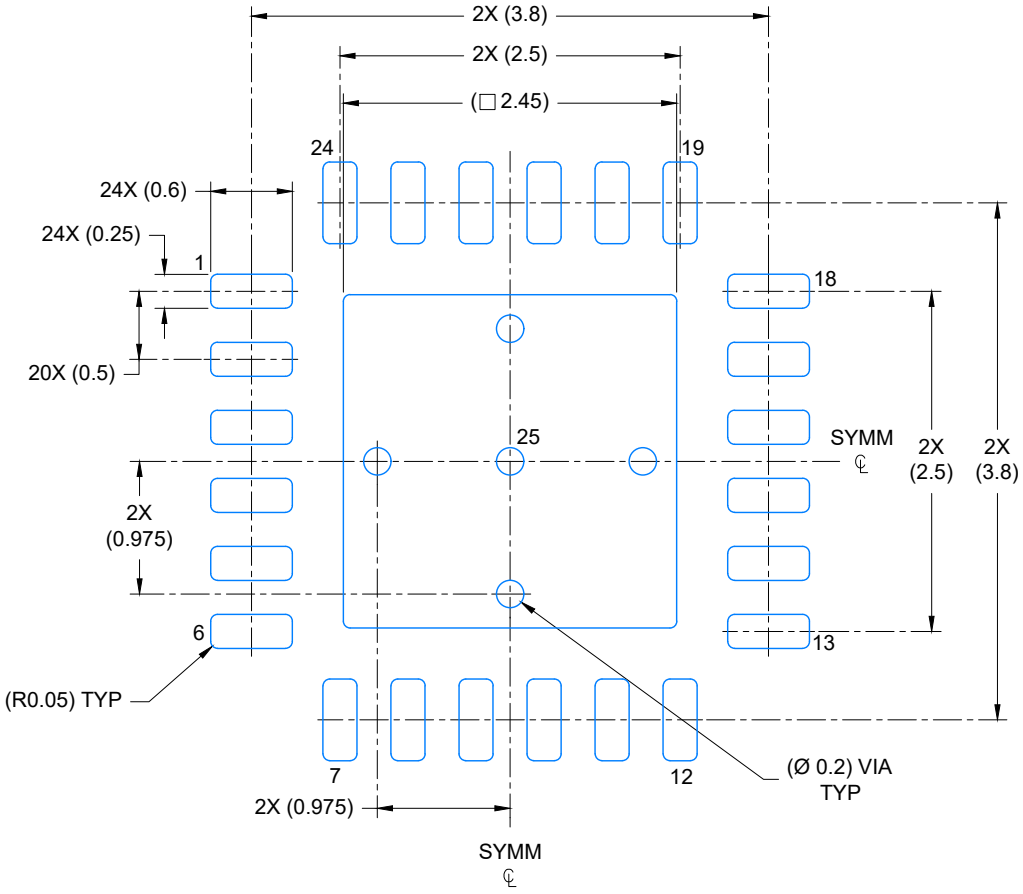
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

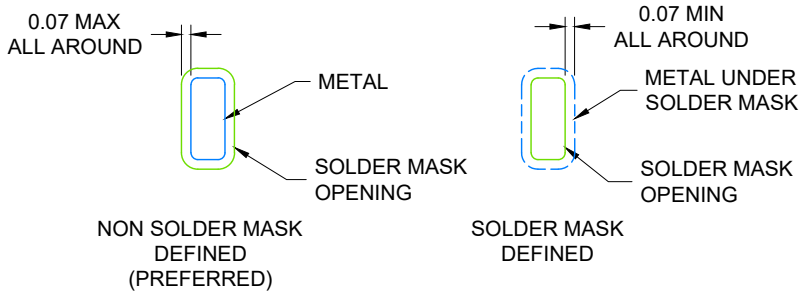


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

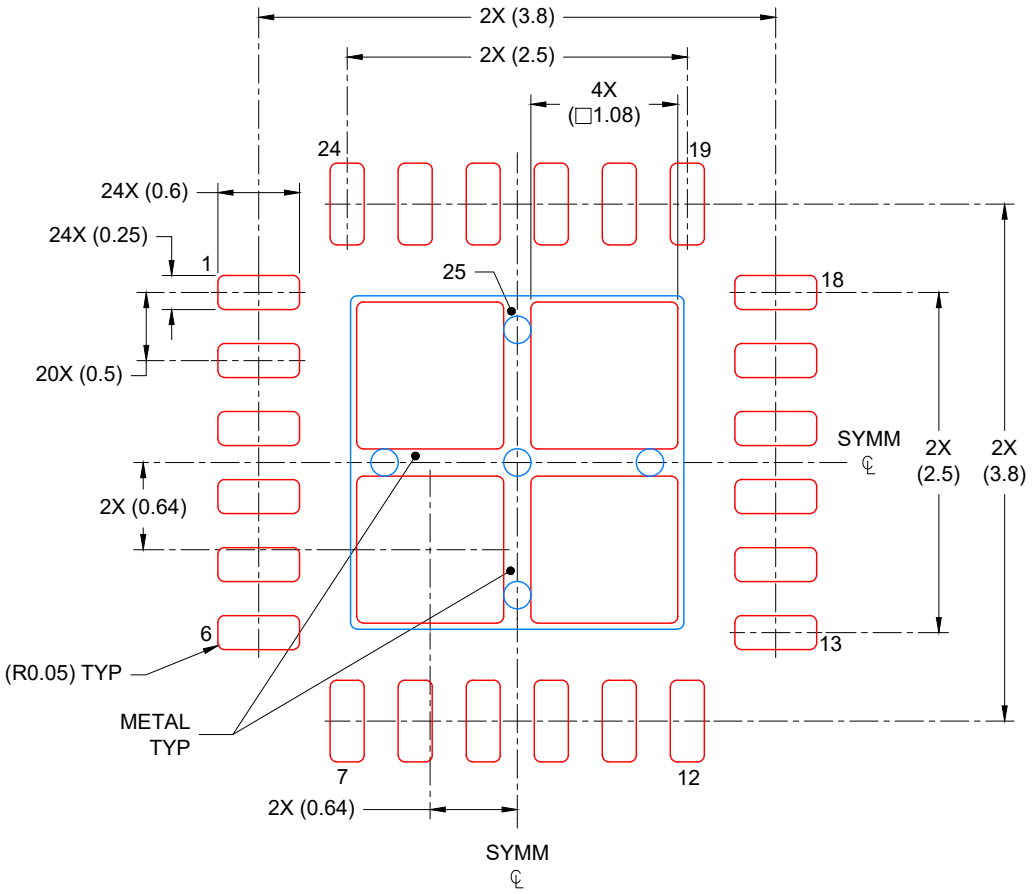


SOLDER MASK DETAILS

4224736/A 12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

4224736/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

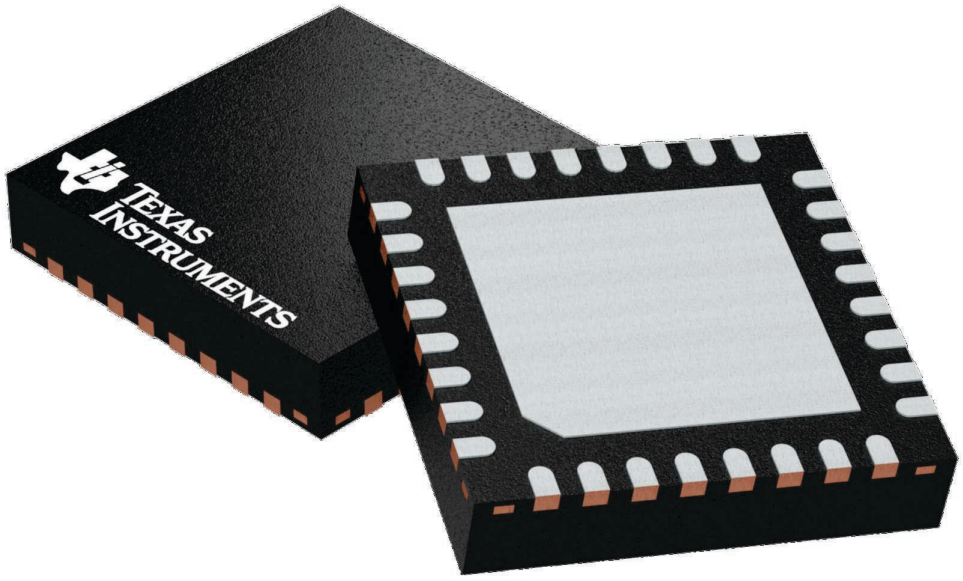
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

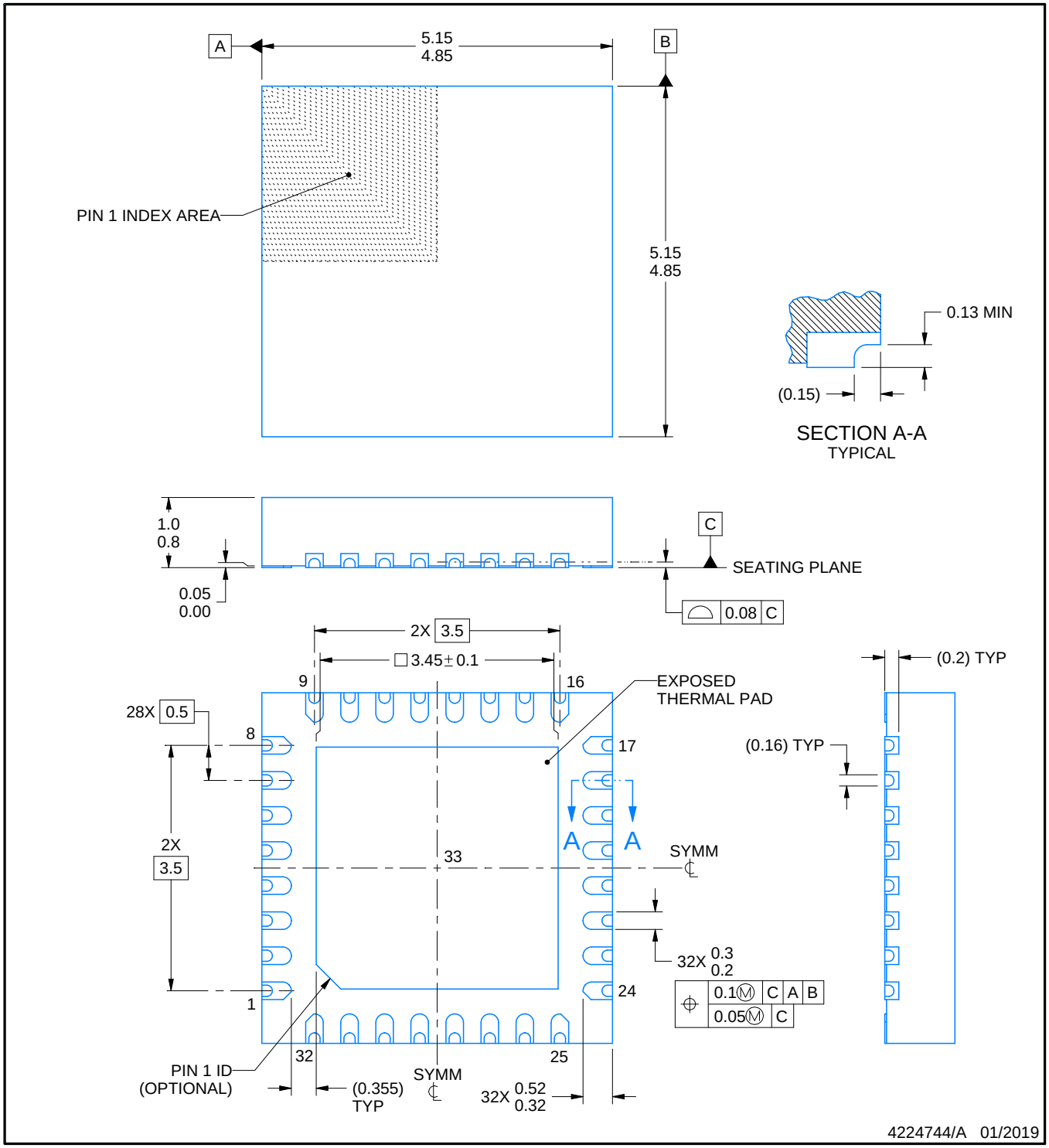
4224745/A

RHB0032T

PACKAGE OUTLINE

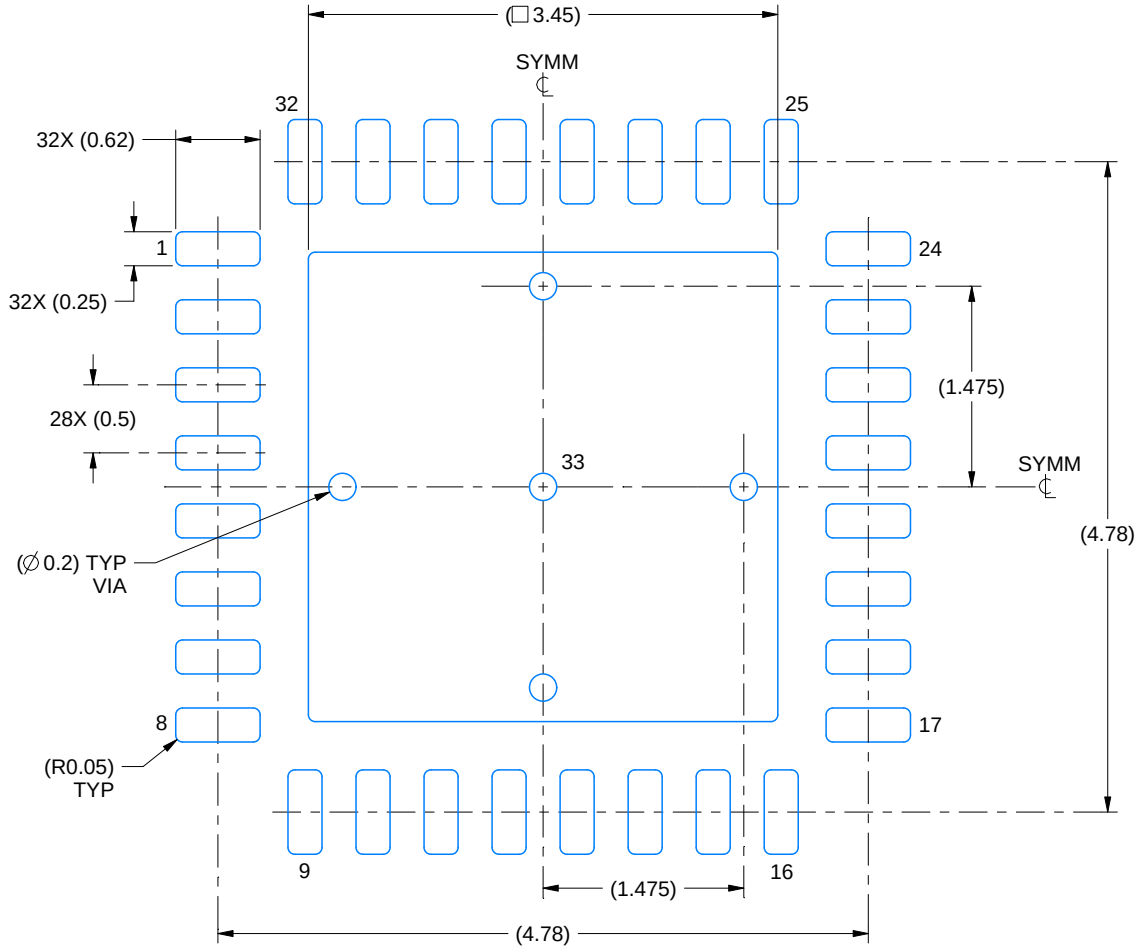
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

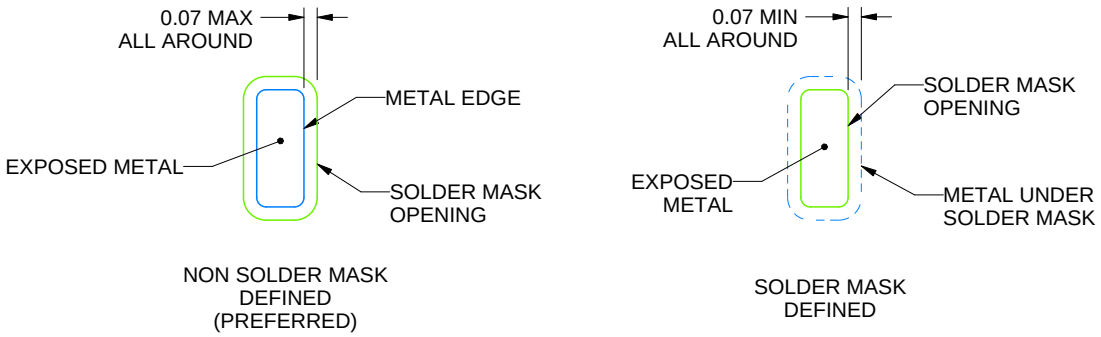
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:18X

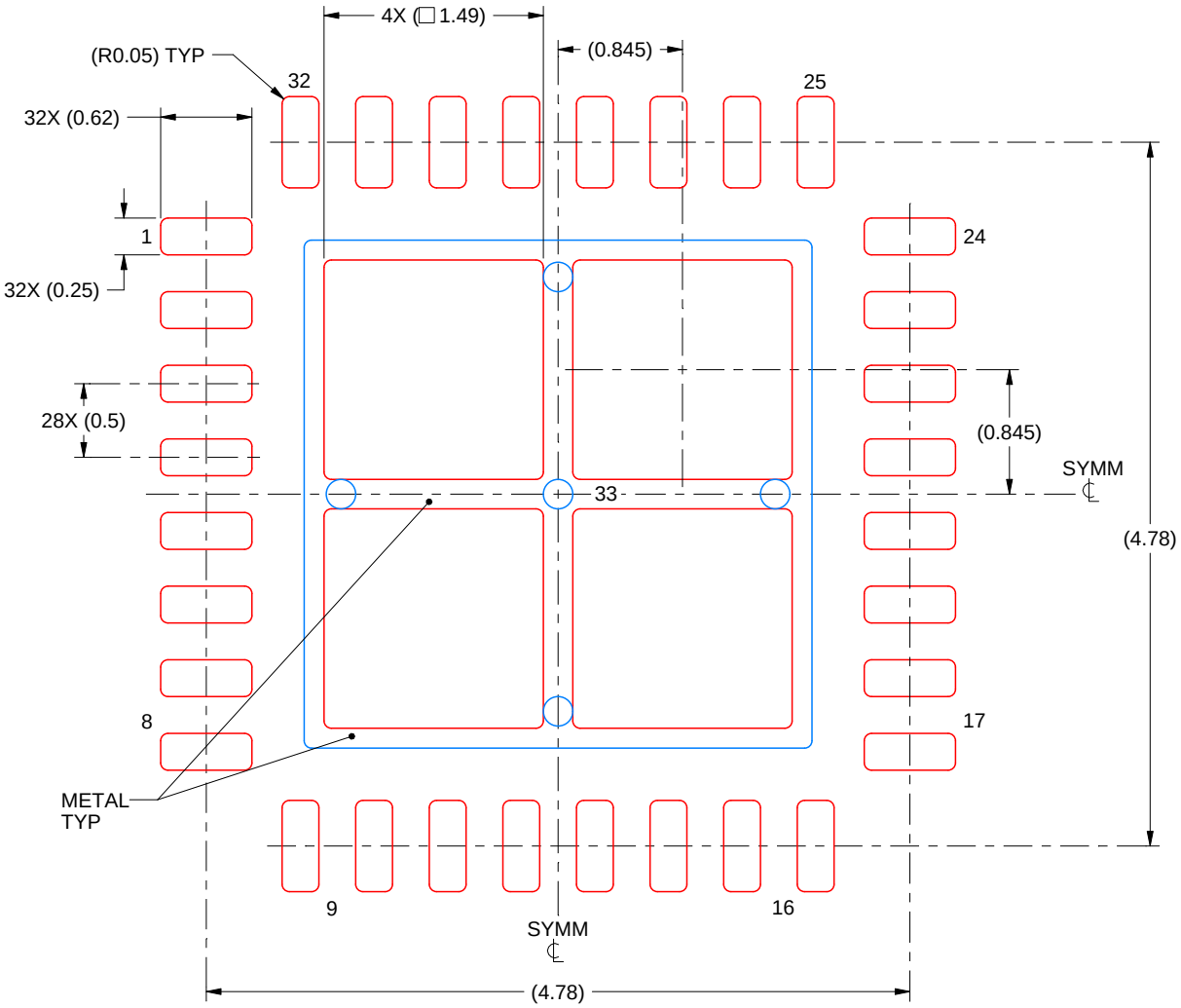


SOLDER MASK DETAILS

4224744/A 01/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224744/A 01/2019

NOTES: (continued)

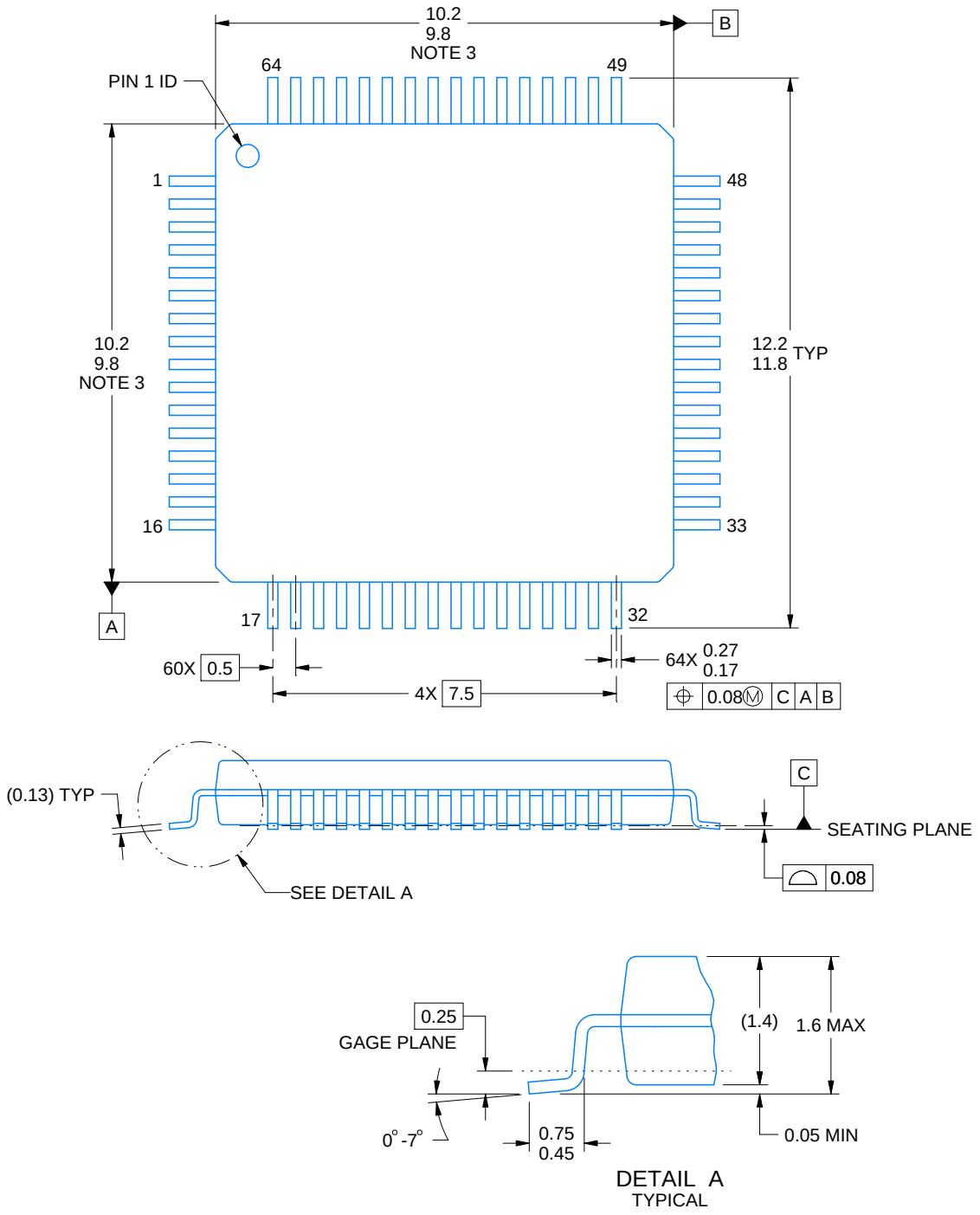
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

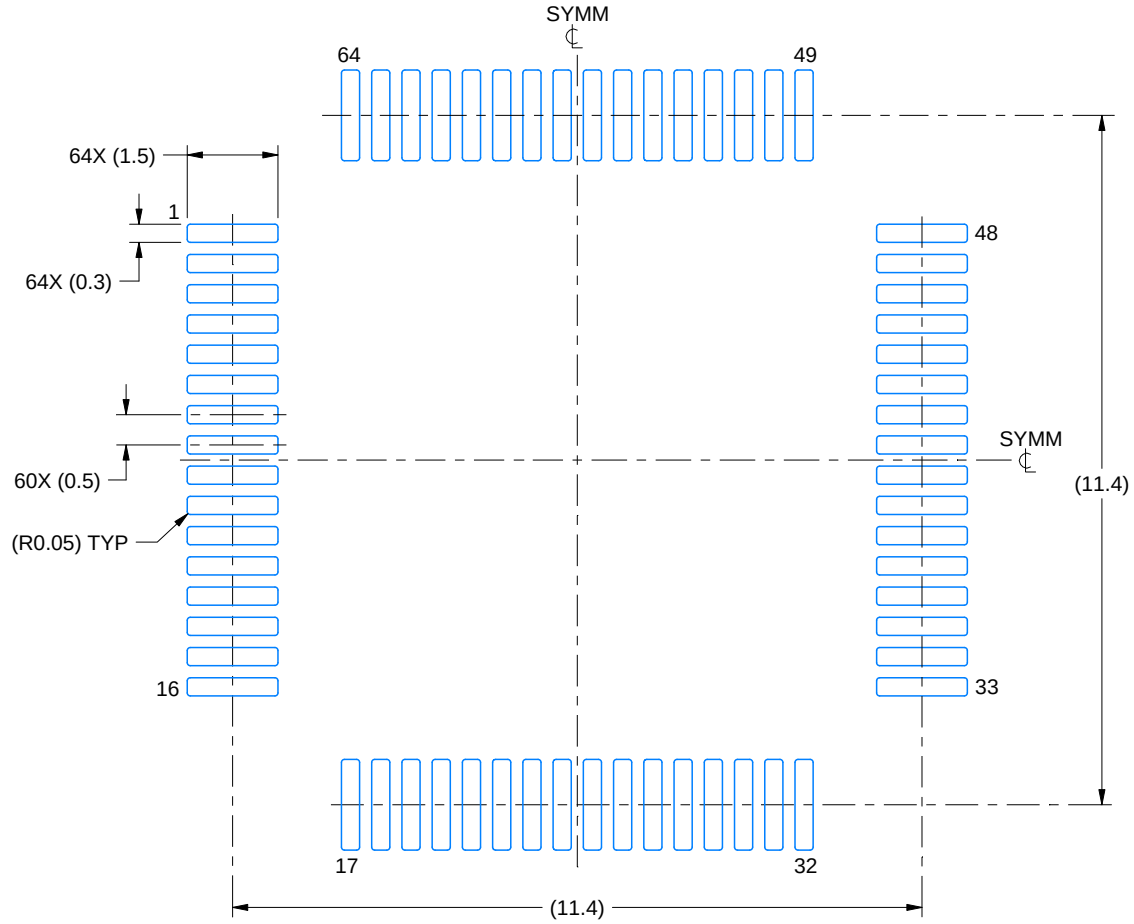
PLASTIC QUAD FLATPACK



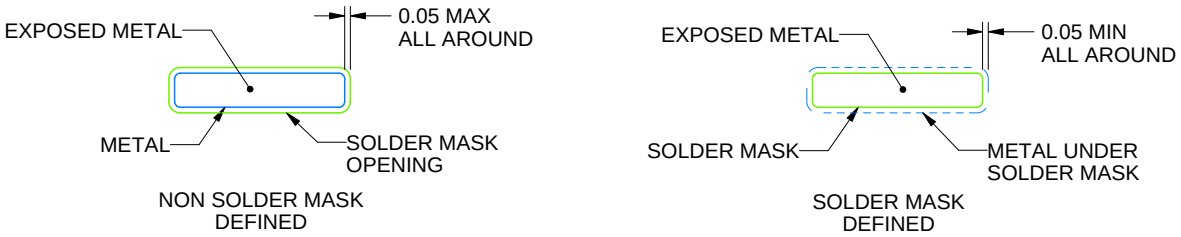
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

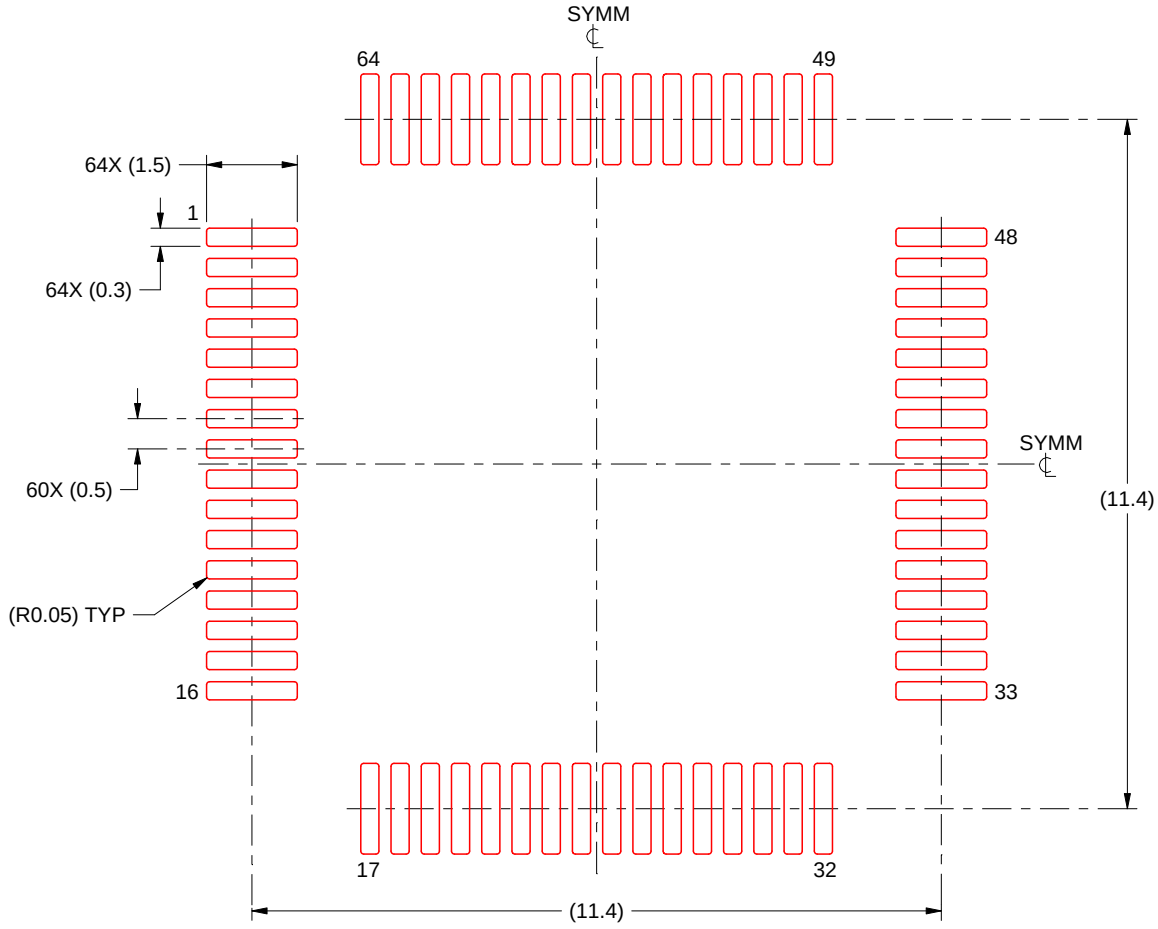


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

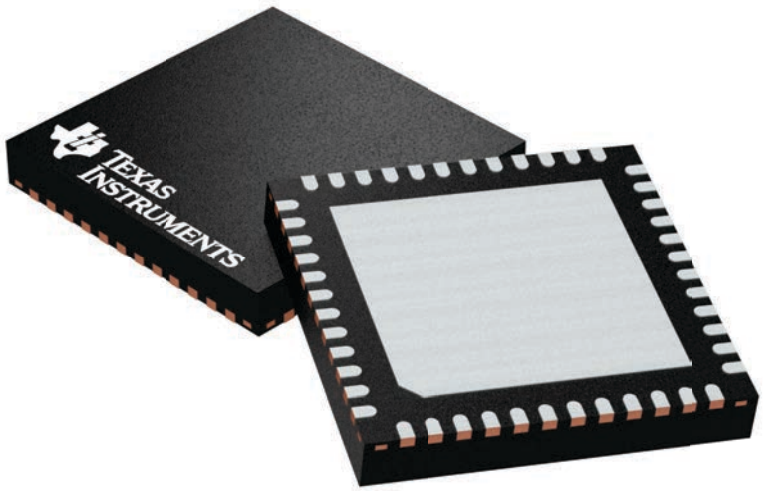
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

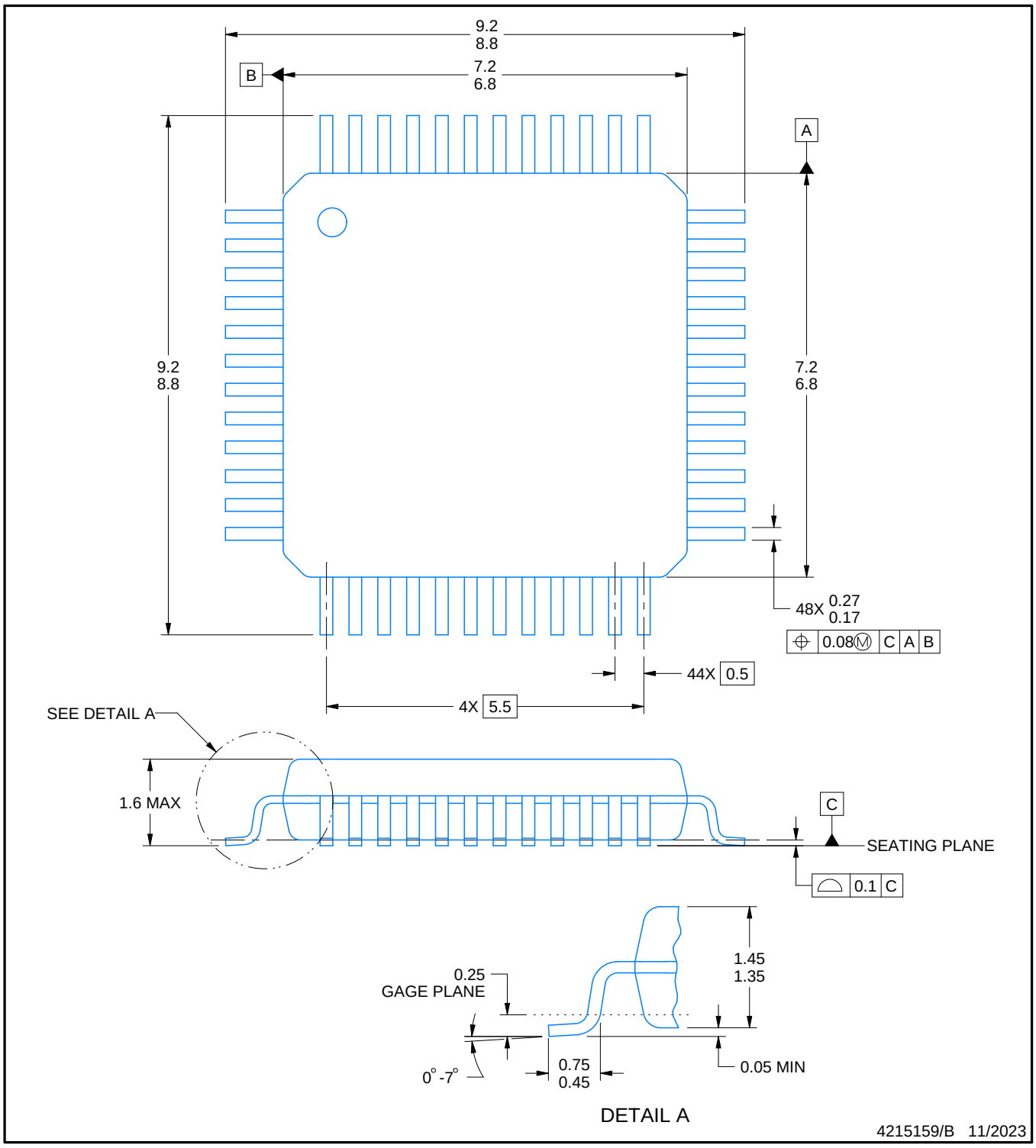
4224671/A

PACKAGE OUTLINE

PT0048A

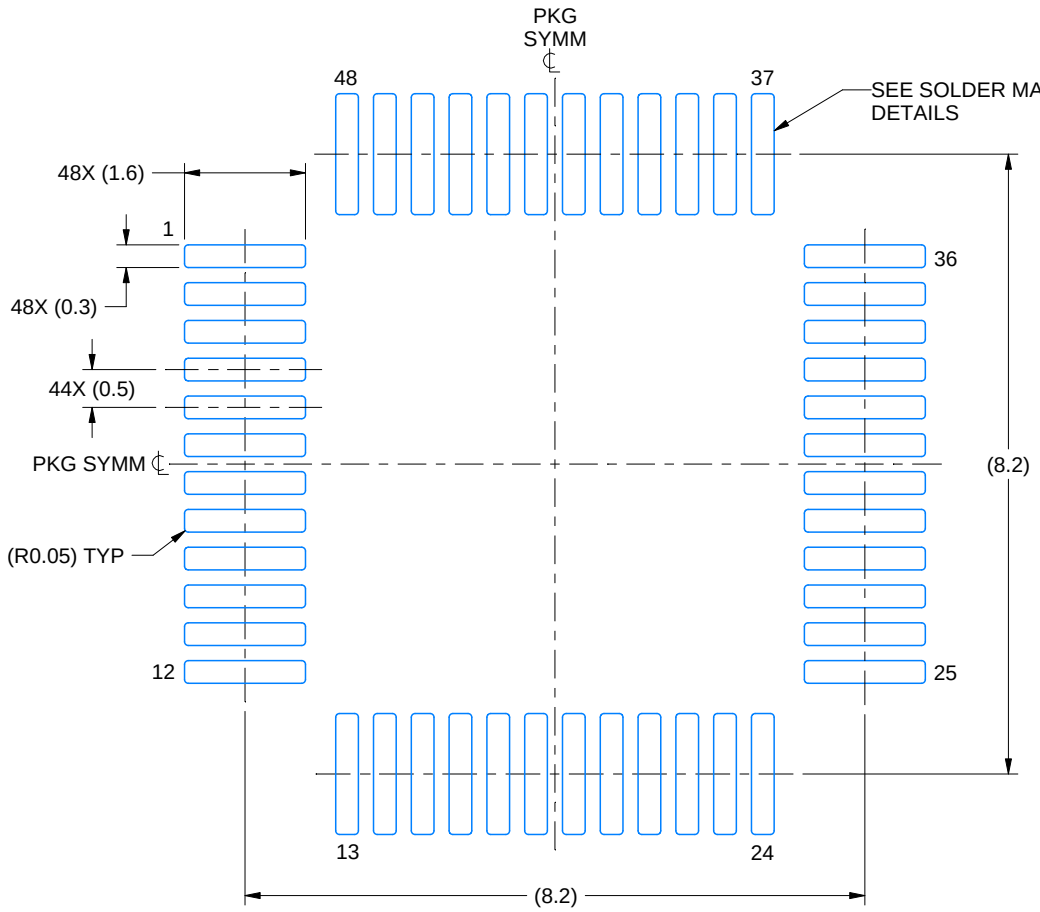
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

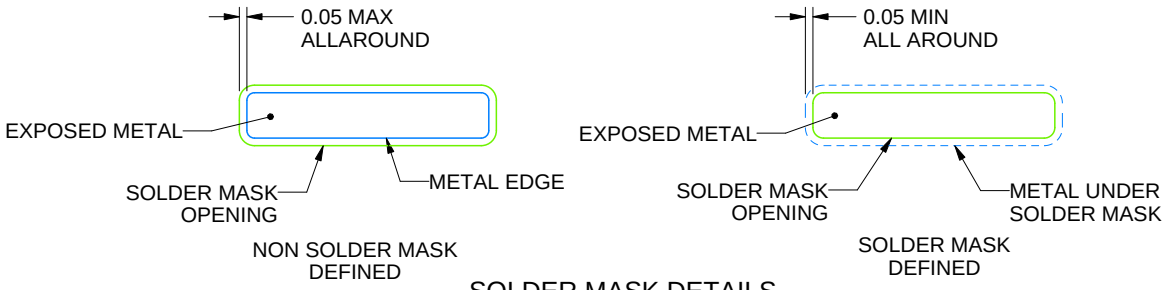


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

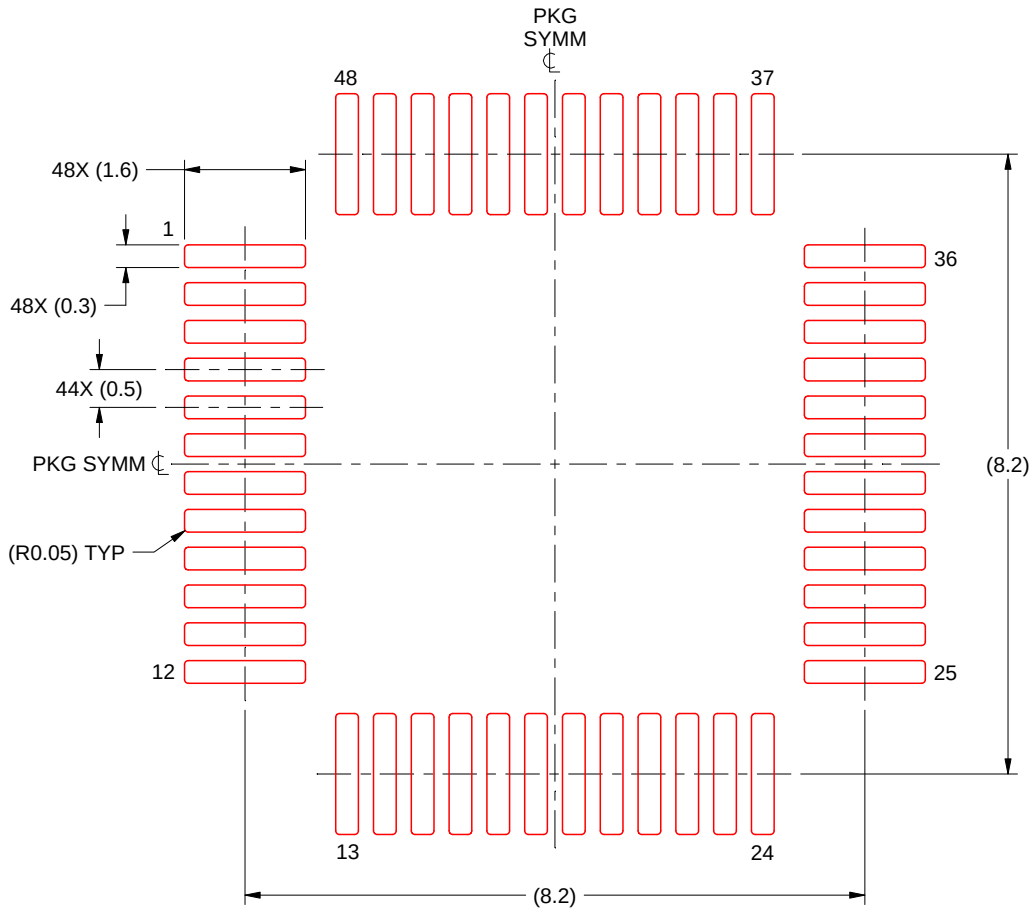


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

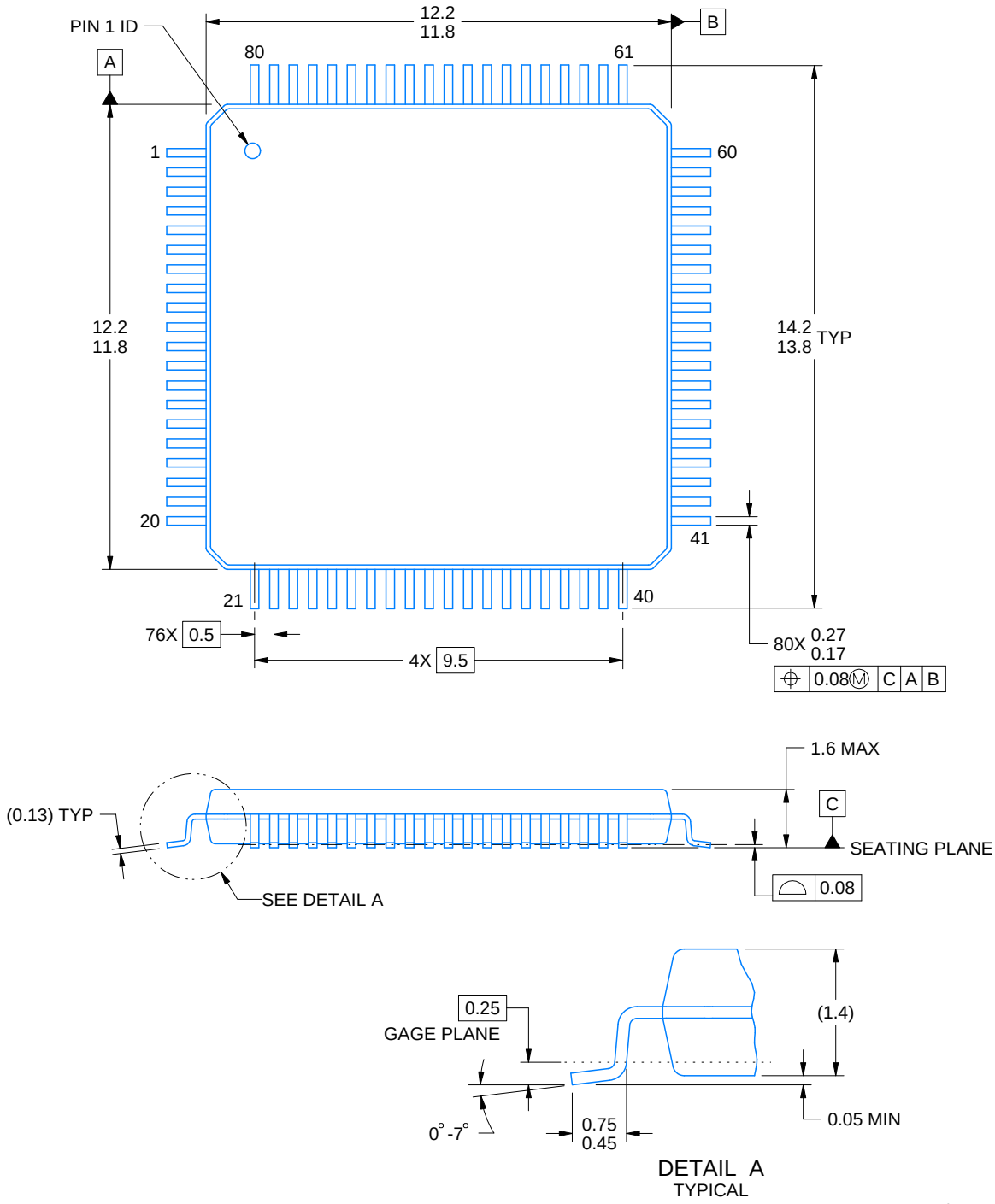
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PN0080A

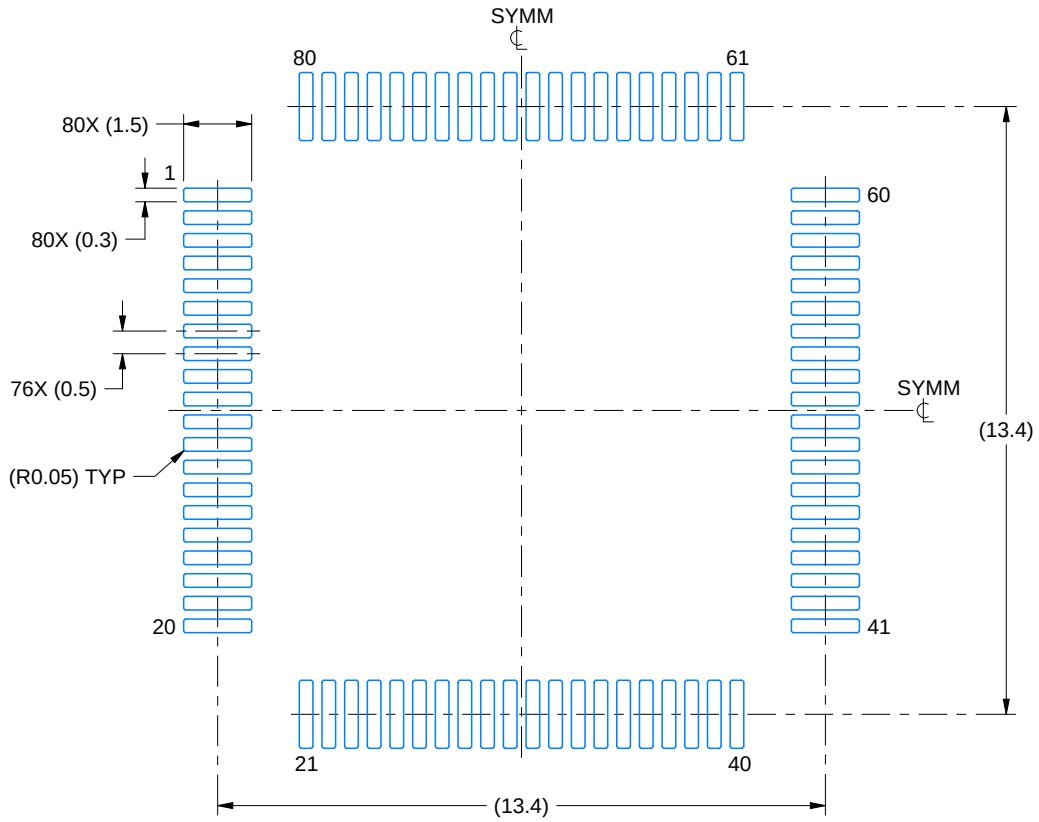
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

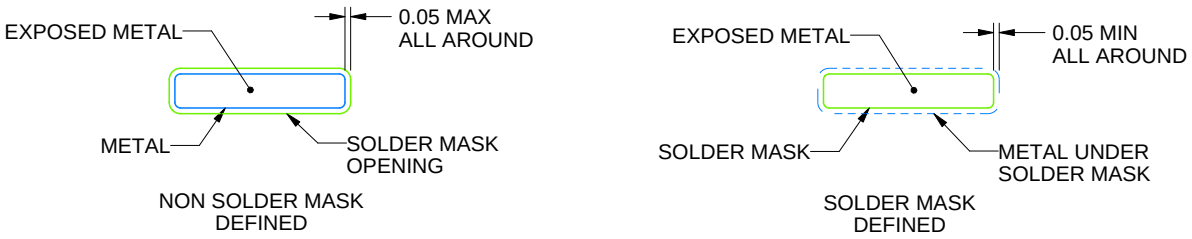


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

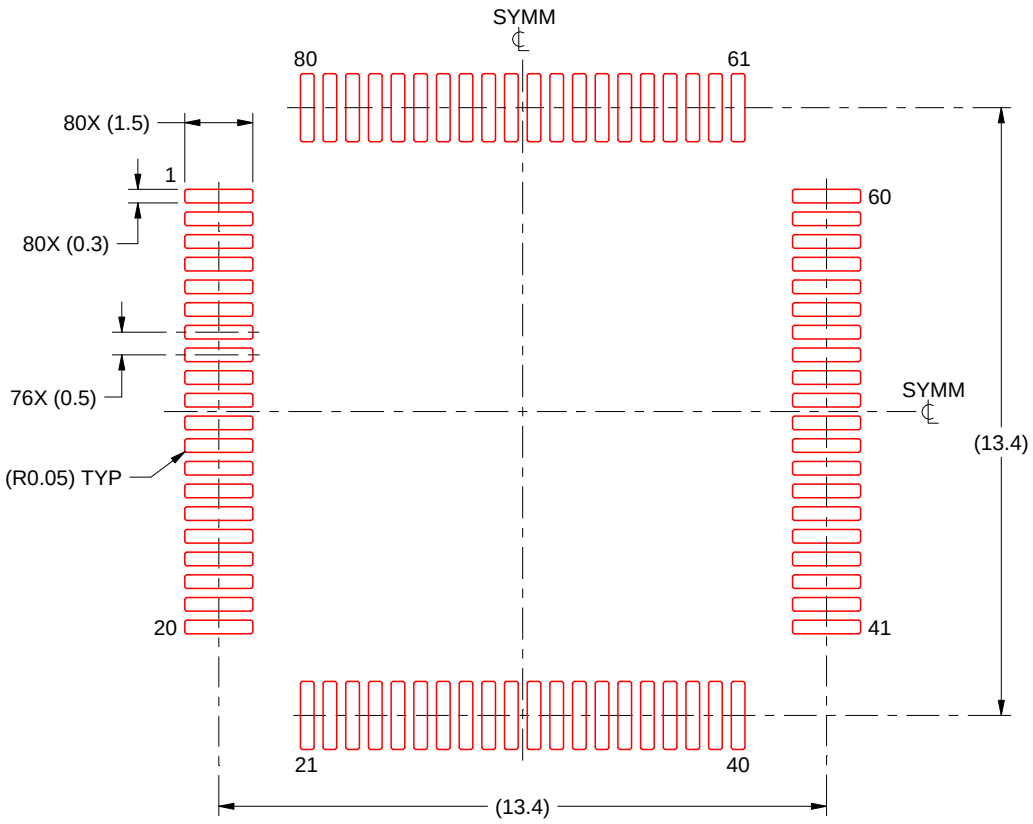


SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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