MUX80X-Q1 100V, Flat R_{ON}, Single 8:1 and Dual 4:1 Multiplexers with Latch-Up Immunity and 1.8V Logic

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature
- High supply voltage capable:
  - Dual supply: ±10V to ±50V
  - Single supply: 10V to 100V
  - Asymmetric dual supply operation
- Consistent parametrics across supply voltages
- Latch-up immune
- Low crosstalk: –110dB
- Removes need for additional logic rail (V_L)
- 1.8V Logic capable
- Fail-safe logic: up to 48V independent of supply
- Integrated pull-down resistor on logic pins
- Bidirectional signal path
- Break-before-make switching
- Wide operating temperature T_A: –40°C to 125°C
- Industry-standard TSSOP and smaller WQFN packages

2 Applications

- High voltage bidirectional switching
- Analog and Digital Multiplexing / Demultiplexing
- Body Control Module (BCM)
- LIDAR Module
- Zone Control Modules (ZCU)
- HEV/EV Battery Management Systems (BMS)
- Advanced Driver Assistance Systems (ADAS)
- EV Charging Systems
- Telematics
- Infotainment

3 Description

The MUX808-Q1 and MUX809-Q1 are modern high voltage capable analog multiplexers in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies, a single supply, or asymmetric supplies up to a maximum supply voltage of 100V. The MUX80x-Q1 devices provide consistent analog parametric performance across the entire supply voltage range. The MUX808-Q1 and MUX809-Q1 support bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins.

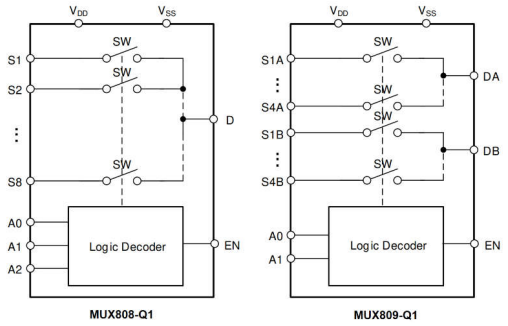
All logic inputs support logic levels of 1.8V, 3.3V, 5V and can be connected as high as 48V, allowing for system flexibility with control signal voltage. Fail-safe logic circuitry allows voltages on the logic pins to be applied before the supply pin, protecting the device from potential damage.

The device family provides latch-up immunity, preventing undesirable high current events between parasitic structures within the device. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows this family of multiplexers to be used in harsh environments.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
MUX808-Q1 MUX809-Q1	PW (TSSOP, 16)	5mm × 6.4mm
	RUM (WQFN, 16)	4mm × 4mm

(1) See *Device Comparison*
(2) For all available packages, see *Section 12*.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



MUX808-Q1 and MUX809-Q1 Block Diagram

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4 Device Comparison Table

PRODUCT	DESCRIPTION
MUX808-Q1	Single channel 8:1 multiplexer
MUX809-Q1	Dual channel 4:1 multiplexer

5 Pin Configuration and Functions

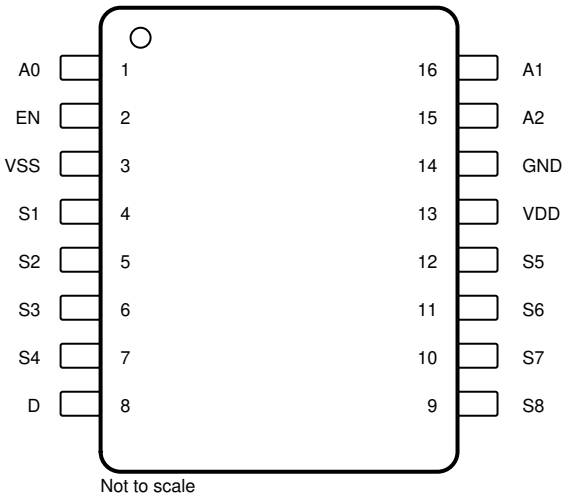


Figure 5-1. PW Package, 16-Pin TSSOP (Top View)

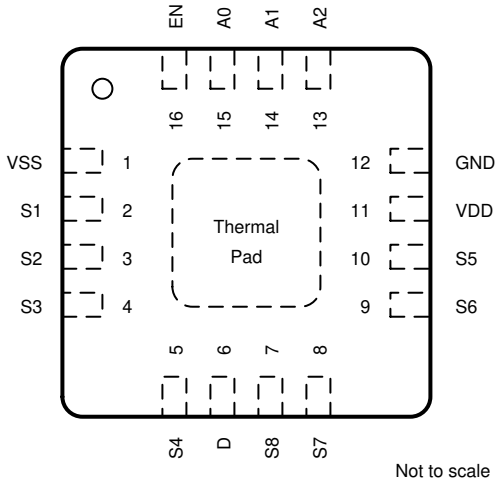


Figure 5-2. RUM Package 16-Pin WQFN (Top View)

Table 5-1. Pin Functions: MUX808-Q1

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0).
EN	2	16	I	Active high digital enable (EN) pin. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND.
S1	4	2	I/O	Source pin 1. Can be an input or output.
S2	5	3	I/O	Source pin 2. Can be an input or output.
S3	6	4	I/O	Source pin 3. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
D	8	6	I/O	Drain pin. Can be an input or output.
S8	9	7	I/O	Source pin 8. Can be an input or output.
S7	10	8	I/O	Source pin 7. Can be an input or output.
S6	11	9	I/O	Source pin 6. Can be an input or output.
S5	12	10	I/O	Source pin 5. Can be an input or output.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
GND	14	12	P	Ground (0V) reference
A2	15	13	I	Logic control input address 2 (A2).
A1	16	14	I	Logic control input address 1 (A1).
Thermal Pad			—	The thermal pad is not connected internally. It is recommended to tie the pad to GND or VSS for the best performance.

(1) I = input, O = output, I/O = input and output, P = power

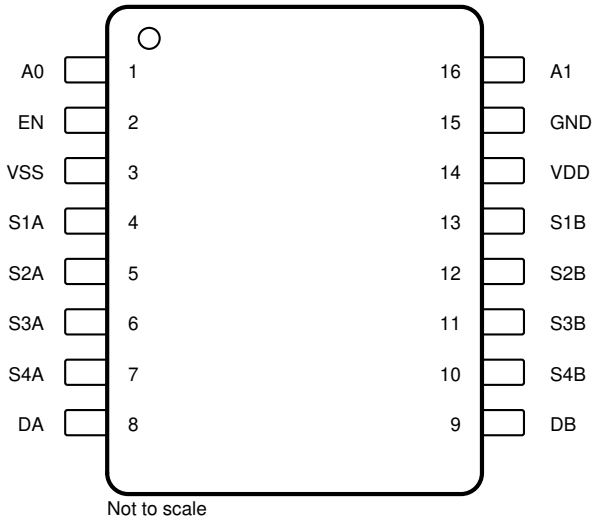


Figure 5-3. PW Package, 16-Pin TSSOP (Top View)

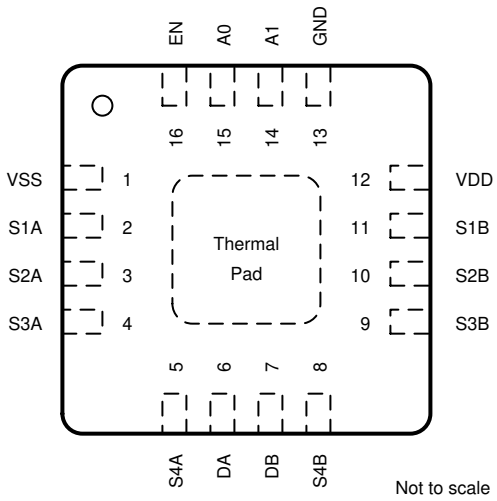


Figure 5-4. RUM Package, 16-Pin WQFN (Top View)

Table 5-2. Pin Functions: MUX809-Q1

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0).
EN	2	16	I	Active high digital enable (EN) pin. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1A	4	2	I/O	Source pin 1A. Can be an input or output.
S2A	5	3	I/O	Source pin 2A. Can be an input or output.
S3A	6	4	I/O	Source pin 3A. Can be an input or output.
S4A	7	5	I/O	Source pin 4A. Can be an input or output.
DA	8	6	I/O	Drain terminal A. Can be an input or output.
DB	9	7	I/O	Drain terminal B. Can be an input or output
S4B	10	8	I/O	Source pin 4B. Can be an input or output.
S3B	11	9	I/O	Source pin 3B. Can be an input or output.
S2B	12	10	I/O	Source pin 2B. Can be an input or output.
S1B	13	11	I/O	Source pin 1B. Can be an input or output.
V_{DD}	14	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	15	13	P	Ground (0 V) reference
A1	16	14	I	Logic control input address 1 (A1).
Thermal Pad			—	The thermal pad is not connected internally. It is recommended to tie the pad to GND or VSS for the best performance.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}–V_{SS}	Supply voltage		110	V
V_{DD}		–0.5	110	V
V_{SS}		–110	0.5	V
V_{Ax} or V_{EN}	Logic control input pin voltage (Ax, EN)	–0.5	50	V
I_{Ax} or I_{EN}	Logic control input pin current (Ax, EN)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS}–2	V_{DD}+2	V
$I_{DC\ (CONT)}$	Source or drain continuous current (Sx, D)	–100	100	mA
I_{IK} (2)	Diode clamp current at 85°C	–100	100	mA
	Diode clamp current at 125°C	–15	15	mA
T_{stg}	Storage temperature	–65	150	°C
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C
P_{tot} (3)	Total power dissipation (TSSOP)		720	mW

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 10.5 mW/°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential		10		100	V
V_{DD}	Positive power supply voltage		10		100	V
V_S or V_D (2)	Signal path input/output voltage (source or drain pin)		V_{SS}		V_{DD}	V
V_A or V_{EN}	Address or enable pin voltage		0		48	V
T_A	Ambient temperature		–40		125	°C
V_S or V_D (2)	Signal path input/output voltage (source or drain pin)		V_{SS}		V_{DD}	V
T_A	Ambient temperature		–40		125	°C
I_{DC} 1ch.(3)	Continuous current through switch for TSSOP or QFN on 1 channel				100	mA
I_{DC} All ch.(4)	Continuous current through switch on all channels at the same time, TSSOP package	T_A = 25°C			75	mA
		T_A = 85°C			50	mA
		T_A = 125°C			25	mA

(1) V_{DD} and V_{SS} can be any value as long as 10V ≤ (V_{DD} – V_{SS}) ≤ 100V, and the minimum V_{DD} is met.
(2) V_S or V_D is the voltage on any Source or Drain pins.
(3) Max continuous current shown for a single channel at a time.
(4) Max continuous current shown for all channels at a time. Refer to max power dissipation (P_{tot}) to ensure package limitations are not violated.

6.4 Thermal Information

THERMAL METRIC(1)		MUX808-Q1	MUX809-Q1	MUX808-Q1 MUX809-Q1	UNIT
		PW (TSSOP)	PW (TSSOP)	RUM (QFN)	
		16 PINS	16 PINS	16 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	97.0	96.4	41.9	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	26.7	26.5	25.8	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	43.8	43.1	17.0	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	1.1	1.1	0.3	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	43.1	42.5	17.0	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)
typical at V_{DD} = +36V, V_{SS} = –36V, GND = 0V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		48	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current	Logic inputs = 0V, 5V, or 48V	–40°C to +125°C		0.4	3.8	µA
I_{IL}	Input leakage current	Logic inputs = 0V, 5V, or 48V	–40°C to +125°C	–0.2	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V, 5V, or 48V	25°C		250	500	µA
			–40°C to +85°C			500	µA
			–40°C to +125°C			500	µA
I_{SS}	V_{SS} supply current	Logic inputs = 0V, 5V, or 48V	25°C		250	420	µA
			–40°C to +85°C			420	µA
			–40°C to +125°C			420	µA

6.6 Electrical Characteristics (±15V Dual Supply)

V_{DD} = +15V ± 10%, V_{SS} = –15V ± 10%, GND = 0V (unless otherwise noted)
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10V to +10V I_D = –5mA	25°C		38	55	Ω
			–40°C to +85°C			75	Ω
			–40°C to +125°C			90	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10V to +10V I_D = –5mA	25°C		0.65		Ω
			–40°C to +85°C			3.5	Ω
			–40°C to +125°C			4.1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10V to +10V I_D = –5mA	25°C		0.5		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –5mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / +10V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	µA
			–40°C to +125°C	-1		1	µA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / +10V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	µA
			–40°C to +125°C	-1		1	µA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is on V_S = V_D = ±10V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	µA
			–40°C to +125°C	-1		1	µA

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

6.7 Electrical Characteristics (±36V Dual Supply)

V_{DD} = +36V ± 10%, V_{SS} = –36V ± 10%, GND = 0V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = -25V to +25V I_D = –5mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = -25V to +25V I_D = –5mA	25°C		0.65		Ω
			–40°C to +85°C			3.5	
			–40°C to +125°C			4.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = -25V to +25V I_D = –5mA	25°C		0.9		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –5mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 39.6V, V_{SS} = –39.6V Switch state is off V_S = +25V / –25V V_D = –25V / +25V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 39.6V, V_{SS} = –39.6V Switch state is off V_S = +25V / –25V V_D = –25V / +25V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 39.6V, V_{SS} = –39.6V Switch state is on V_S = V_D = ±25V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

6.8 Electrical Characteristics (±50V Dual Supply)

V_{DD} = +50V, V_{SS} = –50V, GND = 0V (unless otherwise noted)
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –45V to +45V I_D = –5mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –45V to +45V I_D = –5mA	25°C		0.65		Ω
			–40°C to +85°C			3.5	
			–40°C to +125°C			4.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –45V to +45V I_D = –5mA	25°C		1		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –5mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 50V, V_{SS} = –50V Switch state is off V_S = +45V / –45V V_D = –45V / +45V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 50V, V_{SS} = –50V Switch state is off V_S = +45V / –45V V_D = –45V / +45V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 50V, V_{SS} = –50V Switch state is on V_S = V_D = ±45V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

6.9 Electrical Characteristics (72V Single Supply)

V_{DD} = +72V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to +60V I_D = –5mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0V to +60V I_D = –5mA	25°C		0.65		Ω
			–40°C to +85°C			3.5	
			–40°C to +125°C			4.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to +60V I_D = –5mA	25°C		0.6		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –5mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off V_S = +60V / 1V V_D = 1V / +60V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off V_S = +60V / 1V V_D = 1V / +60V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	Switch state is on V_S = V_D = 1V / +60V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	

(1) When V_S is 60V, V_D is 1V. Or when V_S is 1V, V_D is 60V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

6.10 Electrical Characteristics (100V Single Supply)

V_{DD} = +100V, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to +95V I_D = –5mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0V to +95V I_D = –5mA	25°C		0.65		Ω
			–40°C to +85°C			3.5	
			–40°C to +125°C			4.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to +95V I_D = –5mA	25°C		0.6		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –5mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off V_S = +95V / 1V V_D = 1V / +95V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off V_S = +95V / 1V V_D = 1V / +95V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	Switch state is on V_S = V_D = 1V / +95V	25°C		±0.1		µA
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	-1		1	

(1) When V_S is 95V, V_D is 1V. Or when V_S is 1V, V_D is 95V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

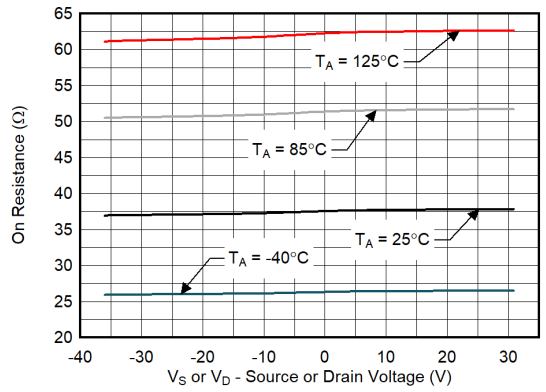
6.11 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)
typical at V_{DD} = +36V, V_{SS} = –36V, GND = 0V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10V R_L = 10kΩ, C_L = 15pF	25°C		3		µs
			–40°C to +85°C			10	
			–40°C to +125°C			12	
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10V R_L = 10kΩ, C_L = 15pF	25°C		3		µs
			–40°C to +85°C			14	
			–40°C to +125°C			15	
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10V R_L = 10kΩ, C_L = 15pF	25°C		0.65		µs
			–40°C to +85°C			3	
			–40°C to +125°C			3	
t_{BBM}	Break-before-make time delay	V_S = 10V, R_L = 10kΩ, C_L = 15pF	25°C		3		µs
			–40°C to +85°C	0.1			
			–40°C to +125°C	0.1			
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} ramp rate = 1V/µs, V_S = 10V, R_L = 10kΩ, C_L = 15pF	25°C		75		µs
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF	25°C		550		ps
Q_{INJ}	Charge injection	V_S = (V_{DD} + V_{SS}) / 2, C_L = 1nF	25°C		–150		pC
O_{ISO}	Off isolation	R_L = 50Ω , C_L = 5pF V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		–110		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		–110		dB
BW	–3dB bandwidth (MUX808Q1)	R_L = 50Ω , C_L = 5pF V_S = (V_{DD} + V_{SS}) / 2	25°C		200		MHz
BW	–3dB bandwidth (MUX809Q1)				380		
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		–2.8		dB
THD+N	Total harmonic distortion + Noise	Dual supply voltage V_{PP} = 5V, V_{BIAS} = (V_{DD} + V_{SS}) / 2 R_L = 1kΩ , C_L = 5pF, f = 20Hz to 20kHz	25°C		0.003		%
$C_{S(OFF)}$	Source off capacitance	V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		3		pF
$C_{D(OFF)}$	Drain off capacitance (MUX808Q1)	V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		20		pF
$C_{D(OFF)}$	Drain off capacitance (MUX809Q1)	V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		10		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (MUX808Q1)	V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		21		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (MUX809Q1)	V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		12		pF

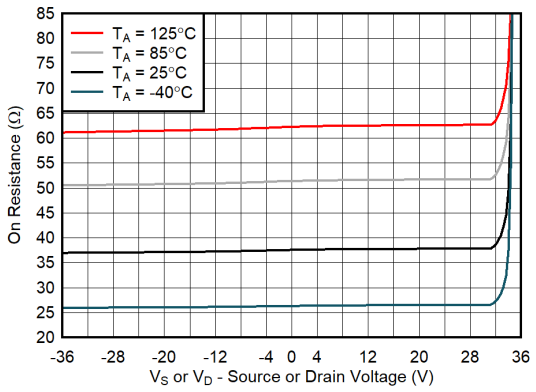
6.12 Typical Characteristics

at T_A = 25°C, V_{DD} = +36V, and V_{SS} = –36V (unless otherwise noted)



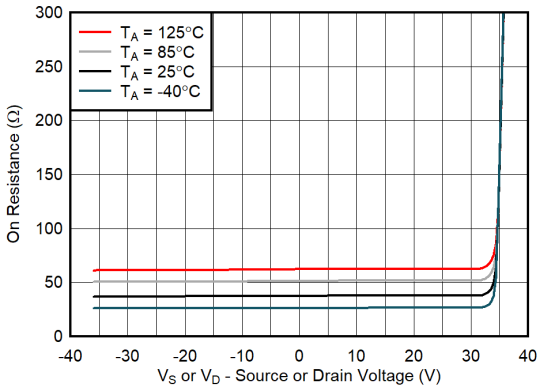
V_{DD} = 36V, V_{SS} = –36V
Flatest Ron Region

Figure 6-1. On-Resistance vs Source or Drain Voltage



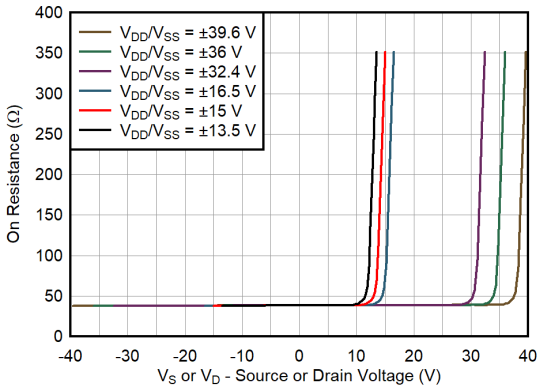
V_{DD} = 36V, V_{SS} = –36V

Figure 6-2. On-Resistance vs Source or Drain Voltage



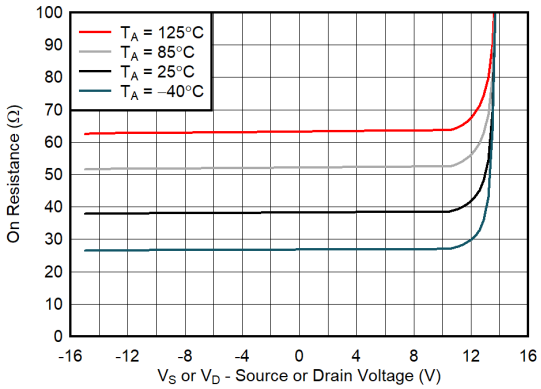
V_{DD} = 36V, V_{SS} = –36V

Figure 6-3. On-Resistance vs Source or Drain Voltage



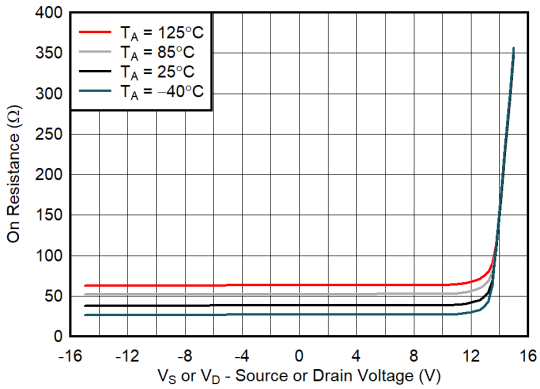
Dual Supply Voltages

Figure 6-4. On-Resistance vs Source or Drain Voltage



V_{DD} = 15V, V_{SS} = –15V

Figure 6-5. On-Resistance vs Source or Drain Voltage

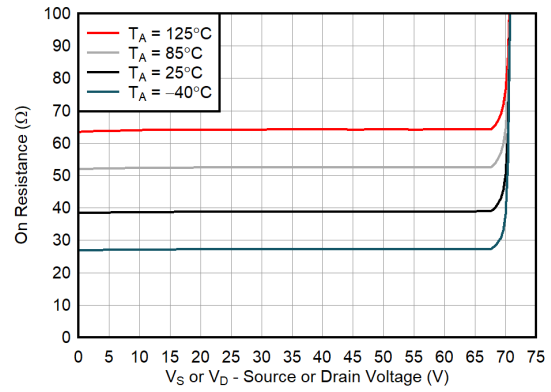


V_{DD} = 15V, V_{SS} = –15V

Figure 6-6. On-Resistance vs Source or Drain Voltage

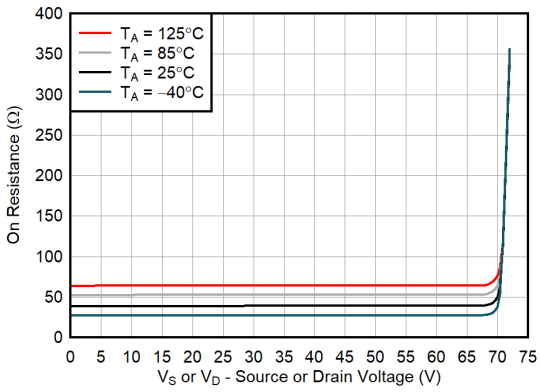
6.12 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36V, and V_{SS} = –36V (unless otherwise noted)



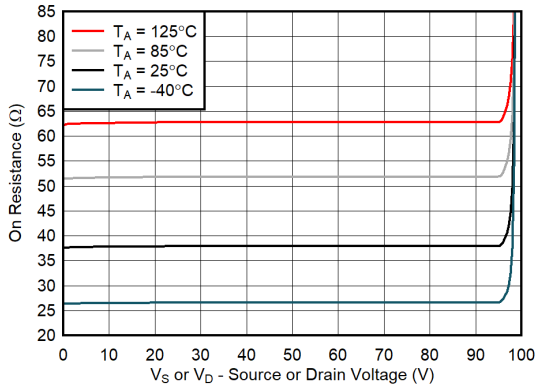
V_{DD} = 72V, V_{SS} = 0V

Figure 6-7. On-Resistance vs Source or Drain Voltage



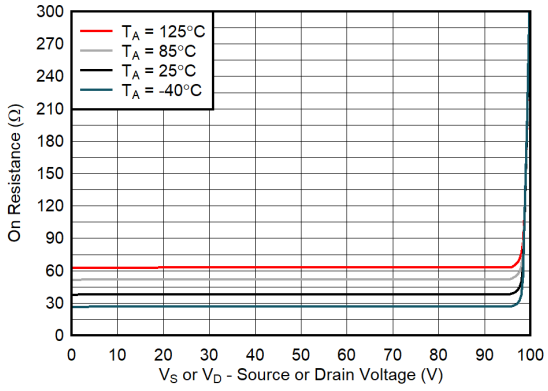
V_{DD} = 72V, V_{SS} = 0V

Figure 6-8. On-Resistance vs Source or Drain Voltage



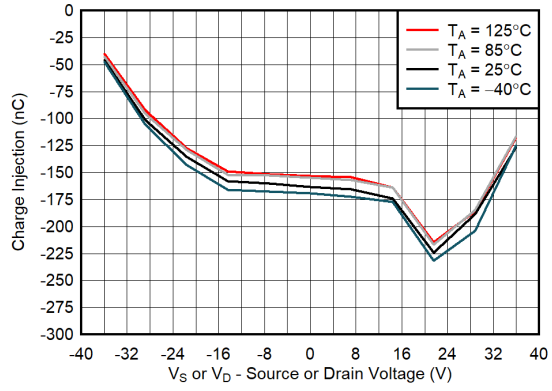
V_{DD} = 100V, V_{SS} = 0V

Figure 6-9. On-Resistance vs Source or Drain Voltage



V_{DD} = 100V, V_{SS} = 0V

Figure 6-10. On-Resistance vs Source or Drain Voltage



V_{DD} = 36V, V_{SS} = –36V

Figure 6-11. Charge Injection vs Source Voltage

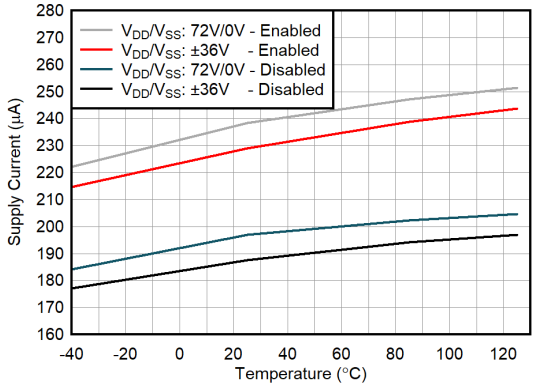
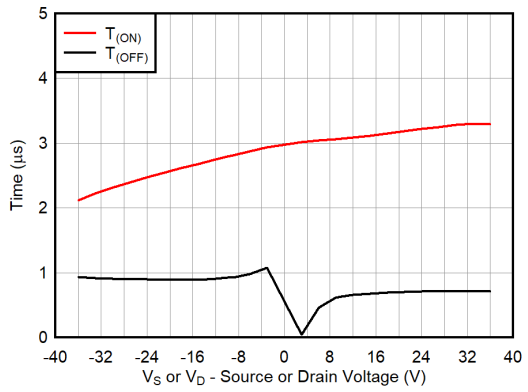


Figure 6-12. Supply Current vs Temperature

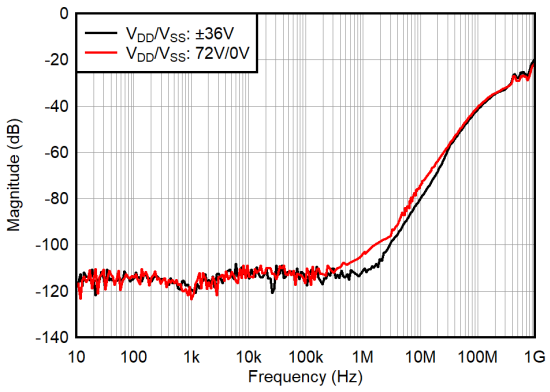
6.12 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36V, and V_{SS} = –36V (unless otherwise noted)



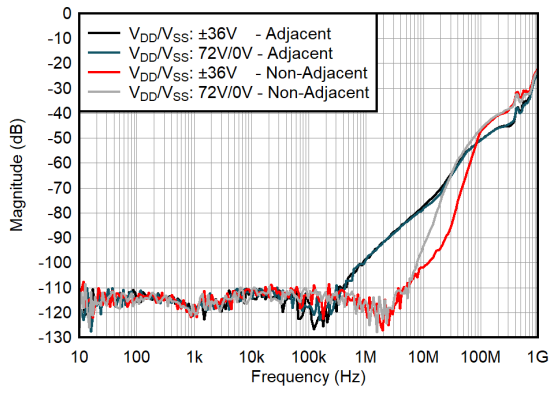
V_{DD} = 36V, V_{SS} = –36V

Figure 6-13. Turn-On and Turn-Off Times vs Source Voltage



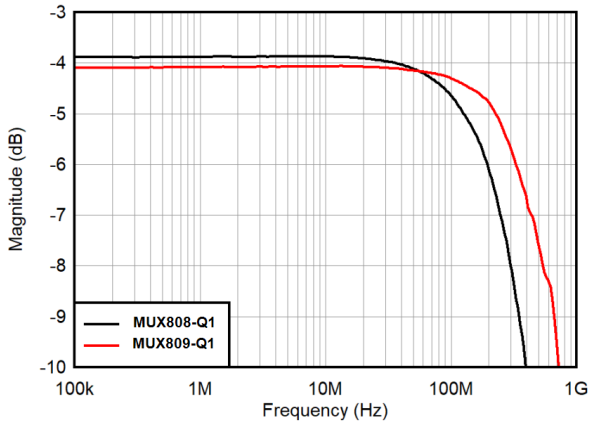
T_A = 25°C

Figure 6-14. Off Isolation vs Frequency



T_A = 25°C

Figure 6-15. Crosstalk vs Frequency



Bandwidth

Figure 6-16. Insertion Loss vs Frequency

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of the MUX808-Q1 and MUX809-Q1 is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. Figure 7-1 shows how the symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is also shown in the following figure. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

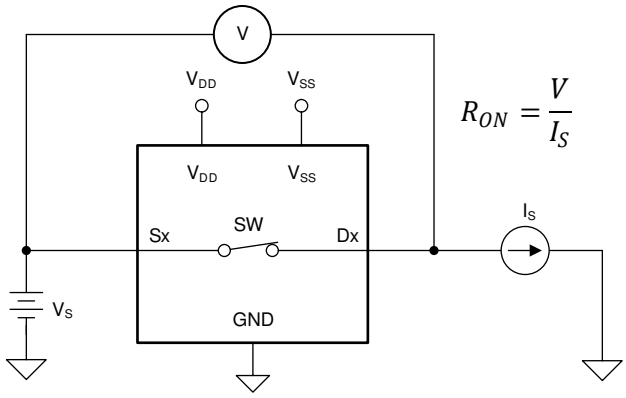


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

Figure 7-2 shows the setup used to measure both off-leakage currents.

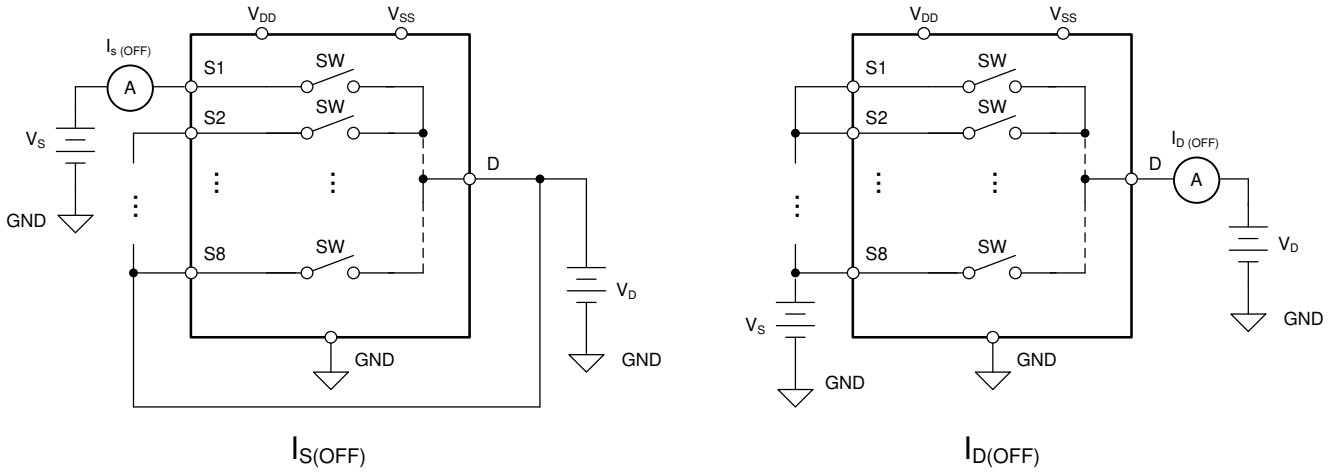


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 7-3 shows the circuit used for measuring the on-leakage currents.

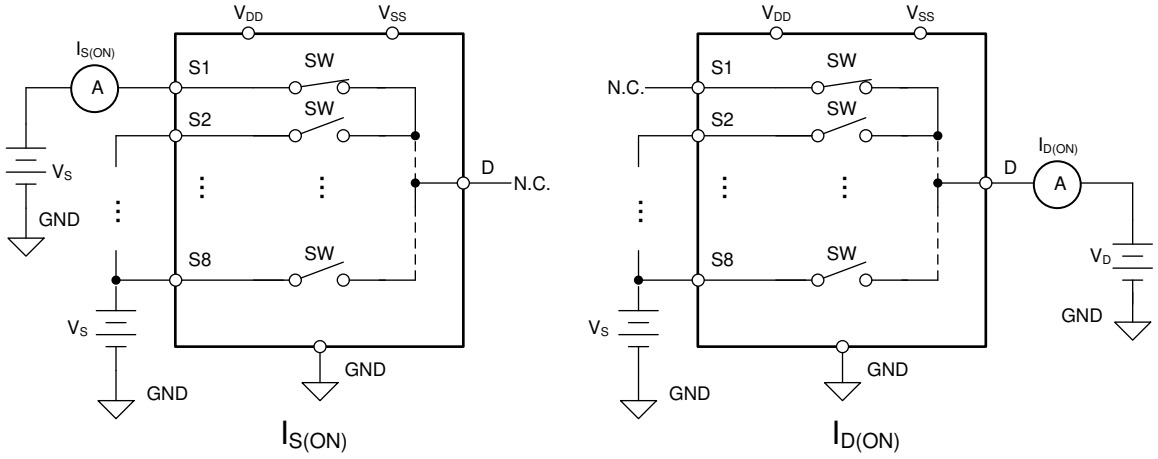


Figure 7-3. On-Leakage Measurement Setup

7.4 Break-Before-Make Delay

The break-before-make delay is a safety feature of the MUX808-Q1 and MUX809-Q1. The ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-4 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

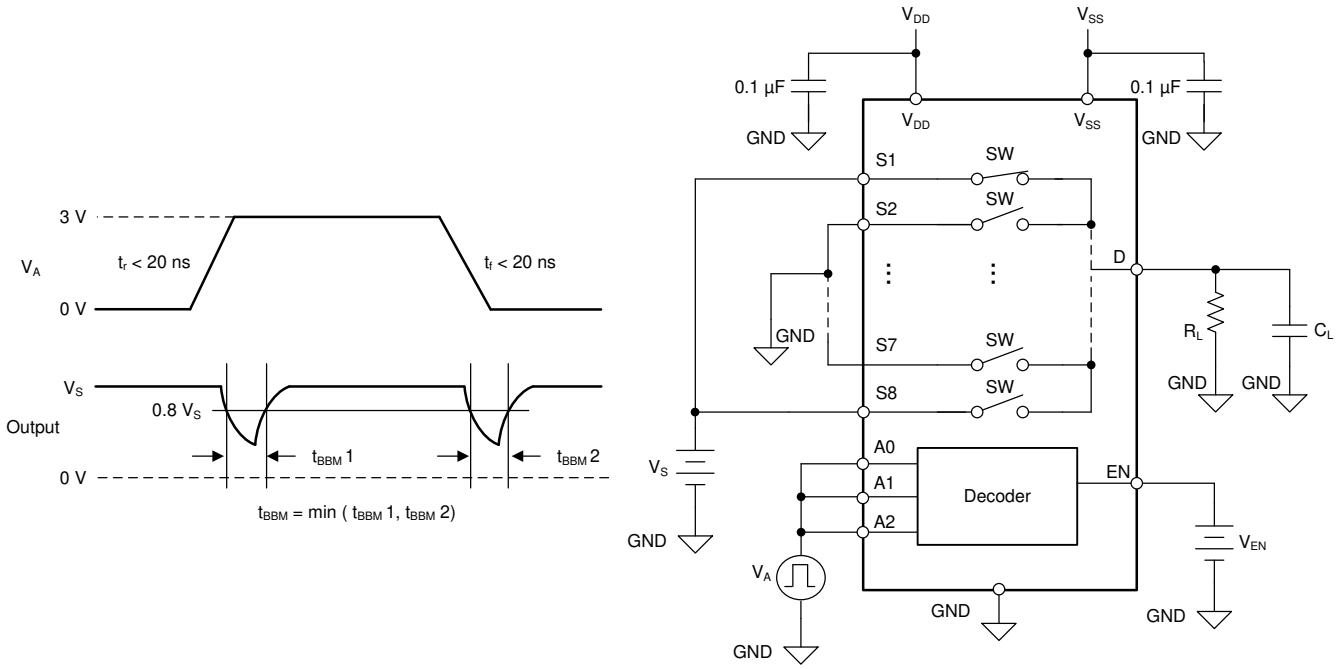


Figure 7-4. Break-Before-Make Delay Measurement Setup

7.5 Enable Turn-on and Turn-off Time

$t_{ON(EN)}$ time is defined as the time taken by the output of the MUX808-Q1 and MUX809-Q1 to rise to a 90% final value after the EN signal has risen to a 50% final value. $t_{OFF(EN)}$ is defined as the time taken by the output of the MUX808-Q1 and MUX809-Q1 to fall to a 10% final value after the EN signal has fallen to a 50% initial value. Figure 7-5 shows the setup used to measure the enable delay time.

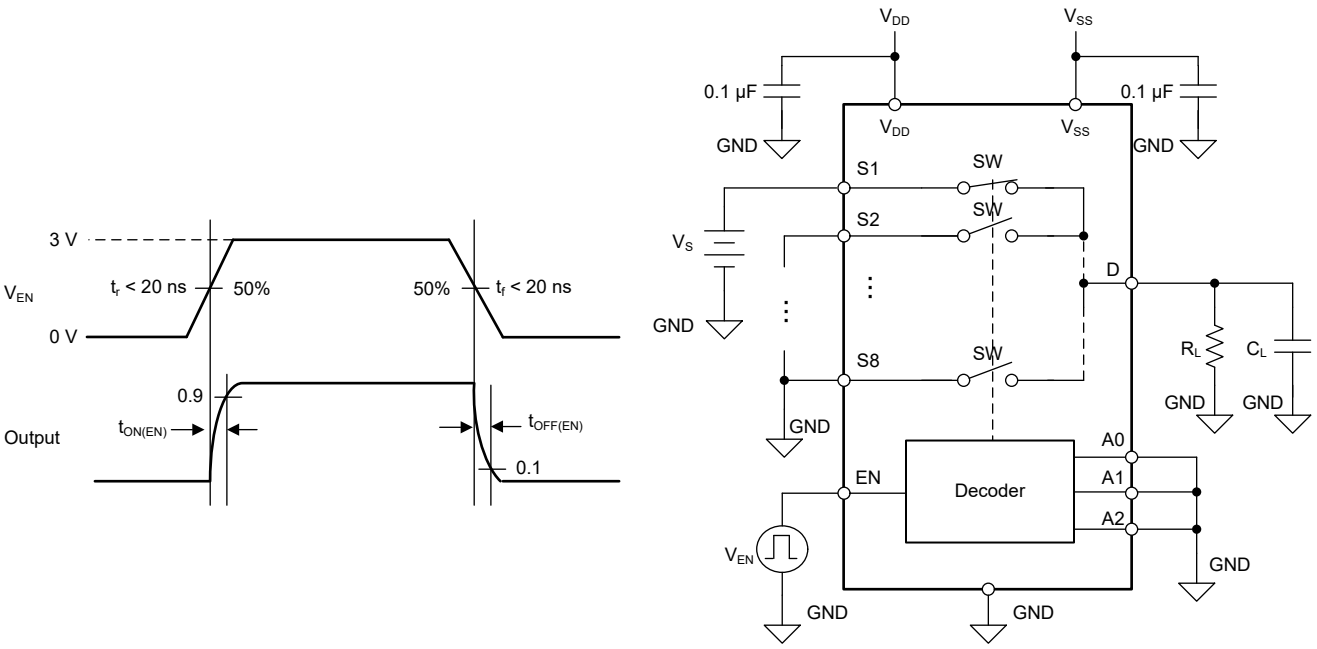


Figure 7-5. Enable Delay Measurement Setup

7.6 Transition Time

Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the address signal (Ax) has fallen or risen to 50% of the transition. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

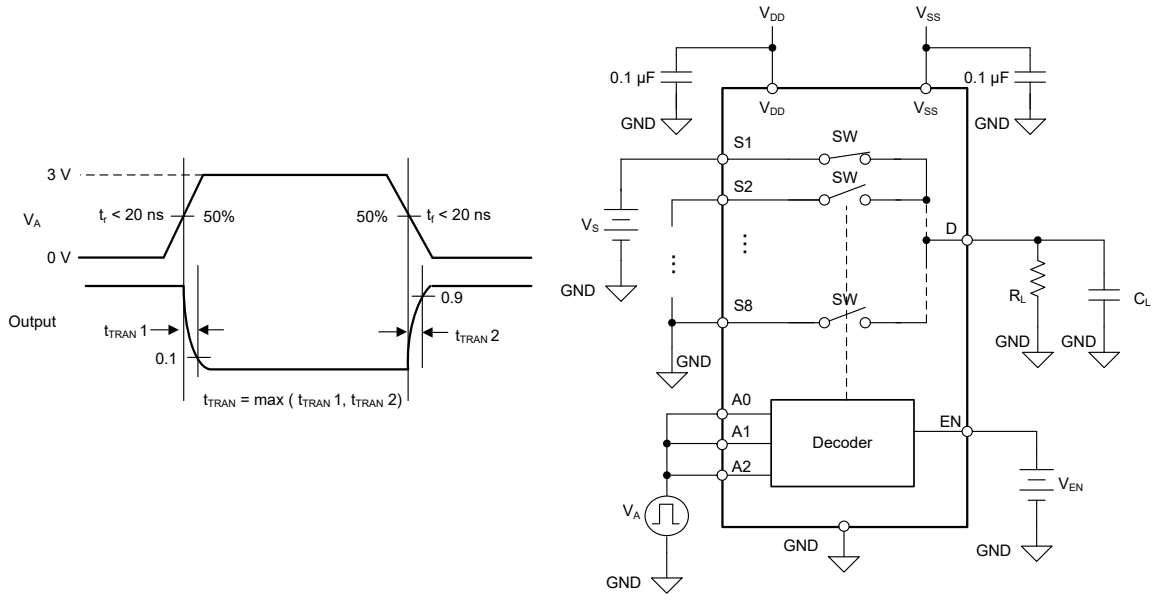


Figure 7-6. Transition Time Measurement Setup

7.7 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching, and is denoted by the symbol Q_{INJ}. Figure 7-7 shows the setup used to measure charge injection from the source to drain.

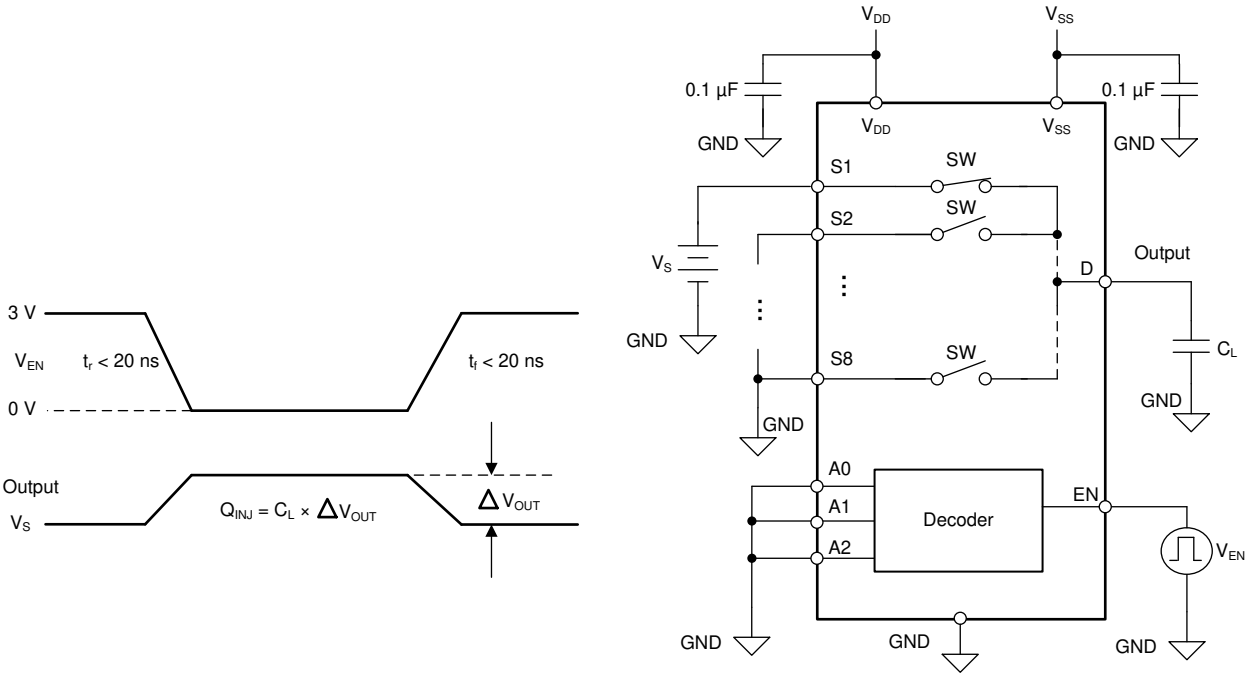
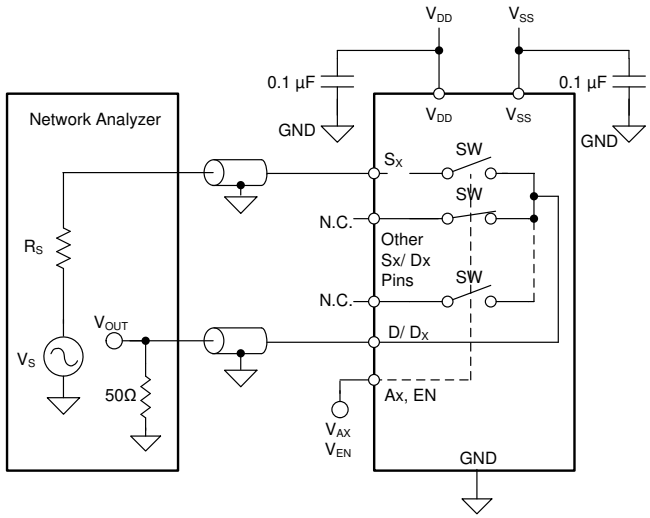


Figure 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance for the measurement (Z_O) is 50 Ω. Figure 7-8 shows the setup used to measure off isolation.



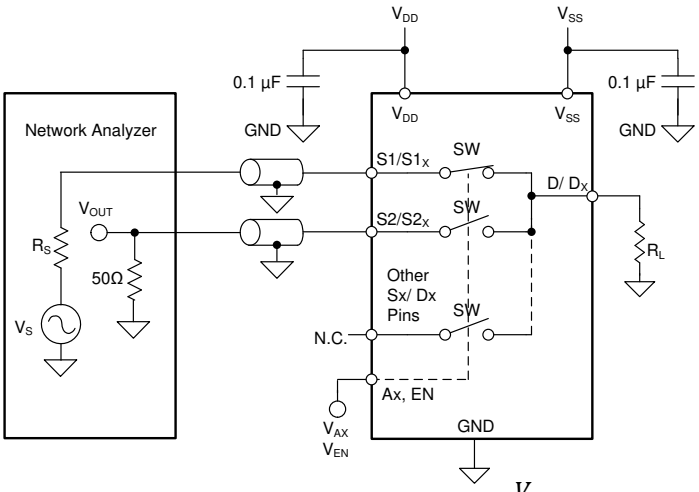
$$Off\ Isolation = 20 \times Log\frac{V_{OUT}}{V_S}$$

Figure 7-8. Off Isolation Measurement Setup

7.9 Crosstalk

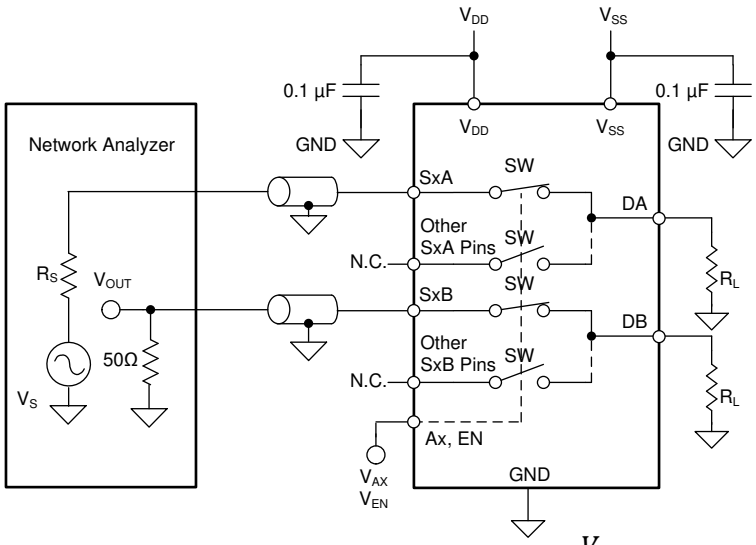
There are two types of crosstalk that can be defined for the devices:

1. Intra-channel crosstalk ($X_{TALK(INTRA)}$): the voltage at the source pin (Sx) of an off-switch input when a signal is applied at the source pin of an on-switch input in the same channel, as shown in Figure 7-9 .
2. Inter-channel crosstalk ($X_{TALK(INTER)}$): the voltage at the source pin (Sx) of an on-switch input when a signal is applied at the source pin of an on-switch input in a different channel, as shown in Figure 7-10. Inter-channel crosstalk applies only to the MUX809-Q1 device.



$$Intra - channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-9. Intra-channel Crosstalk Measurement Setup



$$Inter - channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-10. Inter-channel Crosstalk Measurement Setup

7.10 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D or Dx) of the MUX80x-Q1. Figure 7-11 shows the setup used to measure bandwidth of the switch.

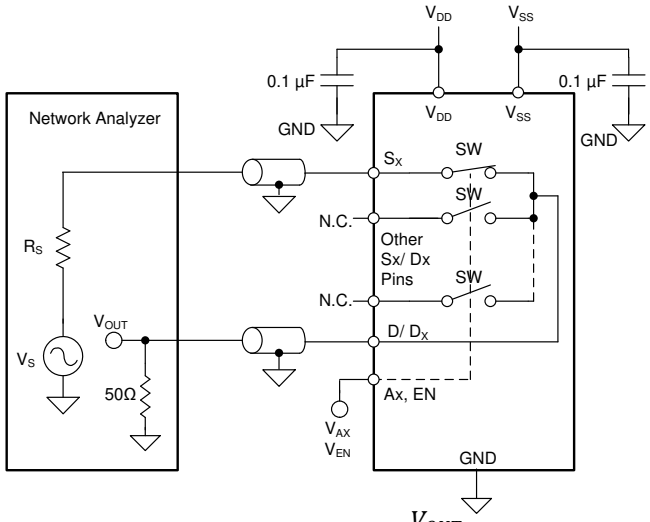


Figure 7-11. Bandwidth Measurement Setup

7.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The on-resistance of the MUX808-Q1 and MUX809-Q1 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 7-12 shows the setup used to measure THD+N of the devices.

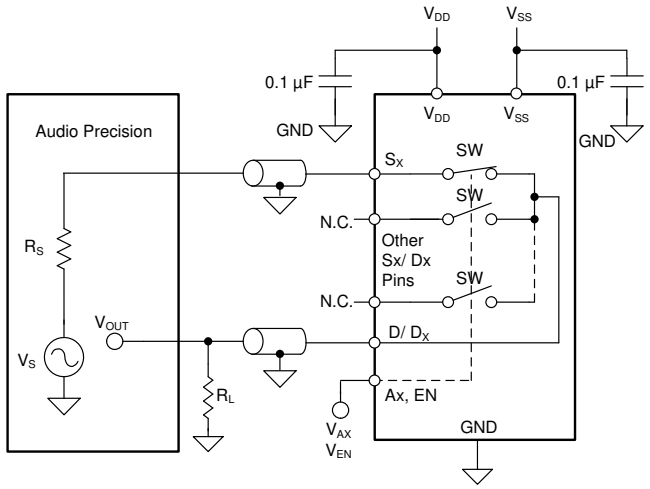


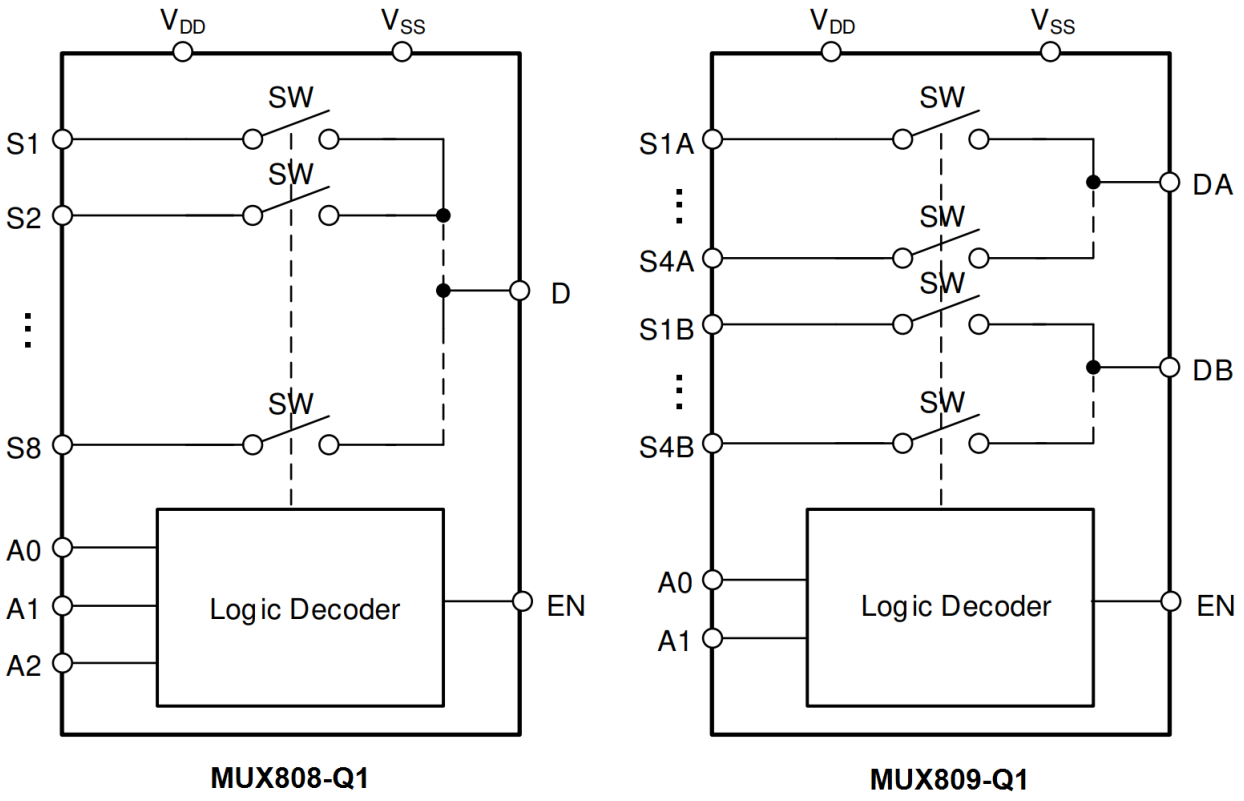
Figure 7-12. THD+N Measurement Setup

8 Detailed Description

8.1 Overview

The MUX808-Q1 and MUX809-Q1 are modern complementary metal-oxide semiconductor (CMOS) analog multiplexers in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies, a single supply, or asymmetric supplies up to 100V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The MUX808-Q1 and MUX809-Q1 conduct equally well from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Each signal path has very similar characteristics in both directions.

8.3.2 Flat On – Resistance

The MUX808-Q1 and MUX809-Q1 are designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operating region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

The flatest on-resistance region extends from V_{SS} to roughly 5V below V_{DD}. Once the signal is within 5V of V_{DD} the on-resistance will exponentially increase and can impact desired signal transmission.

8.3.3 Protection Features

The MUX808-Q1 and MUX809-Q1 offer a number of protection features to enable robust system implementations.

8.3.3.1 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. Additionally the fail safe logic feature allows the logic inputs of the mux to be interfaced with high voltages, allowing for simplified interfacing if only high voltage control signals are present. The logic inputs are protected against positive faults of up to +48V in powered-off condition, but do not offer protection against negative overvoltage condition.

Fail-safe logic also allows the devices to interface with a voltage greater than V_{DD} on the control pins during normal operation to add maximum flexibility in system design. For example, with a V_{DD} = 15V, the logic control pins could be connected to +24V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 48V.

8.3.3.2 ESD Protection

All pins on the MUX808-Q1 and MUX809-Q1 support HBM ESD protection level up to ±2 kV, which helps protect the devices from ESD events during the manufacturing process.

8.3.3.3 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

In the MUX808-Q1 and MUX809-Q1 devices, an insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming. As a result, the devices are latch-up immune under all circumstances by device construction.

The MUX808-Q1 and MUX809-Q1 devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the MUX808-Q1 and MUX809-Q1 to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.3.4 1.8V Logic Compatible Inputs

The MUX808-Q1 and MUX809-Q1 devices have 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the MUX808-Q1 and MUX809-Q1 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of materials cost. For more information on 1.8V logic implementations, refer to *Simplifying Design with 1.8V logic Muxes and Switches*.

8.3.5 Integrated Pull-Down Resistor on Logic Pins

The MUX808-Q1 and MUX809-Q1 have internal weak pull-down resistors to GND so that the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.4 Device Functional Modes

8.4.1 Normal Mode

In Normal Mode operation, signals of up to V_{DD} and V_{SS} can be passed through the switch from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Table 8-1 and Table 8-2 provides the address (Ax) pins and the enable (EN) pin determines which switch path to turn on. The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies (V_{DD} – V_{SS}) must be greater than or equal to 10V. With a minimum V_{DD} of 10V.
- The input signals on the source (Sx) or the drain (Dx) must be between V_{DD} and V_{SS}.
- The logic control address pins (Ax) must have selected the switch path.

8.4.2 Truth Tables

Table 8-1 provides the truth tables for the MUX808-Q1.

Table 8-1. MUX808-Q1 Truth Table

EN	A2	A1	A0	Normal Condition
0	X(1)	X(1)	X(1)	None
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) "X" means "do not care."

Table 8-2 provides the truth tables for the MUX809-Q1.

Table 8-2. MUX809-Q1 Truth Table

EN	A1	A0	Normal Condition
0	X(1)	X(1)	None
1	0	0	S1x
1	0	1	S2x
1	1	0	S3x
1	1	1	S4x

(1) "X" means "do not care."

If unused, then address (Ax) pins must be tied to GND or Logic High in so that the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND for best performance.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The MUX808-Q1 and MUX809-Q1 are high voltage multiplexers capable of supporting analog and digital signals. The high voltage capability of these multiplexers allow them to be used in systems with high voltage signal swings or in systems with high common mode voltages.

Additionally, the MUX80x-Q1 devices provide consistent analog parametric performance across the entire supply voltage range allowing the devices to be powered by the most convenient supply rails in the system while still providing excellent performance.

9.2 Typical Application

One example to take advantage of MUX80x-Q1 performance is the implementation of multiplexed data acquisition front end for multiple input sensors. Applications such as analog input modules for zone control modules (ZCUs), data acquisition (DAQ), and body domain controllers commonly need to monitor multiple signals into a single ADC channel. The multiple inputs can come from different system voltages being monitored, or environmental sensors such as temperature or humidity. Figure 9-1 shows a simplified example of monitoring multiple inputs into a single ADC using a multiplexer.

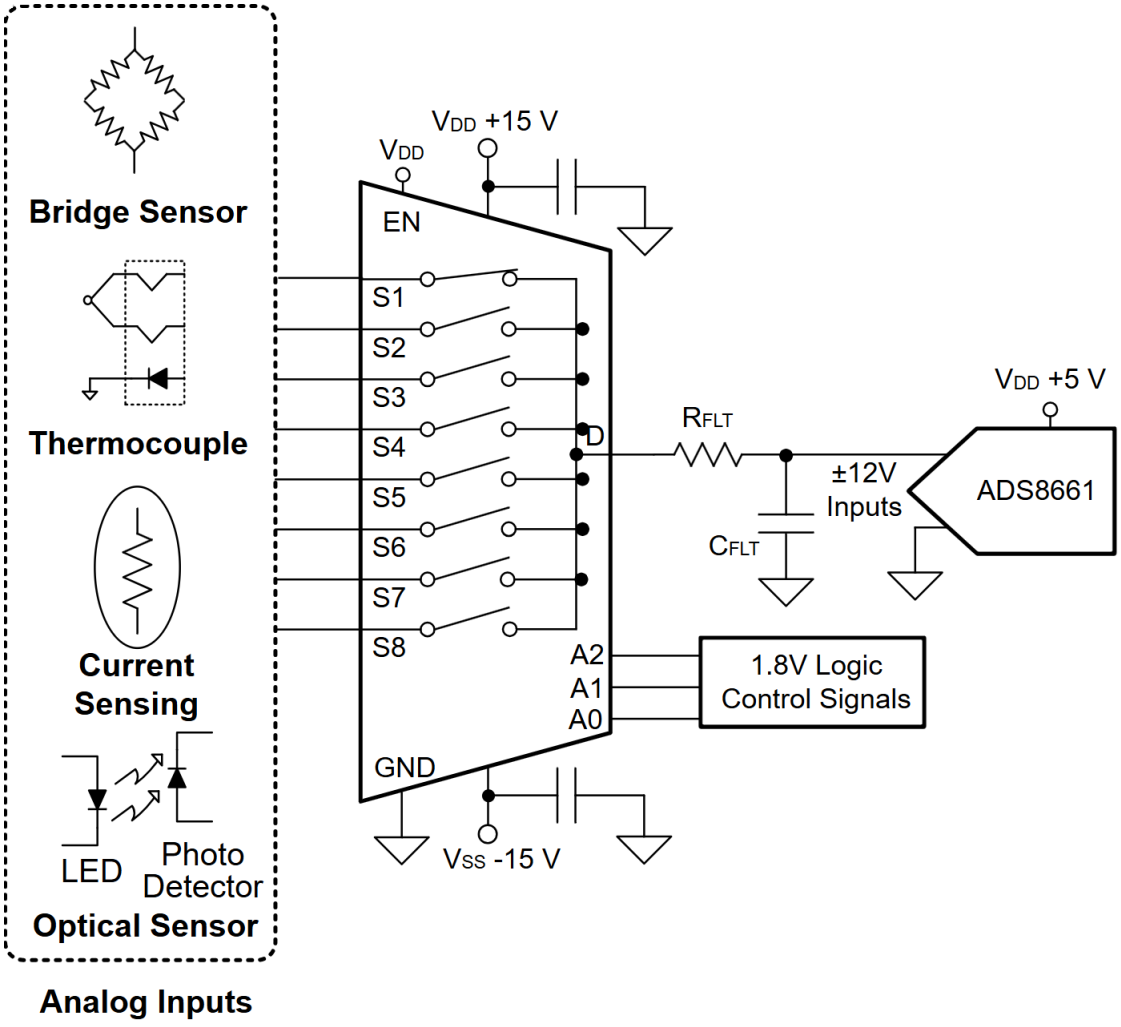


Figure 9-1. Multiplexed Data Acquisition Front End

9.2.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux and Op Amps	+ 15V
Negative supply (V_{SS}) mux and Op Amps	-15V
Maximum input / output signals with common mode shift	-12V to 12V
Mux control logic thresholds	1.8V compatible, up to 48V
Mux temperature range	-40°C to +125°C

9.2.2 Detailed Design Procedure

The application shown in Figure 9-2 demonstrates how a multiplexer can be used to simplify the signal chain and monitor multiple input signals to a single ADC channel. In this example the ADC (ADS8661) has software programmable input ranges up to ±12.288V. The ADC also has overvoltage protection up to ±20V which allows for the multiplexer to be powered with wider supply voltages than the input signal range to maximize on resistance performance of the multiplexer, while still maintaining system level overvoltage protection beyond the useable signal range. Both the multiplexer and the ADC are capable of operation in extended temperature range of -40°C to +125°C allowing for use in a wider array of systems.

Many SAR ADCs have an analog input structure that consists of a sampling switch and a sampling capacitor. Many signal chains has a driver amplifier to help charge the input of the ADC to meet a fast system acquisition time. However a driver amplifier is not always needed to drive SAR ADCs. Figure 9-2 shows a typical diagram of a sensor driving the SAR ADC input directly after being passed through the multiplexer. A filter capacitor (C_{FLT}) is connected to the input of the ADC to reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitor of the ADC.

The sensor block simplifies the device into a Thevenin equivalent voltage source (V_{TH}) and resistance (R_{TH}) which can be extracted from the device datasheets. Similarly the multiplexer can be thought of as a series resistance ($R_{ON(MUX)}$) and capacitance ($C_{ON(MUX)}$). To ensure maximum precision of the signal chain the system must be able to settle within 1/2 of an LSB within the acquisition time of the ADC. The time constant can be calculated as shown in Figure 9-2. This equation highlights the importance of selecting a multiplexer with low on-resistance to further reduce the system time constant. Additionally low charge injection performance of the multiplexer is helpful to reduce conversion errors and improve accuracy of the measurements.

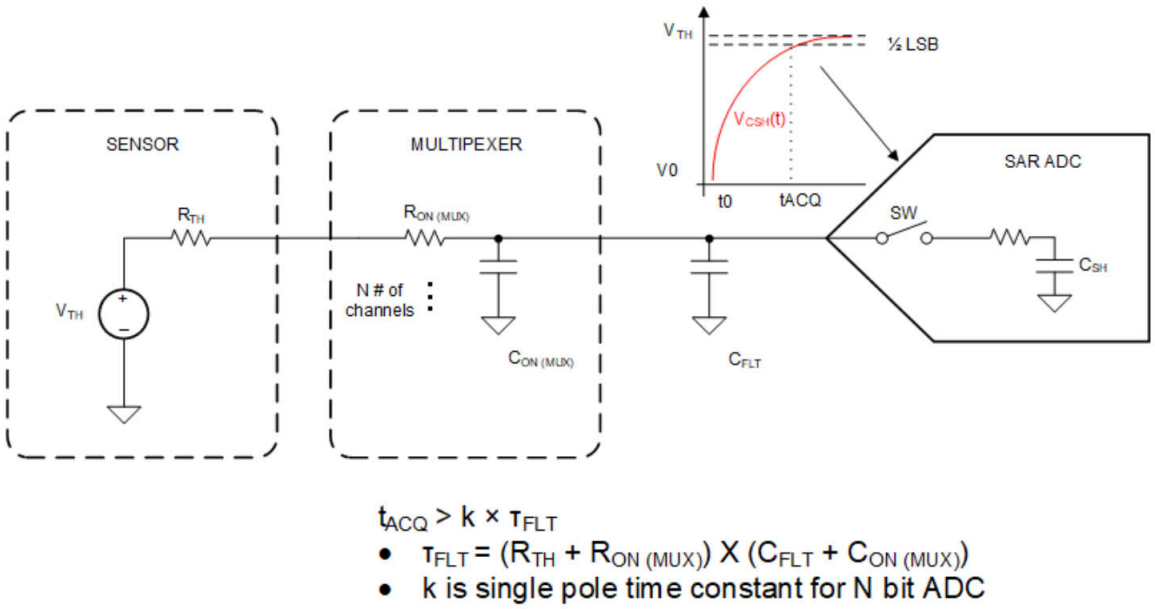
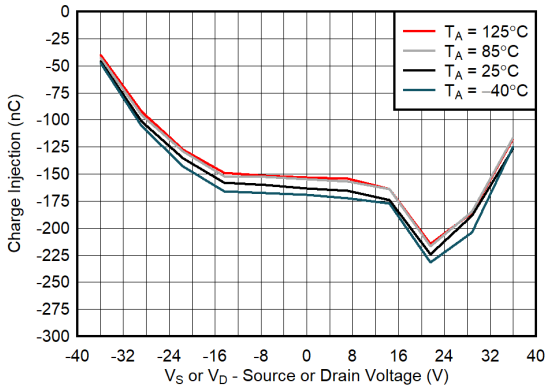


Figure 9-2. Driving SAR ADC

9.2.3 Application Curves

The low on and off leakage currents of MUX80x-Q1 and ultra-low charge injection performance make this device an excellent choice for implementing high precision automotive systems. The MUX80x-Q1 contains specialized architecture to reduce charge injection on the drain side (D). Figure 9-3 shows the plot for the charge injection versus source voltage for the MUX80x-Q1.



T_A = 25°C

Figure 9-3. Charge Injection vs Drain Voltage

9.3 Power Supply Recommendations

The MUX808-Q1 and MUX809-Q1 operate across a wide supply range of ±10V to ±50V (10V to 100V in single-supply mode). They also perform well with asymmetric supplies such as V_{DD} = 50V and V_{SS}= –10V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1µF to 10µF at both the V_{DD} and V_{SS} pins to ground. An additional 0.1µF capacitor placed closest to the supply pins will provide the best supply decoupling solution. Always ensure the ground (GND) connection is established before supplies are ramped.

9.4 Layout

9.4.1 Layout Guidelines

The following images illustrate an example of a PCB layout with the MUX808-Q1 and MUX809-Q1. Some key considerations are:

- For reliable operation, connect at least one decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and V_{SS} to GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

9.4.2 Layout Example

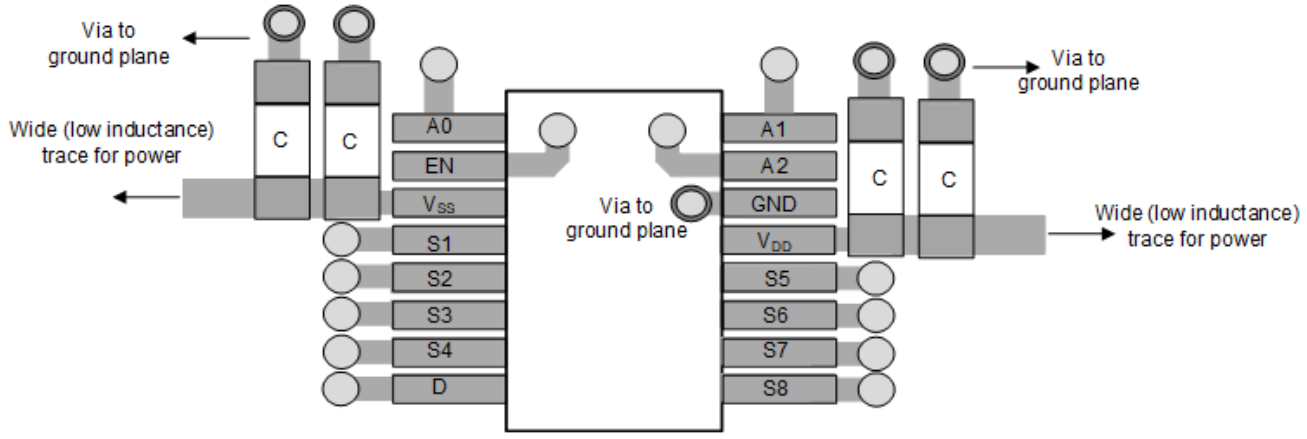


Figure 9-4. MUX808-Q1 TSSOP Layout Example

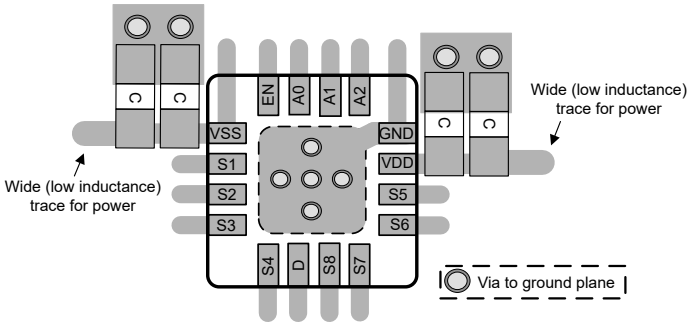


Figure 9-5. MUX808-Q1 QFN Layout Example

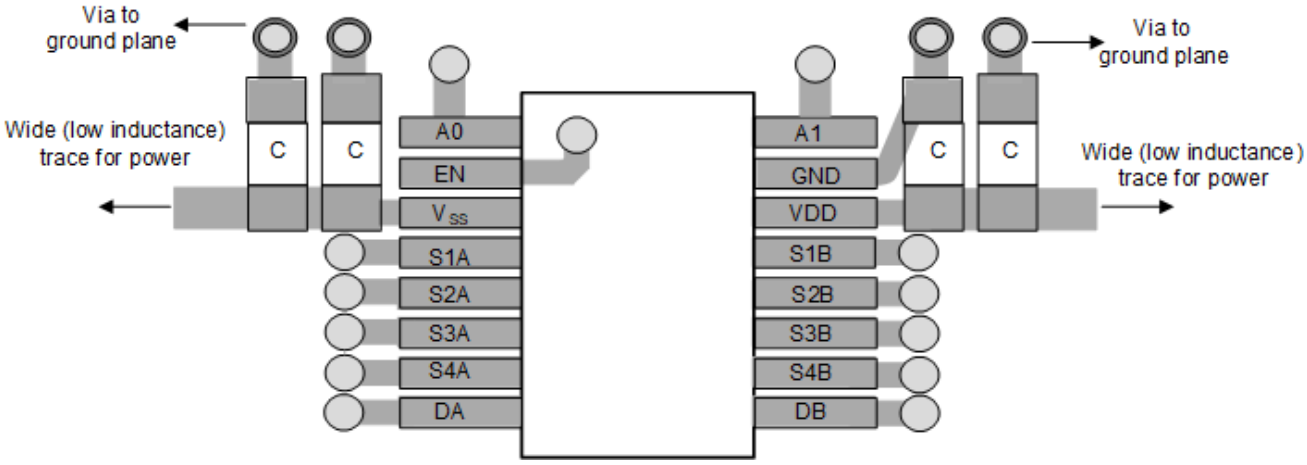


Figure 9-6. MUX809-Q1 TSSOP Layout Example

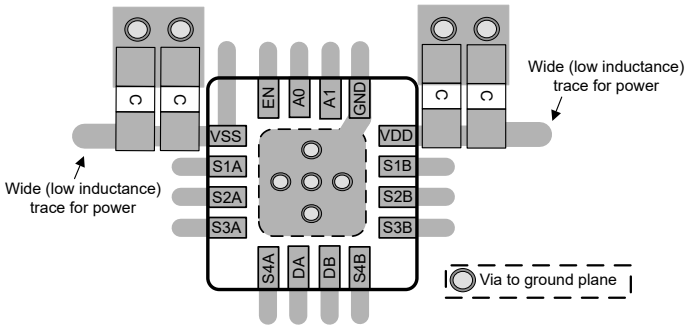


Figure 9-7. MUX809-Q1 QFN Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MUX808QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	808Q
MUX809QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	809Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

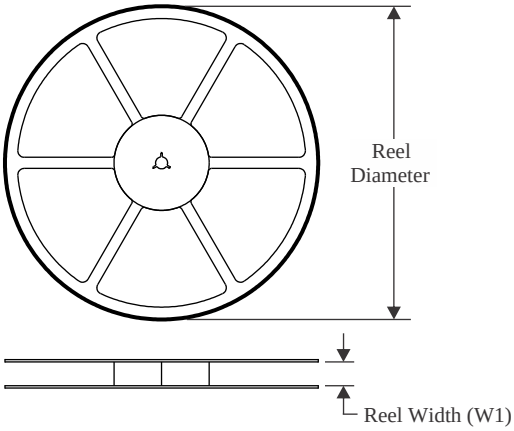
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

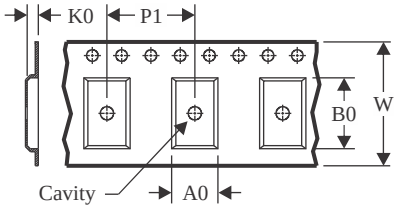
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

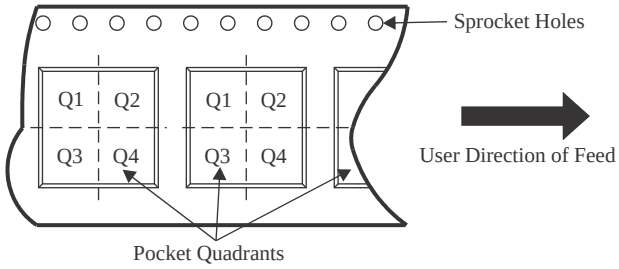


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

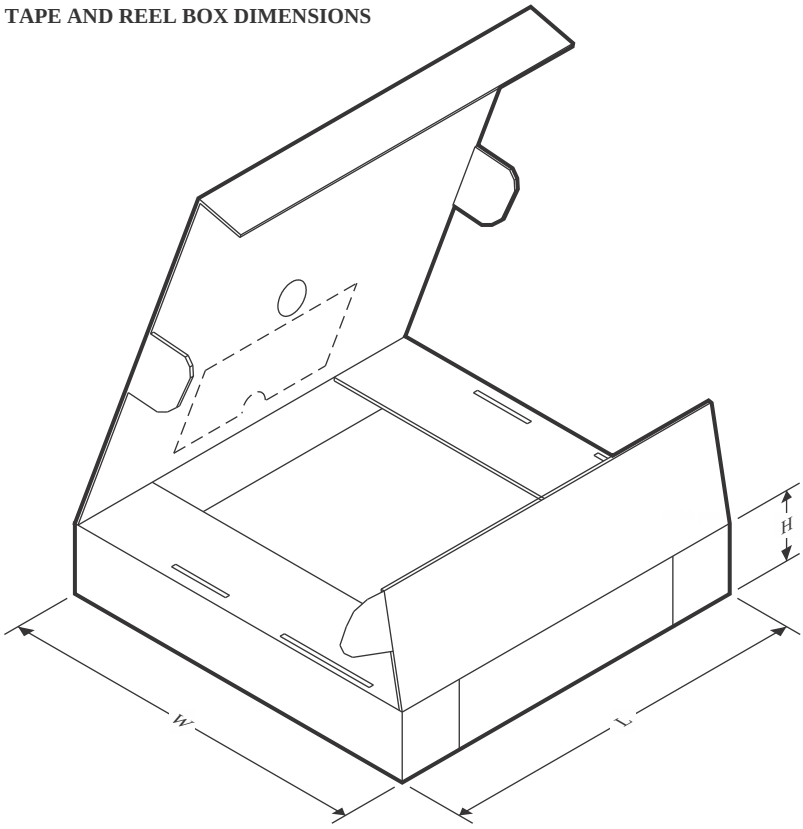
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MUX808QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX809QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

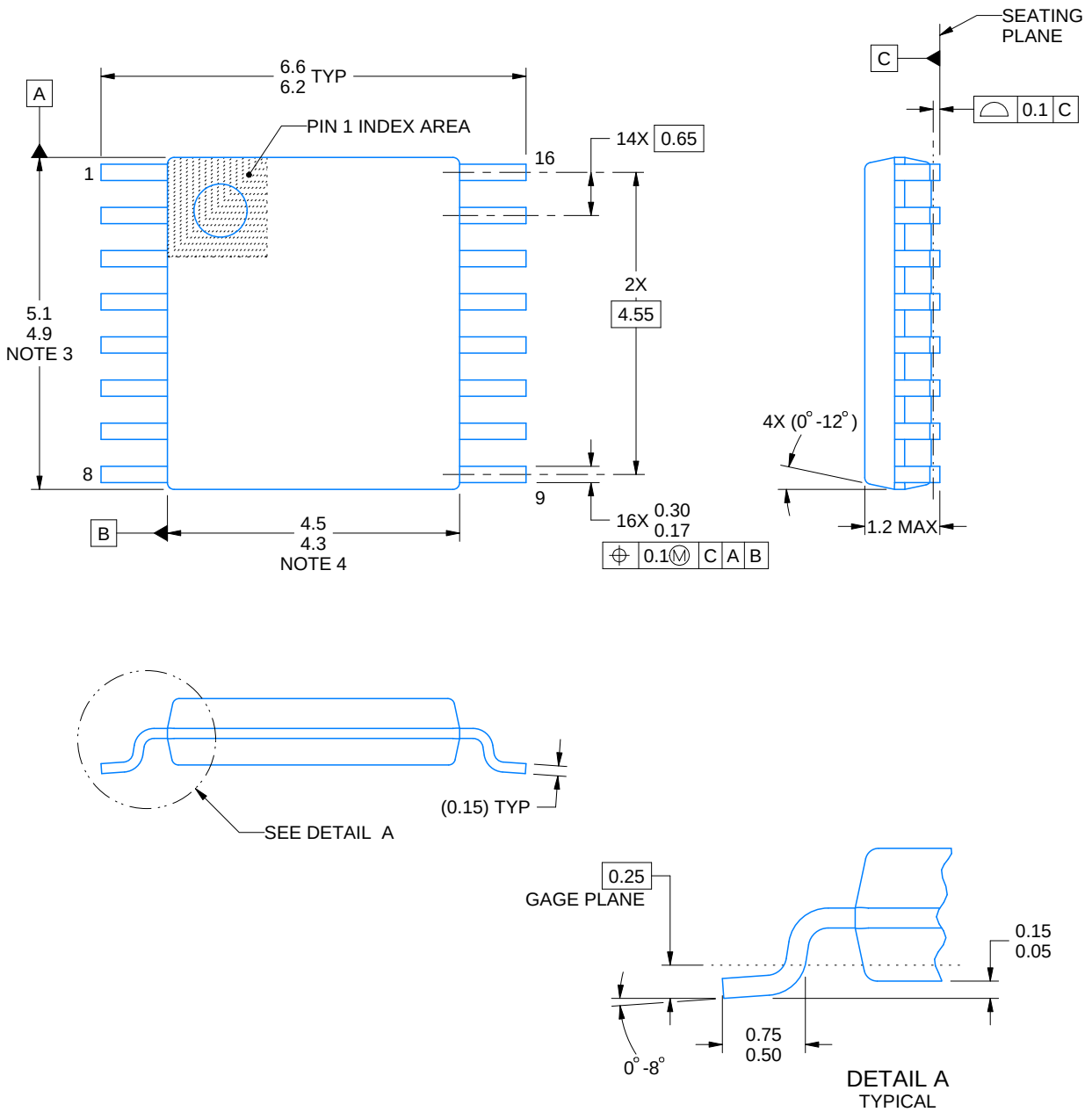
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MUX808QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
MUX809QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

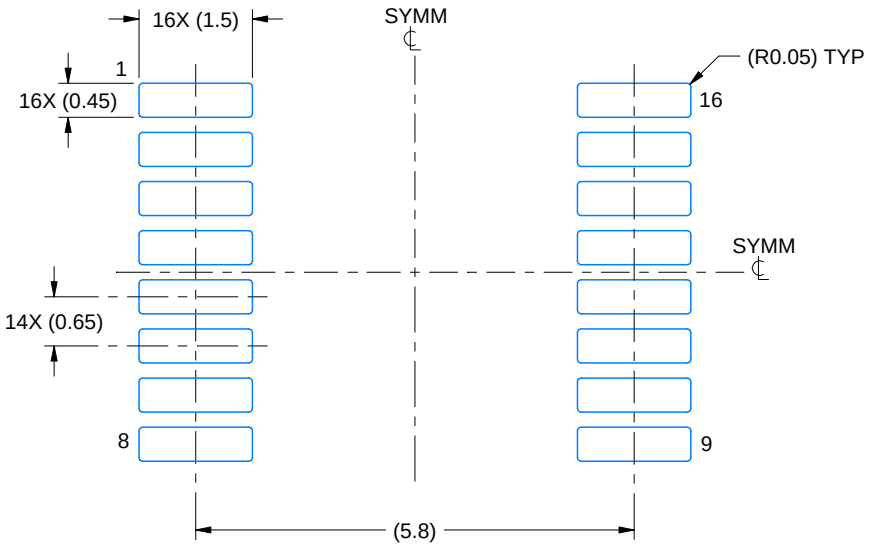
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



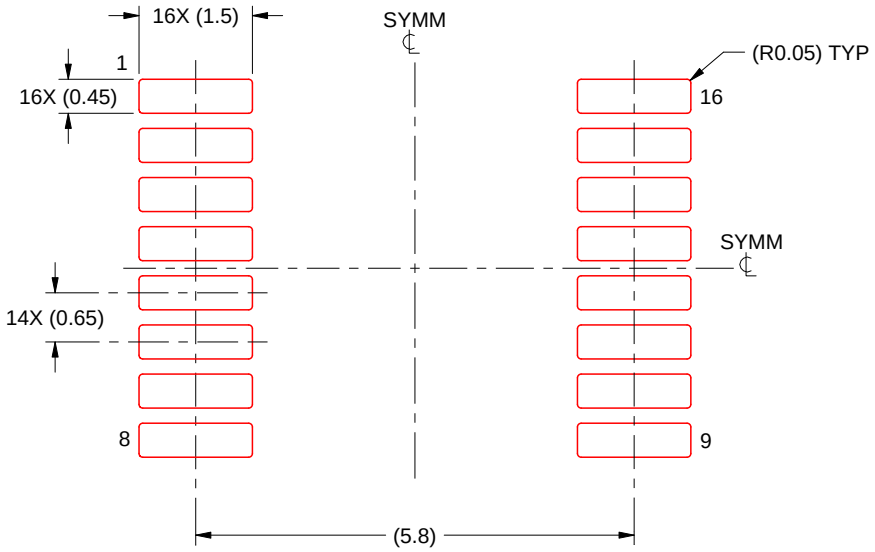
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025