11.3 Gbps Limiting Transimpedance Amplifier With RSSI

Check for Samples: ONET8531T

FEATURES

- **10 GHz Bandwidth**
- **4.5 kΩ Differential Small Signal Transimpedance**
- **2.5 mA_{p-p} Input Overload Current**
- **Received Signal Strength Indication (RSSI)**
- **100 mW Typical Power Dissipation**
- **CML Data Outputs With On-Chip 50 Ω Back-Termination**
- **On Chip Supply Filter Capacitor**
- **Single 3.3 V Supply**
- **Die Size: 940 × 1195 µm**
- **Case temperature operation: –40°C to 100°C**

APPLICATIONS

- **SONET OC-192**
- **SFP+ Optical Receivers**
- **10× Fibre Channel Optical Receivers**
- **10G Ethernet Receivers**
- **PIN Preamplifier-Receivers**
- **APD Preamplifier Receivers**

DESCRIPTION

The ONET8531T is a high-speed and high-gain limiting-transimpedance amplifier, used in optical receivers with data rates up to 12.5 Gbps. It features low input referred noise, 10 GHz bandwidth, 4.5 kΩ small signal transimpedance, and a received signal strength indicator (RSSI).

The ONET8531T is available in die form, includes an on-chip VCC bypass capacitor and is optimized for packaging in a TO can.

The ONET8531T requires a single +3.3V ± 10% supply and its power efficient design typically dissipates less than 105 mW. The device is characterized for operation from –40°C to 100°C case (IC back side) temperature.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

Figure 1 shows an ONET8531T block diagram. The ONET8531T consists of the signal path, supply filters, a control block for DC input bias, automatic gain control (AGC), and a received signal strength indicator (RSSI). The RSSI provides the bias for the TIA stage and the control for the AGC.

The signal path consists of a transimpedance amplifier stage, a voltage amplifier, and a CML output buffer. The on-chip filter circuit provides a filtered V_{CC} for the PIN photodiode and for the transimpedance amplifier.

The DC input bias circuit and automatic gain control use internal low pass filters to cancel the DC current on the input and to adjust the transimpedance amplifier gain. Additionally, the chip provides circuitry to monitor the received signal strength.

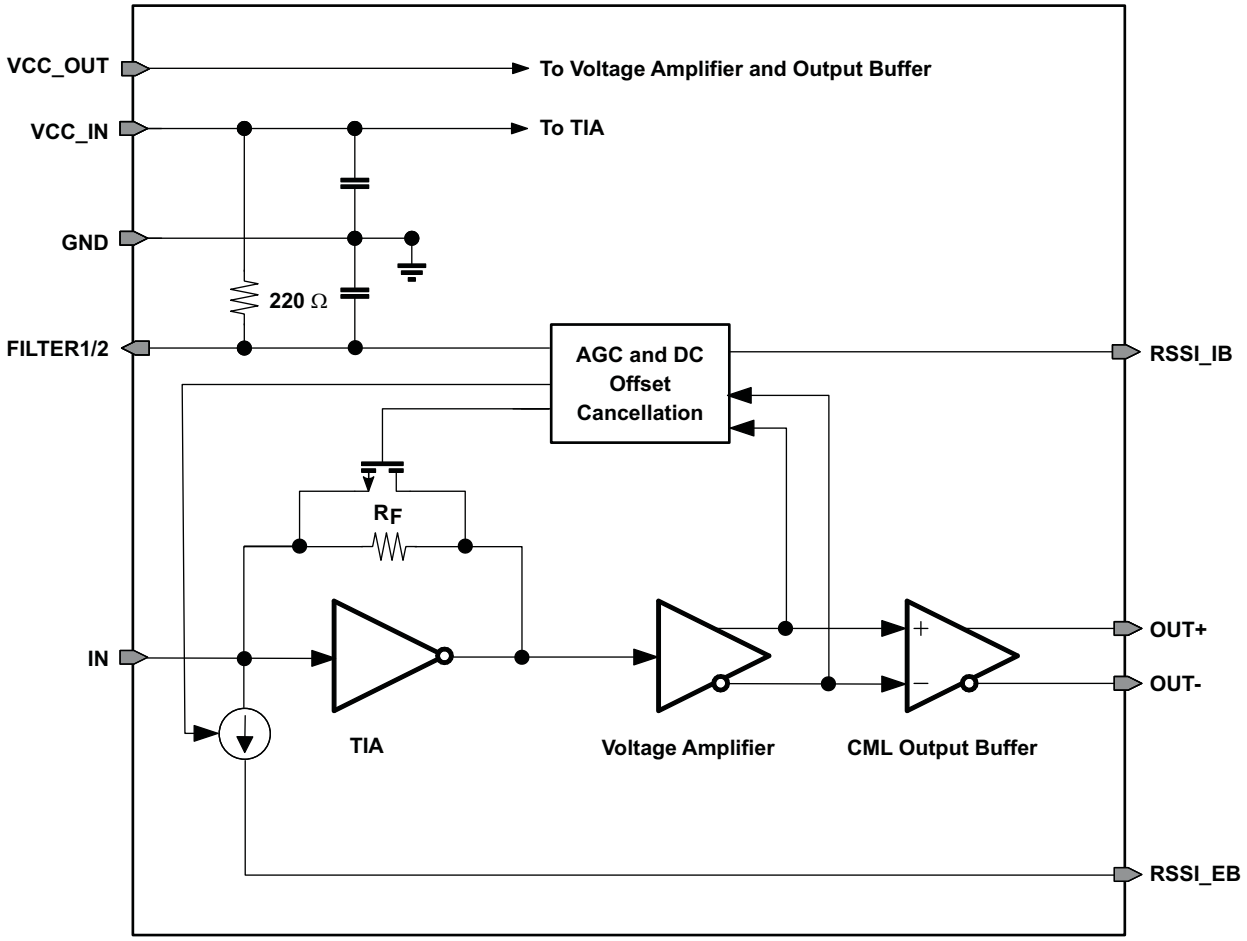


Figure 1. ONET8531T Block Diagram

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BOND PAD ASSIGNMENT

The ONET8531T is available in die form. The locations of the bond pads are shown in Figure 2.

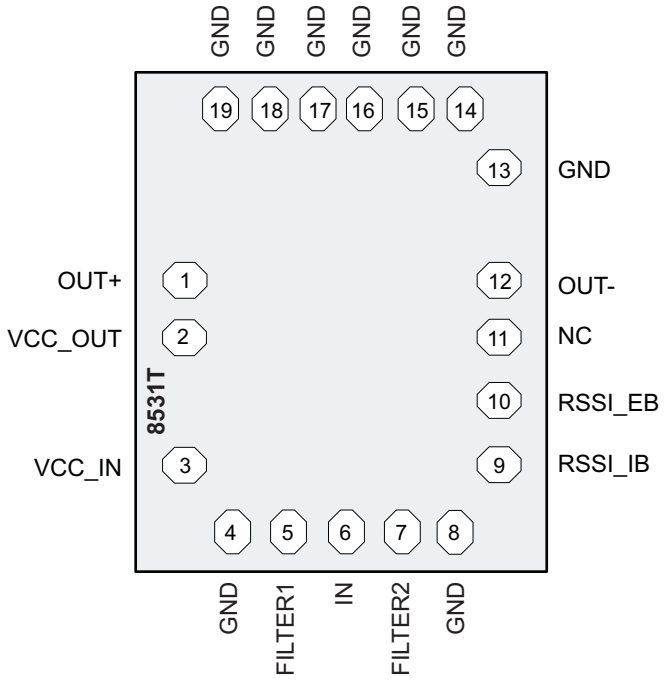


Figure 2. ONET8531T Bond Pad Assignment

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
FILTER	5, 7	Analog	Bias voltage for photodiode cathode. These pads are internally connected to an 220 Ω resistor to V_{CC} and a filter capacitor to ground (GND).
GND	4, 8, 13–19	Supply	Circuit ground. All GND pads are connected on die. Bonding all pads is optional; however for optimum performance a good ground connection is mandatory.
IN	6	Analog input	Data input to TIA (photodiode anode).
OUT+	1	Analog output	Non-inverted CML data output. On-chip 50 Ω back-terminated to V_{CC}.
OUT–	12	Analog output	Inverted CML data output. On-chip 50 Ω back-terminated to V_{CC}.
RSSI_EB	10	Analog output	Optional use when operated with external PD bias (for example, APD). Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI). Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V_{CC}–0.65 V. If the RSSI feature is not used, this pad should be left open.
RSSI_IB	9	Analog output	Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI) if the photo diode is biased from the TIA. Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V_{CC}–0.65 V. If the RSSI feature is not used, this pad should be left open.
VCC_IN	3	Supply	2.97 V to 3.63 V supply voltage for input TIA stage.
VCC_OUT	2	Supply	2.97 V to 3.63 V supply voltage for the voltage and CML amplifiers.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{CC_IN}, V_{CC_OUT}	Supply voltage (2)	–0.3 to 4.0	V
$V_{FILTER1}$, $V_{FILTER2}$, V_{OUT+}, $V_{OUT–}$, V_{RSSI_IB}, V_{RSSI_EB}	Voltage at FILTER1, FILTER2, OUT+, OUT–, RSSI_IB, RSSI_EB (2)	–0.3 to 4.0	V
I_{IN}	Current into IN	–0.7 to 3.5	mA
I_{FILTER}	Current into FILTER1, FILTER2	–8 to 8	mA
I_{OUT+}, $I_{OUT–}$	Continuous current at outputs	–8 to 8	mA
ESD	ESD rating at all pins except input IN, RSSI_IB and RSSI_EB	2	kV (HBM) (3)
	ESD rating at RSSI_IB and RSSI_EB	1	
	ESD rating at input IN	0.5	
$T_{J,max}$	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Human Body Model

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	2.97	3.3	3.63	V
T_A	Operating backside die temperature	–40		100 (1)	°C
L_{FILTER}, L_{IN}	Wire-bond inductor at pins FILTER1, FILTER2, and IN		0.3	0.5	nH
C_{PD}	Photodiode Capacitance		0.2		pF

(1) 105°C maximum junction temperature

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
I_{VCC}	Supply current	Input current I_{IN} < 1500 μA_{P-P}	21	28	41 (1)	mA
		Input current I_{IN} < 2500 μA_{P-P}			44 (1)	
V_{IN}	Input bias voltage		0.75	0.85	0.98	V
R_{OUT}	Output resistance	Single-ended to V_{CC}	40	50	60	Ω
R_{FILTER}	Photodiode filter resistance			220		Ω

(1) Includes RSSI current

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AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{21}	Small signal transimpedance	Differential output; Input current I_{IN} = 20 μA_{p-p}	2500	4500	6500	Ω
$f_{HSS,3dB}$	Small signal bandwidth	I_{IN} = 16 μA_{p-p} (1)	7	10		GHz
$f_{L,3dB}$	Low frequency –3 dB bandwidth	16 µA < I_{IN} < 2000 μA_{p-p}		30	100	kHz
$I_{N,IN}$	Input referred RMS noise	10 GHz bandwidth (2)		0.9	1.6	µA
S_{US}	Unstressed sensitivity optical	10.3125 Gbps, PRBS31 pattern, 850 nm, BER 10^{-12}		–14		dBm
DJ	Deterministic jitter	16 μA_{p-p} < I_{IN} < 500 μA_{p-p} (10.3125 Gbps, PRBS31 pattern)		6	11	ps_{p-p}
		500 μA_{p-p} < I_{IN} < 2000 μA_{p-p} (10.3125 Gbps, PRBS31 pattern)		6	13	
DJ_{OL}	Overload deterministic jitter	2000 μA_{p-p} < I_{IN} < 2500 μA_{p-p} (K28.5 pattern)		6	15	ps_{p-p}
$V_{OUT,D,MAX}$	Maximum differential output voltage	Input current I_{IN} = 200 μA_{p-p}	240	280	350	mV_{p-p}
A_{RSSI_IB}	RSSI gain internal bias	Resistive load to GND (3)	0.48	0.5	0.52	A/A
	RSSI internal bias output offset current (no light) (4)		3.5	10	16	µA
A_{RSSI_EB}	RSSI gain external bias	Resistive load to GND (3)	0.43		0.6	A/A
	RSSI external bias output offset current (no light)			25		µA
PSNR	Power supply noise rejection	F < 10 MHz (5), supply filtering according to SFF8431		–15		dB

(1) The small signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.2 pF and the bond-wire inductance is 0.3 nH. The small signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.
(2) Input referred RMS noise = (RMS output noise) ÷ (gain at 100 MHz).
(3) The RSSI output is a current output, which requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation, ensure that the voltage at RSSI does not exceed V_{CC}–0.65 V.
(4) Offset is added to improve accuracy below 5 µA. When measured without input current (no light) the offset can be subtracted as a constant offset from RSSI measurements.
(5) PSNR is the differential output amplitude divided by the voltage ripple on supply; no input current at IN.

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DETAILED DESCRIPTION

SIGNAL PATH

A transimpedance amplifier serves as the signal path first stage that converts the photodiode current into a voltage. If the input signal current exceeds a certain value, the transimpedance gain is reduced by means of a nonlinear AGC circuit to limit the signal amplitude.

The second stage is a limiting voltage amplifier that provides additional limiting gain and converts the single ended input voltage into a differential data signal. The output stage provides CML outputs with an on-chip 50 Ω back-termination to V_{CC}.

FILTER CIRCUITRY

The FILTER pins provide a filtered VCC for a PIN photodiode bias. The on-chip low pass filter for the photodiode is implemented using a filter resistor of 220 Ω and a capacitor. The corresponding corner frequency is below 5 MHz. The supply voltages for the transimpedance amplifier are filtered by means of on-chip capacitors, thus avoiding the need for an external supply filter capacitor. The input stage has a separate VCC supply (VCC_IN) that is not connected on the chip to the supply of the limiting and CML stages (VCC_OUT).

AGC AND RSSI

The voltage drop across the internal photodiode supply-filter resistor is monitored by the bias and RSSI control circuit block, in the situation where a PIN diode is biased using the FILTER pins.

If the DC input current exceeds a specified level then it is partially cancelled by means of a controlled current source. This keeps the transimpedance amplifier stage within sufficient operating limits for optimum performance. The automatic gain control circuitry adjusts the voltage gain of the AGC amplifier to ensure limiting behavior of the complete amplifier.

Finally, this circuit block senses the current through the filter resistor and generates a mirrored current that is proportional to the input signal strength. The mirrored current is available at the RSSI_IB output and can be sunk to ground (GND) using an external resistor. For proper operation, ensure that the voltage at the RSSI_IB pad does not exceed VCC-0.65 V.

If an APD or PIN photodiode is used with an external bias then the RSSI_EB pin should be used. However, for greater accuracy under external photo diode biasing conditions, it is recommended to derive the RSSI from the external bias circuitry.

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TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = +3.3V and T_A = +25°C (unless otherwise noted).

TRANSIMPEDANCE vs INPUT CURRENT

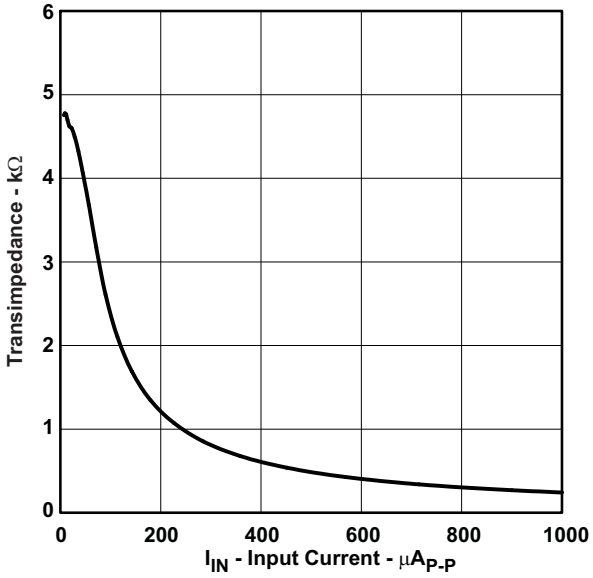


Figure 3.

SMALL SIGNAL TRANSIMPEDANCE vs AMBIENT TEMPERATURE

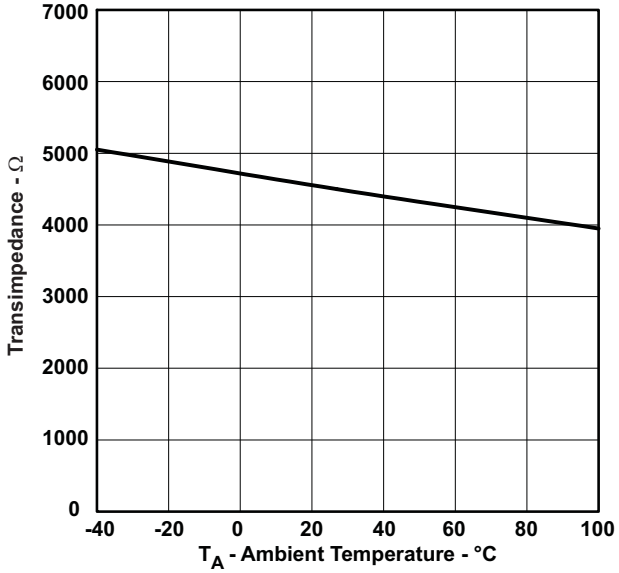


Figure 4.

SMALL SIGNAL TRANSFER CHARACTERISTICS

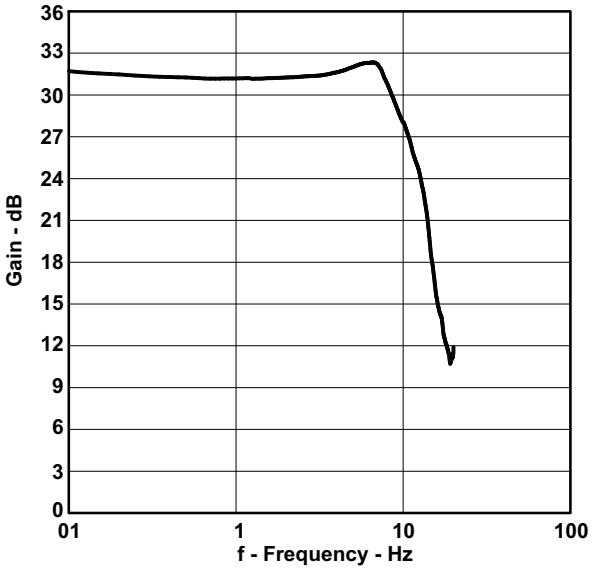


Figure 5.

SMALL SIGNAL BANDWIDTH vs AMBIENT TEMPERATURE

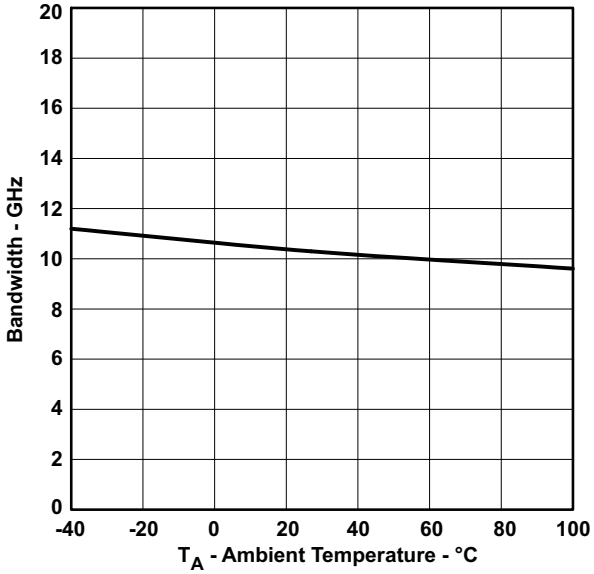


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = +3.3V and T_A = +25°C (unless otherwise noted).

OUTPUT VOLTAGE vs INPUT CURRENT

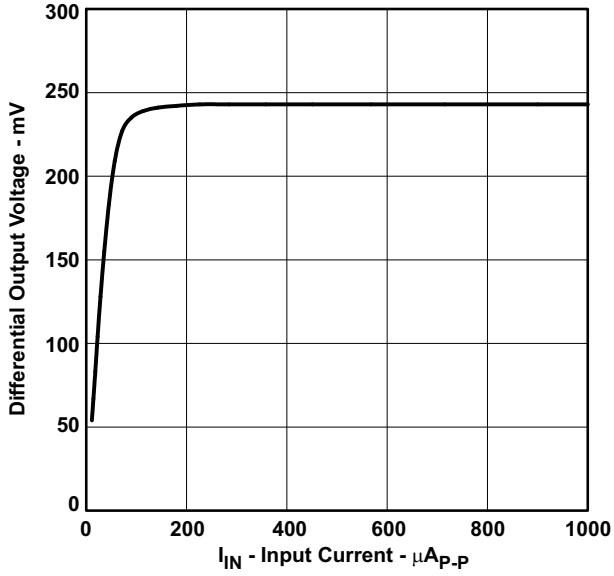


Figure 7.

DETERMINISTIC JITTER vs INPUT CURRENT

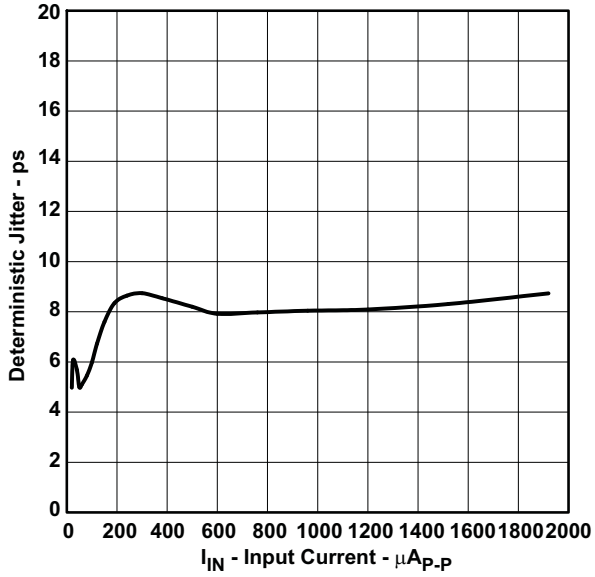


Figure 8.

RSSI_IB OUTPUT CURRENT vs AVERAGE INPUT CURRENT

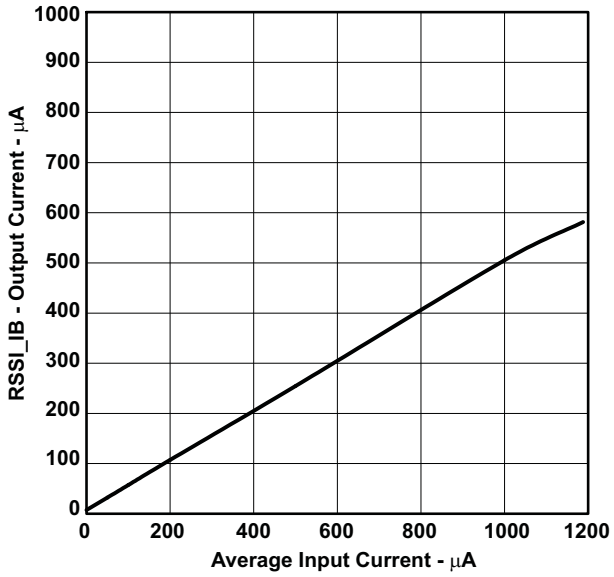


Figure 9.

POWER SUPPLY NOISE REJECTION vs FREQUENCY

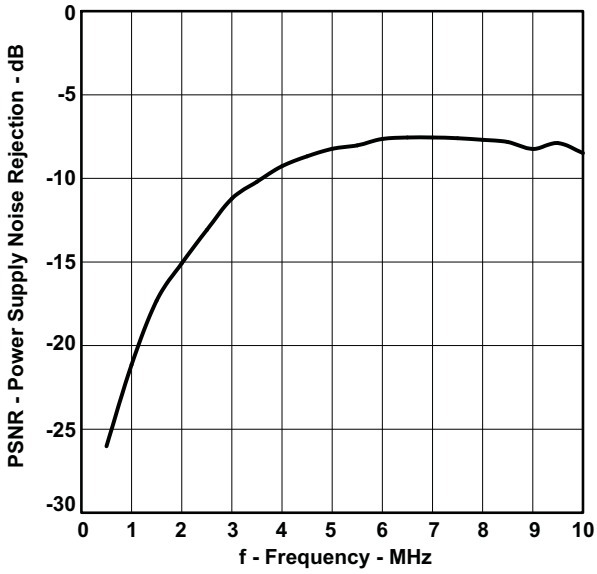


Figure 10.

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TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = +3.3V and T_A = +25°C (unless otherwise noted).

OUTPUT EYE-DIAGRAM AT 10.3 GBPS and 20 μA_{p-p} INPUT CURRENT

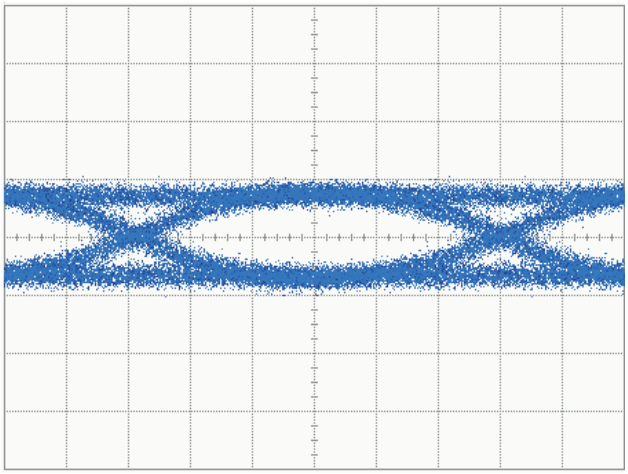


Figure 11.

OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 100 μA_{p-p} INPUT CURRENT

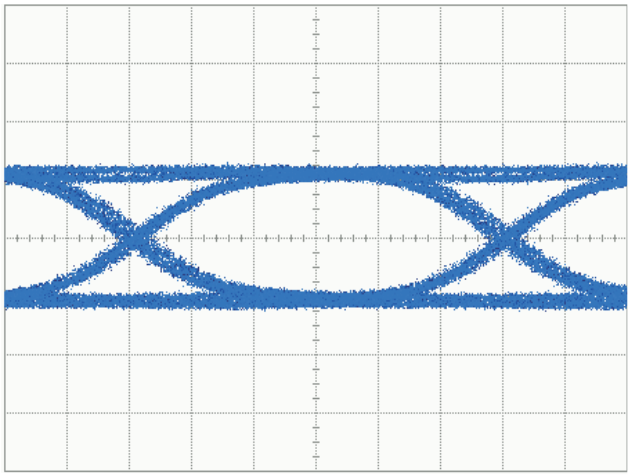


Figure 12.

OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 500 μA_{p-p} INPUT CURRENT

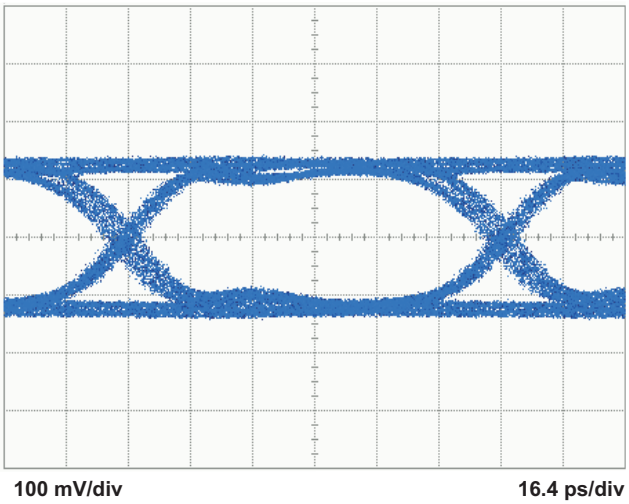


Figure 13.

OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 2000 μA_{p-p} INPUT CURRENT

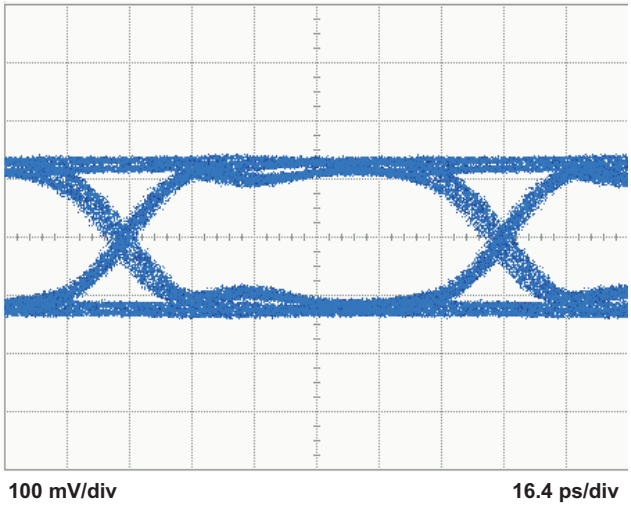


Figure 14.

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APPLICATION INFORMATION

Figure 15 shows the ONET8531T being used in a typical fiber optic receiver circuit using the internal photodiode bias. The ONET8531T converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTER inputs provide a DC bias voltage for the PIN that is low pass filtered by the combination of an internal 220 Ω resistor and a capacitor. Because the voltage drop across the 220 Ω resistor is sensed and used by the bias circuit, the photodiode must be connected to the FILTER pads for the bias to function correctly.

The RSSI output is used to mirror the photodiode output current and can be connected using a resistor to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation of the ONET8531T, ensure that the voltage at RSSI never exceeds V_{CC}–0.65 V. The RSSI output should be left open if it is not used while operating with internal PD bias.

The OUT+ and OUT– pins are internally terminated by 50 Ω pull-up resisters to VCC. The outputs must be AC coupled, for example by using 0.1 µF capacitors, to the succeeding device.

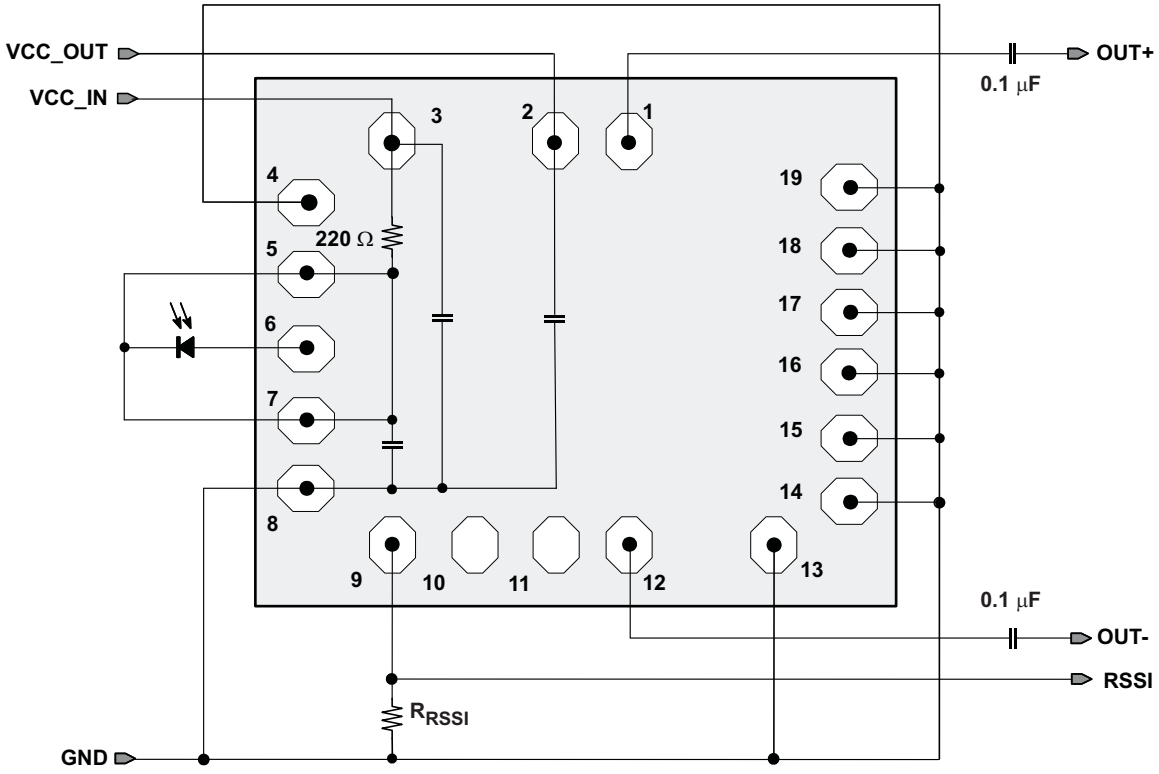


Figure 15. Basic Application Circuit for PIN Receivers

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Figure 16 shows the ONET8531T being used in a typical fiber optic receiver circuit using an external photodiode bias for an APD photodiode. This configuration can also be used for a PIN diode. The external bias RSSI signal is based on a DC offset value and is not as accurate as the internal bias RSSI signal, which is based upon the photodiode current.

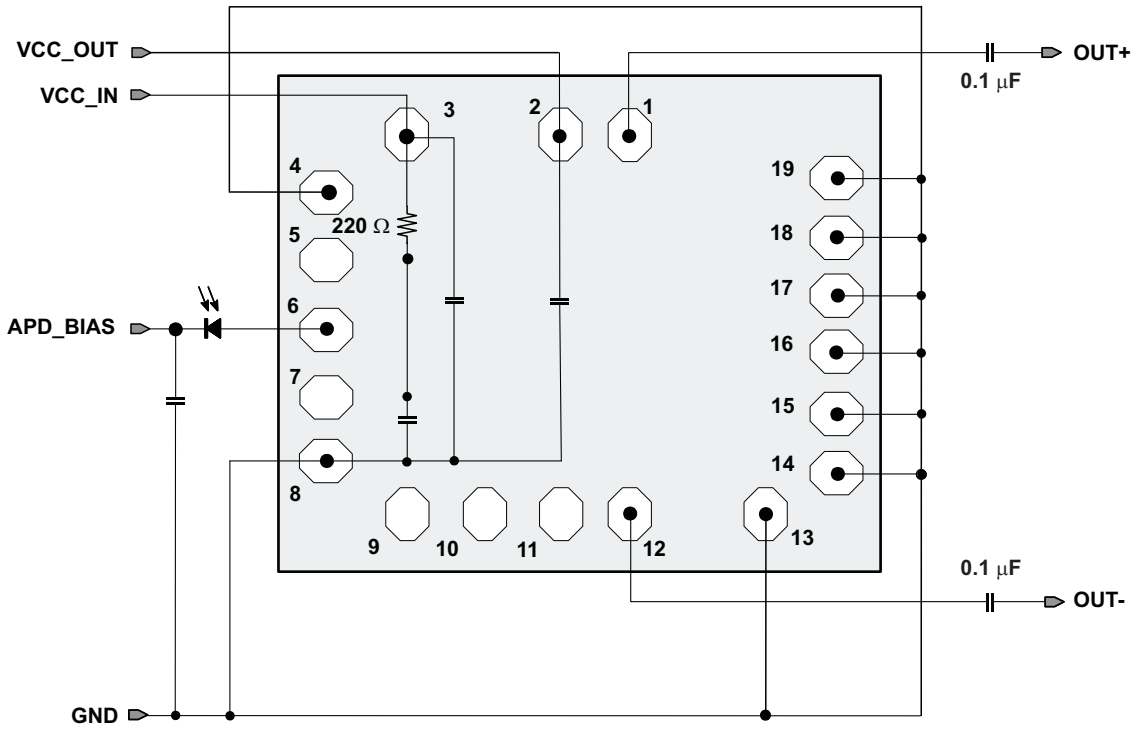


Figure 16. Basic Application Circuit for APD Receivers

ASSEMBLY RECOMMENDATIONS

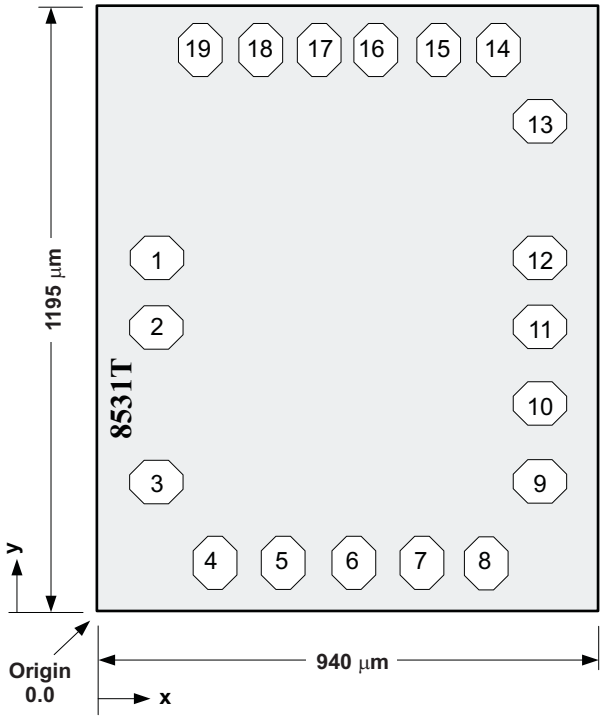
You need to concentrate on assembly parasitics and external components to achieve optimal performance.

Recommendations that optimize performance include:

1. Minimize the total capacitance on the IN pad by using a low capacitance photodiode and compensating for stray capacitances. Place the photodiode close to the ONET8531T die in order to minimize the bond wire length and associated parasitic inductance.
2. Use identical termination and symmetrical transmission lines at the AC coupled differential output pins OUT+ and OUT–.
3. Use short bond wire connections for the supply terminals VCC_IN, VCC_OUT and GND. Supply voltage filtering is provided on chip but filtering may be improved by using an additional external capacitor.

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CHIP DIMENSIONS AND PAD LOCATIONS



Die Thickness: 203 ± 13 µm

Pad Dimensions: 105 × 65 µm

Die Size: 940 ± 40 µm × 1195 ± 40 µm

Table 1. Bond Pad Locations and Descriptions

PAD	COORDINATES (based on typical die size)		SYMBOL	TYPE	DESCRIPTION
	x (µm)	y (µm)			
1	116	739	OUT+	Analog output	Non-inverted data output
2	116	575	VCC_OUT	Supply	3.3V supply voltage
3	116	289	VCC_IN	Supply	3.3V supply voltage
4	243	136	GND	Supply	Circuit ground
5	358	136	FILTER1	Analog	Bias voltage for photodiode
6	473	136	IN	Analog input	Data input to TIA
7	588	136	FILTER2	Analog	Bias voltage for photodiode
8	703	136	GND	Supply	Circuit ground
9	828	289	RSSI_IB	Analog output	RSSI output signal for internally biased receivers
10	828	404	RSSI_EB	Analog output	RSSI output signal for externally biased receivers
11	828	575	NC		Not connected
12	828	739	OUT–	Analog output	Inverted data output
13	828	910	GND	Supply	Circuit ground
14	760	1063	GND	Supply	Circuit ground
15	645	1063	GND	Supply	Circuit ground
16	530	1063	GND	Supply	Circuit ground
17	415	1063	GND	Supply	Circuit ground
18	300	1063	GND	Supply	Circuit ground
19	185	1063	GND	Supply	Circuit ground

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TO46 LAYOUT EXAMPLE

An example for a layout (top view) in a 5-pin TO46 can is shown in Figure 17.

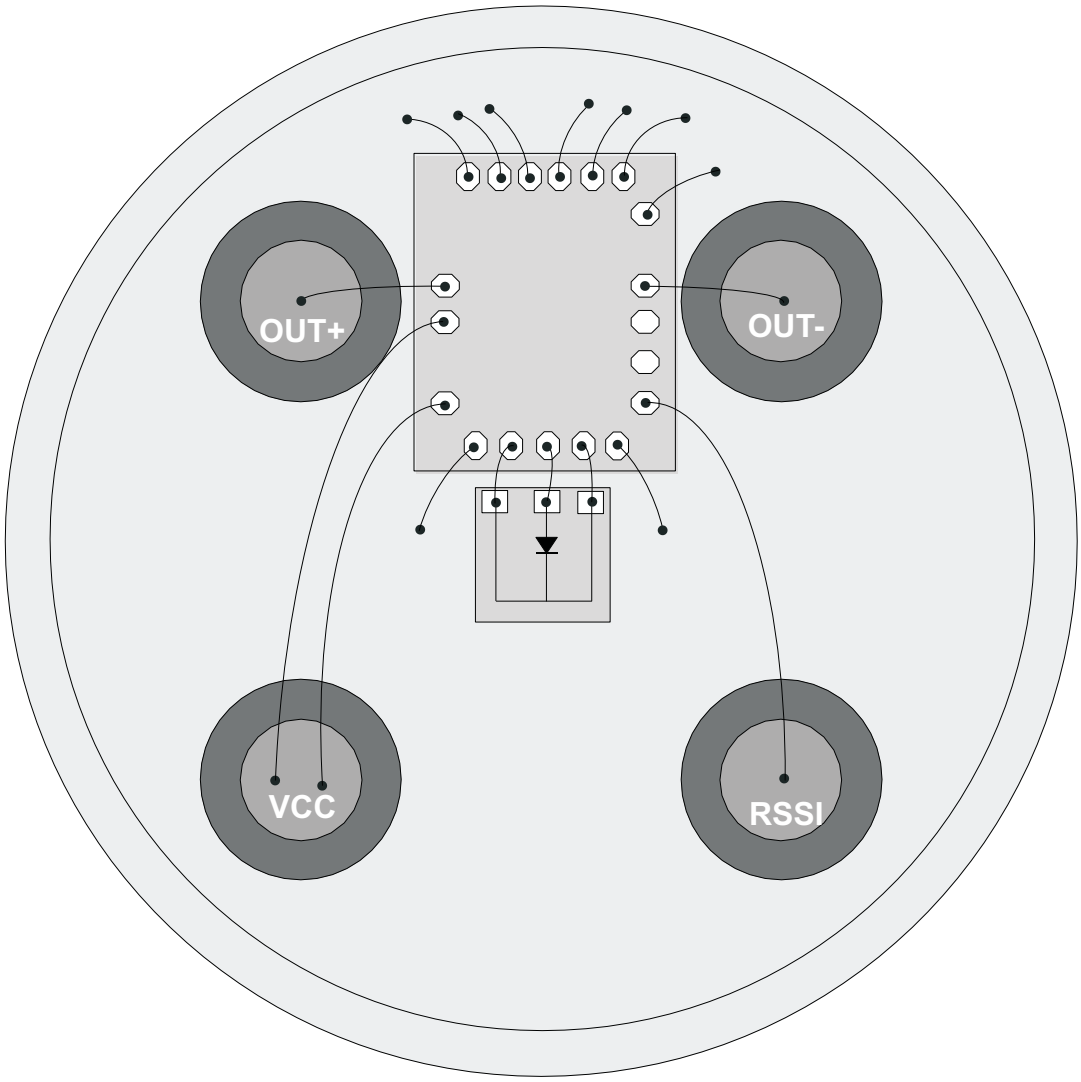


Figure 17. TO46 5 Pin Layout Using the ONET8531T With Dual Cathode PIN Diode

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REVISION HISTORY

Changes from Original (February 2008) to Revision A **Page**

- Changed Features bullet From: Die Size 945 x 1200 µm To: Die Size: 940 × 1195 µm 1
- Changed the CHIP DIMENSIONS AND PAD LOCATIONS image. Y = 1200 µm To: 1195 µm and X = 945 µm To: 940 µm 12
- Added Die Thickness, Pad Dimensions, and Die Size 12

Changes from Revision A (January 2010) to Revision B **Page**

- Changed From: Die Size: 940 ± 20 µm × 1195 ± 20 µm To: Die Size: 940 ± 40 µm × 1195 ± 40 µm 12
- Added the Coordinates column to include " (based on typical die size)" 12

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ONET8531TY	Active	Production	DIESALE (Y) | 0	1800 | JEDEC TRAY (10+1)	-	Call TI	Call TI	0 to 0	
ONET8531TY.A	Active	Production	DIESALE (Y) | 0	1800 | JEDEC TRAY (10+1)	-	Call TI	Call TI	0 to 0	
ONET8531TYS9	Active	Production	DIESALE (Y) | 0	1 | OTHER	-	Call TI	Call TI	-40 to 100	
ONET8531TYS9.A	Active	Production	DIESALE (Y) | 0	1 | OTHER	-	Call TI	Call TI	-40 to 100	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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