OPAx354 250MHz, Rail-to-Rail I/O, CMOS Operational Amplifiers

1 Features

- Unity-gain bandwidth: 250MHz
- Wide bandwidth: 100MHz GBW
- High slew rate: 150V/µs
- Low noise: 6.5nV√Hz
- Rail-to-rail I/O
- High output current: > 100mA
- Excellent video performance:
  - Differential gain: 0.02%, differential phase: 0.09°
  - 0.1dB gain flatness: 40MHz
- Low input bias current: 3pA
- Quiescent current: 5mA
- Thermal shutdown
- Supply range: 2.5V to 5.5V
- *Micro*SIZE and PowerPAD™ integrated circuit packages

2 Applications

- Video processing
- Ultrasound
- Optical networking, tunable laser
- Photodiode transimpedance amplifier
- Active filter
- High-speed integrator
- Analog-to-digital converter (ADC) input buffer
- Digital-to-analog converter (DAC) output amplifier
- Barcode scanner
- Communications

3 Description

The OPAx354 series of high-speed, voltage-feedback CMOS operational amplifiers is designed for video and other applications requiring wide bandwidth. These devices are unity-gain stable and drive large output currents. Differential gain is 0.02% and differential phase is 0.09°. Quiescent current is only 5mA per channel.

The OPAx354 series of op amps is optimized for operation on single or dual supplies as low as 2.5V (±1.25V) and up to 5.5V (±2.75V). Common-mode input range extends beyond the supplies. The output swing is within 100mV of the rails, supporting a wide dynamic range.

For applications requiring the full 100mA of continuous output current, single and dual 8-pin HSOIC (SO PowerPAD) versions are available.

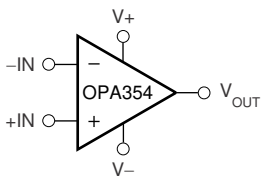
The single version (OPA354) is available in tiny 5-pin SOT-23 and 8-pin HSOIC (SO PowerPAD) packages. The dual version (OPA2354) comes in miniature 8-pin VSSOP and 8-pin HSOIC (SO PowerPAD) packages. The quad version (OPA4354) is offered in 14-pin TSSOP and 14-pin SOIC packages.

Multichannel version features completely independent circuitry for lowest crosstalk and freedom from interaction. All features are specified over the extended –40°C to +125°C temperature range.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
OPA354	Single	DDA (HSOIC, 8)
		DBV (SOT-23, 5)
OPA2354	Dual	DGK (VSSOP, 8)
		DDA (HSOIC, 8)
OPA4354	Quad	D (SOIC, 14)
		PW (TSSOP, 14)

(1) For more information, see Section 11.



Simplified Schematic

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4 Device Comparison Table

FEATURES	PRODUCT
100MHz GBW, RRIO, e-trim™	OPAx620
Shutdown version of OPAx354 family	OPAx357
200MHz GBW, rail-to-rail output, CMOS, shutdown	OPAx355
200MHz GBW, rail-to-rail output, CMOS	OPAx356
38MHz GBW, rail-to-rail input/output, CMOS	OPAx350/OPAx353
75MHz BW G = 2, rail-to-rail output	OPA2631
150MHz BW G = 2, rail-to-rail output	OPA2634
100MHz BW, differential input/output, 3.3V supply	THS412x

5 Pin Configuration and Functions

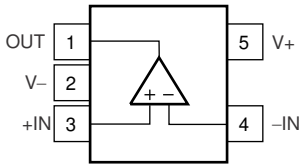


Figure 5-1. OPA354: DBV Package, 5-Pin SOT-23 (Top View)

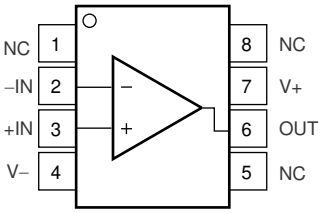


Figure 5-2. OPA354: DDA Package, 8-Pin HSOIC (Top View)

Table 5-1. Pin Functions: OPA354

PIN			TYPE	DESCRIPTION
NAME	DBV (SOT-23)	DDA (HSOIC)		
–IN	4	2	Input	Inverting input
+IN	3	3	Input	Noninverting input
NC	—	1, 5, 8	—	No internal connection (float this pin)
OUT	1	6	Output	Output
V–	2	4	—	Negative (lowest) supply
V+	5	7	—	Positive (highest) supply
Thermal pad	—	Pad	—	Thermal pad must be connected to V− or floated.

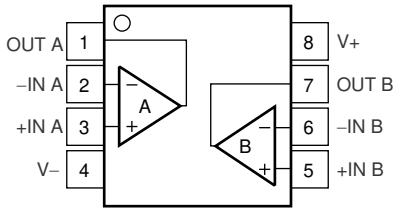


Figure 5-3. OPA2354: DGK Package, 8-Pin VSSOP, and DDA Package, 8-Pin HSOIC (Top View)

Table 5-2. Pin Functions: OPA2354

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V–	4	—	Negative (lowest) supply
V+	8	—	Positive (highest) supply
Thermal pad	pad		DDA package only. Connect thermal pad to V− or float.

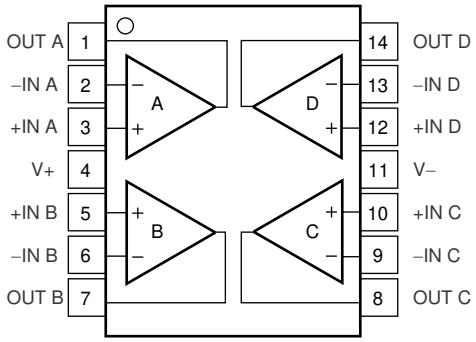


Figure 5-4. OPA4354: D Package, 14-Pin SOIC, and PW Package, 14-Pin TSSOP (Top View)

Table 5-3. Pin Functions: OPA4354

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V–	11	—	Negative (lowest) supply
V+	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		7.5	V
V_I	Signal input terminals	(V–) – 0.5	(V+) + 0.5	V
I_I	Signal input terminals	–10	+10	mA
I_{SC}	Output short-circuit(2)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.5		5.5	V
T_A	Specified temperature	–40	25	125	°C

6.4 Thermal Information OPA354

THERMAL METRIC(1)		OPA354		UNIT
		DBV (SOT-23)	DDA (HSOP)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.3	106.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115.0	121.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.2	79.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	50.3	57.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.7	79.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	64.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information OPA2354

THERMAL METRIC[1]		OPA2354		UNIT
		DDA (HSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	87	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	9.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	86.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information OPA4354

THERMAL METRIC[1]		OPA4354		UNIT
		D (SOIC)	PW(TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	102.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	35.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	57.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	6.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	56.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at T_A = 25°C, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5V, T_A = 25°C		±2	±8	mV
		V_S = 5V, T_A = –40°C to +125°C			±10	mV
dV_{OS}/dT	Input offset voltage drift	V_S = 5V, T_A = –40°C to +125°C		±4		µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7V to 5.5V, V_{CM} = (V_S / 2) − 0.55V		±200	±800	µV/V
		V_S = 2.7V to 5.5V, V_{CM} = (V_S / 2) – 0.55V, T_A = –40°C to +125°C			±900	
INPUT BIAS CURRENT						
I_B	Input bias current(2)			3	±50	pA
I_{OS}	Input offset current(2)			±1	±50	
NOISE						
en	Input voltage noise density	f = 1MHz		6.5		nV/√Hz
i_n	Input current noise density	f = 1MHz, for OPA2354, OPA4354		50		fA/√Hz
		f = 1MHz, for OPA354		300		
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5V, –0.1V < V_{CM} < 3.5V, T_A = 25°C	66	80		dB
		V_S = 5.5V, –0.1V < V_{CM} < 3.5V, T_A = –40°C to +125°C	64			
		V_S = 5.5V, –0.1V < V_{CM} < 5.6V, T_A = 25°C	56	68		
		V_S = 5.5V, –0.1V < V_{CM} < 5.6V, T_A = –40°C to +125°C	55			
INPUT IMPEDANCE						
C_{IN}	Differential			10^{13} || 2		Ω || pF
	Common-mode			10^{13} || 2		
OPEN-LOOP GAIN						
A_{OL}	Open-loop gain	V_S = 5.5V, 0.3V < V_O < 4.7V, T_A = 25°C	94	110		dB
		V_S = 5.5V, 0.4V < V_O < 4.6V, T_A = –40 to +125°C	90			
FREQUENCY RESPONSE						
$f_{–3dB}$	Gain-bandwidth product	G = +1, V_O = 100mV_{PP}, R_F = 25Ω		250		MHz
		G = +2, V_O = 100mV_{PP}		90		
GBW	Gain-bandwidth product	G = +10		100		MHz
$f_{0.1dB}$	Bandwidth for 0.1dB gain flatness	G = +2, V_O = 100mV_{PP}		40		MHz
SR	Slew rate	V_S = 5V, G = +1, 4V step		150		V/µs
		V_S = 5V, G = +1, 2V step		130		
		V_S = 3V, G = +1, 2V step		110		
	Rise-and-fall time	G = +1, V_O = 200mV_{PP}, 10% to 90%, for OPA2354, OPA4354		2		ns
		G = +1, V_O = 200mV_{PP}, 10% to 90%, for OPA354		3		
		G = +1, V_O = 2V_{PP}, 10% to 90%		11		
t_S	Settling time	0.1%, V_S = 5V, G = +1, 2V output step		30		ns
		0.01%, V_S = 5V, G = +1, 2V output step		60		
	Overload recovery time	V_{IN} × G = V_S		5		ns

6.7 Electrical Characteristics (continued)

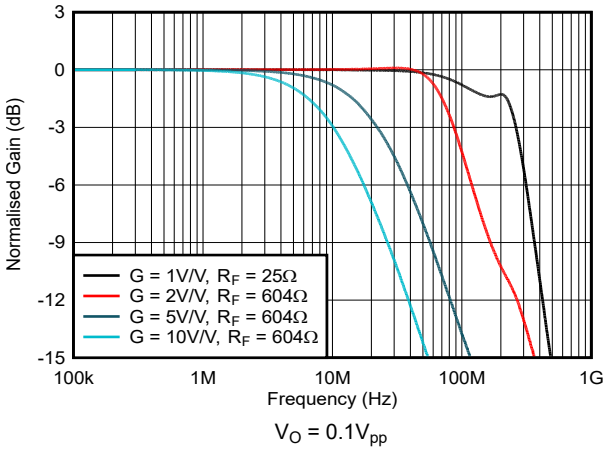
at T_A = 25°C, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	Second-order harmonic distortion	G = +1, f = 1MHz, V_O = 2V_{PP}, R_L = 200Ω, V_{CM} = (V–) + 1.5V		–75		dBc
HD3	Third-order harmonic distortion	G = +1, f = 1MHz, V_O = 2V_{PP}, R_L = 200Ω, V_{CM} = (V–) + 1.5V		-83		dBc
	Differential gain error	NTSC, R_L = 150Ω		0.02%		
	Differential phase error	NTSC, R_L = 150Ω		0.09		°
	Channel-to-channel crosstalk	OPA2354, f = 5MHz		–100		dB
	Channel-to-channel crosstalk	OPA4354, f = 5MHz		-84		dB
OUTPUT						
	Output voltage swing from supply rails	V_S = 5V, A_{OL} > 94dB		0.1	0.3	V
		V_S = 5V, R_L = 1kΩ, A_{OL} > 90dB, T_A = –40°C to +125°C			0.4	
I_O	Output current, single, dual, quad (1) (2)	V_S = 5V	100			mA
		V_S = 3V		50		
	Closed-loop output impedance	f < 100kHz		0.05		Ω
R_O	Open-loop output resistance	For OPA2354, OPA4354		35		Ω
		For OPA354		39		Ω
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)	T_A = 25°C, V_S = 5V (enabled), I_O = 0A, for OPA2354, OPA4354		4.9	6	mA
		T_A = 25°C, V_S = 5V (enabled), I_O = 0A, for OPA354		5	6.3	
		T_A = –40°C to +125°C, for OPA2354, OPA4354			7.5	
		T_A = –40°C to +125°C, for OPA354			7.7	
THERMAL SHUTDOWN: JUNCTION TEMPERATURE						
	Shutdown			160		℃
	Reset from shutdown			140		℃

(1) See the typical characteristic curves for output voltage swing vs output current.
(2) Specified by design.

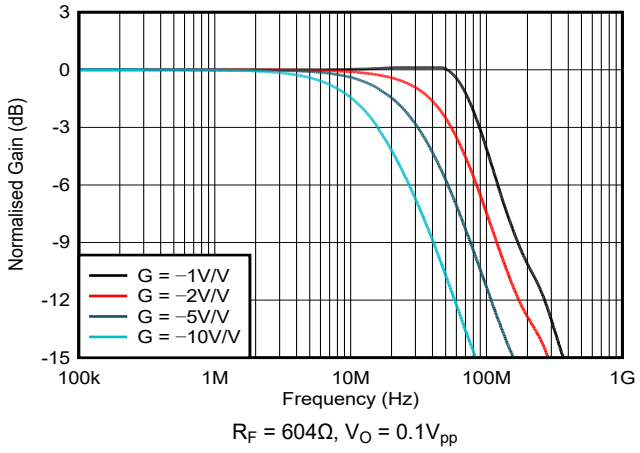
6.8 Typical Characteristics

at T_A = 25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S / 2, unless otherwise noted.



V_O = 0.1V_{pp}

Figure 6-1. Non-inverting Small- Signal Frequency Response



R_F = 604Ω, V_O = 0.1V_{pp}

Figure 6-2. Inverting Small- Signal Frequency Response

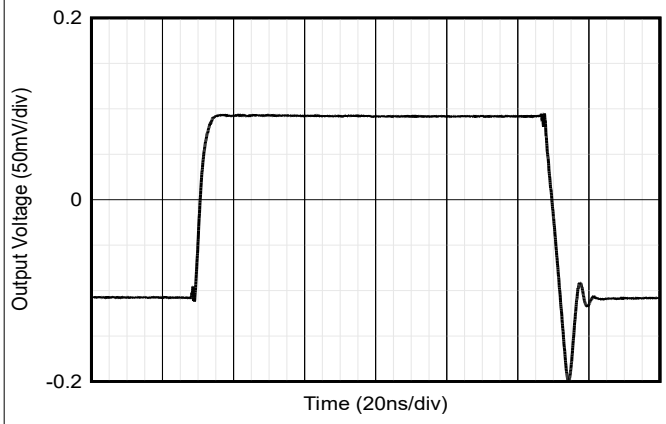


Figure 6-3. Non-inverting Small- Signal Step Response

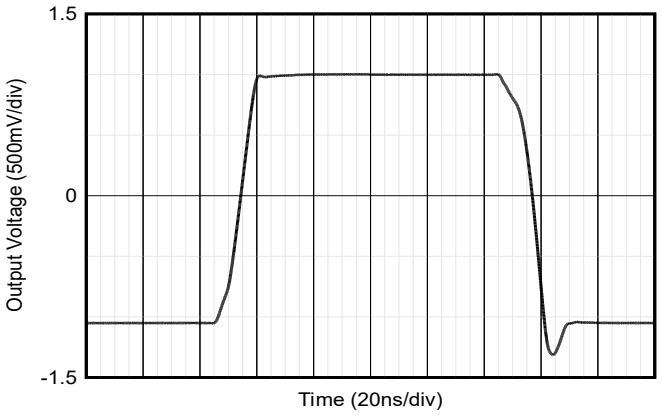
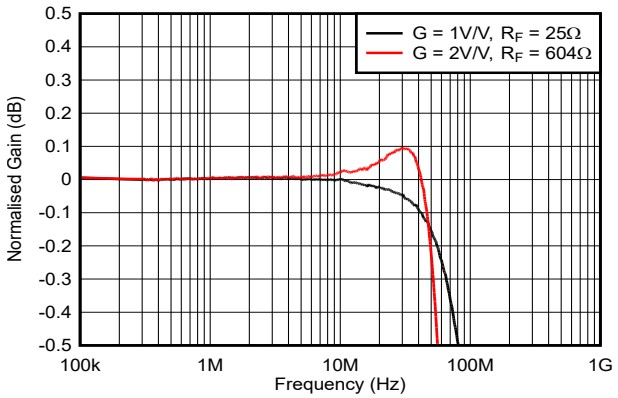
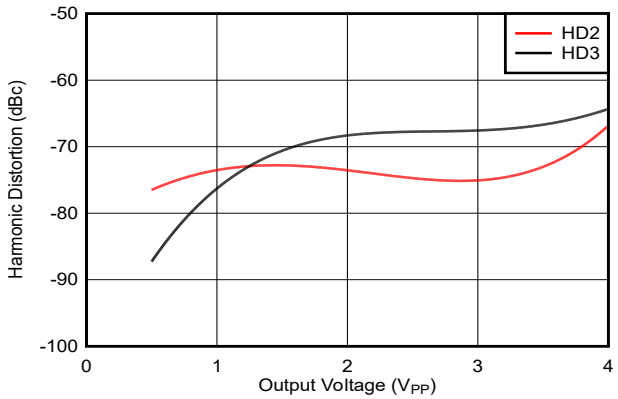


Figure 6-4. Non-inverting Large- Signal Step Response



V_O = 0.1V_{pp}

Figure 6-5. 0.1dB Gain Flatness

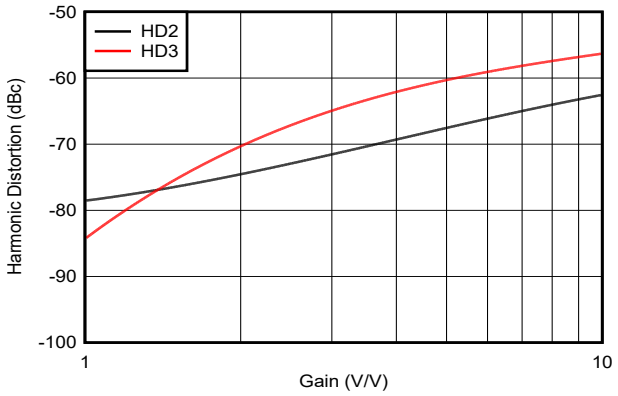


G = –1V/V, f = 1MHz, R_L = 200Ω

Figure 6-6. Harmonic Distortion vs Output Voltage

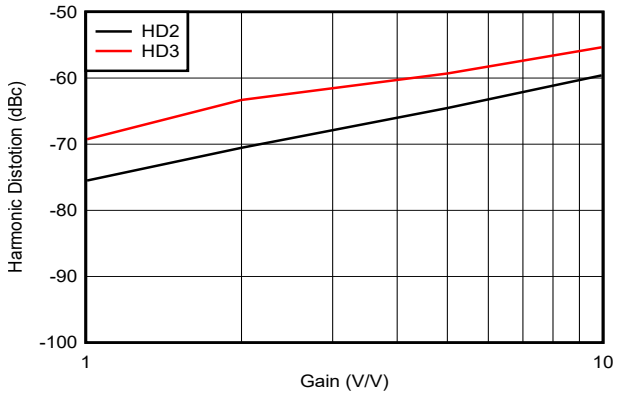
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S / 2, unless otherwise noted.



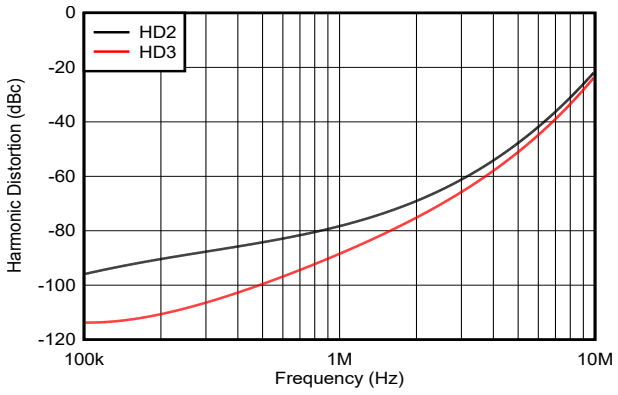
V_O = 2V_{PP}, f = 1MHz, R_L = 200Ω

Figure 6-7. Harmonic Distortion vs Non-inverting Gain



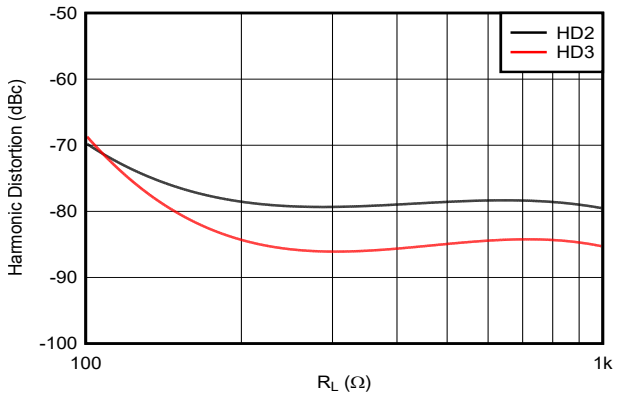
V_O = 2V_{PP}, f = 1MHz, R_L = 200Ω

Figure 6-8. Harmonic Distortion vs Inverting Gain



V_O = 2V_{PP}, R_L = 200Ω, V_{CM} = 1.5V

Figure 6-9. Harmonic Distortion vs Frequency



V_O = 2V_{PP}, f = 1MHz, V_{CM} = 1.5V

Figure 6-10. Harmonic Distortion vs Load Resistance

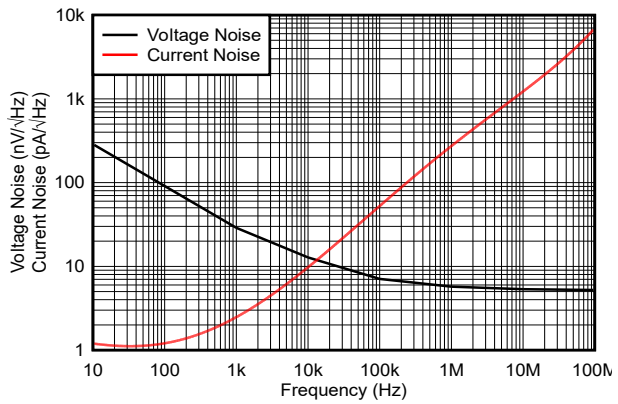
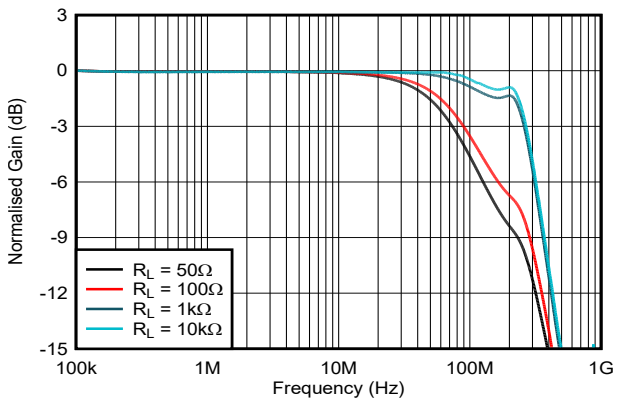


Figure 6-11. Input Voltage and Current Noise Spectral Density vs Frequency



V_O = 0.1V_{pp}, C_L = 0pF

Figure 6-12. Frequency Response vs Various R_L Values

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S / 2, unless otherwise noted.

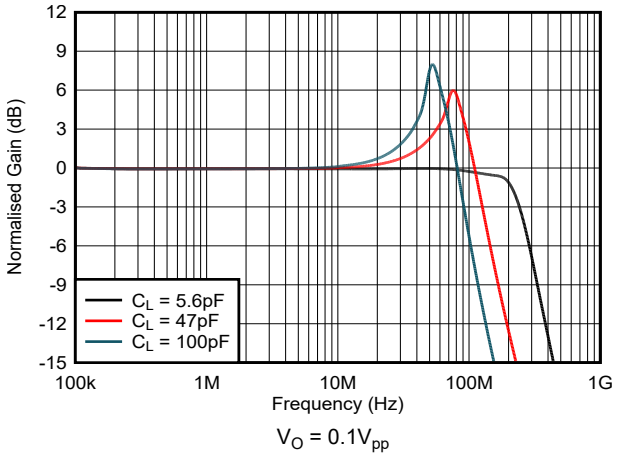


Figure 6-13. Frequency Response for Various C_L Values

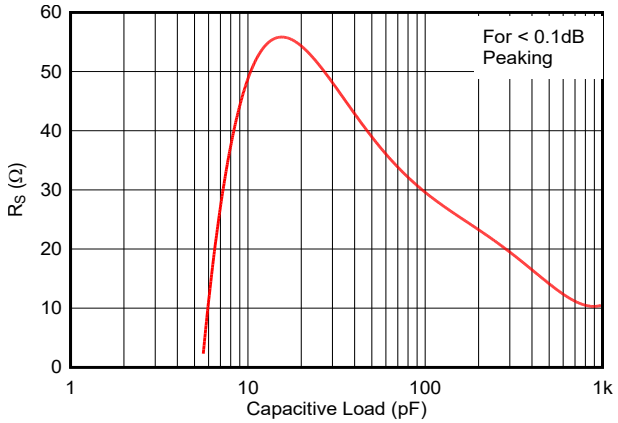


Figure 6-14. Recommended R_S vs Capacitive Load

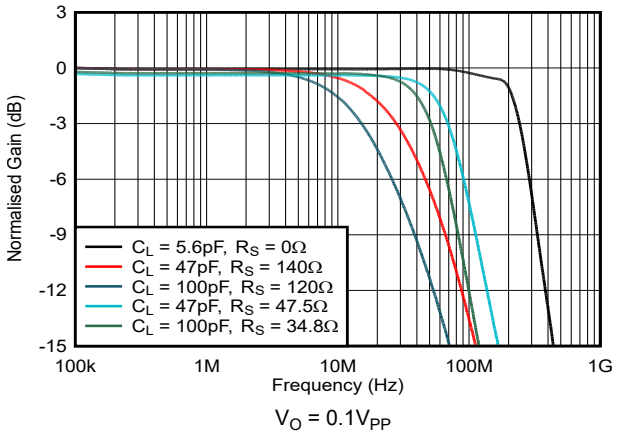


Figure 6-15. Frequency Response vs Capacitive Load

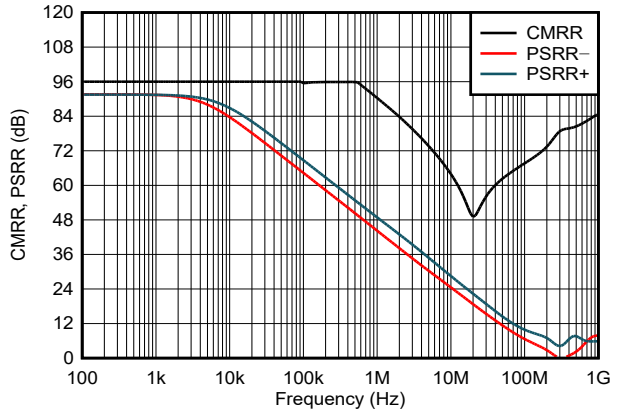


Figure 6-16. Common- Mode Rejection Ratio and Power- Supply Rejection Ratio vs Frequency

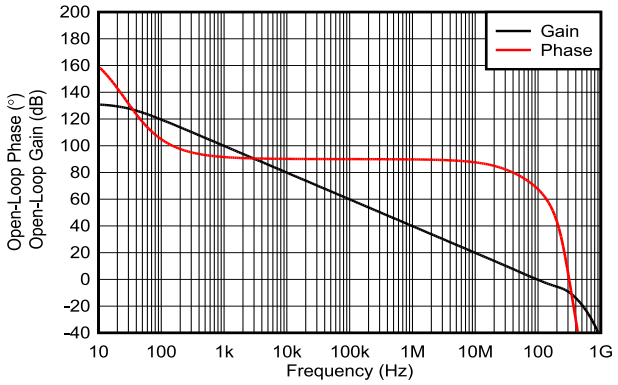


Figure 6-17. Open- Loop Gain and Phase

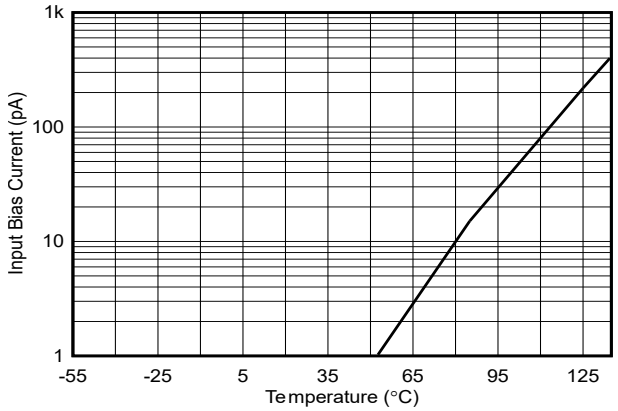


Figure 6-18. Input Bias Current vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S / 2, unless otherwise noted.

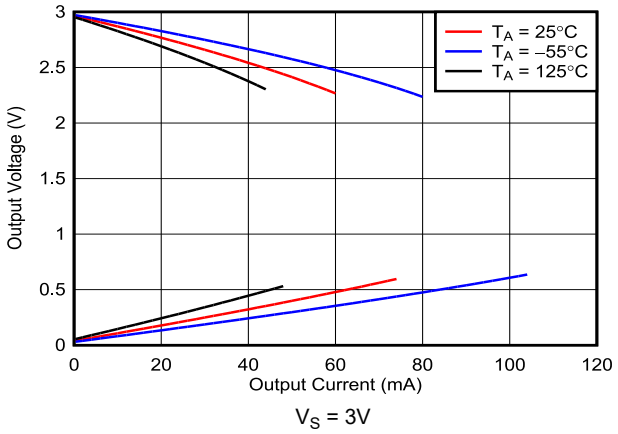


Figure 6-19. Output Voltage Swing vs Output Current

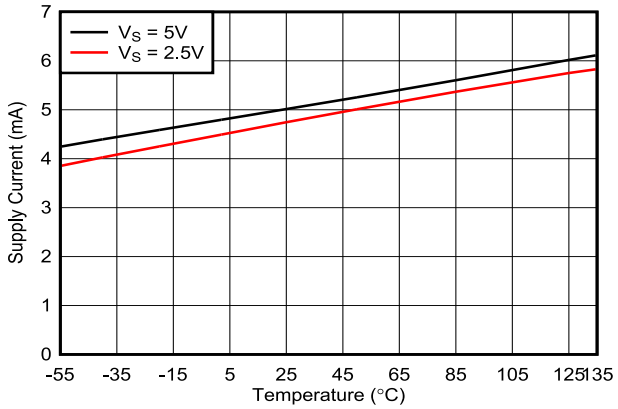


Figure 6-20. Supply Current vs Temperature

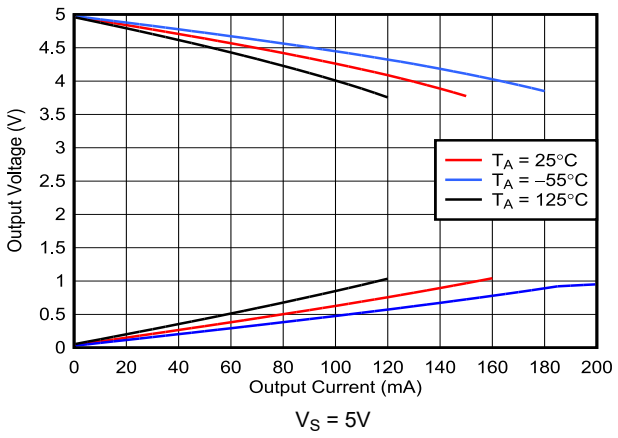


Figure 6-21. Output Voltage Swing vs Output Current

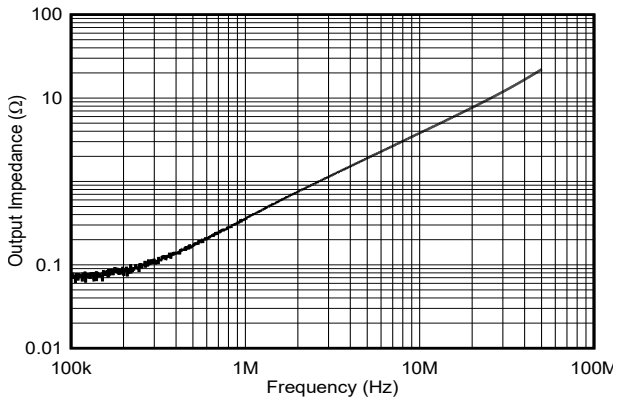


Figure 6-22. Closed- Loop Output Impedance vs Frequency

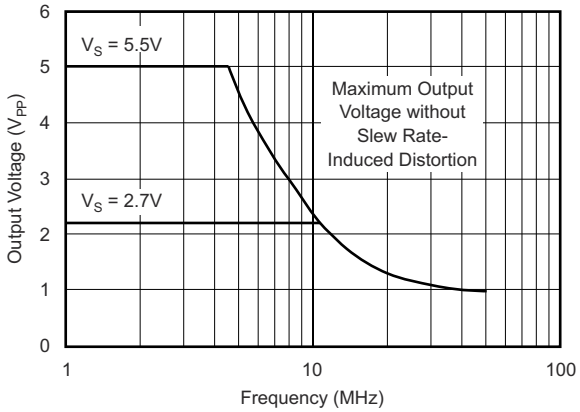


Figure 6-23. Maximum Output Voltage vs Frequency

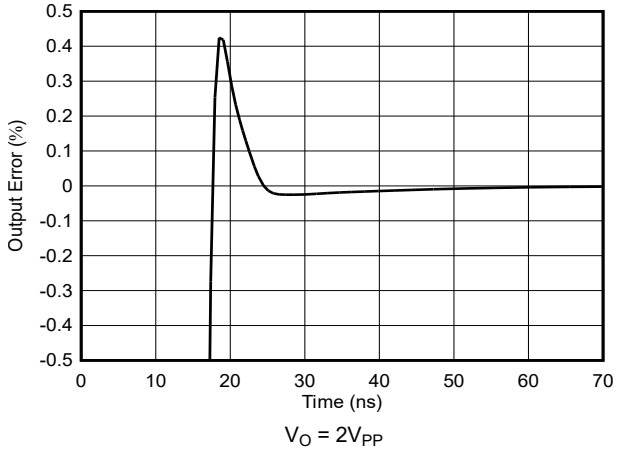


Figure 6-24. Output Settling Time to 0.1%

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, G = +1, R_F = 0Ω, R_L = 1kΩ, and connected to V_S / 2, unless otherwise noted.

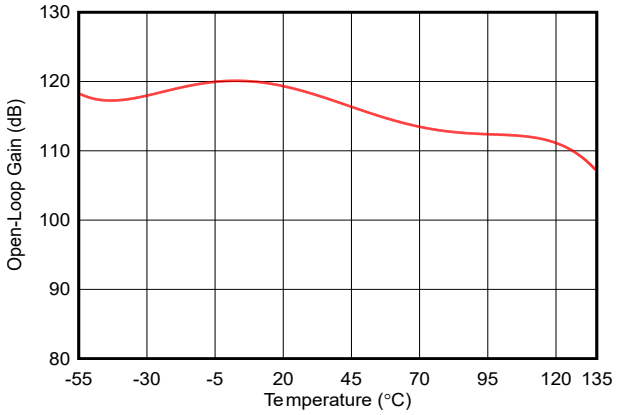


Figure 6-25. Open- Loop Gain vs Temperature

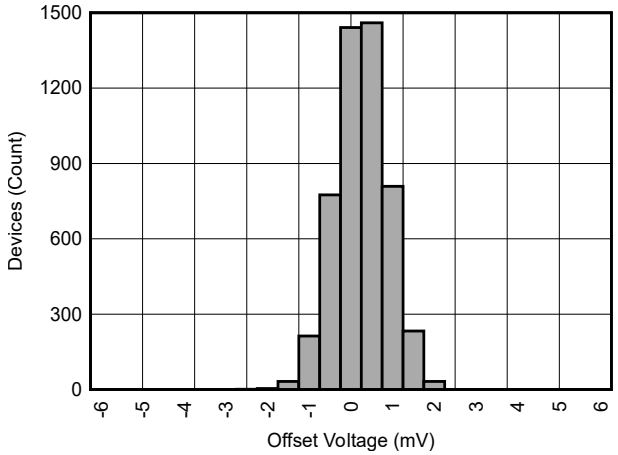


Figure 6-26. Offset Voltage Production Distribution

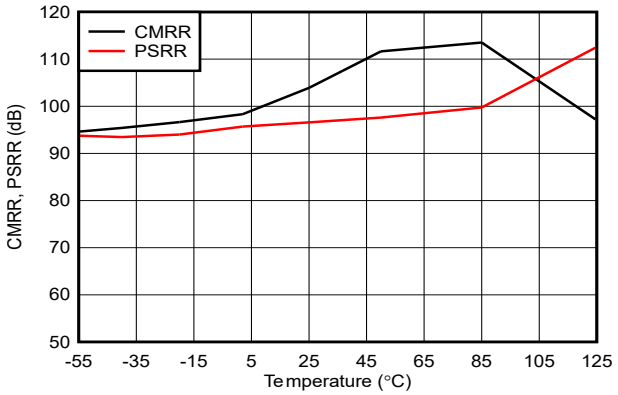


Figure 6-27. Common-mode Rejection Ratio and Power-supply Rejection Ratio vs Temperature

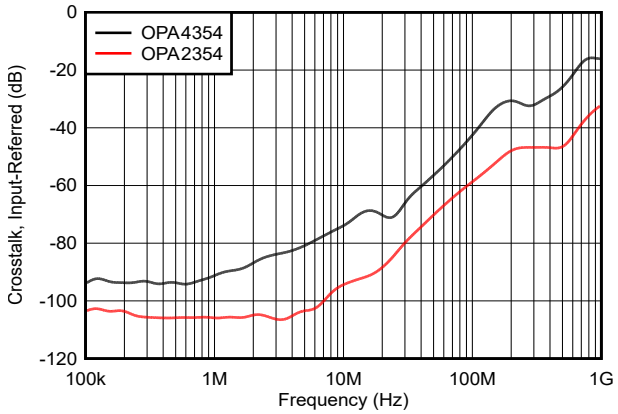


Figure 6-28. Channel-to-channel crosstalk

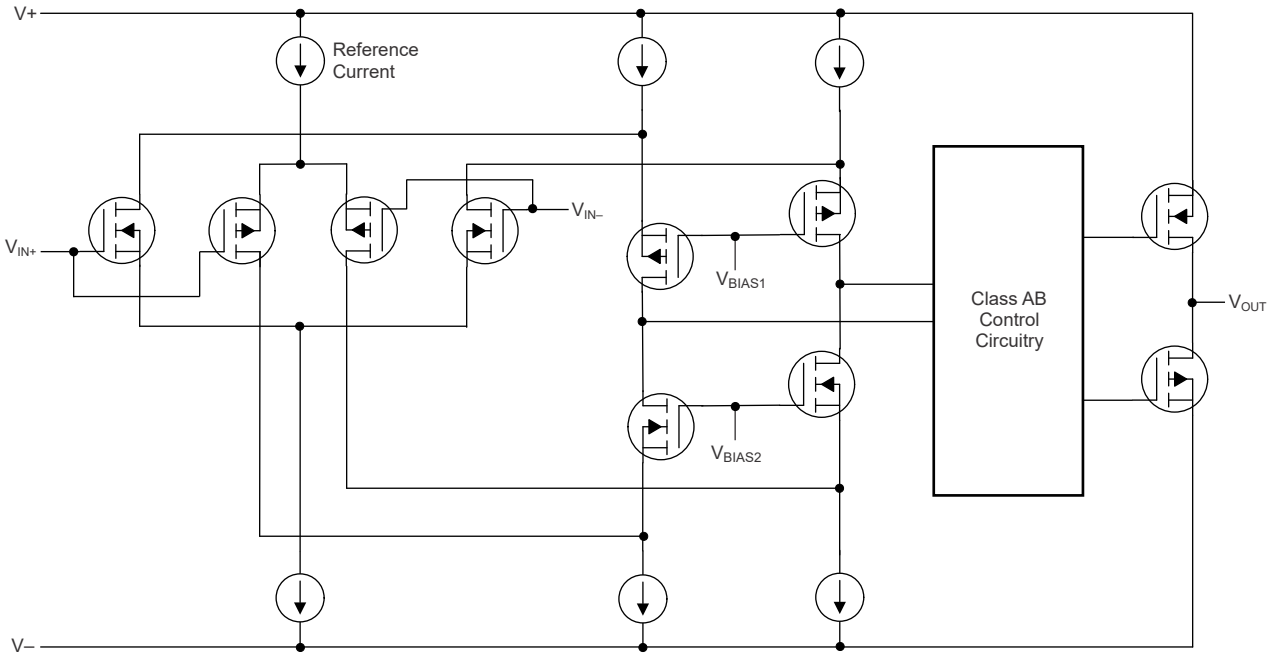
7 Detailed Description

7.1 Overview

The OPAx354 are CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifiers designed for video, high-speed, and other applications. These device are available as single, dual, or quad op amps.

These amplifiers feature a 100MHz gain bandwidth, and 150V/µs slew rate, but the amplifiers are unity-gain stable and operate as a 1V/V voltage follower.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAx354 is specified over a power-supply range of 2.7V to 5.5V (±1.35V to ±2.75V). However, the supply voltage can range from 2.5V to 5.5V (±1.25 V to ±2.75V).

CAUTION
Supply voltages greater than 7.5V (absolute maximum) can permanently damage the amplifier.

See Section 6.8 for parameters that vary over supply voltage or temperature.

7.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the OPAx354 extends 100mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Section 7.2*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2V to 100mV greater than the positive supply, while the P-channel pair is on for inputs from 100mV less than the negative supply to approximately (V+) − 1.2V. There is a small transition region, typically (V+) − 1.5V to (V+) − 0.9V, in which both pairs are on. This 600mV transition region vary ±500 mV with process variation. Therefore, the transition region (both input stages on) range from (V+) − 2V to (V+) − 1.5V on the low end, up to (V+) − 0.9V to (V+) − 0.4V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

7.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors achieves rail-to-rail output. For high-impedance loads (> 200Ω), the output voltage swing is typically 100mV from the supply rails. With 10Ω loads, a useful output swing is achieved while maintaining high open-loop gain. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 6-19 and Figure 6-21).

7.3.4 Output Drive

The OPAx354 output stage supplies a continuous output current of ±100mA and yet provides approximately 2.7V of output swing on a 5V supply, as shown in Figure 7-1. For maximum reliability, do not run a continuous dc current in excess of ±100mA. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 6-19 and Figure 6-21). For supplying continuous output currents greater than ±100mA, the OPAx354 can be operated in parallel, as shown in Figure 7-2.

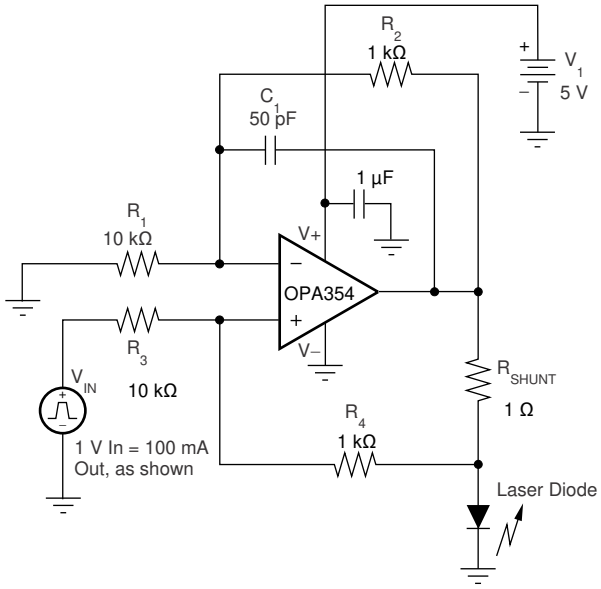


Figure 7-1. Laser Diode Driver

The OPAx354 provides peak currents up to 200mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPAx354 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to less than 140°C.

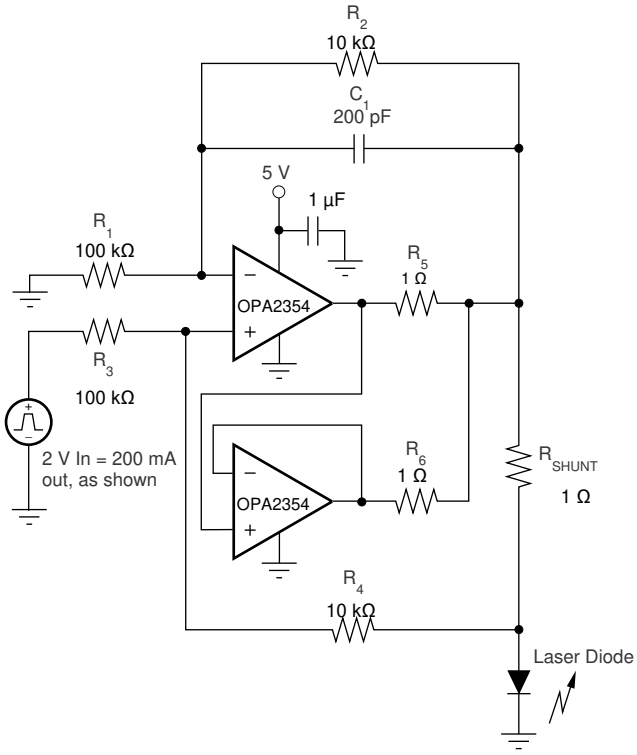


Figure 7-2. Parallel Operation

7.3.5 Video

The OPAx354 output stage is capable of driving standard back-terminated 75Ω video cables, as shown in Figure 7-3. By back-terminating a transmission line, the output stage does not exhibit a capacitive load to the driver. A

properly back-terminated 75Ω cable does not appear as capacitance; the cable presents a 150Ω resistive load to the OPAx354 output.

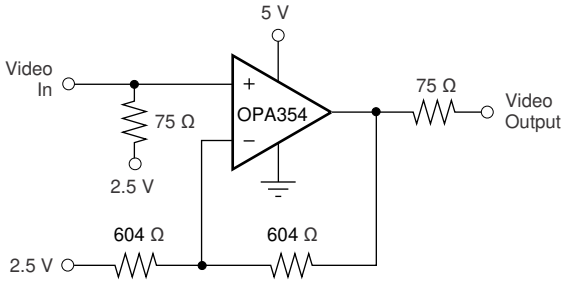
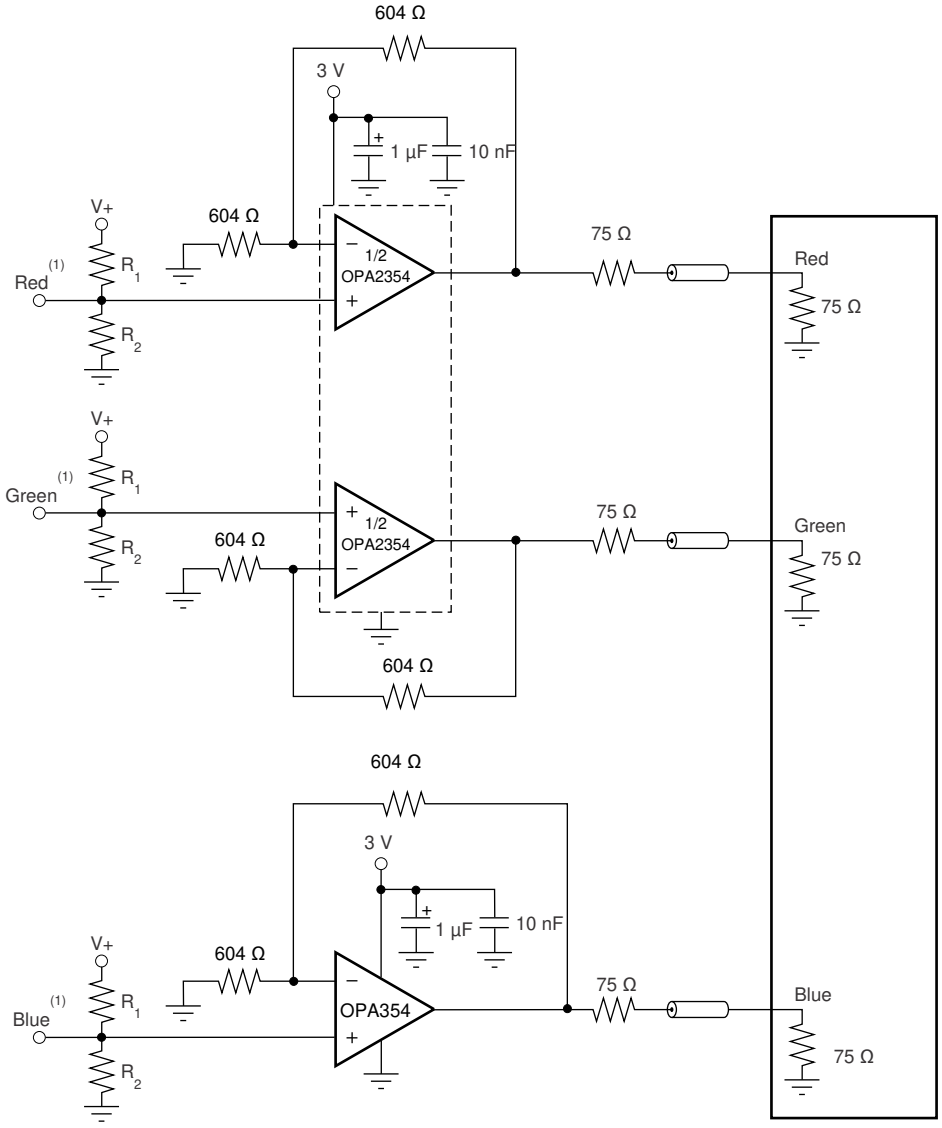


Figure 7-3. Single-Supply Video Line Driver

The OPAx354 is used as an amplifier for RGB graphic signals, which feature a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See Figure 7-4.



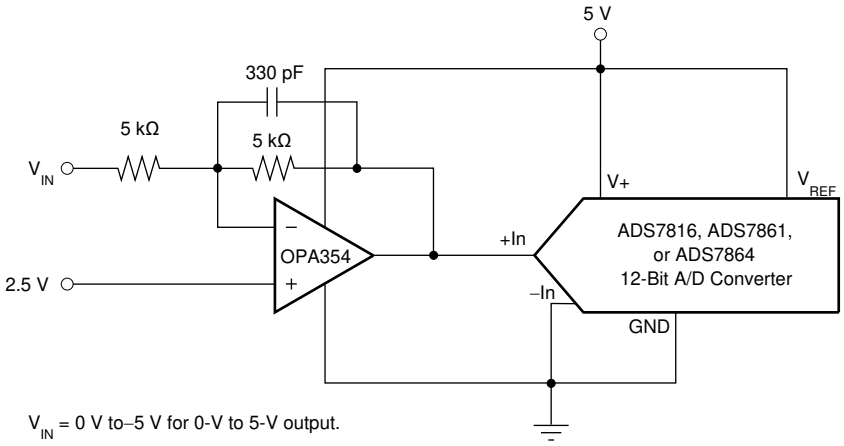
(1) Source video signal offset 300mV above ground to accommodate op amp swing−to−ground capability.

Figure 7-4. RGB Cable Driver

7.3.6 Driving Analog-to-Digital Converters

The OPAx354 series op amps offer 60ns of settling time to 0.01%, making the series a good choice for driving high- and medium-speed sampling ADCs and reference circuits. The OPAx354 series provide an effective means of buffering the
ADC input capacitance and resulting charge injection while providing signal gain. For applications requiring high dc accuracy, the OPA620 series is recommended.

Figure 7-5 shows the OPAx354 driving an ADC. With the OPAx354 in an inverting configuration, a capacitor across the feedback resistor is used to filter high-frequency noise in the signal.



Note: ADC input = 0V to V_{REF}.

Figure 7-5. The OPAx354 in Inverting Configuration Driving the ADS7816

7.3.7 Capacitive Load and Stability

The OPAx354 series op amps drives a wide range of capacitive loads. However, all op amps can become unstable under certain conditions. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. See also the *Frequency Response for Various C_L* typical characteristic curve (Figure 6-13).

The OPAx354 topology enhances the ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. See also the *Recommended R_S vs Capacitive Load* (Figure 6-14) and *Frequency Response vs Capacitive Load* (Figure 6-15) typical characteristic curves.

Figure 7-6 shows one method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor in series with the output. This configuration significantly reduces ringing with large capacitive loads; see the *Frequency Response vs Capacitive Load* typical characteristic curve (Figure 6-15). However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error can be insignificant. For instance, with R_L = 10kΩ and R_S = 20Ω, there is an error of approximately 0.2% at the output.

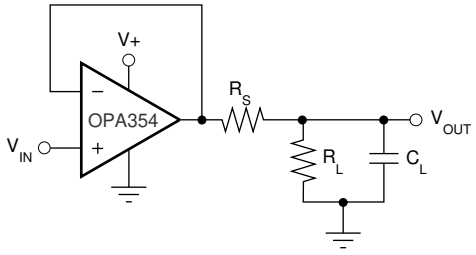


Figure 7-6. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

7.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 a preferred wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design (as shown in Figure 7-7) are the expected diode capacitance [including the parasitic input common-mode and differential-mode input capacitance (2 + 2)pF for the OPAx354], the desired transimpedance gain (R_F), and the gain-bandwidth product (GBW) for the OPAx354 (100MHz, typical). With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response.

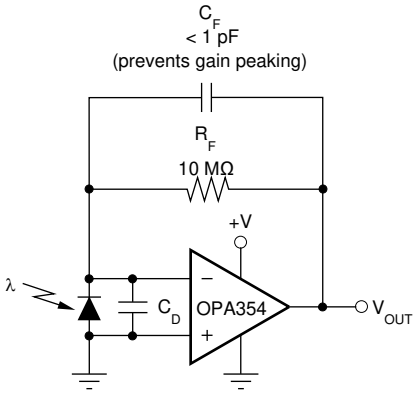


Figure 7-7. Transimpedance Amplifier

To achieve a maximally flat, second-order, Butterworth frequency response, the feedback pole must be set as shown in Equation 1:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \tag{1}$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by Equation 2:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \text{ Hz} \tag{2}$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200MHz GBW) or the OPA655 (400MHz GBW) can be used.

7.4 Device Functional Modes

The OPAx354 devices are powered on when the supply is connected. These devices operate as single-supply operational amplifiers or dual-supply amplifiers depending on the application. The devices are used with asymmetrical supplies, as long as the differential voltage (V– to V+) is at least 1.8V and no greater than 5.5V (example: V– set to –3.5V and V+ set to 1.5V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx354 devices are CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifiers designed for video, high-speed, and other applications. The OPAx354 are available as single, dual, or quad op amps. The amplifiers feature a 100MHz gain bandwidth, and 150V/µs slew rate, are unity-gain stable, and operate as 1V/V voltage followers.

8.2 Typical Application

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 devices excellent wideband photodiode transimpedance amplifiers. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency. The key elements to a transimpedance design, as shown in Figure 8-1, are the expected diode capacitance, (which include the parasitic input common-mode and differential-mode input capacitance) the desired transimpedance gain, and the gain-bandwidth (GBW) for the OPAx354 family of devices (20MHz). With these three variables set, the feedback capacitor value is set to control the frequency response. Feedback capacitance includes the stray capacitance, which is 0.2pF for a typical surface-mount resistor.

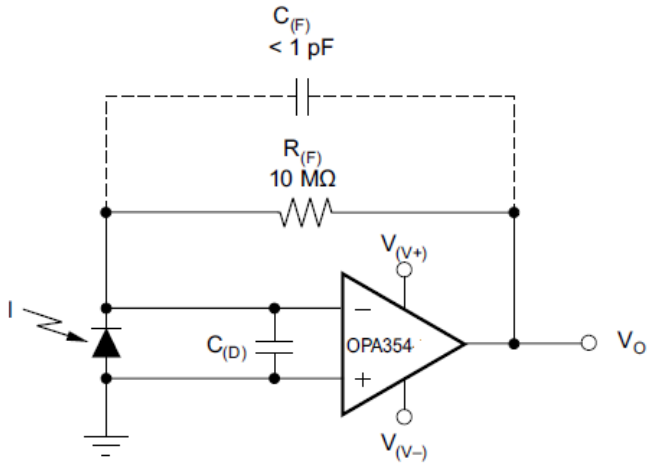


Figure 8-1. Dual-Supply Transimpedance Amplifier

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage, $V_{(V+)}$	2.5V
Supply voltage, $V_{(V–)}$	–2.5V

$C_{(F)}$ is optional to prevent gain peaking. $C_{(F)}$ includes the stray capacitance of $R_{(F)}$.

8.2.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole using Equation 3.

$$\frac{1}{2 \times \pi \times R_{(F)} \times C_{(F)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (3)$$

Calculate the bandwidth using Equation 4.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (4)$$

8.2.2.1 Optimizing the Transimpedance Circuit

To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select $R_{(F)}$ to create the total required gain. Using a lower value for $R_{(F)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(F)}$ increases with the square-root of $R_{(F)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.

2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only the required bandwidth. Use a capacitor across the $R_{(F)}$ to limit bandwidth, even if a capacitor not required for stability.

4. Circuit board leakage degrades the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage helps control leakage.

8.2.3 Application Curve

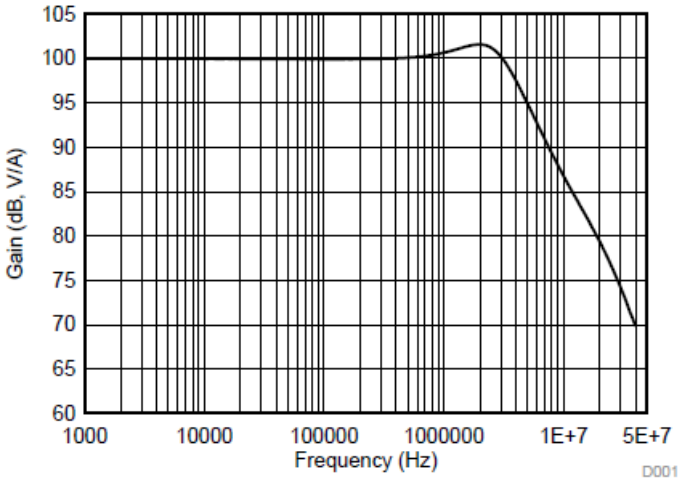


Figure 8-2. AC Transfer Function

8.3 Power Supply Recommendations

The OPAx354 family of devices is specified for operation from 2.5V to 5.5V (±1.25V to ±2.75V); many specifications apply from –40°C to +125°C. Parameters that exhibit significant variance with regard to operating voltage or temperature are shown in *Section 6.8*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. See also Section 8.4.1.

8.4 Layout

8.4.1 Layout Guidelines

Employ good, high-frequency printed-circuit board (PCB) layout techniques for the OPAx354. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin provide clean, stable operation. Large areas of copper provides a means of dissipating heat that is generated in normal operation.

TI does not recommend using sockets with any high-speed amplifier.

A 10nF ceramic bypass capacitor is the minimum recommended value; adding a 1µF or larger tantalum capacitor in parallel is beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving low harmonic and intermodulation distortion.

8.4.1.1 Power Dissipation

Power dissipation depends on power-supply voltage, signal and load conditions. With dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S - V_O$. Power dissipation is minimized by using the lowest possible power-supply voltage necessary to provide the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower. AB-039 *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads See www.ti.com for more details.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 150°C (maximum.) To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

8.4.1.2 Thermally Enhanced PowerPAD Integrated Circuit Package

In addition to the regular 5-pin SOT-23 and 9-pin VSSOP packages, the single and dual versions of the OPAx354 also come in an 8-pin SOIC PowerPAD integrated circuit package. The 98-pin SO with thermal pad is a standard size 8-pin SOIC package where the exposed leadframe on the bottom of the package is soldered directly to the PCB to create a low thermal resistance. This direct attachment enhances the OPAx354 power dissipation capability significantly, and eliminates the use of bulky heat sinks and slugs that are traditionally used in thermal packages. This package is easily mounted using standard PCB assembly techniques.

Note

Because the 8-pin HSOIC PowerPAD integrated circuit package is pin-compatible with standard 8-pin SOIC packages, the OPA354 and OPA2354 can directly replace operational amplifiers in existing sockets. Soldering the thermal pad to the PCB is always required, even with applications that have low power dissipation. This configuration provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD integrated circuit package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the device, as shown in Figure 8-3. This exposed die provides an extremely low thermal

resistance ($R_{\theta JC}$) path between the die and the exterior of the package. The thermal pad on the bottom of the device can then be soldered directly to the PCB, using the PCB as a heat sink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

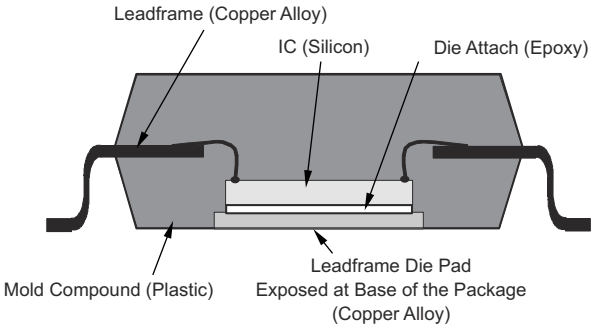


Figure 8-3. Section View of a PowerPAD Integrated Circuit Package

8.4.1.3 PowerPAD™ Integrated Circuit Package Assembly Process

Connect the thermal pad to the most negative supply voltage for the device, which is ground in single-supply applications and V− in split-supply applications.

Prepare the PCB with a top-side etch pattern shown in Figure 8-4. The exact land design can vary based on the specific assembly process requirements. Use etch for the leads and etch for the thermal land.

Place the recommended number of plated-through holes (or thermal vias) in the area of the thermal pad. These holes must be 13mils (0.013in) in diameter. The holes are small so that solder wicking through the holes is not a problem during reflow. TI recommends a minimum of five holes for the 8-pin HSOIC (SO PowerPAD) package as in Figure 8-4.

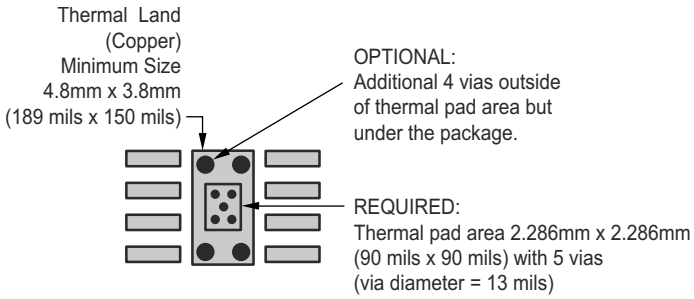


Figure 8-4. 8-Pin PowerPAD PCB Etch and Via Pattern

TI recommends, but does not require, placing a small number of additional holes under the package and outside the thermal pad area. These holes provide additional heat paths between the copper thermal land and the ground plane. The holes can be larger because the holes are not in the area to be soldered, so wicking is not a problem. Figure 8-4 shows this technique.

Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane for single-supply applications, and to V− for split-supply applications.

When laying out these holes, do not use the typical web or spoke via connection methodology, as shown in Figure 8-5. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This feature makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD integrated circuit package must make connection to the internal ground plane with a complete connection around the entire circumference of the plated through-hole.

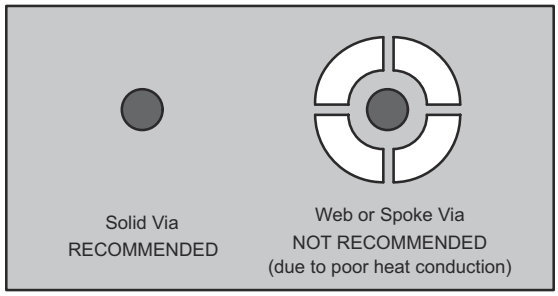


Figure 8-5. Via Connection

The top-side solder mask must leave the pad connections and the thermal pad area exposed. The thermal pad area must leave the 13mil holes exposed. The larger holes outside the thermal pad area can be covered with a solder mask.

Apply solder paste to the exposed thermal pad area and all of the package pins.

With these preparatory steps in place, the PowerPAD integrated circuit package device is placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation and processing results in a part that is properly installed.

For detailed information on the PowerPAD integrated circuit package, including thermal modeling considerations and repair procedures, see also *PowerPAD Thermally Enhanced Package* on www.ti.com.

8.4.2 Layout Example

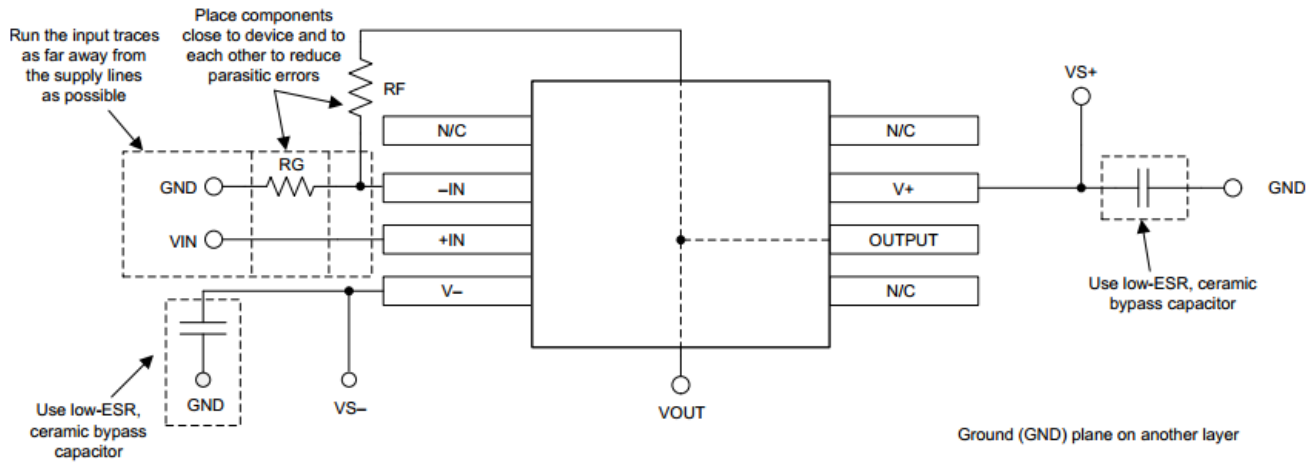


Figure 8-6. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Documentation Support

For related documentation see the following:

- Texas Instruments, *ADS8326 16-Bit, High-Speed, 2.7V to 5.5V microPower Sampling Analog-to-Digital Converter*
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively*
- Texas Instruments, *FilterPro™ user's guide*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps*
- Texas Instruments, *OPA380 and OPA2380 Precision, High-Speed Transimpedance Amplifier*
- Texas Instruments, *OPA355, OPA2355, and OPA3355 200MHz, CMOS Operational Amplifier With Shutdown*
- Texas Instruments, *OPA656 Wideband, Unity-Gain Stable, FET-Input Operational Amplifier*
- Texas Instruments, *Power Amplifier Stress AND Power Handling Limitations*
- Texas Instruments, *PowerPAD Thermally Enhanced Package*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2018) to Revision H (August 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated Thermal Information for OPA354 DBV and DDA packages	5
• Updated Input current noise, rise & fall time, open-loop output resistance, quiescent current in Electrical Characteristics for OPA354	7
• Updated plots in Typical Characteristics	9

Changes from Revision F (June 2016) to Revision G (April 2018)	Page
• Updated plots in Typical Characteristics	9

Changes from Revision E (March 2002) to Revision F (June 2016)	Page
• Added *ESD Ratings*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Deleted *Package/Ordering Information* table, see POA at the end of data sheet	1
• Changed *OPAx354 Related Products* table to *Device Comparison Table*	2

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2354AIDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAG3	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDARG3	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKTG4	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKTG4.B	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA354AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA354AIDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAG3	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA4354AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDRG4	Last Time Buy	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDRG4.B	Last Time Buy	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIPWR	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWR.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWR.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWRG4	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA4354 :

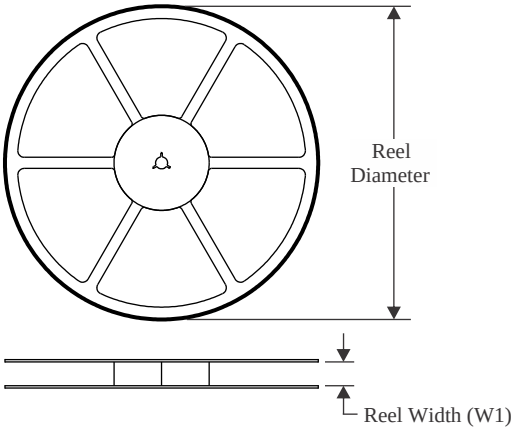
- Automotive : OPA4354-Q1

NOTE: Qualified Version Definitions:

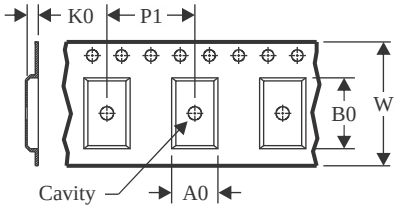
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

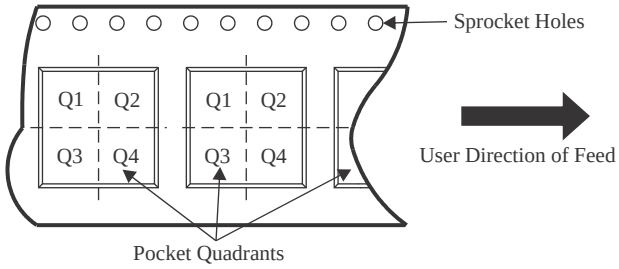


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

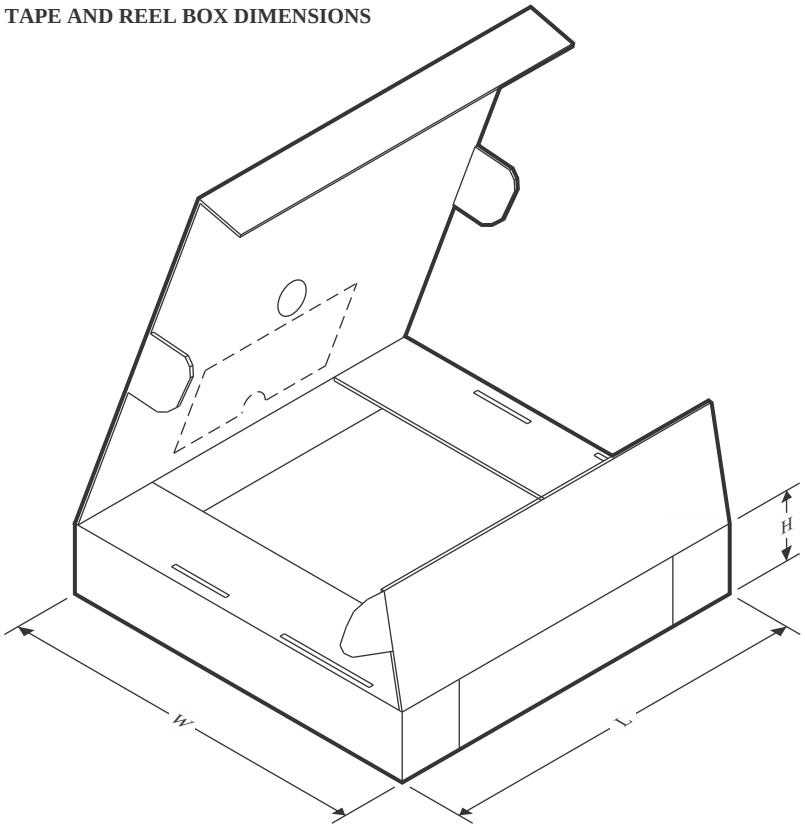
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2354AIDDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA354AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA354AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA354AIDDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4354AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4354AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4354AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4354AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

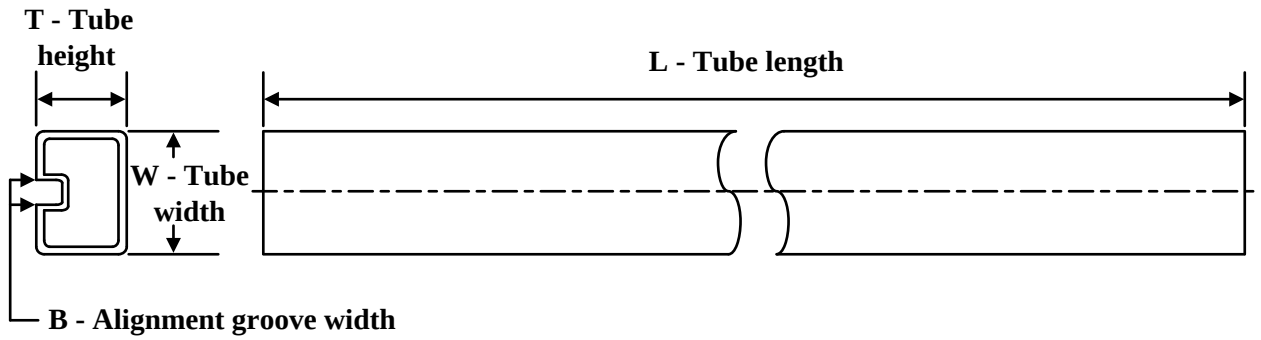
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2354AIDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2354AIDGKTG4	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA354AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA354AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA354AIDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
OPA4354AIDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4354AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
OPA4354AIPWR	TSSOP	PW	14	2500	353.0	353.0	32.0
OPA4354AIPWT	TSSOP	PW	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

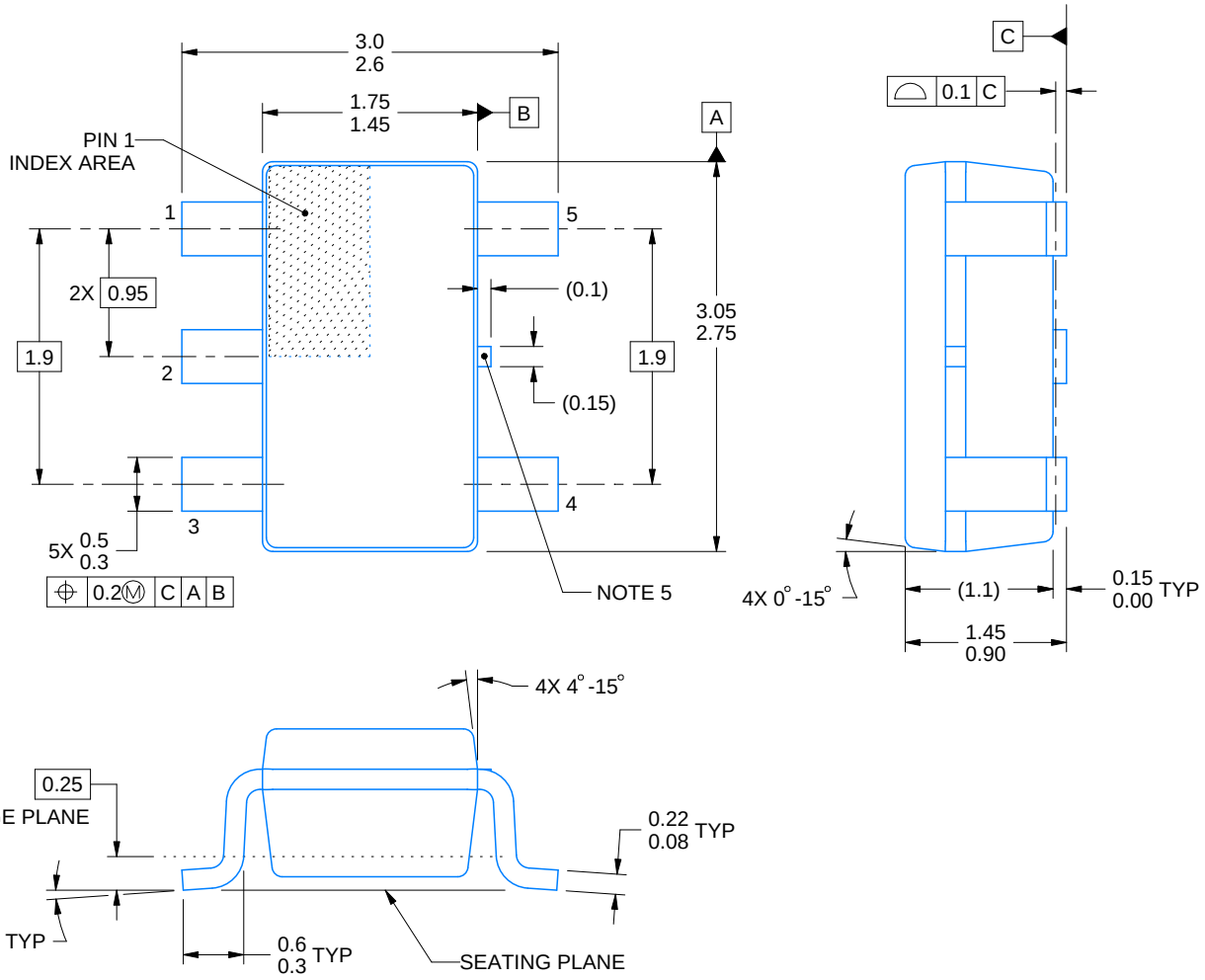
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2354AIDDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA2354AIDDA.B	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA2354AIDDAG3	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA354AIDDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA354AIDDA.B	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA354AIDDAG3	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA4354AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4354AID.B	D	SOIC	14	50	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

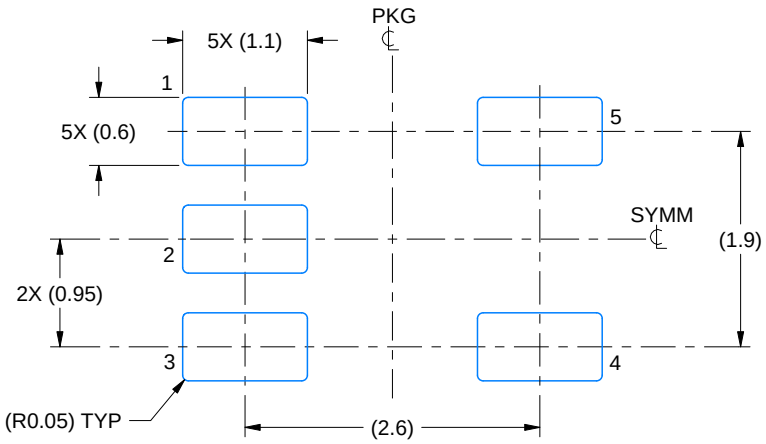
SMALL OUTLINE TRANSISTOR



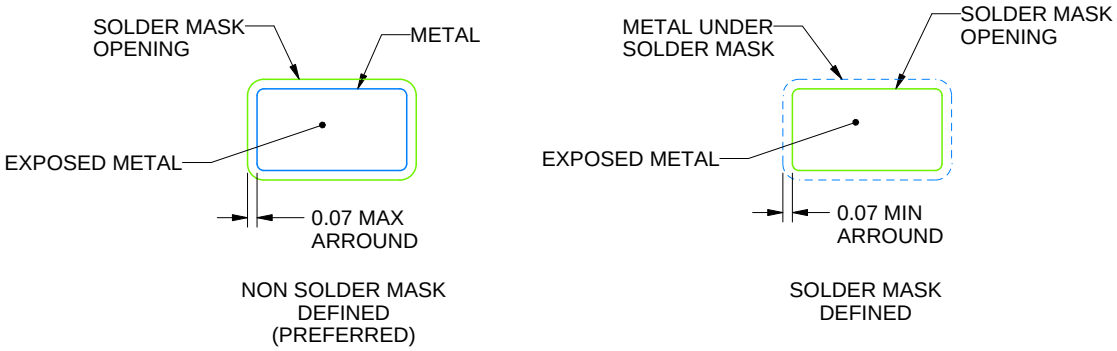
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

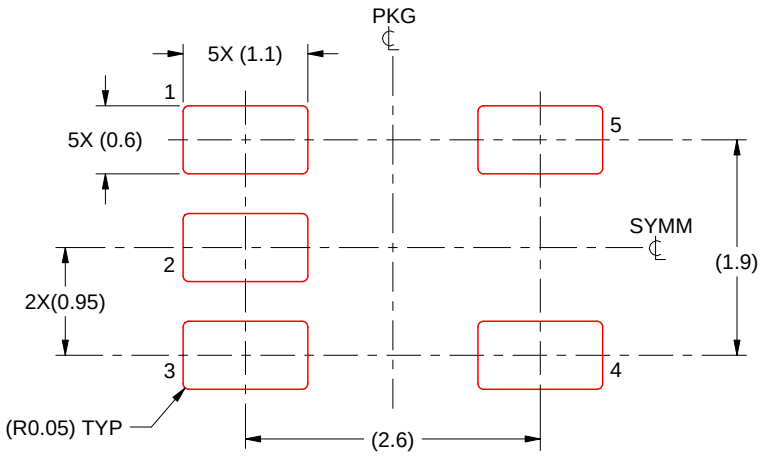


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

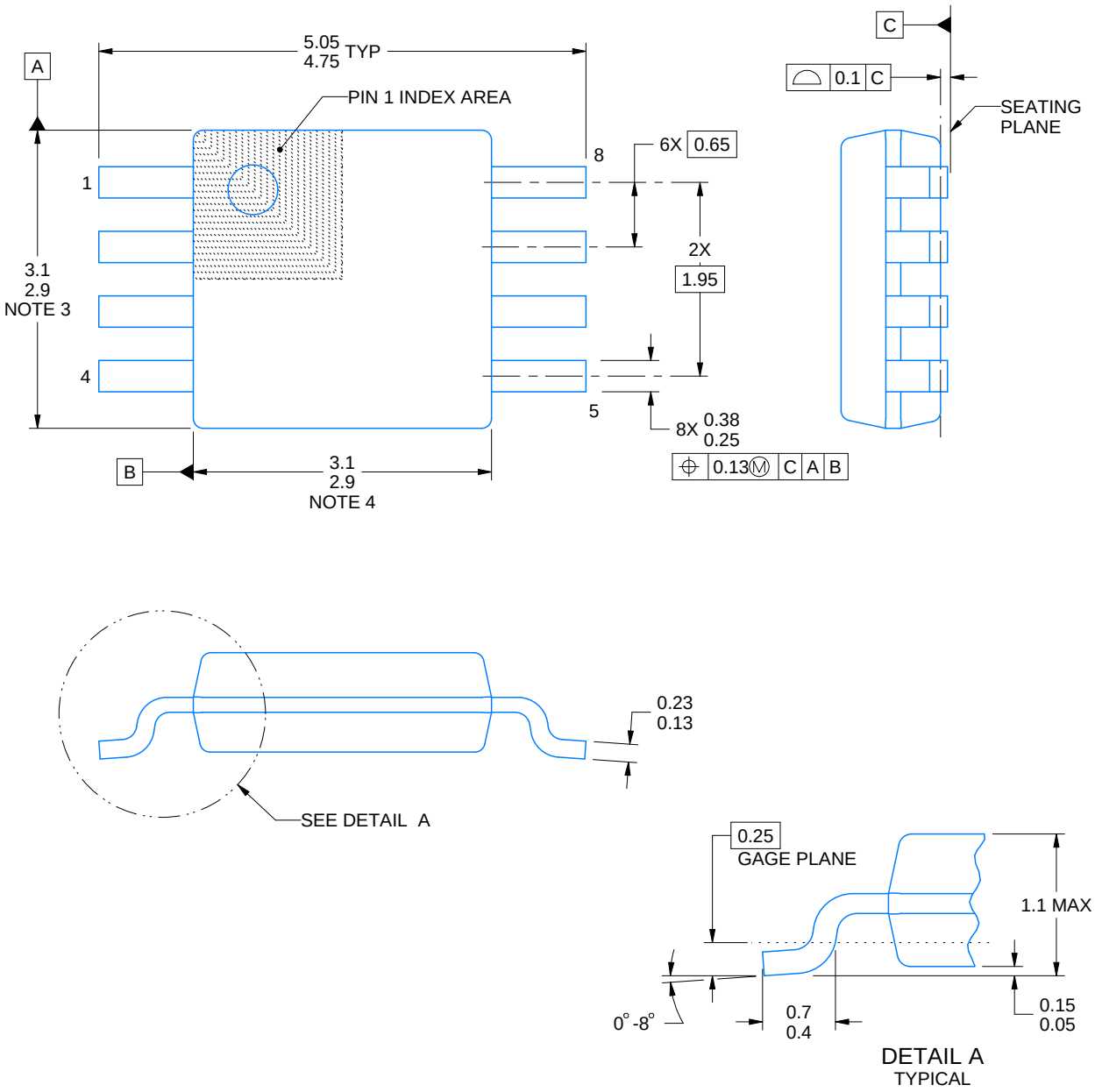
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

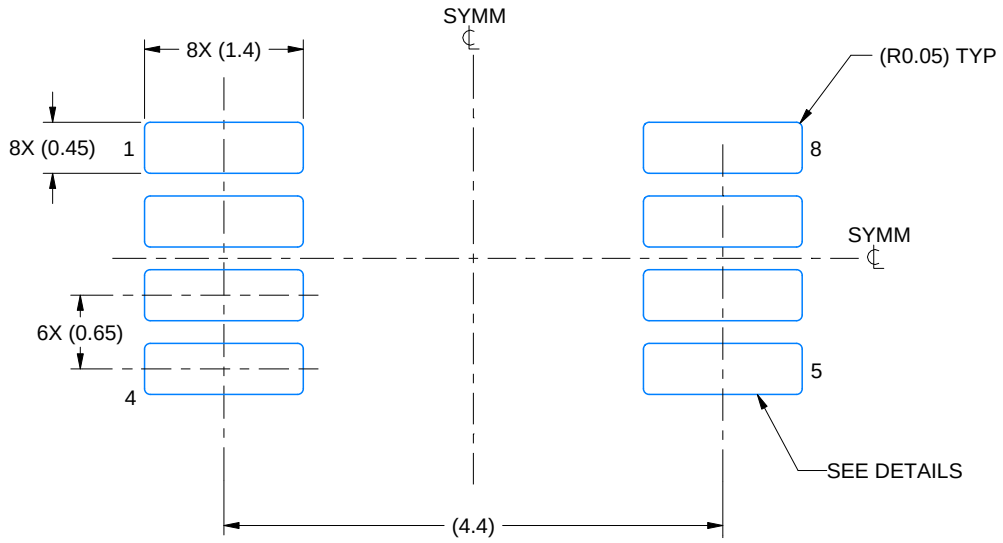
SMALL OUTLINE PACKAGE



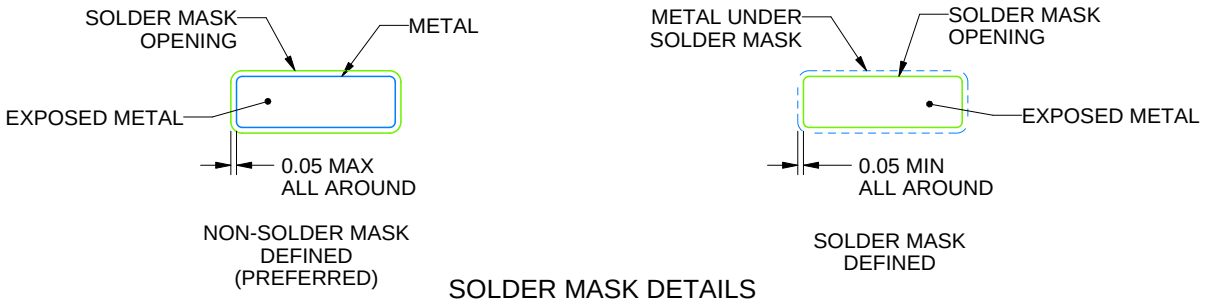
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

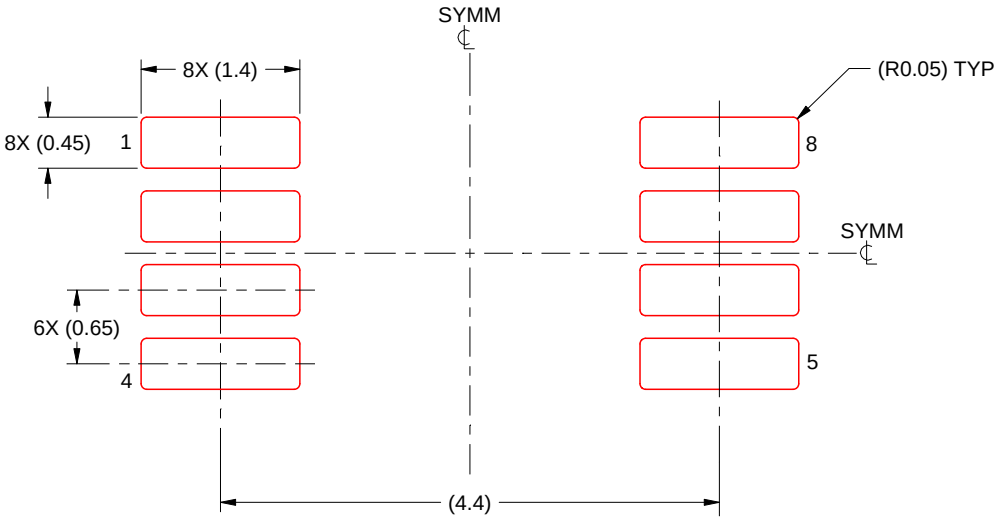


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

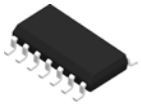


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

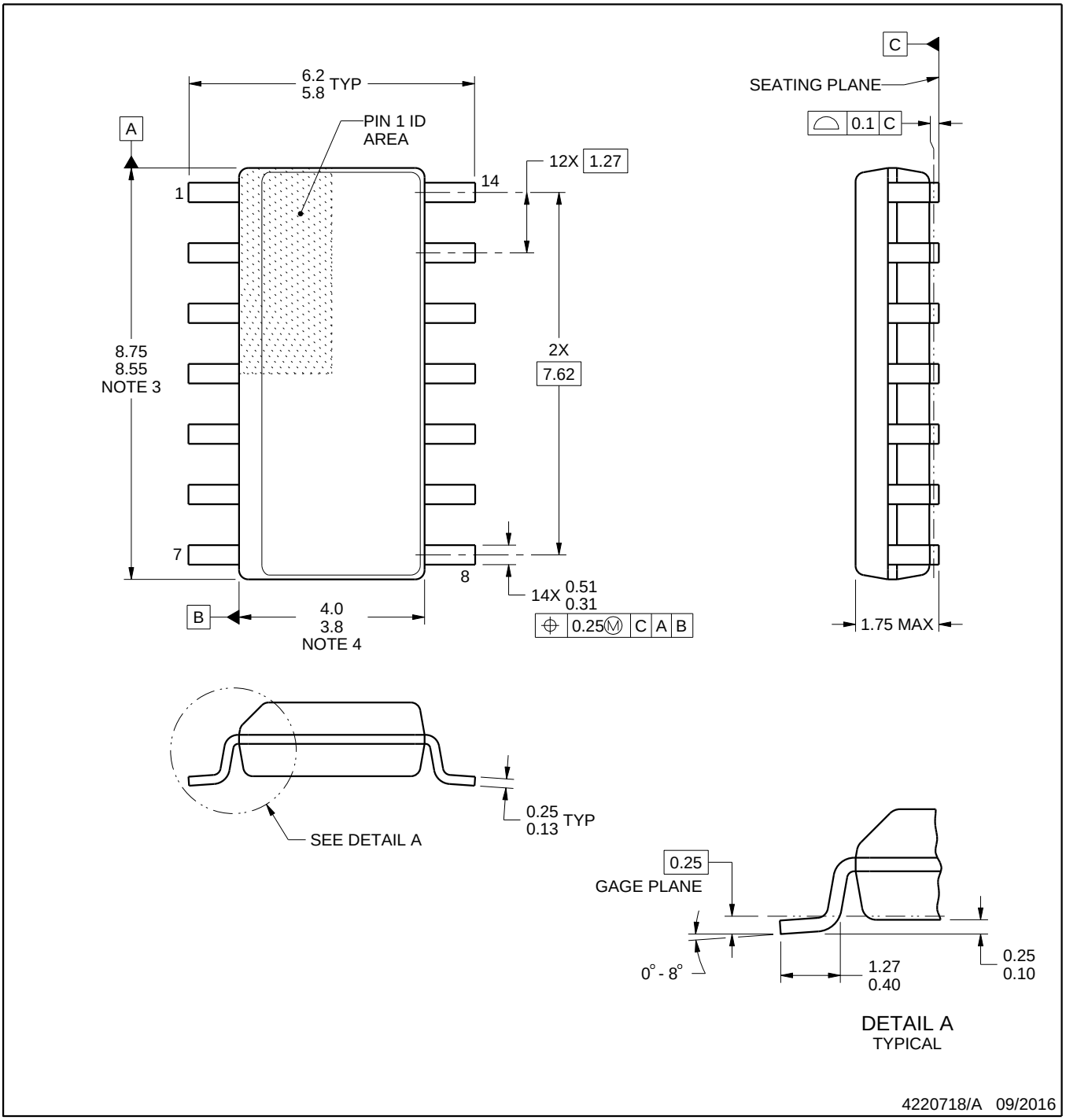


PACKAGE OUTLINE

D0014A

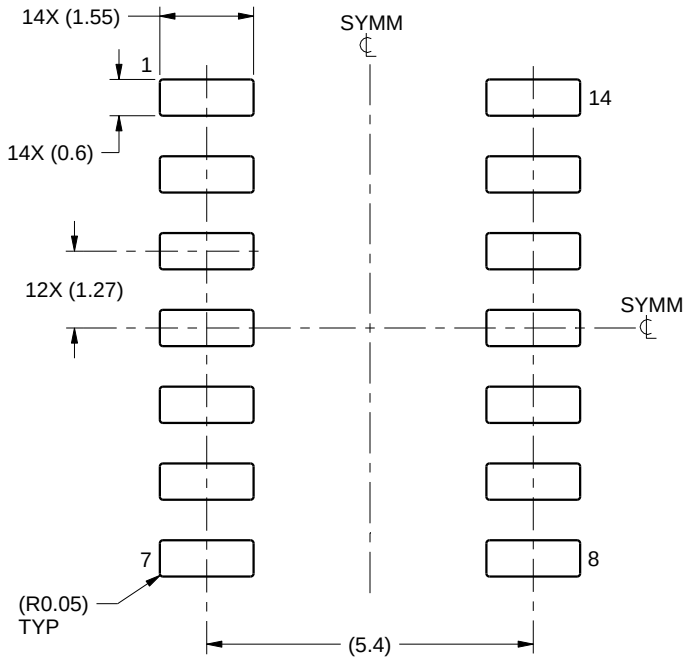
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

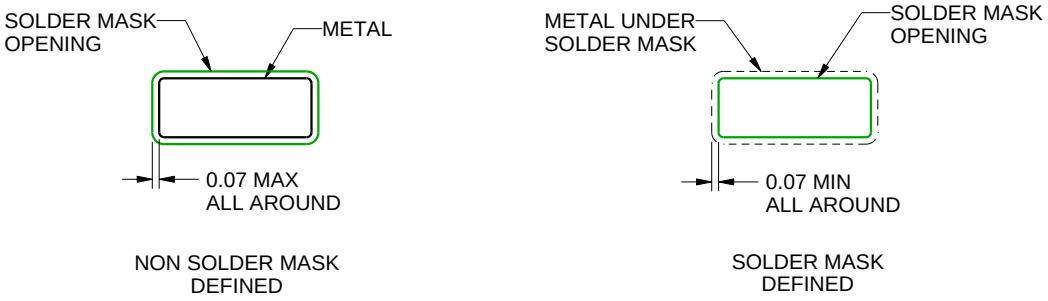


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

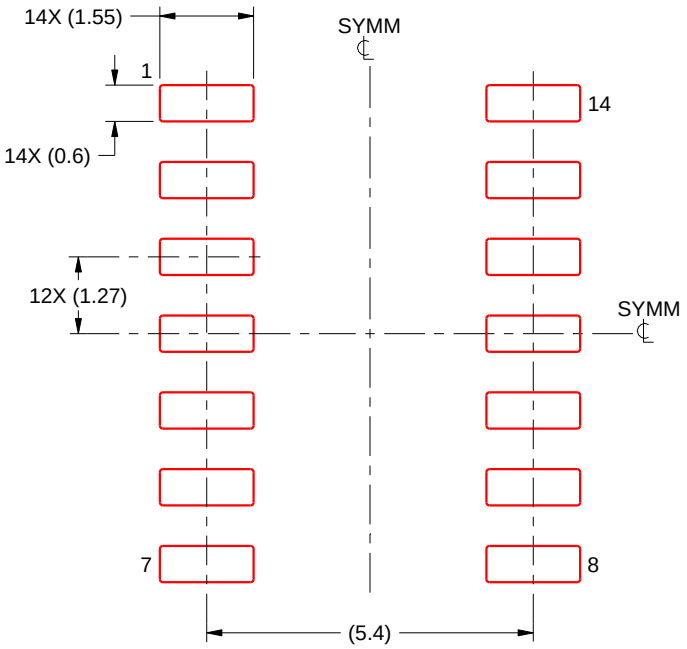
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

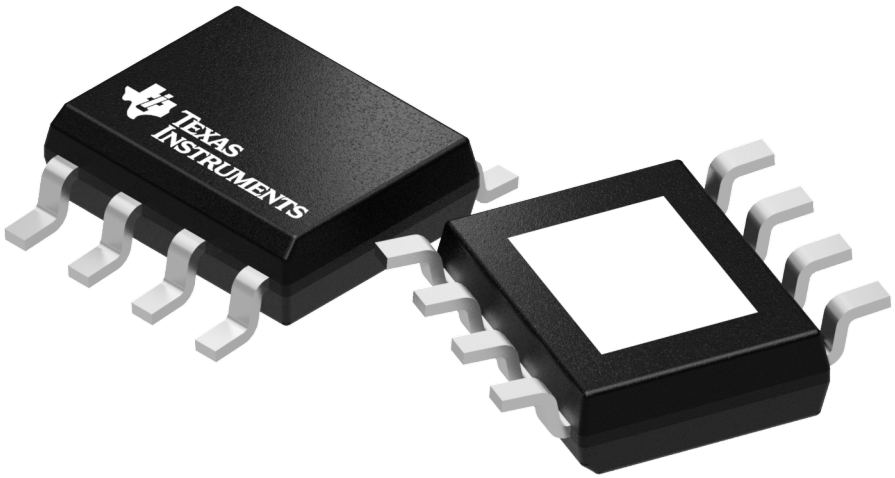
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



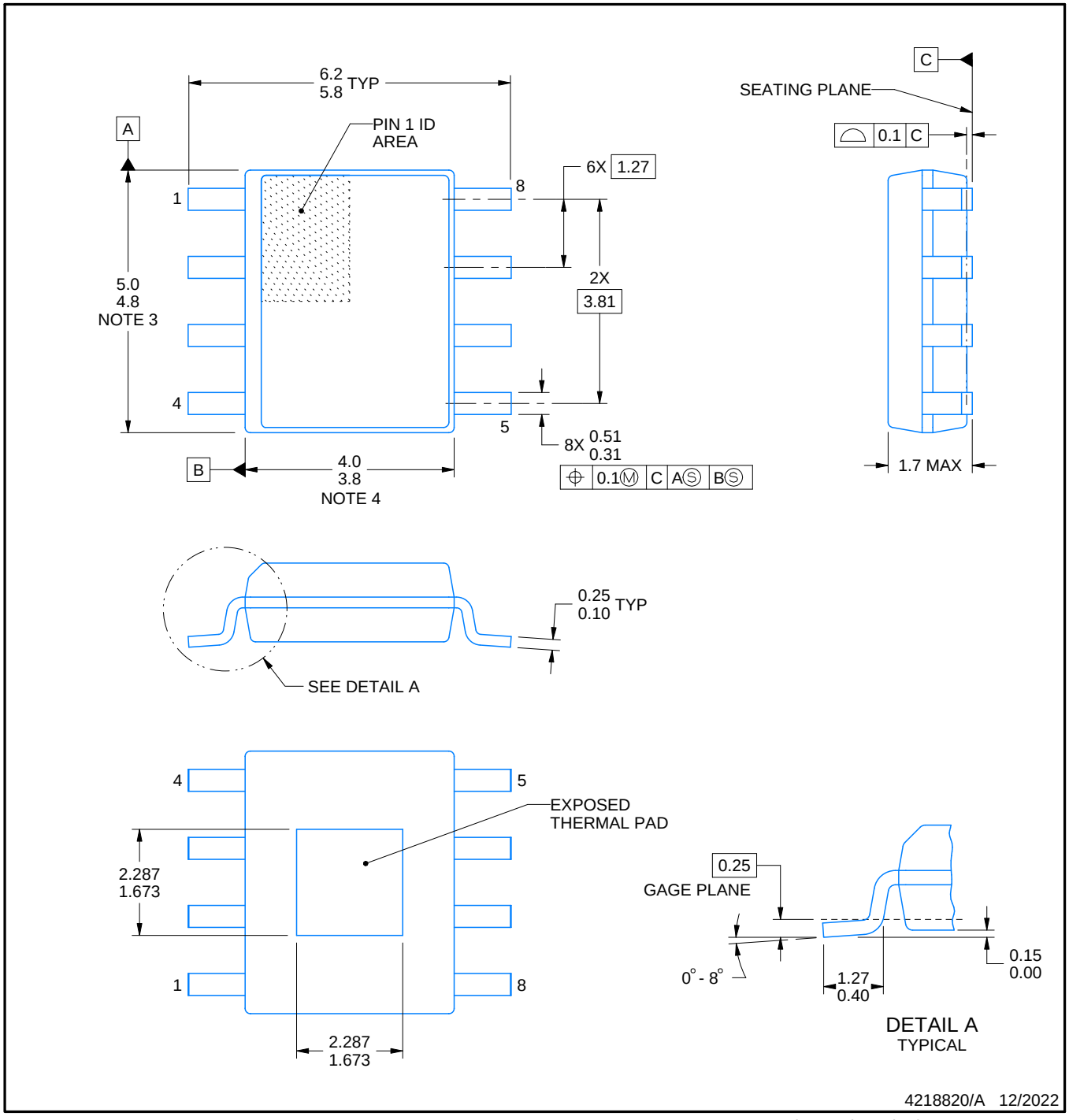
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008D

PowerPAD™ SOIC - 1.7 mm max height

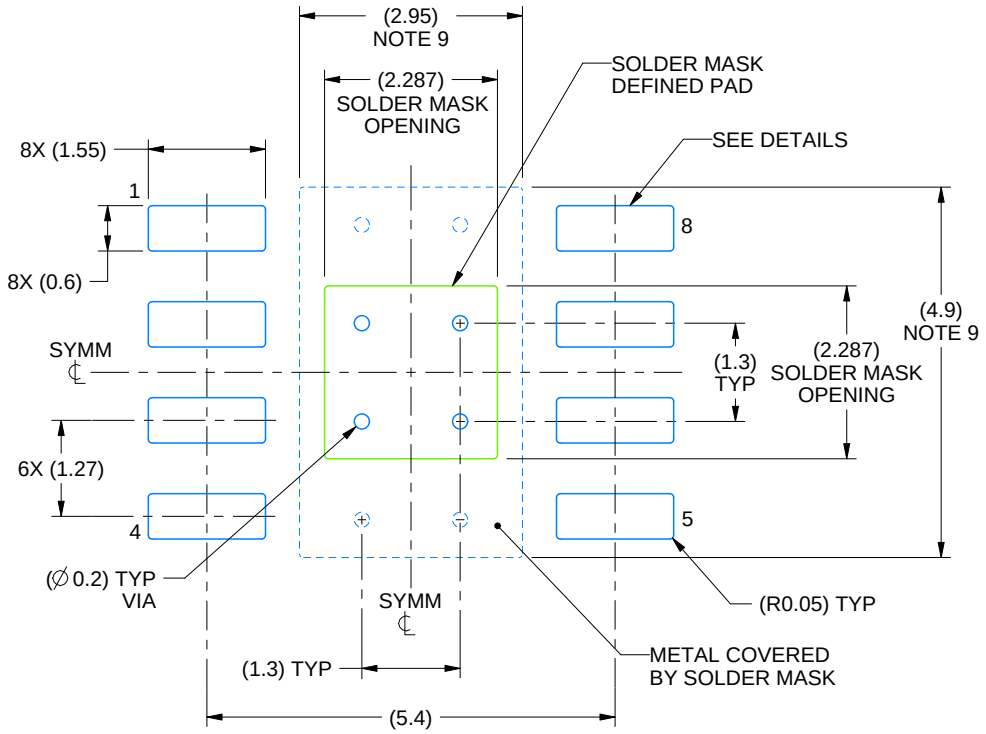
PLASTIC SMALL OUTLINE



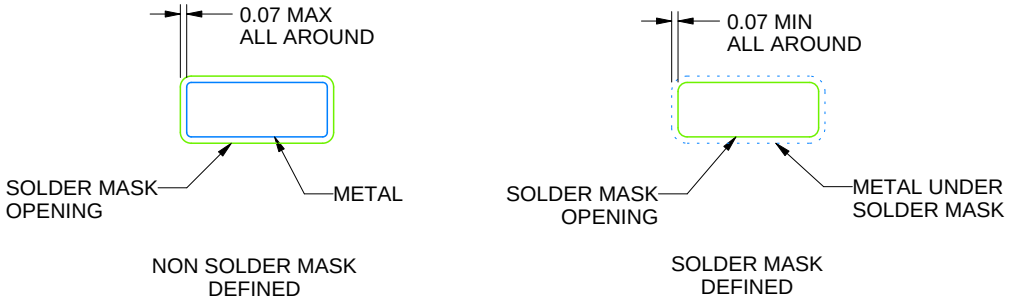
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

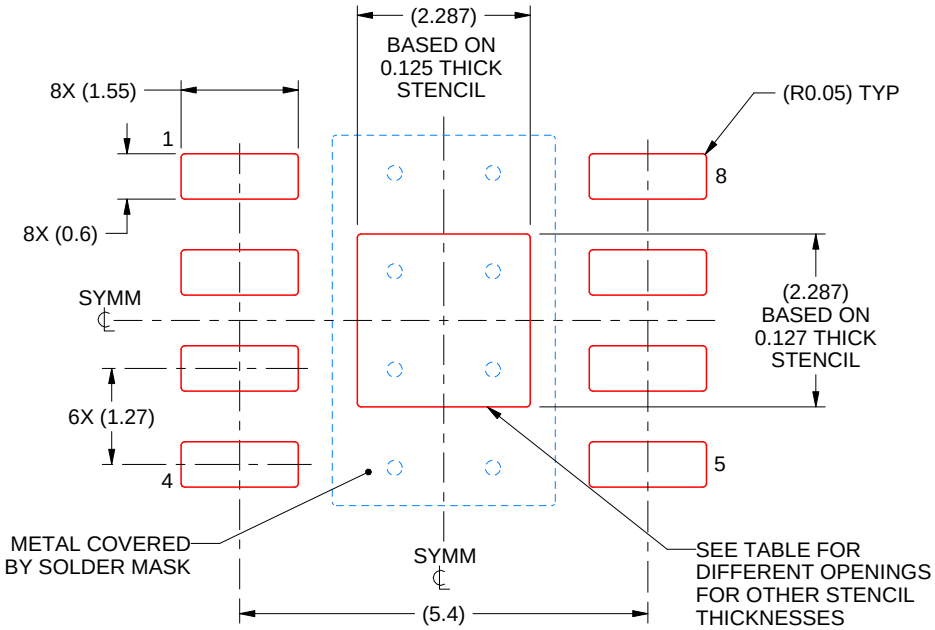


SOLDER MASK DETAILS

4218820/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.557 X 2.557
0.125	2.287 X 2.287 (SHOWN)
0.150	2.088 X 2.088
0.175	1.933 X 1.933

4218820/A 12/2022

NOTES: (continued)

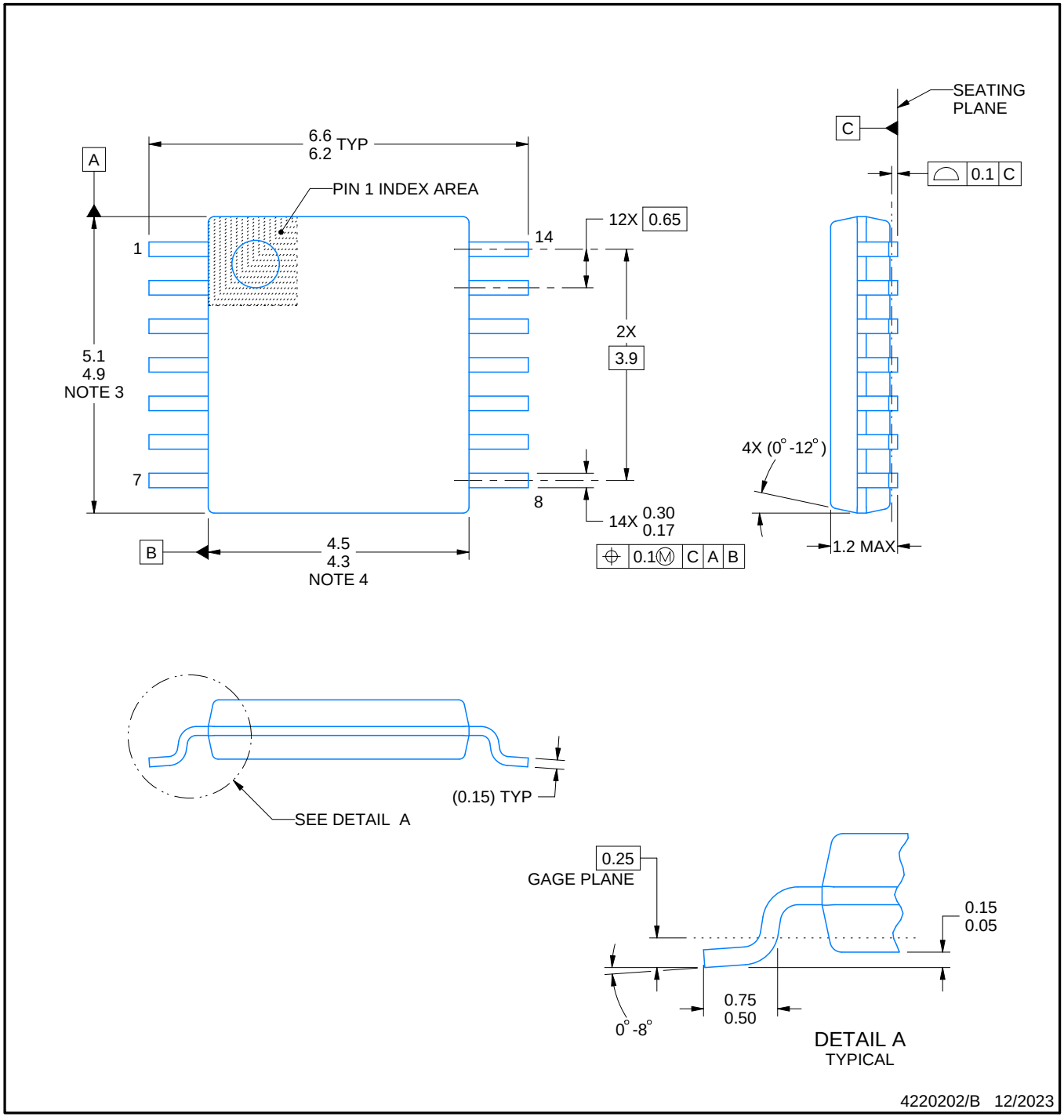
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

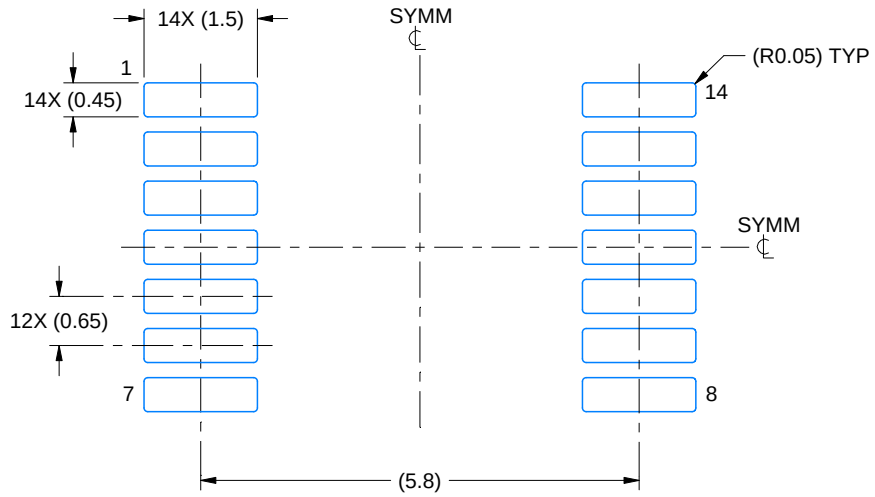
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

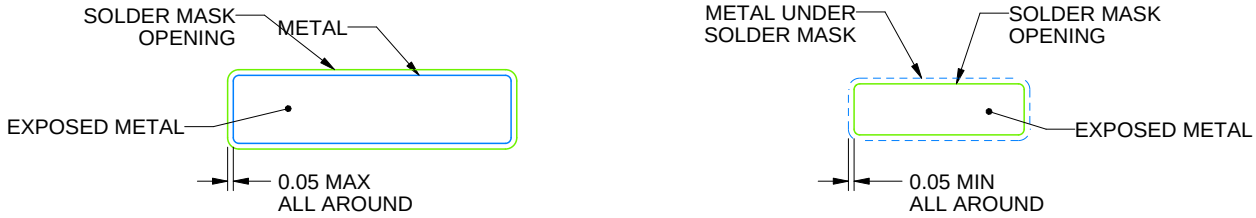


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

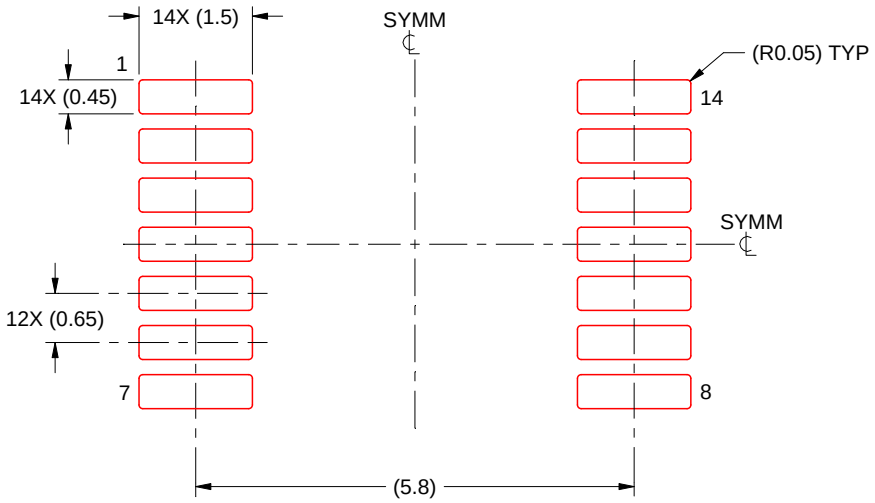


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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