OPAx376-Q1 Low-Noise, Low Quiescent Current, Precision e-trim™ Operational Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional-Safety Capable
  - Documentation available to aid functional safety system design (OPA376-Q1 and OPA2376-Q1)
- Low noise: 7.5 nV/√Hz at 1 kHz
- 0.1-Hz to 10-Hz noise: 0.8 μV_{PP}
- Quiescent current: 760 µA (typical)
- Low offset voltage: 5 µV (typical)
- Gain bandwidth product: 5.5 MHz
- Rail-to-rail input and output
- Single-supply operation
- Supply voltage: 2.2 V to 5.5 V
- Space-saving packages:
  - SC70, SOT-23, VSSOP, TSSOP

2 Applications

- Onboard (OBC) and wireless charger
- Inverter and motor control
- DC/DC converter
- Battery management system (BMS)

3 Description

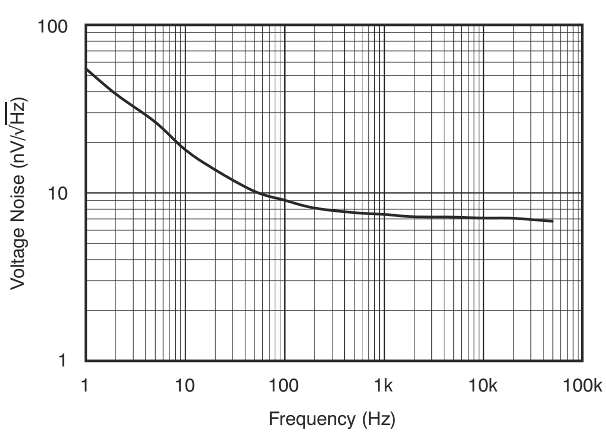
The OPAx376-Q1 family represents a new generation of low-noise e-trim™ operational amplifiers, offering outstanding dc precision and ac performance. Rail-to-rail output, low offset (25 µV maximum), low noise (7.5 nV/√Hz), quiescent current of 950 µA (maximum), and a 5.5-MHz bandwidth make this device very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent PSRR, making the OPA376-Q1 an excellent choice for applications that run directly from batteries without regulation.

The OPA376-Q1 (single version) is available in MicroSIZE SC70-5, SOT23-5, and SOIC-8 packages. The OPA2376-Q1 (dual) is offered in the SOIC-8 and VSSOP-8 package. The OPA4376-Q1 (quad) is offered in a TSSOP-14 package. All versions are specified for operation from –40°C to +125°C.

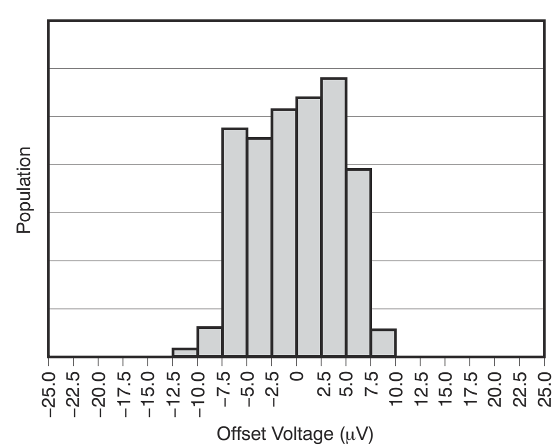
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA376-Q1	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA2376-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4376-Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Input Voltage Noise Spectral Density



Offset Voltage Production Distribution

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2016) to Revision C (March 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document......1
- Deleted HBM and CDM classification levels from *Features* and moved to *ESD Ratings*......1
- Added functional safety links to *Features*......1
- Changed *Applications* bullets......1
- Changed *ESD Ratings* to show HBM and CDM classification levels......6
- Added Figure 6-8, *Common-Mode Voltage vs Temperature*......9
- Added Figure 6-9, *Offset Voltage vs Common-Mode Voltage*......9

Changes from Revision A (January 2016) to Revision B (May 2016) **Page**

- Updated *Applications* examples......1
- Updated the *Pin Functions Table* for OPA4376-Q1......3
- Updated *HBM ESD Rating*......6
- Changed units on *Channel Separation*......8
- Deleted the temperature range parameters from the *Electrical Characteristics* table......8
- Removed section regarding *WCSP photosensitivity*......21

Changes from Revision * (April 2011) to Revision A (January 2016) **Page**

- Added *Pin Functions* table, *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section......1
- Released the OPA2376-Q1 device as *Production Data*......1
- Added the *Input Offset Voltage and Input Offset Voltage Drift* section to the *Feature Description*......13

5 Pin Configuration and Functions

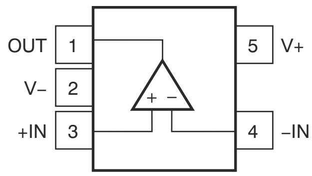


Figure 5-1. OPA376-Q1: DBV (5-Pin SOT-23) Package, Top View

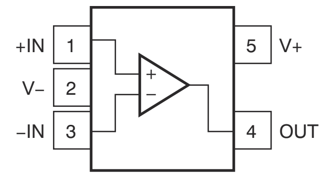
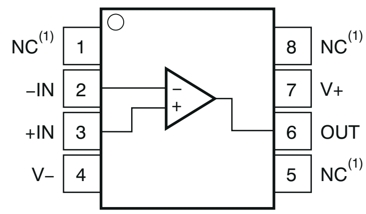


Figure 5-2. OPA376-Q1: DCK (5-Pin SC70) Package, Top View



(1) NC denotes no internal connection.

Figure 5-3. OPA376-Q1: D (8-Pin SOIC) Package, Top View

Table 5-1. Pin Functions: OPA376-Q1

PIN				I/O	DESCRIPTION
NAME	NO.				
	SOT-23	SC70	SOIC		
+IN	3	1	3	I	Noninverting input^{+}
–IN	4	3	2	I	Inverting input$^{–}$
NC	—	—	1, 5, 8	—	No internal connection
OUT	1	4	6	O	Output
V+	5	5	7	—	Positive (highest) power supply^{+}
V–	2	2	4	—	Negative (lowest) power supply$^{–}$

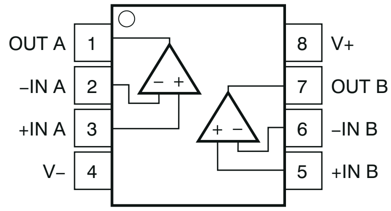


Figure 5-4. OPA2376-Q1: D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

Table 5-2. Pin Functions: OPA2376-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A+
–IN A	2	I	Inverting input, channel A–
+IN B	5	I	Noninverting input, channel B+
–IN B	6	I	Inverting input, channel B–
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

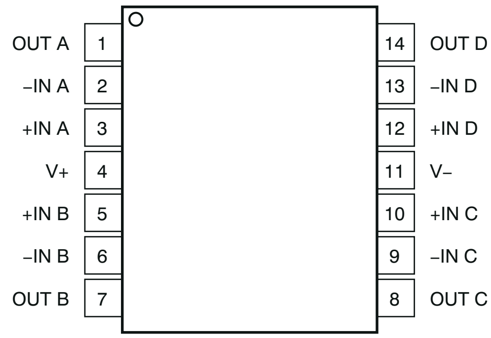


Figure 5-5. OPA4376-Q1: PW (14-Pin TSSOP) Package, Top View

Table 5-3. Pin Functions: OPA4376-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A^{+}
–IN A	2	I	Inverting input, channel A^{-}
+IN B	5	I	Noninverting input, channel B^{+}
–IN B	6	I	Inverting input, channel B^{-}
+IN C	10	I	Noninverting input, channel C^{+}
–IN C	9	I	Inverting input, channel C^{-}
+IN D	12	I	Noninverting input, channel D^{+}
–IN D	13	I	Inverting input, channel D^{-}
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage		7	V
	Signal input pin voltage[2]	(V–) – 0.5	(V+) + 0.5	V
	Signal input pin current[2]	–10	10	mA
	Output short-circuit current[3]	Continuous		
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD classification level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage	2.2 (±1.1)	5.5 (±2.75)	V
T_A	Operating temperature	–40	150	°C

6.4 Thermal Information: OPA376-Q1

THERMAL METRIC[(1)]		OPA376-Q1 DCK (SC70) 5 PINS	OPA376-Q1 DBV (SOT-23) 5 PINS	OPA376-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	267	273.8	100.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.9	126.8	42.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	85.9	41	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	10.9	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.1	84.9	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2376-Q1

THERMAL METRIC[(1)]		OPA2376-Q1 D (SOIC) 8 PINS	OPA2376-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	63.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.5	9.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.2	91.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4376-Q1

THERMAL METRIC[(1)]		OPA4376-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				5	25	µV
dV_{OS}/dT	Input offset voltage versus temperature	T_A = –40°C to +85°C			0.26	1	µV/°C
		T_A = –40°C to +125°C			0.32	2	µV/°C
PSRR	Input offset voltage versus power supply	V_S = 2.2 V to 5.5 V, V_{CM} < (V+) – 1.3 V	T_A = 25°C		5	20	µV/V
			T_A = –40°C to +125°C		5		µV/V
	Channel separation, dc (dual, quad)				0.5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			0.2	10	pA
		T_A = –40°C to +125°C			See *Section 6.8*		pA
I_{OS}	Input offset current				0.2	10	pA
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.8		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz			7.5		$nV/\sqrt{Hz}$
i_n	Input current noise	f = 1 kHz			2		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	See *Figure 6-8*		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.3 V		76	90		dB
INPUT CAPACITANCE							
	Differential				6.5		pF
	Common-mode				13		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	50 mV < V_O < (V+) – 50 mV, R_L = 10 kΩ		120	134		dB
		100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ		120	126		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 100 pF, V_S = 5.5 V			5.5		MHz
SR	Slew rate	G = 1, C_L = 100 pF, V_S = 5.5 V			2		V/µs
t_S	Settling time	0.1%, 2-V Step , G = 1, C_L = 100 pF, V_S = 5.5 V			1.6		µs
		0.01%, 2-V Step , G = 1, C_L = 100 pF, V_S = 5.5 V			2		µs
	Overload recovery time	V_{IN} × Gain > V_S			0.33		µs
THD+N	THD + noise	V_O = 1 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ			0.00027%		
OUTPUT							
	Voltage output swing from rail	R_L = 10 kΩ	T_A = 25°C		10	20	mV
			T_A = –40°C to +125°C			40	mV
		R_L = 2 kΩ	T_A = 25°C		40	50	mV
			T_A = –40°C to +125°C			80	mV
I_{SC}	Short-circuit current				30 / –50		mA
C_{LOAD}	Capacitive load drive				See *Section 6.8*		
R_O	Open-loop output impedance				150		Ω
POWER SUPPLY							
V_S	Specified voltage			2.2		5.5	V
	Operating voltage				2 to 5.5		V
I_Q	Quiescent current per amplifier	I_O = 0, V_S = 5.5 V, V_{CM} < (V+) – 1.3 V	T_A = 25°C		760	950	µA
			T_A = –40°C to +125°C			1	mA

6.8 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

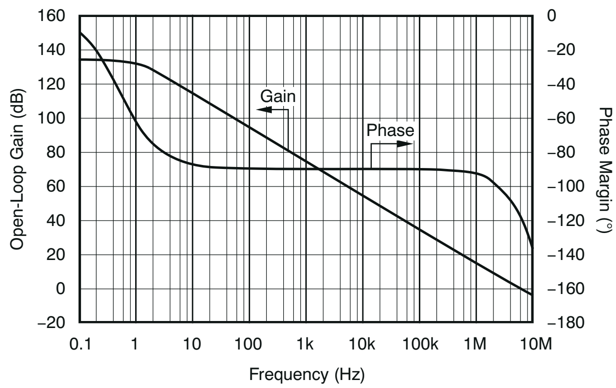


Figure 6-1. Open-Loop Gain and Phase vs Frequency

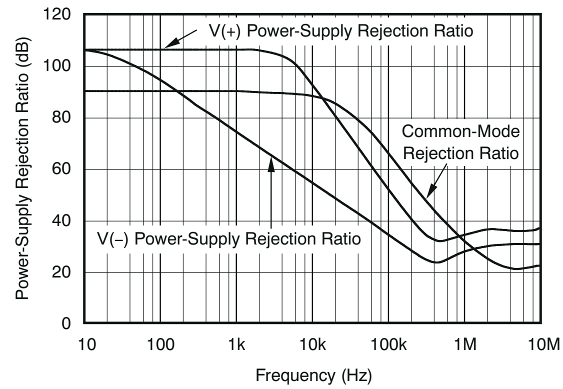


Figure 6-2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

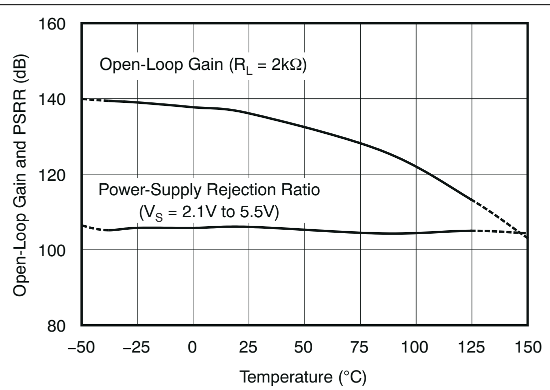


Figure 6-3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

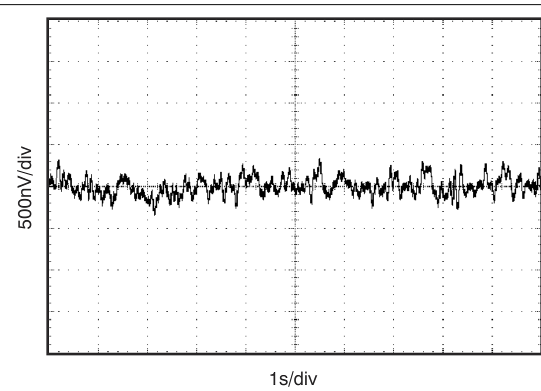


Figure 6-4. 0.1-Hz to 10-Hz Input Voltage Noise

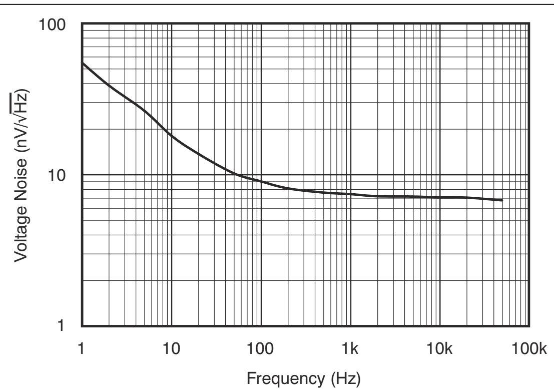


Figure 6-5. Input Voltage Noise Spectral Density

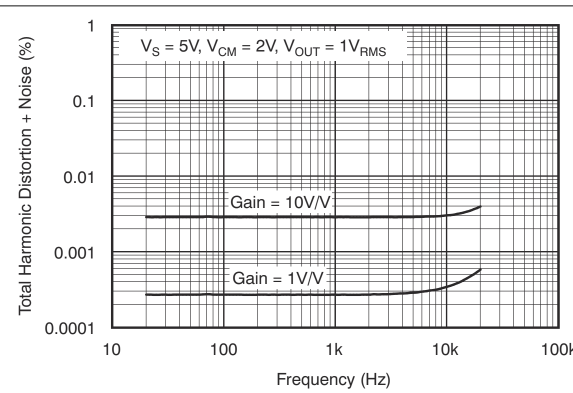


Figure 6-6. Total Harmonic Distortion + Noise vs Frequency

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

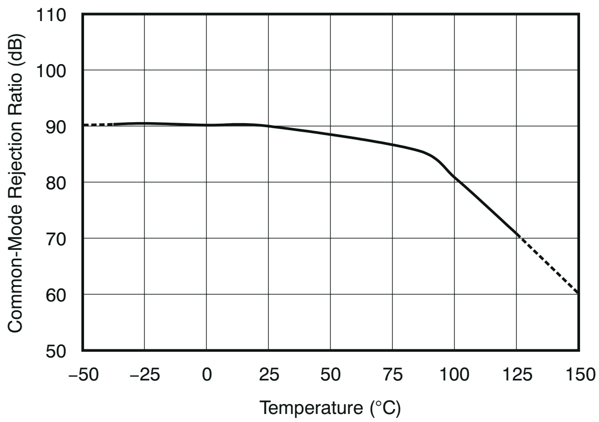


Figure 6-7. Common-Mode Rejection Ratio vs Temperature

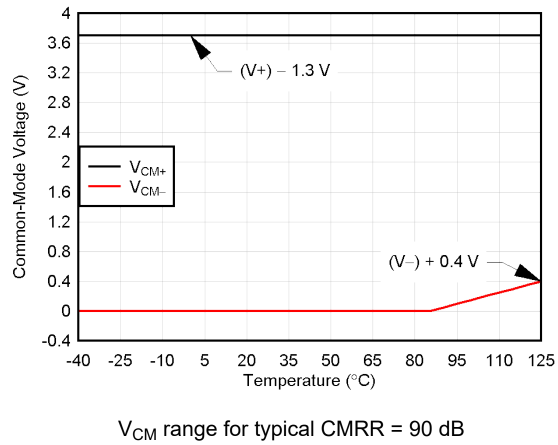


Figure 6-8. Common-Mode Voltage vs Temperature

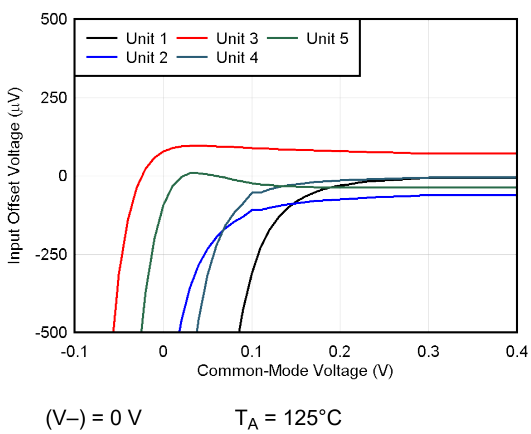


Figure 6-9. Offset Voltage vs Common-Mode Voltage

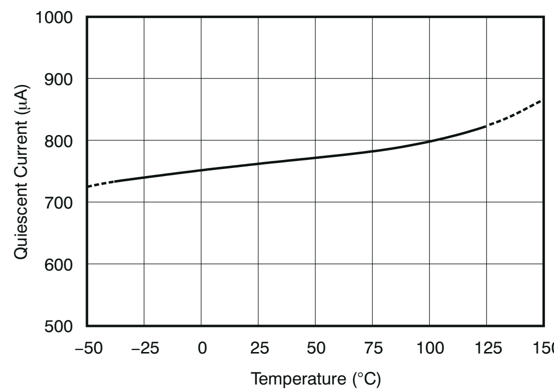


Figure 6-10. Quiescent Current vs Temperature

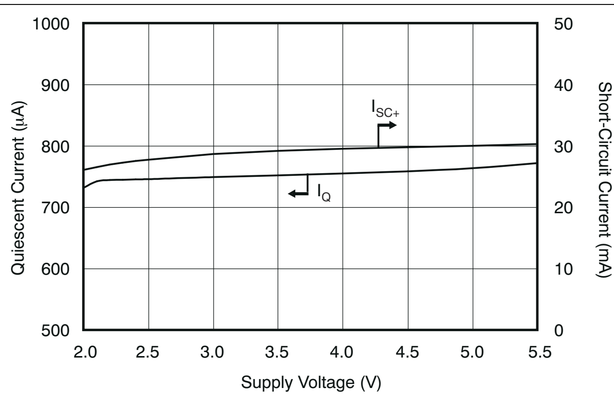


Figure 6-11. Quiescent and Short-Circuit Current vs Supply Voltage

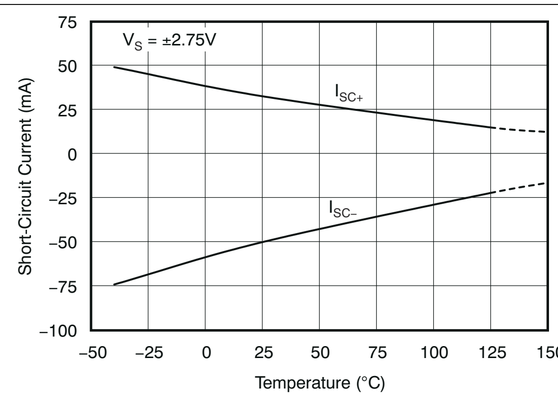


Figure 6-12. Short-Circuit Current vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

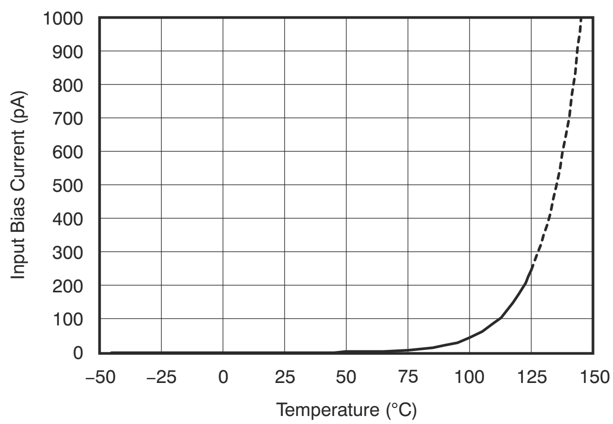


Figure 6-13. Input Bias Current vs Temperature

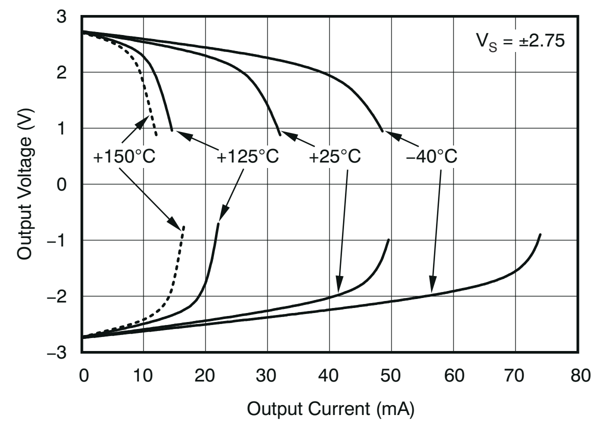


Figure 6-14. Output Voltage vs Output Current

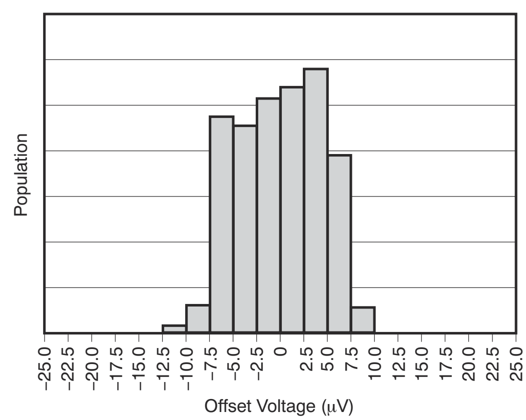


Figure 6-15. Offset Voltage Production Distribution

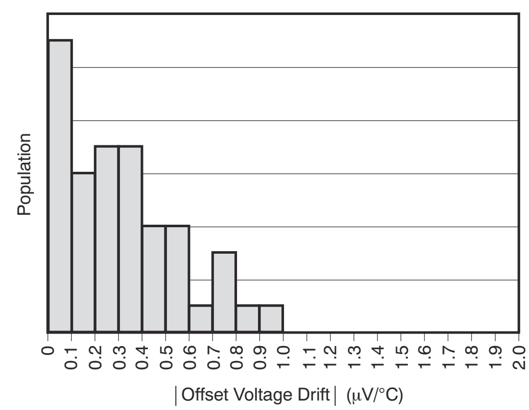


Figure 6-16. Offset Voltage Drift Production Distribution (–40°C to +125°C)

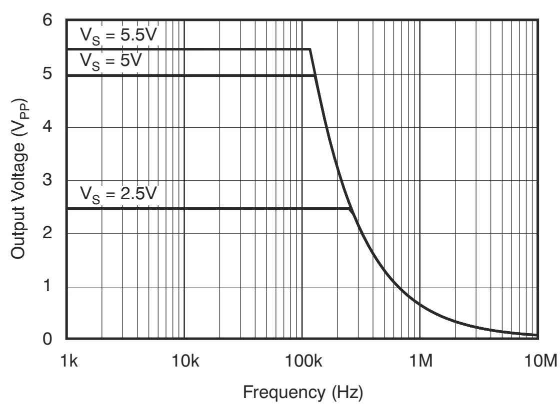


Figure 6-17. Maximum Output Voltage vs Frequency

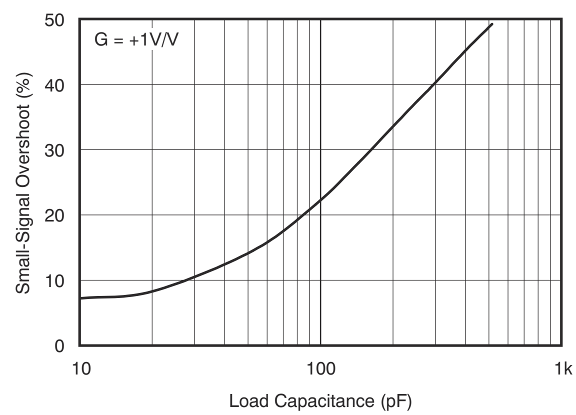


Figure 6-18. Small-Signal Overshoot vs Load Capacitance

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

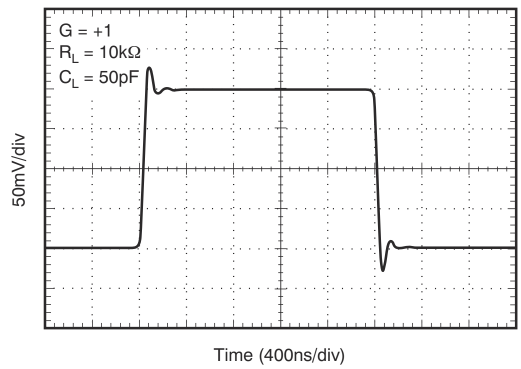


Figure 6-19. Small-Signal Pulse Response

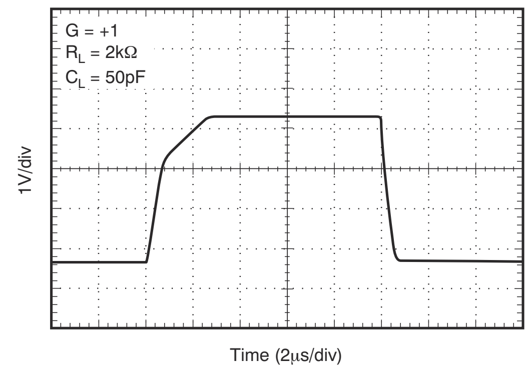


Figure 6-20. Large-Signal Pulse Response

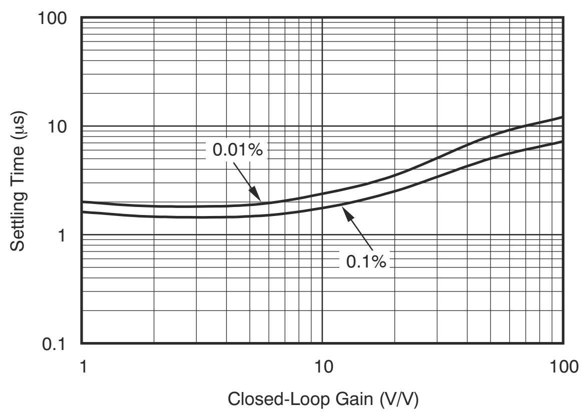


Figure 6-21. Settling Time vs Closed-Loop Gain

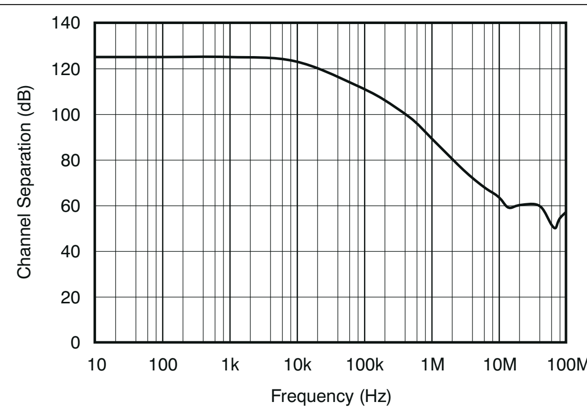


Figure 6-22. Channel Separation vs Frequency

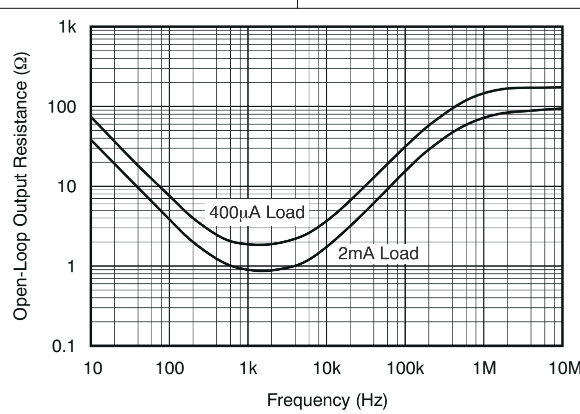


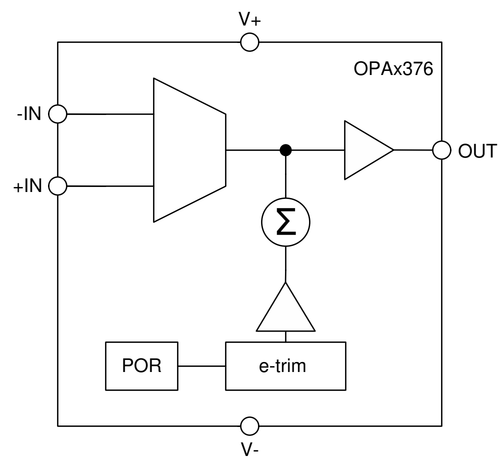
Figure 6-23. Open-Loop Output Resistance vs Frequency

7 Detailed Description

7.1 Overview

The OPAx376-Q1 family belongs to a new generation of low-noise e-trim operational amplifiers, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, low offset, and drawing a low quiescent current, make these devices an excellent choice for a variety of precision and portable applications. In addition, these devices have a wide supply range with excellent PSRR, making the OPAx376-Q1 a great option for applications that are battery powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx376-Q1 family of precision amplifiers offers excellent dc performance as well as excellent ac performance. Operating from a single power-supply the OPAx376-Q1 is capable of driving large capacitive loads, has a wide input common-mode voltage range, and is well-suited to drive the inputs of successive-approximation response (SAR) analog-to-digital converters (ADCs) as well as 24-bit and higher resolution converters. Including internal ESD protection, the OPAx376-Q1 family is offered in a variety of industry-standard packages, including a wafer chip-scale package for applications that require space savings.

7.3.1 Operating Voltage

The OPAx376-Q1 family of amplifiers operate over a power-supply range of 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 6.8*.

7.3.2 Input Offset Voltage and Input Offset Voltage Drift

The OPAx376-Q1 family of e-trim operational amplifiers is manufactured using TI's proprietary trim technology, a method of trimming internal device parameters during either wafer probing or final testing. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift.

7.3.3 Capacitive Load and Stability

The OPAx376-Q1 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx376-Q1 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is be stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

The OPAx376 in a unity-gain configuration can directly drive up to 250 pF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot Figure 6-18, *Small-Signal Overshoot vs Load Capacitance*. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 7-1. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S / R_L, and is generally negligible at low output current levels.

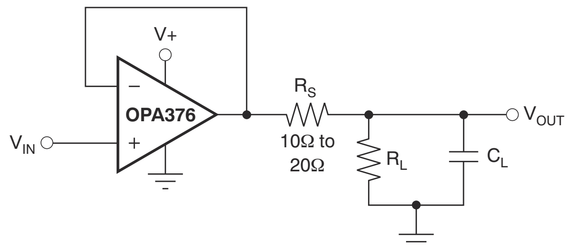


Figure 7-1. Improving Capacitive Load Drive

7.3.4 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx376-Q1 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is very low, from approximately (V–) to (V+) – 1 V, as shown in Figure 7-2. The offset voltage increases as common-mode voltage exceeds (V+) –1 V. Common-mode rejection is specified from (V–) to (V+) – 1.3 V.

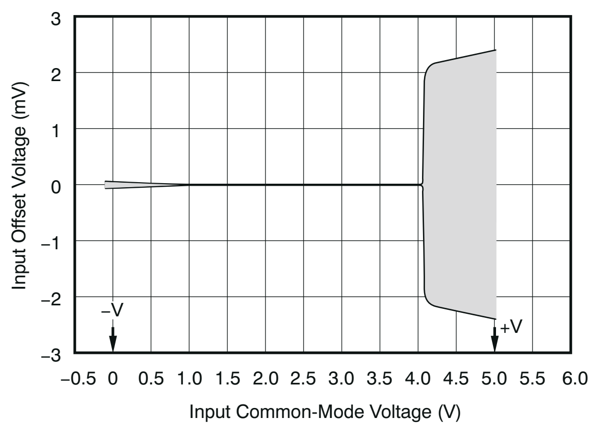


Figure 7-2. Offset and Common-Mode Voltage

7.3.5 Input and ESD Protection

The OPAx376-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in *Section 6.1*.

Figure 7-3 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.

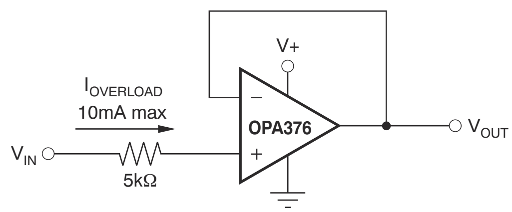


Figure 7-3. Input Current Protection

7.4 Device Functional Modes

The OPAx376-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPAx376-Q1 is 5.5 V (±2.75 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx376-Q1 family of e-trim operational amplifiers is built using a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. This technique compensates for performance shifts that can occur during the molding process. Through *e-trim* operational amplifier technology, the OPAx376-Q1 family delivers excellent offset voltage (5 µV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. These 5.5-MHz CMOS op amps operate on 760 µA (typical) quiescent current.

8.1.1 Basic Amplifier Configurations

The OPAx376-Q1 family is unity-gain stable. It does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 8-1. The OPA376-Q1 is configured as a basic inverting amplifier with a gain of –10 V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown in Figure 8-1, this voltage is 2.5 V, but may be any value within the common-mode input voltage range.

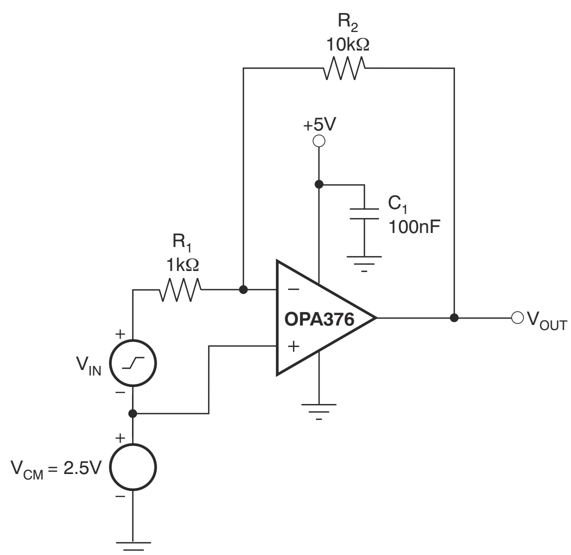


Figure 8-1. Basic Single-Supply Connection

8.1.2 Active Filtering

The OPA376-Q1 series is well-suited for filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 8-2 shows a 50-kHz, second-order, low-pass filter. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an ADC.

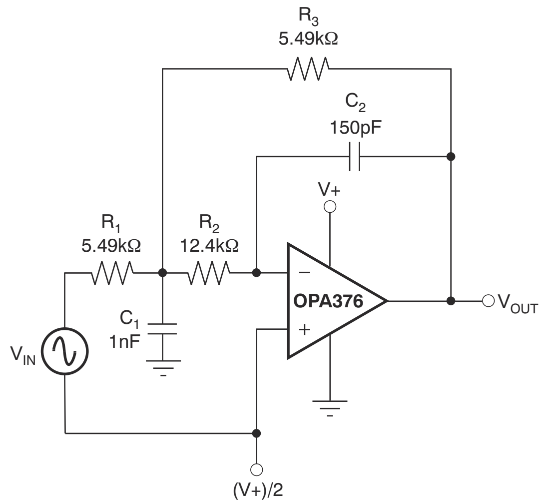
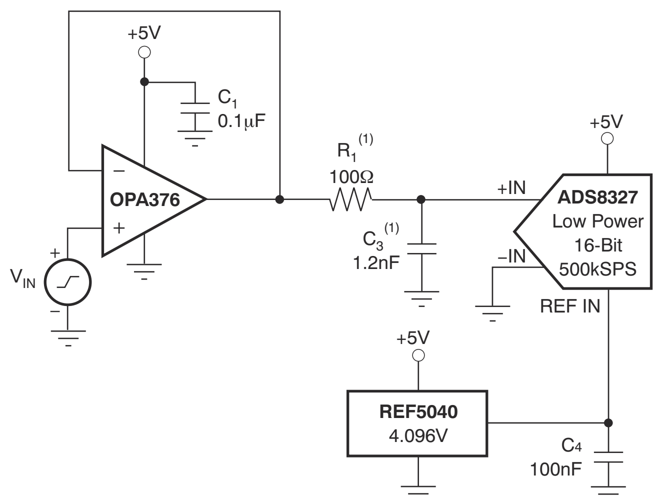


Figure 8-2. Second-Order Butterworth, 50-kHz Low-Pass Filter

8.1.3 Driving an Analog-to-Digital Converter

The low noise and wide gain bandwidth of the OPA376-Q1 family make it an ideal driver for ADCs. Figure 8-3 illustrates the OPA376-Q1 driving an ADS8327, 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer.



(1) Suggested value; may require adjustment based on specific application.

Figure 8-3. Driving an ADS8327

8.1.4 Phantom-Powered Microphone

The circuit shown in Figure 8-4 depicts how a remote microphone amplifier can be powered by a phantom source on the output side of the signal cable. The cable serves double duty, carrying both the differential output signal from and dc power to the microphone amplifier stage.

An OPA2376-Q1 serves as a single-ended input to a differential output amplifier with a 6-dB gain. Common-mode bias for the two op amps is provided by the dc voltage developed across the electret microphone element. A 48-V phantom supply is reduced to 5.1 V by the series 6.8-kΩ resistors on the output side of the cable, and the 4.7-kΩ resistors and zener diode on the input side of the cable. AC coupling blocks the different dc voltage levels from each other on each end of the cable.

An INA163 instrumentation amplifier provides differential inputs and receives the balanced audio signals from the cable.

The INA163 gain may be set from 0 dB to 80 dB by selecting the R_G value. The INA163 circuit is typical of the input circuitry used in mixing consoles.

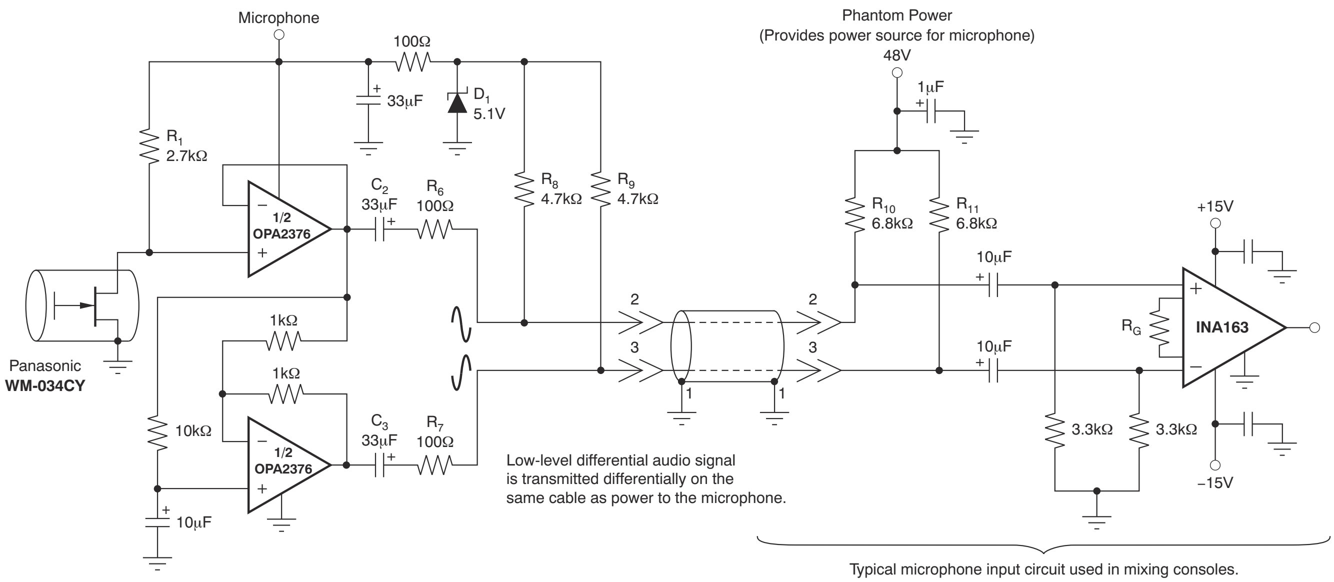
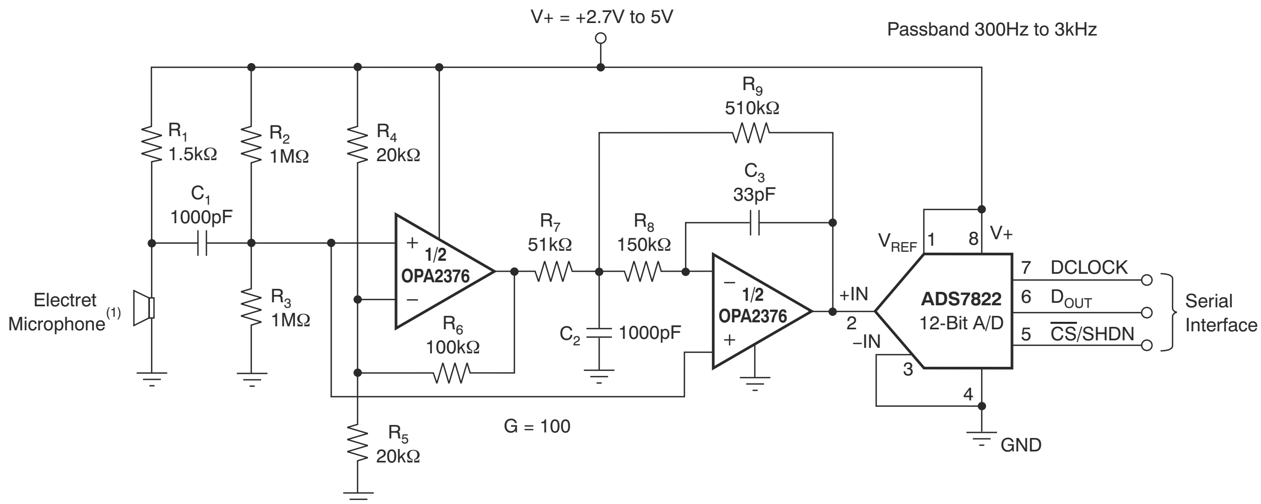


Figure 8-4. Phantom-Powered Electret Microphone

8.1.5 Speech Bandpass-Filtered Data Acquisition System

Figure 8-5 illustrates the OPA2376-Q1 driving a speech bandpass-filtered data acquisition system.



(1) Electret microphone powered by R_1.

Figure 8-5. OPA2376-Q1 as a Speech Bandpass-Filtered Data Acquisition System

8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA376-Q1 is ideally suited to construct high-speed, high-precision active filters. Figure 8-6 shows a second-order, low-pass filter commonly encountered in signal processing applications.

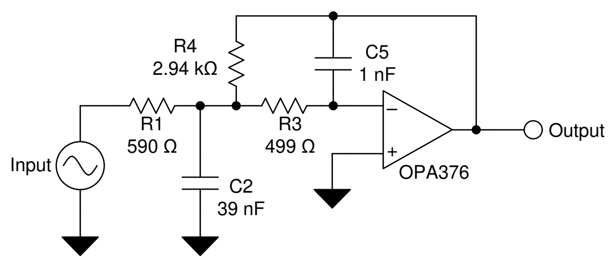


Figure 8-6. Typical Application Schematic

8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 8-6. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$
$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

8.2.3 Application Curve

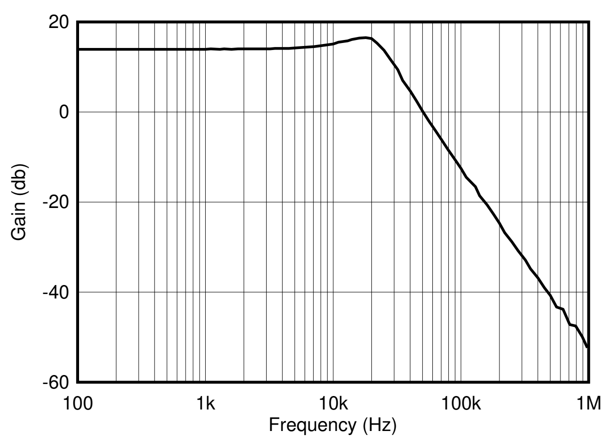


Figure 8-7. Low-Pass Filter Transfer Function

9 Power Supply Recommendations

The OPAx376-Q1 family of devices is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in Section 6.8.

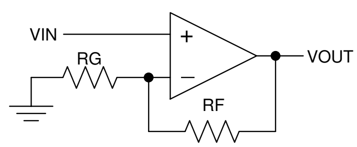
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to the *Circuit Board Layout Techniques* application report.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 10-1, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



(Schematic Representation)

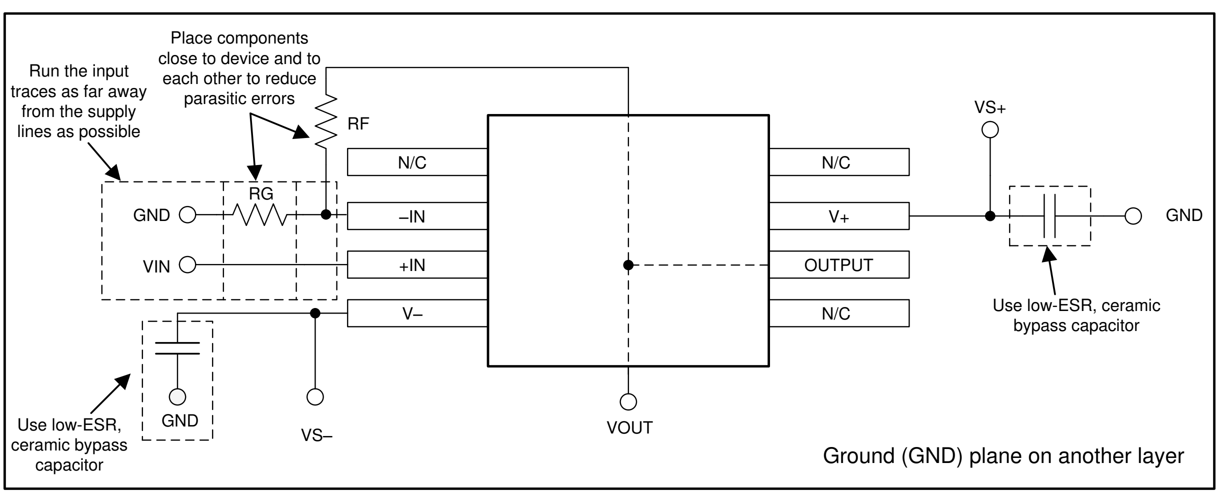


Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ simulation software is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA163 Low-Noise, Low-Distortion Instrumentation Amplifier* data sheet
- Texas Instruments, *Operational Amplifier Gain stability, Part 3: AC Gain-Error Analysis*
- Texas Instruments, *Operational Amplifier Gain Stability, Part 2: DC Gain-Error Analysis*
- Texas Instruments, *Op Amp Performance Analysis*
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes*
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers*
- Texas Instruments, *Tuning in Amplifiers*
- Texas Instruments, *Using Infinite-Gain, MFB Filter Topology in Fully Differential Active Filters*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

e-trim™, TINA-TI™, and TI E2E™ are trademarks of Texas Instruments.
TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2376AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2376Q1	Samples
OPA2376QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2376	Samples
OPA376AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUHQ	Samples
OPA4376AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4376Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

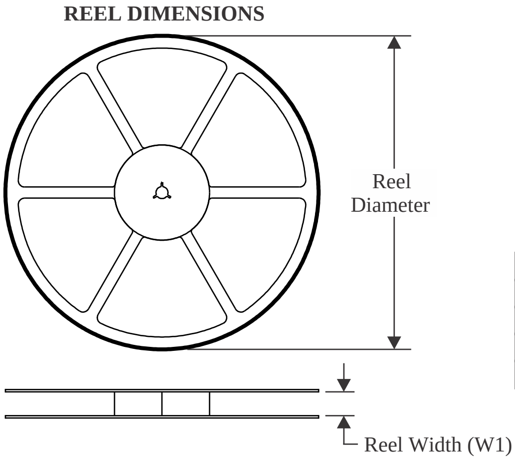
OTHER QUALIFIED VERSIONS OF OPA2376-Q1, OPA376-Q1, OPA4376-Q1 :

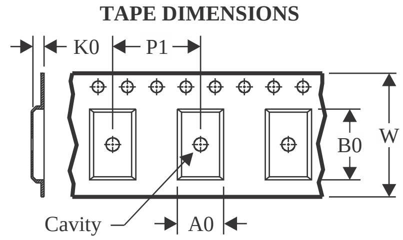
- Catalog: OPA2376, OPA376, OPA4376

NOTE: Qualified Version Definitions:

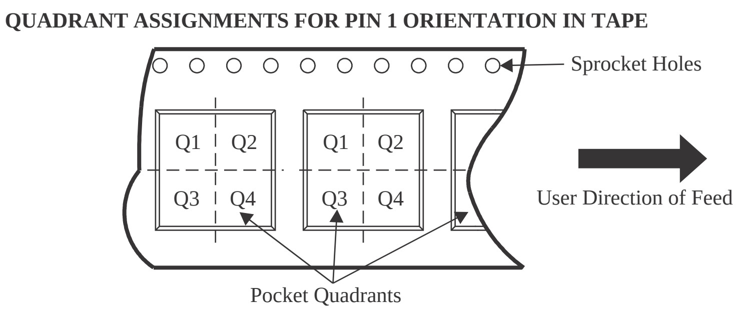
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





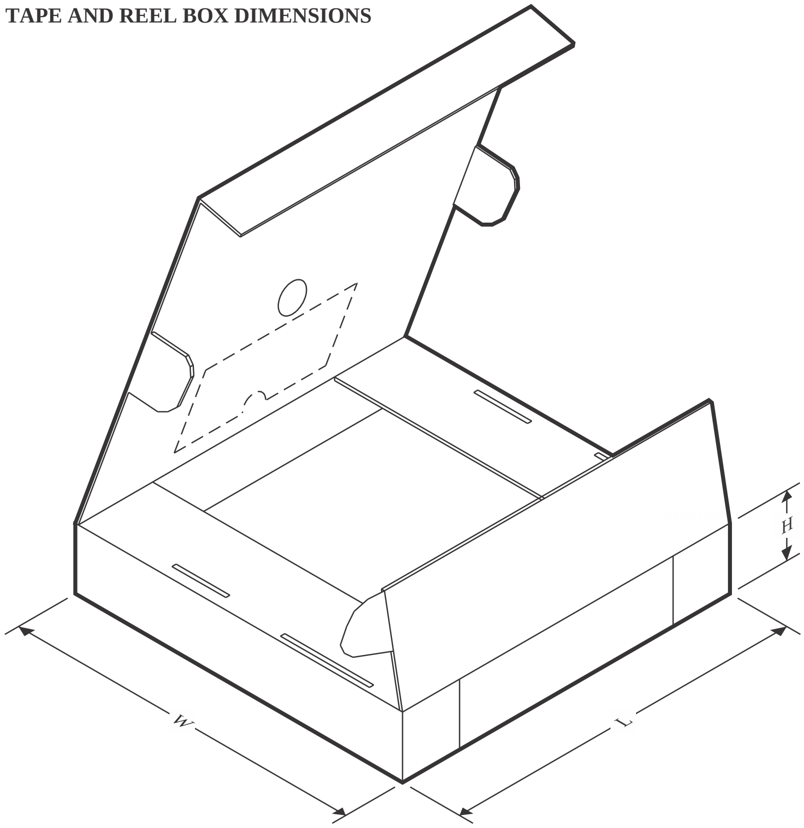
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2376AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2376QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA376AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA4376AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

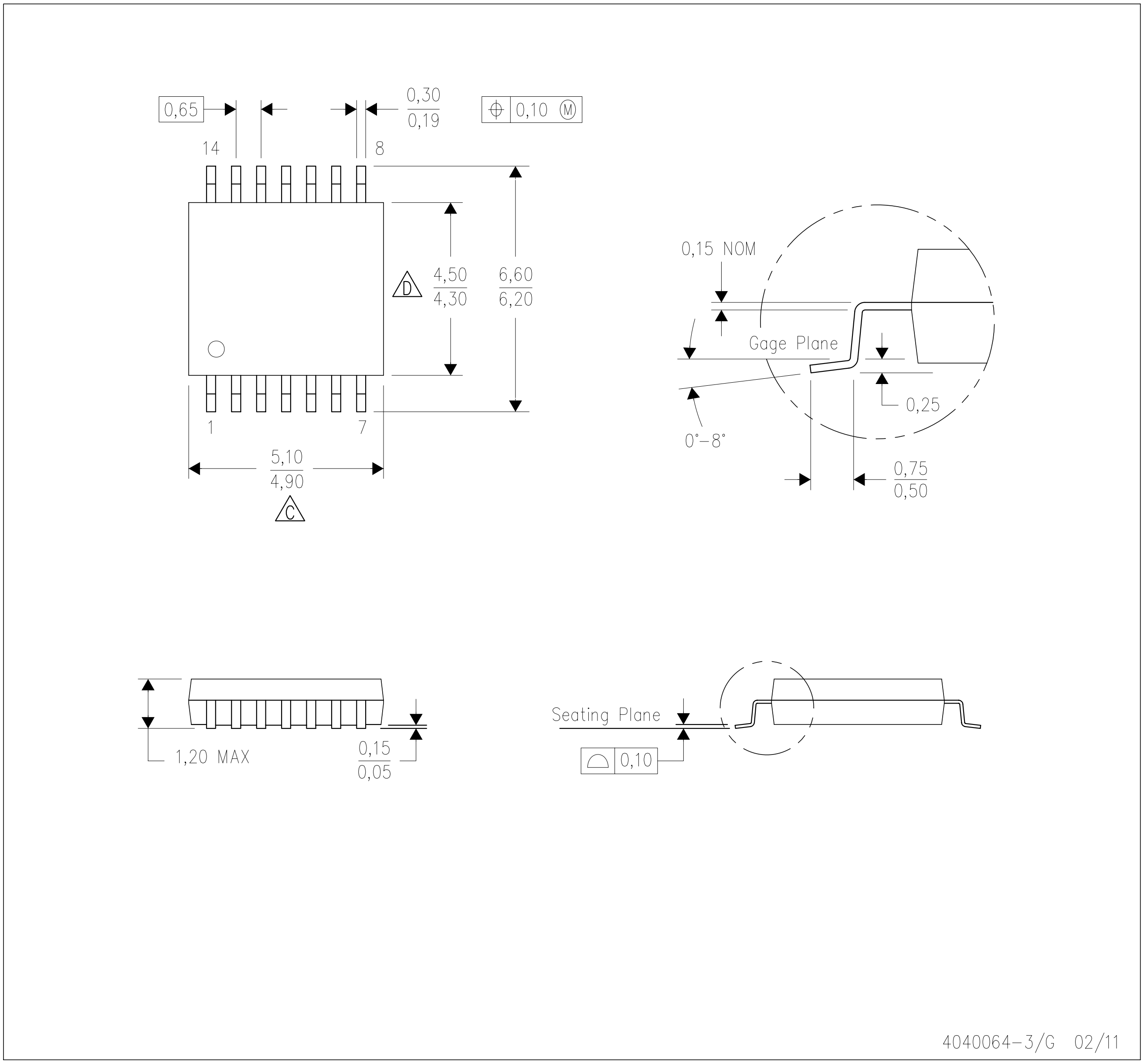
TAPE AND REEL BOX DIMENSIONS



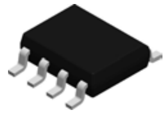
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2376AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
OPA2376QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA376AQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA4376AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

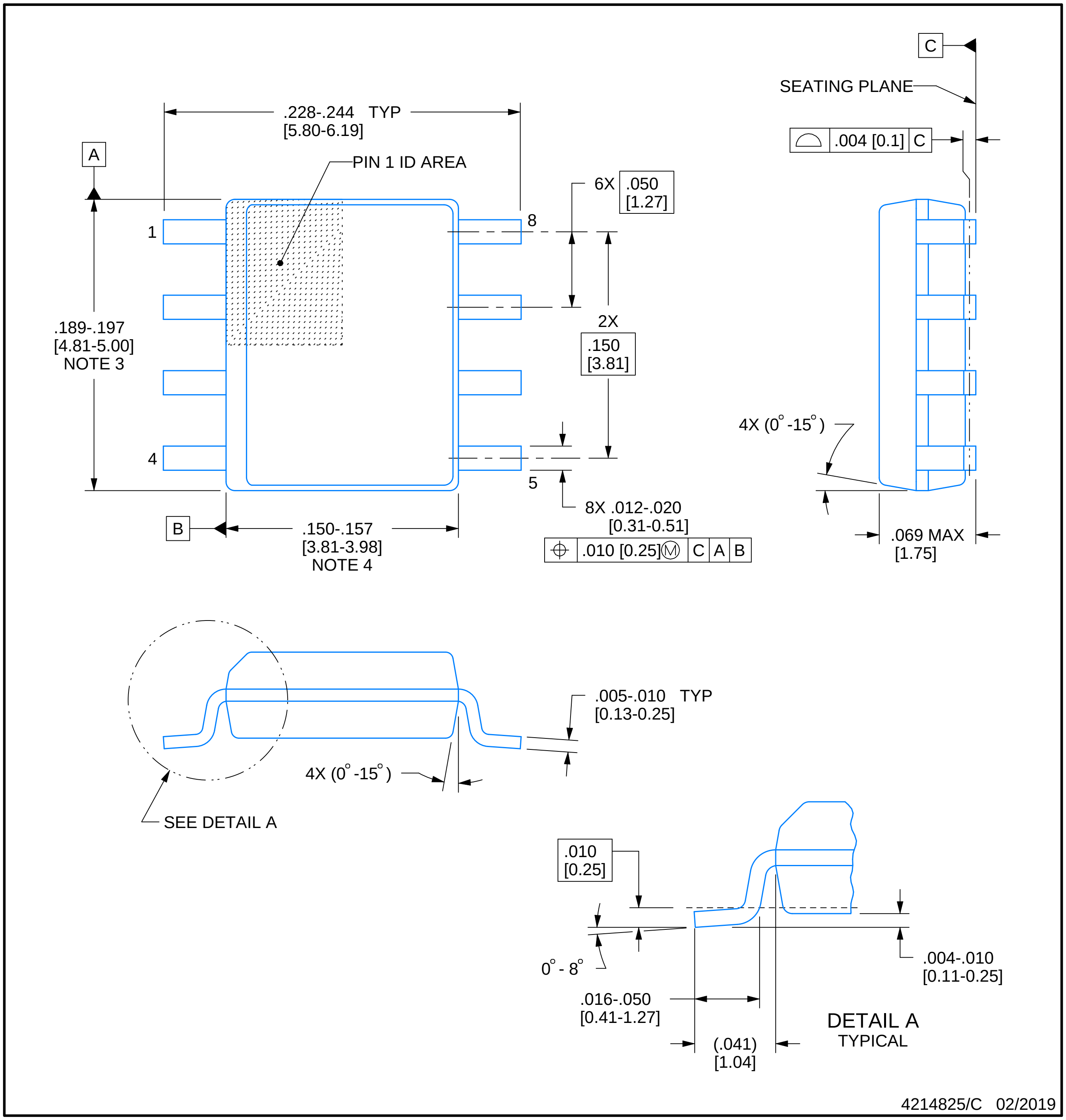


PACKAGE OUTLINE

D0008A

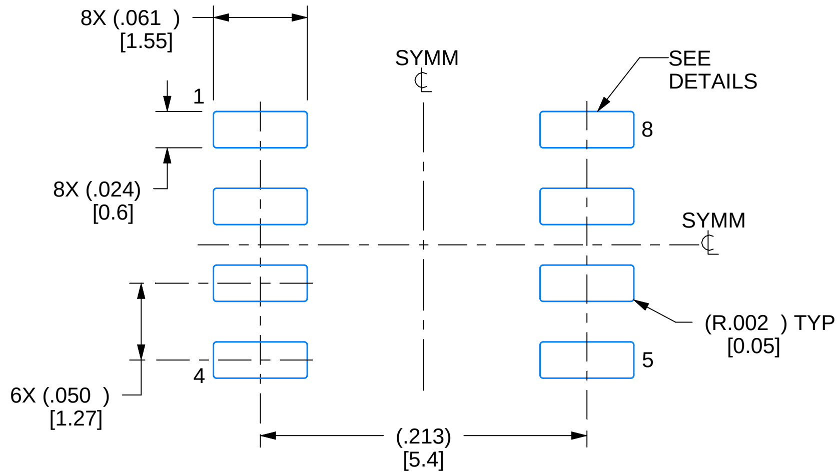
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

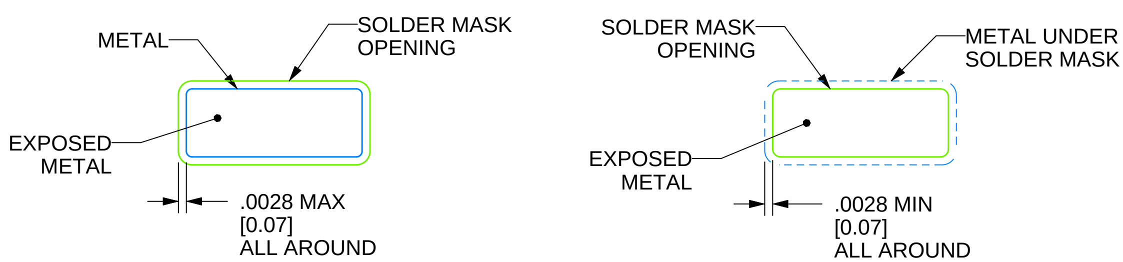


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

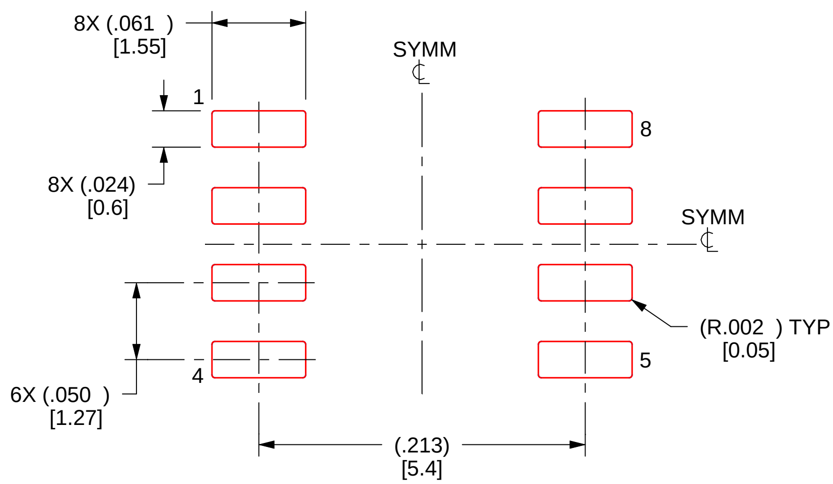
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

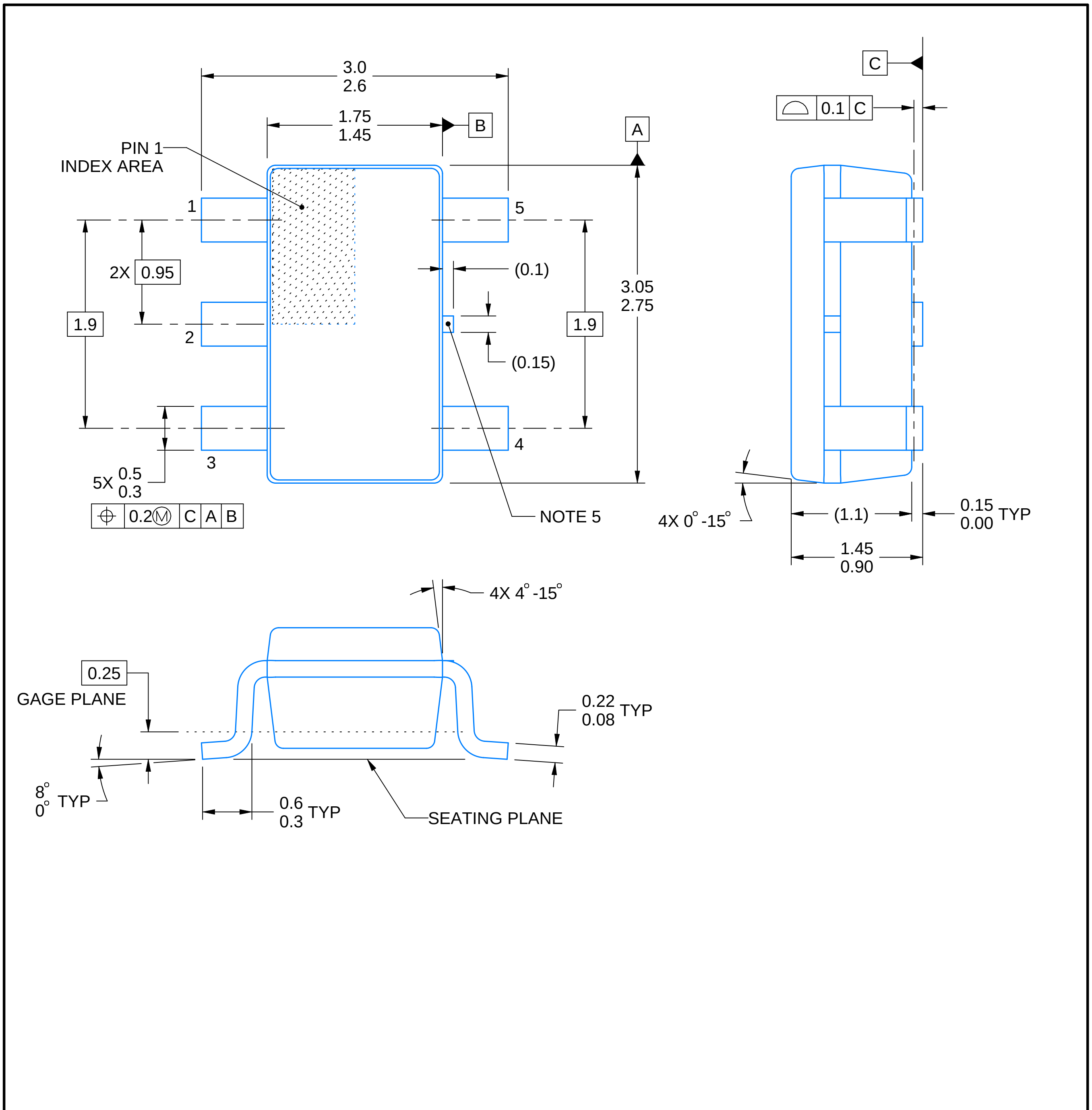


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

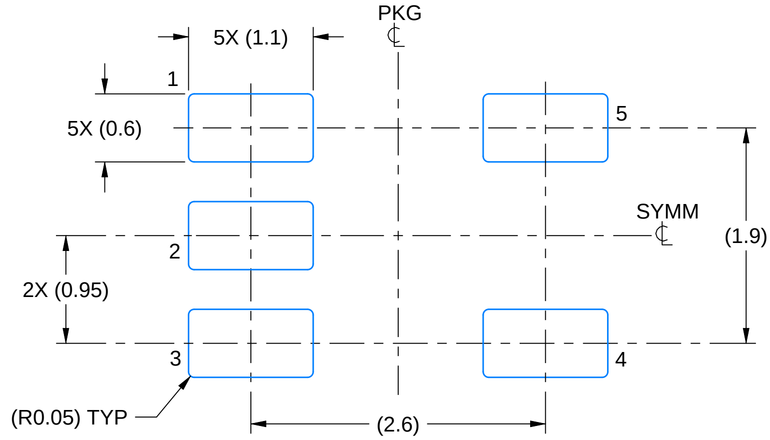
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



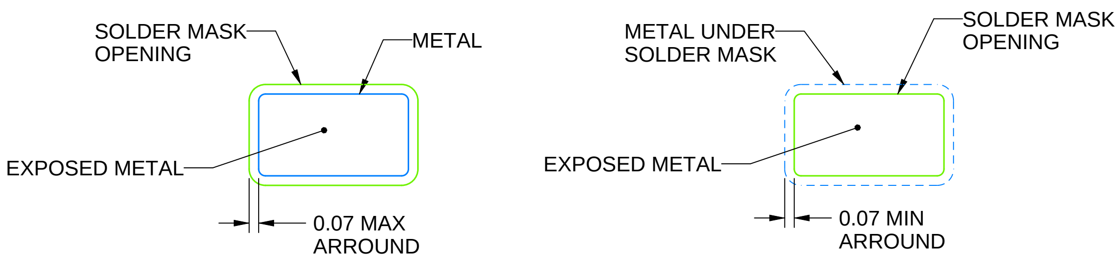
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

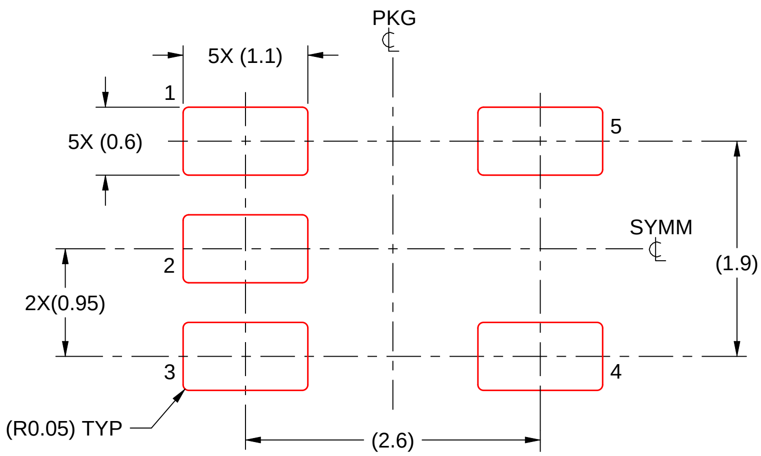
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



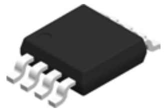
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

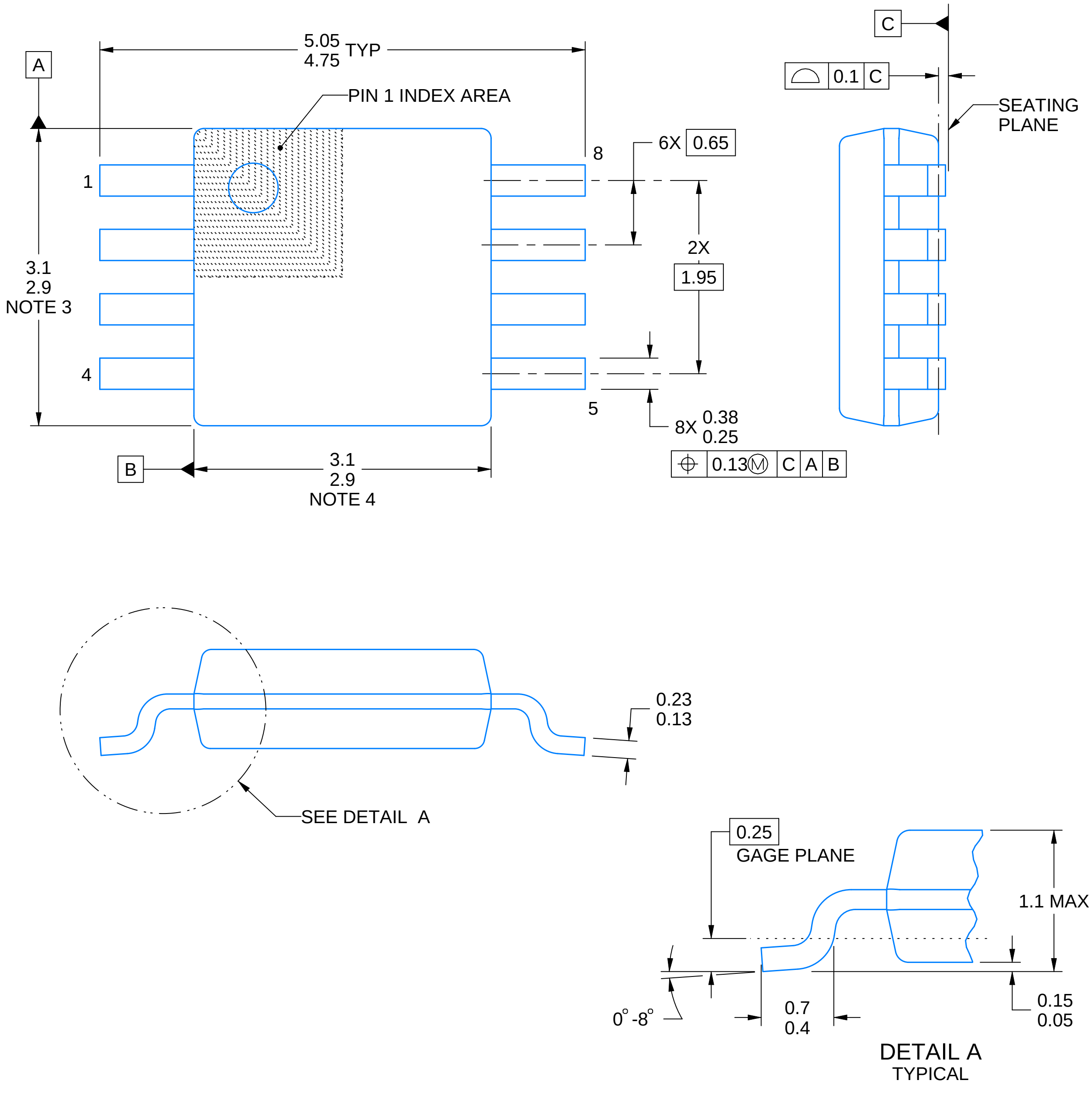
PACKAGE OUTLINE



DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

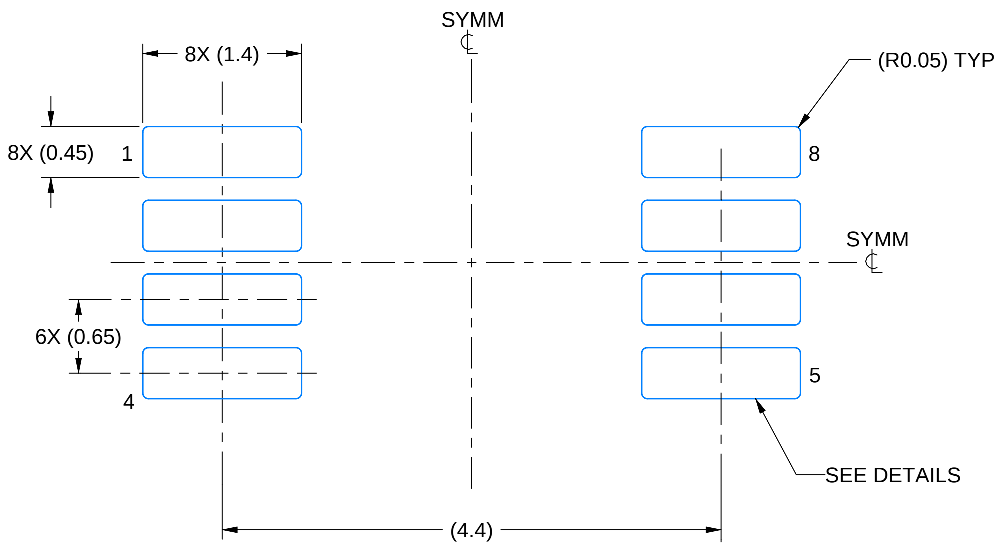


4214862/A 04/2023

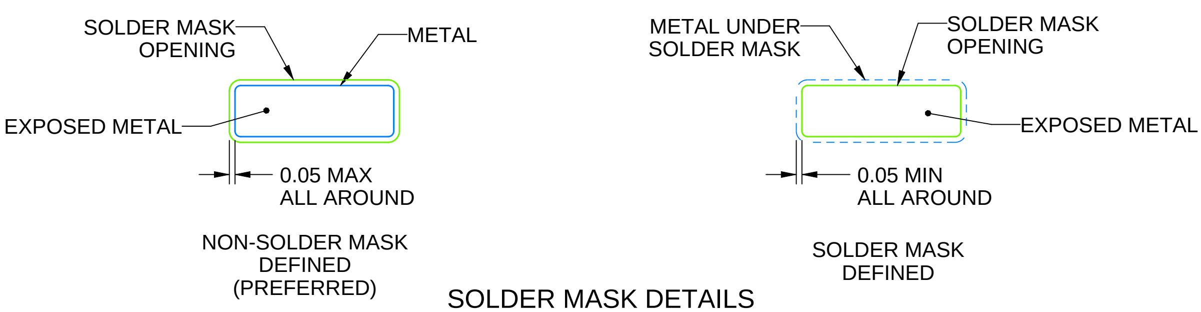
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

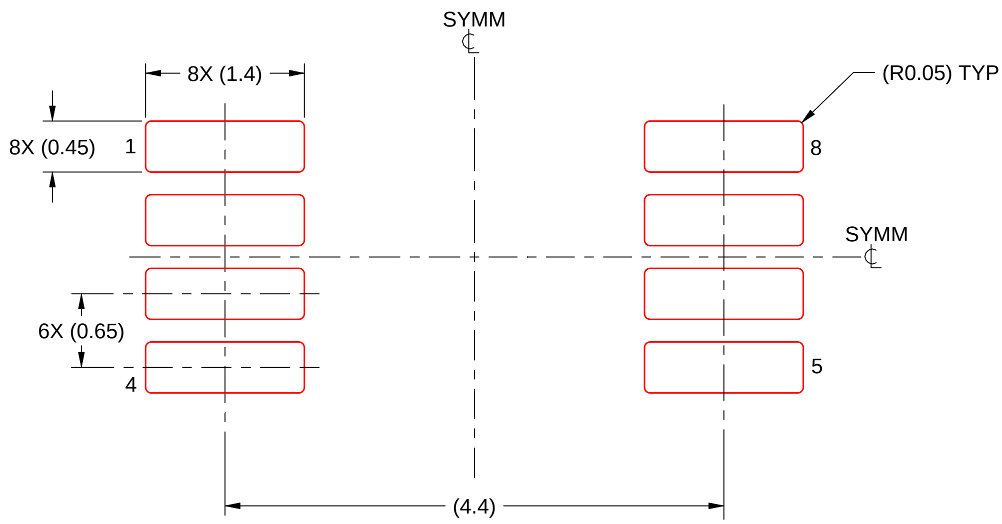


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265