OPA27, OPA37 Ultralow-Noise, Precision Operational Amplifiers

1 Features

- Low noise: 3nV/√Hz
- Wide bandwidth:
  - OPA27: 8MHz, 2.3V/µs
  - OPA37: 33MHz, 10V/µs
- High CMRR: 138dB
- High open-loop gain: 160dB
- Low offset voltage: 100µV maximum
- Single, dual, and quad versions

2 Applications

- Precision instrumentation
- Data acquisition
- Test equipment
- Professional audio equipment
- Transducer amplifiers
- Radiation hard equipment

3 Description

The OPA27 and OPA37 series operational amplifiers combine low noise and wide bandwidth with high precision to make them an excellent choice for applications requiring both ac and precision dc performance.

The OPA27 are unity-gain stable and features high slew rate (3.4V/µs) and wide bandwidth (8MHz). The OPA37 are optimized for closed-loop gains of 5 or greater, and offers higher speed with a slew rate of 11V/µs and a bandwidth of 33MHz.

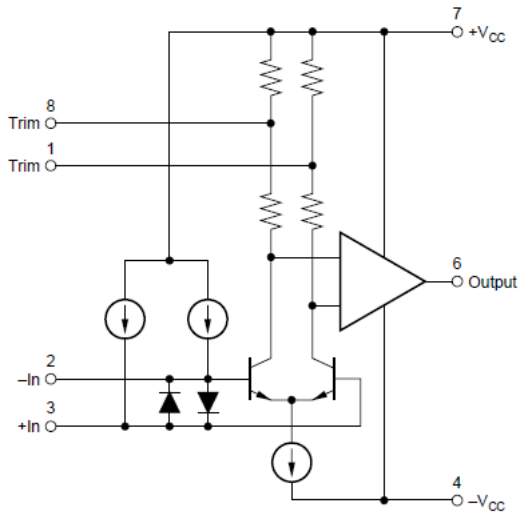
The OPA27 and OPA37 series operational amplifiers are an excellent choice for professional audio equipment. In addition, low quiescent current and low cost make these op amps an excellent choice for portable applications requiring high precision.

The OPA27 and OPA37 are available in DIP-8 and SO-8 packages.

Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA27, OPA37	Single	P (PDIP, 8)
		D (SOIC, 8)

(1) For all available packages, see *Section 9*.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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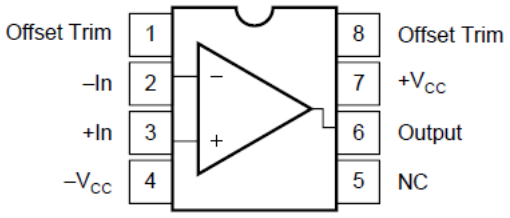
4 Pin Configuration and Functions



Note: NC = No connection.

Figure 4-1. D Package, 8-Pin DIP and P Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: OPA227 and OPA228

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	Offset Trim	Input	Input offset voltage trim (leave floating if not used)
2	-In	Input	Inverting input
3	+In	Input	Non inverting input
4	V-	—	Negative (lowest) power supply
5	NC	—	No internal connection (can be left floating)
6	Output	Output	Output
7	V+	—	Positive (highest) power supply
8	Offset Trim	—	Input offset voltage trim (leave floating if not used)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Single supply voltage, V_S = (V+) – (V–)		8	36	V
	Dual supply voltage, V_S = (V+) – (V–)		±4	±18	
	Signal input pins	Voltage	(V–) – 0.7	(V+) + 0.7	V
		Current		20	mA
I_{SC}	Output short circuit(2)		Continuous		
T_A	Operating temperature		–40	+85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	+150	°C

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5.2 Electrical Characteristics OPA27

at T_A = +25°C, V_S = ±5V to ±15V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±100	µV
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +85°C		±0.3	±2	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±4V to ±18V			±0.5	±2	µV/V
			T_A = –40°C to +85°C			±2	
	Long-term drift				0.2		µV/mo
	Channel separation (dual, quad)	DC			0.2		µV/V
		f = 1kHz, R_L = 5kΩ			110		dB
INPUT BIAS CURRENT							
I_B	Input bias current				±2.5	±10	nA
I_{OS}	Input offset current				±2.5	±10	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			90		nV_{PP}
					15		nV_{RMS}
e_n	Input voltage noise density	f = 10Hz			3.5		$nV/\sqrt{Hz}$
		f = 100Hz			3		
		f = 1kHz			3		
i_n	Input current noise density	f = 1kHz			0.4		$pA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2V < V_{CM} < (V+) – 2V		120	138		dB
INPUT IMPEDANCE							
	Differential				10 || 12		MΩ || pF
	Common-mode	V_{CM} = (V–) + 2V to (V+) – 2V			1 || 3		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 2V < V_O < (V+) – 2V		132	160		dB
		(V–) + 3.5V < V_O < (V+) – 3.5V, R_L = 600Ω		132	160		
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				8		MHz
SR	Slew rate				3.4		V/µs
	Settling time	G = 1, 10V step, C_L = 100pF	To 0.1%		5		µs
			To 0.01%		5.6		
	Overload recovery time	V_{IN} × G = V_S			1.3		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1kHz, V_O = 3.5V_{RMS}			0.00005		%
OUTPUT							
	Voltage output	T_A = –40°C to +85°C		(V–) + 2		(V+) + 2	V
			R_L = 600Ω	(V–) + 3.5		(V+) + 3.5	V
I_{SC}	Short-circuit current				±45		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics			
Z_O	Open-loop output impedance	f = 1MHz			27		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0A			±3.7	±3.8	mA

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5.3 Electrical Characteristics: OPA37

at T_A = +25°C, V_S = ±5V to ±15V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±100	µV
dV_{OS}/dT	Input offset voltage drift				±0.3	±2	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±4V to ±18V			±0.5	±2	µV/V
			T_A = –40°C to +85°C			±2	
	Long-term drift				0.2		µV/mo
	Channel separation (dual, quad)	DC			0.2		µV/V
		f = 1kHz, R_L = 5kΩ			110		dB
INPUT BIAS CURRENT							
I_B	Input bias current				±2.5	±10	nA
I_{OS}	Input offset current				±2.5	±10	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			90		nV_{PP}
					15		nV_{RMS}
e_n	Input voltage noise density	f = 10Hz			3.5		$nV/\sqrt{Hz}$
		f = 100Hz			3		
		f = 1kHz			3		
i_n	Input current noise density	f = 1kHz			0.4		$pA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2V < V_{CM} < (V+) – 2V		120	138		dB
INPUT IMPEDANCE							
	Differential				10 || 12		MΩ || pF
	Common-mode	V_{CM} = (V–) + 2V to (V+) – 2V			1 || 3		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 2V < V_O < (V+) – 2V		132	160		dB
		(V–) + 3.5V < V_O < (V+) – 3.5V, R_L = 600Ω		132	160		
FREQUENCY RESPONSE							
	Minimum closed-loop gain				5		V/V
GBW	Unity gain bandwidth				33		MHz
SR	Slew rate				11		V/µs
	Settling time	G = 1, 10V step, C_L = 100pF	To 0.1%		1.5		µs
			To 0.01%		2		
	Overload recovery time	V_{IN} × G = V_S			0.6		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1kHz, V_O = 3.5V_{RMS}			0.00005		%
OUTPUT							
	Voltage output	T_A = –40°C to +85°C		(V–) + 2		(V+) + 2	V
			R_L = 600Ω	(V–) + 3.5		(V+) + 3.5	
I_{SC}	Short-circuit current				±45		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1MHz			27		Ω
POWER SUPPLY							

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5.3 Electrical Characteristics: OPA37 (continued)

at T_A = +25°C, V_S = ±5V to ±15V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current per amplifier	I_O = 0A			±3.7	±3.8	mA

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5.4 Typical Characteristics

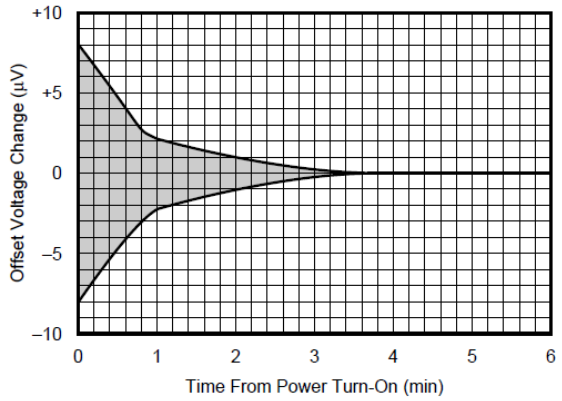

Figure 5-1. Input Offset Voltage Warm-Up Drift (Legacy Die)

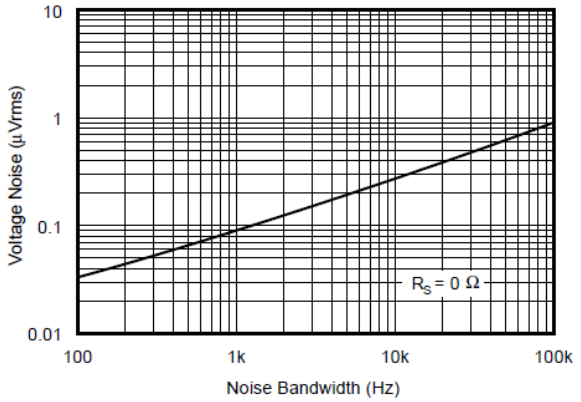

Figure 5-2. Input Voltage Noise vs Noise Bandwidth (0.1Hz to Indicated Frequency) (Legacy Die)

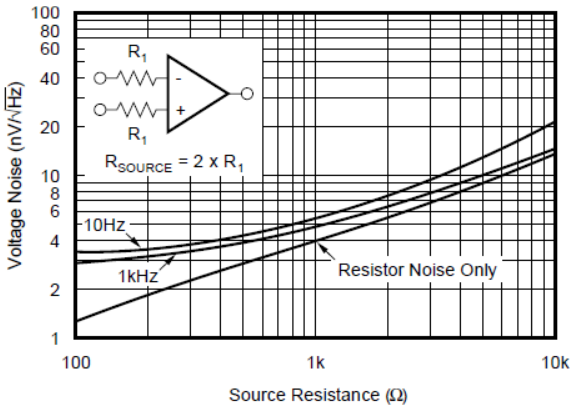

Figure 5-3. Total Input Voltage Noise Spectral Density vs Source Resistance (Legacy Die)

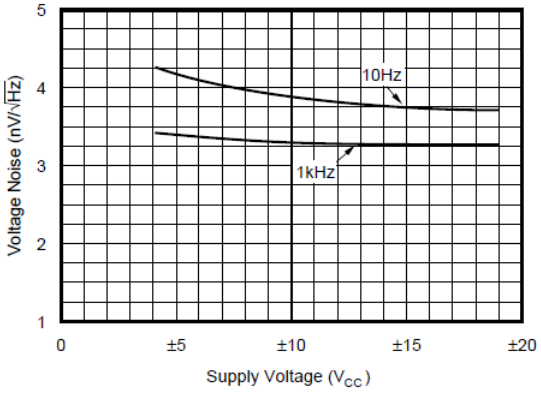

Figure 5-4. Voltage Noise Spectral Density vs Supply Voltage (Legacy Die)

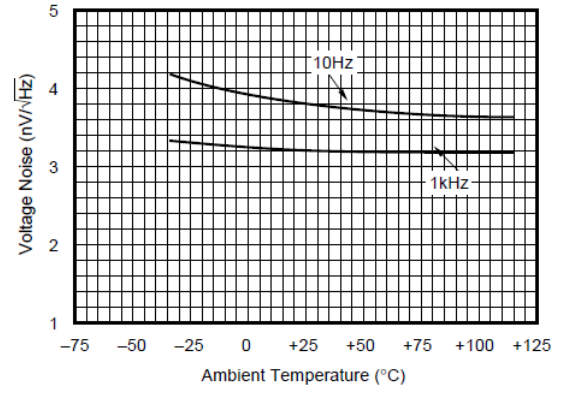

Figure 5-5. Voltage Noise Spectral Density vs Temperature (Legacy Die)

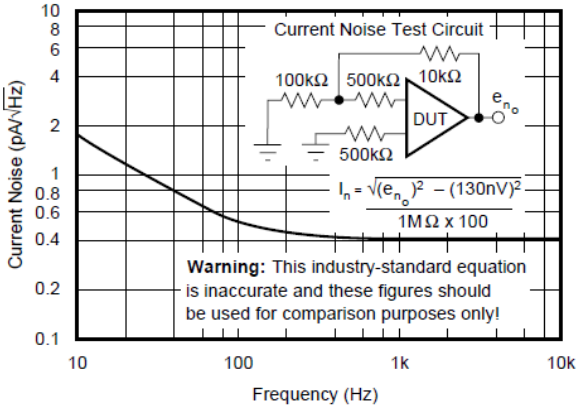

Figure 5-6. Input Current Noise Spectral Density (Legacy Die)

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5.4 Typical Characteristics (continued)

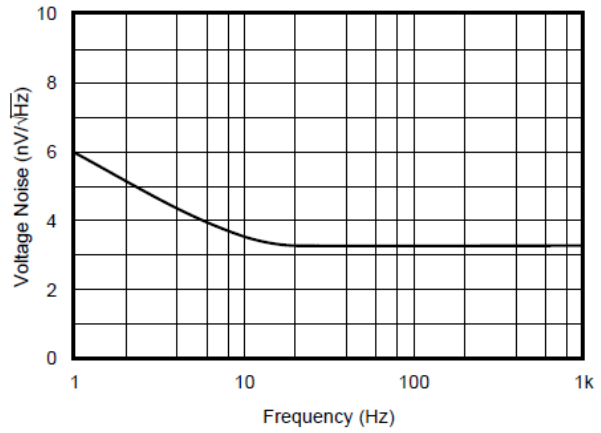

Figure 5-7. Input Voltage Noise Spectral Density (Legacy Die)

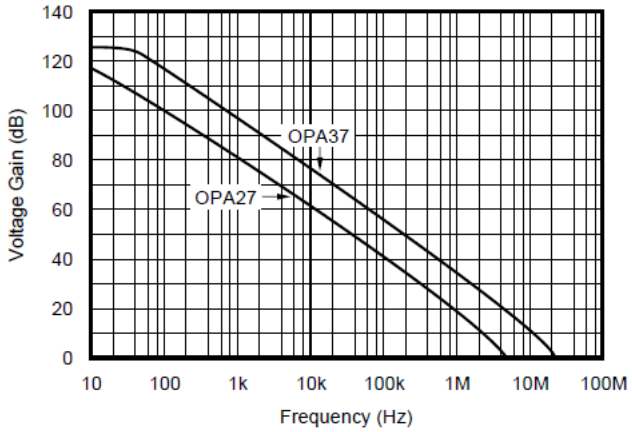

Figure 5-8. Open-Loop Frequency Response (Legacy Die)

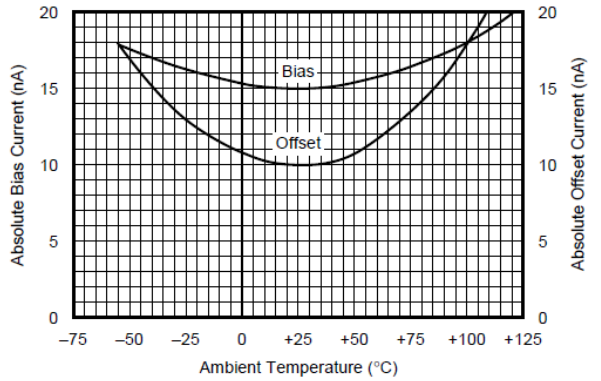

Figure 5-9. Bias and Offset Current vs Temperature (Legacy Die)

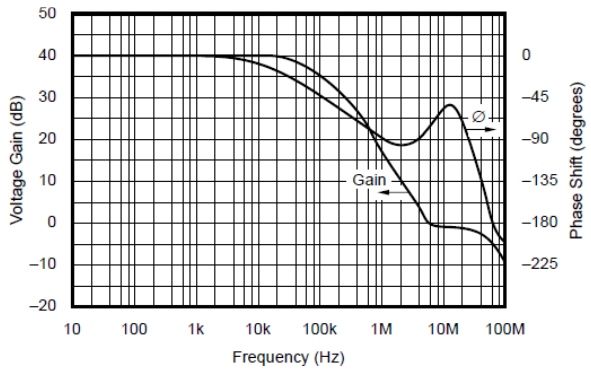

Figure 5-10. OPA27 Closed-Loop Voltage Gain and Phase Shift vs Frequency (G = 100) (Legacy Die)

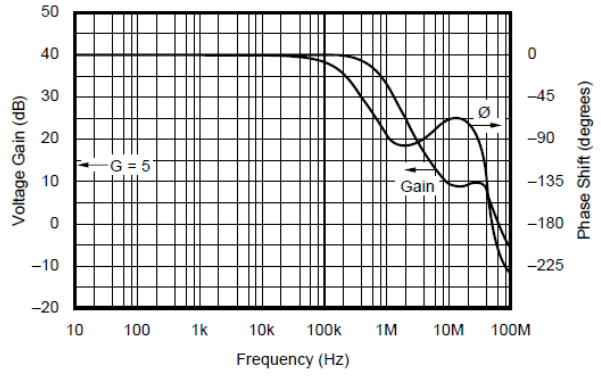

Figure 5-11. OPA37 Closed-Loop Voltage Gain and Phase Shift vs Frequency (G = 100) (Legacy Die)

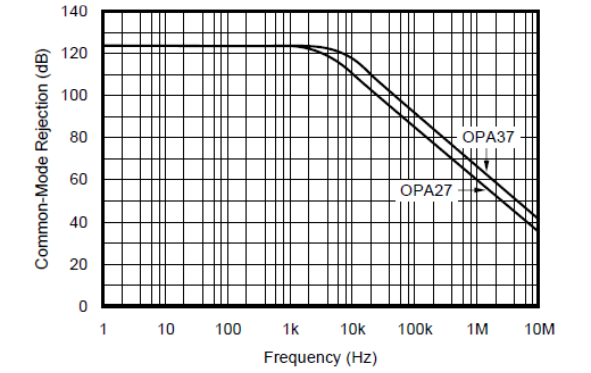

Figure 5-12. Common-Mode Rejection vs Frequency (Legacy Die)

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5.4 Typical Characteristics (continued)

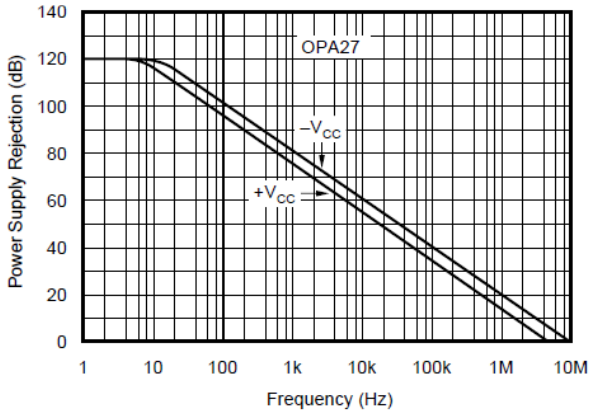

Figure 5-13. Power Supply Rejection vs Frequency (Legacy Die)

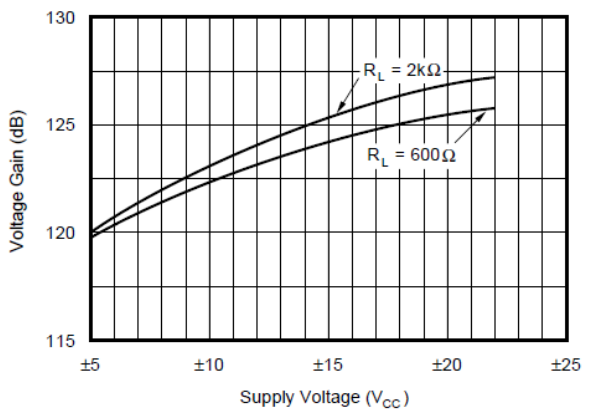

Figure 5-14. Open-Loop Voltage Gain vs Supply Voltage (Legacy Die)

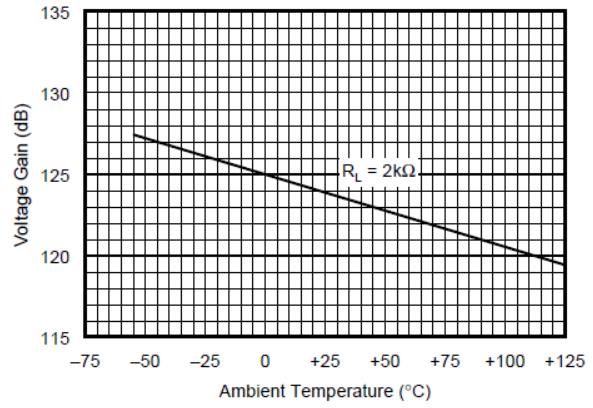

Figure 5-15. Open-Loop Voltage Gain vs Temperature (Legacy Die)

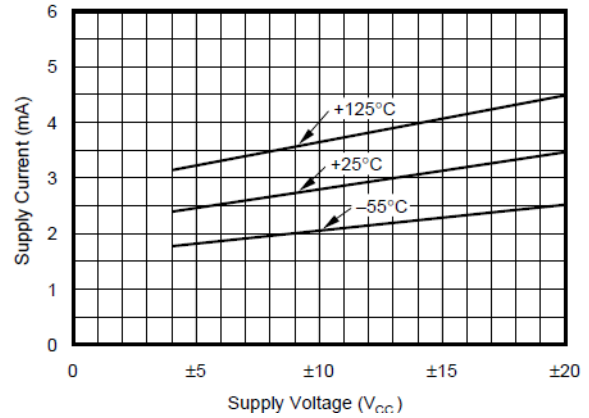

Figure 5-16. Supply Current vs Supply Voltage (Legacy Die)

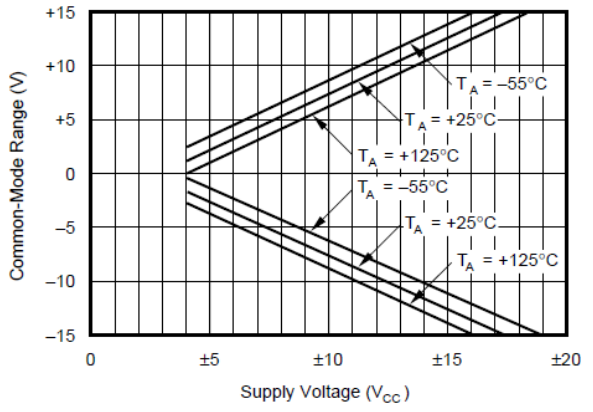

Figure 5-17. Common-Mode Input Voltage Range vs Supply Voltage (Legacy Die)

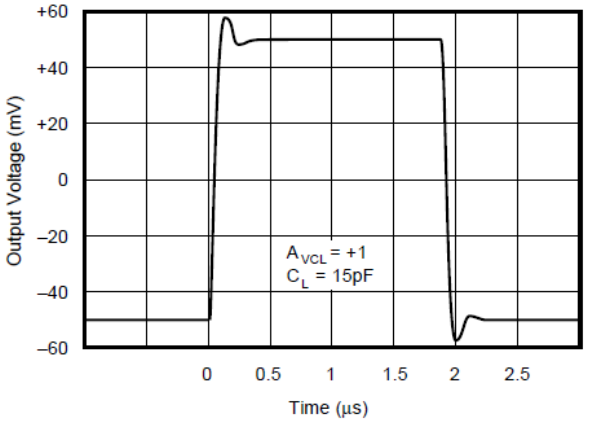

Figure 5-18. OPA27 Small Signal Transient Response (Legacy Die)

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5.4 Typical Characteristics (continued)

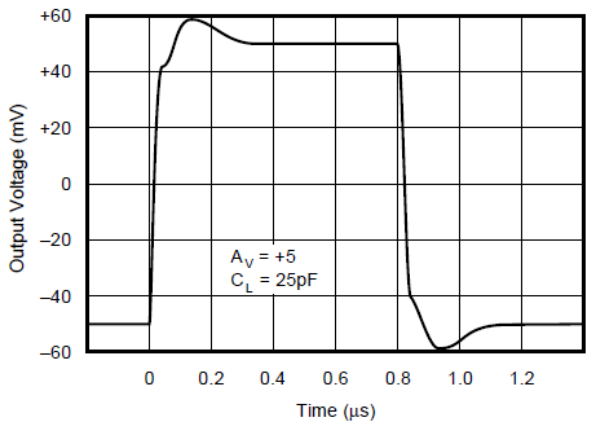

Figure 5-19. OPA37 Small Signal Transient Response (Legacy Die)

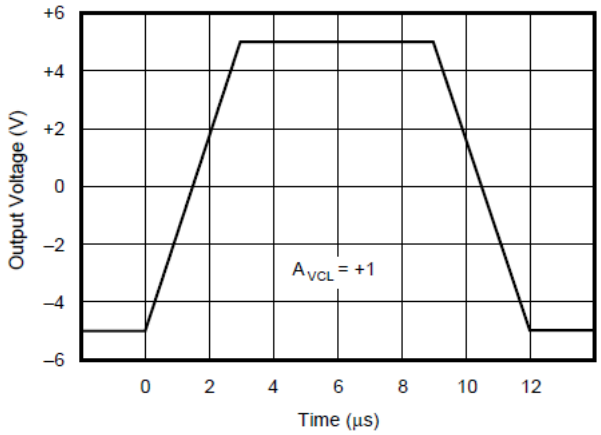

Figure 5-20. OPA27 Large Signal Transient Response (Legacy Die)

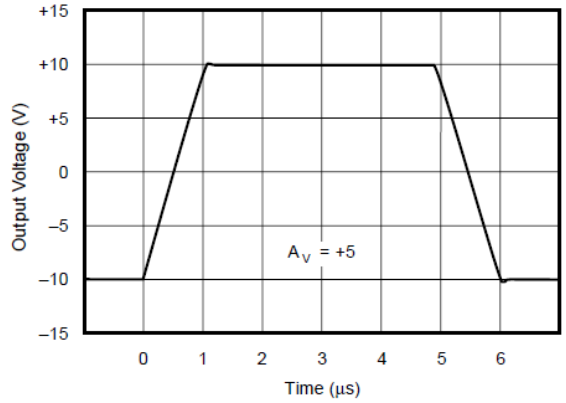

Figure 5-21. OPA37 Large Signal Transient Response (Legacy Die)

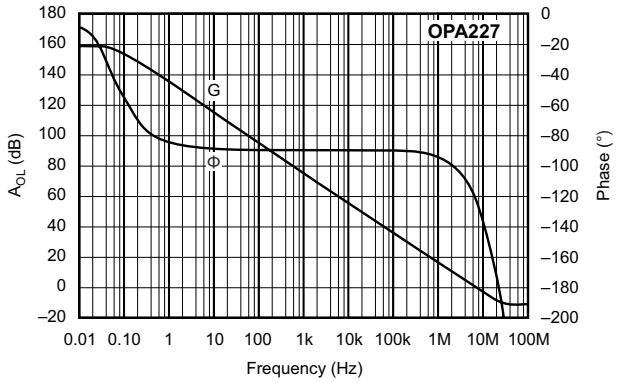

Figure 5-22. Open-Loop Gain and Phase vs Frequency (New Die)

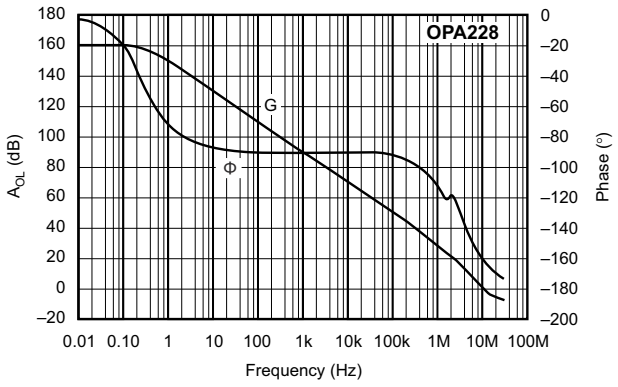

Figure 5-23. Open-Loop Gain and Phase vs Frequency (New Die)

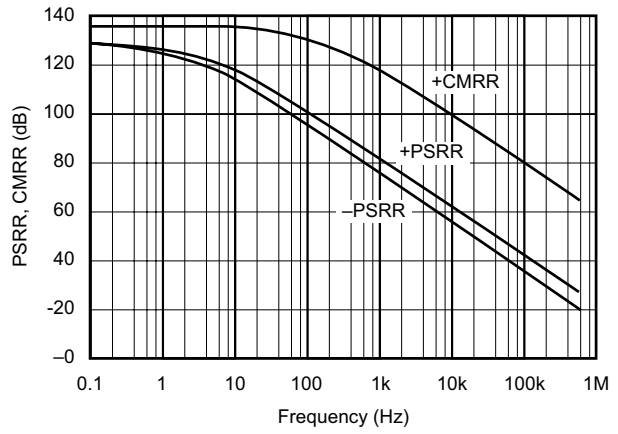

Figure 5-24. Power Supply and Common-Mode Rejection Ratio vs Frequency (New Die)

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5.4 Typical Characteristics (continued)

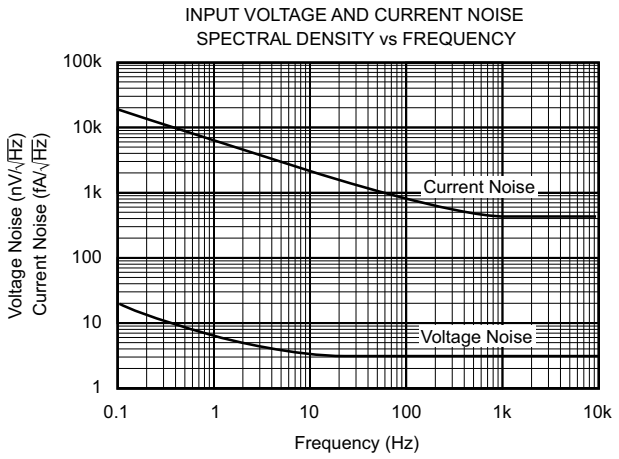

Figure 5-25. Input Voltage and Current Noise Spectral Density vs Frequency (New Die)

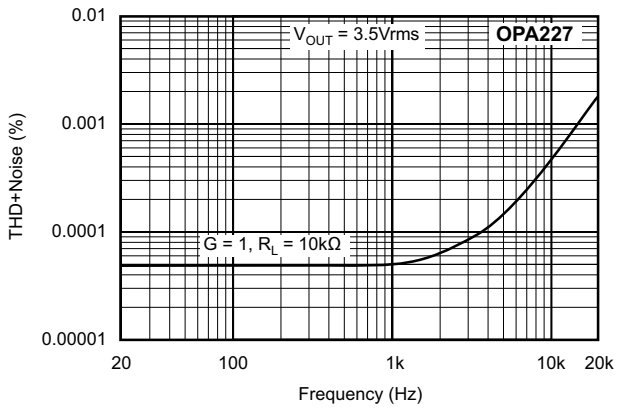

Figure 5-26. Total Harmonic Distortion + Noise vs Frequency (New Die)

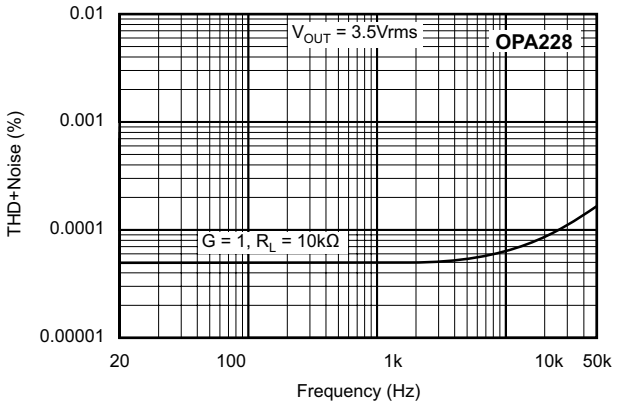

Figure 5-27. Total Harmonic Distortion + Noise vs Frequency (New Die)

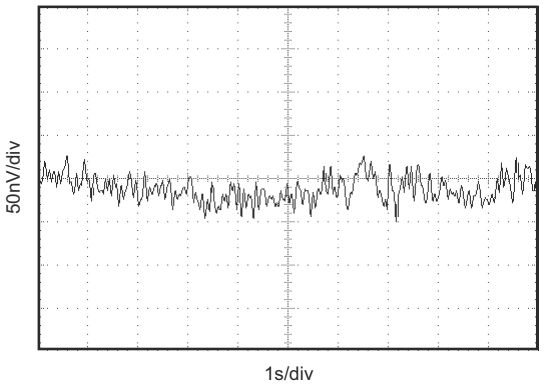

Figure 5-28. Input Noise Voltage vs Time (New Die)

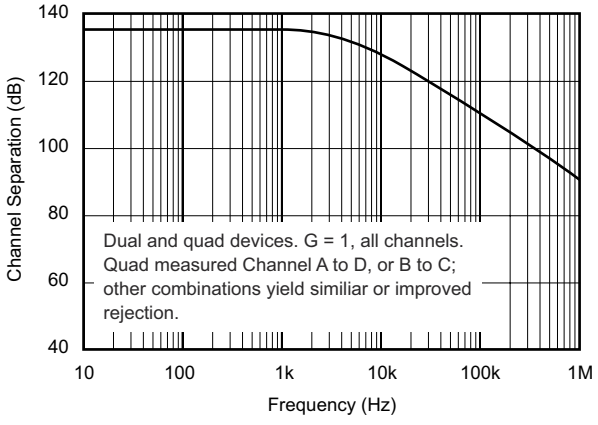

Figure 5-29. Channel Separation vs Frequency (New Die)

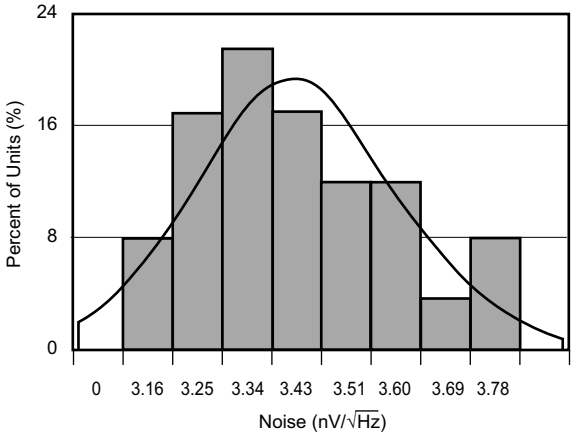

Figure 5-30. Voltage Noise Distribution (10Hz) (New Die)

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5.4 Typical Characteristics (continued)

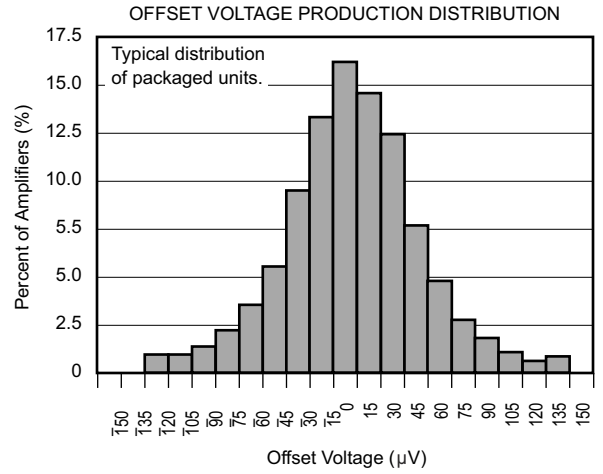

Figure 5-31. Offset Voltage Production Distribution (New Die)

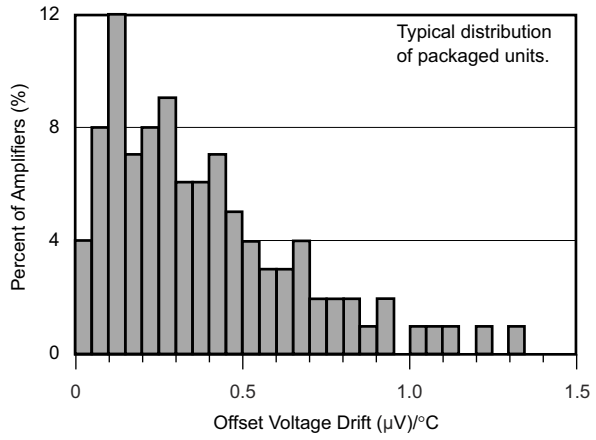

Figure 5-32. Offset Voltage Drift Production Distribution (New Die)

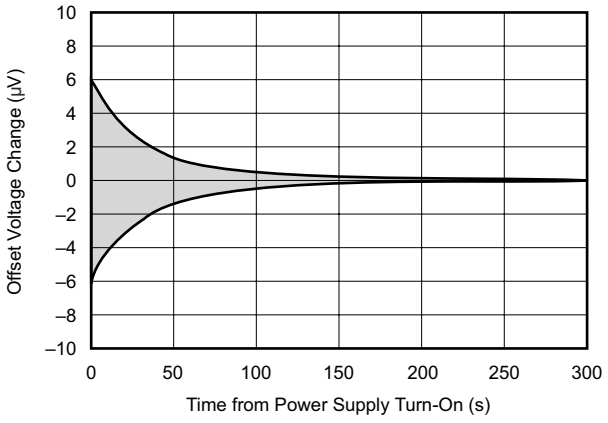

Figure 5-33. Warm-Up Offset Voltage Drift (New Die)

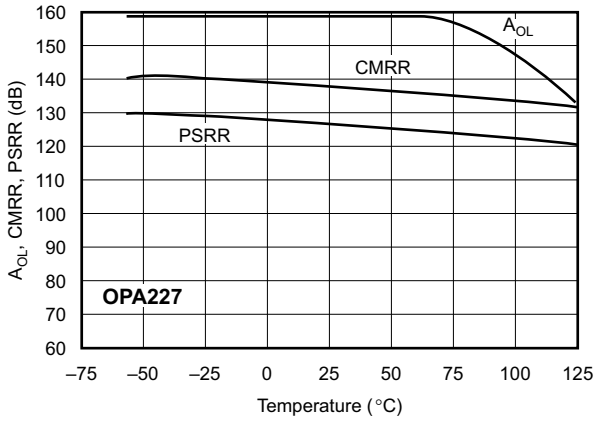

Figure 5-34. A_{OL}, CMRR, PSRR vs Temperature (New Die)

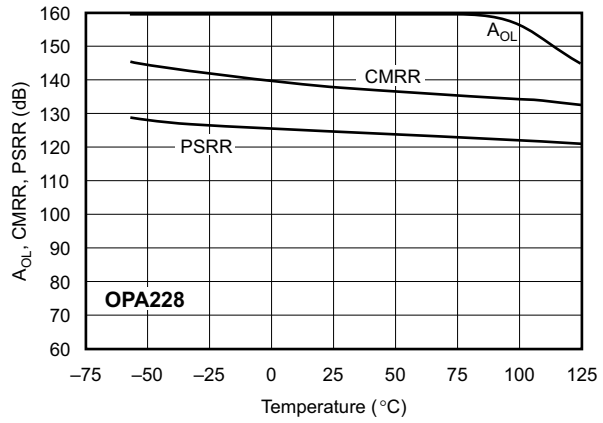

Figure 5-35. A_{OL}, CMRR, PSRR vs Temperature (New Die)

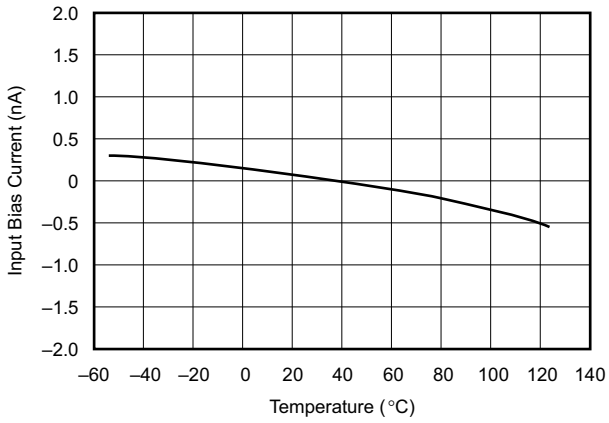

Figure 5-36. Input Bias Current vs Temperature (New Die)

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5.4 Typical Characteristics (continued)

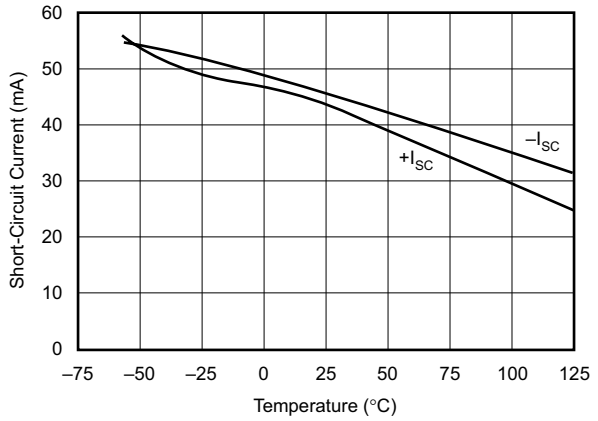

Figure 5-37. Short-Circuit Current vs Temperature (New Die)

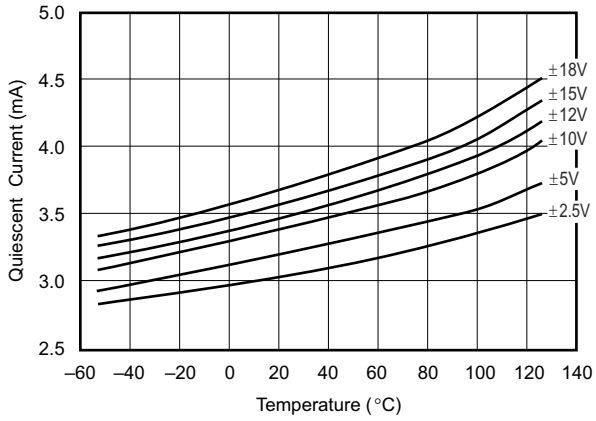

Figure 5-38. Quiescent Current vs Temperature (New Die)

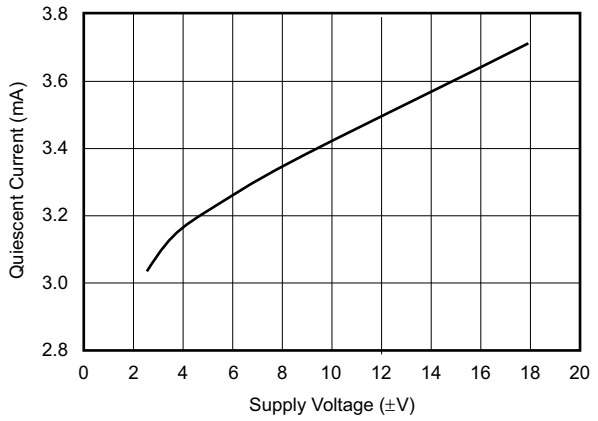

Figure 5-39. Quiescent Current vs Supply Voltage (New Die)

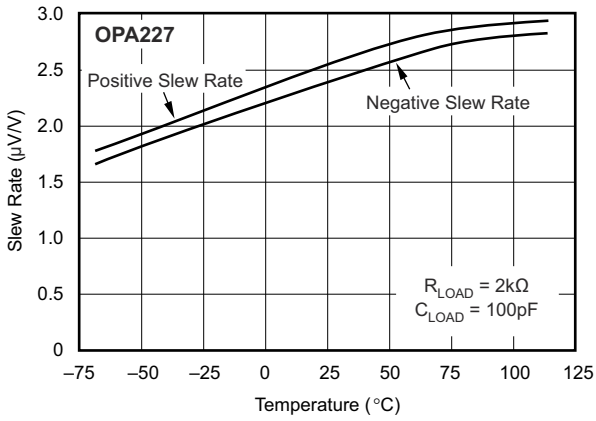

Figure 5-40. Slew Rate vs Temperature (New Die)

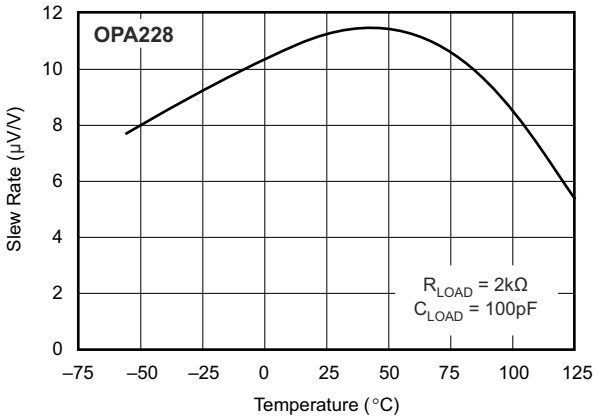

Figure 5-41. Slew Rate vs Temperature (New Die)

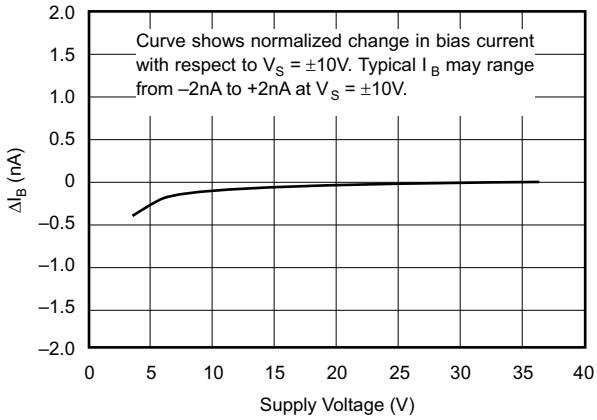

Figure 5-42. Change in Input Bias Current vs Power Supply Voltage (New Die)

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5.4 Typical Characteristics (continued)

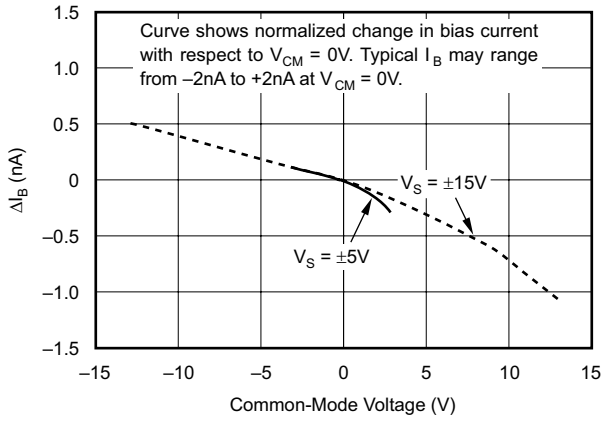

Figure 5-43. Change in Input Bias Current vs Common-Mode Voltage (New Die)

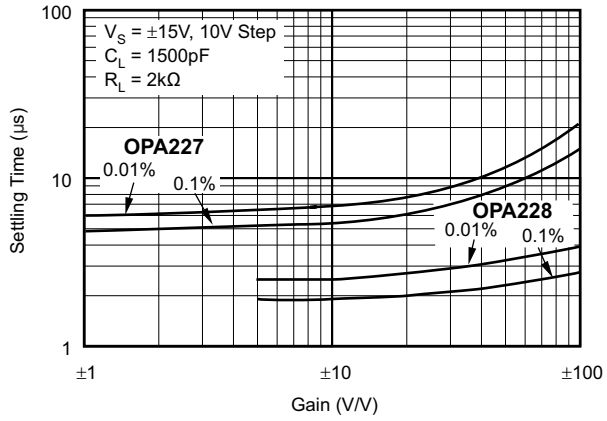

Figure 5-44. Settling Time vs Closed-Loop Gain (New Die)

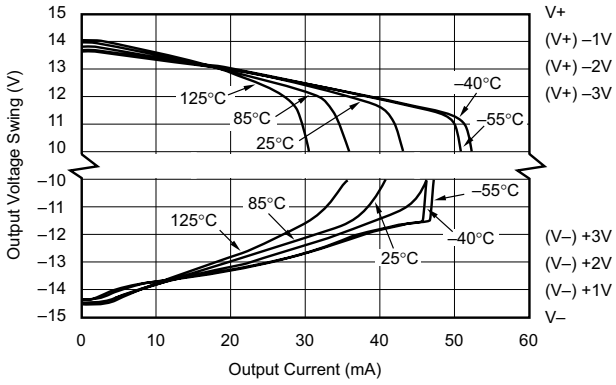

Figure 5-45. Output Voltage Swing vs Output Current (New Die)

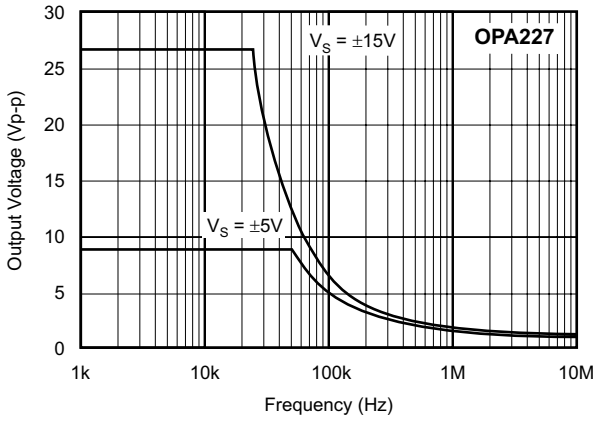

Figure 5-46. Maximum Output Voltage vs Frequency (New Die)

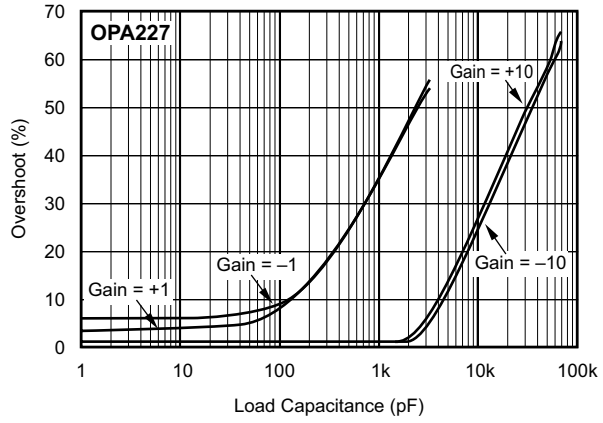

Figure 5-47. Small-Signal Overshoot vs Load Capacitance (New Die)

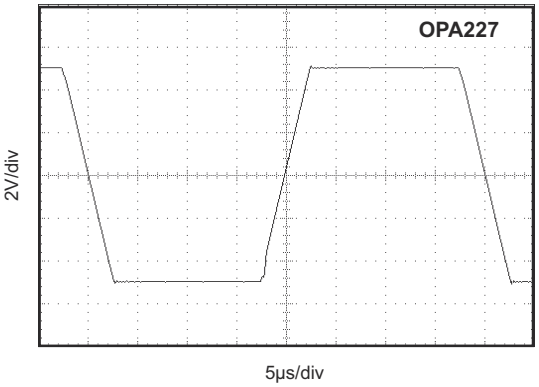

Figure 5-48. Large-Signal Step Response (New Die)

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5.4 Typical Characteristics (continued)

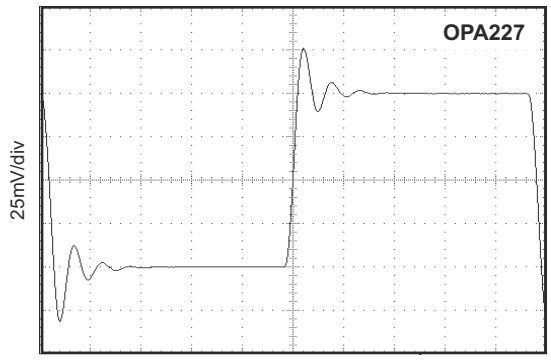

Figure 5-49. Small-Signal Step Response (New Die)

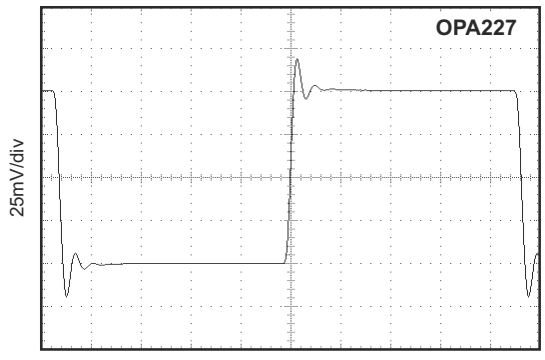

Figure 5-50. Small-Signal Step Response (New Die)

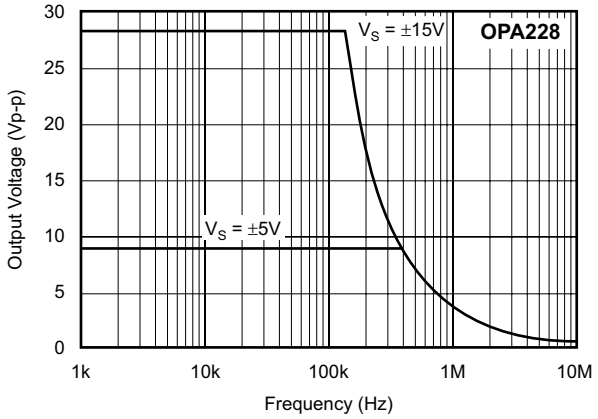

Figure 5-51. Maximum Output Voltage vs Frequency (New Die)

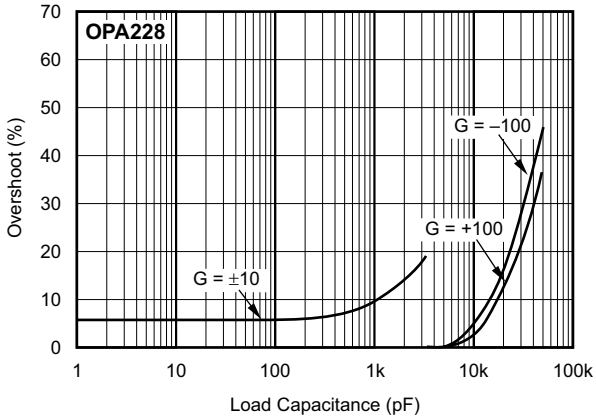

Figure 5-52. Small-Signal Overshoot vs Load Capacitance (New Die)

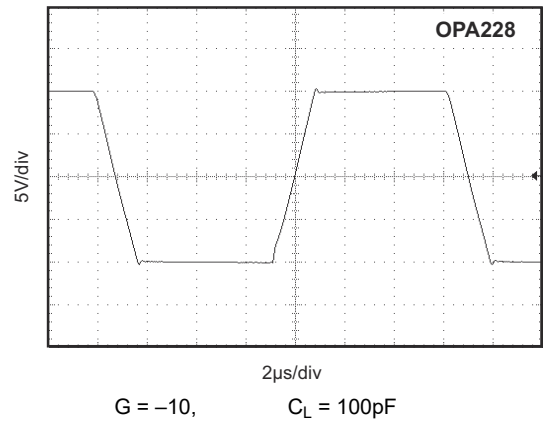

Figure 5-53. Large-Signal Step Response (New Die)

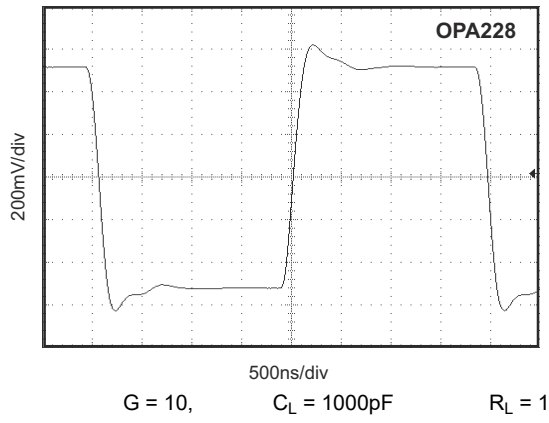

Figure 5-54. Small-Signal Step Response (New Die)

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5.4 Typical Characteristics (continued)

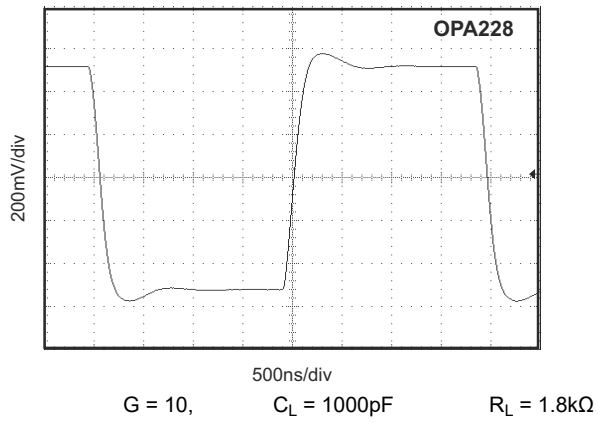

Figure 5-55. Small-Signal Step Response (New Die)

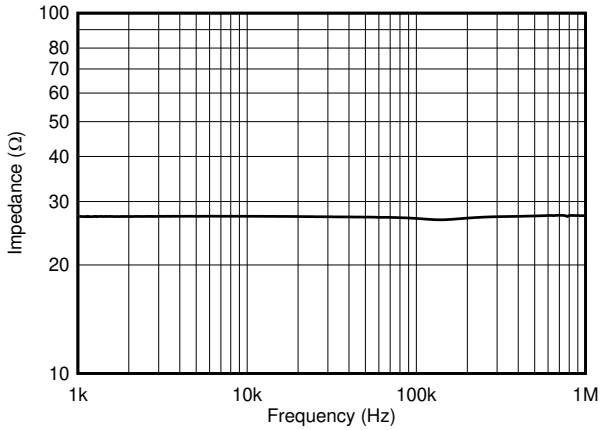

Figure 5-56. Open-loop Output Impedance (New Die)

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6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Offset Voltage Adjustment

The OPA27 and OPA37 offset voltages are laser-trimmed and require no further trim for most applications. Offset voltage drift does not degrade when the input offset is nulled with a 10-kΩ trim potentiometer. Other potentiometer values from 1 kΩ to 1 MΩ can be used, but V_{OS} drift is degraded by an additional 0.1 µV/°C to 0.2 µV/°C. Nulling large system offsets by use of the offset trim adjust degrades drift performance by approximately 3.3 µV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 6-1. For trimming very small offsets, the higher resolution circuit shown in Figure 6-2 is recommended.

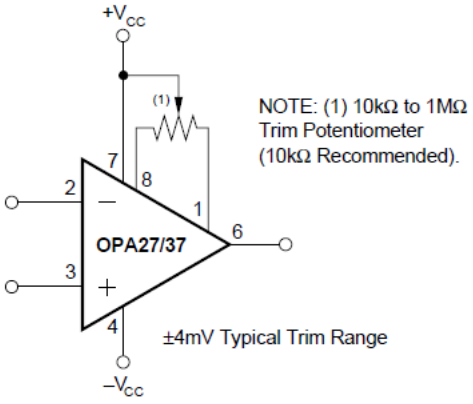

Figure 6-1. Offset Voltage Trim

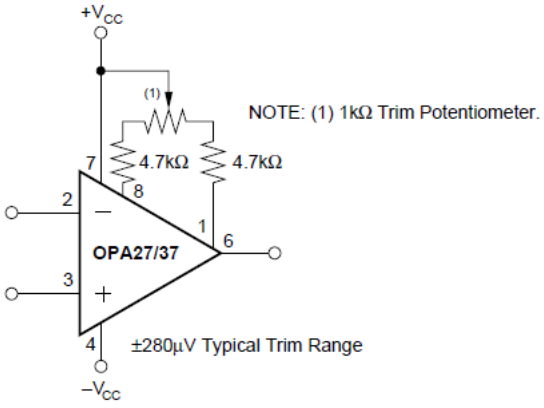

Figure 6-2. High Resolution Offset Voltage Trim

The OPA27 and OPA37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

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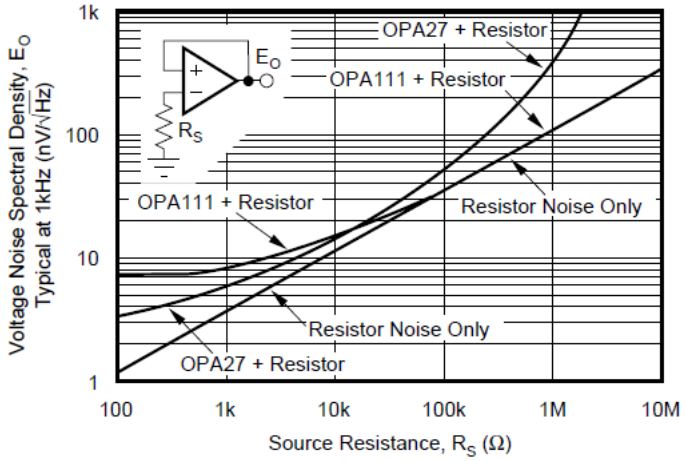
6.1.2 Noise: Bipolar Versus FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances, the high current noise of a bipolar amplifier becomes a serious liability. Above about 15 kΩ, the OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27, as shown in Figure 6-3.



A. $E_O = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S}$ F_O = 1kHz

Figure 6-3. Voltage Noise Spectral Density Versus Source Resistance

6.1.3 Compensation

Although internally compensated for unity-gain stability, the OPA27 can require a small capacitor in parallel with a feedback resistor (R_F) that is greater than 2kΩ. This capacitor compensates the pole generated by R_F and C_{IN} and eliminates peaking or oscillation.

6.1.4 Legacy vs. New Die

As of Rev. D of this data sheet, Texas Instruments has replaced the previous generation of this die with the newer generation. This device is also sold as OPA227 for the OPA27 replacement, and OPA228 for the OPA37 replacement. This data sheet contains information from both legacy die and the new die in the typical characteristics section. The legacy die is phased out and no longer available for purchase.

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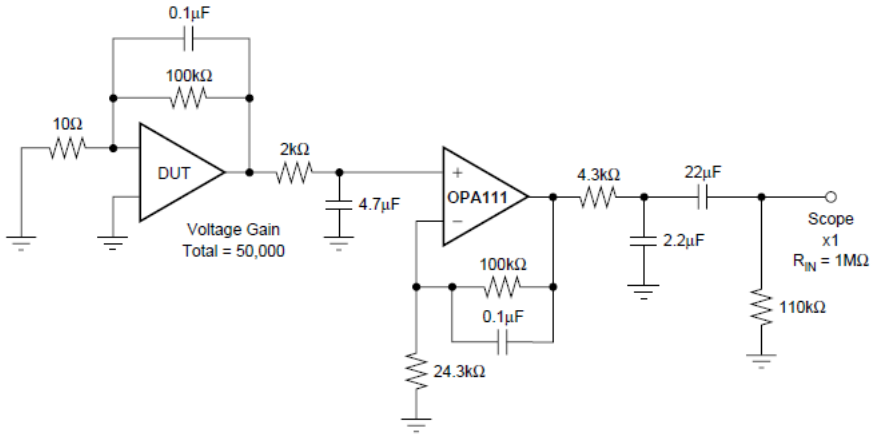
6.2 Typical Applications



Note: All capacitor values are for nonpolarized capacitors only.

Figure 6-4. 0.1Hz to 10Hz Noise Test Circuit

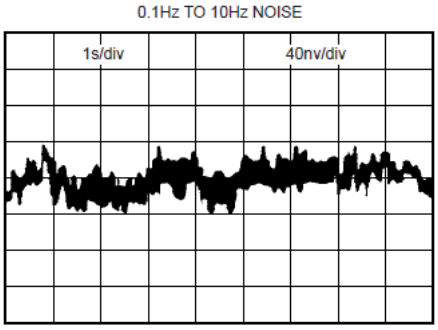


Figure 6-5. Low Frequency Noise

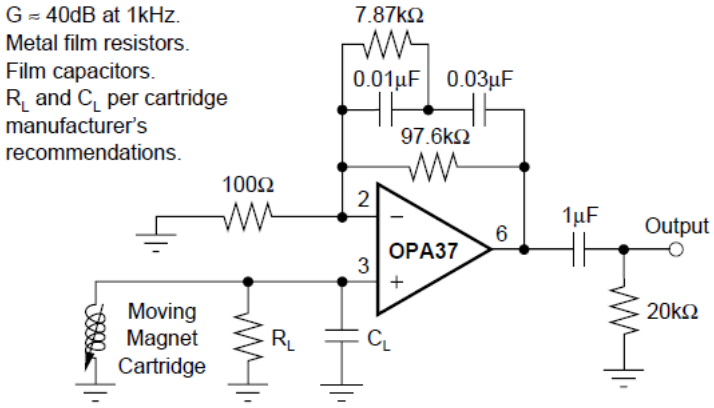


Figure 6-6. Low-Noise RIAA Preamplifier

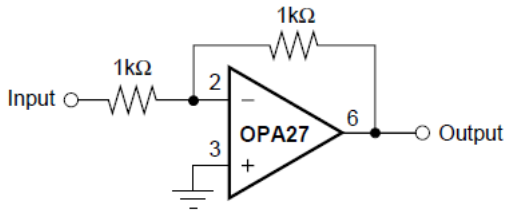


Figure 6-7. Unity-Gain Inverting Amplifier

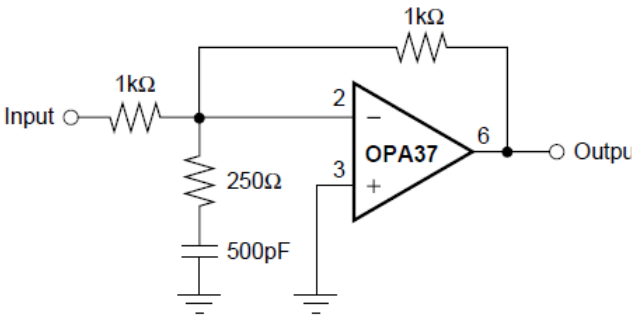


Figure 6-8. High Slew Rate Unity-Gain Inverting Amplifier

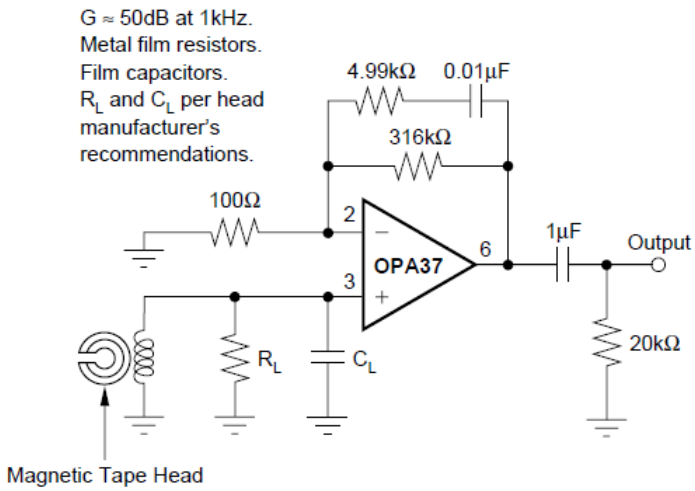


Figure 6-9. NAB Tape Head Preamplifier

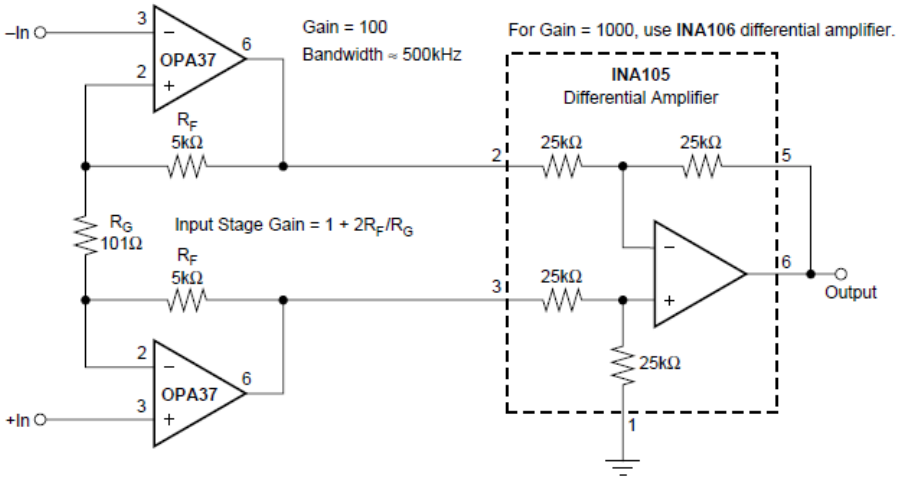


Figure 6-10. Low Noise Instrumentation Amplifier

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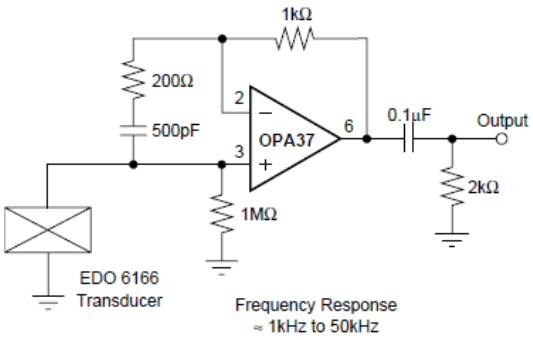

Figure 6-11. Hydrophone Preamplifier

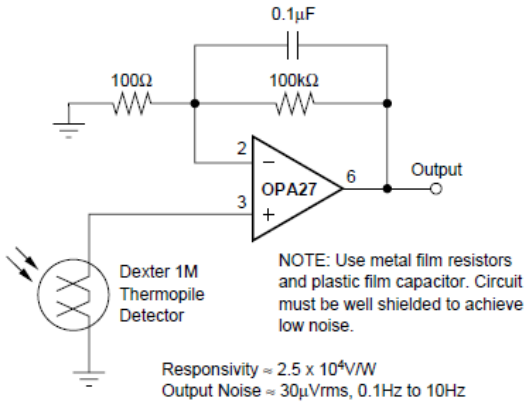

Figure 6-12. Long-Wavelength Infrared Detector Amplifier

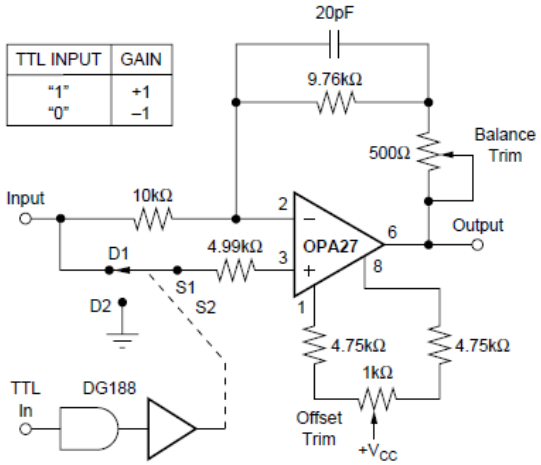

Figure 6-13. High Performance Synchronous Demodulator

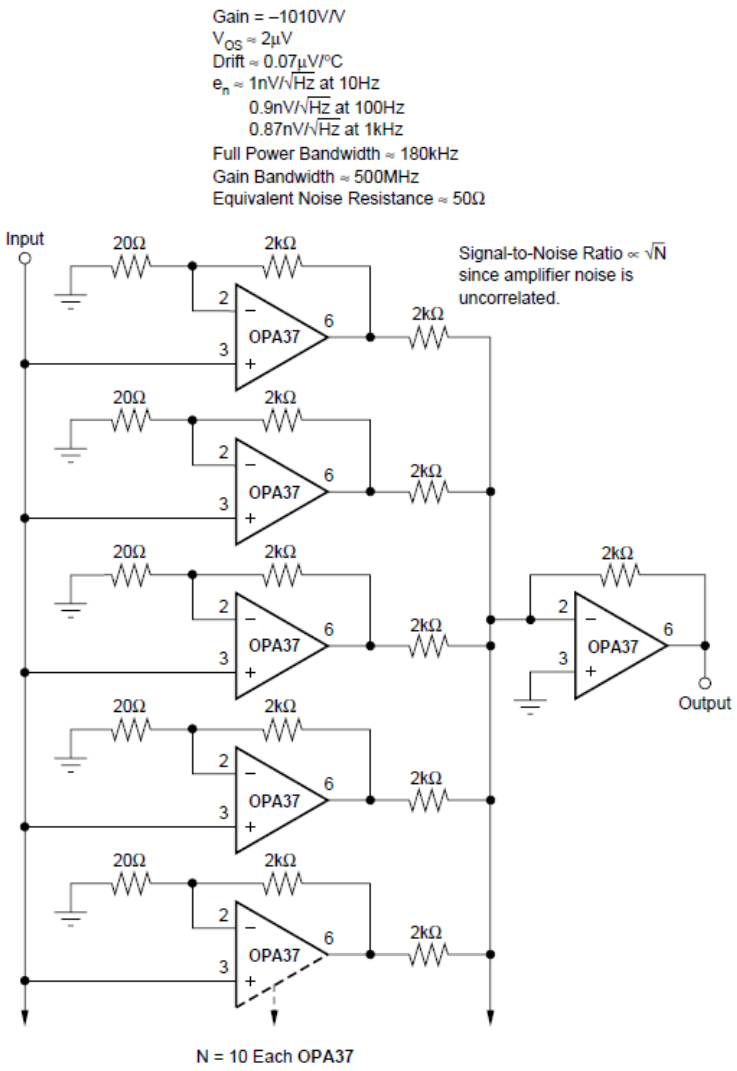

Figure 6-14. Ultra-Low Noise “N”-Stage Parallel Amplifier

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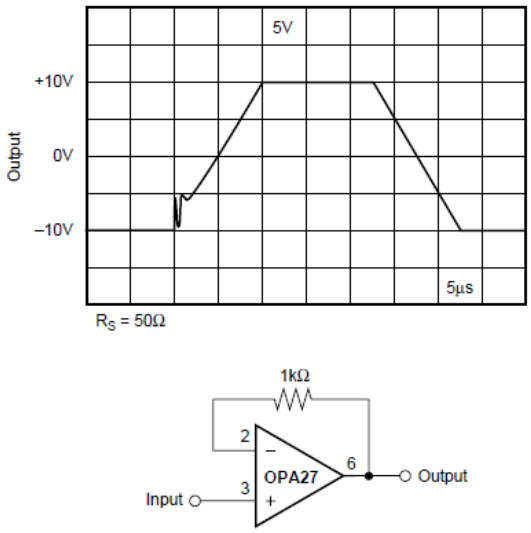

Figure 6-15. Unity-Gain Buffer

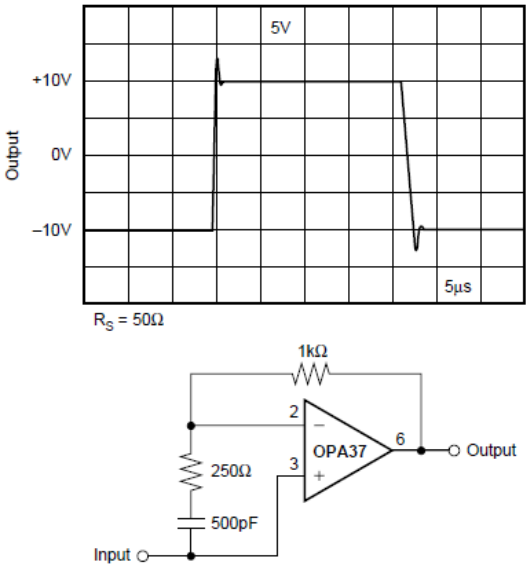

Figure 6-16. High Slew Rate Unity-Gain Buffer

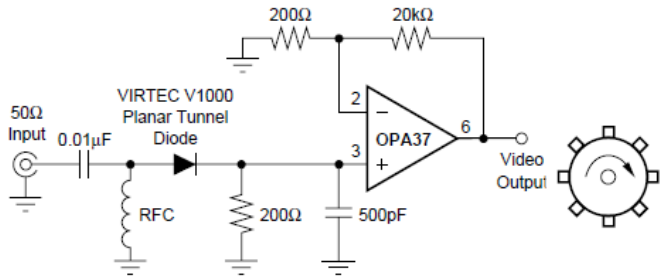

Figure 6-17. RF Detector and Video Amplifier

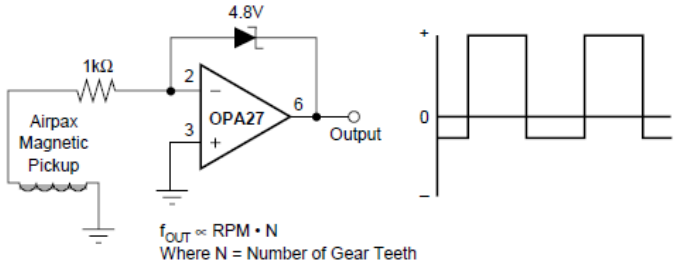

Figure 6-18. Magnetic Tachometer

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

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7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2005) to Revision D (October 2026)	Page
• Changed GBW from 45MHz to 33MHz for OPA37	1
• Changed Input bias current from 80nA max to 10nA max	1
• Changed Input Offset Current from 75nA to 10nA	1
• Changed Maximum Supply voltage from 44V (+/- 22V) to 36V (+/- 18V)	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed Offset Voltage Drift max. from	4
• Changed Voltage Output min/max from (V-)+3V/(V+)-3V to (V-)+2V/(V+)-2V	4
• Changed CMRR from 100dB min. to 120dB min	4
• Changed Input common-mode voltage range from (V-)+4V/(V+)-4V to (V-)+2V/(V+)-2V	4
• Changed Offset Voltage Drift max. from 1.8µV/°C to 2µV/°C	4
• Changed PSRR min. from 94dB to 114dB (2uV/V)	4
• Changed Slew rate for OPA27 from 1.9V/µs to 3.4V/µs	4
• Changed Slew rate for OPA37 from 11.9V/µs to 11V/µs	4
• Changed Output impedance from 70Ω to 27Ω	4
• Changed Short circuit current from 25mA to ±45mA	4
• Changed Quiescent current from "3.3mA (typ), 5.7mA (max)" to "±3.7mA (typ), ±3.8mA (max)"	4
• Added New die plot files	7

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA27GP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA27GP
OPA27GP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA27GP
OPA27GU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 27U
OPA27GU.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 27U
OPA27GU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 27U
OPA27GU/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 27U
OPA37GP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA37GP
OPA37GP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA37GP
OPA37GPG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA37GP
OPA37GU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 37U
OPA37GU.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 37U
OPA37GU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 37U
OPA37GU/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 37U

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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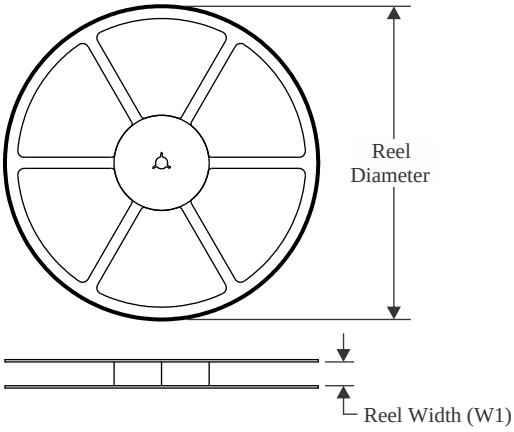
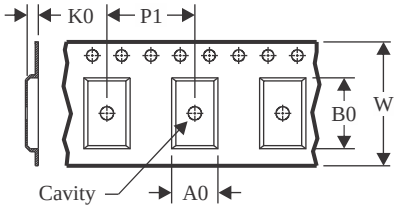
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

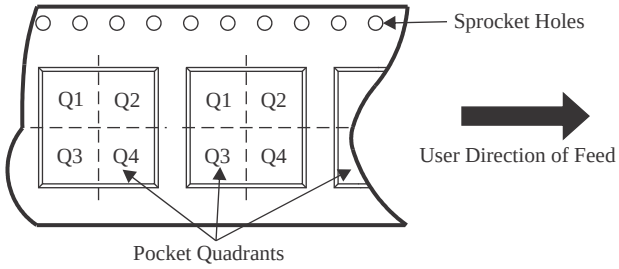


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

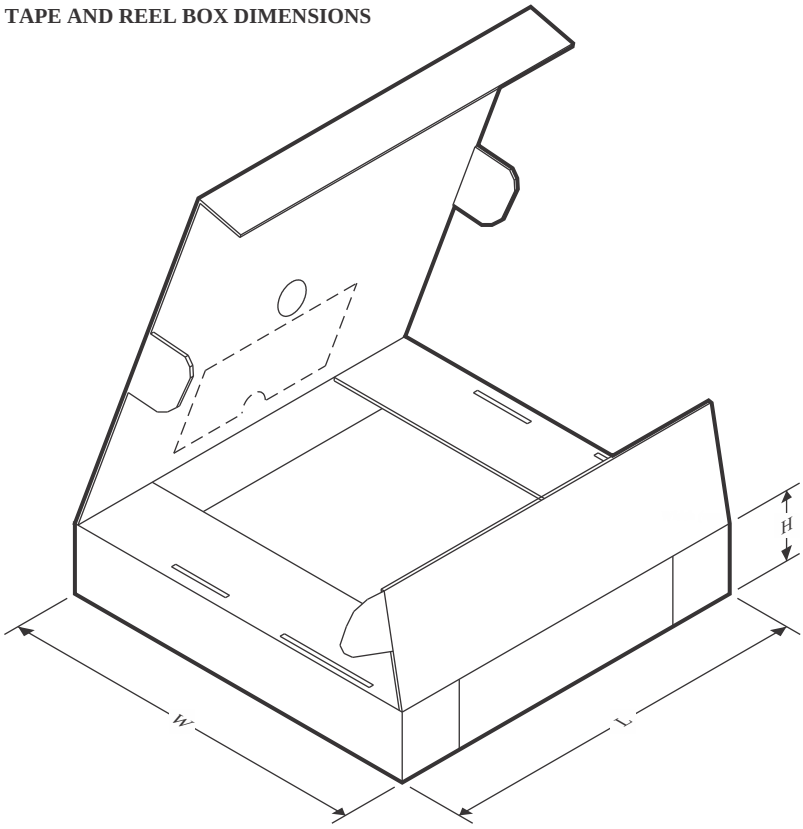
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA27GU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA27GU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA37GU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

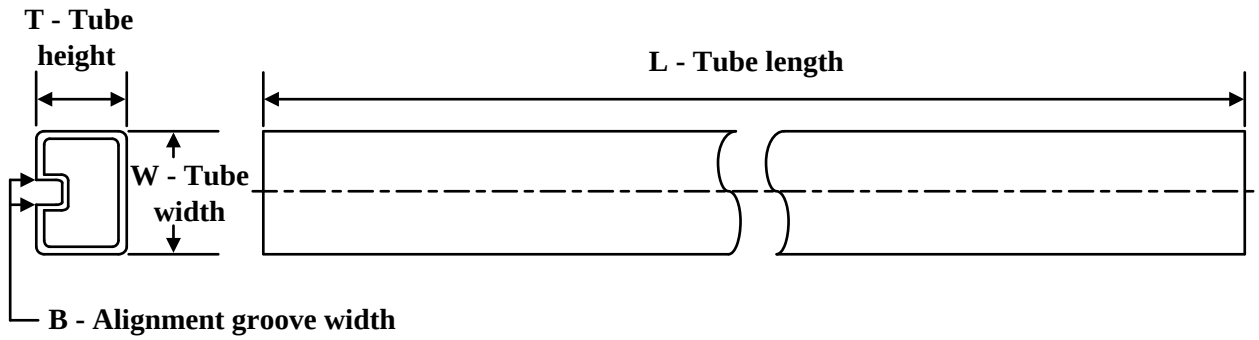
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

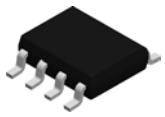
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA27GU/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA27GU/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA37GU/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA27GP	P	PDIP	8	50	506	13.97	11230	4.32
OPA27GP.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA27GU	D	SOIC	8	75	506.6	8	3940	4.32
OPA27GU.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA37GP	P	PDIP	8	50	506	13.97	11230	4.32
OPA37GP.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA37GPG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA37GU	D	SOIC	8	75	506.6	8	3940	4.32
OPA37GU.B	D	SOIC	8	75	506.6	8	3940	4.32

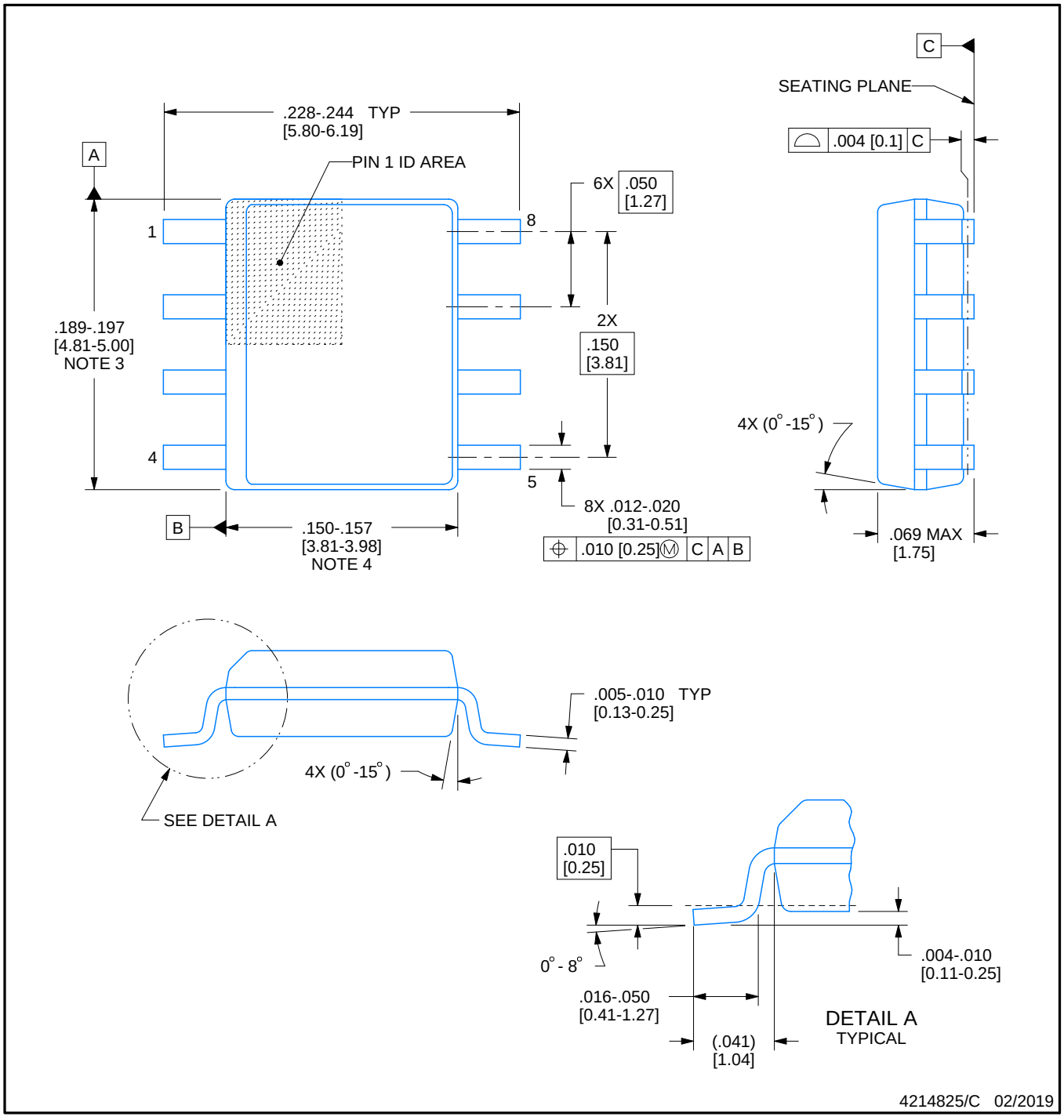


PACKAGE OUTLINE

D0008A

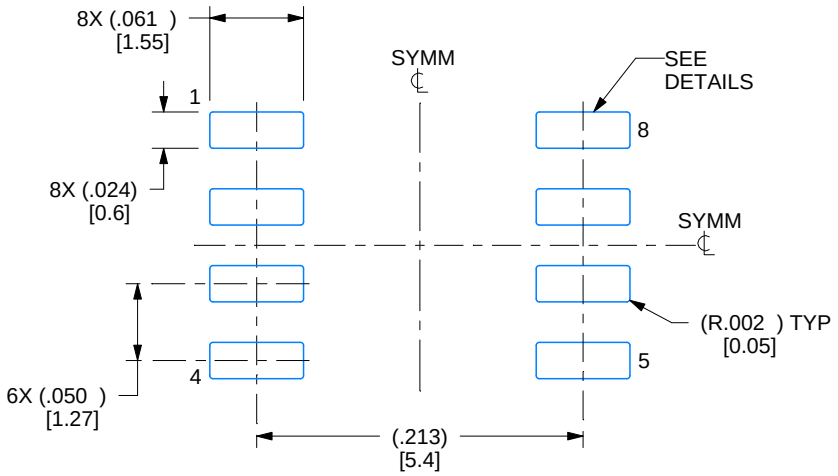
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

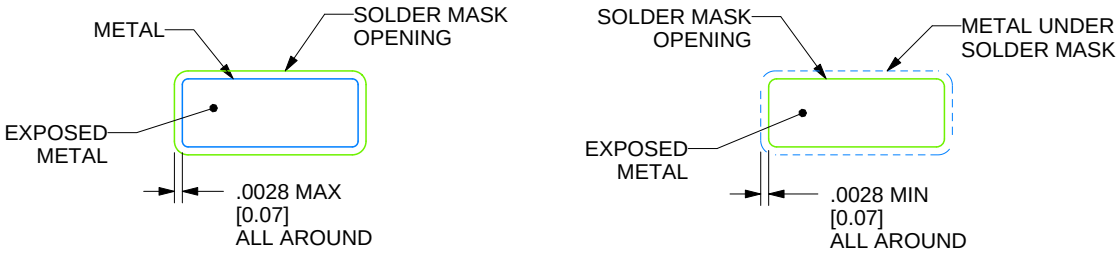


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

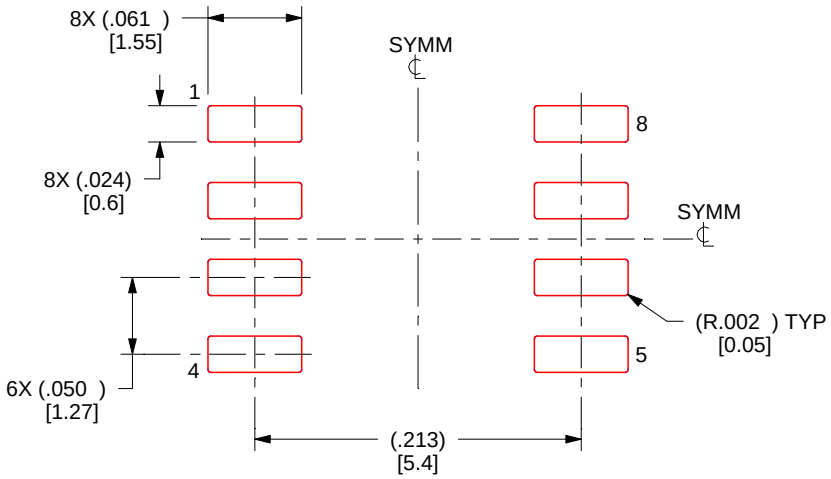
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



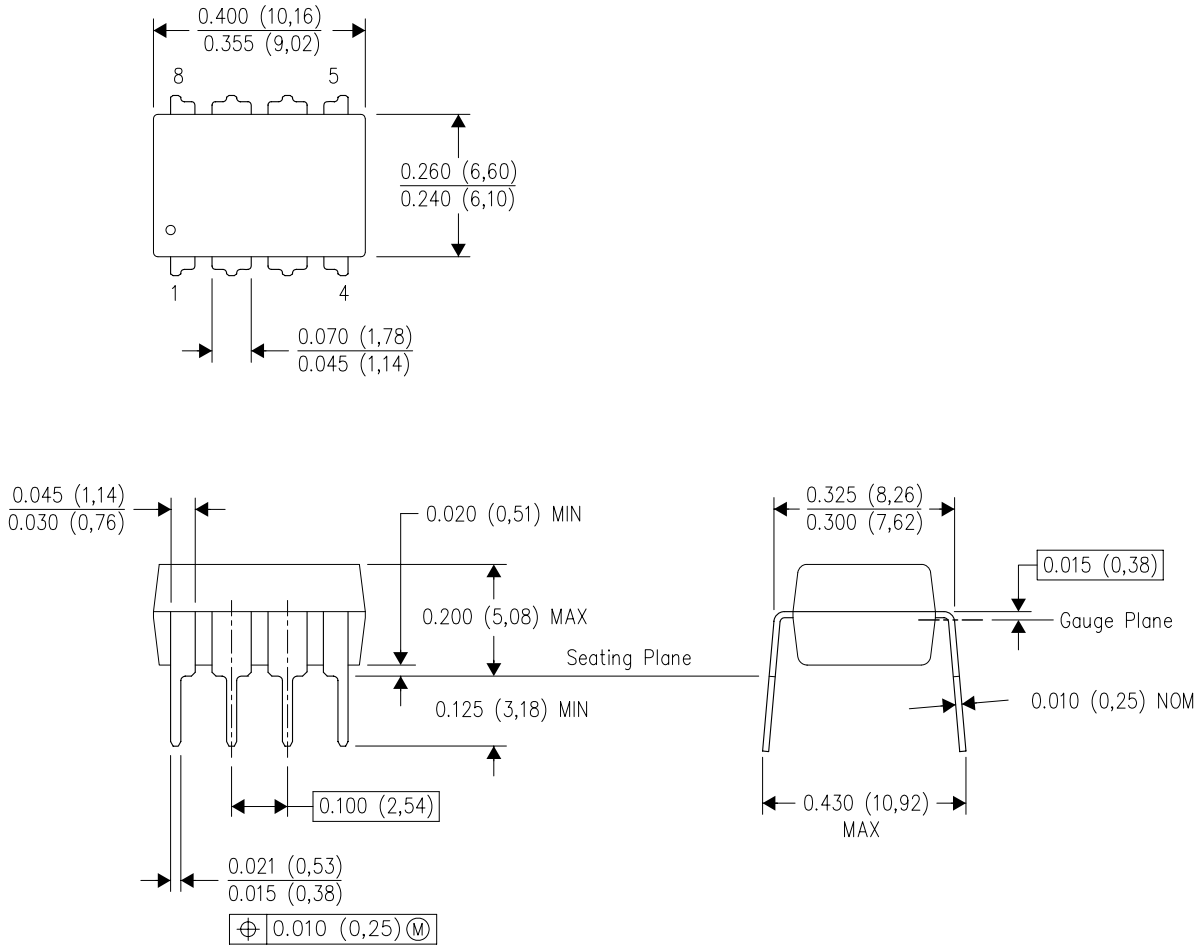
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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