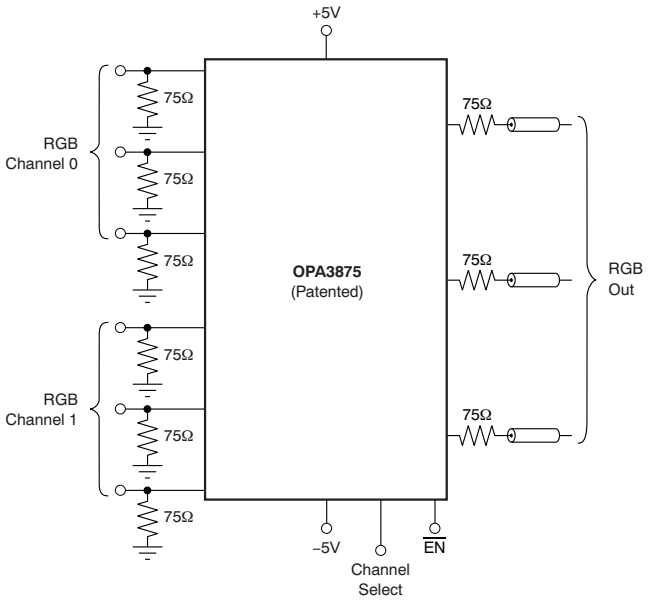
Triple 2:1 High-Speed Video Multiplexer

FEATURES

- 700MHz SMALL-SIGNAL BANDWIDTH (A_V = +2)
- 425MHz, 4V_{PP} BANDWIDTH
- 0.1dB GAIN FLATNESS to 150MHz
- 4ns CHANNEL SWITCHING TIME
- LOW SWITCHING GLITCH: 40mV_{PP}
- 3100V/µs SLEW RATE
- 0.025%/0.025° DIFFERENTIAL GAIN, PHASE
- HIGH GAIN ACCURACY: 2.0V/V ±0.4%

APPLICATIONS

- RGB SWITCHING
- LCD PROJECTOR INPUT SELECT
- WORKSTATION GRAPHICS
- TRIPLE ADC INPUT MUX
- DROP-IN UPGRADE TO LT1675



RGB Switching

DESCRIPTION

The OPA3875 offers a very wideband, 3-channel, 2:1 multiplexer in a small SSOP-16 package. Using only 11mA/ch, the OPA3875 provides three, gain of +2, video amplifier channels with greater than 400MHz large-signal bandwidth (4V_{PP}). Gain accuracy and switching glitch are improved over earlier solutions using a new (patented) input stage switching approach. This technique uses current steering as the input switch while maintaining an overall closed-loop design. Gain matching between each of the 3-channel pairs is also significantly improved using this technique (<0.2% gain mismatch). With greater than 700MHz small-signal bandwidth at a gain of 2, the OPA3875 gives a typical 0.1dB gain flatness to greater than 150MHz.

System power may be reduced using the chip enable feature for the OPA3875. Taking the chip enable line high powers down the OPA3875 to less than 900µA total supply current. Muxing multiple OPA3875 outputs together, then using the chip enable to select which channels are active, increases the number of possible inputs to the 3-channel outputs.

Where a single channel of the OPA3875 is required, consider the OPA875.

OPA3875				
SELECT	**$\overline{\text{ENABLE}}$**	**RED OUT**	**GREEN OUT**	**BLUE OUT**
1	0	R0	G0	B0
0	0	R1	G1	B1
X	1	Off	Off	Off

OPA3875 RELATED PRODUCTS

	DESCRIPTION
OPA875	Single-Channel OPA3875
OPA4872	Quad 510MHz 4:1 Multiplexer
OPA3693	Triple 650MHz Video Buffer

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3875	SSOP-16	DBQ	–45°C to +85°C	OP3875	OPA3875IDBQ	Rails, 75
					OPA3875IDBQR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

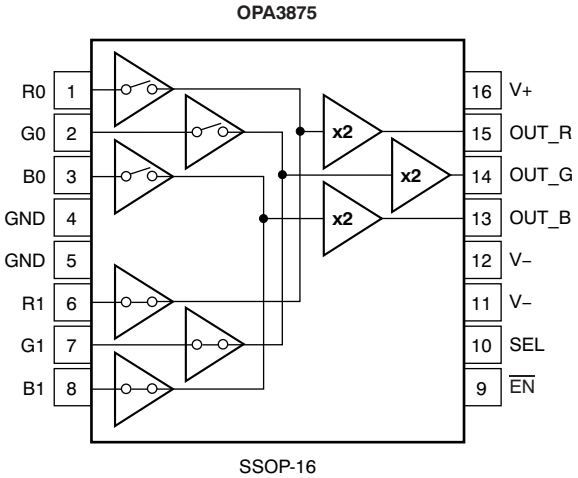
ABSOLUTE MAXIMUM RATINGS

Over operating temperature range, unless otherwise noted.

	OPA3875	UNIT
Power Supply	±6.5	V
Internal Power Dissipation	See Thermal Analysis	
Input Voltage Range	$\pm V_S$	V
Storage Temperature Range	–65 to +125	°C
Lead Temperature (soldering, 10s)	+260	°C
Operating Junction Temperature	+150	°C
Continuous Operating Junction Temperature	+140	°C
ESD Rating:		
Human Body Model (HBM)	2000	V
Charge Device Model (CDM)	1500	V
Machine Model (MM)	200	V

PIN CONFIGURATION

Top View SSOP



SSOP-16

ELECTRICAL CHARACTERISTICS: V_S = ±5V

At G = +2, R_L = 150Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3875 TYP +25°C	OPA3875 MIN/MAX OVER TEMPERATURE +25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/MAX	TEST LEVEL[1]
AC PERFORMANCE	See Figure 1							
Small-Signal Bandwidth	V_O = 200mV$_{PP}$, R_L = 150Ω	700	525	515	505	MHz	min	B
Large-Signal Bandwidth	V_O = 4V$_{PP}$, R_L = 150Ω	425	390	380	370	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	V_O = 200mV$_{PP}$	150				MHz	typ	C
Maximum Small-Signal Gain	V_O = 200mV$_{PP}$, R_L = 150Ω, f = 5MHz	2.0	2.02	2.03	2.05	V/V	max	B
Minimum Small-Signal Gain	V_O = 200mV$_{PP}$, R_L = 150Ω, f = 5MHz	2.0	1.98	1.97	1.95	V/V	min	B
SFDR	10MHz, V_O = 2V$_{PP}$, R_L = 150Ω	–68	–65	–64	–63	dBc	max	B
Input Voltage Noise	f > 100kHz	6.7	7.0	7.2	7.4	nV/√Hz	max	B
Input Current Noise	f > 100kHz	3.8	4.2	4.6	4.9	pA/√Hz	max	B
NTSC Differential Gain	R_L = 150Ω	0.025				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.025				°	typ	C
Slew Rate	V_O = ±2V	3100	2800	2700	2600	V/µs	min	B
Rise Time and Fall Time	V_O = 0.5V Step	460				ps	typ	C
	V_O = 1.4V Step	600				ps	typ	C
CHANNEL-TO-CHANNEL PERFORMANCE								
Gain Match	Channel to Channel, R_L = 150Ω	±0.05	**±0.25**	±0.3	±0.35	%	max	A
	All inputs, R_L = 150Ω	±0.1	**±0.5**	±0.6	±0.7	%	max	A
Output Offset Voltage Mismatch	All three outputs	±3	**±9**	±10	±12	mV	max	A
All Hostile Crosstalk	f = 50MHz, R_L = 150Ω	–50				dB	typ	C
Channel-to-Channel Crosstalk	f = 50MHz, R_L = 150Ω	–58				dB	typ	C
CHANNEL AND CHIP-SELECT PERFORMANCE								
SEL (Channel Select) Swtiching Time	R_L = 150Ω	4				ns	typ	C
$\overline{EN}$ (Chip Select) Switching Time	Turn On	9				ns	typ	C
	Turn Off	60				ns	typ	C
SEL (Channel Select) Switching Glitch	All Inputs to Ground, At Matched Load	40				mV$_{PP}$	typ	C
$\overline{EN}$ (Chip-Select) Switching Glitch	All Inputs to Ground, At Matched Load	15				mV$_{PP}$	typ	C
All Hostile Disable Feedthrough	50MHz, Chip Disabled ($\overline{EN}$ = High)	–68				dB	typ	C
Maximum Logic 0	$\overline{EN}$, SEL		0.8	0.8	0.8	V	max	B
Minimum Logic 1	$\overline{EN}$, SEL		2.0	2.0	2.0	V	min	B
$\overline{EN}$ Logic Input Current	0V to 4.5V	75	**100**	125	150	µA	max	A
SEL Logic Input Current	0V to 4.5V	160	**200**	250	300	µA	max	A
DC PERFORMANCE								
Output Offset Voltage	R_{IN} = 0Ω, G = +2V/V	±2.5	**±14**	±15.8	±17	mV	max	A
Average Output Offset Voltage Drift	R_{IN} = 0Ω, G = +2V/V			±50	±50	µV/°C	max	B
Input Bias Current		±5	**±18**	±19.5	±20.5	µA	max	A
Average Input Bias Current Drift				±40	±40	nA/°C	max	B
Gain Error (from 2V/V)	V_O = ±2V	0.4	**1.4**	1.5	1.6	%	max	A
INPUT								
Input Voltage Range		±2.8				V	typ	C
Input Resistance		1.75				MΩ	typ	C
Input Capacitance	Channel Selected	0.9				pF	typ	C
	Channel Deselected	0.9				pF	typ	C
	Chip Disabled	0.9				pF	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +36°C at high temperature limit for over temperature specifications.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2, R_L = 150Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3875 TYP +25°C	OPA3875 MIN/MAX OVER TEMPERATURE +25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
OUTPUT								
Output Voltage Range		±3.5	**±3.4**	±3.35	±3.3	V	min	A
Output Current	V_O = 0V, Linear Operation	±70	**±50**	±45	±40	mA	min	A
Output Resistance	Chip enabled	0.3				Ω	typ	C
	Chip Disabled, Maximum	800	**912**	915	918	Ω	max	A
	Chip Disabled, Minumum	800	**688**	685	682	Ω	min	A
Output Capacitance	Chip Disabled	2				pF	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Minimum Operating Voltage			±3.0	±3.0	±3.0	V	min	B
Maximum Operating Voltage			**±6.3**	±6.3	±6.3	V	max	A
Maximum Quiescent Current	Chip Selected, V_S = ±5V	33	**34**	35	36	mA	max	A
Minimum Quiescent Current	Chip Selected, V_S = ±5V	33	**31**	30	27	mA	min	A
Maximum Quiescent Current	Chip Deselected	0.9	**1.2**	1.4	1.5	mA	max	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	56	**50**	48	47	dB	min	A
(–PSRR)	Input-Referred	55	**51**	49	48	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range D Package		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}	Junction-to-Ambient							
DBQ SSOP-16		85				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At G = +2 and R_L = 150Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

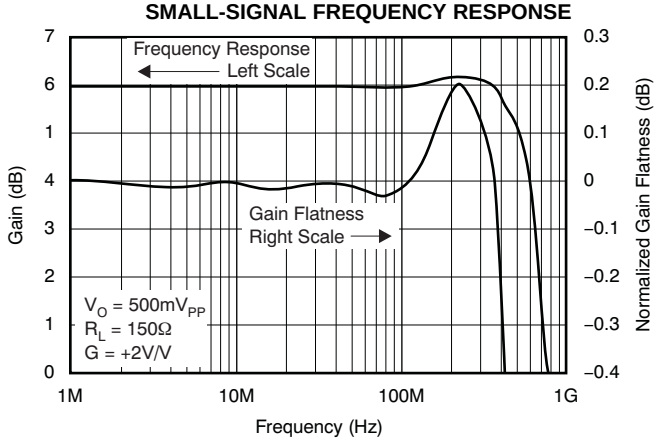


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

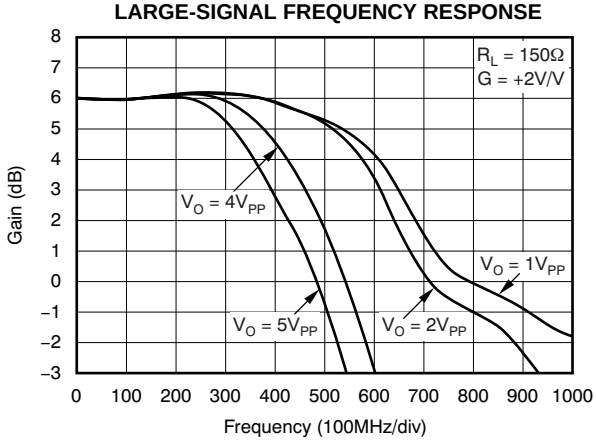


Figure 2.

NONINVERTING PULSE RESPONSE

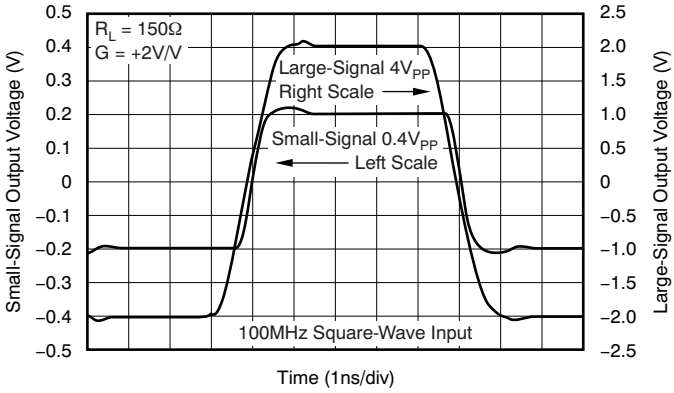


Figure 3.

ALL INPUT DISABLE FEEDTHROUGH vs FREQUENCY

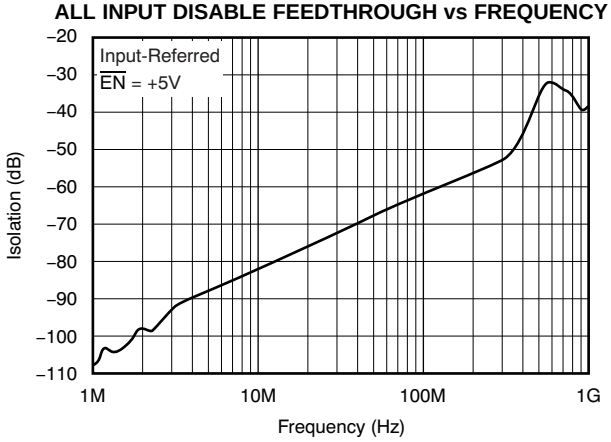


Figure 4.

RECOMMENDED R_S vs CAPACITIVE LOAD

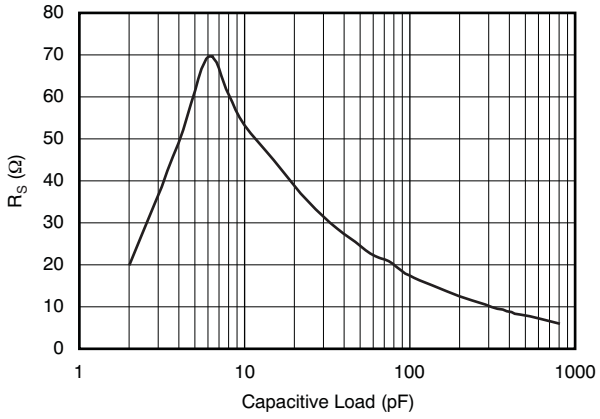


Figure 5.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

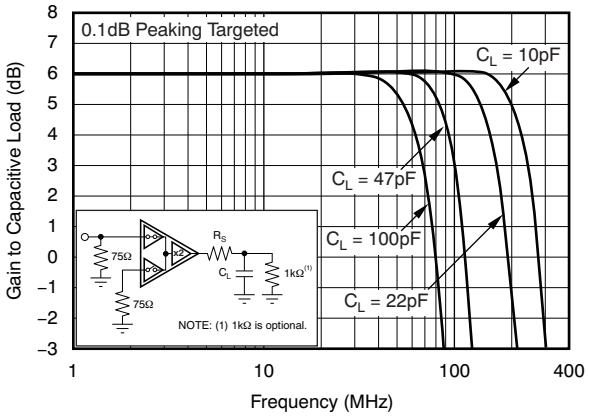


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

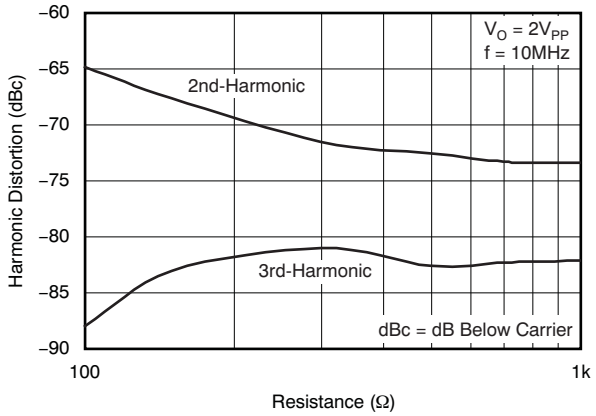


Figure 7.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

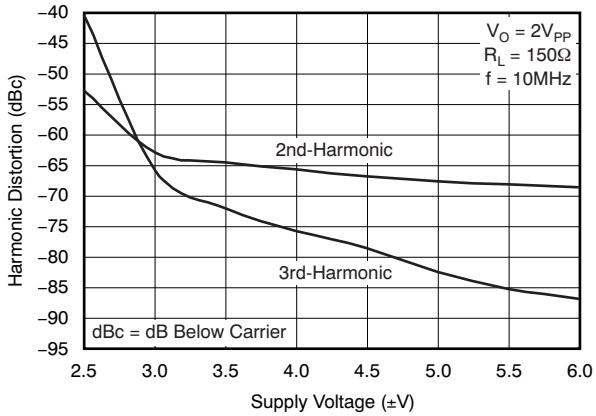


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

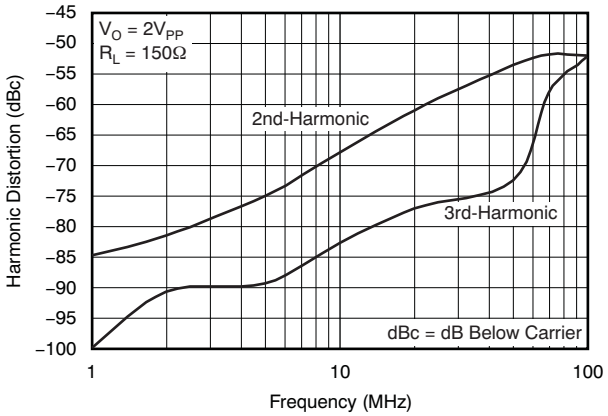


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

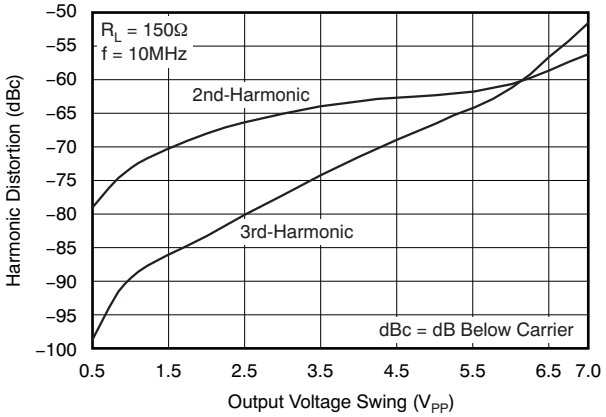


Figure 10.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

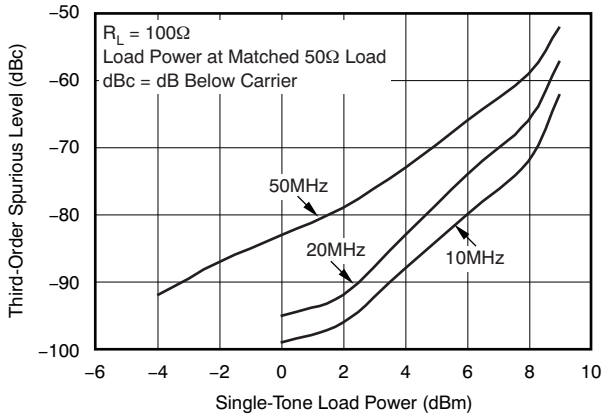


Figure 11.

OUTPUT VOLTAGE AND CURRENT LIMITIATIONS

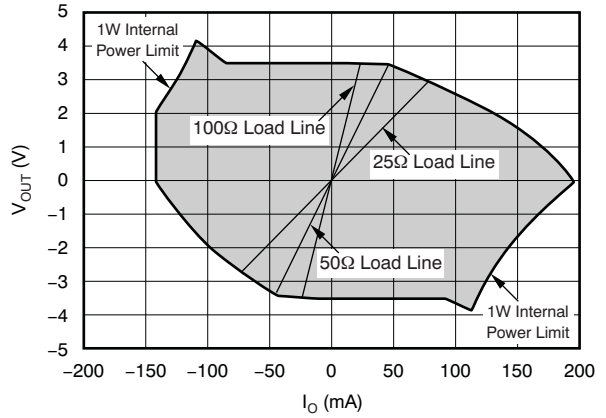


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

CHANNEL SWITCHING

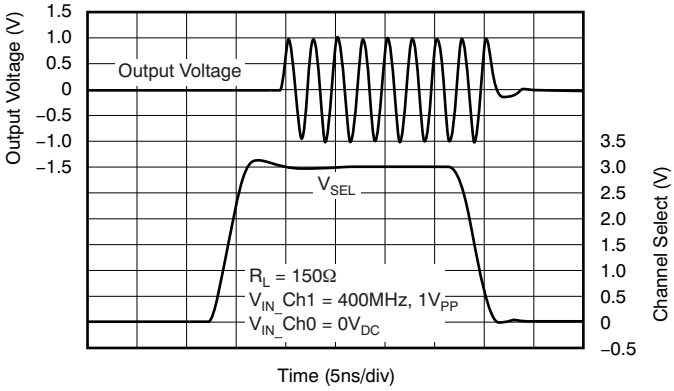


Figure 13.

CHANNEL-TO-CHANNEL SWITCHING TIME

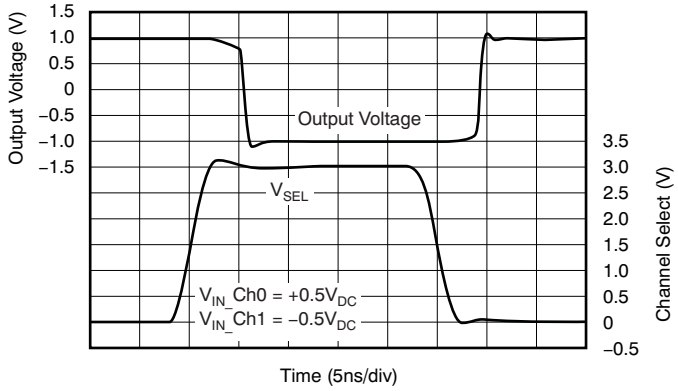


Figure 14.

CHANNEL SWITCHING GLITCH

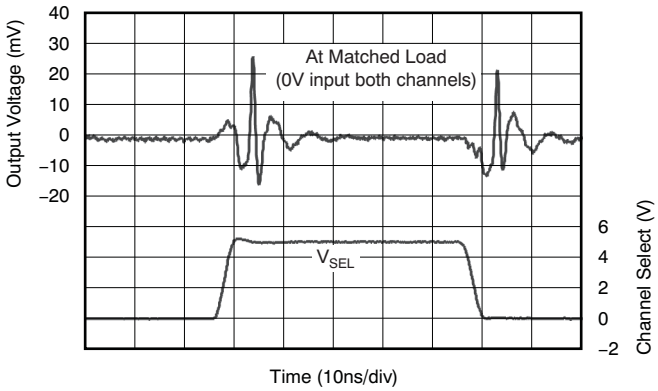


Figure 15.

DISABLE/ENABLE TIME

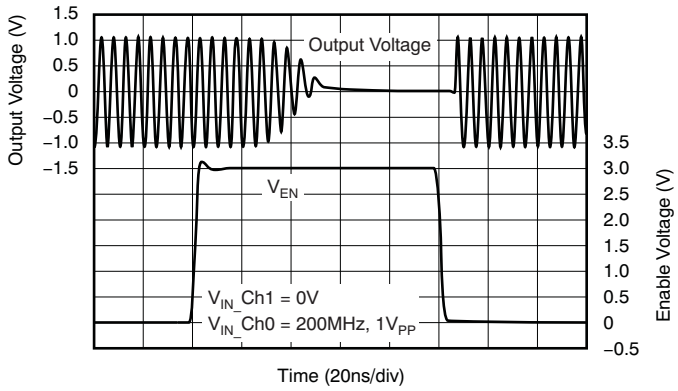


Figure 16.

DISABLE/ENABLE SWITCHING GLITCH

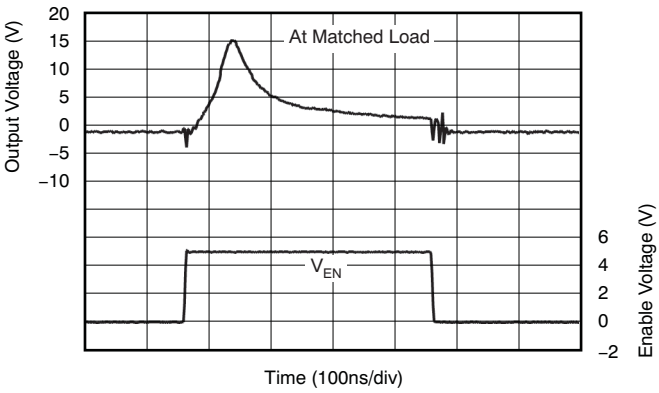


Figure 17.

CHANNEL-TO-CHANNEL CROSSTALK

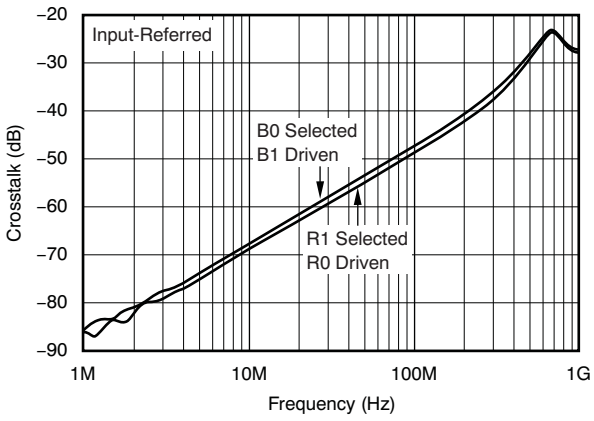


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

ALL HOSTILE AND ADJACENT-CHANNEL CROSSTALK vs FREQUENCY

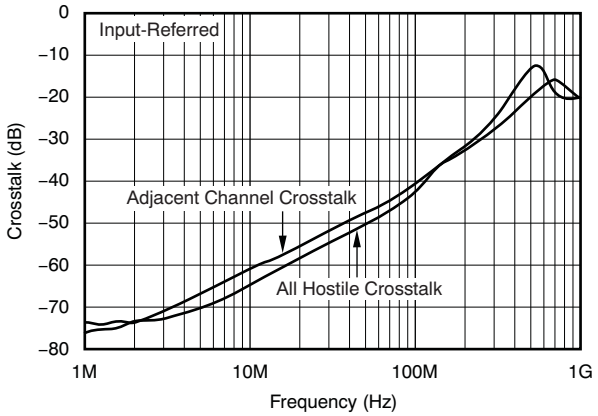


Figure 19.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

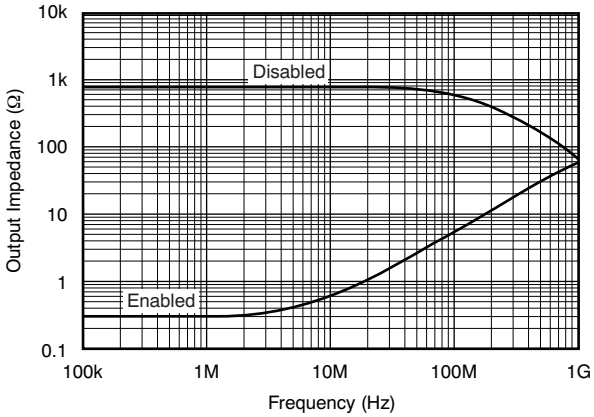


Figure 20.

INPUT IMPEDANCE vs FREQUENCY

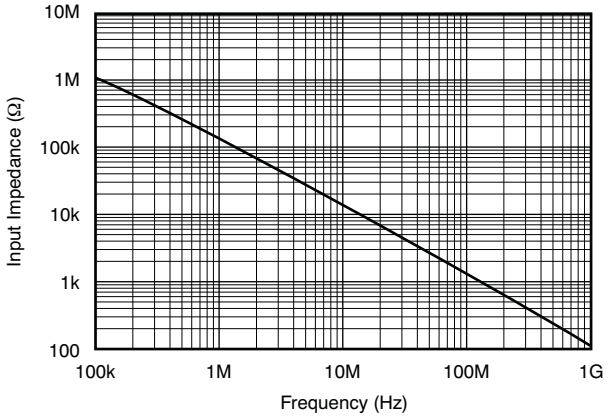


Figure 21.

PSRR vs FREQUENCY

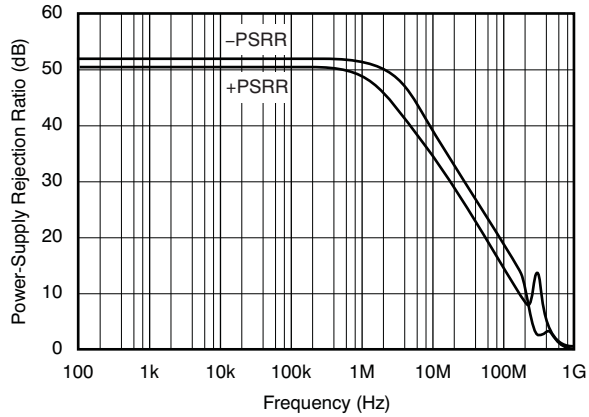


Figure 22.

SUPPLY CURRENT vs TEMPERATURE

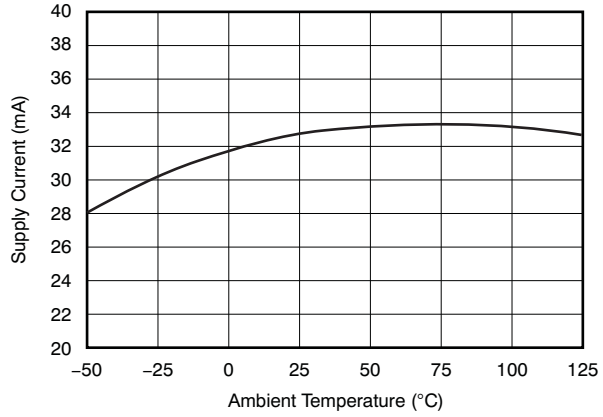


Figure 23.

TYPICAL DC DRIFT OVER TEMPERATURE

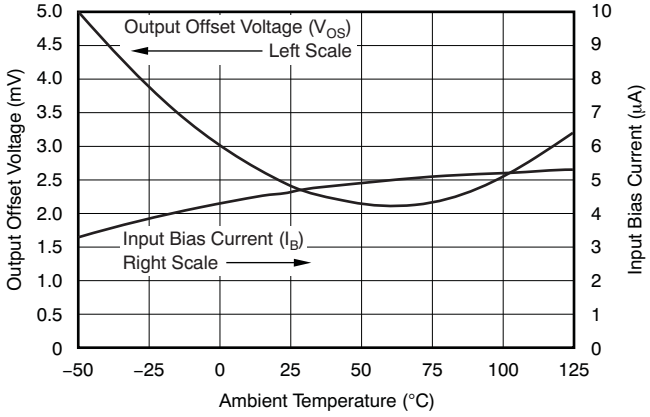


Figure 24.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

INPUT VOLTAGE AND CURRENT NOISE

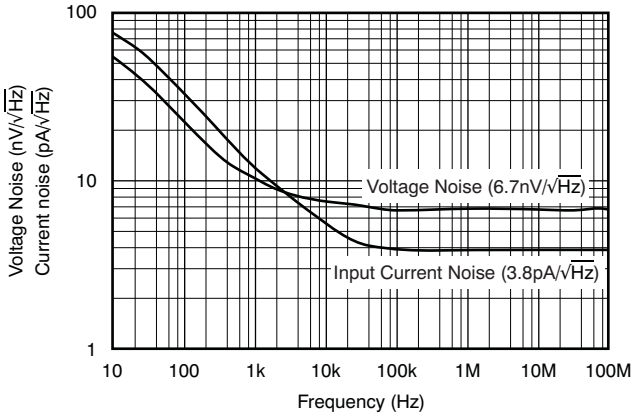


Figure 25.

APPLICATIONS INFORMATION

2:1 HIGH-SPEED VIDEO MULTIPLEXER OPERATION

The OPA3875 can be used as a triple 2:1 high-speed video multiplexer, as illustrated in the front page schematic for an RGB signal. Figure 26 shows a simplified version of the front page schematic in which one output is shown with its input and output impedance matching resistors.

RGB VIDEO INVERTER

Figure 27 illustrates an extension of the previously shown RGB switching circuit with a noninverting signal going through channel 1 and an inverted signal going through channel two. Here, the output impedance of the OPA3875 is set to 75Ω. Looking at the input part of this circuit, we see that the RGB signal is inverted with an OPA3693 fixed gain set in an inverting configuration with a reference voltage on the noninverting node. The reference voltage, set here at 0.714V, has a gain of 1 at the output of the OPA3691 as the input signal is AC-coupled (not represented here). This bias voltage is required to prevent the video from swinging negative. Note also that the 75Ω input matching impedance is set here by the parallel combination of 92Ω and 402Ω. In order not to disturb the sync, color burst, and blanking if present, the inverting amplifiers are only switched on during active video.

LOGO INSERTER

Figure 28 illustrates the principle of overlaying a picture in a picture. The picture comes through U1; the signal to be overlayed comes through U2. Here we have a reference voltage of 0.714V in channel 2 indicating that we will highlight a section of the picture with white (for NTSC-related RGB video). How much white comes through depends on the combination of select 1 and select 2 pins as well as the series output resistance of each OPA3875. To match the 75Ω output impedance of the video cable, the parallel combination of the series output resistance (R and nR) needs to be 75Ω. The two select pins gives us 2 bits of control. By selecting n = 2, you have the capability of a 0% highlight (full original video signal), 33% highlight, 66% highlight, and 100% highlight (all white). By selecting n = 3, you have 0%, 25%, 75%, and 100% highlight capabilities, etc.

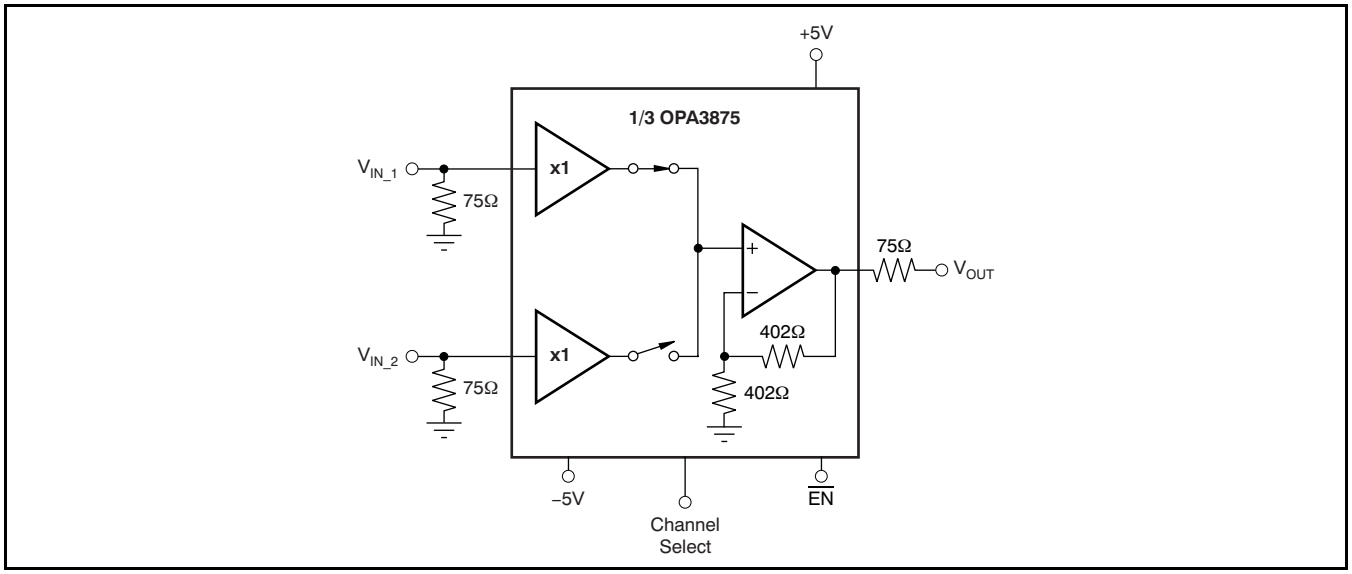


Figure 26. Triple 2:1 High-Speed Video Multiplexer

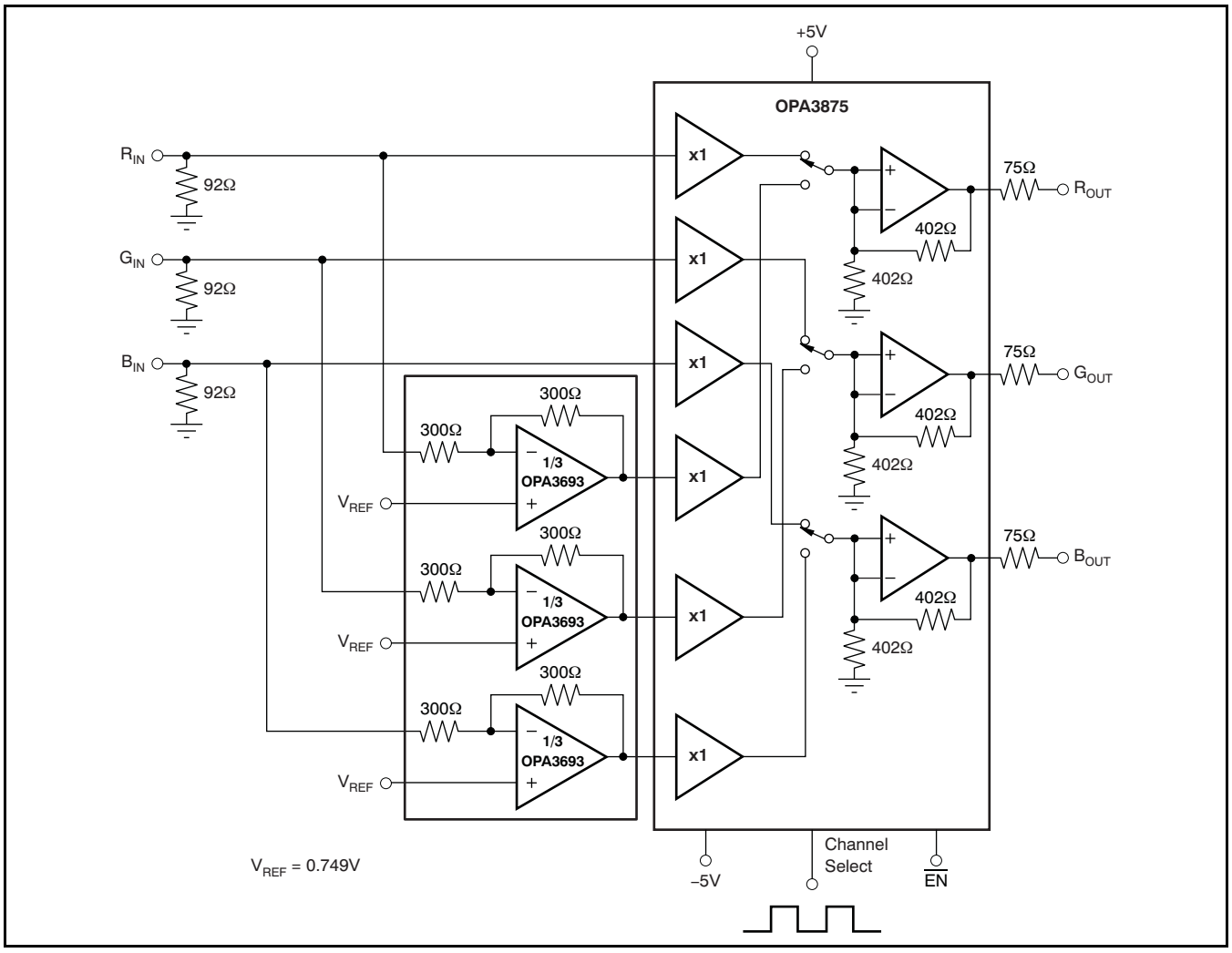


Figure 27. RGB Video Inverter

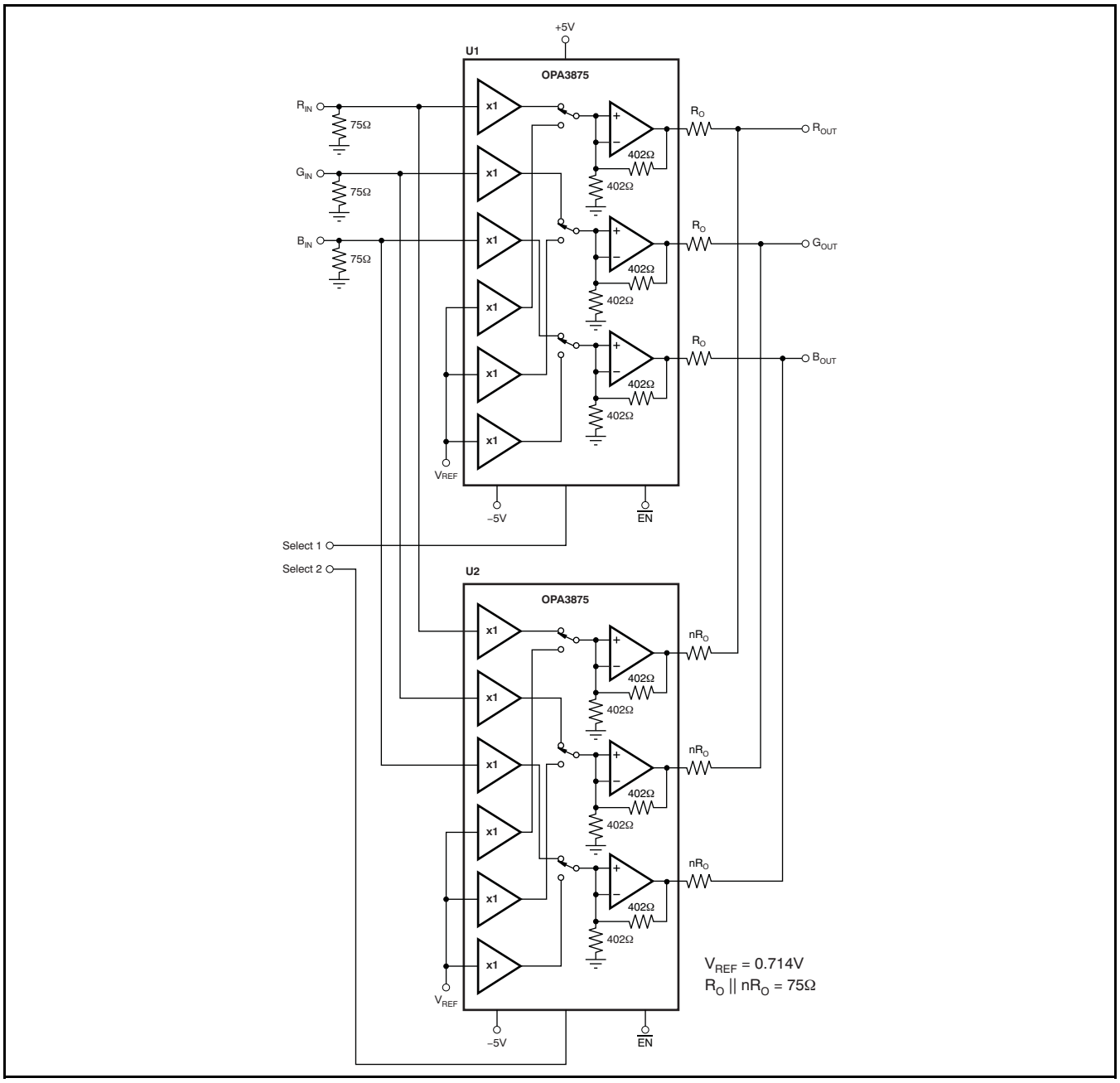


Figure 28. Logo Inserter

ADC INPUT MUX

Figure 29 shows the OPA3875 used as a multiplexer in a high-speed data acquisition signal chain.

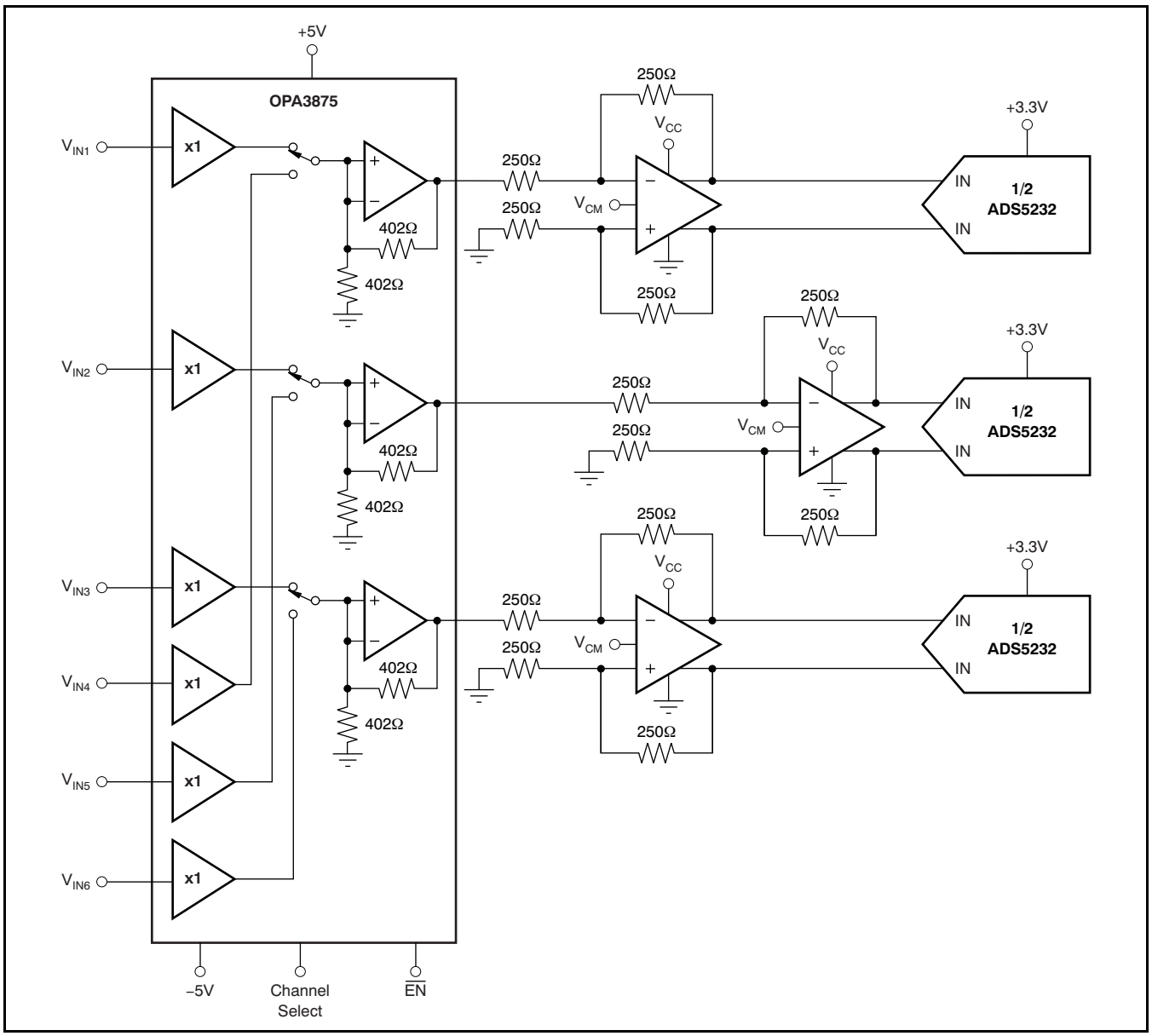


Figure 29. ADC Input Multiplexer

DESIGN-IN TOOLS

DEMONSTRATION FIXTURE

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA3875. The fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 1.

Table 1. OPA3875 Demonstration Fixture

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA3875IDBQ	SSOP-16	DEM-OPA-SSOP-3E	SBOU043

The demonstration fixture can be requested at the Texas Instruments web site at (www.ti.com) through the OPA3875 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA875 is available through the Texas Instruments web site at www.ti.com. Use three of these models to simulate the OPA3875. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance nor do they predict channel-to-channel effects.

OPERATING SUGGESTIONS

DRIVING CAPACITIVE LOADS

One of the most demanding, yet very common load conditions is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed device such as the OPA3875 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the device open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This isolation resistor does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load; see Figure 5 and Figure 6, respectively. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA3875. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA3875 output pin (see the Board Layout Guidelines section).

DC ACCURACY

The OPA3875 offers excellent DC signal accuracy. Parameters that influence the output DC offset voltage are:

- Output offset voltage
- Input bias current
- Gain error
- Power-supply rejection ratio
- Temperature

Leaving both temperature and gain error parameters aside, the output offset voltage envelope can be described as shown in Equation 1:

$$V_{OSO\_envelope} = V_{OSO} + (R_S \bullet I_b) \times G \pm \left|5 - (V_{S+})\right| \times 10^{-\frac{PSRR+}{20}} \pm \left|-5 - (V_{S+})\right| \times 10^{-\frac{PSRR-}{20}} + V_{CM} \times 10^{-\frac{CMRR}{20}} \quad (1)$$

With:

V_{OSO}: Output offset voltage

R_S: Input resistance seen by R0, R1, G0, G1, B0, or B1.

I_b: Input bias current

G: Gain

V_{S+}: Positive supply voltage

V_{S-}: Negative supply voltage

PSRR+: Positive supply PSRR

PSRR–: Negative supply PSRR

Evaluating the front-page schematic, using a worst-case, +25°C offset voltage, bias current and PSRR specifications and operating at ±6V, gives a worst-case output equal to Equation 2:

$$\pm 14mV + 75\Omega \times \pm 18\mu A \times 2 \pm \left|5 - 6\right| \times 10^{-\frac{50}{20}} \pm \left|-5 - (-6)\right| \times 10^{-\frac{51}{20}} = \pm 22.7mV \quad (2)$$

DISTORTION PERFORMANCE

The OPA3875 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2X rate while the 3rd-harmonic increases at a little less than the expected 3X rate. Where the test power doubles, the 2nd-harmonic increases only by less than the expected 6dB, whereas the 3rd-harmonic increases by less than the expected 12dB. This also shows up in the two-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 4dBm/tone into a matched 50Ω load (that is, $1V_{PP}$ for each tone at the load, which requires $4V_{PP}$ for the overall 2-tone envelope at the output pin), the Typical Characteristics show a 82dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels.

NOISE PERFORMANCE

The OPA3875 offers an excellent balance between voltage and current noise terms to achieve low output noise. As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. Figure 30 shows this device noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

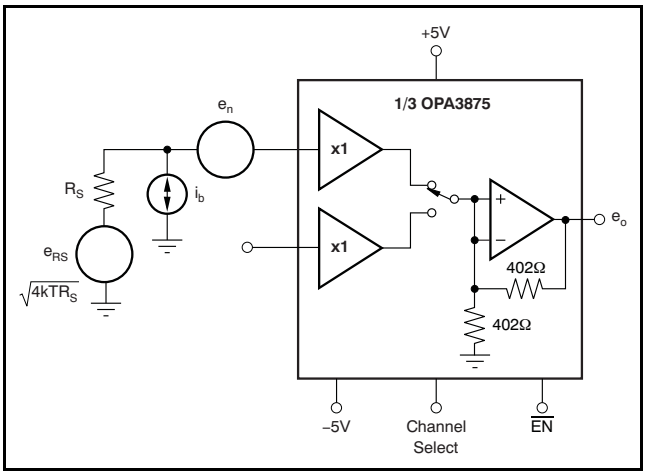


Figure 30. Noise Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms shown in Figure 30.

$$e_o = 2\sqrt{e_n^2 + (i_b R_S)^2 + 4kTR_S} \quad (3)$$

Dividing this expression by the device gain (2V/V) gives the equivalent input-referred spot noise voltage at the noninverting input as shown in Equation 4.

$$e_n = \sqrt{e_n^2 + (i_b R_S)^2 + 4kTR_S} \quad (4)$$

Evaluating these two equations for the OPA3875 circuit and component values shown in Figure 26 gives a total output spot noise voltage of 13.6nV/√Hz and a total equivalent input spot noise voltage of 6.8nV/√Hz. This total input-referred spot noise voltage is higher than the 6.7nV/√Hz specification for the mux voltage noise alone. This number reflects the noise added to the output by the bias current noise times the source resistor.

THERMAL ANALYSIS

Heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as discussed in this document. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but, for a grounded resistive load, is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA3875 in the circuit of Figure 26 operating at the maximum specified ambient temperature of +85°C with all three outputs driving a grounded 100Ω load to +2.5V:

$P_D = 10V \times 36mA + 3(5^2/4 \times (100\Omega \parallel 804\Omega)) = 571mW$

Maximum $T_J = +85°C + (0.57W \times 85°C/W) = 133°C$

This worst-case condition is approaching the maximum +150°C junction temperature. Normally, this extreme case is not encountered. Careful attention to internal power dissipation is required.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier such as the OPA3875 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output pin can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 9, 11, 13, and 15) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA3875. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Figure 5. Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA3875 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the Distortion versus Load plots.

With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA3875 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA3875 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in Figure 5. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA3875 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA3875 onto the board.

INPUT AND ESD PROTECTION

The OPA3875 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 31.

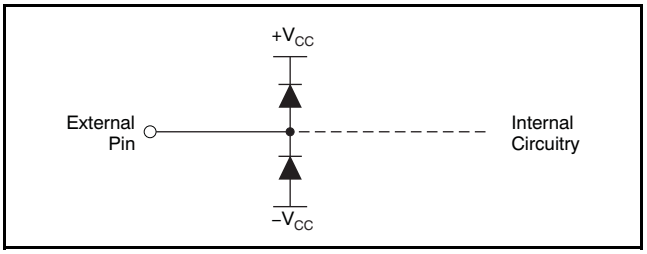


Figure 31. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA3875), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

Revision History

Changes from Revision C (September 2007) to Revision D **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2

Changes from Revision B (December 2006) to Revision C **Page**

- Changed the ordering number column in Table 1. 14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA3875IDBQ	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP3875
OPA3875IDBQ.A	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP3875
OPA3875IDBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP3875
OPA3875IDBQR.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP3875

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

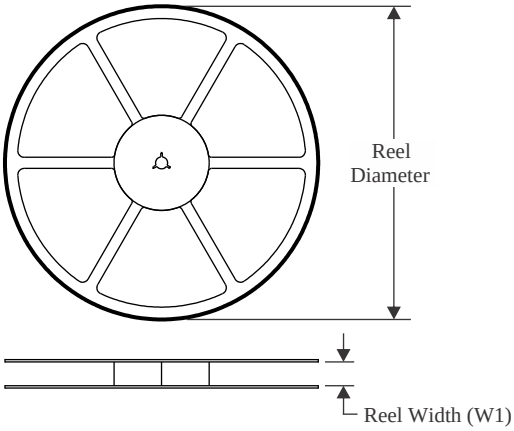
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

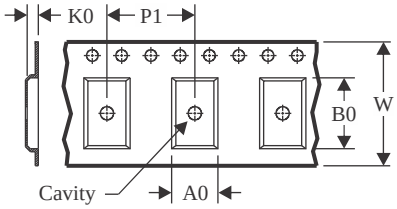
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

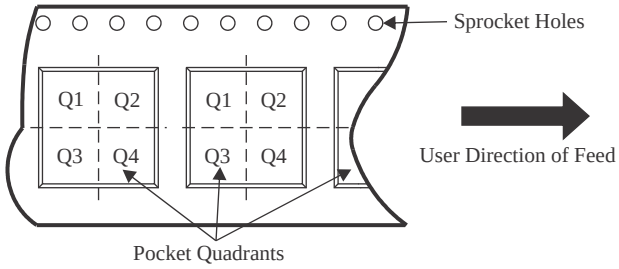


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

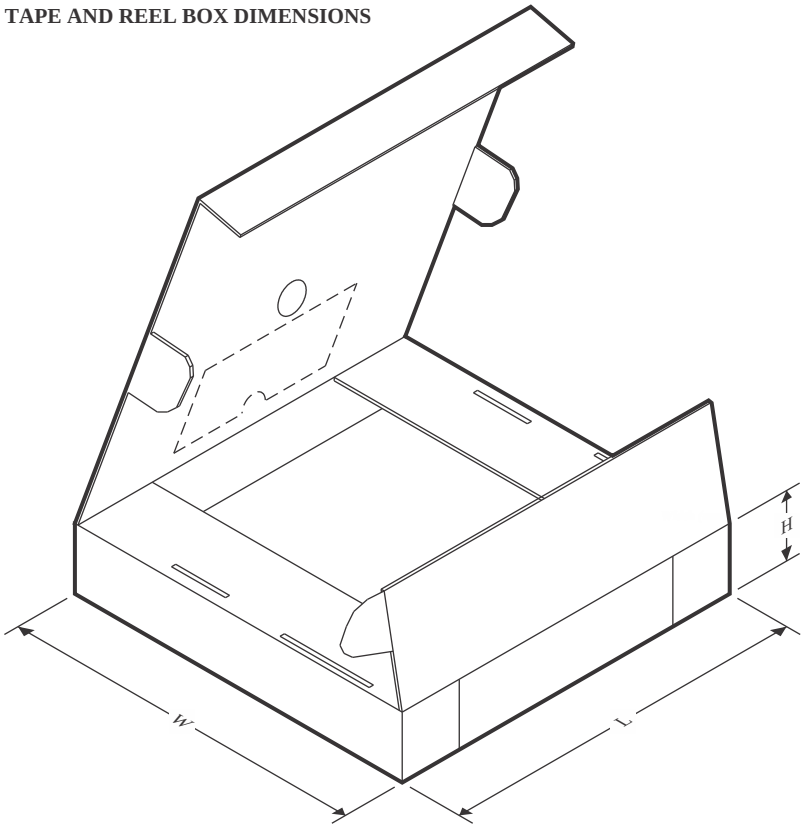
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA3875IDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

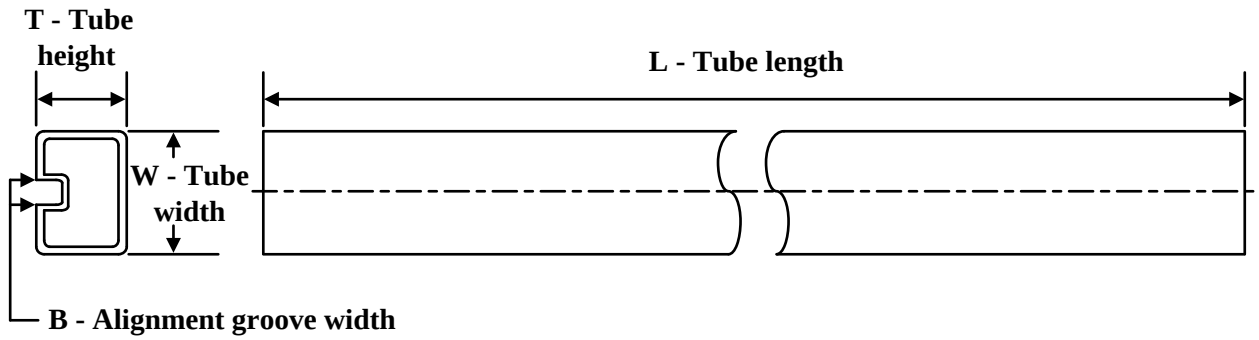
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

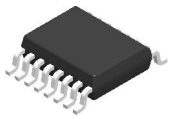
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA3875IDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA3875IDBQ	DBQ	SSOP	16	75	506.6	8	3940	4.32
OPA3875IDBQ.A	DBQ	SSOP	16	75	506.6	8	3940	4.32

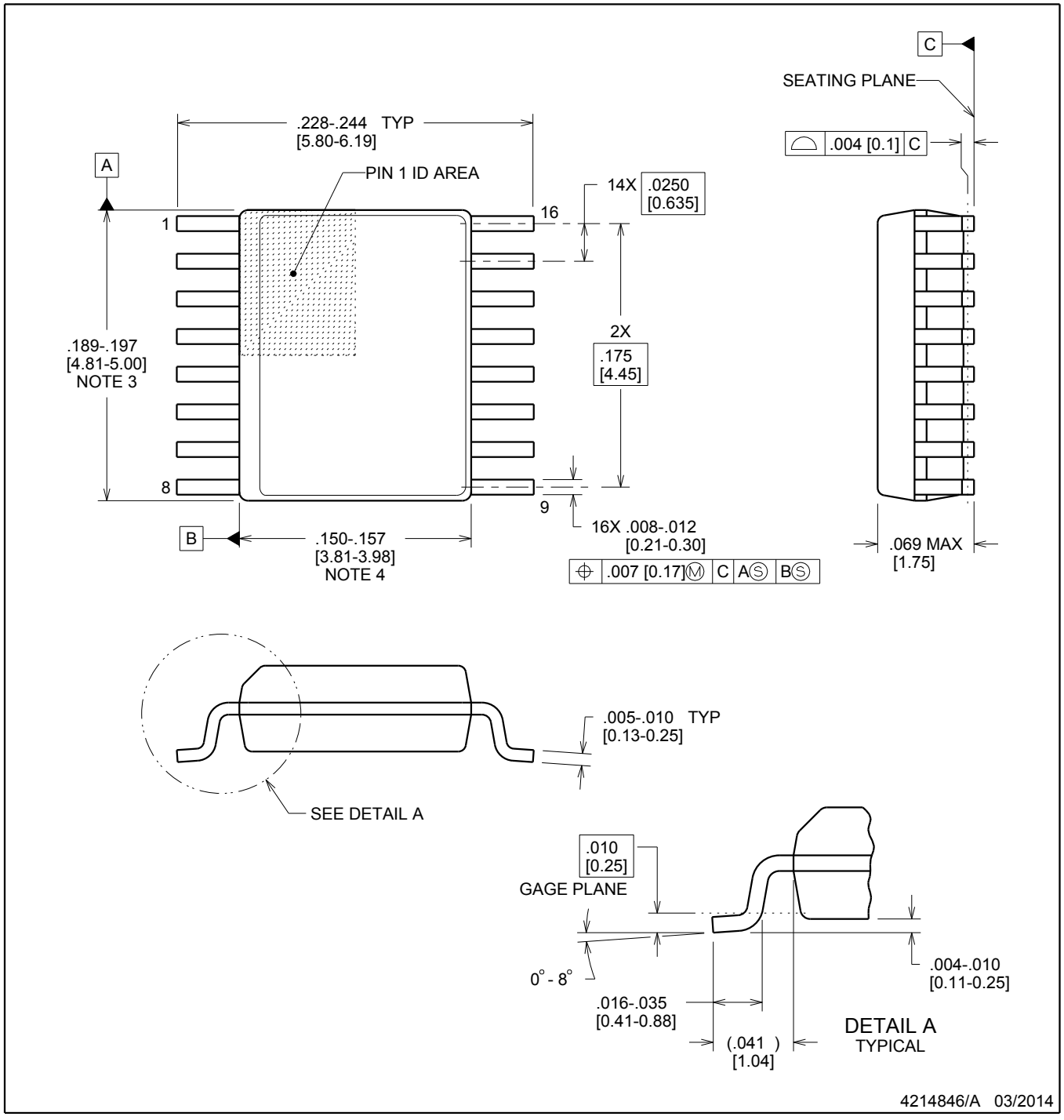


PACKAGE OUTLINE

DBQ0016A

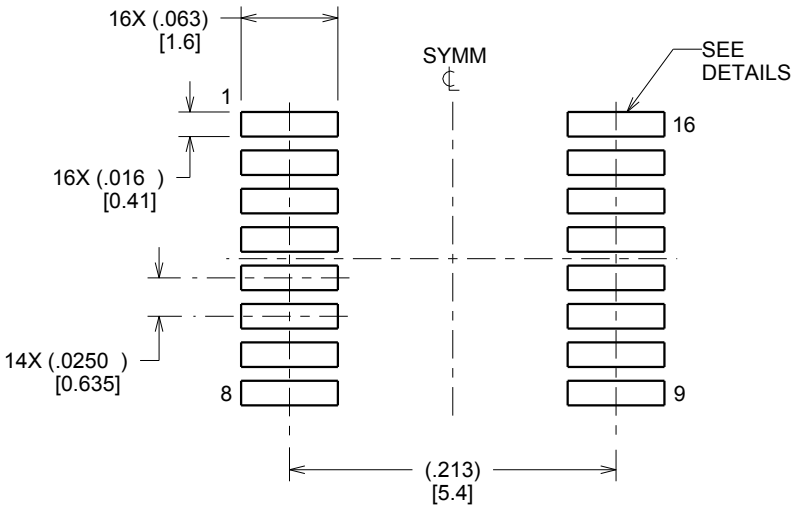
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

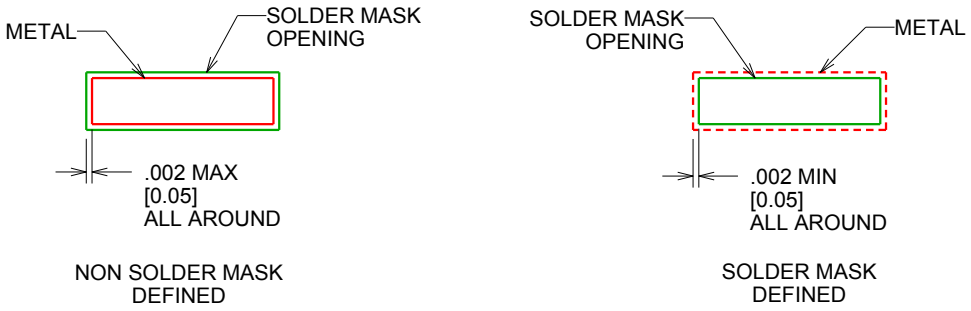


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

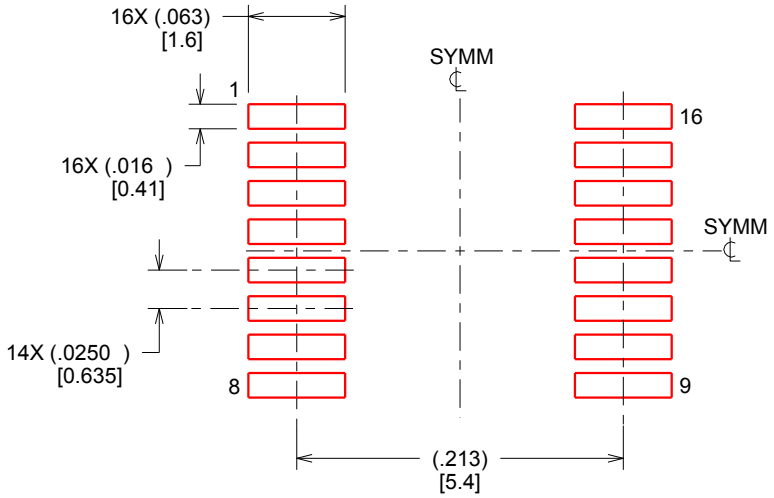
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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