

OPAx396 Precision, Low I_Q, Low Input Bias Current Op Amps

1 Features

- Low I_Q: 23.5µA
- Gain bandwidth product: 1MHz
- Low input bias current: 10fA (typical)
- Low offset voltage: ±100µV (maximum)
- Low drift: ±1.2µV/°C
- Low supply voltage operation: 1.7V to 5.5V
- Input common mode range ±100mV beyond rail
- Fast slew rate: 1V/µs
- High load capacitance drive
- High output current drive: 60mA
- Rail-to-rail output
- EMI/RFI filtered inputs

2 Applications

- [Portable electronics](#)
- [Flow transmitter](#)
- [Blood glucose monitor](#)
- [Process analytics \(pH, gas, force, humidity\)](#)
- [Temperature transmitter](#)
- [Pressure transmitter](#)
- [Medical sensor patches](#)
- [Building automation](#)
- [Wearable fitness and activity monitor](#)
- [Gas detector](#)
- [Analog security camera](#)

3 Description

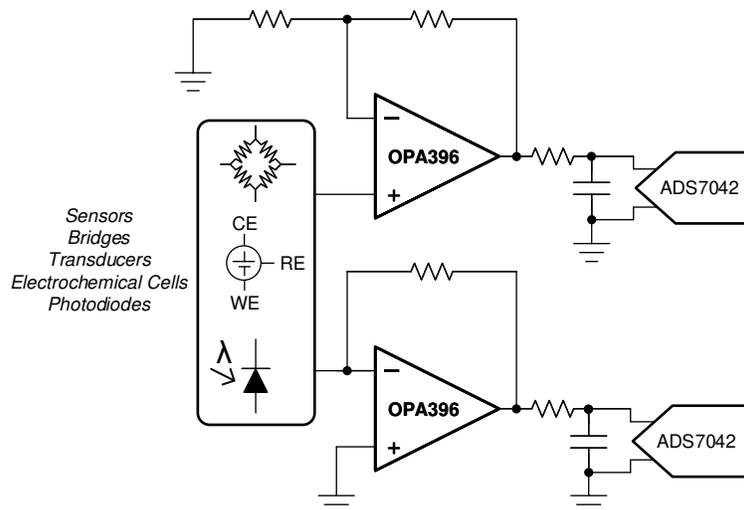
The OPA396, OPA2396, and OPA4396 (OPAx396) feature a combination of high bandwidth (1MHz) along with very low quiescent current (23.5µA) in a high-precision amplifier. These features combined with rail-to-rail input and output make these devices an excellent choice in high-gain, low-power applications. An ultra-low input bias current of 10fA, 100µV of offset (maximum), and 1.2µV/°C of drift over temperature help maintain high precision in ratiometric and amperometric sensor front ends that have demanding low-power requirements.

The OPAx396 use Texas Instrument's proprietary e-trim™ operational amplifier technology, enabling a unique combination of ultra-low offset and low input offset drift without the need for any input switching or auto-zero techniques. The CMOS-based technology platform also features a modern, robust output stage design that is tolerant of high output capacitance, alleviating stability problems that are common in typical low-power amplifiers.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
OPA396	Single	DCK (SC70, 5)	2.00mm × 2.1mm
OPA2396	Dual	DGK (VSSOP, 8)	3.0mm × 4.9mm
OPA4396	Quad	PW (TSSOP, 14)	5.0mm × 6.4mm

- (1) For all available packages, see the package option addendum at the end of the datasheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



High-Input-Impedance, Low-Offset Buffer



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4 Pin Configuration and Functions

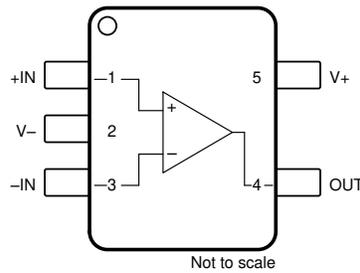


Figure 4-1. OPA396: DCK (5-Pin SC70) Package, Top View

Table 4-1. Pin Functions: OPA396

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
-IN	3	I	Inverting input
+IN	1	I	Noninverting input
OUT	4	O	Output
V-	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

(1) I = Input; O=Output

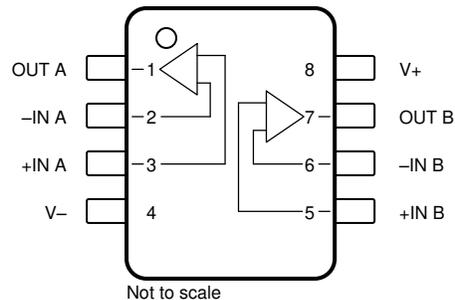
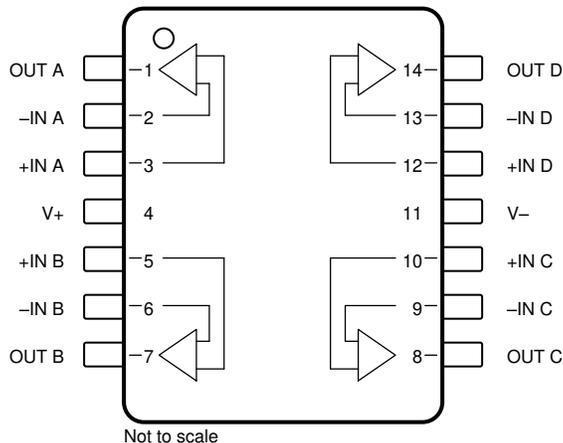


Figure 4-2. OPA2396 DGK Package
8-Pin VSSOP
Top View

Table 4-2. Pin Functions: OPA2396

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
-IN A	B1	I	Inverting input, channel A
-IN B	B3	I	Inverting input, channel B
+IN A	C1	I	Noninverting input, channel A
+IN B	C3	I	Noninverting input, channel B
EN	B2	I	Enable pin. High = both amplifiers enabled.
OUT A	A1	O	Output, channel A
OUT B	A3	O	Output, channel B
V-	C2	—	Negative (lowest) power supply
V+	A2	—	Positive (highest) power supply

(1) I = Input; O=Output



Not to scale

**Figure 4-3. OPA4396 PW Package
14-Pin TSSOP
Top View**

Table 4-3. Pin Functions: OPA4396

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	NO.	PW (TSSOP)		
-IN A	2		I	Inverting input, channel A
-IN B	6		I	Inverting input, channel B
-IN C	9		I	Inverting input, channel C
-IN D	13		I	Inverting input, channel D
+IN A	3		I	Noninverting input, channel A
+IN B	5		I	Noninverting input, channel B
+IN C	10		I	Noninverting input, channel C
+IN D	12		I	Noninverting input, channel D
EN AB	—		I	Enable pin for A and B amplifiers. High = amplifiers A and B are enabled.
EN CD	—		I	Enable pin for C and D amplifiers. High = amplifiers C and D are enabled.
OUT A	1		O	Output, channel A
OUT B	7		O	Output, channel B
OUT C	8		O	Output, channel C
OUT D	14		O	Output, channel D
Thermal Pad	—		—	Connect thermal pad to V-
V-	11		—	Negative (lowest) power supply
V+	4		—	Positive (highest) power supply

(1) I = Input; O=Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.5	
	Input current, all pins			±10	mA
	Output short circuit ⁽²⁾		Continuous	Continuous	
T _A	Operating temperature		–55	150	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
	Input voltage	Differential	–0.5		+0.5	
T _A	Specified temperature		–40		125	°C

5.4 Thermal Information: OPA396

THERMAL METRIC ⁽¹⁾		OPA396	
		DCK (SC70)	
		5 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Thermal Information: OPA2396

THERMAL METRIC ⁽¹⁾		OPA2396	
		DGK (VSSOP)	
		8 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.6 Thermal Information: OPA4396

THERMAL METRIC ⁽¹⁾		OPA4396	
		PW (TSSOP)	
		14 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.7 Electrical Characteristics

at $V_S = 1.7V$ to $5.5V$, $T_A = 25^\circ C$, and $V_{CM} = V_S / 2$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$V_S = 5.0V$		± 10	± 100	μV
		$V_{CM} = (V+) - 0.3V, V_S = 5.0V$		± 60	± 750	
		$V_{CM} = (V-) - 0.1V$	$T_A = -40^\circ C$ to $+125^\circ C^{(1)}$	± 15	± 100	
dV_{OS}/dT	Input offset voltage drift	$T_A = 0^\circ C$ to $85^\circ C^{(1)}$		± 1	± 5	$\mu V/^\circ C$
		$T_A = -40^\circ C$ to $+125^\circ C^{(1)}$		± 1.2	± 6	
PSRR	Power supply rejection ratio	$V_{CM} = (V-) - 0.1V$			40	$\mu V/V$
INPUT BIAS CURRENT						
I_B	Input bias current	$T_A = 25^\circ C^{(1)}$		± 0.01	10	pA
		$T_A = -40^\circ C$ to $+125^\circ C^{(1)}$		± 3.78		
I_{OS}	Input offset current	$T_A = 25^\circ C^{(1)}$		± 0.01	10	pA
		$T_A = -40^\circ C$ to $+125^\circ C^{(1)}$		± 1.00		
NOISE						
	Input voltage noise	$f = 0.1Hz$ to $10Hz, V_{CM} = (V-)$		0.91		μV_{RMS}
				6.0		μV_{PP}
e_n	Input voltage noise density	$f = 10Hz$		130		nV/\sqrt{Hz}
		$f = 1kHz$		60		
		$f = 10kHz$		55		
i_n	Input current noise density	$f = 1kHz$		30		fA/\sqrt{Hz}
INPUT VOLTAGE						
V_{CM}	Common-mode voltage	$T_A = -40^\circ C$ to $+125^\circ C^{(1)}$		$(V-) - 0.1V$	$(V+) + 0.1V$	V
CMRR	Common-mode rejection ratio	$(V-) - 0.1V \leq V_{CM} \leq (V+) - 1.5V$		89	100	dB
			$(V-) - 0.1V \leq V_{CM} \leq (V+) - 1.5V, V_S = 5.5V$		100	
		$(V+) - 0.6V \leq V_{CM} \leq (V+) + 0.1V$	$T_A = -40^\circ C$ to $+125^\circ C^{(1)}$	90	100	
					69	
INPUT IMPEDANCE						
Z_{id}	Differential input impedance			$0.1 \parallel 1$		$G\Omega \parallel pF$
Z_{ic}	Common-mode input impedance			$1 \parallel 1$		$T\Omega \parallel pF$

5.7 Electrical Characteristics (continued)

at $V_S = 1.7V$ to $5.5V$, $T_A = 25^\circ C$, and $V_{CM} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$V_S = 5.5V$	$(V^-) + 0.1V < V_O < (V^+) - 0.1V$, $V_{CM} = (V^-) - 100mV$, $R_L = 10k\Omega$	100	121		dB
			$(V^-) + 0.45V < V_O < (V^+) - 0.45V$, $V_{CM} = (V^-) - 100mV$, $R_L = 2k\Omega$	100	121		
		$V_S = 1.7V$	$(V^-) + 0.1V < V_O < (V^+) - 0.1V$, $V_{CM} = (V^+) - 1.5V$, $R_L = 10k\Omega$	90	113		
			$(V^-) + 0.45V < V_O < (V^+) - 0.45V$, $V_{CM} = (V^+) - 1.5V$, $R_L = 2k\Omega$	90	107		
FREQUENCY RESPONSE							
UGB	Unity-gain bandwidth	$G = 1$	$I_{OUT} = 0\mu A$, $R_L = 10k\Omega$		450		kHz
			$I_{OUT} = 0\mu A$, $R_L = 50k\Omega$		0.85		MHz
			$I_{OUT} = 100\mu A$, $R_L = 10k\Omega$		0.75		
GBW	Gain-bandwidth product				1		MHz
SR	Slew rate	$G = -1$, 4V step			1		V/ μs
t_S	Settling time	To 0.1%, $V_S = 5.5V$, $G = 1$, 1V step			8		μs
t_{OR}	Overload recovery time	$V_{IN} \times G = V_S$			15		μs
OUTPUT							
V_O	Voltage output swing from rail	No load				3	mV
		$R_L = 10k\Omega$				10	
		$R_L = 2k\Omega$				40	
		$T_A = -40^\circ C$ to $+125^\circ C$, both rails, $R_L = 10k\Omega^{(1)}$				10	
I_{SC}	Short-circuit current	$V_S = 5.5V$			60		mA
Z_O	Open-loop output impedance	$f = 1MHz$, no load			1.6		$k\Omega$
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$V_{CM} = (V^+) - 1.5V$			23.5	30	μA
			$T_A = -40^\circ C$ to $+125^\circ C^{(1)}$				

(1) Specification established from device population bench system measurements across multiple lots.

5.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{pF}$ (unless otherwise noted)

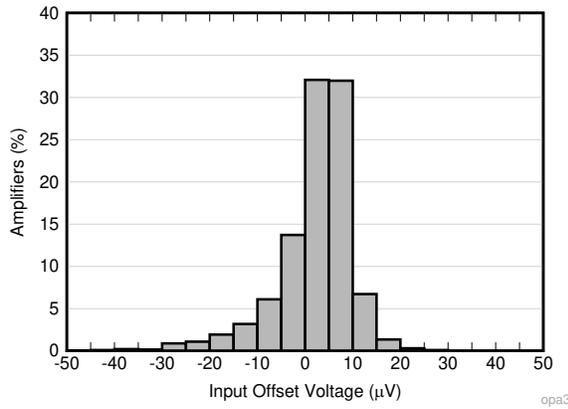


Figure 5-1. Offset Voltage Distribution

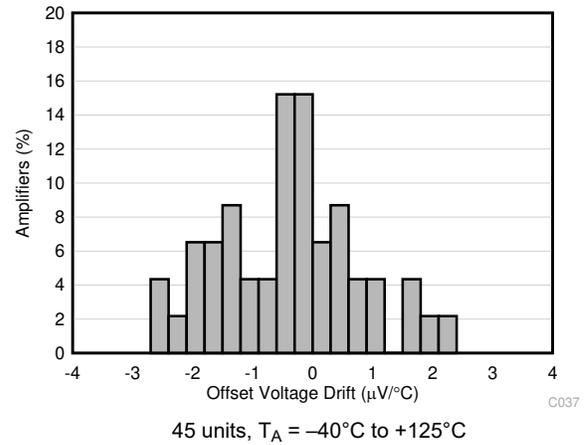


Figure 5-2. Offset Voltage Drift Distribution

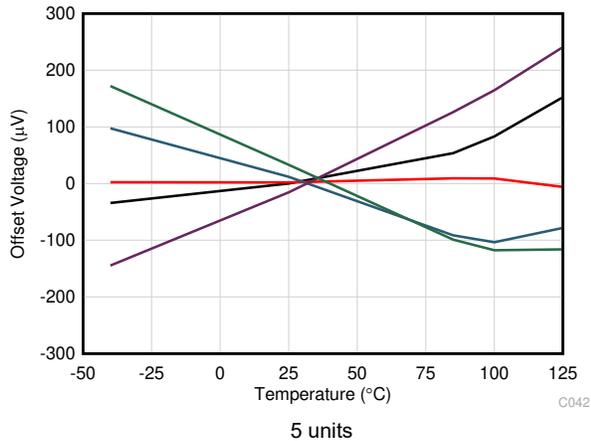


Figure 5-3. Offset Voltage vs Temperature

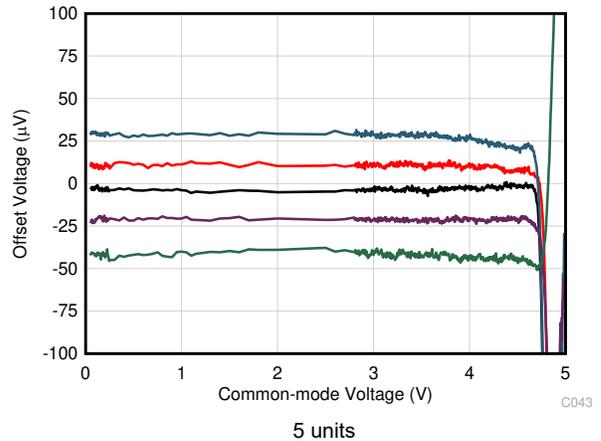


Figure 5-4. Offset Voltage vs Common-Mode Voltage

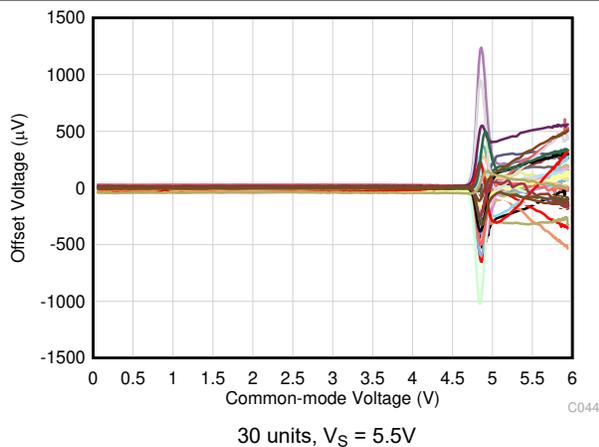


Figure 5-5. Offset Voltage vs Common-Mode Voltage

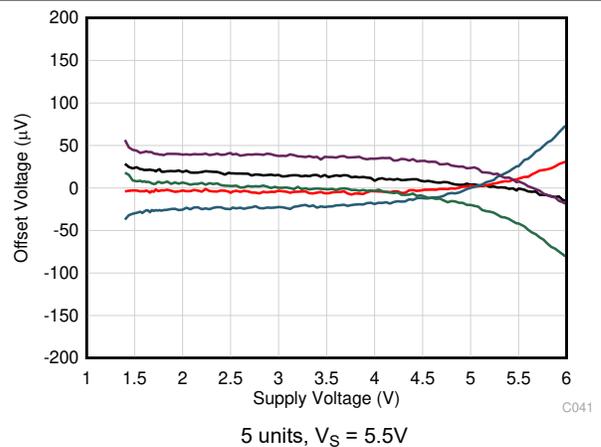


Figure 5-6. Offset Voltage vs Supply Voltage

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{pF}$ (unless otherwise noted)

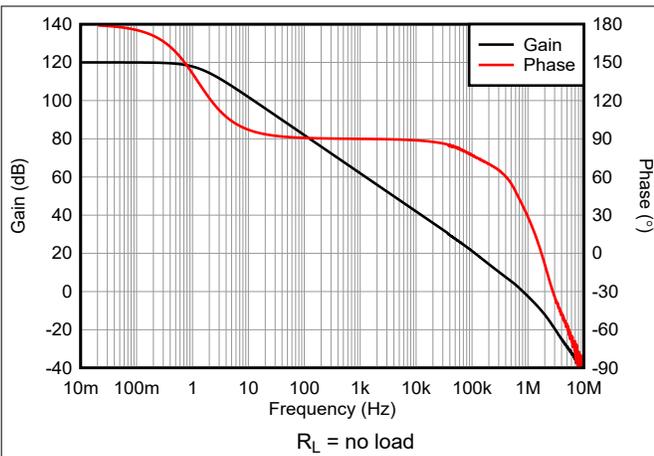


Figure 5-7. Open-Loop Gain and Phase vs Frequency

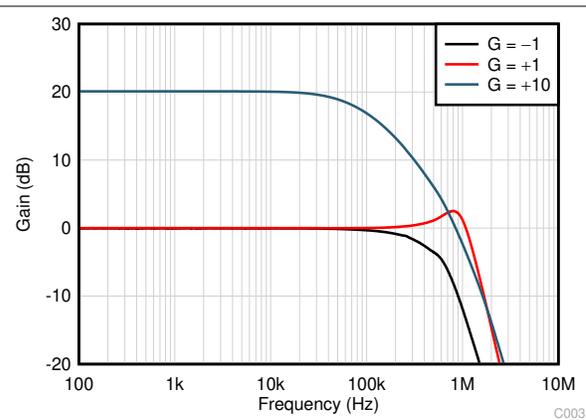


Figure 5-8. Closed-Loop Gain and Phase vs Frequency

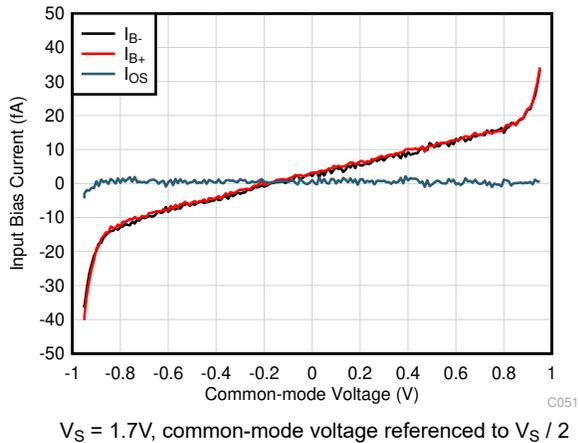


Figure 5-9. Input Bias Current vs Common-Mode Voltage

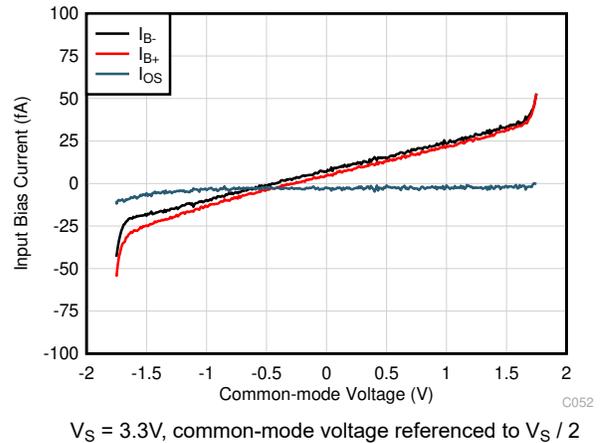


Figure 5-10. Input Bias Current vs Common-Mode Voltage

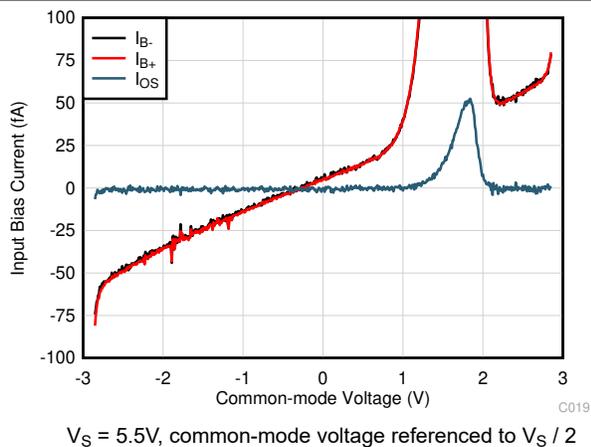


Figure 5-11. Input Bias Current vs Common-Mode Voltage

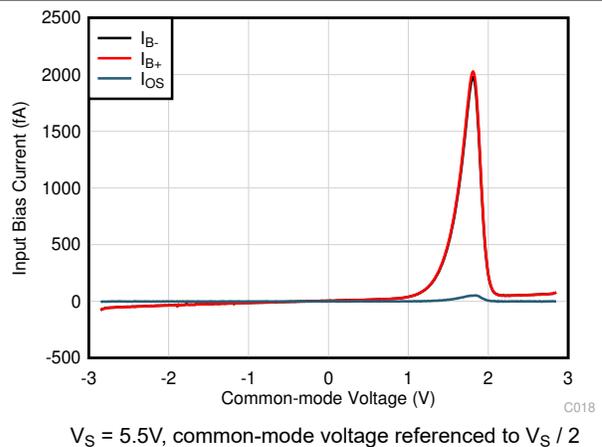


Figure 5-12. Input Bias Current vs Common-Mode Voltage

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{pF}$ (unless otherwise noted)

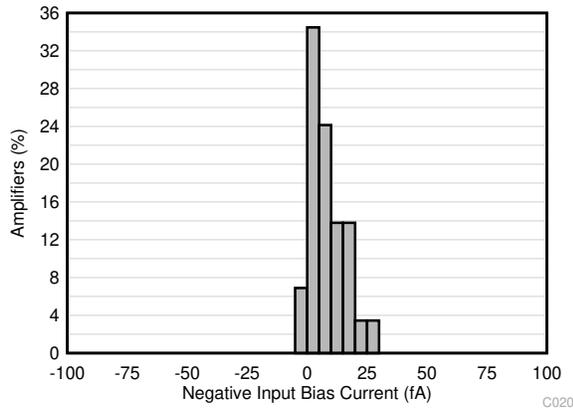


Figure 5-13. Negative Input Bias Current Distribution

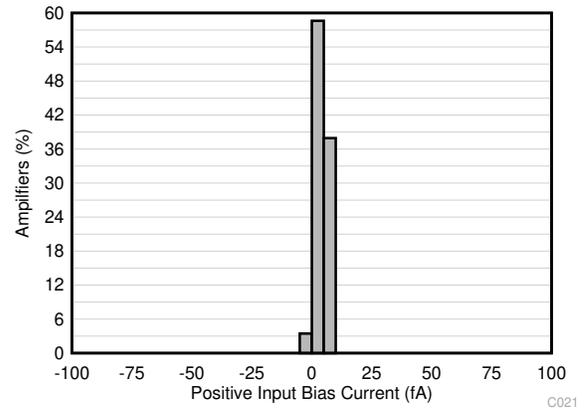


Figure 5-14. Positive Input Bias Current Distribution

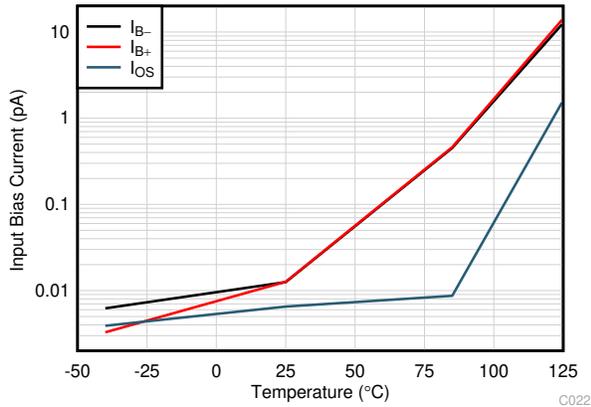


Figure 5-15. Input Bias Current vs Temperature

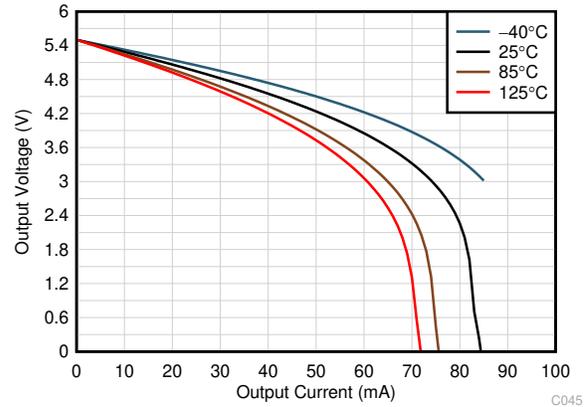


Figure 5-16. Output Voltage Swing vs Output Current (Maximum Supply)

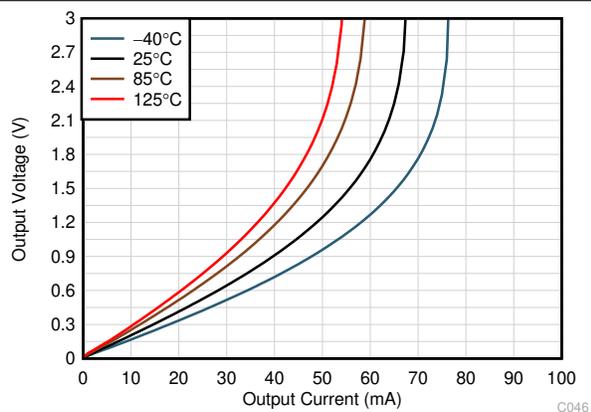


Figure 5-17. Output Voltage Swing vs Output Current (Maximum Supply)

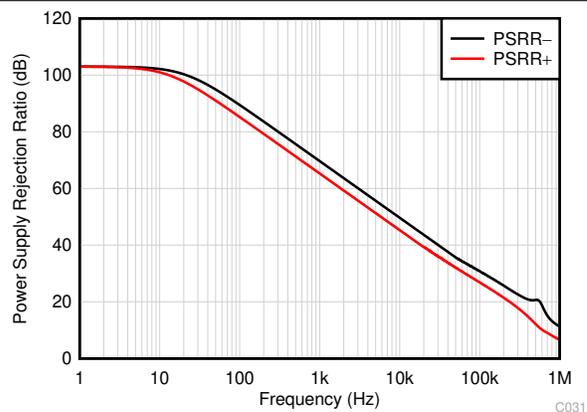
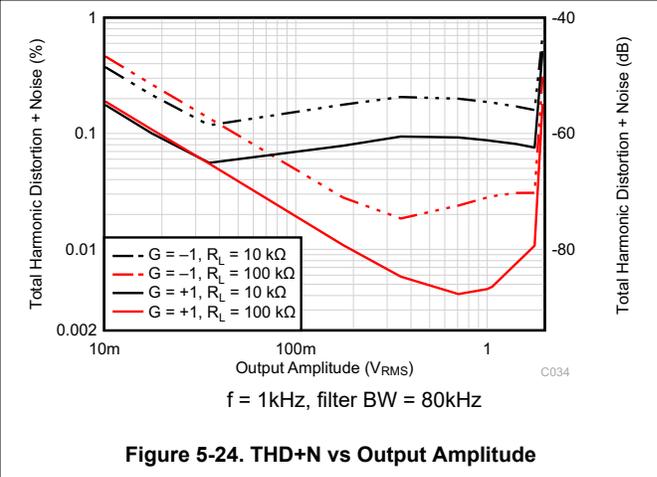
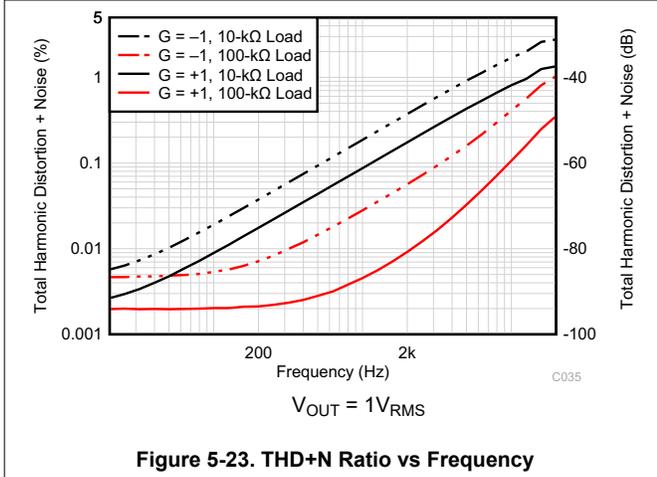
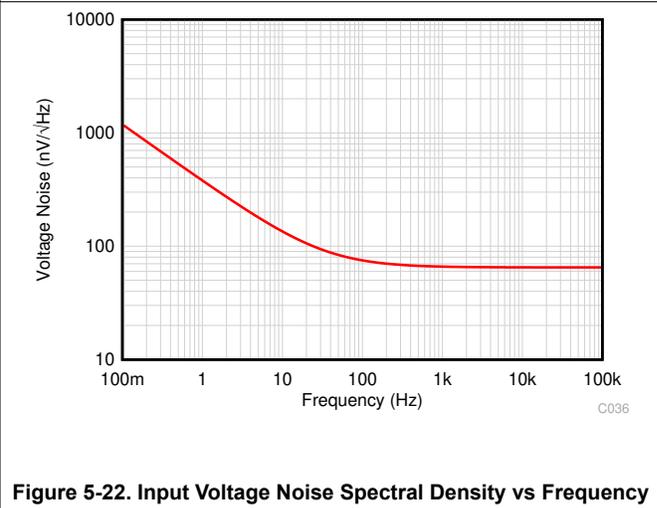
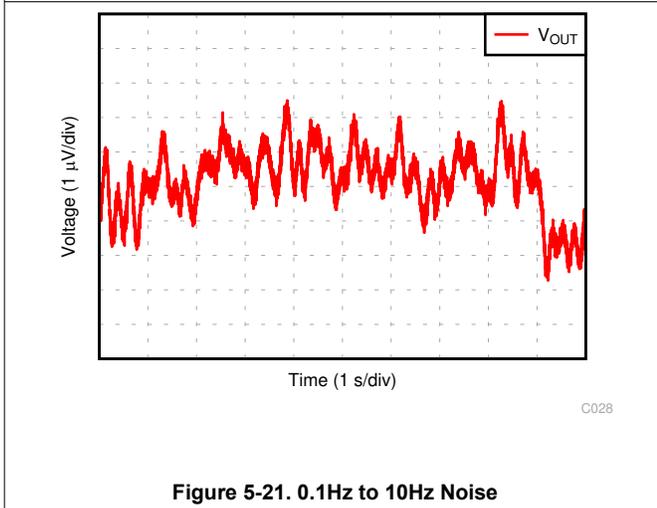
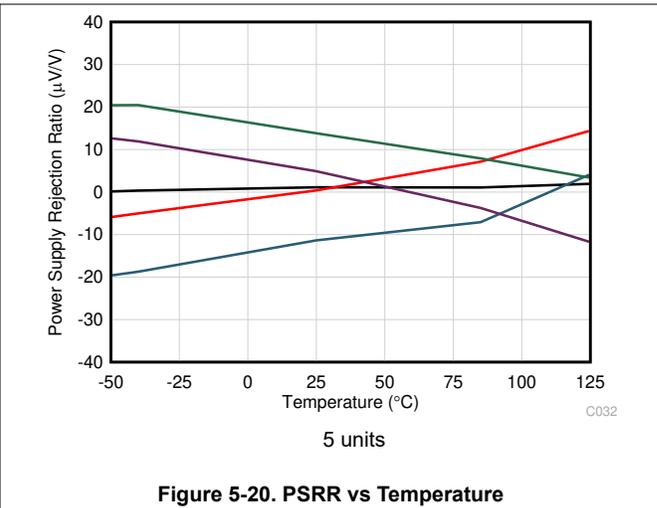
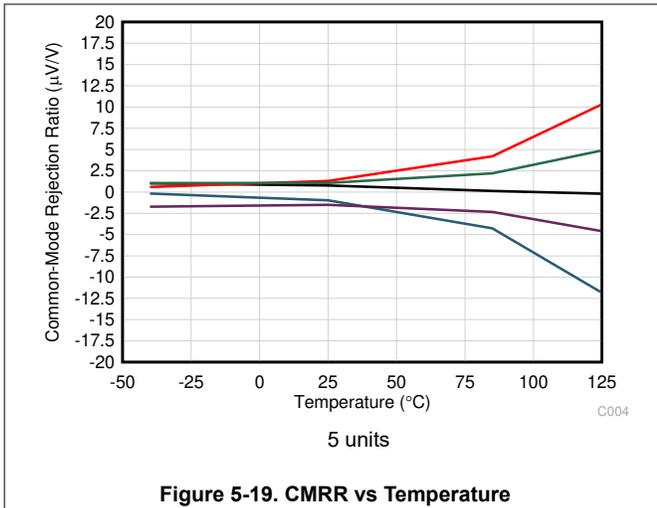


Figure 5-18. PSRR vs Frequency

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{pF}$ (unless otherwise noted)



5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{pF}$ (unless otherwise noted)

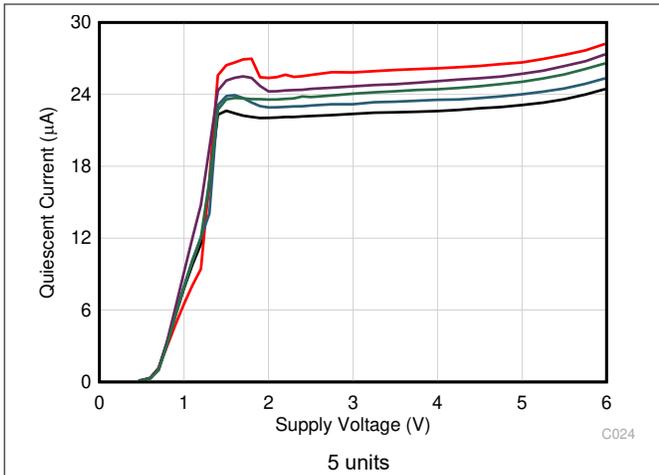


Figure 5-25. Quiescent Current vs Supply Voltage

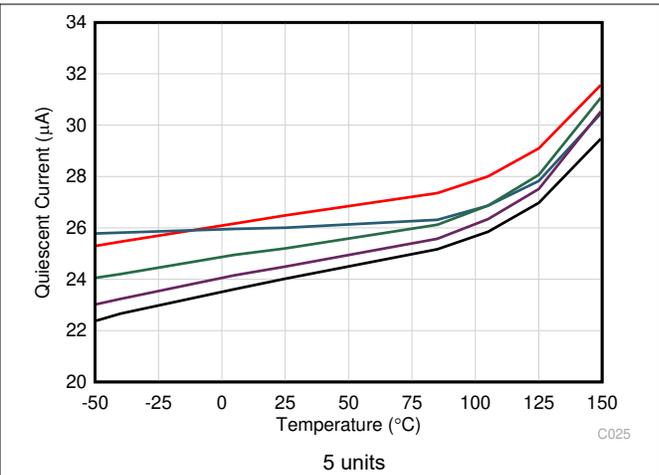


Figure 5-26. Quiescent Current vs Temperature

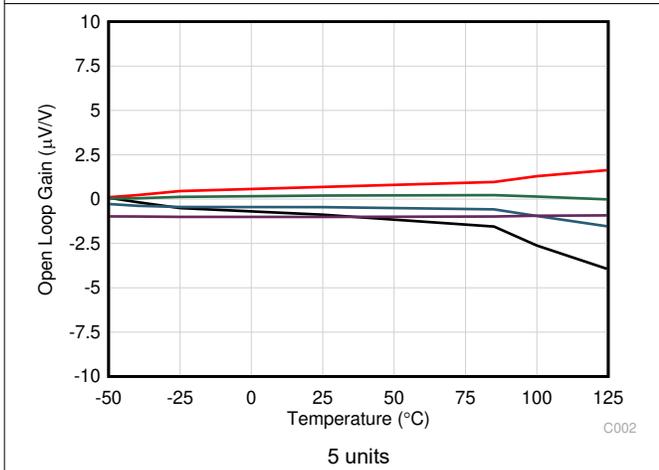


Figure 5-27. Open-Loop Gain vs Temperature

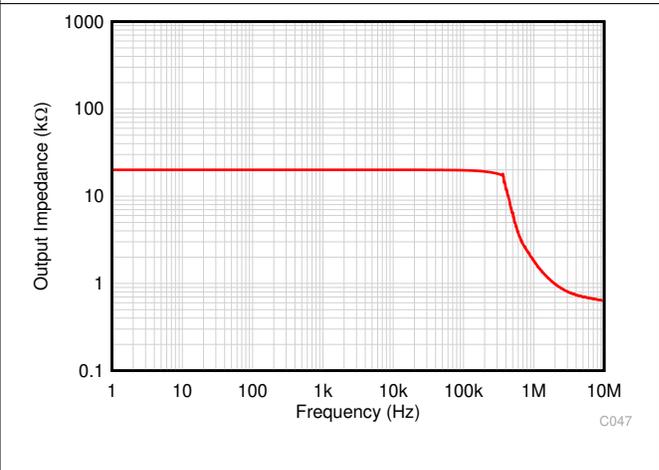


Figure 5-28. Open-Loop Output Impedance vs Frequency

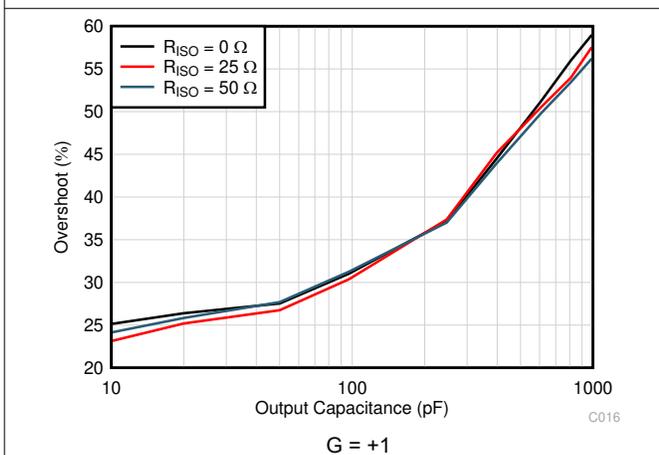


Figure 5-29. Small-Signal Overshoot vs Capacitive Load (10mV Step)

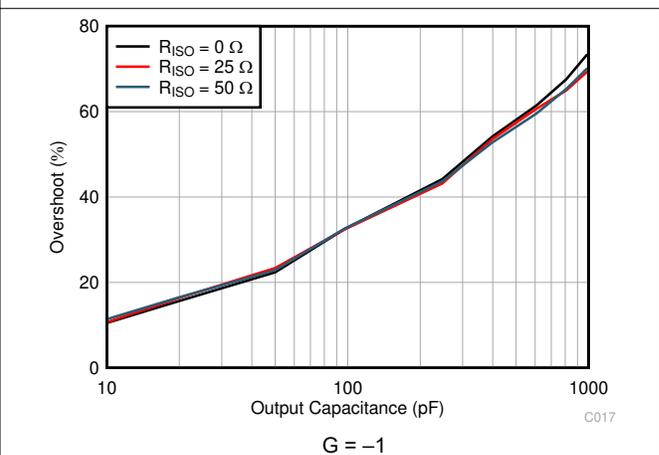
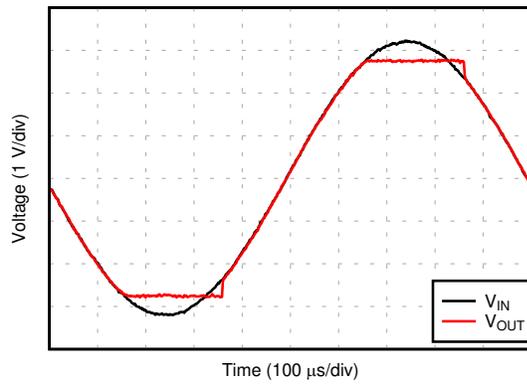


Figure 5-30. Small-Signal Overshoot vs Capacitive Load (10mV Step)

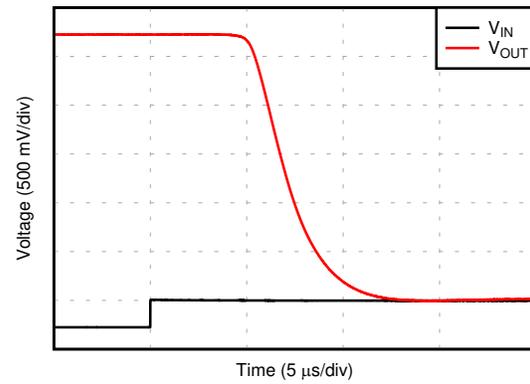
5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{pF}$ (unless otherwise noted)



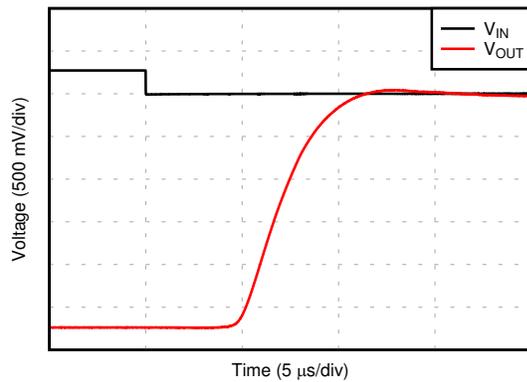
C029

Figure 5-31. No Phase Reversal



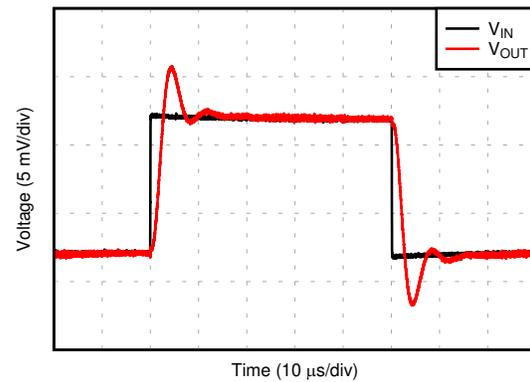
C048

Figure 5-32. Positive Overload Recovery



C027

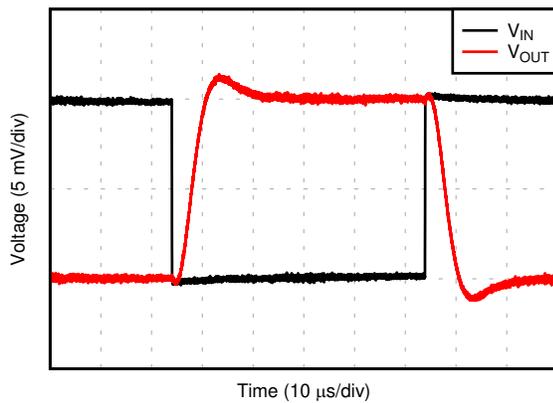
Figure 5-33. Negative Overload Recovery



C015

$G = +1$

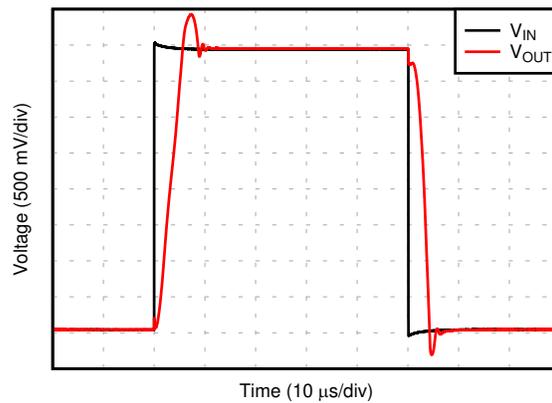
Figure 5-34. Small-Signal Step Response (10mV Step)



C049

$G = -1$

Figure 5-35. Small-Signal Step Response (10mV Step)



C013

$G = +1$

Figure 5-36. Large-Signal Step Response (4V Step)

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{pF}$ (unless otherwise noted)

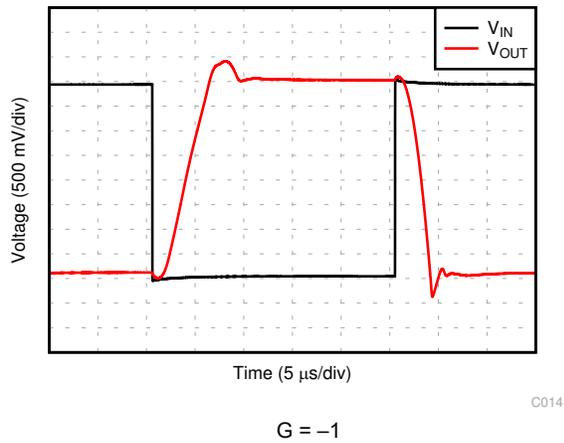


Figure 5-37. Large-Signal Step Response (4V Step)

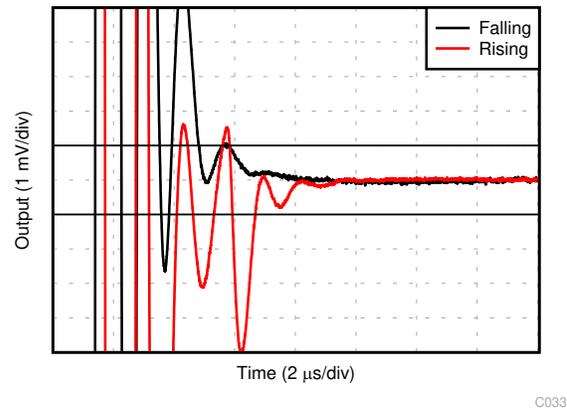


Figure 5-38. Settling Time (1V Positive Step)

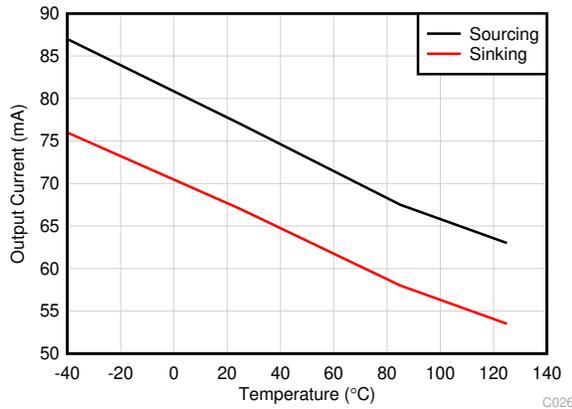


Figure 5-39. Short-Circuit Current vs Temperature

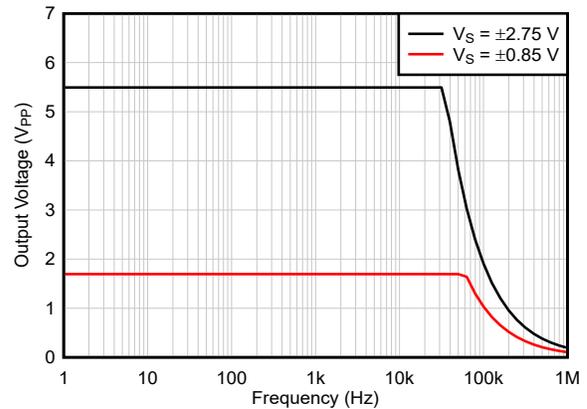


Figure 5-40. Maximum Output Voltage vs Frequency

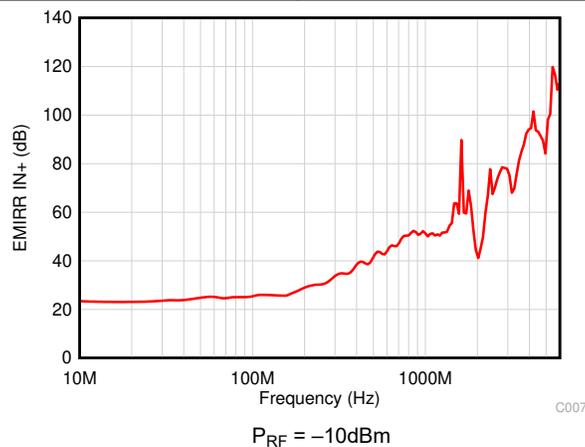


Figure 5-41. EMIRR vs Frequency

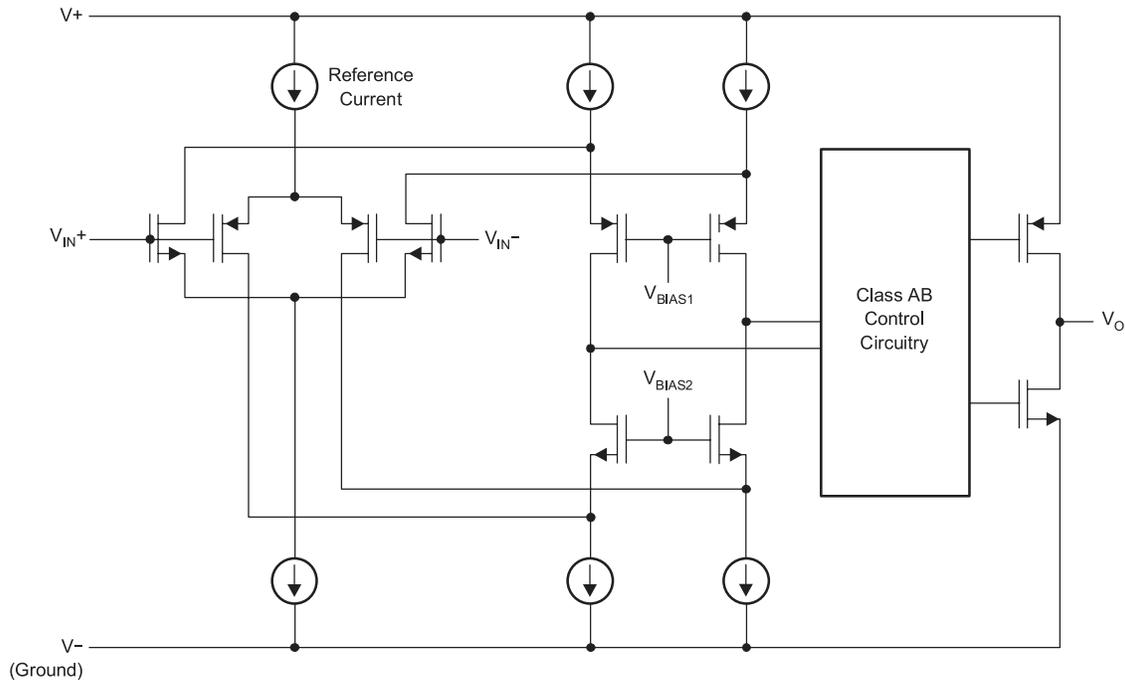
6 Detailed Description

6.1 Overview

The OPAx396 are low-offset, low-power, e-trim operational amplifiers (op amps) that uses a proprietary offset trim technique. These op amps offer ultra-low input offset voltage, drift, and input bias current, while achieving an excellent bandwidth-to-quiescent-current ratio. The OPAx396 operate from 1.7V to 5.5V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications.

The output features an advanced output stage that tolerates high capacitive loading for solid and stable performance. The OPAx396 strengths make these devices an excellent amplifier for high-impedance sensors, where input bias current, offset voltage, and power consumption are critical.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Low Input Bias Current

The OPAx396 achieve very low input bias current as a result of CMOS inputs and advanced electrostatic discharge (ESD) protection circuitry. Input bias current (I_B) is primarily a function of the input protection scheme in CMOS input amplifiers. If careful consideration is not taken with the ESD cells, a CMOS input device can exhibit large input bias currents, especially over temperature. The OPAx396 achieve excellent input bias current ratings of $\pm 30\text{pA}$ maximum at 125°C .

6.3.2 Input Differential Voltage

The OPAx396 do not have any diodes connected between the input nodes, allowing for input voltages anywhere between the supply voltage. The input structure can be seen in [Figure 6-1](#). Although these devices can tolerate any differential input voltage that does not exceed the supply voltage, do not operate continuously at differential input voltages greater than 0.5V .

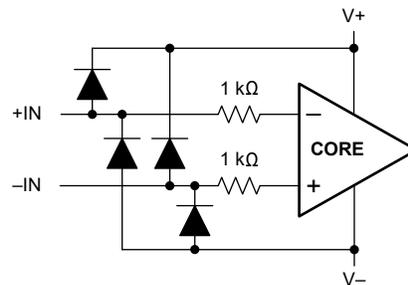


Figure 6-1. Equivalent Input Circuit

6.3.3 Capacitive Load Drive

The OPAx396 feature advanced output drive circuitry that maintain stability even with capacitive loads as high as 1 nF . Many low-quiescent-current amplifiers exhibit poor stability when connected to a capacitive load as a result of the low levels of current used to bias the output stage. The OPAx396 are designed with an output stage that adapts to high capacitive loads without sacrificing additional current consumption. This feature helps produce a highly stable device across all temperature and supply conditions, enabling robust system performance.

6.3.4 EMI Rejection

The OPAx396 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx396 benefit from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz . [Figure 6-2](#) shows the results of this testing on the OPAx396. [Table 6-1](#) lists the EMIRR +IN values for the OPAx396 at particular frequencies commonly encountered in real-world applications. Applications listed in [Table 6-1](#) can be centered on or operated near the particular frequency shown. Detailed information can also be found in the [EMI Rejection Ratio of Operational Amplifiers application note](#), available for download from www.ti.com.

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR +IN, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects because the amplifier does not have sufficient loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Make sure to properly shield and isolate sensitive analog nodes from noisy radio signals, digital clocks, and interfaces.

The EMIRR +IN of the OPAx396 is plotted versus frequency as shown in Figure 6-2. The OPAx396 unity-gain bandwidth is 1MHz. EMIRR performance less than this frequency denotes interfering signals that fall within the op amp bandwidth.

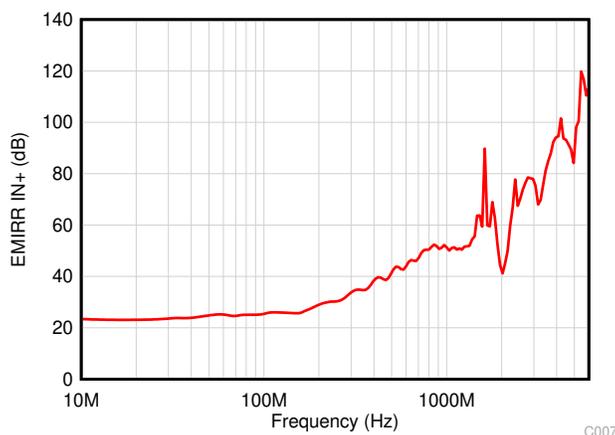


Figure 6-2. EMIRR Testing

Table 6-1. OPAx396 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	39.1dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	46.5dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	61.3dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	69.8dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.5dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	83.6dB

6.4 Device Functional Modes

The OPAx396 have a single functional mode and are operational when the power-supply voltage is greater than 1.7 V (± 0.85 V). The maximum specified power-supply voltage for the OPAx396 is 5.5 V (± 2.75 V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx396 are unity-gain stable, precision operational amplifier free from unexpected output and phase reversal. The OPAx396 are optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100mV beyond the supplies and can tolerate the full supply voltage across the input. The OPAx396 precision amplifier is designed for sensor amplification, low-power analog signal chain applications in low or high gains, as well as a low-power discrete MOSFET or bipolar driver.

7.2 Typical Applications

7.2.1 Three-Terminal CO Gas Sensor

Figure 7-1 shows a simple micropower potentiostat circuit for use with three-terminal unbiased CO sensors. This same design is applicable to many other type of three-terminal gas sensors or electrochemical cells. The basic sensor has three electrodes: the sense or working electrode (WE), counter electrode (CE), and reference electrode (RE). A current flows between CE and WE proportional to the detected concentration. The RE monitors the potential of the internal reference point. For an unbiased sensor, the WE and RE must be maintained at the same potential by adjusting the bias on CE. Through the potentiostat circuit formed by U1, the servo feedback action maintains the RE pin at a potential set by V_{REF} . R1 maintains stability as a result of the large capacitance of the sensor. C1 and R2 form the potentiostat integrator and set the feedback time constant. U2 forms a transimpedance amplifier (TIA) to convert the resulting sensor current into a proportional voltage. Equation 1 calculates the transimpedance gain, and resulting sensitivity, using R_F :

$$V_{TIA} = (-I \times R_F) + V_{REF} \quad (1)$$

R_{Load} is a load resistor with a value that is normally specified by the sensor manufacturer (typically, 10Ω). The potential at WE is set by the applied V_{REF} .

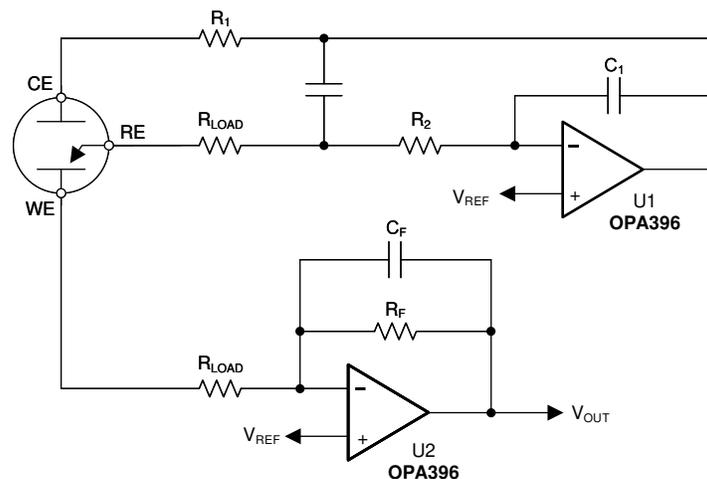


Figure 7-1. Three-Terminal CO Gas Sensor

7.2.1.1 Design Requirements

For this example, Figure 7-2 shows an electrical model of a CO sensor is used to simulate the sensor performance. The simulation is designed to model a CO sensor with a sensitivity of 69nA/ppm. The supply voltage and maximum analog-to-digital converter (ADC) input voltage is 2.5V, and the maximum concentration is 300ppm.

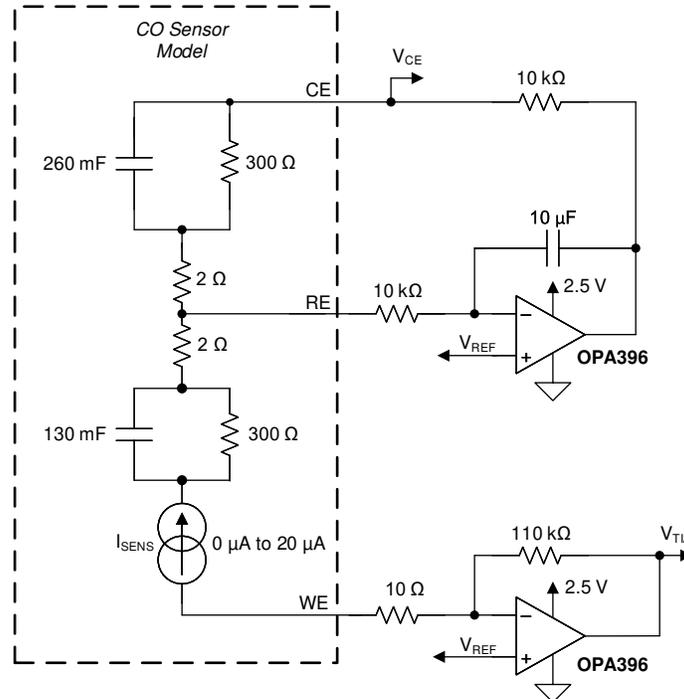


Figure 7-2. CO Sensor Simulation Schematic

7.2.1.2 Detailed Design Procedure

First, determine the V_{REF} voltage. This voltage is a compromise between maximum headroom and resolution, as well as allowance for the minimum swing on the CE terminal because the CE terminal generally goes negative in relation to the RE potential as the concentration (sensor current) increases. Bench measurements found the difference between CE and RE to be 180mV at 300ppm for this particular sensor. To allow for negative CE swing, footroom, and voltage drop across the 10kΩ resistor, 300mV is chosen for V_{REF} .

$$V_{ZERO} = V_{REF} = 300\text{mV} \quad (2)$$

where

- V_{REF} is the reference voltage (300mV).
- V_{ZERO} is the concentration voltage (300mV).

Next, calculate the maximum sensor current at highest expected concentration:

$$I_{SENSMAX} = I_{PERPPM} \times \text{ppmMAX} = 69\text{nA} \times 300\text{ppm} = 20.7\mu\text{A} \quad (3)$$

where

- $I_{SENSMAX}$ is the maximum expected sensor current.
- I_{PERPPM} is the manufacturer specified sensor current in amperes per ppm.
- ppmMAX is the maximum required ppm reading.

Then, find the available output swing range greater than the reference voltage available for the measurement:

$$V_{\text{SWING}} = V_{\text{OUTMAX}} - V_{\text{ZERO}} = 2.5\text{V} - 0.3\text{V} = 2.2\text{V} \tag{4}$$

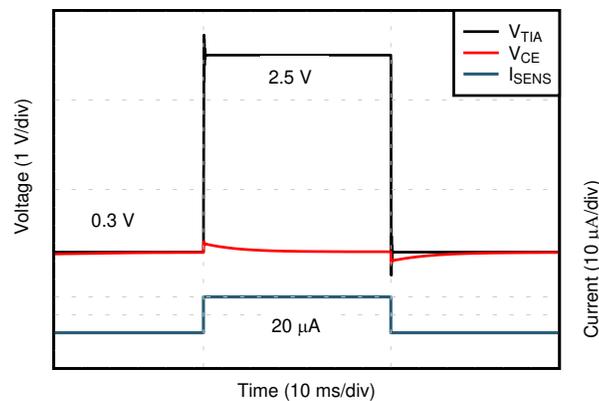
where

- V_{SWING} is the expected change in output voltage.
- V_{OUTMAX} is the maximum amplifier output swing.

Finally, calculate the transimpedance resistor (R_F) value using the maximum swing and the maximum sensor current:

$$R_F = \frac{V_{\text{SWING}}}{I_{\text{SENSMAX}}} = \frac{2.2\text{V}}{20.7\mu\text{A}} = 106.28\text{k}\Omega \text{ (use } 110\text{k}\Omega \text{ for a common value)} \tag{5}$$

7.2.1.3 Application Curve



C012

Figure 7-3. Sensor Transient Response to Simulated 300ppm CO Exposure

7.2.2 4mA to 20mA Loop Design

Factory automation systems commonly use the 4mA to 20mA (4-20mA) communication protocol to enable process automation. In typical 2-wire, 4mA to 20mA loop applications, power to the remote transmitter is limited to less than 4mA total consumption. As a result of the power limitations, low power consumption is essential. The OPAx396 solves many design challenges in 4mA to 20mA loop applications, where low power, high accuracy, and high bandwidth are required.

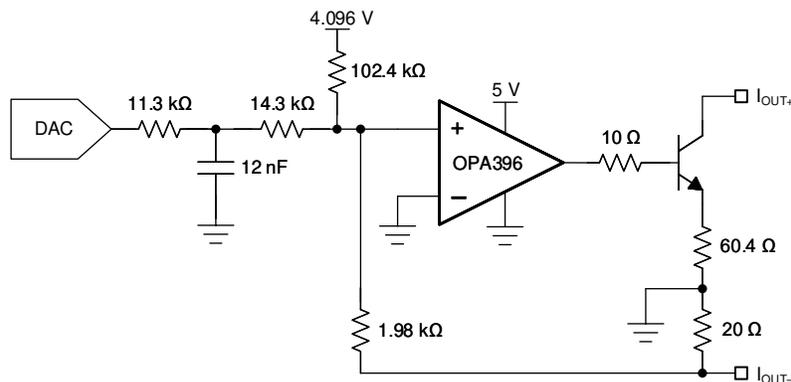


Figure 7-4. 4-20mA Loop Interface Schematic

7.2.2.1 Design Requirements

Table 7-1. Design Parameters

PARAMETER	VALUE
Total current consumption	< 100µA
DAC control voltage	0V to 4.096V
Output current	4mA to 20mA

7.2.2.2 Application Curve

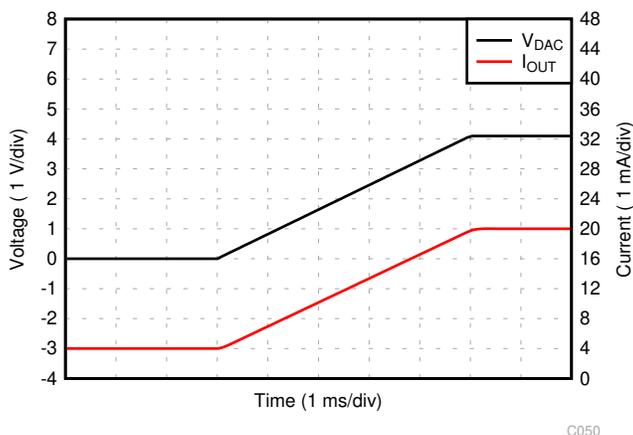


Figure 7-5. 4mA to 20mA Loop Response

7.3 Power Supply Recommendations

The OPAx396 devices are specified for operation from 1.7V to 5.5V (± 0.85 V to ± 2.75 V).

7.4 Layout

7.4.1 Layout Guidelines

Paying attention to good layout practice is always recommended:

- Keep traces short.
- When possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close as possible to the device pins.
- Place a 0.1 μ F capacitor closely across the supply pins.

These guidelines must be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

7.4.2 Layout Example

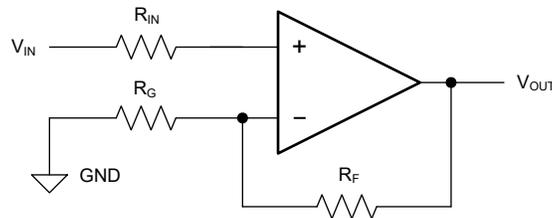


Figure 7-6. Schematic Representation

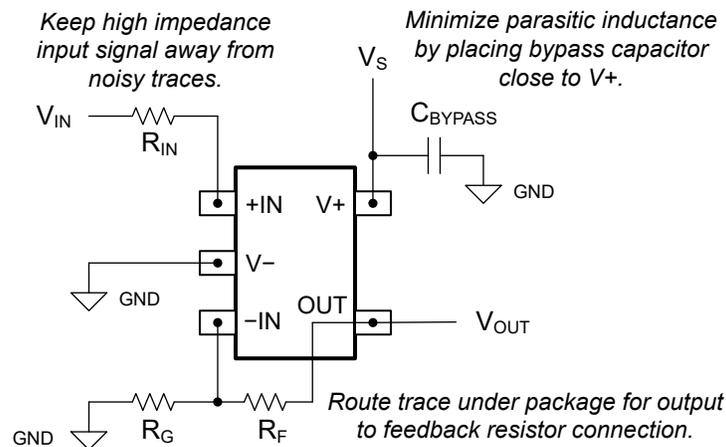


Figure 7-7. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design and simulation tools](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter With HART Modem reference design](#)
- Texas Instruments, [Micropower Electrochemical Gas Sensor Amplifier reference design](#)
- Texas Instruments, [Compensate Transimpedance Amplifiers Intuitively application report](#)
- Texas Instruments, [Designing With pH Electrodes application report](#)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision * (July 2021) to Revision A (March 2026)	Page
• Added OPA2396DGKR and OPA4396PWR to the data sheet.....	1
• Added pinout information for OPA2396 and OPA4396 in <i>Pin Configuration and Function</i> section.....	3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2396DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3BPS
OPA396DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1JJ
OPA396DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1JJ
OPA396DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1JJ
OPA396DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1JJ
OPA396DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1JJ
OPA396DCKT.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1JJ
OPA4396PWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4396

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

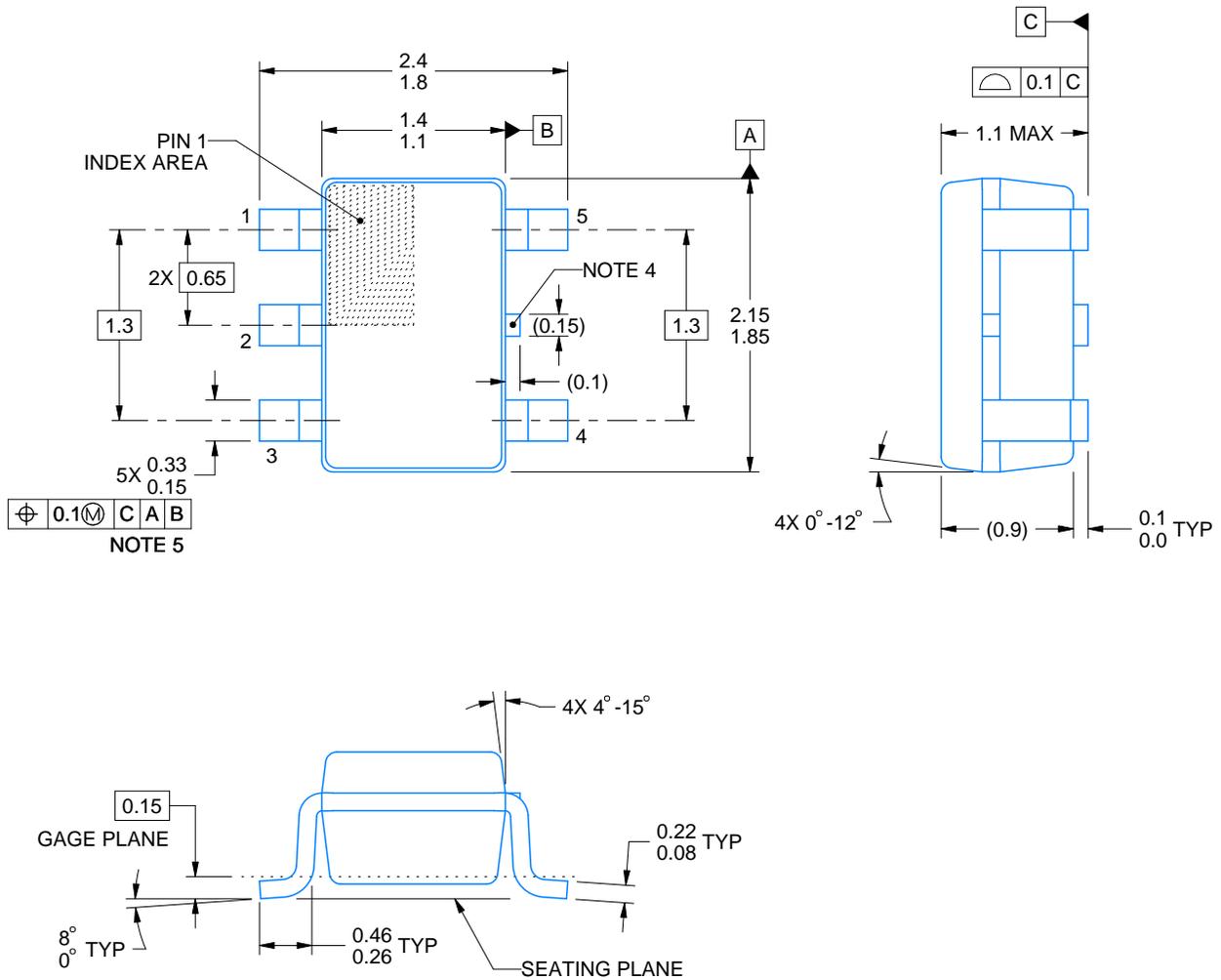

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2396DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA396DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA396DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA396DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4396PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2396DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA396DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA396DCKRG4	SC70	DCK	5	3000	190.0	190.0	30.0
OPA396DCKT	SC70	DCK	5	250	190.0	190.0	30.0
OPA4396PWR	TSSOP	PW	14	3000	353.0	353.0	32.0



4214834/G 11/2024

NOTES:

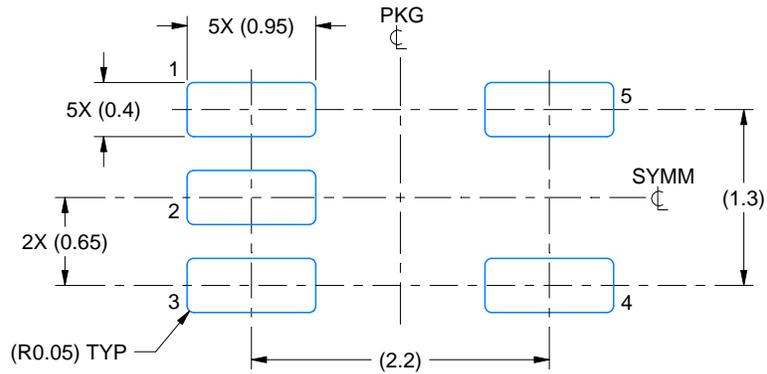
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

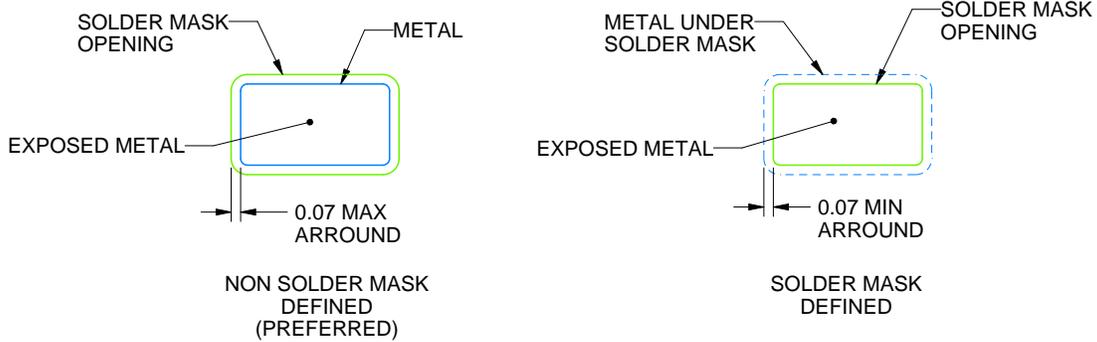
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

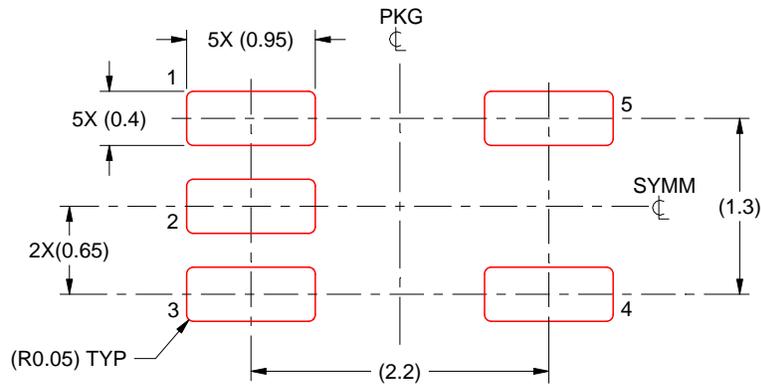
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

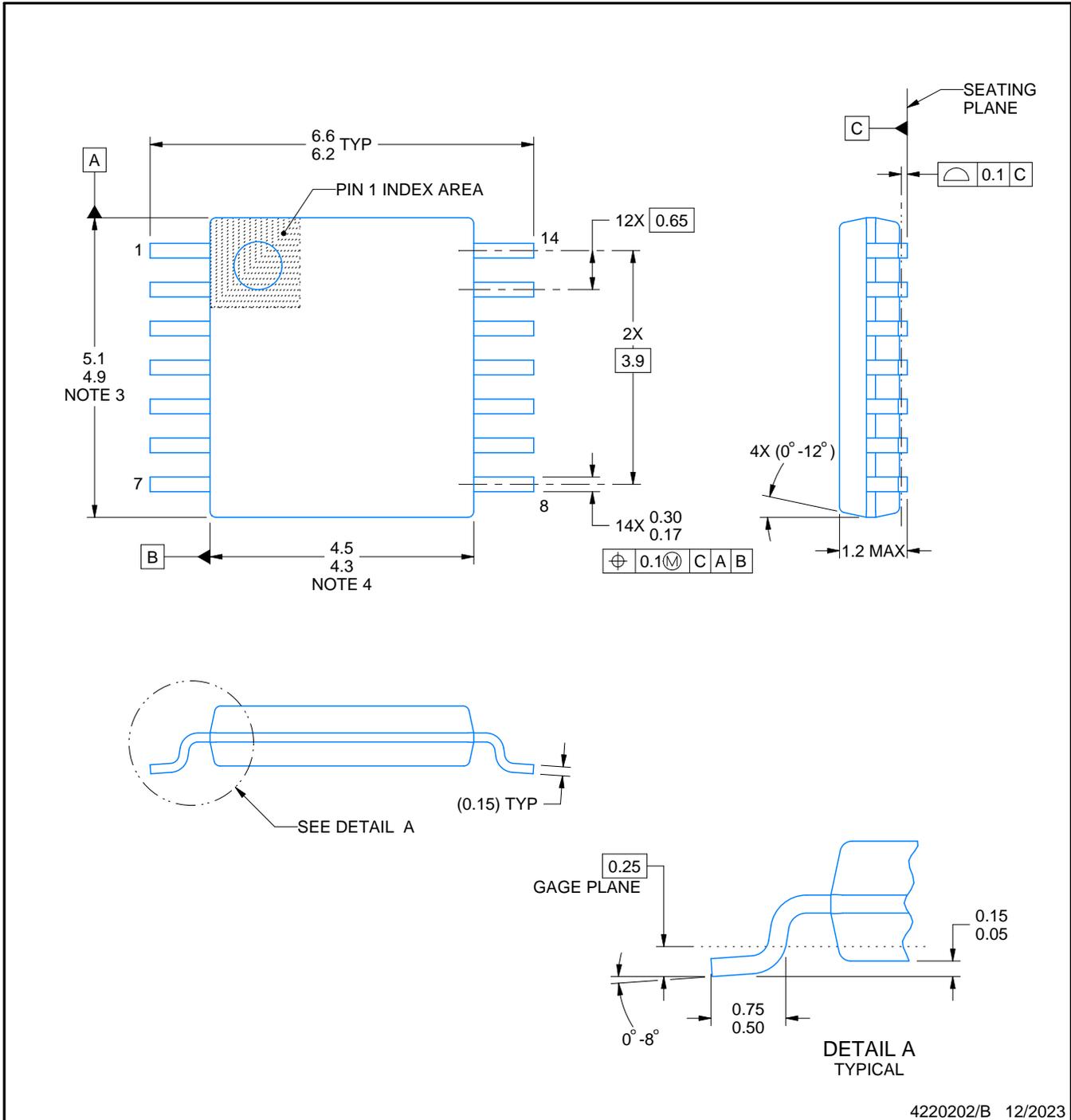
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

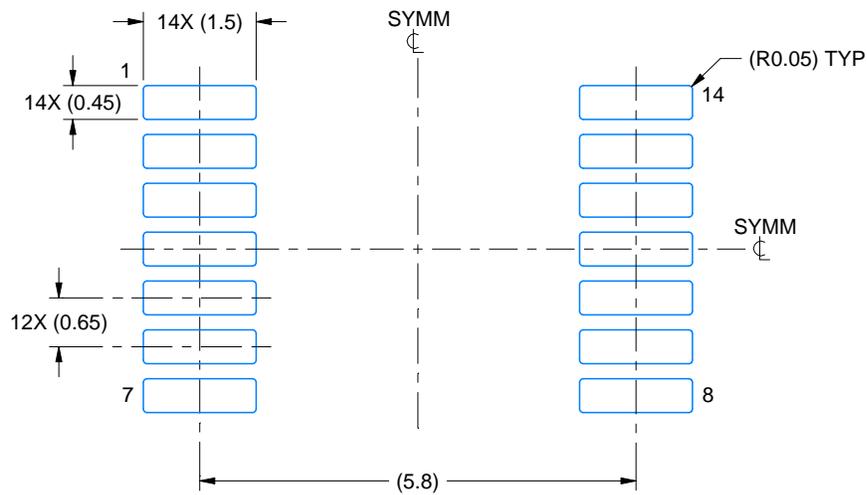
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

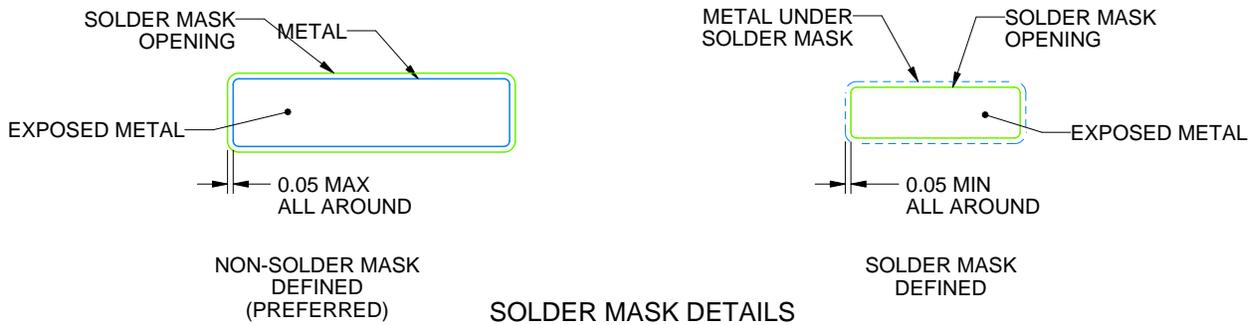
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

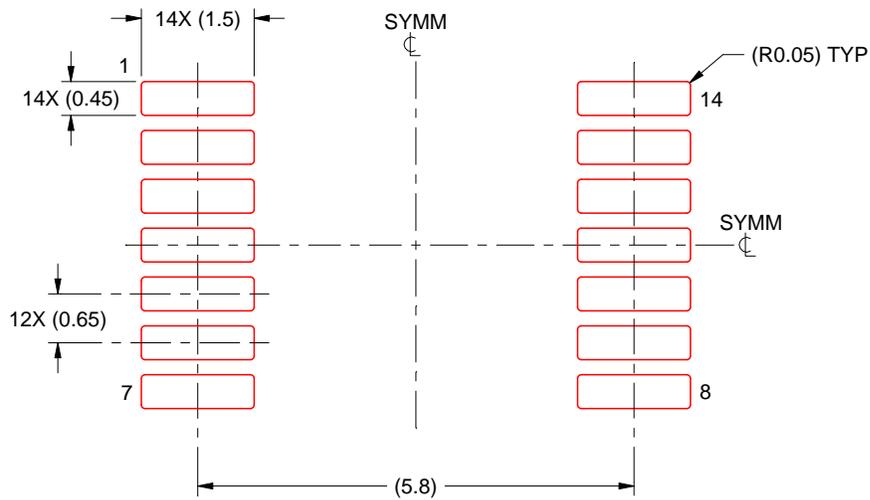
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

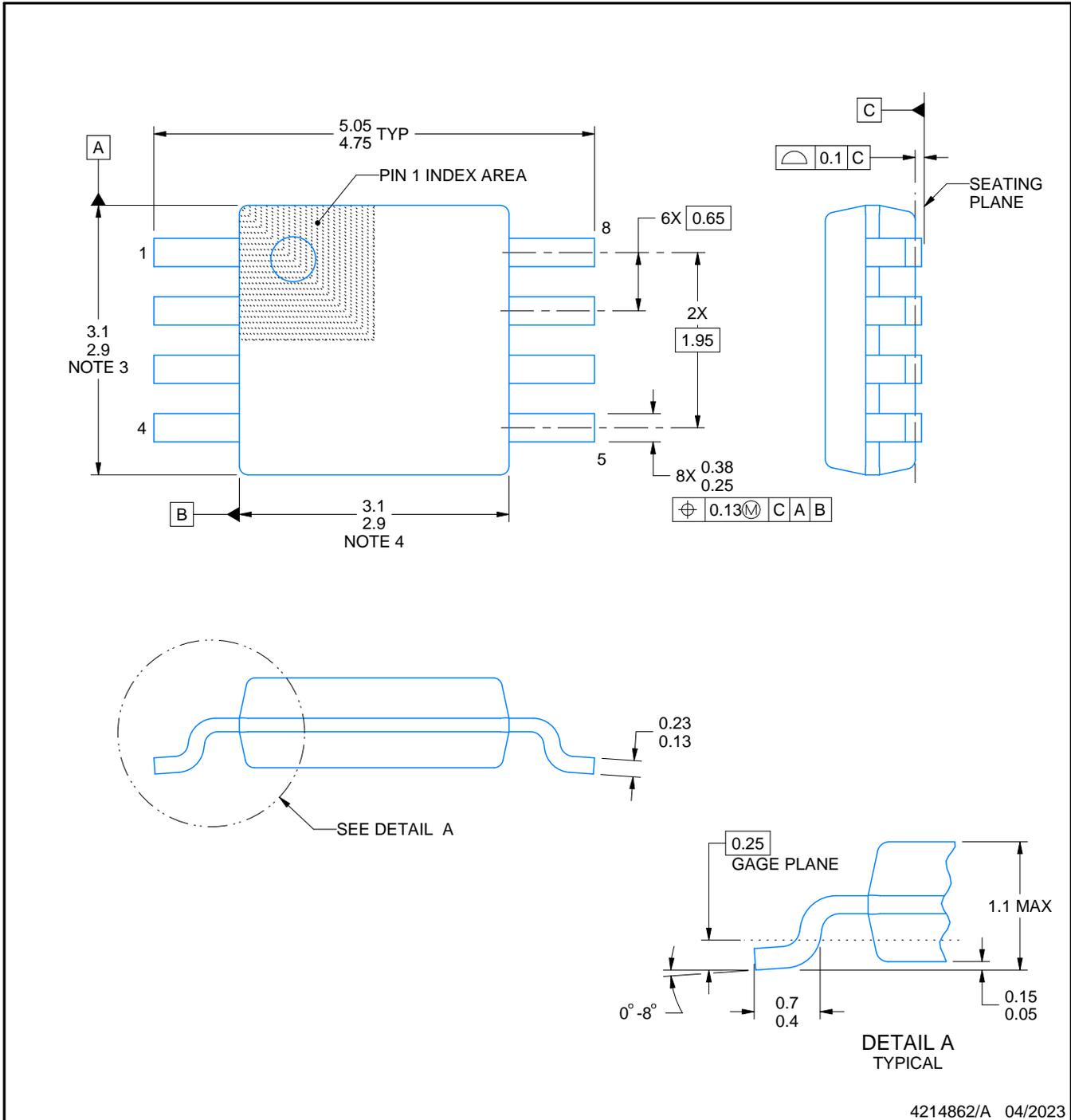
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

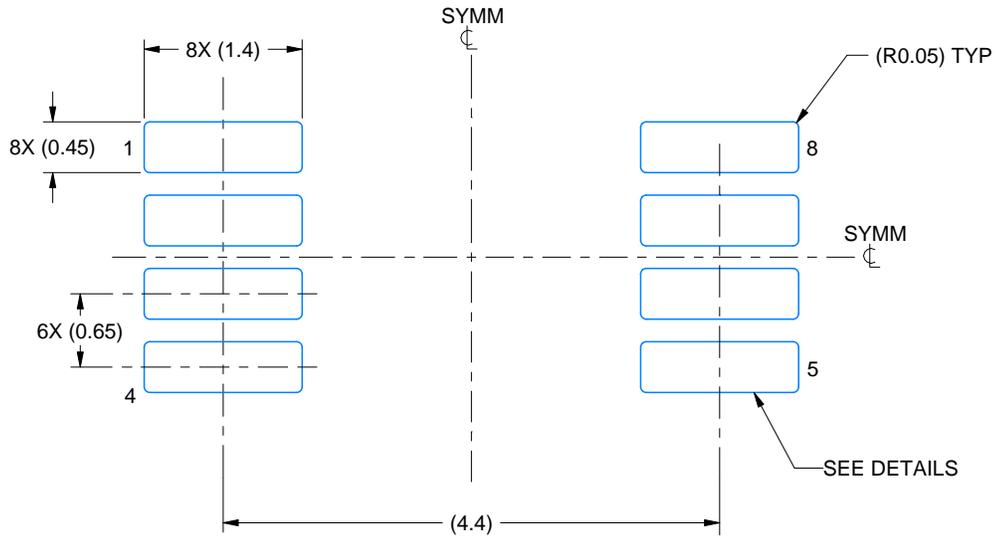
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

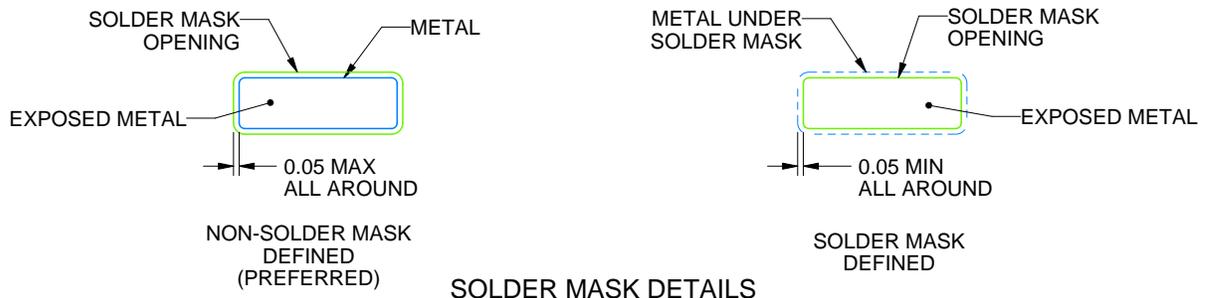
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

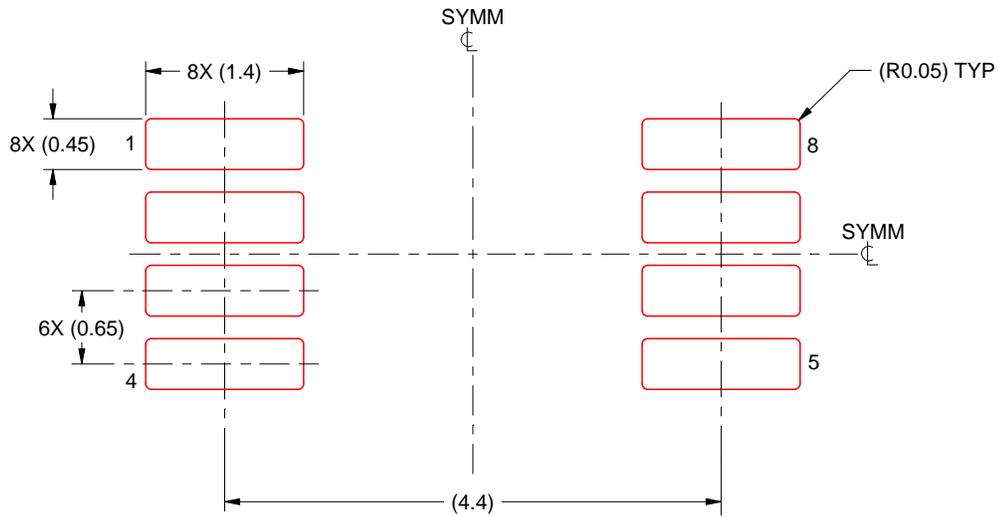
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025