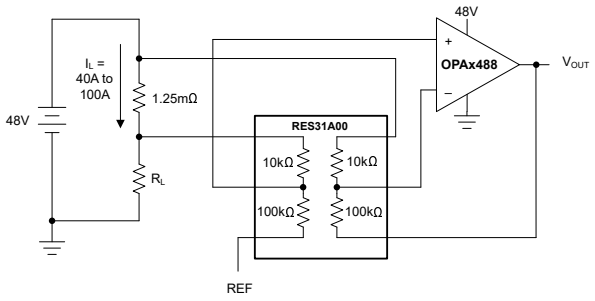
OPAx488 Low-Noise, Zero-Drift, Wide-Bandwidth, Mux-Friendly Operational Amplifiers

1 Features

- Supply range: 4.5V to 48V
- High dc precision:
  - Zero drift: 0.025µV/°C, max
  - Low offset voltage: 7.5µV, max
  - High PSRR: 140dB, min
  - High CMRR: 140dB, min
- Excellent ac performance:
  - Gain bandwidth: 14MHz
  - Slew rate: 40V/µs
  - Low broadband noise: 7.5nV/$\sqrt{Hz}$
  - Near zero flicker noise: 160nV$_{PP}$
- Input includes the negative rail
- Low quiescent current: 1.5mA
- Thermal shutdown
- Latch-up protection
- Temperature: –40°C to +125°C

2 Applications

- Battery test equipment
- Weigh scale
- Analog input module
- Pressure transmitter
- Programmable DC power supply
- Semiconductor test



High-Side Current Shunt Monitor Application

3 Description

The OPA488, OPA2488, and OPA4488 (OPAx488) are 48V, wide-bandwidth, low noise, zero-drift operational amplifiers (op amps). The OPAx488 provides a pin compatible replacement to many industry standard amplifiers that can benefit from a higher operating voltage. The 48V operating voltage and the 60V absolute maximum enable robust circuit designs.

These op amps feature only 7.5µV of offset voltage (max) and 0.025µV/°C of offset voltage drift (max) over a wide temperature range. The OPAx488 feature very fast settling time due in part to the wide gain bandwidth and very high slew rate. The settling time is further enhanced in multichannel systems by the proprietary MUX-friendly input architecture.

The combination of high precision, fast settling, and low noise make the OPAx488 an excellent choice for a wide range of applications, including signal measurement, precision instrumentation, and data acquisition.

The OPAx488 are available in industry standard packages as well as micro-size packages to fit in the most space constrained applications. The devices are specified for operation from –40°C to +125°C.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(2)
OPA488(3)	Single	D (SOIC, 8)	4.90mm × 6.00mm
		DBV (SOT-23, 5)	2.90mm × 2.80mm
		DRL (SOT, 5)	1.60mm × 1.60mm
OPA2488(3)	Dual	D (SOIC, 8)	4.90mm × 6.00mm
		DGK (VSSOP, 8)	3.00mm × 4.90mm
		DSG (WSON, 8)	2.00mm × 2.00mm
OPA488	Quad	D (SOIC, 14)	8.65mm × 6.00mm
		PW (TSSOP-14)	5.00mm × 6.40mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Preview information (not Production Data).

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4 Pin Configuration and Functions

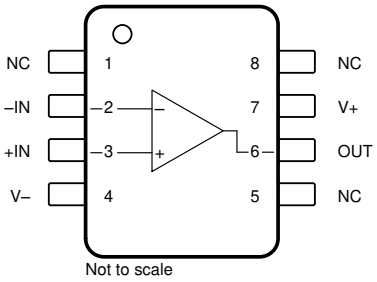


Figure 4-1. OPAx488: D Package, 8-Pin SOIC (Top View)

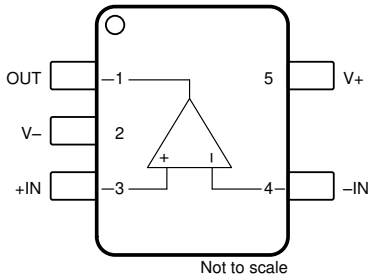


Figure 4-2. OPAx488: DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: OPAx488

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D	DBV		
–IN	2	4	Input	Inverting input
+IN	3	3	Input	Noninverting input
NC	1, 8, 5	–	_	No connection (can be left floating)
OUT	6	1	Output	Output
V–	4	2	Power	Negative (lowest) power supply
V+	7	5	Power	Positive (highest) power supply

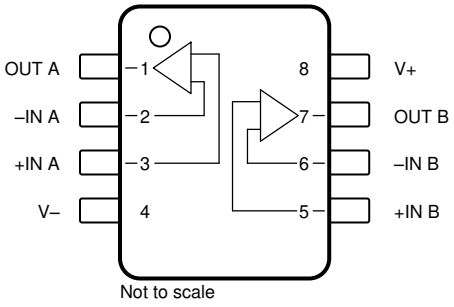


Figure 4-3. OPAx488: D Package, 8-Pin SOIC and DGK Package, 8-pin VSSOP (Top View)

Table 4-2. Pin Functions: OPAx488

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
+IN A	3	Input	Noninverting input channel A
–IN B	6	Input	Inverting input channel B
+IN B	5	Input	Noninverting input channel B
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply

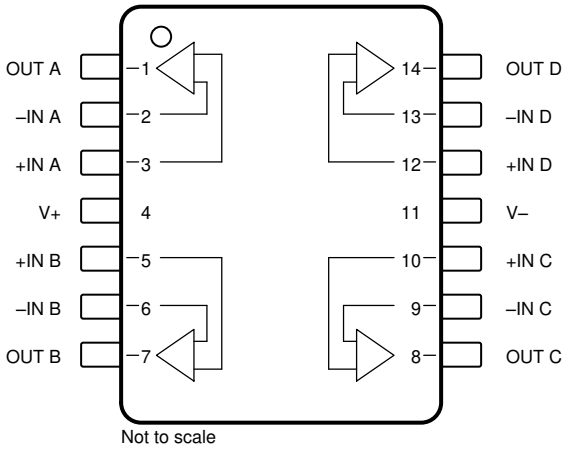


Figure 4-4. OPAx488: D Package, 14-Pin SOIC and PW Package, 14-Pin TSSOP (Top View)

Table 4-3. Pin Functions: OPA4488

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
–IN C	9	Input	Inverting input channel C
–IN D	13	Input	Inverting input channel D
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
+IN C	10	Input	Noninverting input channel C
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V–	11	Power	Negative supply
V+	4	Power	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+)		60	V
	Signal input voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–)	
	Current			±10	mA
	Output short circuit[2]		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
DBV package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	
All other packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+)	4.5		48	V
		Dual-supply, V_S = (V+) – (V–)	±2.25		±24	
T_A	Operating temperature		–40		125	°C

5.4 Thermal Information: OPA488

THERMAL METRIC[1]		OPA488		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	144	197	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82	96	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89	65	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26	33	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	88	64	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: OPA2488

THERMAL METRIC[1]		OPA2488		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132	159	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82	93	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20	3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	81	92	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information: OPA4488

THERMAL METRIC[1]		OPA4488		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95	102	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	37	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	61	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18	9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics

at T_A = 25°C, V_S = 4.5V to 48V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage(1)				±1	±7.5	µV
		T_A = –40°C to +125°C				±10	
dV_{OS}/dT	Input offset voltage drift(1)	T_A = –40°C to +125°C			±0.004	±0.025	µV/°C
PSRR	Power-supply rejection ratio(1)	T_A = –40°C to +125°C			±0.03	±0.1	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±55	±350	pA
		T_A = –40°C to +125°C				±7	nA
I_{OS}	Input offset current(1)				±100	±600	pA
		T_A = –40°C to +125°C				±3	nA
NOISE							
E_n	Input voltage noise	f = 0.1Hz to 10Hz			0.160		μV_{PP}
e_n	Input voltage noise density	f = 10Hz			7.6		$nV/\sqrt{Hz}$
		f = 100Hz			7.6		
		f = 1kHz			7.5		
		f = 10kHz			11.4		
i_n	Input current noise density	f = 1Hz			165		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) – 1.7	V
CMRR	Common-mode rejection ratio	(V–) – 0.1V ≤ V_{CM} ≤ (V+) – 1.7V	V_S = ±2.25V	118	135		dB
			V_S = ±24V	140	150		
		(V–) – 0.1V ≤ V_{CM} ≤ (V+) – 1.7V, T_A = –40°C to +125°C(1)	V_S = ±2.25V	118	130		
			V_S = ±24V	140	150		
INPUT IMPEDANCE							
z_{id}	Differential input impedance				100 || 1.6		MΩ || pF
z_{ic}	Common-mode input impedance				1 || 1.9		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 48V, (V–) + 0.6V < V_O < (V+) – 0.6V, R_{LOAD} = 10kΩ		130	140		dB
			T_A = –40°C to +125°C(1)	130			
		V_S = 48V, (V–) + 1.7V < V_O < (V+) – 1.7V, R_{LOAD} = 2kΩ		130	140		
			T_A = –40°C to +125°C(1)	130			

at T_A = 25°C, V_S = 4.5V to 48V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwith product	Gain = 14V/V			14		MHz
		Gain = 1V/V			11		
SR	Slew rate	Gain = 1, 10V step			40		V/µs
THD+N	Total harmonic distortion + noise	Gain = 1, f = 1kHz, V_O = 3.5V_{RMS}			0.00012%		
	Crosstalk		At dc		120		dB
			f = 10kHz		100		
t_S	Settling time	V_S = 48V, gain = 1, 5V step	To 0.1%		1		µs
			To 0.01%		15		
t_{OR}	Overload recovery time	V_{IN} × gain = V_S = ±24V			300		ns
f_{CH}	Chopping frequency				200		kHz
OUTPUT							
V_O	Voltage output swing from rail	Positive rail, V_S = 48V	No load(1), OPA488, OPA2488			40	mV
			No load(1), OPA4488			50	
			R_{LOAD} = 10kΩ			200	
			R_{LOAD} = 2kΩ			850	
		Negative rail, V_S = 48V	No load(1), OPA488, OPA2488			40	
			No load(1), OPA4488			50	
			R_{LOAD} = 10kΩ			200	
			R_{LOAD} = 2kΩ			850	
I_{SC}	Short-circuit current				±42		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		pF
Z_O	Open-loop output impedance	f = 1MHz			220		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0A			1.5	1.8	mA
			T_A = –40°C to +125°C(1)		1.5	1.9	

(1) Specification established from device population bench system measurements across multiple lots.

5.8 Typical Characteristics

at T_A = 25°C, V_S = 48V, V_{CM} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

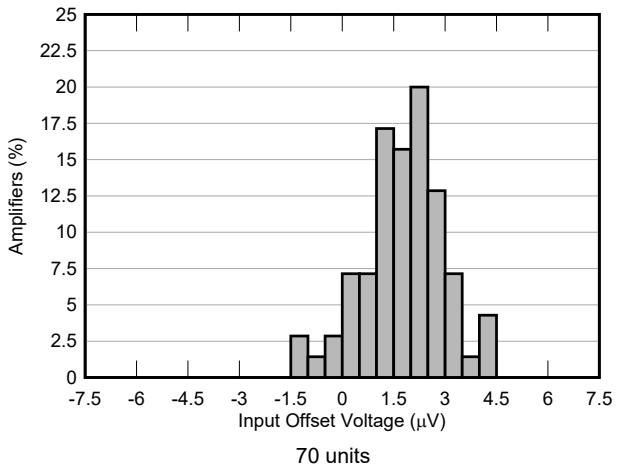


Figure 5-1. Offset Voltage Distribution

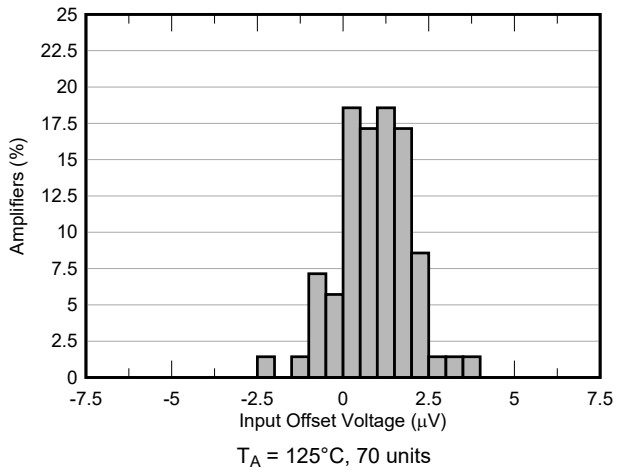


Figure 5-2. Offset Voltage Distribution

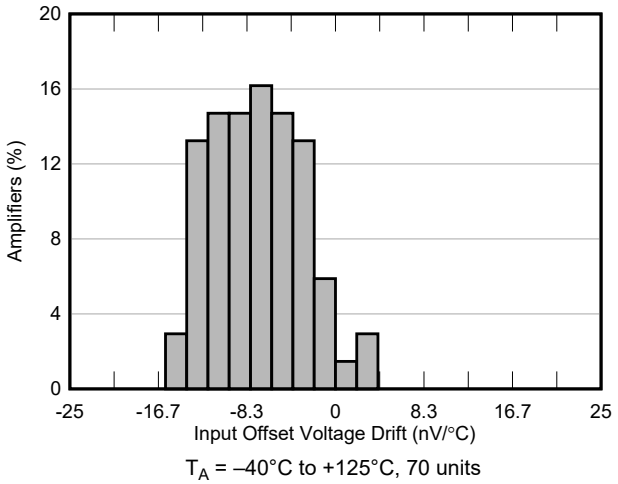


Figure 5-3. Offset Voltage Drift

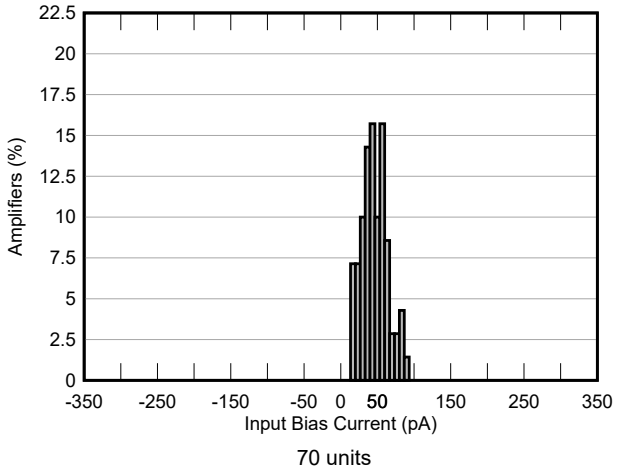


Figure 5-4. Input Bias Current Distribution, I_{BN}

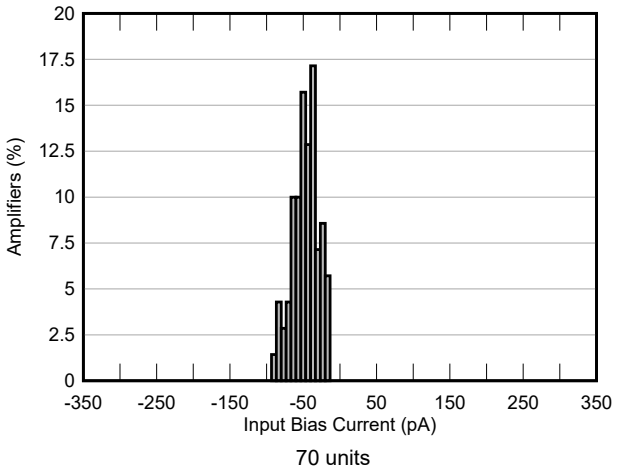


Figure 5-5. Input Bias Current Distribution, I_{BP}

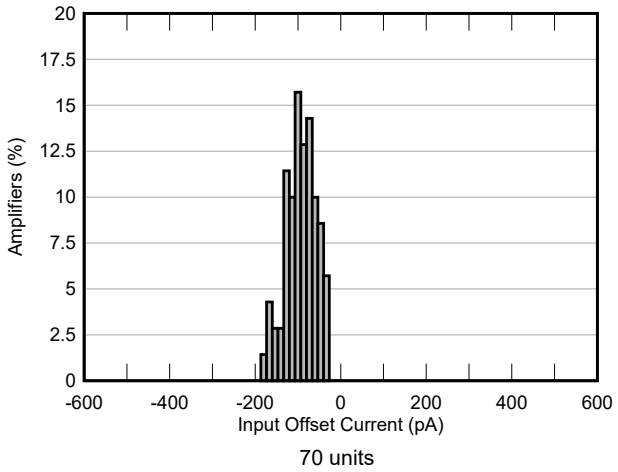


Figure 5-6. Input Offset Current Distribution

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 48V, V_{CM} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

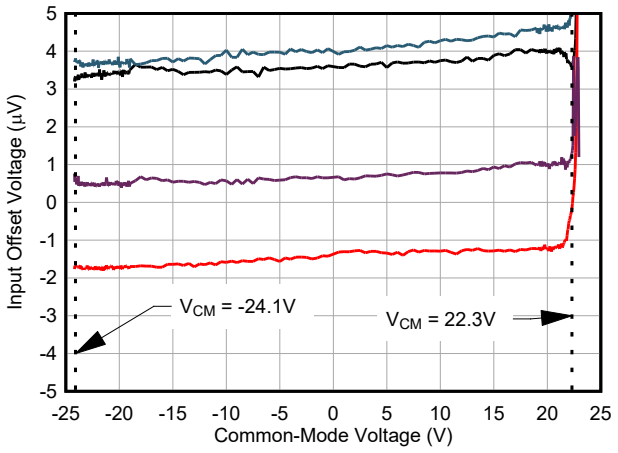
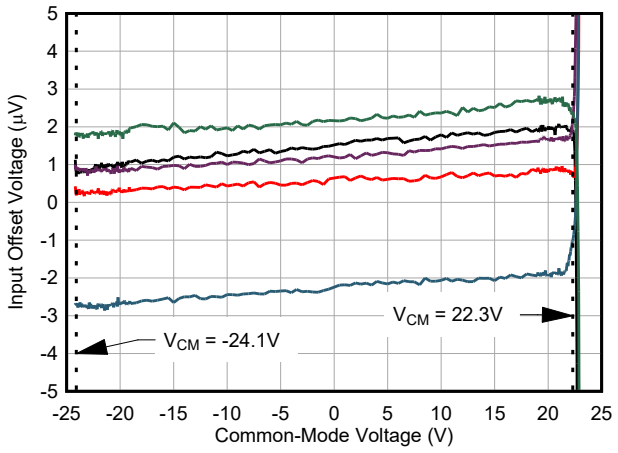
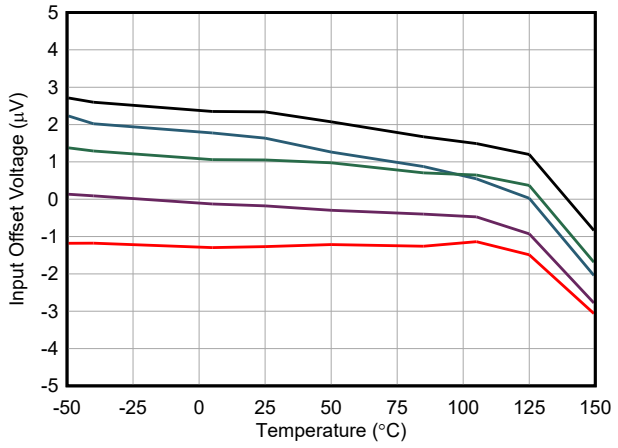


Figure 5-7. Offset Voltage vs Common-Mode Voltage



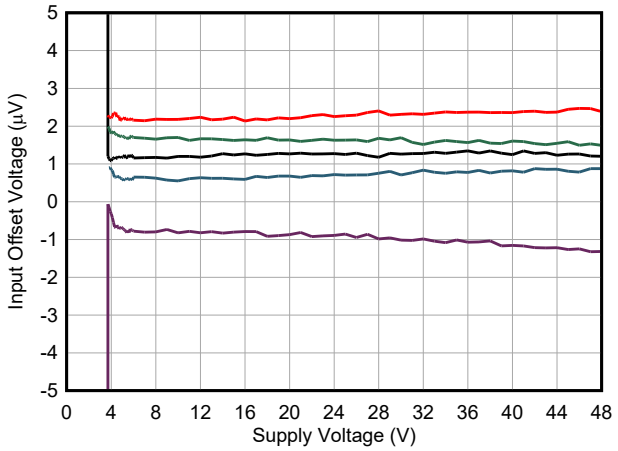
T_A = 125°C

Figure 5-8. Offset Voltage vs Common-Mode Voltage



5 typical units

Figure 5-9. Offset Voltage vs Temperature



5 typical units

Figure 5-10. Offset Voltage vs Supply Voltage

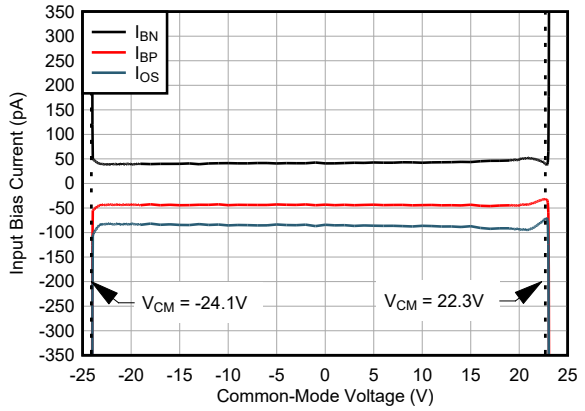


Figure 5-11. Input Bias Current vs Common-Mode Voltage

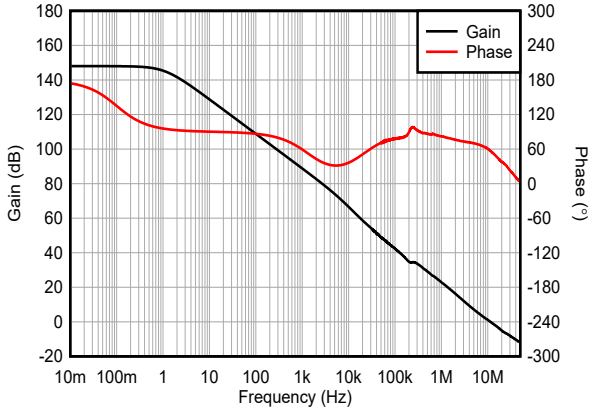


Figure 5-12. Open-Loop Gain and Phase vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 48V, V_{CM} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

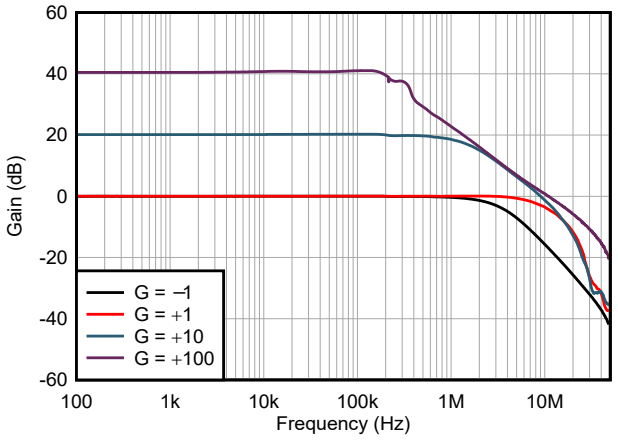


Figure 5-13. Closed-Loop Gain vs Frequency

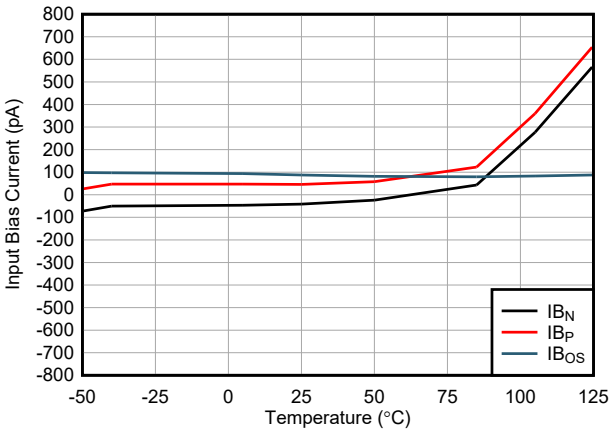


Figure 5-14. Input Bias Current and Offset Current vs Temperature

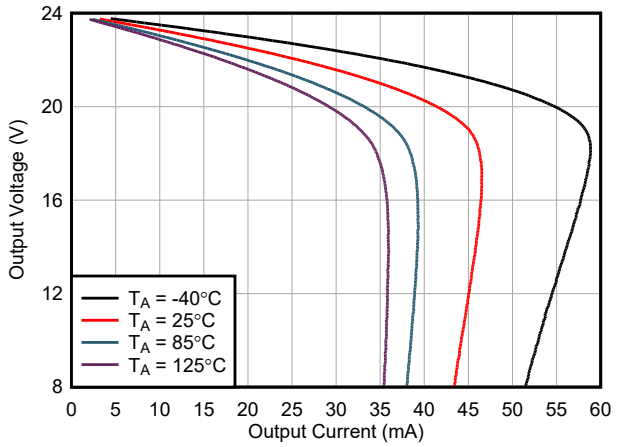


Figure 5-15. Output Voltage Swing vs Output Current (Sourcing)

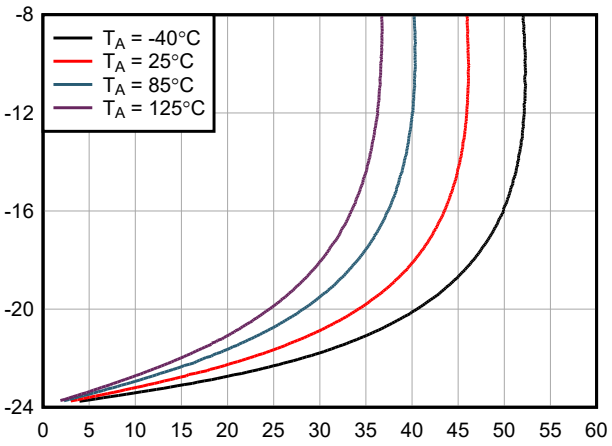


Figure 5-16. Output Voltage Swing vs Output Current (Sinking)

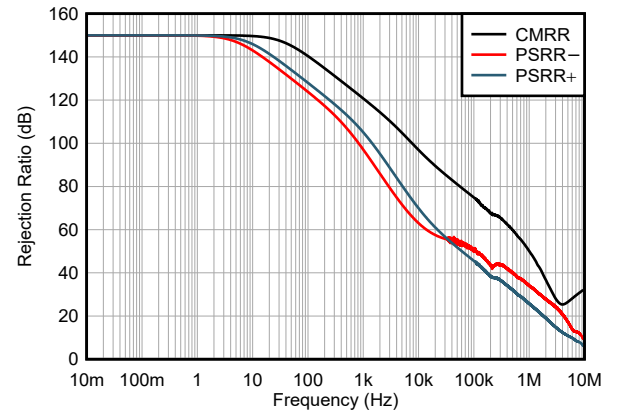


Figure 5-17. CMRR and PSRR vs Frequency

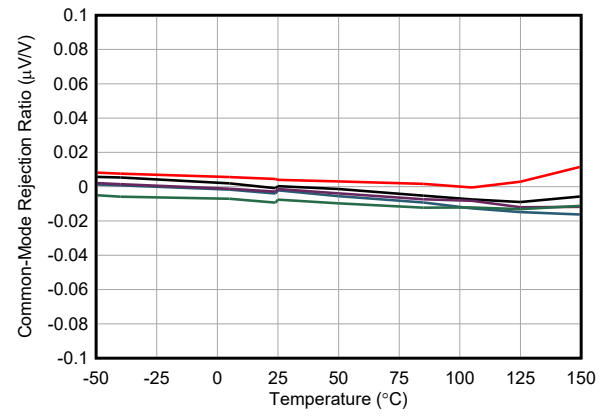


Figure 5-18. CMRR vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 48V, V_{CM} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

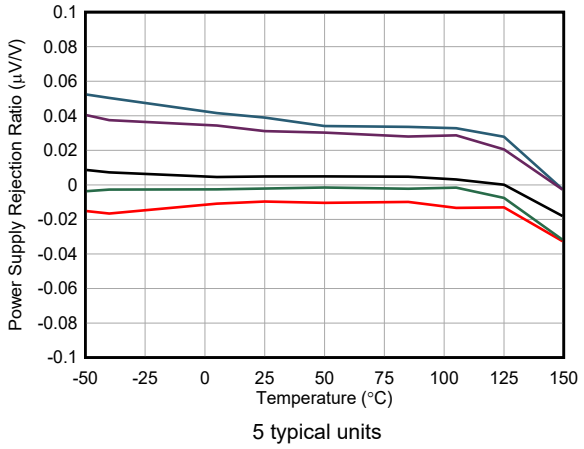


Figure 5-19. PSRR vs Temperature

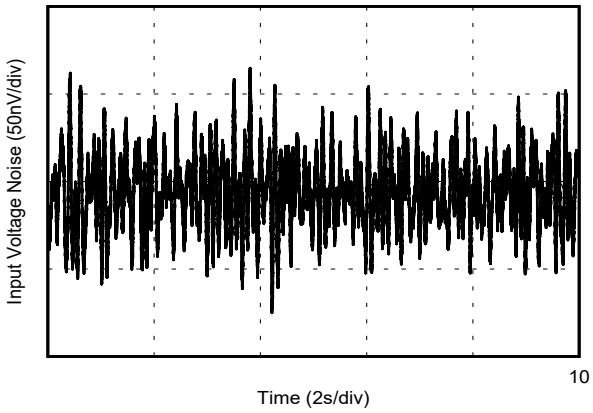


Figure 5-20. 0.1Hz to 10Hz Voltage Noise

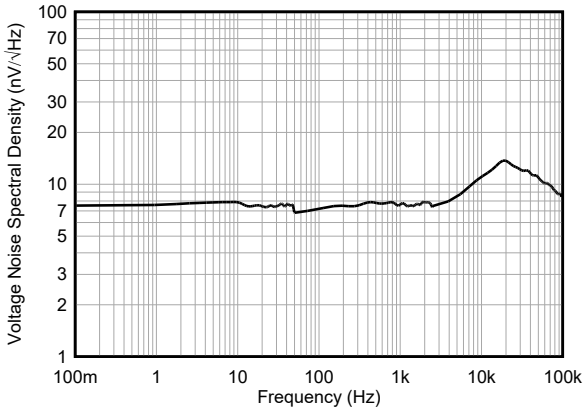


Figure 5-21. Input Voltage Noise Spectral Density vs Frequency

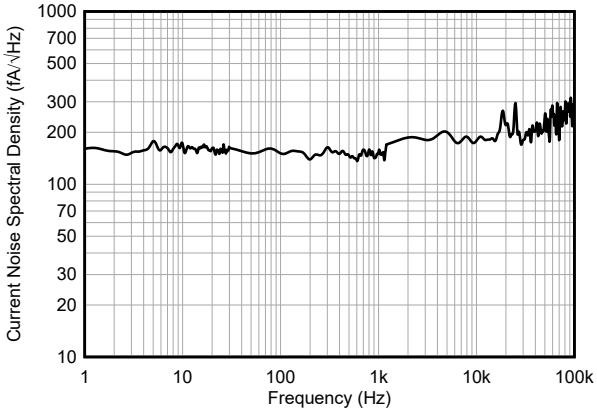


Figure 5-22. Input Current Noise Spectral Density vs Frequency

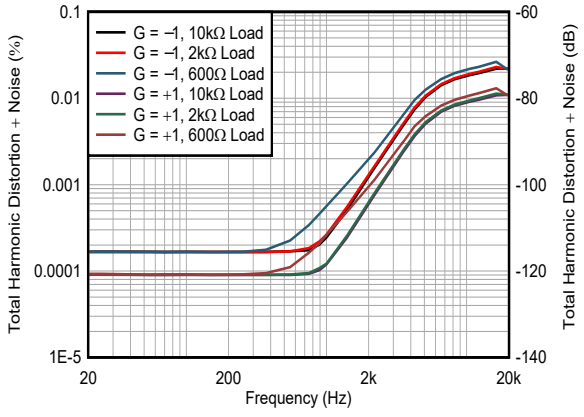


Figure 5-23. THD+N vs Frequency

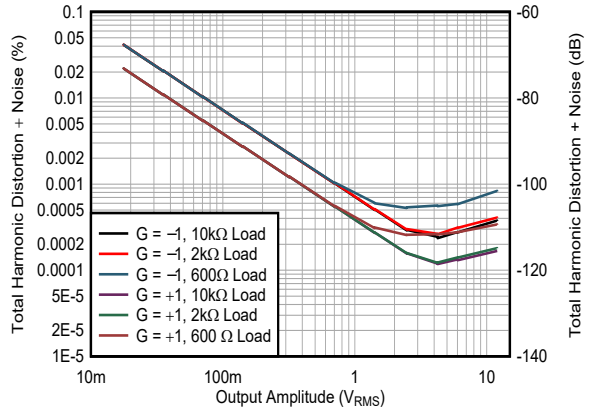


Figure 5-24. THD+N vs Output Amplitude

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 48V, V_{CM} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

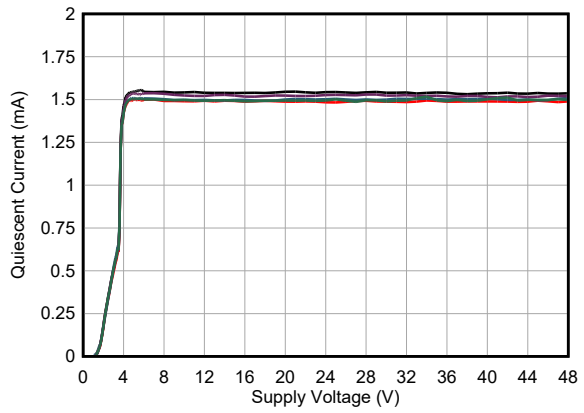


Figure 5-25. Quiescent Current vs Supply Voltage

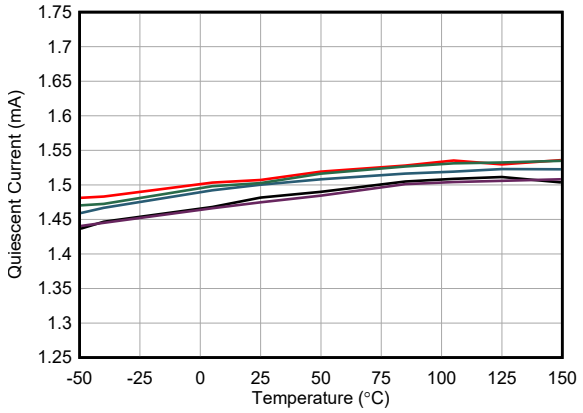


Figure 5-26. Quiescent Current vs Temperature

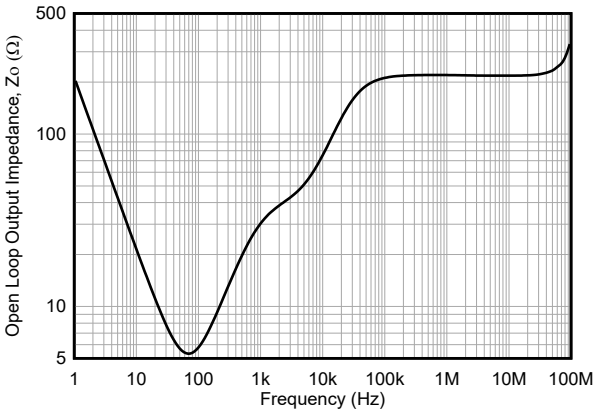


Figure 5-27. Open-Loop Output Impedance vs Frequency

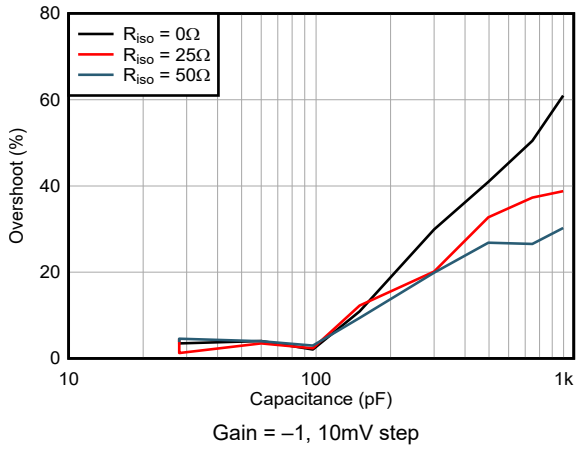


Figure 5-28. Small-Signal Overshoot vs Capacitive Load

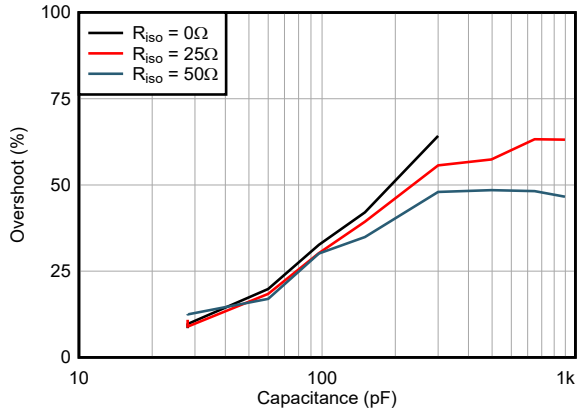


Figure 5-29. Small-Signal Overshoot vs Capacitive Load

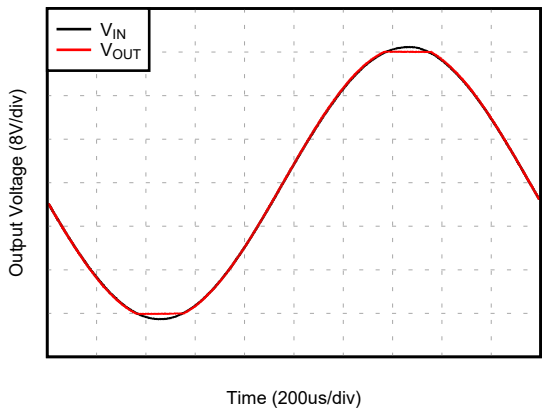


Figure 5-30. No Phase Reversal

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 48V, V_{CM} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

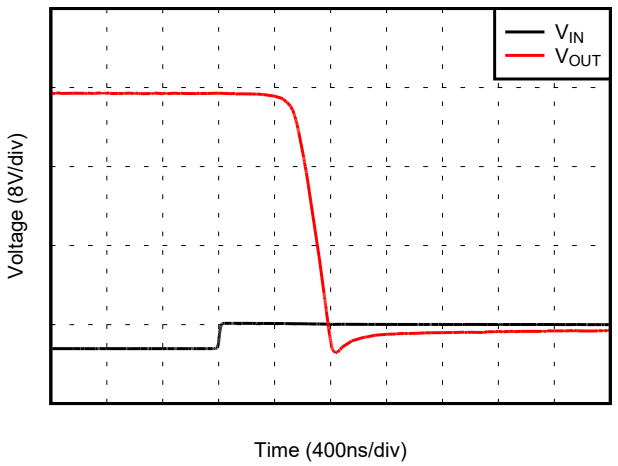


Figure 5-31. Positive Overload Recovery

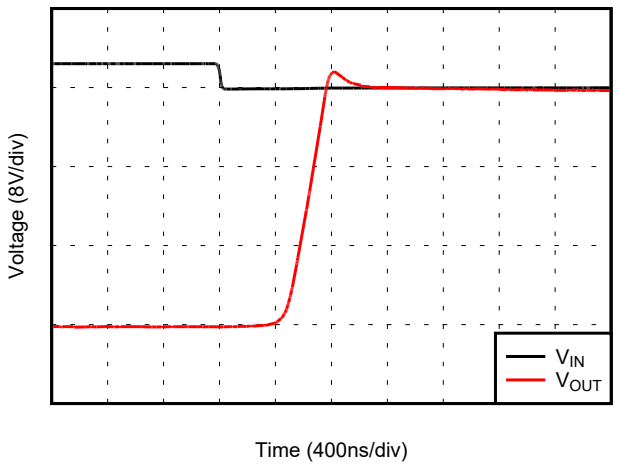


Figure 5-32. Negative Overload Recovery

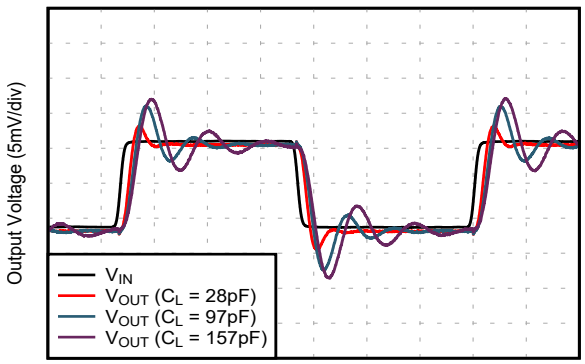


Figure 5-33. Small-Signal Step Response

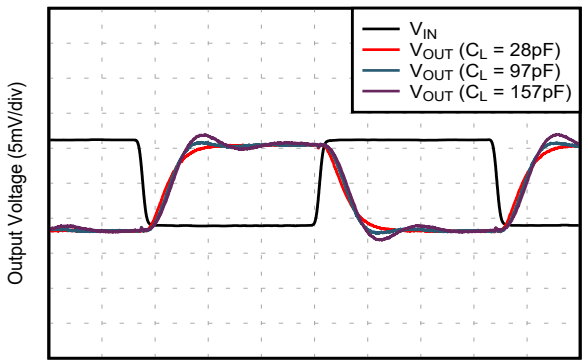


Figure 5-34. Small-Signal Step Response

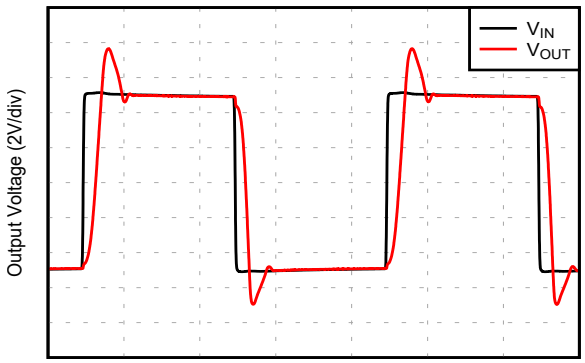


Figure 5-35. Large-Signal Step Response

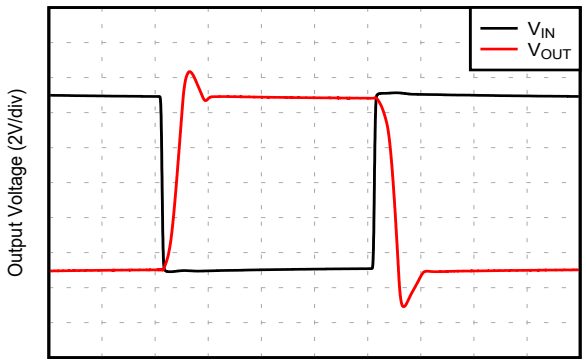


Figure 5-36. Large-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 48V, V_{CM} = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

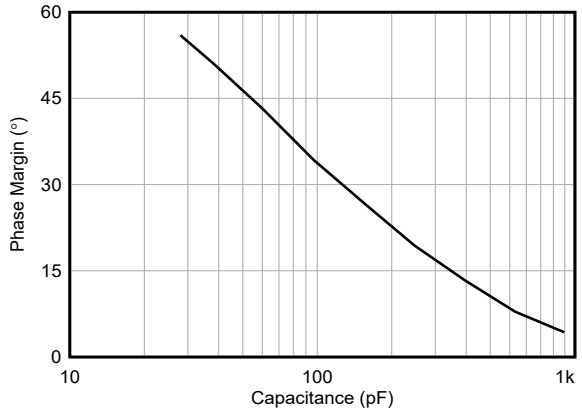
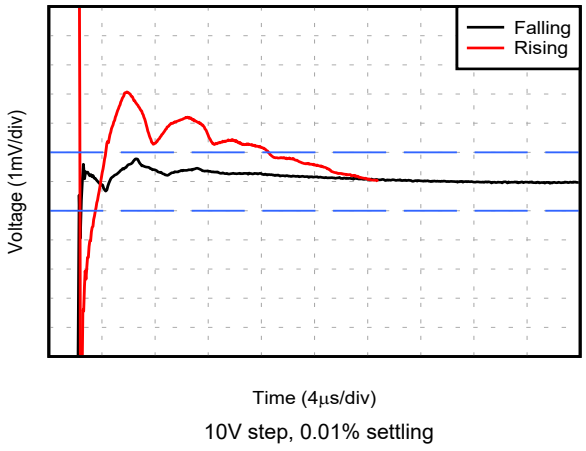


Figure 5-37. Phase Margin vs Capacitive Load



10V step, 0.01% settling

Figure 5-38. Settling Time

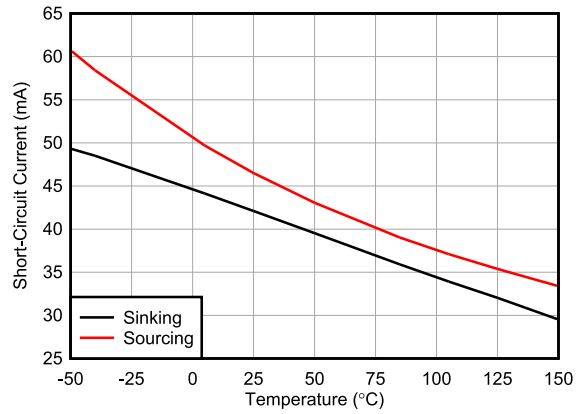


Figure 5-39. Short Circuit Current vs Temperature

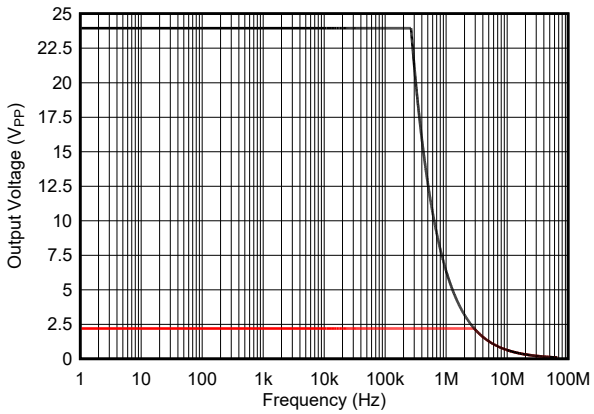


Figure 5-40. Maximum Output Voltage vs Frequency

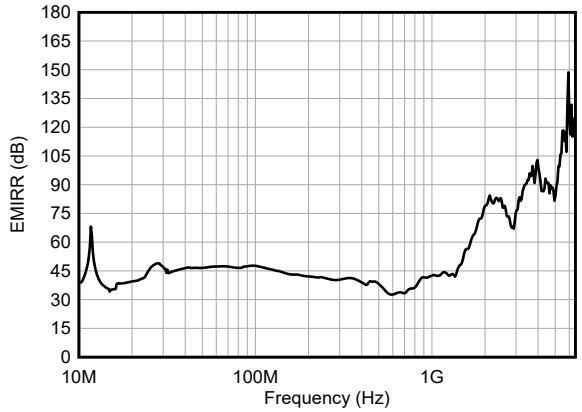


Figure 5-41. EMIRR vs Frequency

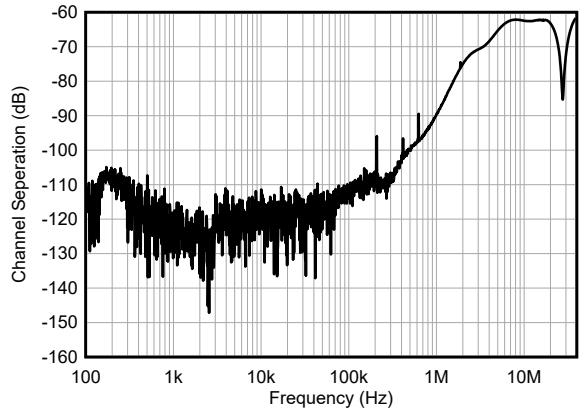


Figure 5-42. Channel Separation

6 Detailed Description

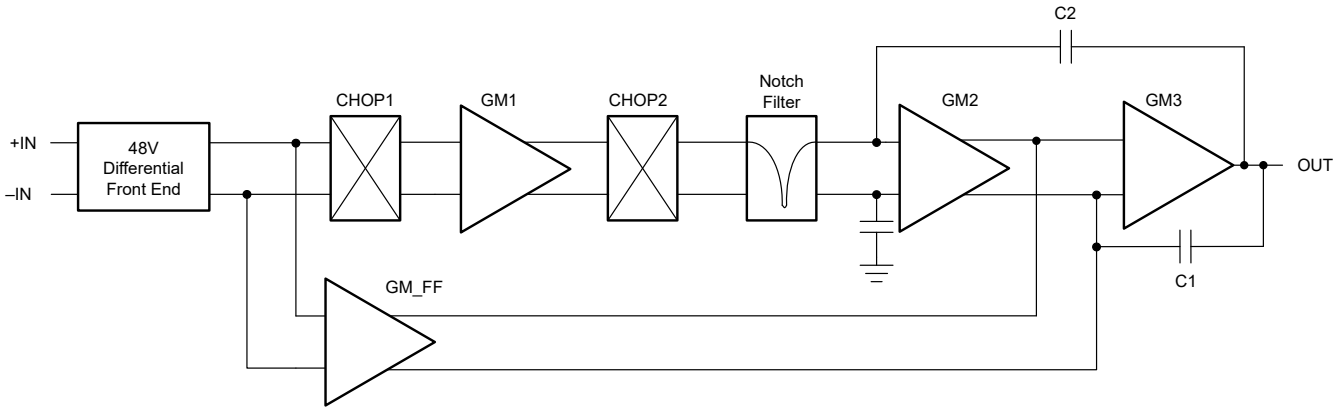
6.1 Overview

The OPAx488 are next generation operational amplifiers that provide 48V operating voltage and exceptional precision. The combination of ultra-low offset and drift with excellent dynamic performance makes these devices a great choice for a wide variety of precision applications. The precision maximum offset drift of only 0.025µV/°C provides stability over the entire operating temperature range of –40°C to +125°C. In addition, this device offers excellent linear performance with high CMRR, PSRR, and A_{OL}. The OPAx488 provide a wide gain-bandwidth of 14MHz to support very high gain configurations, and high frequency precision signal conditioning.

Additionally, the unity-gain stable OPAx488 are equipped with other features to enhance the signal conditioning performance. The devices feature MUX-friendly inputs, a patented technology that improves settling behavior and enables high precision multiplexed systems. The zero-drift architecture provides an additional benefit to the near-zero input offset voltage drift over temperature and time, as the architecture also eliminates the flicker noise of the amplifier

The following section shows a representation of the proprietary OPAx488 architecture.

6.2 Functional Block Diagram



6.3 Feature Description

The OPAx488 features a 48V operating and a 60V absolute maximum voltage to enable robust system designs. These operational amplifiers use a proprietary, periodic autocalibration technique to provide low input offset voltage and very low input offset voltage drift over time and temperature. The devices have several integrated features to help maintain a high level of precision through a variety of applications. These include a phase-reversal protection, EMI rejection, electrical overstress protection, and MUX-friendly inputs.

6.3.1 Input Common-Mode Range

The OPAx488 provide a wide input common-mode voltage range that extends beyond the negative rail making them an excellent choice for single supply operation. The positive input common-mode voltage extends to within 1.7V from the positive supply. The wide input common-mode voltage was designed to accommodate a wide range of different applications.

6.3.2 Phase-Reversal Protection

The OPAx488 have internal phase-reversal protection. Some op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx488 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 6-1 shows this performance.

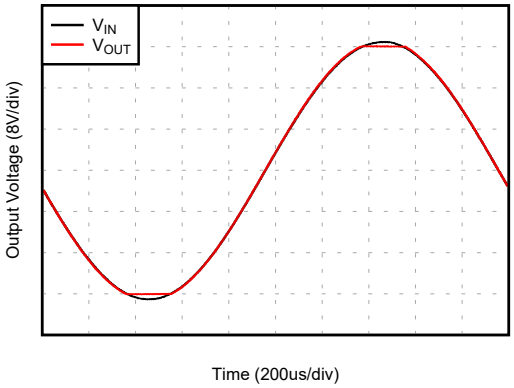


Figure 6-1. No Phase Reversal

6.3.3 Chopping Transients

Zero-drift amplifiers such as the OPAx488 use a switching architecture on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from being amplified; however, the pulses can be coupled to the output of the amplifier through the feedback network. Use low value resistors to minimize the input transient effects at the output of the amplifier. Use a low-pass filter, such as an RC network, to minimize any additional noise attributed to the transients. For more details on this topic, visit the Optimizing Chopper Amplifier Accuracy application report.

6.3.4 EMI Rejection

The OPAx488 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx488 benefits from these design improvements.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects, as there is insufficient amplifier loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

6.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin.

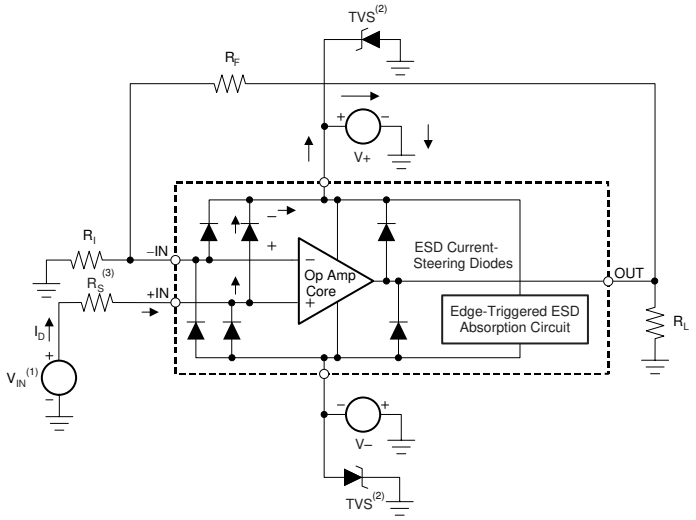
Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 6-2 shows an illustration of the ESD circuits contained in the OPAx186 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger or threshold voltage that is greater than the normal operating voltage of the OPAx488, but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

Figure 6-2 shows that when the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive, and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits are biased on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.



(1) V_{IN} = (V+) + 500mV

(2) TVS: 60V > $V_{TVSBR\ (min)}$ > V+, where $V_{TVSBR\ (min)}$ is the minimum specified value for the transient voltage suppressor breakdown voltage.

(3) Suggested value is approximately 5kΩ in overvoltage condition.

Figure 6-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

Figure 6-2 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current-steering diodes. This state is not a normal biasing condition for the amplifier and can result in specification degradation or abnormal operation. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see also Figure 6-2. The Zener voltage must be selected such that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

6.3.6 MUX-Friendly Inputs

The OPAx488 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature antiparallel diodes that protect input transistors from large V_{GS} voltages that can exceed the semiconductor process maximum and permanently damage the device. Large V_{GS} voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator.

The OPAx488 solves these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This input architecture addresses many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials.Figure 6-3 shows a typical application where MUX-Friendly inputs can improve settling time performance. The OPAx488 offers outstanding settling performance as a result of these design innovations and built-in slew-rate boost and wide bandwidth. The OPAx488 can also be used as a comparator. Differential and common-mode input ranges still apply.

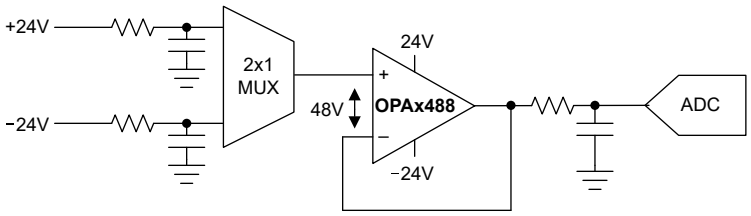


Figure 6-3. Multiplexed Application

6.4 Device Functional Modes

The OPAx488 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The recommended power supply voltage for the OPAx488 is between 4.5V (±2.25V) and 48V (±24V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx488 operational amplifiers offer a unique combination of excellent dc and ac characteristics making them an excellent choice for a wide variety of applications. For example, the combination of 48V operation, fast settling, and exceptional offset and drift, make these devices superb choices for demanding high side current sense applications. Other applications that benefit from the performance of the OPAx488 include strain gauges, force sensors, and thermocouples.

7.1.1 Basic Noise Calculations

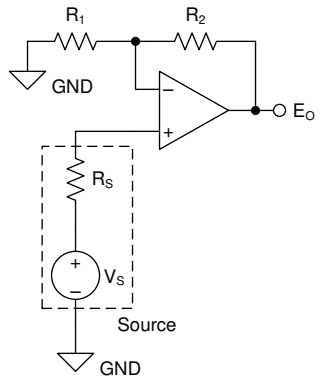
Low-noise circuit design requires careful analysis of all noise sources. In many cases, external noise sources can dominate; consider the effect of source resistance on overall op-amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is usually fixed; consequently, select op amp and the feedback resistors that minimize the respective contributions to the total noise.

Figure 7-1 shows both noninverting *(A)* and inverting *(B)* op-amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the low current noise of the OPAx488 means that the current noise contribution can be ignored.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + \left(e_{R_1 \| R_2}\right)^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

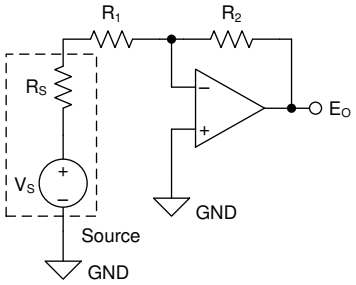
$$(2)\quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_S$$

$$(3)\quad e_{R_1 \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \text{ || } R_2$$

$$(4)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + \left(e_{R_1 + R_S \| R_2}\right)^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1 + R_S \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_S) \text{ || } R_2$$

$$(8)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

Where e_n is the voltage noise spectral density of the amplifier. For the OPAx488 operational amplifier, e_n = 7.5nV/$\sqrt{Hz}$ at 1kHz.
NOTE: For additional resources on noise calculations, visit *TI Precision Labs*.

Figure 7-1. Noise Calculation in Gain Configurations

7.2 Typical Applications

7.2.1 High-Side Current Sensing

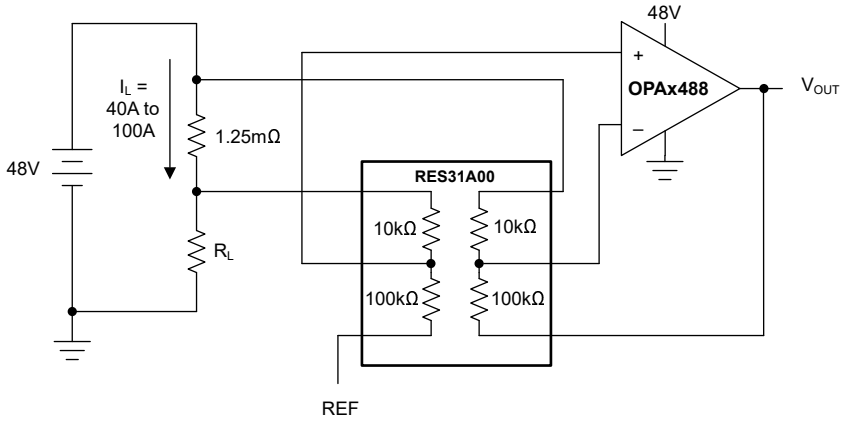


Figure 7-2. High-Side Current Monitor

7.2.1.1 Design Requirements

Current monitoring is a critical function in a wide range of applications. In power supplies, for example, current monitoring is part of a closed loop system that regulates the power being delivered to a load. While ample, readily available current monitors exist today, a number of applications have current sensing requirements which cannot be met by monolithic devices in the market. Some of these requirements can include flexible gain, high speed, high common-mode voltage, and high impedance.

A current monitor that meets application specific requirements can be designed using a high voltage, high precision op amp such as the OPAx488 and the RESx1A series of precision matched resistors. The combination of the OPAx488 op amp and the RESx1A matched resistor pair enables a high impedance, high input common-mode, high precision current monitor to be built.

Use the following parameters for this design example:

- Power supply voltage rating: 48V
- Input common-mode voltage range: 48V
- Load current, I_L: 50A to 200A

The following design details and equations can be used to reconfigure this design for specific requirements.

7.2.1.2 Detailed Design Procedure

High-side current sense circuits require special consideration of the input and output common-mode limitations of the amplifier. The biggest challenge in high-side current measurements is making sure that the amplifier can support and mitigate the errors that are inherent to high common-mode voltage. Specific design requirements for common-mode voltage, shunt resistance, and current range leave designers with important decisions about input impedance, cost, complexity, and gain trade-offs.

For example, a very high common-mode voltage current monitor can be easily designed, but a simple high-common mode voltage current monitor results in large resistors and attenuating gain. High value resistors can be expensive, physically large, and difficult to source. Furthermore, the resulting attenuation requires larger shunt resistors to be used, and/or additional gain stages.

With a few more resistors, designers can build a unity-gain, high common-mode voltage amplifier, but an additional gain stage is necessary to adequately digitize the information. More importantly, consider that the drop across the shunt resistor is very small and the output of the current monitor is driven close to ground which is outside of the linear output voltage range of most single supply amplifiers. A simple resolution, of course, is to power the amplifier with dual supplies. However, dual supplies limit the maximum positive voltage that can be used, which limits the maximum input common-mode voltage range of the amplifier. Additional components, such as the LM27761 can be used to generate a small negative bias to accommodate the low level signal, but that also adds cost.

One obvious way to improve the input common-mode voltage of the amplifier is to use a higher voltage amplifier. Higher operating voltage eases the need for very high resistor values, and enables higher gain configurations. The OPAx488 provides a very wide operating voltage thereby eliminating the need for supplementary components and minimizing overall system complexity. The OPAx488 is configured as a current monitor as illustrated in Figure 7-2.

This design is expected to measure current for a high power, high voltage power supply with ratings of 48V and up to 9600W. These high wattage power supplies can be found in data centers and electric scooters. The high voltage supply reduces the amount of current necessary to deliver a set amount of power when compared to a lower voltage supply. However, 9600W still amounts to a very high current output of about 200A at 48V. The current monitor designed here can reliably measure currents from 40A to 200A with a common-mode voltage of up to 48V.

The maximum common-mode voltage is a function of the current monitor gain and the supply voltage of the op amp as shown in Equation 2 and Equation 3. As discussed earlier, increasing the voltage divider ratio to improve the common-mode voltage capability of the monitor results in low gain and increasing the supply voltage enables better results. The OPAx488 is configured with a gain of 10V/V to provide a maximum output voltage of 2.5V at the full scale current range across a 1.25mΩ shunt resistor. The gain is given by Equation 1. Make sure that the shunt resistor is appropriately rated to handle the power dissipation of about 50W for this application.

$$G = \frac{R_G}{R_{IN}} \tag{1}$$

$$V_{IN}\left(\frac{G}{G+1}\right) + V_{REF}\left(\frac{1}{G+1}\right) \leq V_+ - 1.7V \tag{2}$$

$$V_{IN}\left(\frac{G}{G+1}\right) + V_{REF}\left(\frac{1}{G+1}\right) \geq V_- - 0.1V \tag{3}$$

Another thing to consider in this application is the input impedance of the current monitor which is set by R1 and R2. To maintain the precision and noise performance of the OPAx488, keep R1 as small as possible. A trade-off must be made between performance and input impedance. In this application, 10kΩ and 100kΩ resistors provide a good compromise for noise and precision. The matching of these resistors is critical to maintain precision measurements so the RES31A matched resistor pairs are used. The RES31A achieves significantly better common-mode rejection ratio (CMRR) than discrete 0.1% resistors, as shown in Figure 7-3.

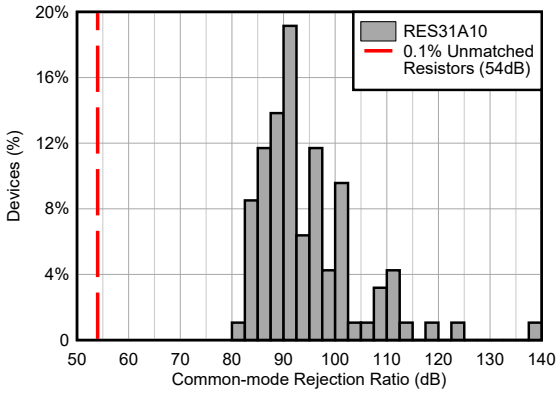


Figure 7-3. RES31A Common-Mode Rejection Ratio

Despite the advantages rendered, the design is not without limitations. The first is that the output swing to ground is limited by the linear output swing of the OPAx488 given in *Electrical Characteristics* under open-loop voltage gain (AOL). The output swing limitation to ground introduces a threshold to which the current monitor is able to accurately measure. To widen the lower limit current range, simply add a small negative bias voltage of −1V using the LM27761.

Another limitation to consider is the limited output voltage swing to the positive rail. This limitation is set by the maximum gain of the monitor and prevents the full scale range of a given 3V or 5V analog-to-digital (ADC) converter to be used. Increasing the gain simply requires a new set of resistor ratios not currently available in a monolithic chip from Texas Instruments. Recall that the maximum gain available is limited by the input common-mode range of the amplifier. With the given constraints in this application, the gain is limited to about 27V/V which is considerably higher than 2.5V/V for a 36V amplifier.

The limited input impedance is another potential drawback in some applications. This is especially true when measuring much smaller currents. To achieve very high input impedance, buffer the inputs of the current monitor with the OPAx488. The downside to this circuit is that the input common-mode voltage range is now limited by that of the buffer. With the OPAx488, the input common-mode is limited to (V−) to (V+) − 1.7V, or from 0V to 46.3V given the constraints of this application. Consider using an even higher voltage amplifier like the OPA596 with input common-mode voltage of up to 81.5V.

The circuit in Figure 7-2 was checked using the TINA Spice circuit simulation tool to verify the correct operation of the OPAx488 high-side current monitor. The simulation results are seen in Figure 7-4. Upon careful inspection of the plots, one unexpected outcome is that V_{OUT} continues well above 200A, where V_{OUT} is greater than 2.5V. The output of the OPAx488 can swing well beyond 2.5V, but the power dissipated across the shunt becomes the limiting factor on the upper end of the current measurement range. V_{OUT} also continues towards zero well below 48A, where V_{OUT} is 600mV or less, but the lower end of the current measurement range is limited by the linear output swing of the amplifier.

The OPAx488 output, as well as other CMOS output amplifiers, often swing closer to 0V than the linear output parameters suggest. The voltage output swing, V_O (see the *Electrical Characteristics* table), is not an indication of the linear output range, but rather how close the output can move towards the supply rail. In that region, the amplifier output approaches saturation, and the amplifier ceases to operate linearly. Thus, in the current-monitor application, the current-measurement capability can continue to much less than the 600mV output level. However, keep in mind that the linearity errors are becoming large.

This current monitor circuit can be used to measure alternating current (AC) as well. The OPAx488 provide excellent performance over frequency with ample slew rate and bandwidth to support the output voltage swing range and waveform of a wide range of high frequency signals.

For more information about amplifier-based, high-side current monitors, see the *TI Analog Engineer's Circuit Cookbook: Amplifiers*.

7.2.1.3 Application Curve

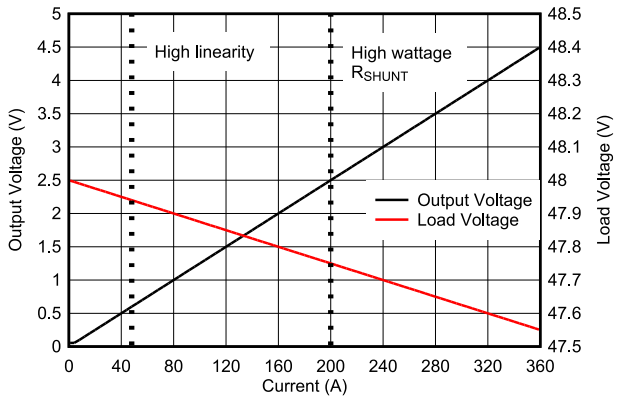


Figure 7-4. High-Side Current Monitor Results

7.2.2 Programmable Current Source

There are many applications that require a precise current source. Resistance temperature detectors (RTDs), for example, often require a precision current source to accurately measure temperature.Figure 7-5 shows a common configuration for a precision current source using the OPAx488. The circuit provides designers the ability to program the current for different use cases with a voltage source, such as a digital-to-analog converter (DAC).

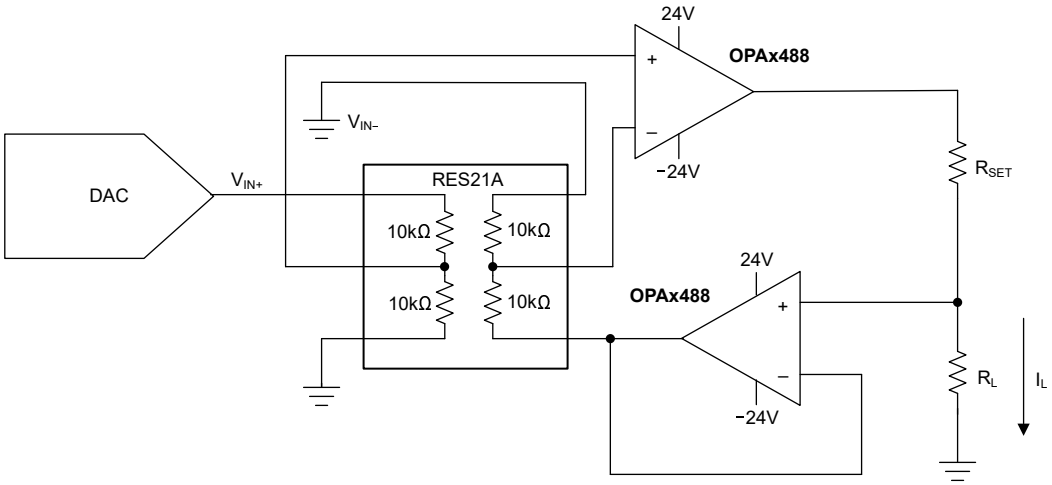


Figure 7-5. Howland Current Pump

The current is set by the differential input voltage, $V_{IN+} - V_{IN-}$. Note that you can short one of the input voltages to control the current with a single ended signal as is the case here. The current is programmed according to Equation 4. Note that the maximum source and sink current is limited by the output drive capability of the amplifier. The Howland current pump is a great option for low level, very high precision current sources. The OPAx488 supply voltage of 48V provides the added benefit of a higher compliance voltage.

$$I_L = \frac{(V_{IN+} - V_{IN-})}{R_{SET}} \quad (4)$$

To learn more about this circuit, visit the Analysis of Improved Howland Current Pump Configurations application report.

7.2.3 Programmable Current Source For A Grounded Load

Figure 7-6 shows the OPAx488 configured as a programmable current source for a ground referenced load. To achieve single supply operation, a two stage design is employed. The first stage sets a reference current, and the second stage acts as a current mirror with gain. The OPAx488 are used to regulate the current sourced from the transistors in both stages. This design benefits from the higher operating voltage of the OPAx488. The 48V operation enables a higher supply voltage to be used to increase compliance voltage and allow a higher maximum load resistance, R_L.

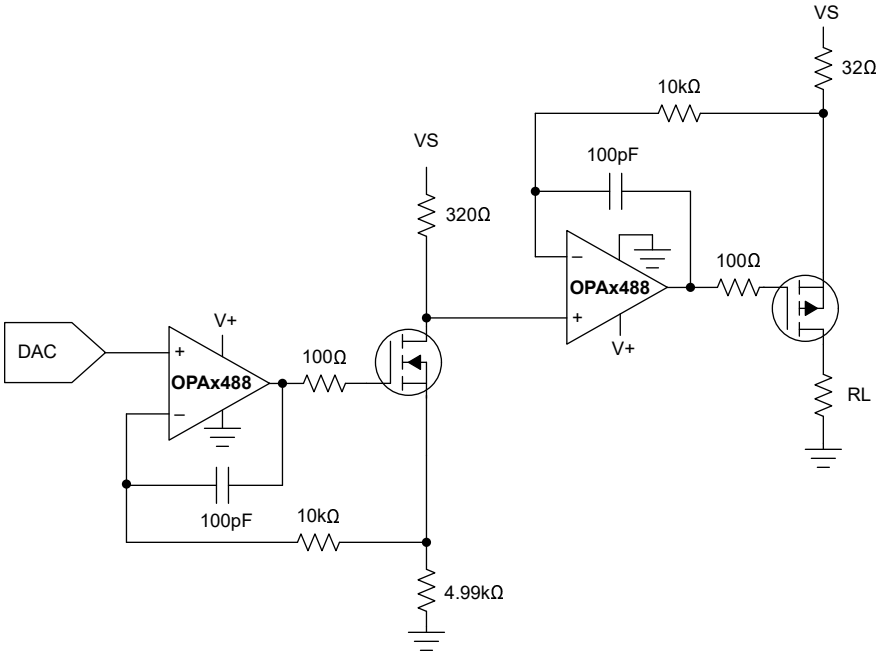


Figure 7-6. Single Supply Programmable Current Source For A Ground Referenced Load

7.3 Power Supply Recommendations

The OPAx488 are specified for operation from 4.5V to 48V (±2.25V to ±24V). The OPAx488 can operate on both single and dual supplies. The OPAx488 do not require symmetrical supplies; the op amps only require a minimum voltage of 4.5V to operate.

CAUTION

Supply voltages larger than 60V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 7.4*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices:

- For the lowest offset voltage, avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Also:
  - Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
  - Thermally isolate components from power supplies or other heat sources.
  - Shield operational amplifier and input circuitry from air currents, such as cooling fans.
- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see the *The PCB is a component of op amp design* analog application journal.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As Figure 7-7 shows, keep the feedback resistor (R3) and gain resistor (R4) close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

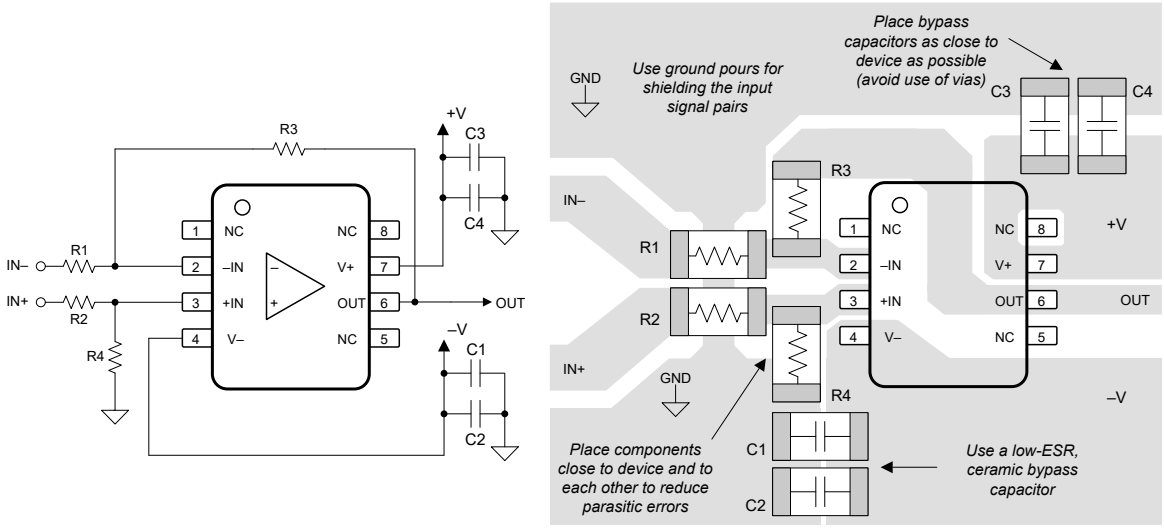


Figure 7-7. Operational Amplifier Board Layout for Difference Amplifier Configuration

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Zero-drift Amplifiers: Features and Benefits* application brief
- Texas Instruments, *The PCB is a component of op amp design* application note
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters* application note
- Texas Instruments, *Op Amp Performance Analysis*
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application note
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application note
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application note
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* application note
- Texas Instruments, *TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4488DR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4488
OPA4488PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4488

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

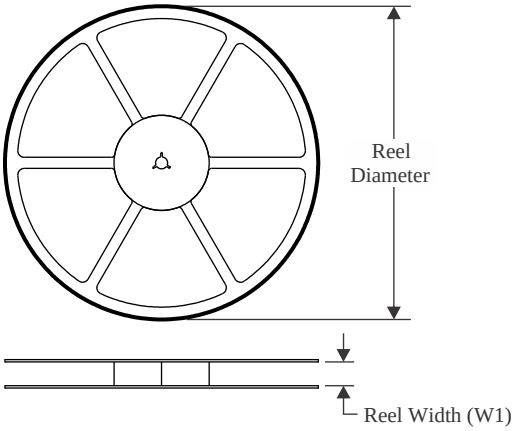
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

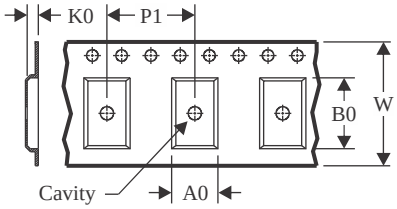
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

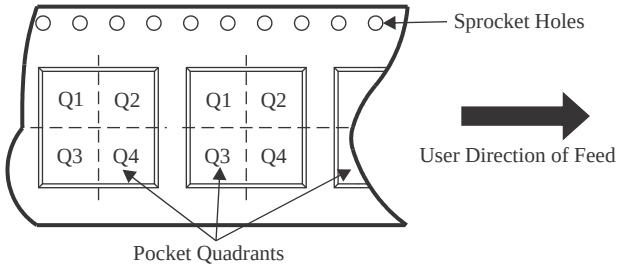


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

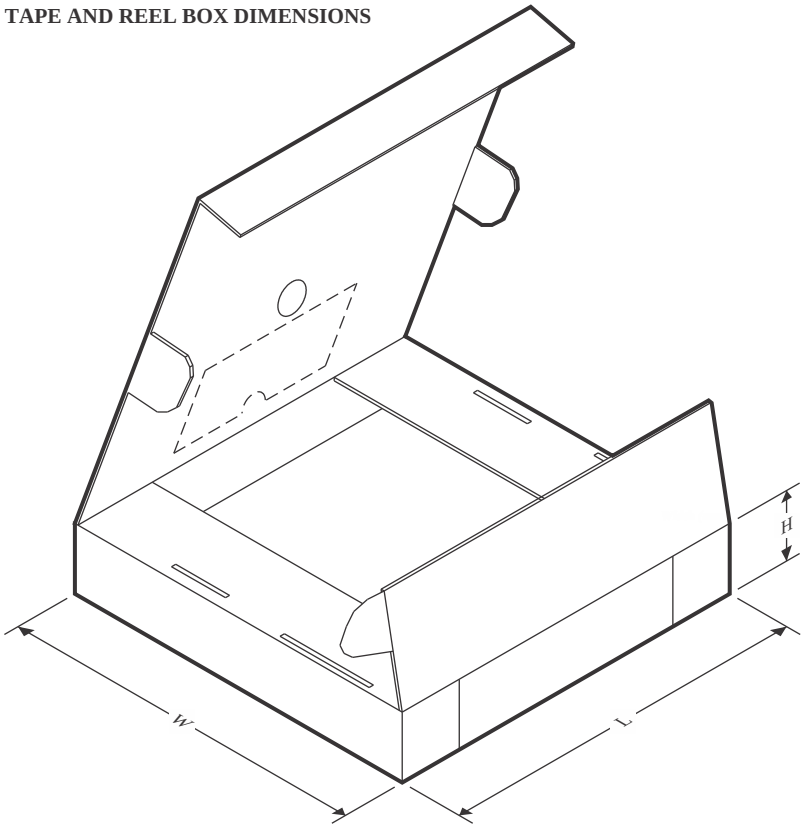
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

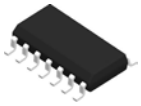
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4488PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4488PWR	TSSOP	PW	14	3000	353.0	353.0	32.0

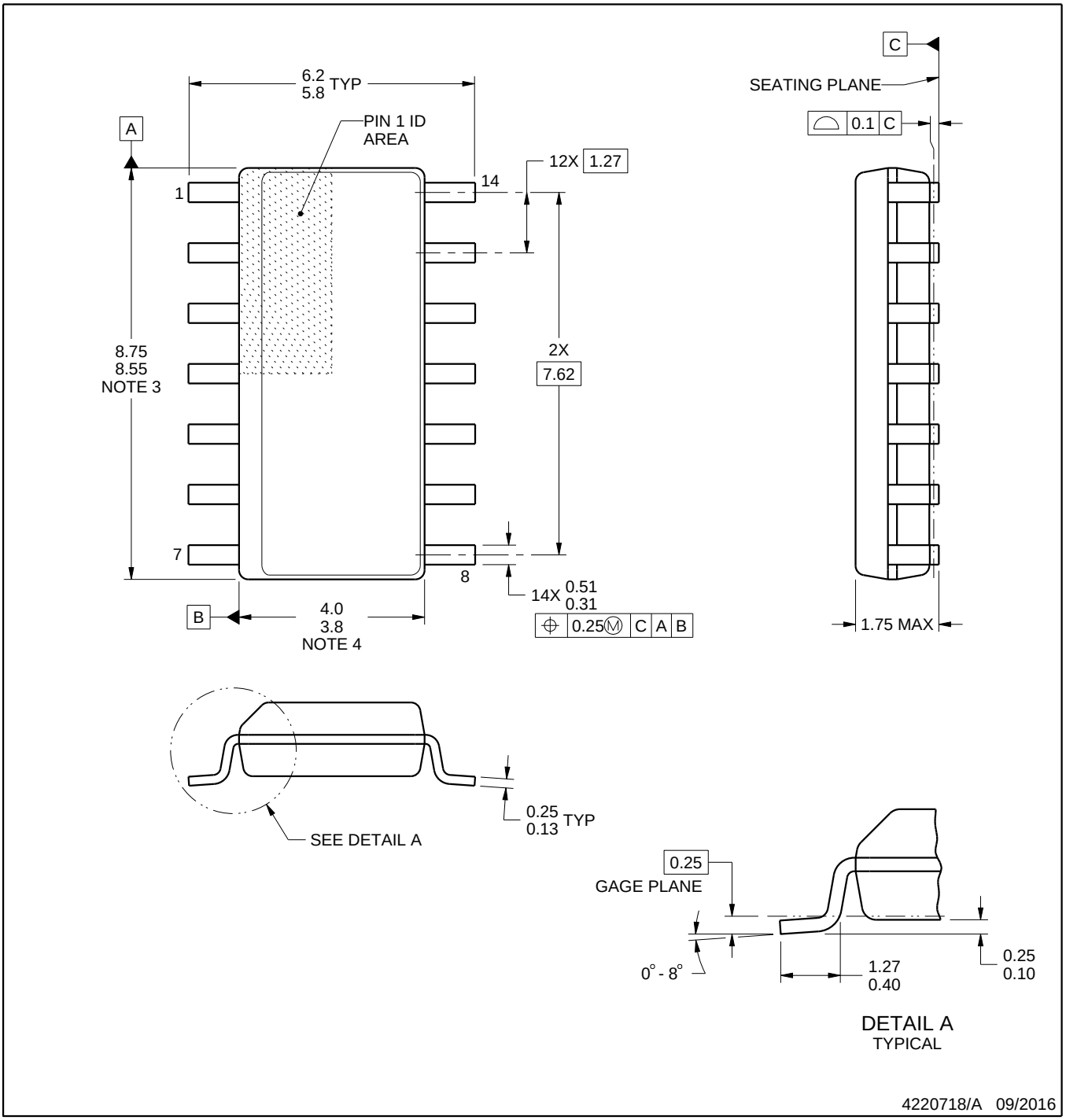


PACKAGE OUTLINE

D0014A

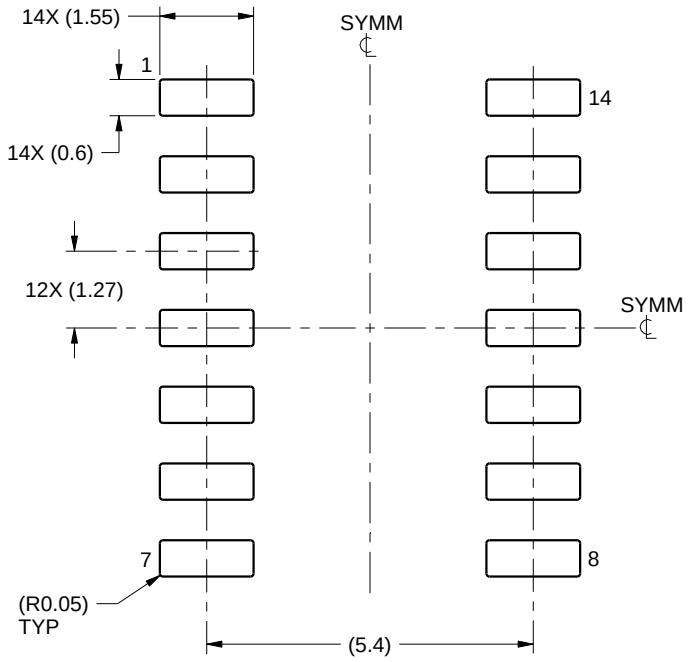
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

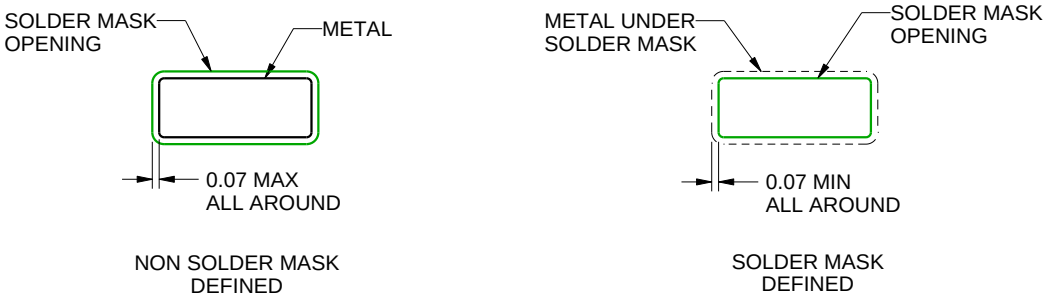


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

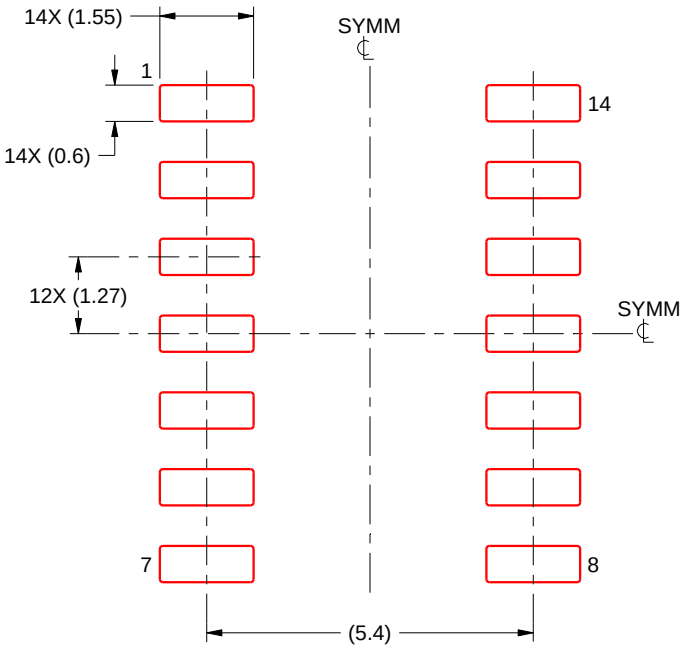
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

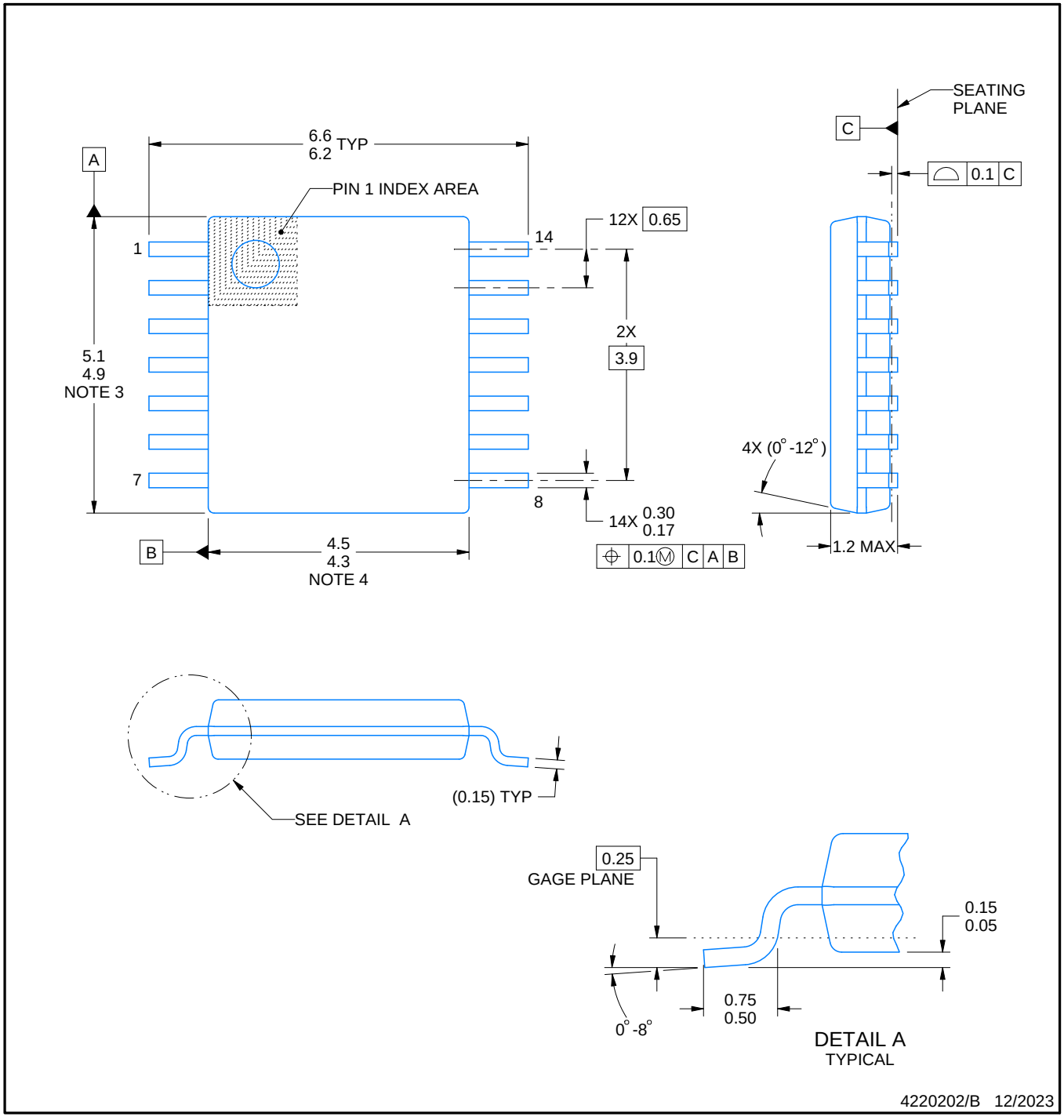
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

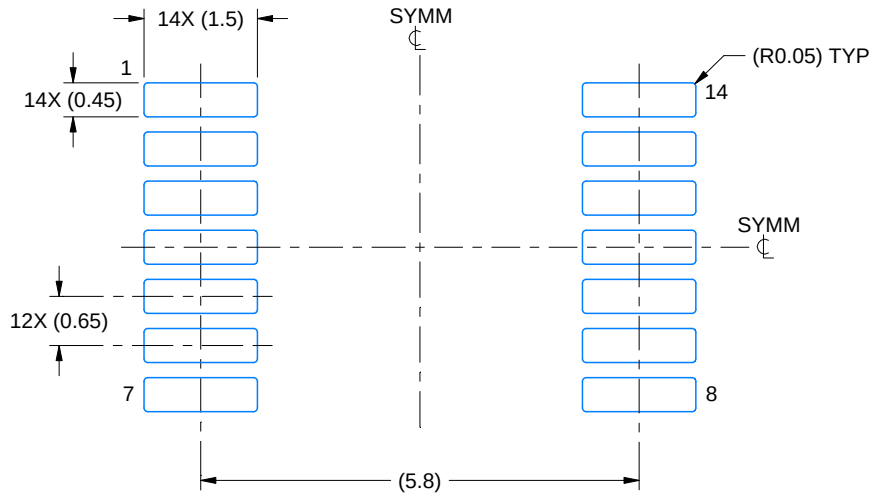
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

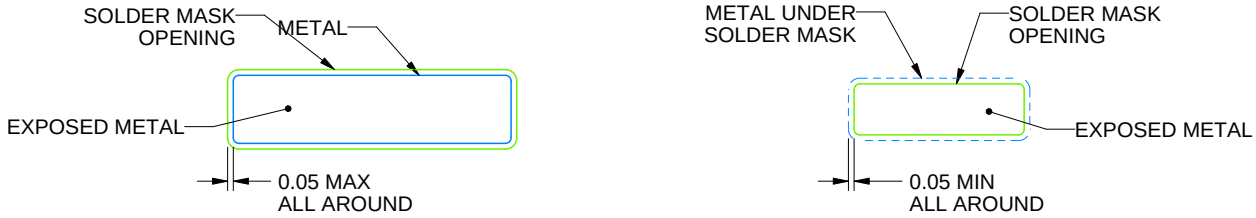


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

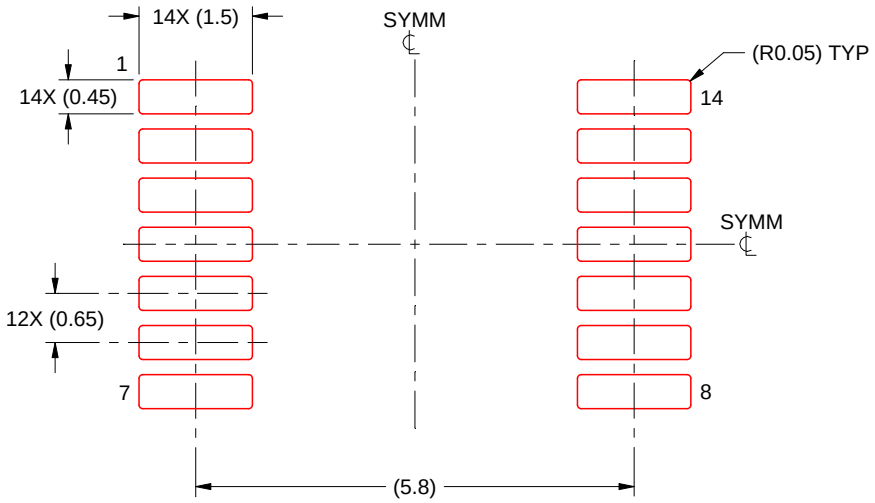


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025