

80V, 50mA OPERATIONAL AMPLIFIERS

FEATURES

- **WIDE POWER-SUPPLY RANGE:**
 $\pm 10\text{V}$ to $\pm 40\text{V}$
- **HIGH OUTPUT LOAD DRIVE:**
50mA Continuous
- **WIDE OUTPUT VOLTAGE SWING:** 1V to Rail
- **FULLY PROTECTED:**
Thermal Shutdown
Output Current-Limited
- **WIDE OPERATING TEMPERATURE RANGE:**
 -40°C TO $+125^{\circ}\text{C}$
- **PACKAGE OPTIONS:**
TO220-7
DDPACK-7 Surface-Mount

APPLICATIONS

- **PIEZOELECTRIC CELLS**
- **TEST EQUIPMENT**
- **AUDIO AMPLIFIERS**
- **TRANSDUCER DRIVERS**
- **SERVO DRIVERS**

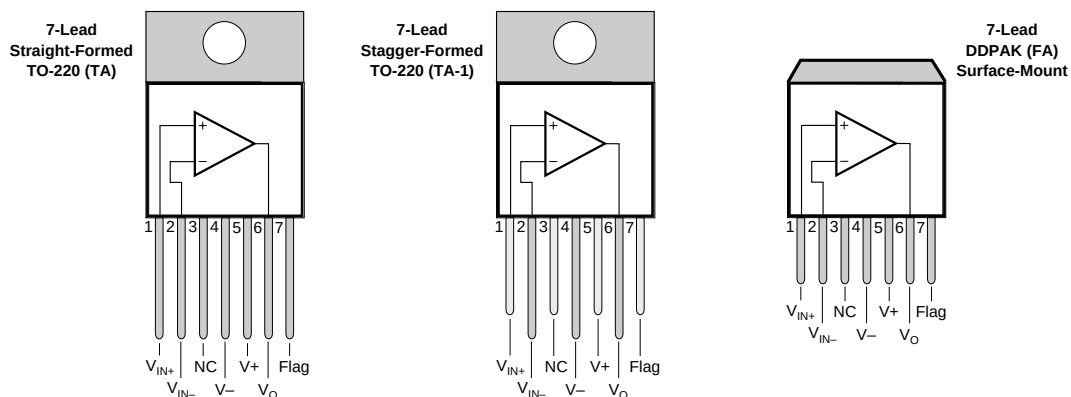
DESCRIPTION

The OPA452 and OPA453 are low-cost operational amplifiers with high-voltage (80V) and high-current capabilities (50mA). The OPA452 is unity-gain stable and has a gain bandwidth product of 1.8MHz, whereas the OPA453 is optimized for gains greater than 5 and has a 7.5MHz bandwidth.

The OPA452 and OPA453 are internally protected against over-temperature conditions and current overloads. Power supplies in the range of $\pm 10\text{V}$ to $\pm 40\text{V}$ can be used. Unlike most other power op amps, the OPA452 and OPA453 have ensured specifications over the entire power-supply range.

These laser-trimmed, monolithic integrated circuits provide excellent low-level accuracy along with wide output swing. Special design considerations assure that the product is easy to use and free from phase inversion problems often found in other amplifiers.

The OPA452 and OPA453 are available in TO220-7 and DDPACK-7 options. They are specified for a junction temperature range of -40°C to $+125^{\circ}\text{C}$.



NOTE: Tabs are electrically connected to $V-$ supply.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V–	80V
Signal Input Terminals, Voltage ⁽²⁾	(V–) – 0.5V to (V+) + 0.5V
Current ⁽²⁾	5mA
Output Short-Circuit	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering 10s, TO-220)	300°C
(soldering 3s, DDPAK)	240°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 5mA or less.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.



ELECTROSTATIC
DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: OPA453; $V_S = \pm 10V$ to $\pm 40V$

Boldface limits apply over the specified junction temperature range, $T_J = -40^{\circ}C$ to $+125^{\circ}C$.

At $T_J = +25^{\circ}C$, $R_L = 3.8k\Omega$ connected to ground, and $V_{OUT} = 0V$, unless otherwise noted.

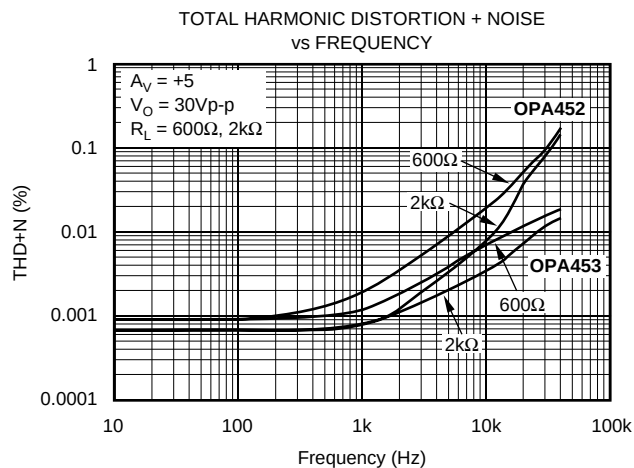
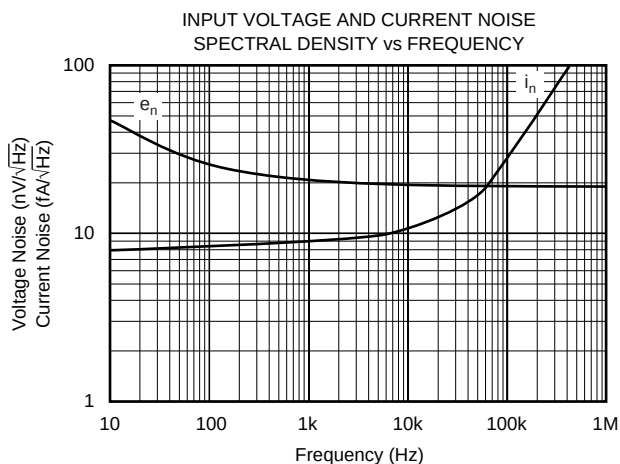
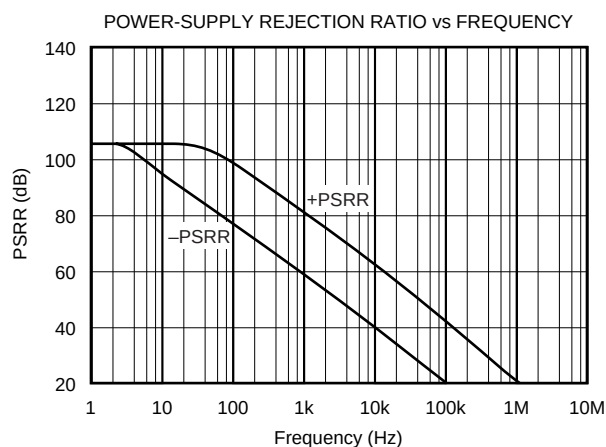
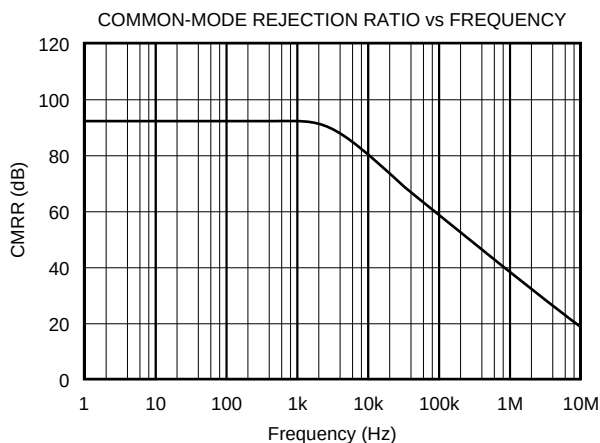
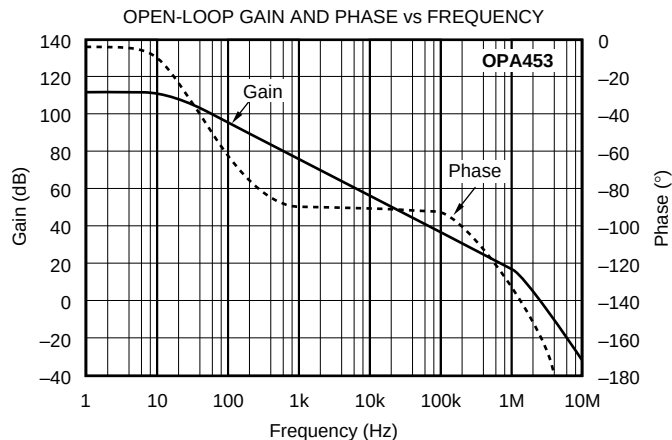
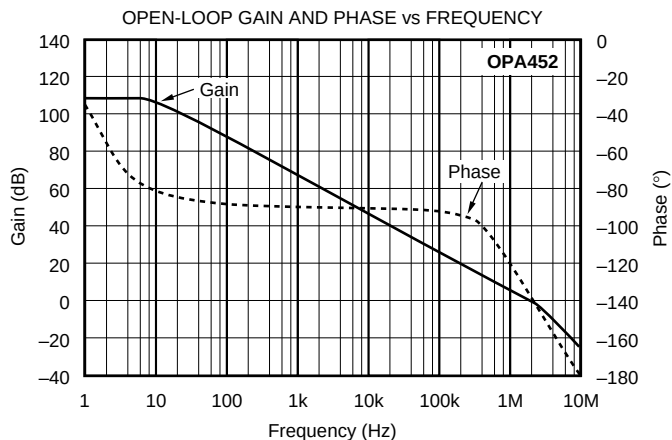
PARAMETER	CONDITION	OPA453TA, FA			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage over Temperature Drift vs Power Supply over Temperature	V_{OS} dV_{OS}/dT PSRR $V_S = \pm 40V, V_{CM} = 0V, I_O = 0V$ $V_S = \pm 10V$ to $\pm 40V, V_{CM} = 0V$		± 1 ± 5 5	± 3 ± 6 30 45	mV mV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$
INPUT BIAS CURRENT ⁽¹⁾ Input Bias Current Input Offset Current	I_B I_{OS} $V_S = \pm 40V, V_{CM} = 0V$ $V_S = \pm 40V, V_{CM} = 0V$		± 7 ± 1	± 100 ± 100	pA pA
NOISE Input Voltage Noise Density Current Noise Density	e_n i_n $f = 1kHz$ $f = 1kHz$		21 9		$nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio over Temperature	V_{CM} CMRR $V_S = \pm 40V, -35V < V_{CM} < 39.5V$ $V_S = \pm 40V, -35V < V_{CM} < 39.5V$	$(V-) + 5$ 86 76	94	$(V+) - 0.5$	V dB dB
INPUT IMPEDANCE Differential Common-Mode	$V_S = \pm 40V, -35V < V_{CM} < 39.5V$		$10^{13} \parallel 2$ $10^{13} \parallel 6$		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain over Temperature over Temperature	A_{OL} $I_O = 10mA, -V_S + 2V < V_O < +V_S - 2V$ $I_O = 10mA, -V_S + 2V < V_O < +V_S - 2V$ $I_O = 50mA, -V_S + 4V < V_O < +V_S - 4V$ $I_O = 50mA, -V_S + 5V < V_O < +V_S - 5.5V$	105 96	110 107 110 105		dB dB dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise	GBW SR THD+N $V_S = \pm 40V$ $V_S = \pm 40V$ $V_S = \pm 40V, G = +5, 10V$ Step, $C_L = 100pF$ $V_S = \pm 40V, G = +5, 10V$ Step, $C_L = 100pF$ $V_{IN} \cdot \text{Gain} = V_S$ $V_S = \pm 40V, V_O = 30Vp-p, G = 5$ $f = 1kHz, R_L = 2k\Omega$		7.5 +23/-38 1 1.5 1 0.0008		MHz V/ μs μs μs μs %
OUTPUT Voltage Output over Temperature Voltage Output over Temperature Output Current Short-Circuit Current Capacitive Load Drive	V_{OUT} I_{SC} C_{LOAD} $I_O = 50mA$ $I_O = 50mA$ $I_O = 10mA$ $I_O = 10mA$	$(V-) + 4.0$ $(V-) + 5$ $(V-) + 2$ $(V-) + 2$ ± 50	± 125 See Typical Characteristic	$(V+) - 4$ $(V+) - 5.5$ $(V+) - 2$ $(V+) - 2$	V V V V mA mA
SHUTDOWN FLAG Thermal Shutdown Status Output Normal Operation Thermally Shutdown Junction Temperature Shutdown Reset from Shutdown	$V_S = \pm 40V$ $V_S = \pm 40V$	100	0.1 140 +160 +145	1.0 165	μA μA $^{\circ}C$ $^{\circ}C$
POWER SUPPLY Supply Voltage Range Quiescent Current (per amplifier) over Temperature	V_S I_Q $I_O = 0$	± 10	± 5.5	± 40 ± 6.5 ± 7.5	V mA mA
TEMPERATURE RANGE Specified Range (junction) Operating Range (junction) Storage Range (ambient) Thermal Resistance TO200-7 DDPAK-7	T_J T_J T_A θ_{JC} 	-40 -55 -65		+125 +125 +150	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$

NOTE: (1) All tests are high-speed tested at $+25^{\circ}C$ ambient temperature. Effective junction temperature is $+25^{\circ}C$, unless otherwise noted.

TYPICAL CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, and $R_L = 3.8\text{k}\Omega$, unless otherwise noted.

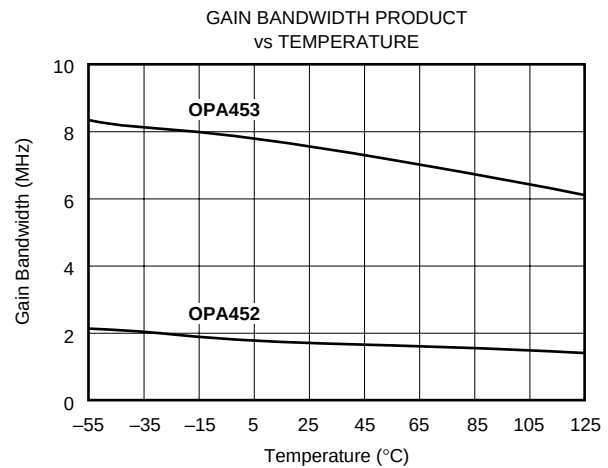
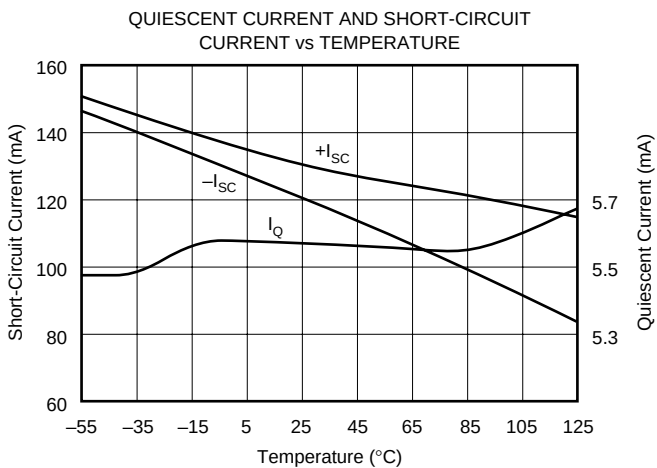
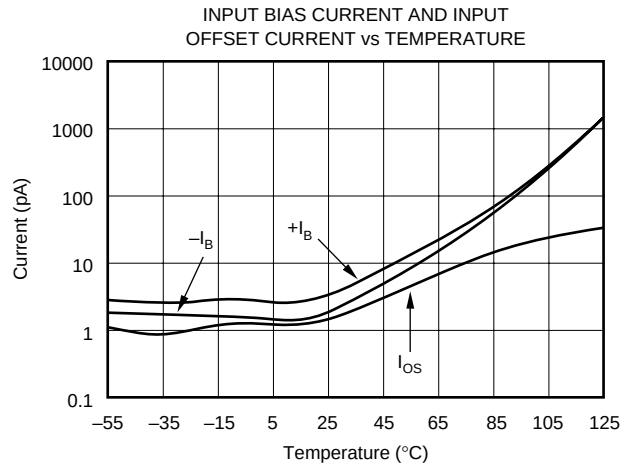
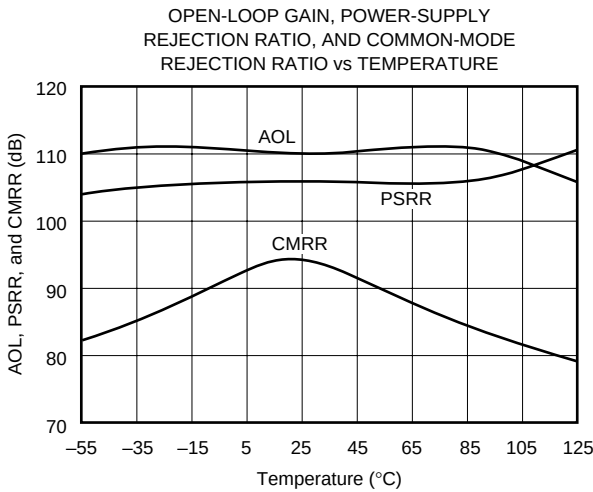
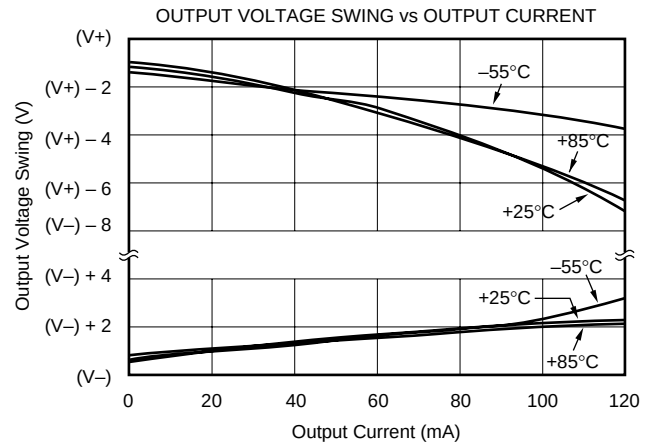
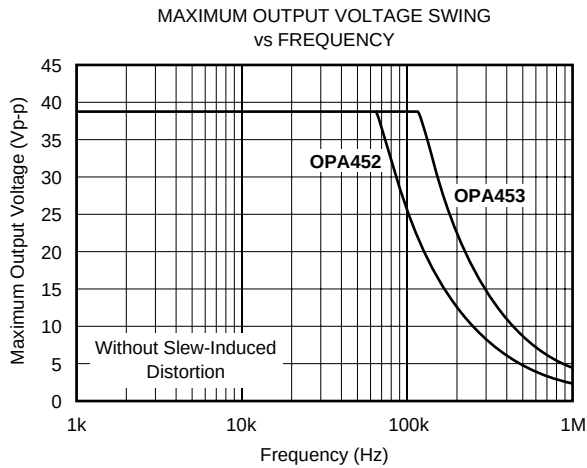
All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.



TYPICAL CHARACTERISTICS (Cont.)

At $T_J = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, and $R_L = 3.8\text{k}\Omega$, unless otherwise noted.

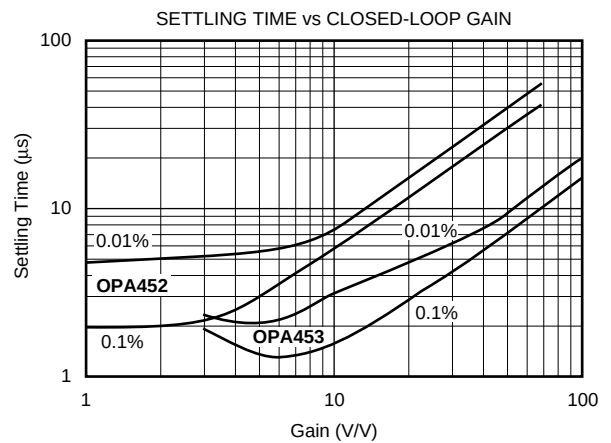
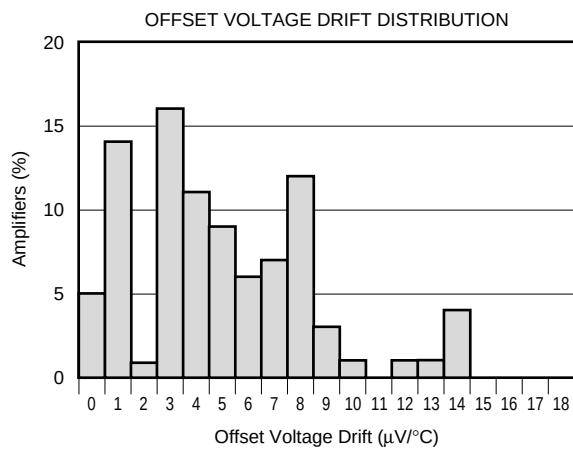
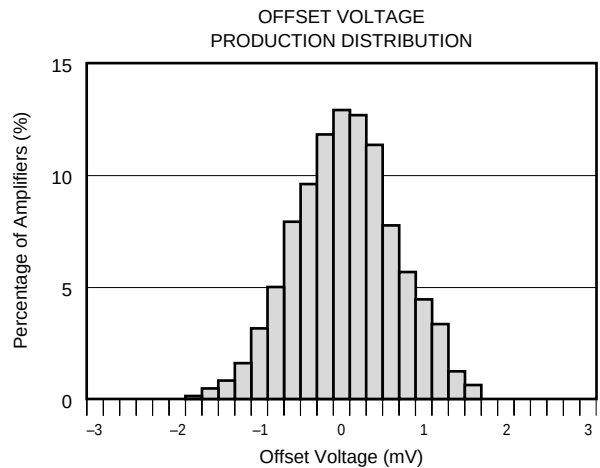
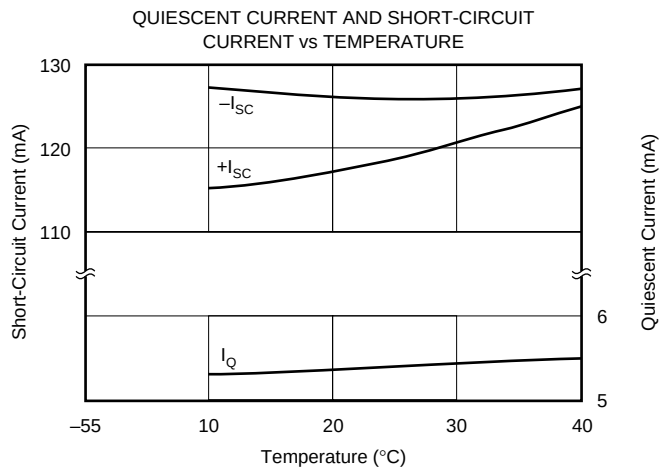
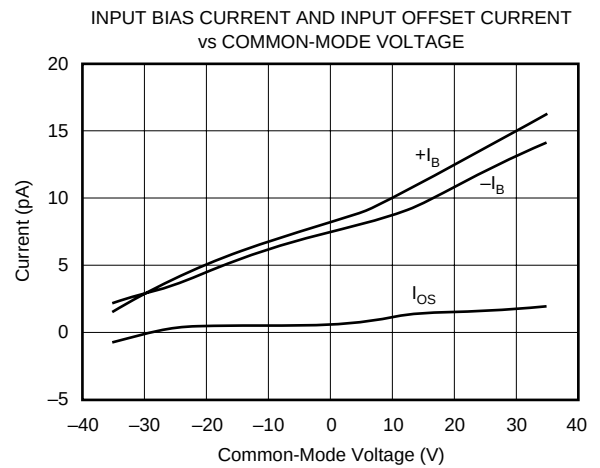
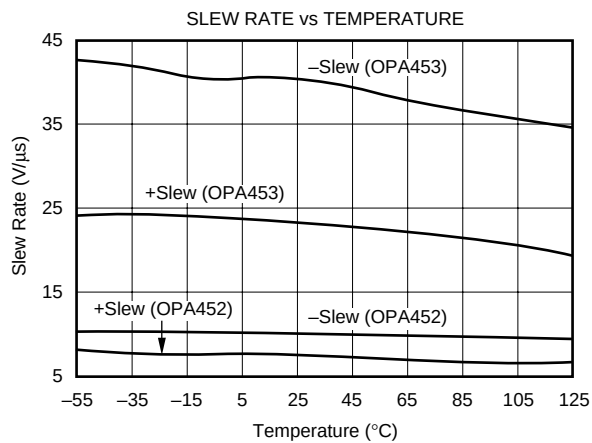
All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.



TYPICAL CHARACTERISTICS (Cont.)

At $T_J = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, and $R_L = 3.8\text{k}\Omega$, unless otherwise noted.

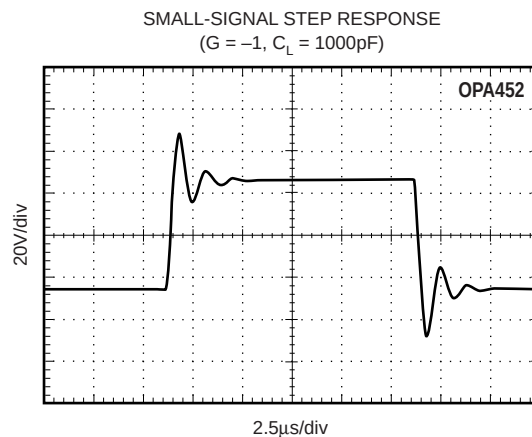
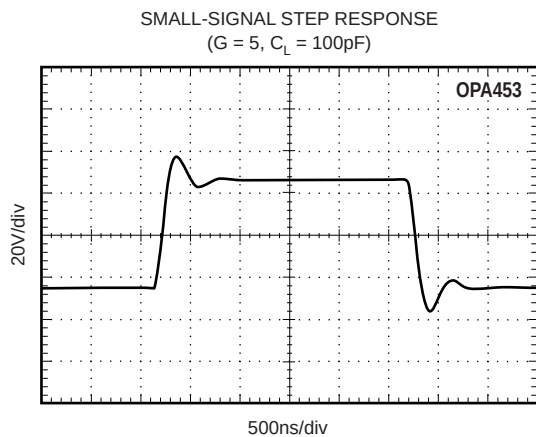
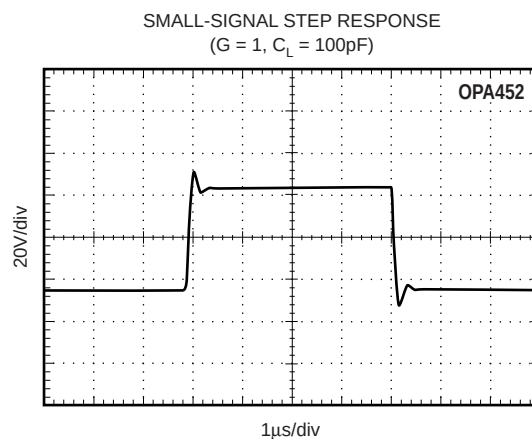
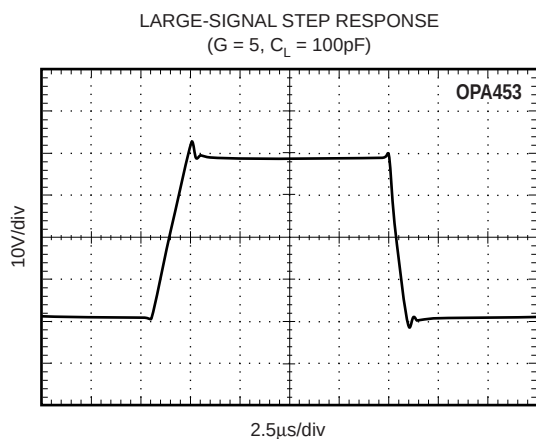
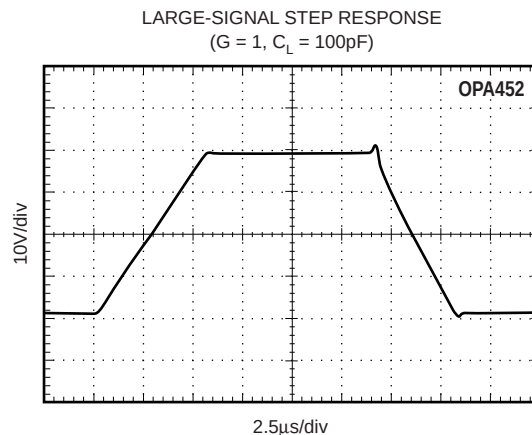
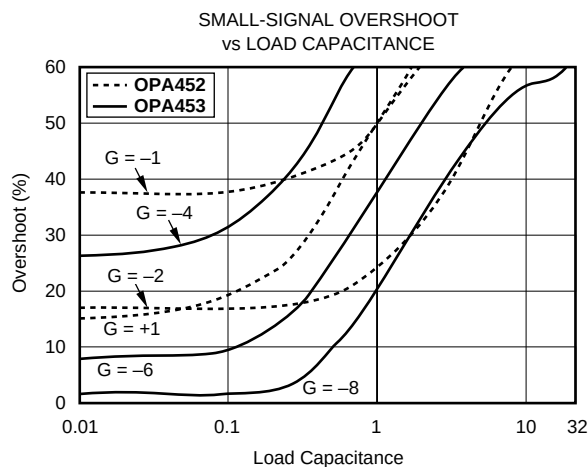
All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.



TYPICAL CHARACTERISTICS (Cont.)

At $T_J = +25^\circ\text{C}$, $V_S = \pm 40\text{V}$, and $R_L = 3.8\text{k}\Omega$, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.



APPLICATIONS INFORMATION

Figure 1 shows the OPA452 connected as a basic noninverting amplifier. The OPA452 can be used in virtually any op amp configuration. The OPA453 is designed for use in configurations with gains of 5 or greater. Power-supply terminals should be bypassed with 0.1µF capacitors, or greater, near the power-supply pins. Be sure that the capacitors are appropriately rated for the power-supply voltage used. The OPA452 and OPA453 can supply output currents up to 50mA with excellent performance.

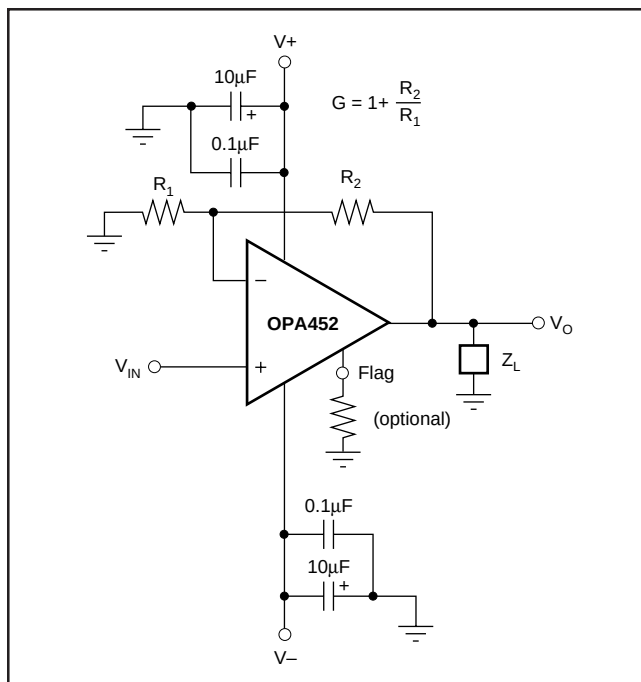


FIGURE 1. Basic Circuit Connections.

CURRENT LIMIT

The OPA452 and OPA453 are designed with internal current-limiting circuitry that limits the output current to approximately 125mA. The current limit varies slightly with increasing junction temperature and supply voltage, as shown in the Typical Characteristics. Current limit, in combination with the thermal protection circuitry, provides protection from most types of overload conditions including short-circuit to ground.

THERMAL PROTECTION

The OPA452 and OPA453 have thermal shutdown circuitry that protects the amplifier from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled.

The thermal shutdown function is not intended to replace proper heat sinking. Activation of the thermal shutdown circuitry is an indication of excessive power dissipation or an inadequate heat sink. Continuously running the amplifier into thermal shutdown can degrade reliability.

The Thermal Shutdown Indicator (Flag) pin can be monitored to determine if shutdown is occurring. During normal operation, the current output from the flag pin is typically 50nA. During shutdown, the current output from the flag pin increases to 140µA (typical). This current output allows for easy interfacing to external logic. Figure 2 shows two examples implementing this function.

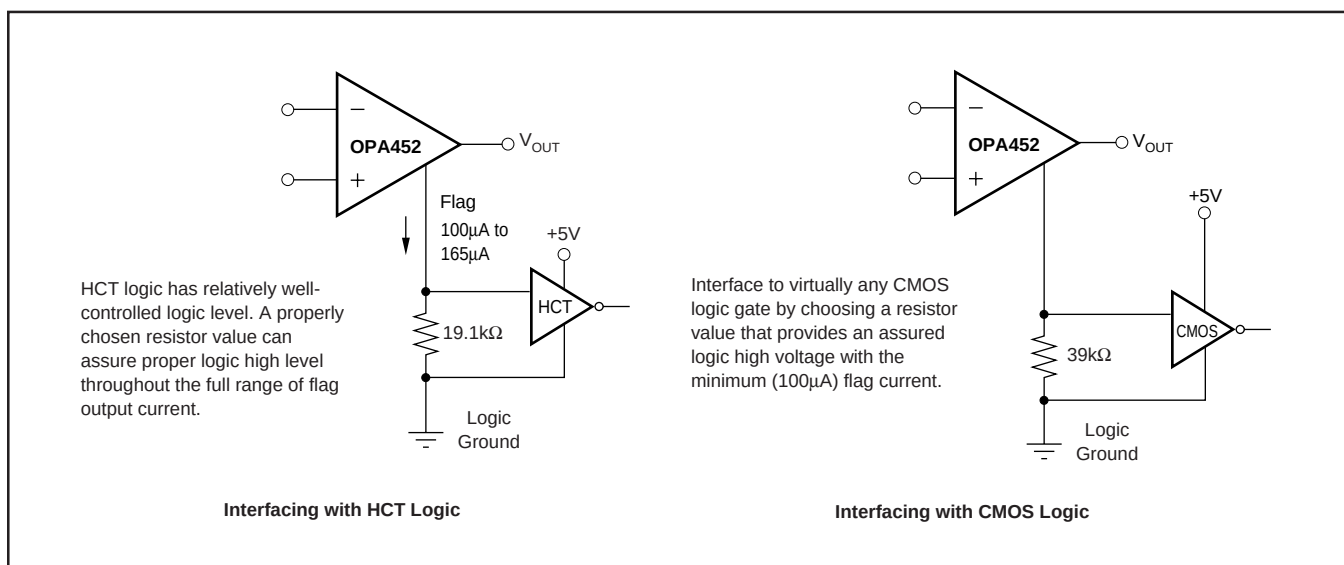


FIGURE 2. Thermal Shutdown Indicator.

POWER SUPPLIES

The OPA452 and OPA453 may be operated from power supplies of $\pm 10\text{V}$ to $\pm 40\text{V}$, or a total of 80V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics.

For applications that do not require symmetrical output voltage swing, power-supply voltages do not need to be equal. The OPA452 and OPA453 can operate with as little as 20V between the supplies or with up to 80V between the supplies. For example, the positive supply could be set to 70V with the negative supply at -10V or vice-versa.

The tabs of the DDPK-7 and TO220 packages are electrically connected to the negative supply (V_-), however, these connections should not be used to carry current. For best thermal performance, the tab should be soldered directly to the circuit board copper area (see Heat Sinking section).

POWER DISSIPATION

Internal power dissipation of these op amps can be quite large. All of the specifications for the OPA452 and OPA453 may change with junction temperature. If the device is not subjected to internal self-heating, the junction temperature will be the same as the ambient. However, in practical applications, the device will self-heat and the junction temperature will be significantly higher than ambient. The following calculation can be performed to establish junction temperature as a function of ambient temperature and the conditions of the application.

Consider the OPA452 in a circuit configuration where the load is 600Ω and the output voltage is 20V . The supplies are at $\pm 40\text{V}$ and the ambient temperature (T_A) is 40°C . The θ_{JA} for the package plus heat sink is 30°C/W .

First, the quiescent heating of the op amp is as follows:

$$P_{D(\text{internal})} = I_Q \cdot V_S = 6\text{mA} \cdot 80\text{V} = 480\text{mW}$$

The output current (I_O) can be calculated:

$$I_O = V_O / R_L = 20\text{V} / 600\Omega = 33.33\text{mA}$$

The power being dissipated (P_D) in the output transistor of the amplifier can be calculated:

$$P_{D(\text{output stage})} = I_O \cdot (V_S - V_O) = 33.3\text{mA} \cdot (40 - 20) = 667\text{mW}$$

$$P_{D(\text{total})} = P_{D(\text{internal})} + P_{D(\text{output stage})} = 480\text{mW} + 667\text{mW} = 1147\text{mW}$$

The resulting junction temperature can be calculated:

$$T_J = T_A + P_D \theta_{JA}$$

$$T_J = 40^\circ\text{C} + 1147\text{mW} \cdot 30^\circ\text{C/W} = 74.4^\circ\text{C}$$

Where,

V_O = output voltage

V_S = supply voltage

I_O = output current

R_L = load resistance

T_J = junction temperature ($^\circ\text{C}$)

T_A = ambient temperature ($^\circ\text{C}$)

θ_{JA} = junction-to-air thermal resistance ($^\circ\text{C/W}$)

To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than $+35^\circ\text{C}$ above the maximum expected ambient condition of your application. This ensures a maximum junction temperature of $+125^\circ\text{C}$ at the maximum expected ambient condition.

Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation because a larger voltage can be impressed across the conducting output transistor. Consult Application Bulletin SBOA022 at www.ti.com for further information on how to calculate or measure power dissipation.

Power dissipation can be minimized by using the lowest possible supply voltage. For example, with a 50mA load, the output will swing to within 5.0V of the power-supply rails. Power supplies set to no more than 5.0V above the maximum output voltage swing required by the application will minimize the power dissipation.

SAFE OPERATING AREA

The Safe Operating Area (SOA curves, Figure 3) shows the permissible range of voltage and current. The safe output current decreases as the voltage across the output transistor ($V_S - V_O$) increases. For further insight on SOA, consult Application Report SBOA022.

Output short circuits are a very demanding case for SOA. A short-circuit to ground forces the full power-supply voltage (V_+ or V_-) across the conducting transistor and produces a

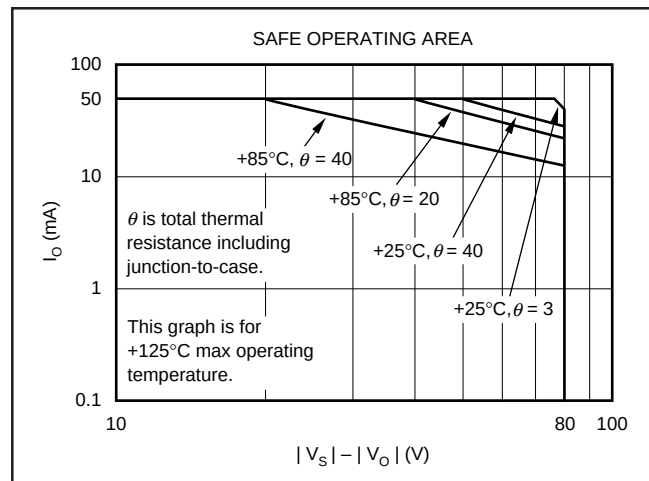


FIGURE 3. DDPK-7 and TO220-7 Safe Operating Area.

typical output current of 125mA. With $\pm 40\text{V}$ power supplies, this creates an internal dissipation of 10W. This far exceeds practical heat sinking and is not recommended. If operation in this region is unavoidable, use the part with a heat sink.

HEAT SINKING

Power dissipated in the OPA452 or OPA453 will cause the junction temperature to rise. For reliable operation, the junction temperature should be limited to $+125^{\circ}\text{C}$. Many applications will require a heat sink to assure that the maximum operating junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions.

For heat sinking purposes, the tab of the DDPAK is typically soldered directly to a circuit board copper area. Increasing the copper area improves heat dissipation. Figure 4 shows typical thermal resistance from junction-to-ambient as a function of copper area.

Depending on conditions, additional heat sinking may be required. Aavid Thermal Products Inc. manufactures surface-mountable heat sinks designed specifically for use with these packages. Further information is available on Aavid's web site, www.aavid.com.

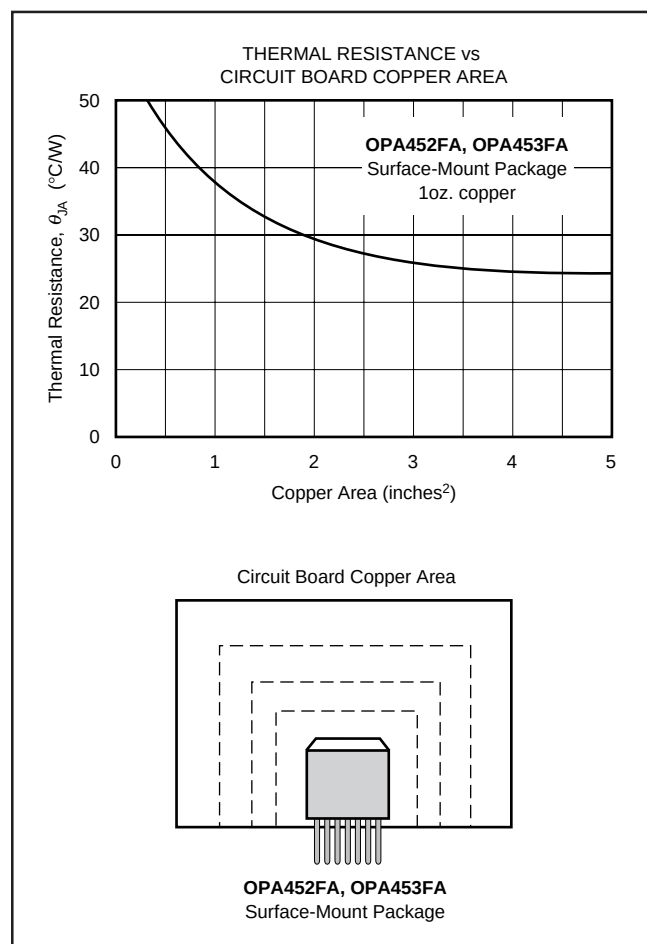


FIGURE 4. DDPAK Thermal Resistance versus Circuit Board Copper Area.

CAPACITIVE LOADS

The dynamic characteristics of the OPA452 and OPA453 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Figure 5 shows a circuit that preserves phase margin with capacitive load. Figure 6 shows the small-signal step response for the circuit in Figure 5. Consult Application Bulletin SBOA015, at www.ti.com, for more information.

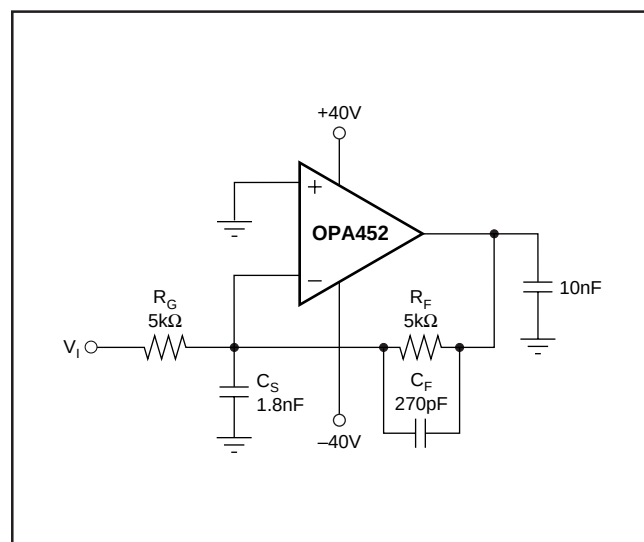


FIGURE 5. Driving Large Capacitive Loads.

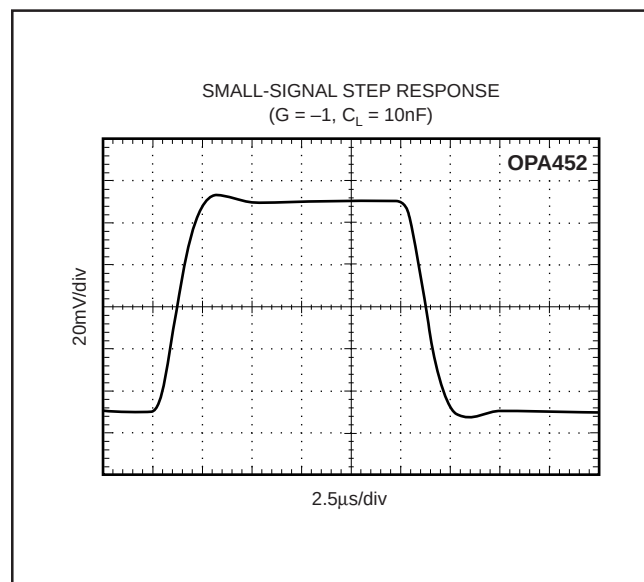


FIGURE 6. Small-Signal Step Response for Figure 5.

INCREASING OUTPUT CURRENT

In those applications where the 50mA of output current is not sufficient to drive the desired load, output current can be increased by connecting two or more OPA452s or OPA453s in parallel, as shown in Figure 7. Amplifier A1 is the master amplifier and may be configured in virtually any op amp circuit. Amplifier A2, the slave, is configured as a unity gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 8 is capable of supplying output currents up to 1A. Alternatively, the OPA547, OPA548, and OPA549 series power op amps should be considered for high output current drive, along with programmable current limit and output disable capability.

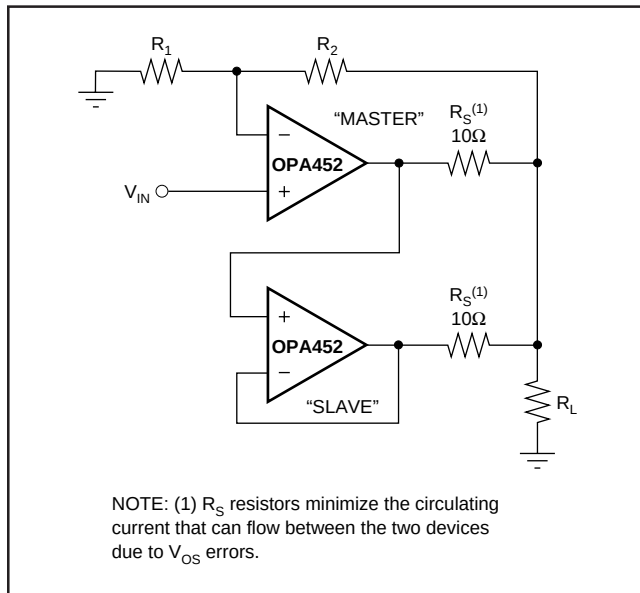


FIGURE 7. Parallel Amplifiers Increase Output Current Capability.

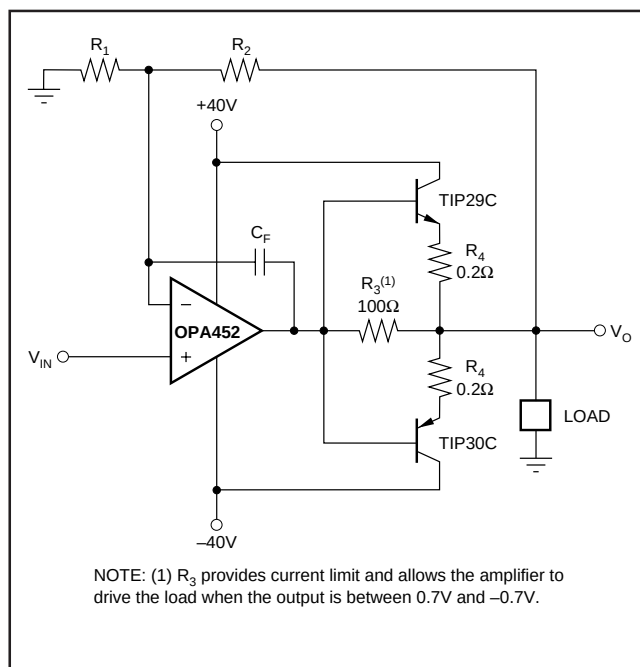


FIGURE 8. External Output Transistors Boost Output Current Up to 1 Amp.

INPUT PROTECTION

The OPA452 and OPA453 feature internal clamp diodes to protect the inputs when voltages beyond the supply rails are encountered. However, input current should be limited to 5mA. In some cases, an external series resistor may be required. Many input signals are inherently current-limited, therefore, a limiting resistor may not be required. Please consider that a large series resistor, in conjunction with the input capacitance, can affect stability.

USING THE OPA453 IN LOW GAINS

The OPA453 is intended for applications with signal gains of 5 or greater, but it is possible to take advantage of its high slew rate in lower gains using an external compensation technique in an inverting configuration. This technique maintains low noise characteristics of the OPA453 architecture at low frequencies. Depending on the application, a small increase in high-frequency noise may result. This technique shapes the loop gain for good stability while giving an easily controlled 2nd-order low-pass frequency response.

Considering only the noise gain (noninverting signal gain) for the circuit of Figure 9, the low-frequency noise gain (NG_1) will be set by the resistor ratios, whereas the high-frequency noise gain (NG_2) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain, determined by $NG_2 = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp and the noise gain pole, set by $1/R_F C_F$, is placed correctly, a very well controlled, 2nd-order low-pass frequency response will result.

To choose the values for both C_S and C_F , two parameters and only three equations need to be solved. First, the target for the high-frequency noise gain (NG_2) should be greater than the minimum stable gain for the OPA453. In the circuit in Figure 9, a target NG_2 of 10 is used. Second, the signal gain of -1 in Figure 10 sets the low-frequency noise gain to $NG_1 = 1 + R_F/R_G (= 2$ in this example). Using these two gains, knowing the Gain Bandwidth Product (GBP) for the OPA453 (7.5MHz), and targeting a maximally flat 2nd-order, low-pass Butterworth frequency response ($Q = 0.707$), the key frequency in the compensation can be found.

For the values in Figure 9, the f_{-3dB} will be approximately 180kHz. This is less than that predicted by simply dividing the GBP by NG_1 . The compensation network controls the bandwidth to a lower value while providing good slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \cdot Z_0$. The capacitor values in Figure 10 are calculated for $NG_1 = 2$ and $NG_2 = 10$ with no adjustment for parasitics.

Actual circuit values can be optimized by checking the small-signal step response with actual load conditions. See Figure 9 for the small-signal step response of this OPA453, $G = -1$ circuit with a 1000pF load. It is well-behaved with no tendency to oscillate. If C_S and C_F were removed, the circuit would be unstable.

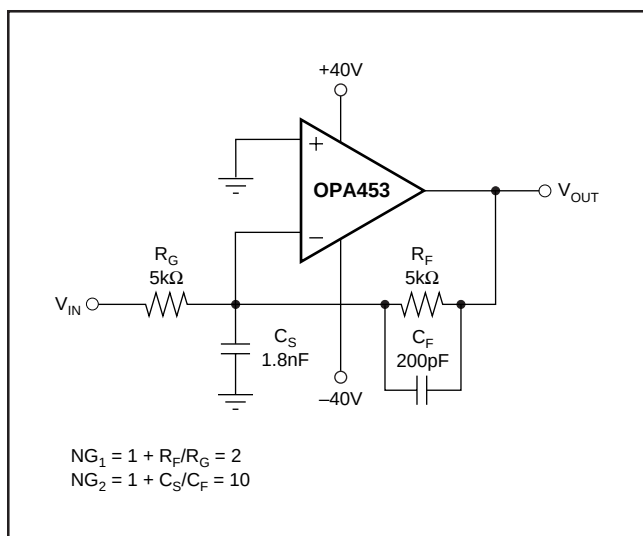


FIGURE 9. Compensation of the OPA453 for $G = -1$.

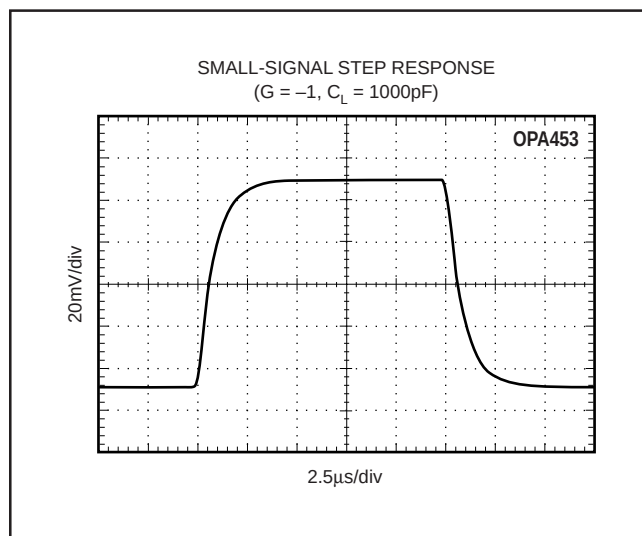


FIGURE 10. Small-Signal Step Response for Figure 9.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA452FA/500	Active	Production	DDPAK/TO-263 (KTW) 7	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	OPA452F
OPA452FA/500.A	Active	Production	DDPAK/TO-263 (KTW) 7	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	OPA452F
OPA452FAKTWT	Active	Production	DDPAK/TO-263 (KTW) 7	250 SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	OPA452F
OPA452FAKTWT.A	Active	Production	DDPAK/TO-263 (KTW) 7	250 SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	OPA452F
OPA453FAKTWT	Active	Production	DDPAK/TO-263 (KTW) 7	250 SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	OPA453F
OPA453FAKTWT.A	Active	Production	DDPAK/TO-263 (KTW) 7	250 SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	OPA453F
OPA453TA	Active	Production	TO-220 (KC) 7	50 TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	OPA453T
OPA453TA-1	Active	Production	TO-220 (KVT) 7	50 TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	OPA453T
OPA453TA-1.A	Active	Production	TO-220 (KVT) 7	50 TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	OPA453T
OPA453TA.A	Active	Production	TO-220 (KC) 7	50 TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	OPA453T

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

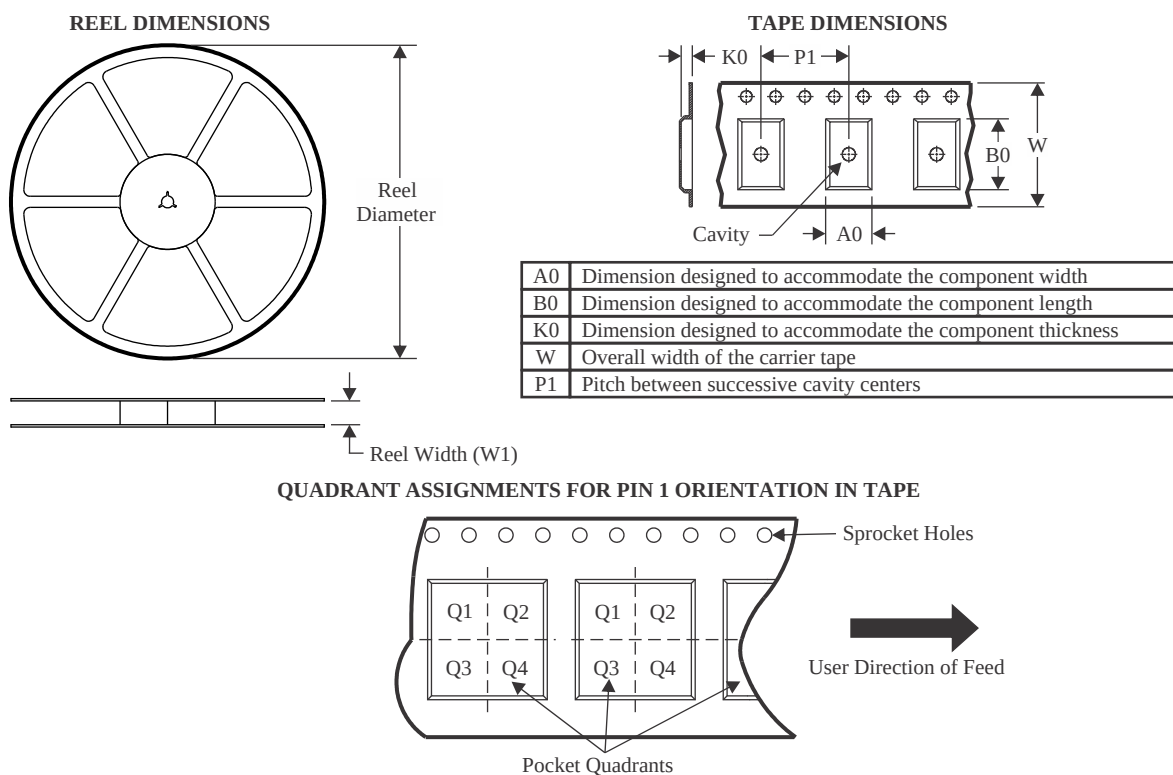
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

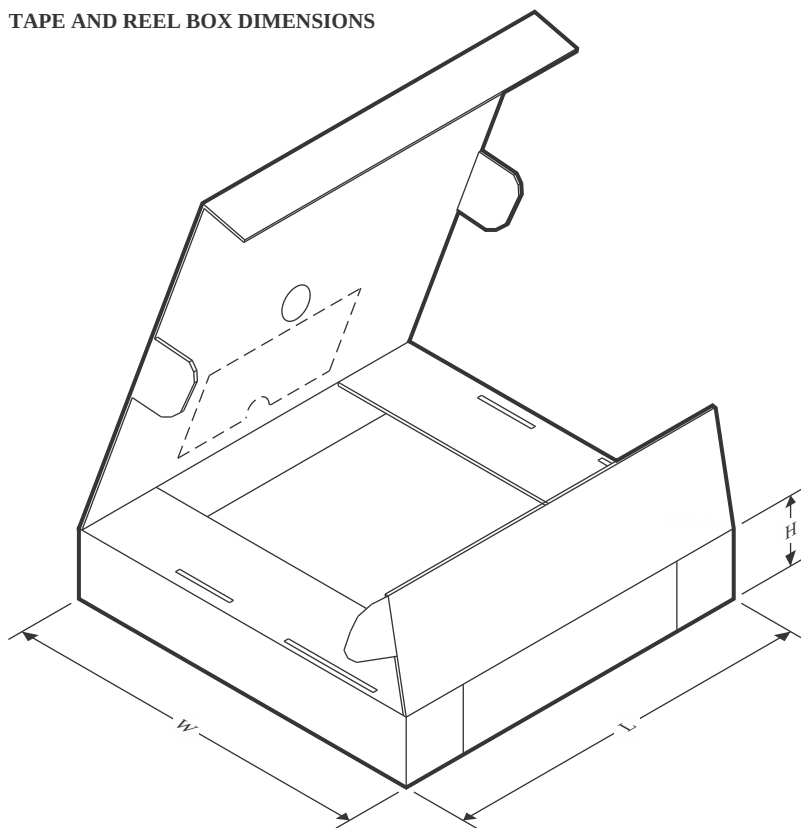
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA452FA/500	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
OPA452FAKTWT	DDPAK/ TO-263	KTW	7	250	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
OPA453FAKTWT	DDPAK/ TO-263	KTW	7	250	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2

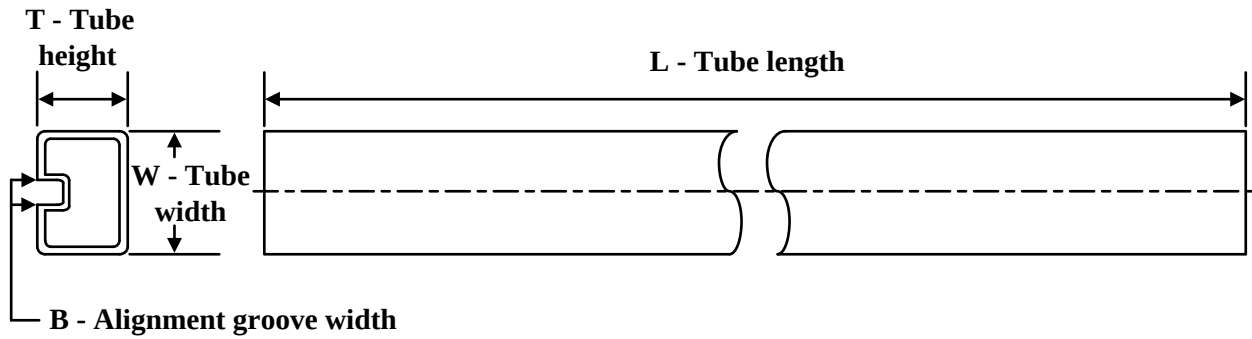
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA452FA/500	DDPAK/TO-263	KTW	7	500	356.0	356.0	45.0
OPA452FAKTWT	DDPAK/TO-263	KTW	7	250	356.0	356.0	45.0
OPA453FAKTWT	DDPAK/TO-263	KTW	7	250	356.0	356.0	45.0

TUBE

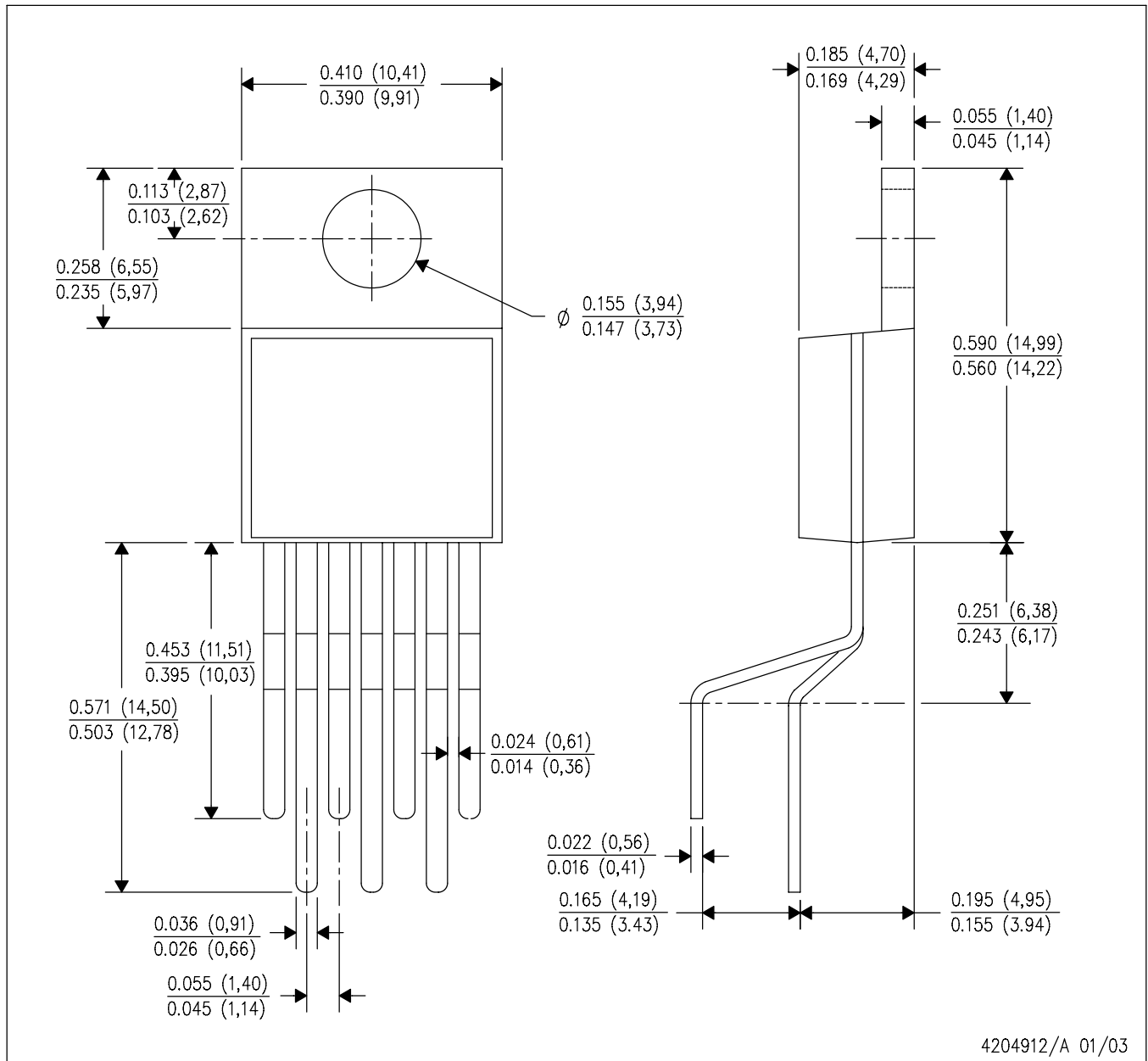


*All dimensions are nominal

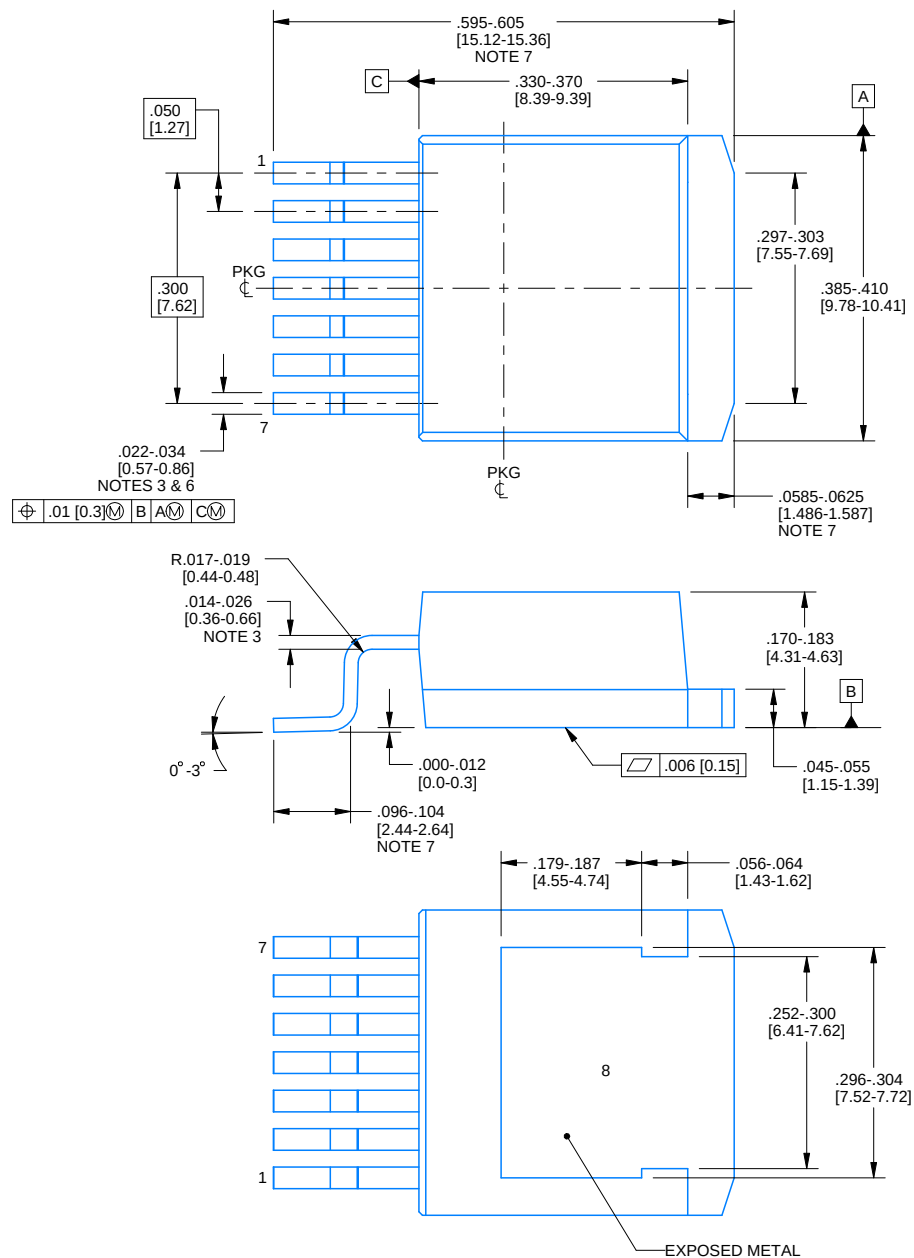
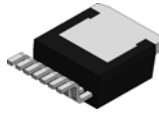
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA453TA	KC	TO-220	7	50	532.13	34.54	13340	NA
OPA453TA-1	KVT	TO-220	7	50	532.13	34.54	13340	NA
OPA453TA-1.A	KVT	TO-220	7	50	532.13	34.54	13340	NA
OPA453TA.A	KC	TO-220	7	50	532.13	34.54	13340	NA

KVT (R-PZFM-T7)

PLASTIC FLANGE MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.



4232469/A 11/2025

NOTES:

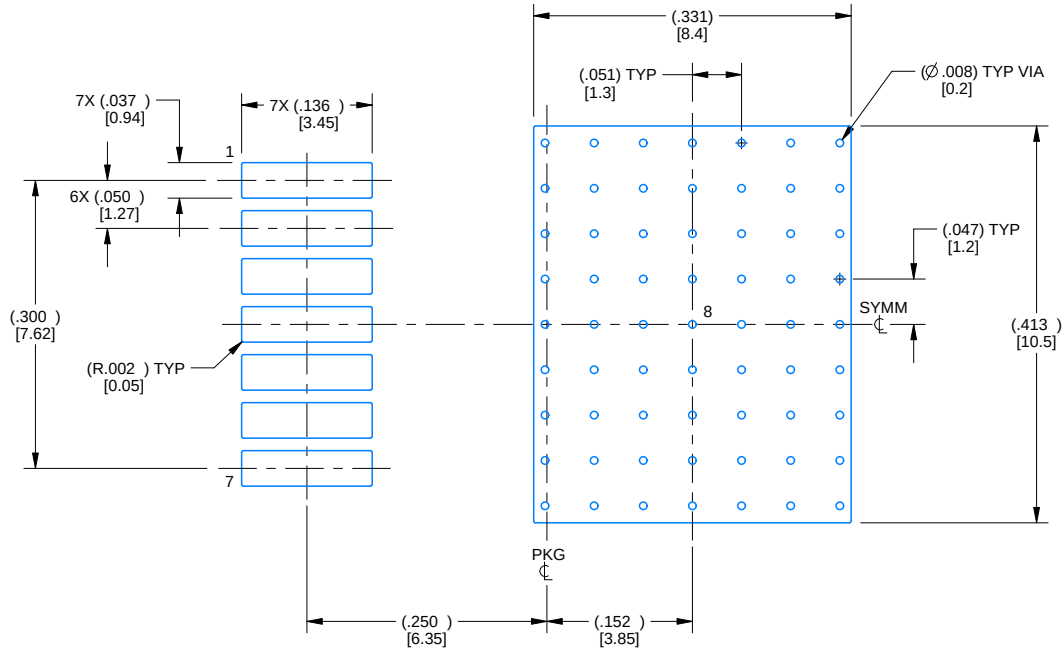
1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead width and height dimensions apply to the plated lead.
4. Leads are not allowed above the Datum B.
5. Stand-off height is measured from lead tip with reference to Datum B.
6. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003".
7. Falls within JEDEC MO-169 with the exception of the dimensions indicated.

EXAMPLE BOARD LAYOUT

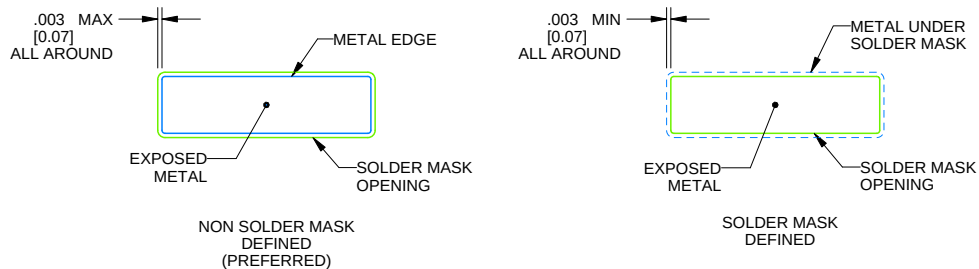
KTW0007A

TO-263 - 5 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 5X



SOLDER MASK DETAILS

4232469/A 11/2025

NOTES: (continued)

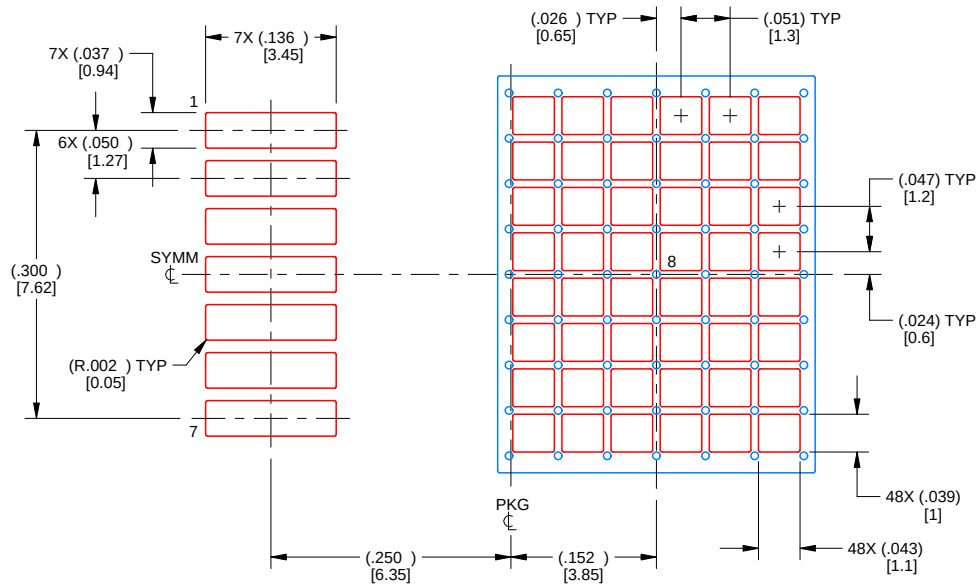
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTW0007A

TO-263 - 5 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 5X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 8: 60%

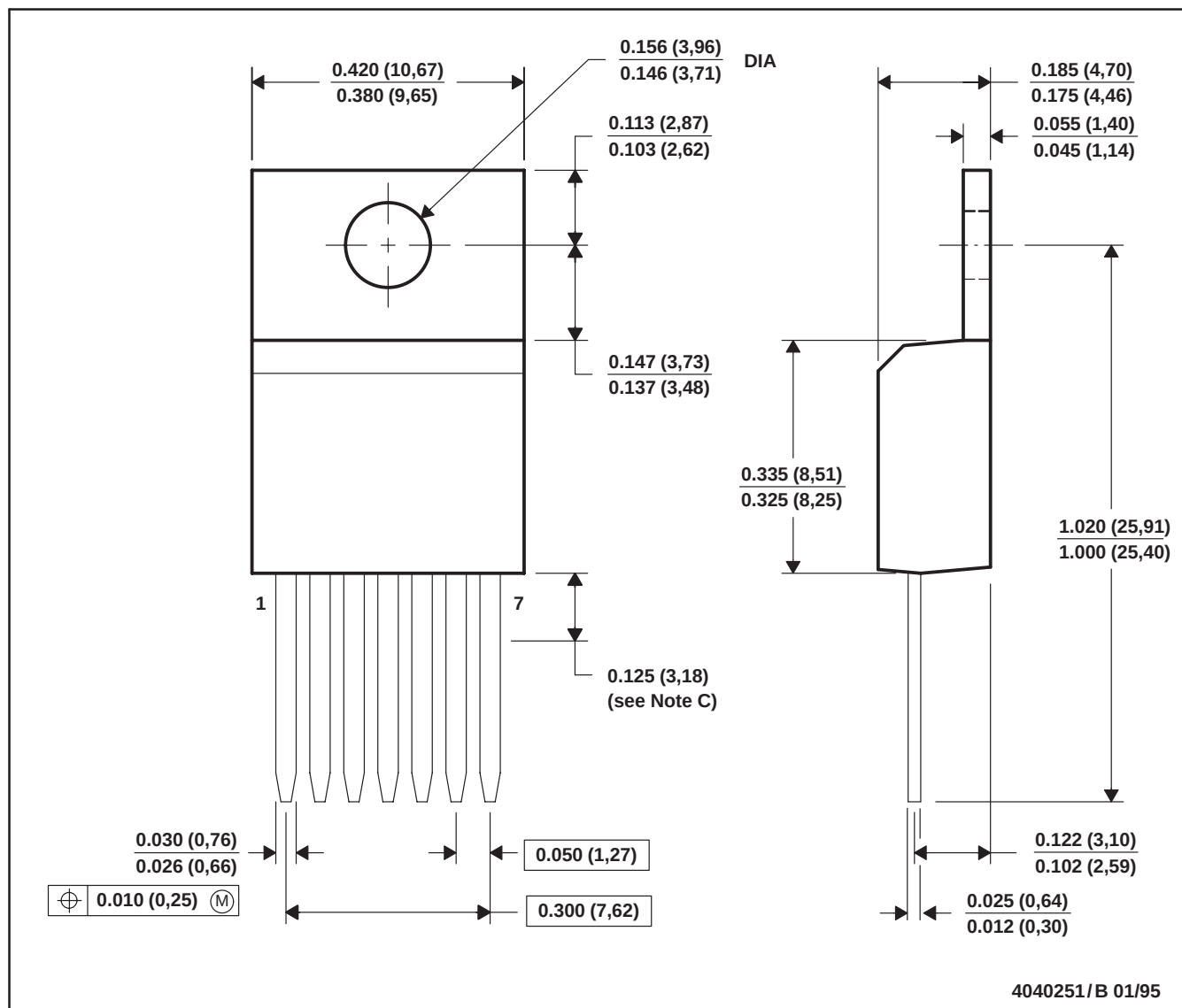
4232469/A 11/2025

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

KC (R-PSFM-T7)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Lead dimensions are not controlled within this area.
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025