OPA4H838-SEP Precision, Zero-Drift, Zero-Crossover, True Rail-to-Rail Input, Output Operational Amplifier

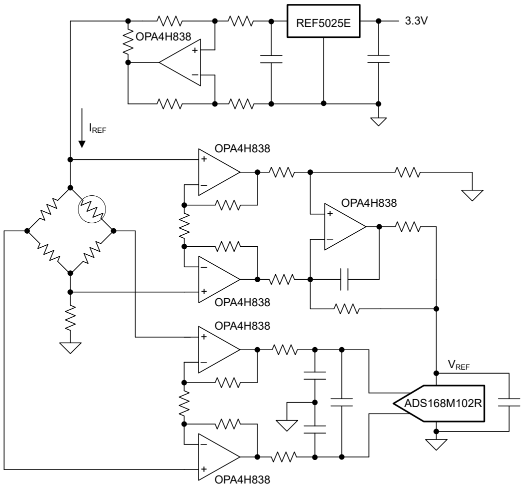
1 Features

- Radiation tolerant
  - Single event latch-up (SEL) immune to 43MeV-cm^2/mg at 125°C
  - ELDRS free to 30krad(Si)
  - Total Ionizing Dose (TID) RLAT for every wafer lot up to 30krad(Si)
- Supports defense and aerospace applications
  - Controlled baseline
  - One fabrication, assembly, and test site
  - Extended product life cycle
  - Product traceability
  - Outgassing test performed per ASTM E595

- Ultra-low offset voltage: ±0.25μV
- Zero drift: ±0.01μV/°C
- Zero crossover: 140dB CMRR true RRIO
- Low noise: $7.0nV\sqrt{Hz}$ at 1kHz
- No 1/f noise: 140nV$_{PP}$ (0.1Hz to 10Hz)
- Fast settling: 2μs (1V to 0.01%)
- Gain bandwidth: 10MHz
- Supply voltage: ±1.25V to ±2.75V, 2.5V to 5.5V
- True rail-to-rail input and output
- EMI/RFI filtered inputs

2 Applications

- Satellite health monitoring and telemetry
- Scientific exploration payload
- Altitude and orbit control system (AOCS)
- Satellite electrical power system (EPS)
- Communications payload
- Radar imaging payload



The OPA4H838-SEP in a Bridge Sensor Front End

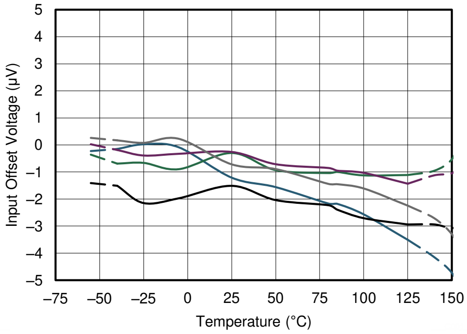
3 Description

The OPA4H838-SEP precision amplifier is an ultra-low noise, fast-settling, zero-drift, zero-crossover device that provides rail-to-rail input and output operation. These features and excellent ac performance, combined with only 0.25μV of offset and 0.01μV/°C of drift over temperature, makes the OPA4H838-SEP a great choice for driving high-precision, analog-to-digital converters (ADCs) or buffering the output of high-resolution, digital-to-analog converters (DACs). This design results in excellent performance when driving analog-to-digital converters (ADCs) without degradation of linearity. The OPA4H838-SEP is offered in a TSSOP-14 package. The OPA4H838-SEP is specified from –55°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
OPA4H838-SEP	PW (TSSOP, 14)	5mm × 6.4mm

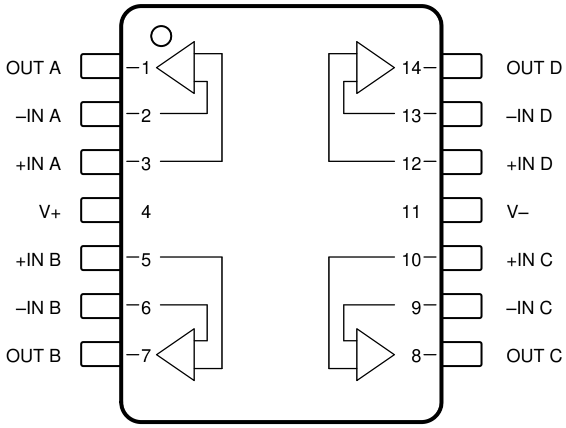
(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable



Ultra-Low Offset Voltage Drift

Table of Contents

4 Pin Configuration and Functions



Not to scale

Figure 4-1. OPA4H838-SEP PW Package, 14-Pin TSSOP-14 (Top View)

Table 4-1. Pin Functions: OPA4H838-SEP

PIN		TYPE[1]	DESCRIPTION
NAME	**PW (TSSOP)**		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

1. I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current[3]			±10	mA
Output short circuit[2]			Continuous	Continuous	
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Currents on input signal pins exceeding absolute maximum rating may increase the risk of latch-up. External current-limiting protection is required.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single-supply	2.5		5.5	V
	Dual-supply	±1.25		±2.75	
Specified temperature		–55		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		OPA4H838-SEP	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: V_S = ±1.25 V to ±2.75 V (V_S = 2.5 to 5.5 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5.5 V			±2.25	±10.5	µV
V_{OS}	Input offset voltage	T_A = –55°C to +125°C, V_S = 5.5 V(1)				±11	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –55°C to +125°C, V_S = 5.5 V(1)			±0.01	±0.05	µV/°C
PSRR	Power-supply rejection ratio	T_A = –55°C to +125°C(1)			±1.25	±3.5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	R_{IN} = 100 kΩ			±30	±1000	pA
			T_A = -55°C to +125°C(1)			±1000	
I_{OS}	Input offset current	R_{IN} = 100 kΩ				±1000	
			T_A = –55°C to +125°C(1)			±1100	
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			0.14		$µV_{PP}$
e_N	Input voltage noise density	f = 10 Hz			7		nV/√Hz
		f = 100 Hz			7		
		f = 1 kHz			7		
		f = 10 kHz			7		
I_N	Input current noise density	f = 1 kHz			100		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	V_S = ±1.25 V	102	110		dB
			V_S = ±2.75 V	124	140		
		(V–) < V_{CM} < (V+) + 0.1 V, T_A = –55°C to +125°C(1)	V_S = ±1.25 V	102	107		
		(V–) – 0.05 V < V_{CM} < (V+) + 0.1 V, T_A = –55°C to +125°C(1)	V_S = ±2.75 V	124	140		
INPUT IMPEDANCE							
z_{id}	Differential input impedance				100 || 2		MΩ || pF
z_{ic}	Common-mode input impedance				60 || 4.5		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		126	148		dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ, V_S = 5.5 V T_A = –55°C to +125°C(1)		120	126		
		(V–) + 0.25 V < V_O < (V+) – 0.25 V, R_{LOAD} = 2 kΩ		126	148		
		(V–) + 0.30 V < V_O < (V+) – 0.30 V, R_{LOAD} = 2 kΩ, V_S = 5.5 V T_A = –55°C to +125°C(1)		120	126		
FREQUENCY RESPONSE							
GBW	Unity-gain bandwidth				10		MHz
SR	Slew rate	G = 1, 4 V step			5		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 1 V_{RMS}			0.0005%		
t_S	Settling time	To 0.1%	V_S = ±2.5 V, G = 1, 1-V step		0.75		µs
		To 0.01%	V_S = ±2.5 V, G = 1, 1-V step		2		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			10		µs
OUTPUT							

5.5 Electrical Characteristics: V_S = ±1.25 V to ±2.75 V (V_S = 2.5 to 5.5 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output swing from rail	Positive rail	No load		1	17	mV
			R_{LOAD} = 10 kΩ		5	20	
			R_{LOAD} = 2 kΩ		20	50	
		Negative rail	No load		5	17	
			R_{LOAD} = 10 kΩ		10	20	
			R_{LOAD} = 2 kΩ		40	60	
		R_{LOAD} = 10 kΩ, both rails,T_A = –55°C to +125°C(1)			10	25	
I_{SC}	Short-circuit current	V_S = 5.5 V			±60		mA
		V_S = 2.5 V			±30		mA
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			100		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±1.25 V (V_S = 2.5 V)	I_O = 0 A		1.7	2.4	mA
			I_O = 0 A, T_A = –55°C to +125°C(1)		1.7	2.4	
		V_S = ±2.75 V (V_S = 5.5 V)	I_O = 0 A		1.9	2.6	
			I_O = 0 A, T_A = –55°C to +125°C(1)		1.9	2.6	

(1) Specification established from device population bench system measurements across multiple lots.

5.6 Typical Characteristics

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

Table 5-1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 5-1
Offset Voltage Drift Distribution From –40°C to +125°C	Figure 5-2
Offset Voltage vs Temperature	Figure 5-3
Offset Voltage vs Common-Mode Voltage	Figure 5-4
Offset Voltage vs Power Supply	Figure 5-5
Offset Voltage vs Power Supply	Figure 5-6
Offset Voltage Long Term Drift	Figure 5-7
Open-Loop Gain and Phase vs Frequency	Figure 5-8
Closed-Loop Gain and Phase vs Frequency	Figure 5-9
Input Bias Current vs Common-Mode Voltage	Figure 5-10
Input Bias Current vs Temperature	Figure 5-11
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 5-12
CMRR and PSRR vs Frequency	Figure 5-13
CMRR vs Temperature	Figure 5-14
PSRR vs Temperature	Figure 5-15
0.1Hz to 10Hz Noise	Figure 5-16
Input Voltage Noise Spectral Density vs Frequency	Figure 5-17
THD+N Ratio vs Frequency	Figure 5-18
THD+N vs Output Amplitude	Figure 5-19
Spectral Content	Figure 5-20, Figure 5-21
Quiescent Current vs Supply Voltage	Figure 5-22
Quiescent Current vs Temperature	Figure 5-23
Open-Loop Gain vs Temperature	Figure 5-24
Open-Loop Output Impedance vs Frequency	Figure 5-25
Small-Signal Overshoot vs Capacitive Load (10mV Step)	Figure 5-26
No Phase Reversal	Figure 5-27
Positive Overload Recovery	Figure 5-28
Negative Overload Recovery	Figure 5-29
Small-Signal Step Response (10mV Step)	Figure 5-30, Figure 5-31
Large-Signal Step Response (4V Step)	Figure 5-32 , Figure 5-33
Settling Time	Figure 5-34, Figure 5-35
Short-Circuit Current vs Temperature	Figure 5-36
Maximum Output Voltage vs Frequency	Figure 5-37
EMIRR vs Frequency	Figure 5-38

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

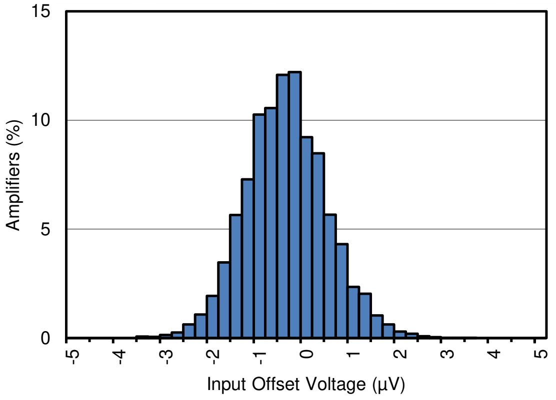


Figure 5-1. Offset Voltage Production Distribution

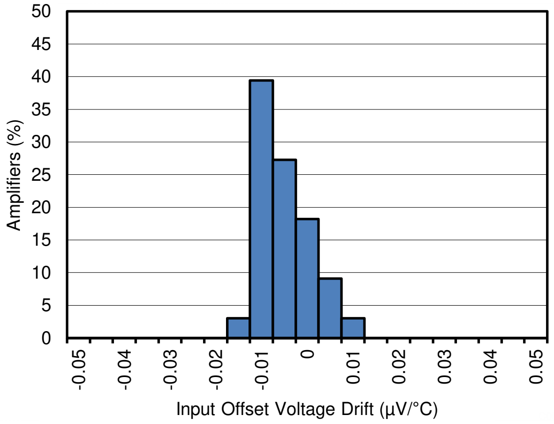


Figure 5-2. Offset Voltage Drift Distribution From –40°C to +125°C

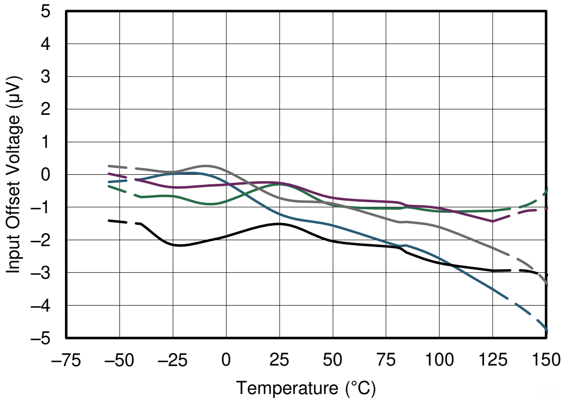


Figure 5-3. Offset Voltage vs Temperature

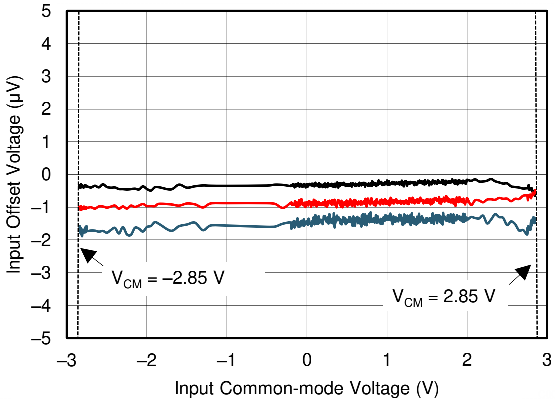


Figure 5-4. Offset Voltage vs Common-Mode Voltage

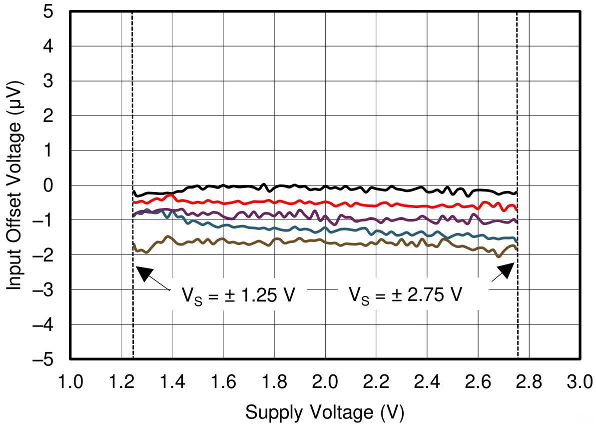


Figure 5-5. Offset Voltage vs Supply Voltage

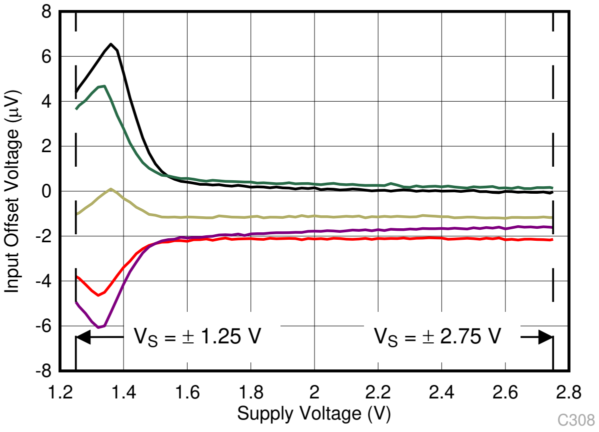


Figure 5-6. Offset Voltage vs Supply Voltage

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

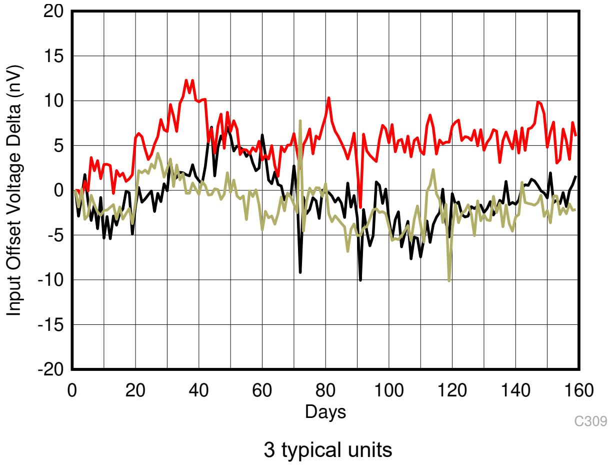


Figure 5-7. Offset Voltage Long Term Drift

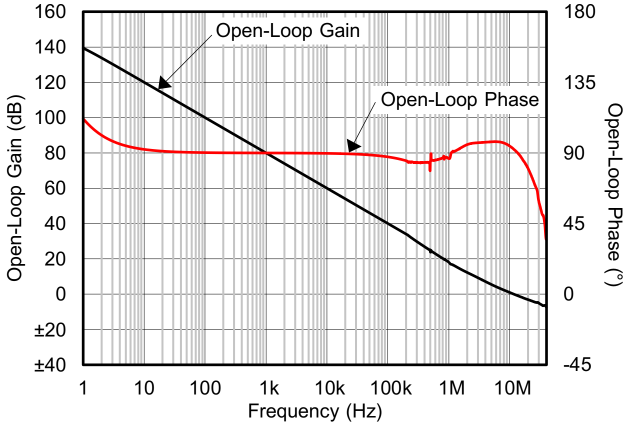


Figure 5-8. Open-Loop Gain and Phase vs Frequency

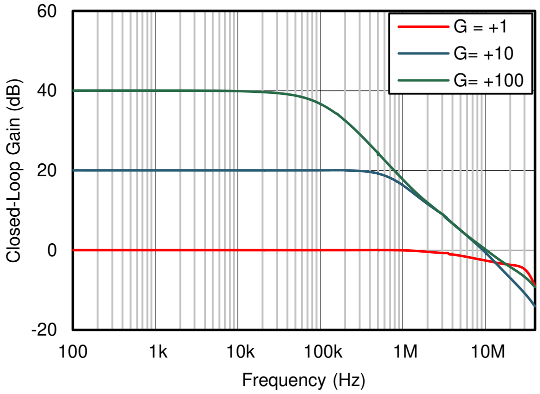


Figure 5-9. Closed-Loop Gain and Phase vs Frequency

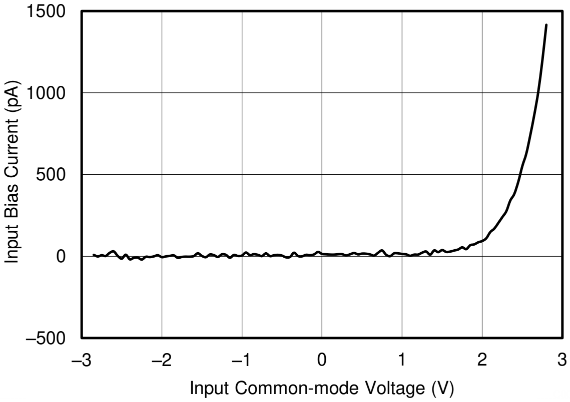


Figure 5-10. Input Bias Current vs Common-Mode Voltage

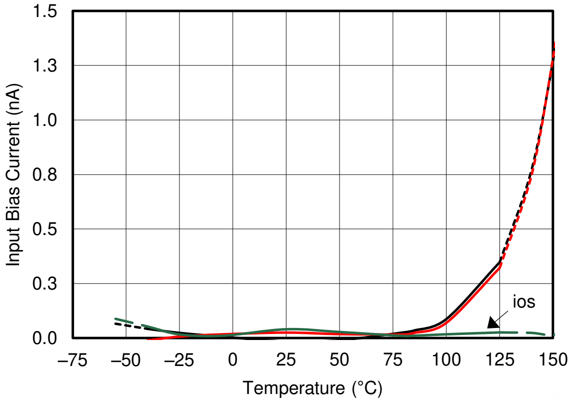


Figure 5-11. Input Bias Current vs Temperature

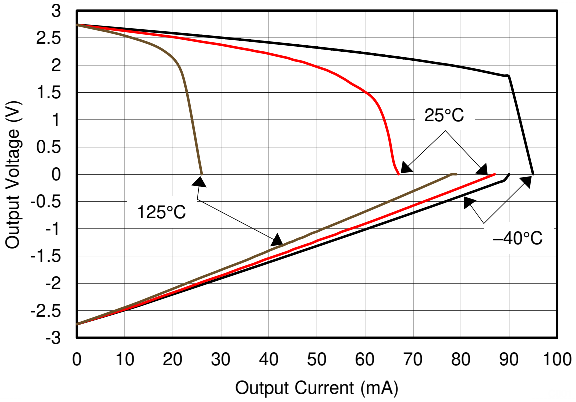


Figure 5-12. Output Voltage Swing vs Output Current (Maximum Supply)

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

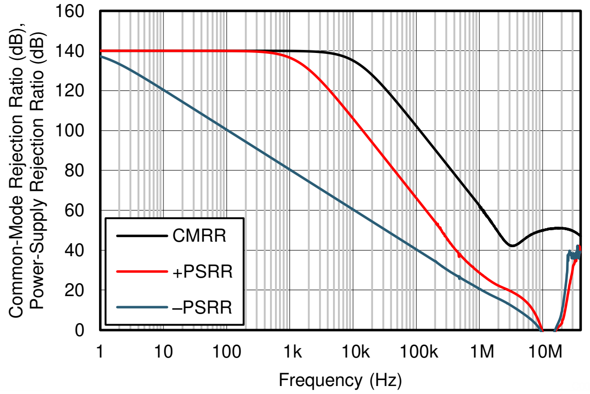


Figure 5-13. CMRR and PSRR vs Frequency

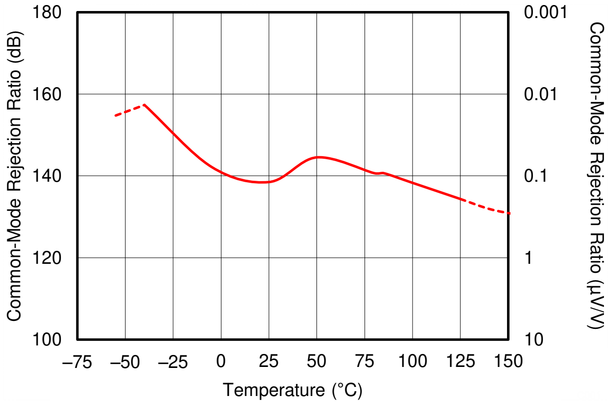


Figure 5-14. CMRR vs Temperature

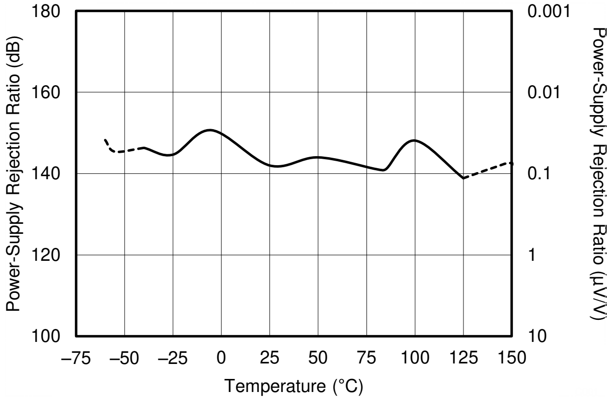


Figure 5-15. PSRR vs Temperature

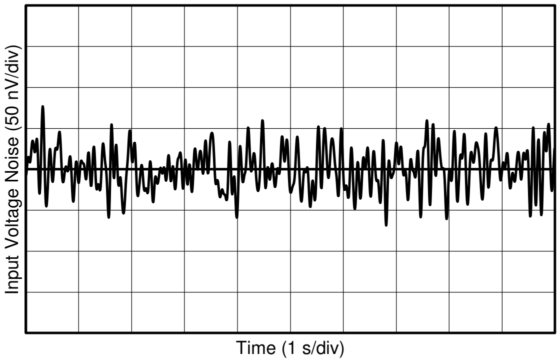


Figure 5-16. 0.1Hz to 10Hz Noise

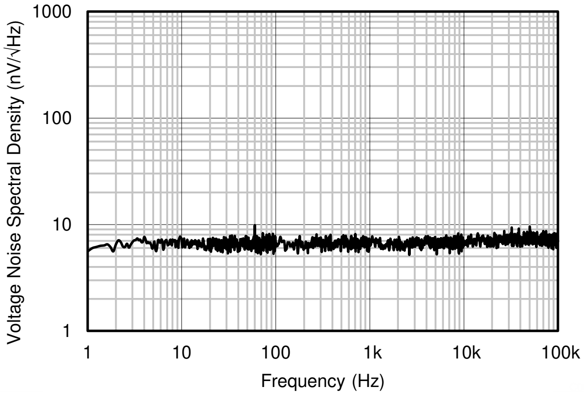


Figure 5-17. Input Voltage Noise Spectral Density vs Frequency

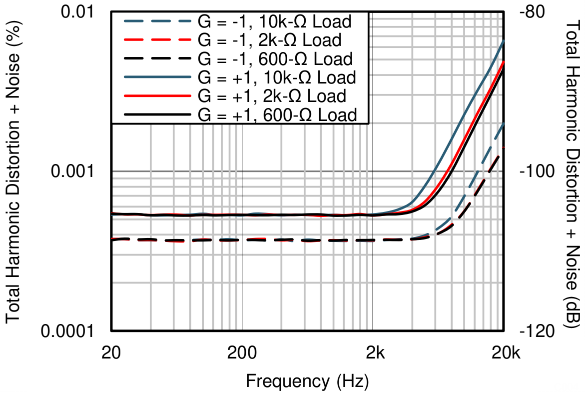


Figure 5-18. THD+N Ratio vs Frequency

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

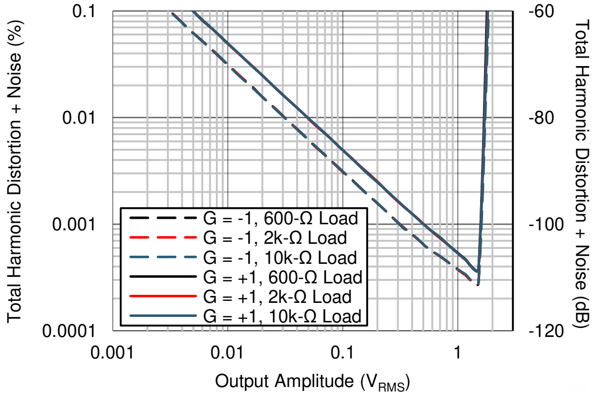
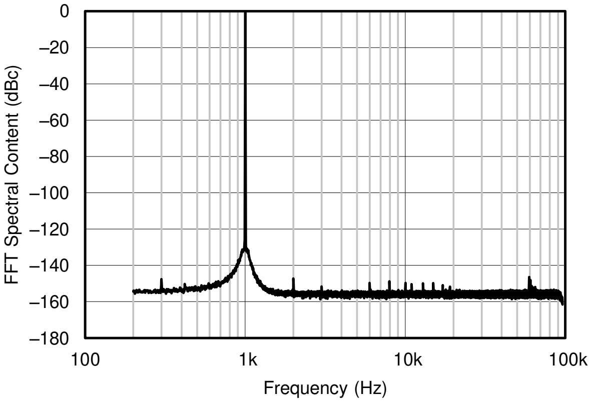
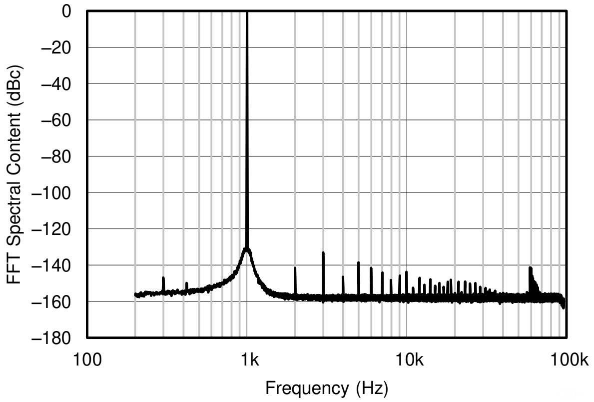


Figure 5-19. THD+N vs Output Amplitude



G = +1, f = 1kHz, V_O = 4.5V_{PP}, R_L = 10kΩ, BW = 90kHz

Figure 5-20. Spectral Content (With 10kΩ Load)



G = +1, f = 1kHz, V_O = 4.5V_{PP}, R_L = 2kΩ, BW = 90kHz

Figure 5-21. Spectral Content (With 2kΩ Load)

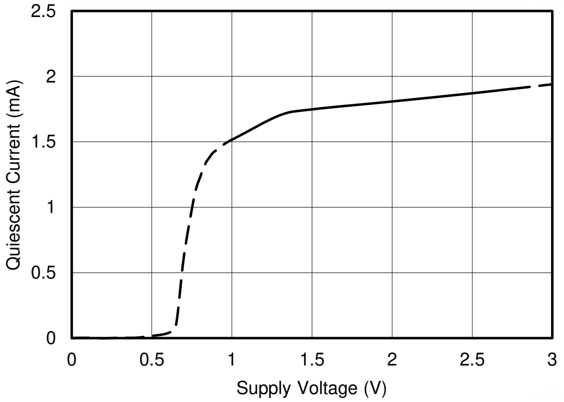


Figure 5-22. Quiescent Current vs Supply Voltage

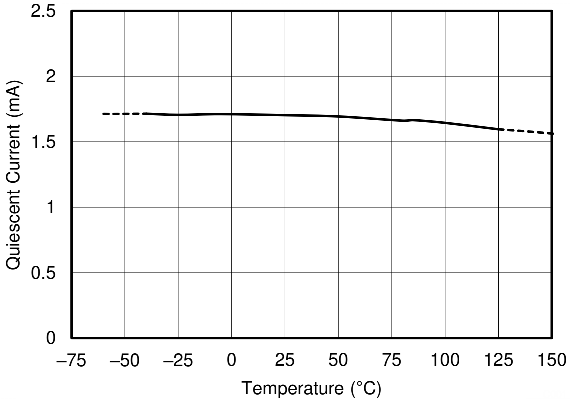


Figure 5-23. Quiescent Current vs Temperature

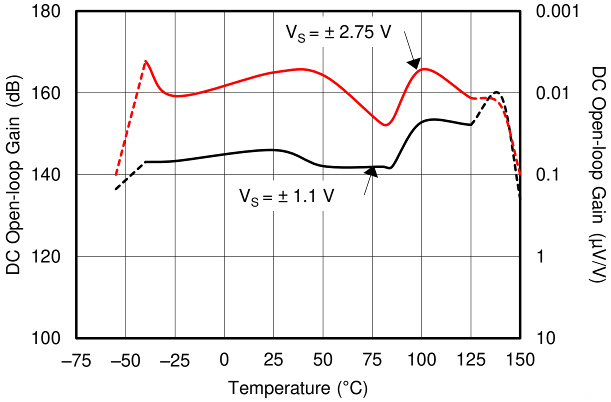


Figure 5-24. Open-Loop Gain vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

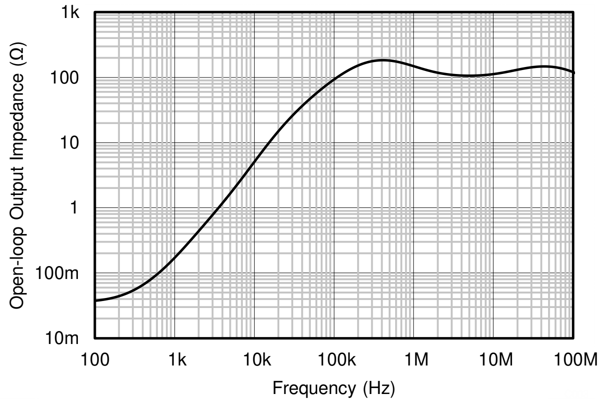


Figure 5-25. Open-Loop Output Impedance vs Frequency

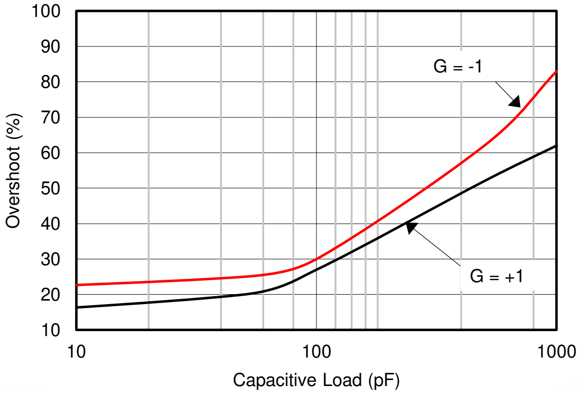


Figure 5-26. Small-Signal Overshoot vs Capacitive Load (10mV Step)

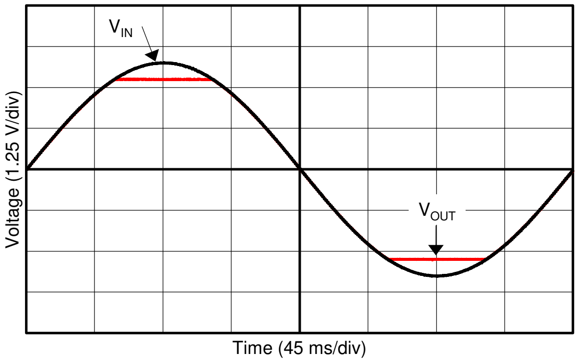


Figure 5-27. No Phase Reversal

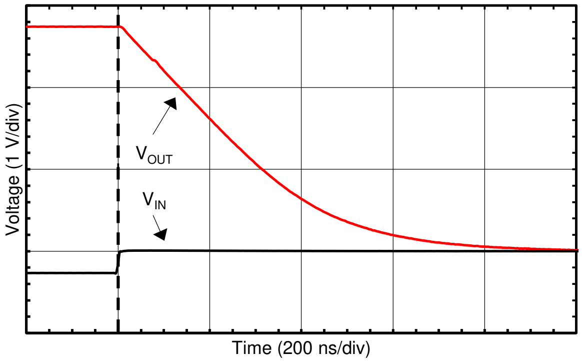


Figure 5-28. Positive Overload Recovery

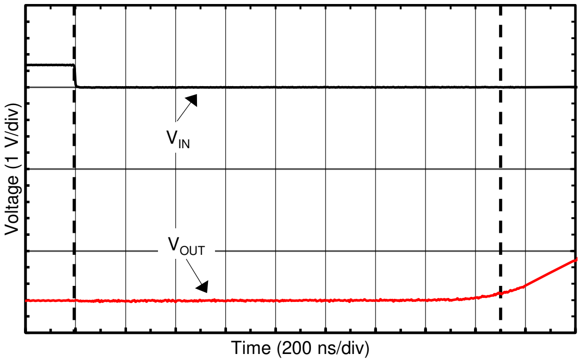
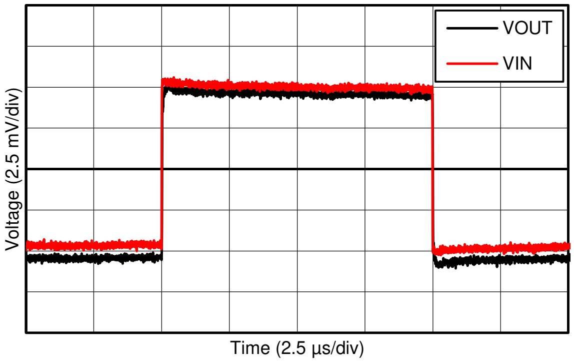


Figure 5-29. Negative Overload Recovery

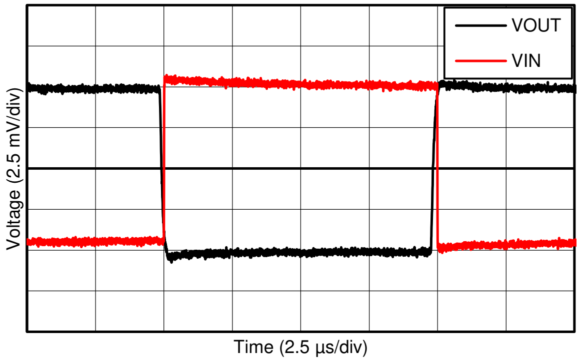


G = +1

Figure 5-30. Small-Signal Step Response (10mV Step)

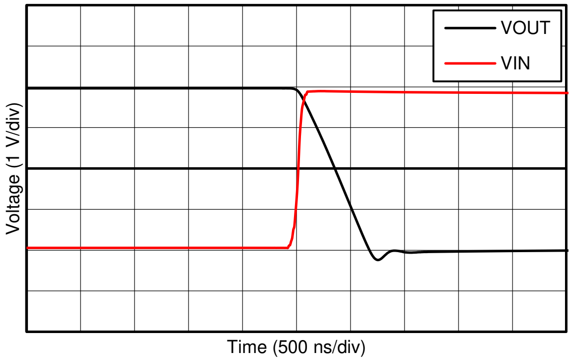
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



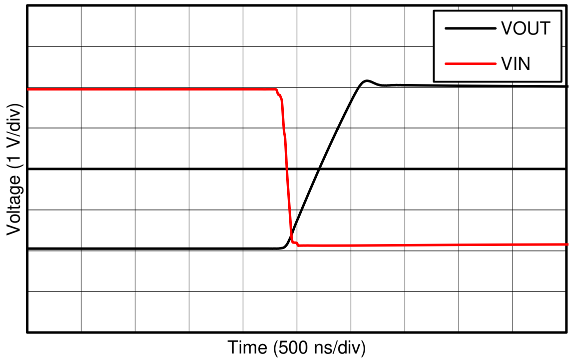
G = –1

Figure 5-31. Small-Signal Step Response (10mV Step)



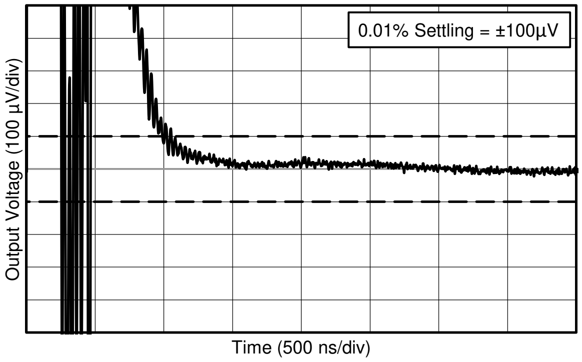
Falling output

Figure 5-32. Large-Signal Step Response (4V Step)



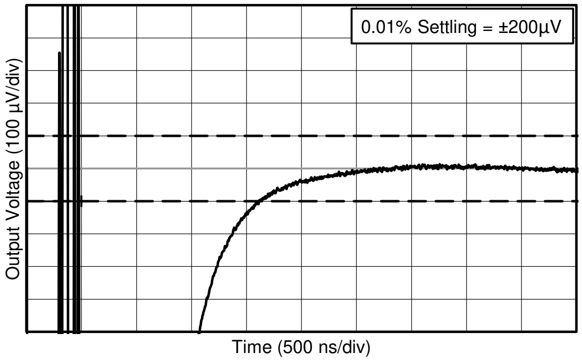
Rising output

Figure 5-33. Large-Signal Step Response (4V Step)



0.01% settling = ±100 µV

Figure 5-34. Settling Time (1V Positive Step)



0.01% settling = ±200 µV

Figure 5-35. Settling Time (1V Negative Step)

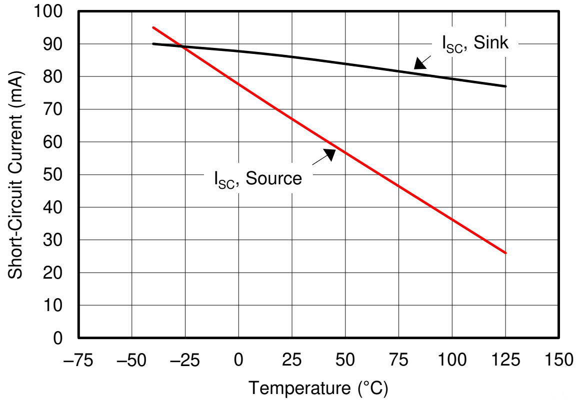


Figure 5-36. Short-Circuit Current vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

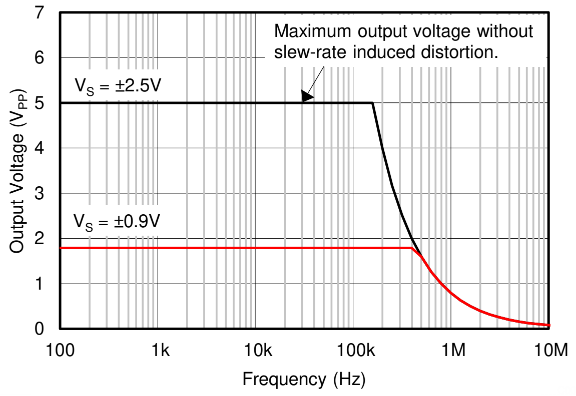


Figure 5-37. Maximum Output Voltage vs Frequency

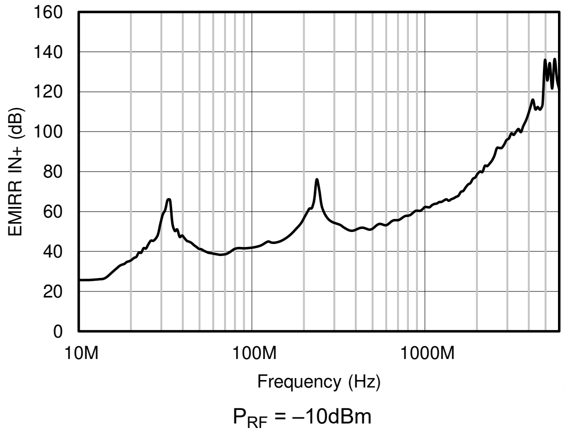


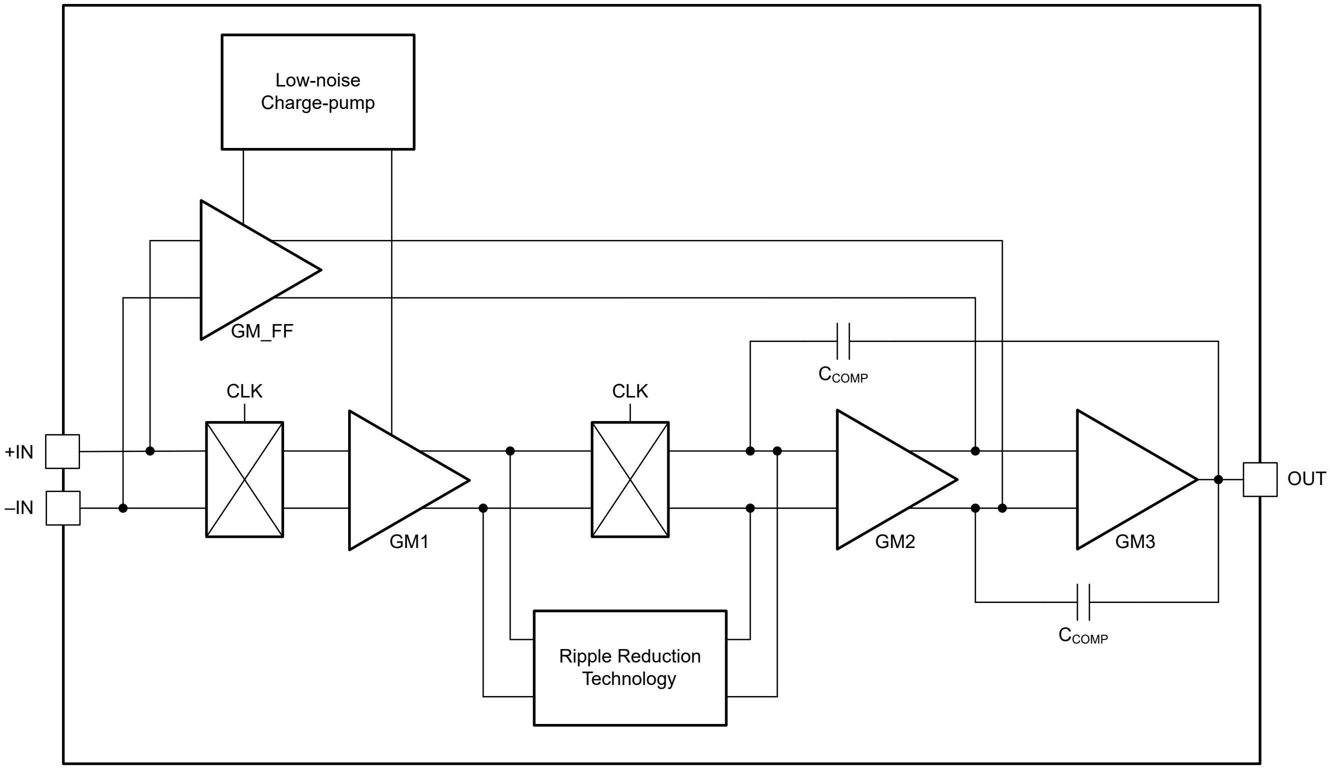
Figure 5-38. EMIRR vs Frequency

6 Detailed Description

6.1 Overview

The OPA4H838-SEP zero-drift amplifier is engineered with the unique combination of a proprietary precision auto-calibration technique paired with a low-noise, low-ripple, input charge pump. These offers an ultra-low input offset voltage and drift and achieves excellent input and output dynamic linearity. The OPA4H838-SEP operates from 2.5V to 5.5V, is unity-gain stable, and is designed for a wide range of general-purpose and precision applications. The integrated, low-noise charge pump allows true rail-to-rail input common-mode operation without distortion associated with complementary rail-to-rail input topologies (input crossover distortion). The OPA4H838-SEP strengths also include a 10MHz bandwidth, 7 $nV/\sqrt{Hz}$ noise spectral density, and no 1/f noise, making the OPA4H838-SEP an excellent choice for interfacing with sensor modules and buffering high-fidelity, digital-to-analog converters (DACs).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Voltage

The OPA4H838-SEP can be used with single or dual supplies from an operating range of V_S = 2.5V (±1.25V) up to 5.5V (±2.75V). Supply voltages greater than 7V can permanently damage the device (see the *Absolute Maximum Ratings* table).

6.3.2 Input Voltage and Zero-Crossover Functionality

The OPA4H838-SEP input common-mode voltage range extends 0.1V beyond the supply rails. This amplifier is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers. Operating a complementary rail-to-rail input amplifier with signals traversing the transition region results in unwanted non-linear behavior and polluted spectral content. Figure 6-1 and Figure 6-2 contrast the performance of a traditional complementary rail-to-rail input stage amplifier with the performance of the zero-crossover OPA4H838-SEP. Significant harmonic content and distortion is generated during the differential pair transition (such a transition does not exist in the OPA4H838-SEP. Crossover distortion is eliminated through the use of a single differential pair coupled with an internal low-noise charge pump. The OPA4H838-SEP maintains noise, bandwidth, and offset performance throughout the input common-mode range, thus reducing printed circuit board (PCB) and bill of materials (BOM) complexity through the reduction of power-supply rails.

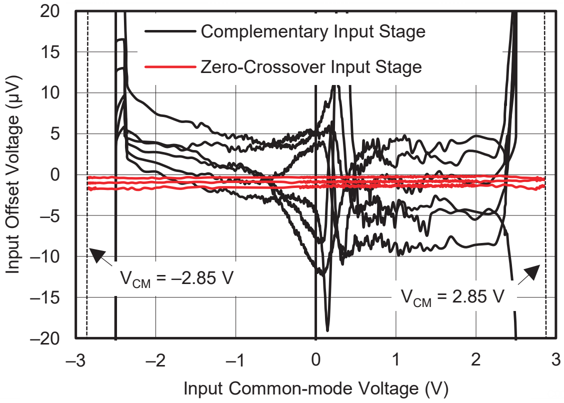


Figure 6-1. Input Crossover Distortion Nonlinearity

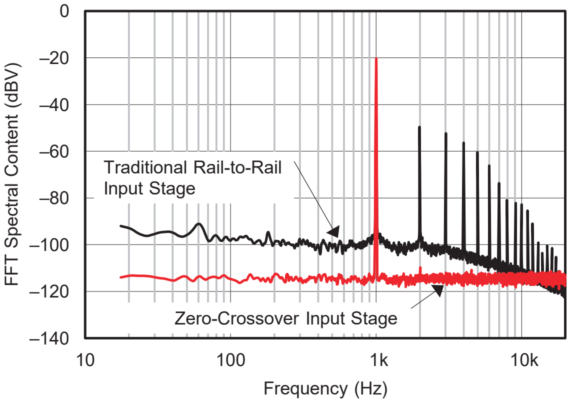


Figure 6-2. Input Crossover Distortion Spectral Content

Typically, input bias current is approximately ±30pA. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This limitation is easily accomplished with an input resistor, as shown in Figure 6-3.

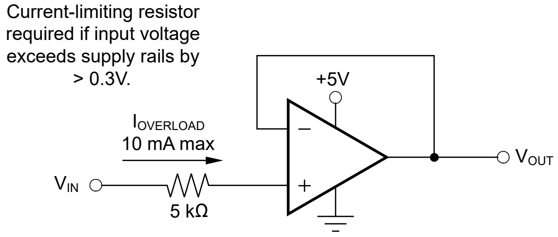


Figure 6-3. Input Current Protection

6.3.3 Input Differential Voltage

The typical input bias current of the OPA4H838-SEP during normal operation is approximately 30pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 6-4. Notice that the input bias current remains within specification in the linear region.

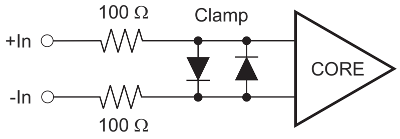


Figure 6-4. Equivalent Input Circuit

6.3.4 Internal Offset Correction

The OPA4H838-SEP family of operational amplifiers uses an auto-calibration technique with a time-continuous, 200kHz operational amplifier in the signal path. This amplifier is zero-corrected every 5µs using a proprietary technique. At power-up, the amplifier requires approximately 1ms to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

6.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA4H838-SEP operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20MHz (–3dB), with a rolloff of 20dB per decade.

6.4 Device Functional Modes

The OPA4H838-SEP has a single functional mode and is operational when the power-supply voltage is greater than 2.5V (±1.25V). The maximum specified power-supply voltage for the OPA4H838-SEP is 5.5V (±2.75V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The OPA4H838-SEP is a unity-gain stable, precision operational amplifier family free from unexpected output and phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPA4H838-SEP family is optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100mV beyond the supplies without input crossover distortion and a rail-to-rail output that swings within 5mV of the supplies under normal test conditions. The OPA4H838-SEP series of precision amplifiers is designed for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

7.2 Typical Applications

7.2.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1A to +1A. The single-ended output spans from 110mV to 3.19V. This design uses the OPA4H838-SEP because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 7-1 shows the solution.

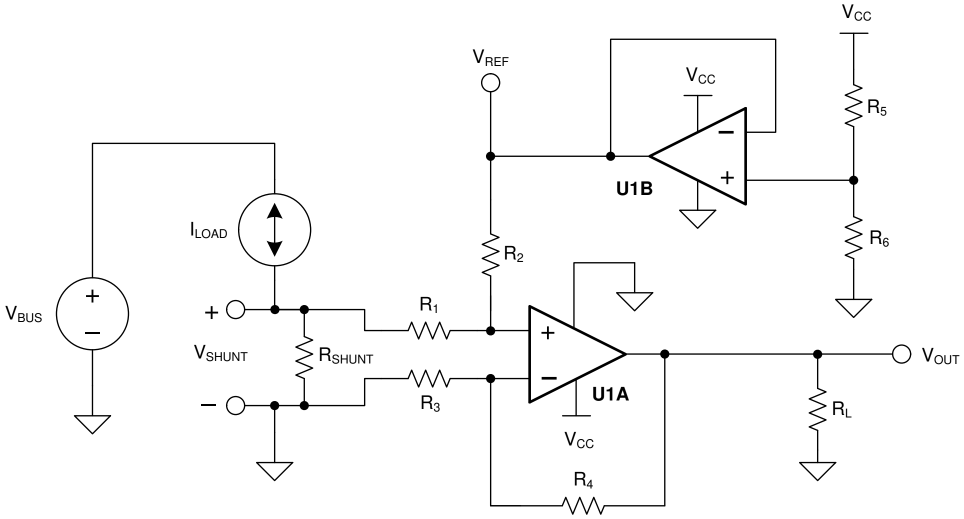


Figure 7-1. Bidirectional Current-Sensing Schematic

7.2.1.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3V
- Input: –1A to 1A
- Output: 1.65V ±1.54V (110mV to 3.19V)

7.2.1.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \tag{1}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \dfrac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\dfrac{R_6}{R_5 + R_6}\right)$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\text{ mV}}{1\text{ A}} = 100\text{ m}\Omega \tag{2}$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100mV to 100mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA4H838-SEP, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the OPA4H838-SEP has a typical offset voltage of merely ±0.25 µV (±5 µV maximum).

Given a symmetric load current of –1A to 1A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA4H838-SEP must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA4H838-SEP given a 3.3V supply.

$$-100\text{mV} < V_{CM} < 3.4\text{V} \tag{3}$$

$$100\text{mV} < V_{OUT} < 3.2\text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{\text{OUT\_Max}} - V_{\text{OUT\_Min}}}{R_{\text{SHUNT}} \times (I_{\text{MAX}} - I_{\text{MIN}})} = \frac{3.2\text{ V} - 100\text{ mV}}{100\text{ m}\Omega \times [1\text{ A} - (-1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R_1 and R_3 was 1kΩ. 15.4kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

7.2.1.3 Application Curve

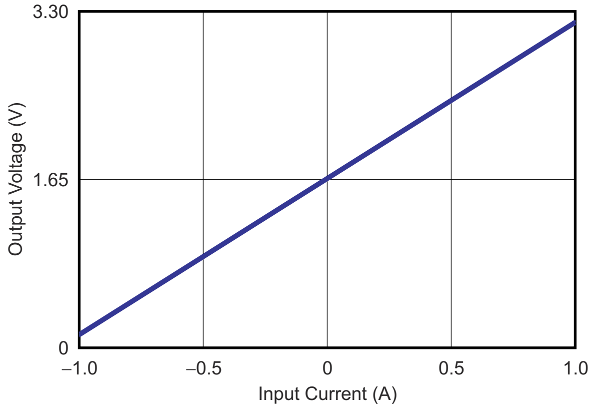


Figure 7-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

7.2.2 Single Operational Amplifier Bridge Amplifier

Figure 7-3 shows the basic configuration for a bridge amplifier.

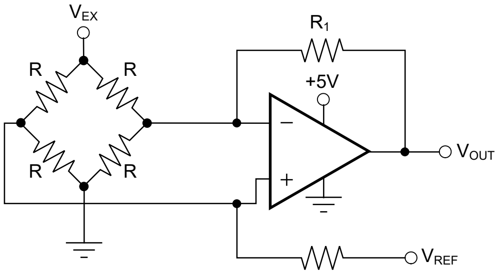


Figure 7-3. Single Operational Amplifier Bridge Amplifier Schematic

7.2.3 Programmable High-Side Current Source

The OPA4H838-SEP can be configured as a programmable two-stage high-side current source as shown in Figure 7-4, in conjunction with the DAC121S101-SEP.

This circuit supplies adjustable current (0–100mA) to a ground-referenced load. The first stage sets a reference current based on the DAC output voltage. The second stage acts as a current mirror that scales the reference current and regulates the output through PMOS transistor Q2. Resistors R_{SET}, R_A, and R_B set the output current based on the DAC voltage, while C_{COMP}, R_{ISO}, and R_{FB} provide stability compensation

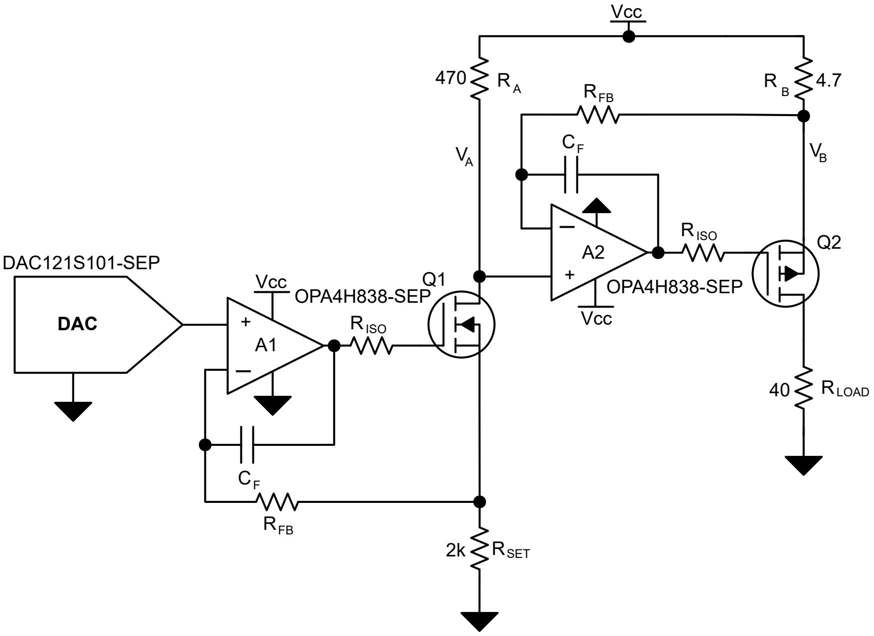


Figure 7-4. Two Stage Current Source

7.2.4 Load Cell Measurement

Figure 7-5 shows the OPA4H838-SEP in a high-CMRR dual-op amp instrumentation amplifier with a trim resistor and 6-wire load cell for precision measurement. Figure 7-6 illustrates the output voltage as a function of load cell resistance change, along with the nonlinearity of the system.

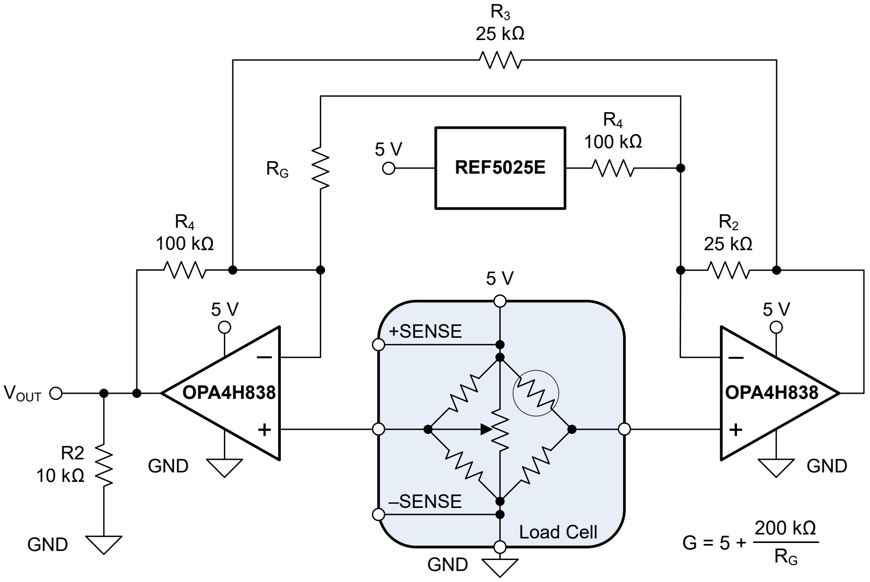


Figure 7-5. Load Cell Measurement Schematic

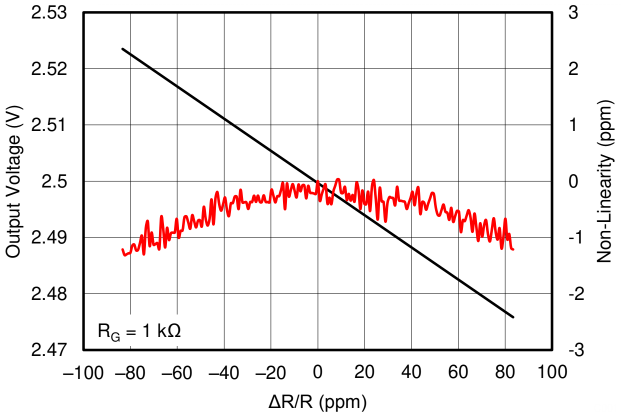


Figure 7-6. Load Cell Measurement Output

7.3 Power Supply Recommendations

The OPA4H838-SEP family of devices is specified for operation from 2.5V to 5.5V (±1.25V to ±2.75V).

7.4 Layout

7.4.1 Layout Guidelines

Paying attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1µV/°C or higher, depending on materials used.

7.4.2 Layout Example

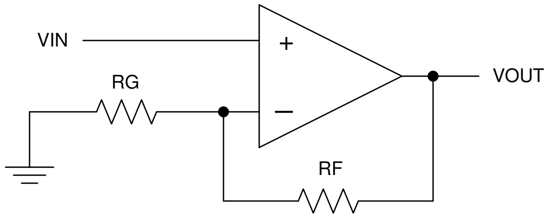


Figure 7-7. Schematic Representation

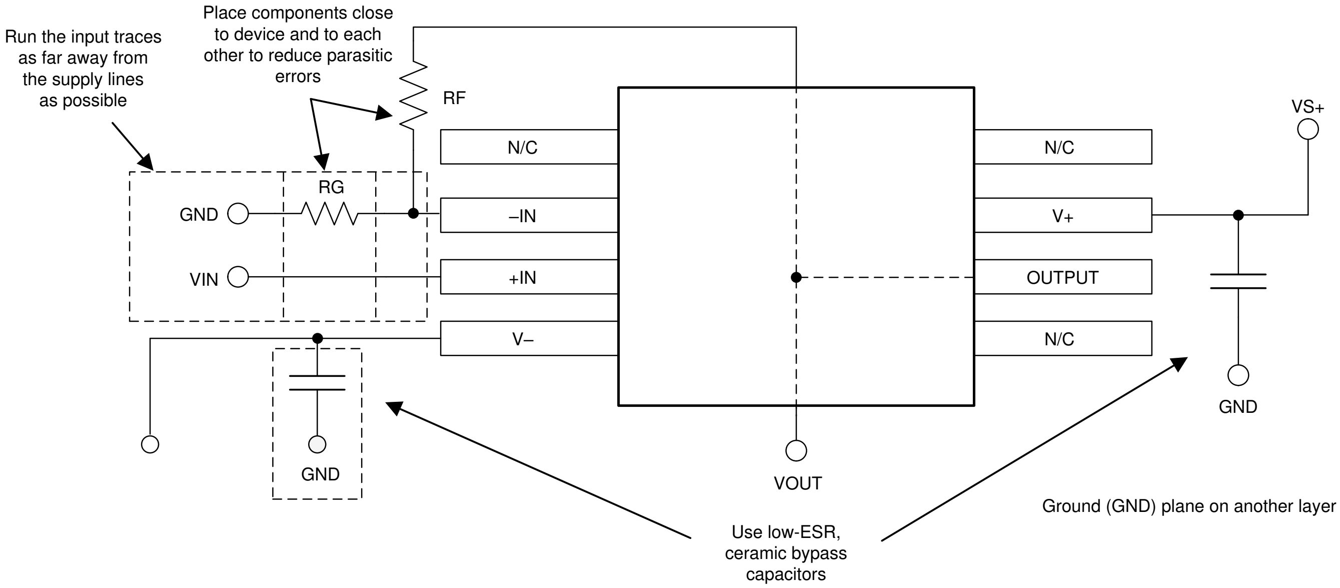


Figure 7-8. OPA4H838-SEP Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.1.2 Development Support

8.1.2.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Circuit board layout techniques*
- Texas Instruments, *DAC121S101-SEP 12-Bit, Micro Power, RRO Digital-to-Analog Converter* data sheet

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2025) to Revision A (April 2026)	Page
• Changed the document status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
POPA4H838MPWTSEP	Active	Preproduction	TSSOP (PW) | 14	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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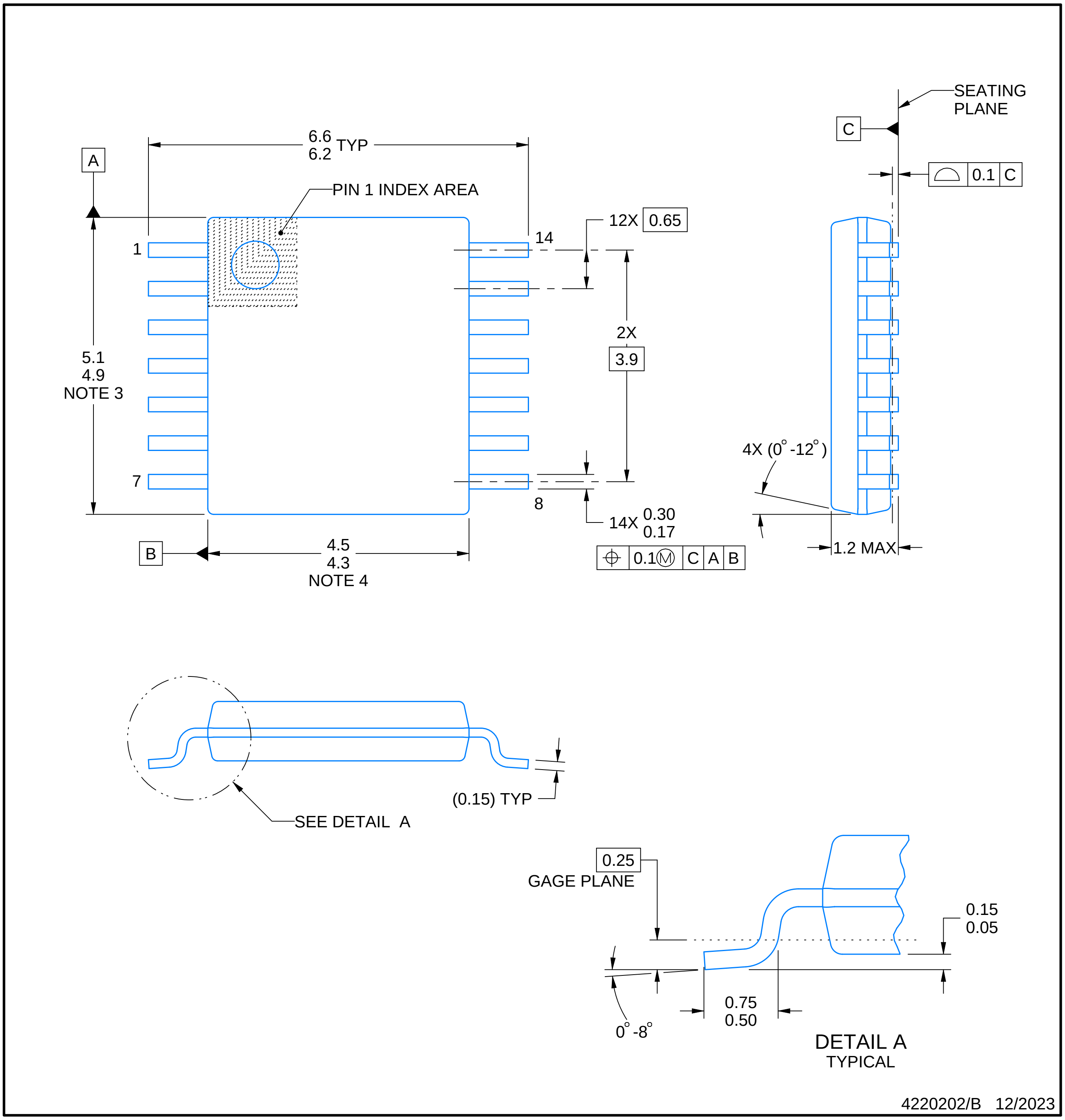
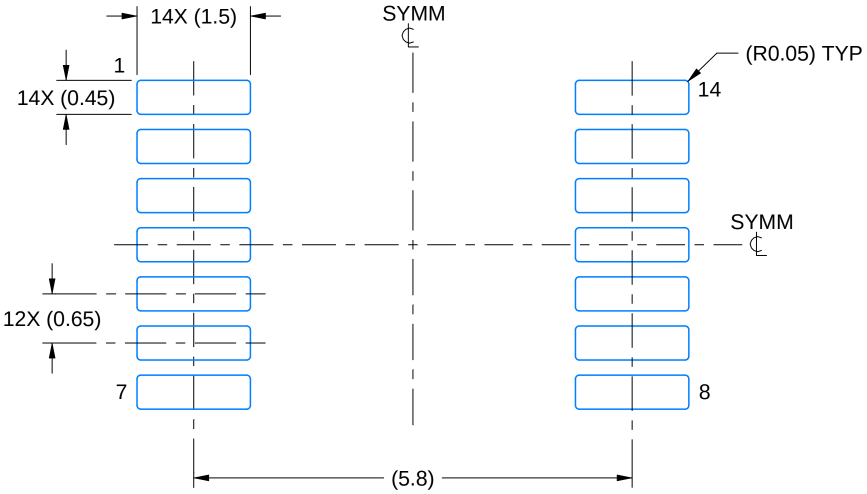
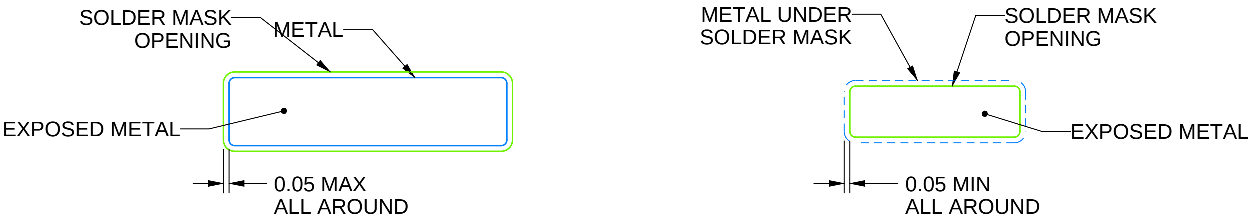


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)

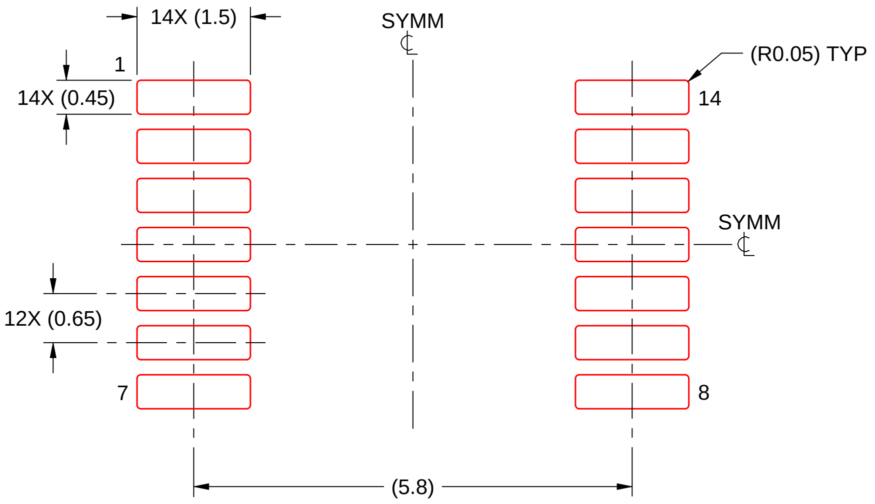
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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