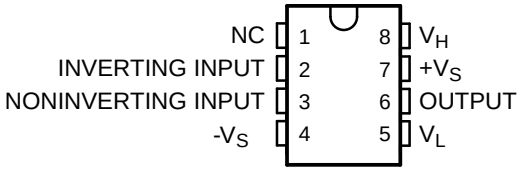
UNITY-GAIN STABLE WIDEBAND VOLTAGE LIMITING AMPLIFIER

FEATURES

- **High Linearity Near Limiting**
- **Fast Recovery from Overdrive: 1 ns**
- **Limiting Voltage Accuracy: ±15 mV**
- **-3-dB Bandwidth (G = +1): 450 MHz**
- **Slew Rate: 1100 V/ms**
- **±5-V and 5-V Supply Operation**
- **Unity Gain Version of the OPA699**

JD PACKAGE
(TOP VIEW)



NC - No internal connection

P0013-01

APPLICATIONS

- **Fast Limiting ADC Input Buffers**
- **CCD Pixel Clock Stripping**
- **Video Sync Stripping**
- **HF Mixers**
- **IF Limiting Amplifiers**
- **AM Signal Generation**
- **Non-Linear Analog Signal Processing**
- **OPA688M Replacement**

DESCRIPTION

The OPA698 is a wideband, unity gain stable voltage-feedback op amp that offers bipolar output voltage limiting. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15 mV. The op amp operates linearly to within 30 mV of the output limit voltages.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100 mV of the desired linear output range. A fast 1-ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain and allows the OPA698 to be used in all standard op amp applications.

Non-linear analog signal processing benefits from the ability of the OPA698 to sharply transition from linear operation to output limiting. The quick recovery time supports high-speed applications.

The OPA698M is available in an industry standard pinout CDIP-8 package. For higher gain or transimpedance applications requiring output limiting with fast recovery, consider the OPA699M.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – JD	Tube	OPA698MJD	OPA698MJD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		UNIT
	Power supply	±6.5 V
V_{ICM}	Common-mode input voltage	$\pm V_S$
V_{ID}	Differential input voltage	$\pm V_S$
	Limiter voltage range	$\pm(V_S$ - 0.7 V)
T_A	Operating free-air temperature range	-55°C to 125°C
T_{stg}	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C
T_J	Junction temperature	150°C
θ_{JC}	Package thermal impedance[2] (JD Package)	14.5°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is measured per MIL-STD-883, Method 1012.1.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Operating voltage	Split-rail operation		±5	±6	V
	Single-supply operation		5	12	
Operating free-air temperature		–55		125	°C

ELECTRICAL CHARACTERISTICS

V_S = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE (see Figure 47)					
Small signal bandwidth	V_O < 0.2 Vp-p, G = +1, R_F = 25 Ω		450		MHz
	V_O < 0.2 Vp-p, G = +2		215		
	V_O < 0.2 Vp-p, G = –1		215		
Gain-bandwidth product (G ≥ 5)	V_O < 0.2 Vp-p		250		MHz
Bandwidth for 0.1-dB gain flatness	V_O = 0.2 V		30		MHz
Gain peaking	V_O < 0.2 Vp-p, G = +1, R_F = 25 Ω		5		dB
Large signal bandwidth	V_O = 4 Vp-p, V_H = $-V_L$ = 2.5 V		160		MHz
Slew rate	4 V step, V_H = $-V_L$ = 2.5 V		1100		V/µs
Rise and fall time	0.2 V step		1.6		ns
Settling time to 0.05%	2 V step		8		ns
Second harmonic distortion	V_O = 2 Vp-p, f = 5 MHz		–74		dB
Third harmonic distortion	V_O = 2 Vp-p, f = 5 MHz		–87		dB
Differential gain	R_L = 500 Ω, NTSC, PAL		0.012%		
Differential phase	R_L = 500 Ω, NTSC, PAL		0.008		°
Input noise, voltage noise density	f ≥ 1 MHz		5.6		nV/√Hz
Input noise, current noise density	f ≥ 1 MHz		2.2		pA/√Hz

(1) All typical limits are at T_A = 25°C unless otherwise specified.

ELECTRICAL CHARACTERISTICS (continued)

V_S = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE						
Open-loop voltage gain (AVOL)	V_O = ±0.5 V	T_A = 25°C	52	58		dB
		T_A = Full range	43			
Input offset voltage (V_{IO})		T_A = 25°C		±2	±8	mV
		T_A = Full range			±12	
Input bias current (I_{IB})(2)		T_A = 25°C		±3	±10	µA
		T_A = Full range			±18	
Input offset current (I_{IO})		T_A = 25°C		±0.3	±3	µA
		T_A = Full range			±4	
INPUT						
Common-mode rejection ratio (CMRR)	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	52	58		dB
		T_A = Full range	47			
Common-mode input voltage range (V_{ICR})(3)		T_A = 25°C	±3.2	±3.3		MΩ pF
		T_A = Full range	±3.1			
Input impedance, differential mode				0.32 1		MΩ pF
Input impedance, common mode				3.5 1		MΩ pF
OUTPUT						
Output voltage range (V_{OH}, V_{OL})	V_H = 4.3 V, V_L = –4.3 V, R_L≥ 500 Ω	T_A = 25°C	±3.9	±4		V
		T_A = Full range	±3.7			
Current output, sourcing (I_{OH})	V_H = 4.3 V, V_L = –4.3 V, R_L = 20 Ω	T_A = 25°C	110	165		mA
		T_A = Full range	100			
Current output, sinking (I_{OL})	V_H = 4.3 V, V_L = –4.3 V, R_L = 20 Ω	T_A = 25°C	–90	–130		mA
		T_A = Full range	–80			
Closed-loop output impedance	G = +1, R_F = 25 Ω, f < 100 kHz			0.2		Ω
POWER SUPPLY						
Operating voltage (V_S)				±5	±6	V
Quiescent current (I_S)		T_A = 25°C	15	15.5	16	mA
		T_A = Full range	13.5		18	
Power supply rejection ratio (PSRR)	Input referred, V_S = ±4.5 V to ±5.5 V	T_A = 25°C	65	76		dB
		T_A = Full range	60			dB
OUTPUT VOLTAGE LIMITERS (pins 5 and 8)						
Default output limited voltage	Limiter pins open	T_A = 25°C	±3.3	±3.6		V
		T_A = Full range	±3			
Limiter output offset voltage	(V_O – V_H) or (V_O – V_L)	T_A = Full range		±15	±50	mV
Limiter input bias current magnitude(4)	V_O = 0 V	T_A = 25°C	40	55	65	µA
		T_A = Full range	35		70	
Limiter input impedance				3.4 1		MΩ pF
Limiter feedthrough(5)	f = 5 MHz			–68		dB
Maximum limiter voltage					±4.3	V
Minimum limiter voltage separation			400			mV
Op amp bias current shift (2)				3		µA

(2) Current is considered positive out of node.
(3) CMIR tested as < 3-dB degradation from minimum CMRR at specified limits.
(4) I_{VH} (V_H bias current) is positive and I_{VL} (V_L bias current) is negative under these conditions. See Note 2, Figure 47 and Figure 66.
(5) Limiter feedthrough is the ratio of the output magnitude to the sine wave added to V_H (or V_L) when VIN = 0.

ELECTRICAL CHARACTERISTICS (continued)

V_S = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Limiter small signal bandwidth	V_I = ±2 V, V_O < 0.02 Vp-p			600		MHz
Limiter slew rate(6)				125		V/µs
Limiter step response, overshoot	V_I = ±2 V			250		mV
Limiter step response, recovery time	V_I = ±2 V			1		ns
Linearity guardband(7)	V_O = 2 Vp-p, f = 5 MHz			30		mV

(6) V_H slew rate conditions are: V_{IN} = +2 V, G = +2, V_L = -2 V, V_H = step between 2 V and 0 V. V_L slew rate conditions are similar.
(7) Linearity Guardband is defined for an output sinusoid (f = 5 MHz, V_O = 0 V_{DC} ±1 VP-P) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3 dB (see Figure 67).

ELECTRICAL CHARACTERISTICS

V_S = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (see Figure 48)						
Small signal bandwidth	V_O < 0.2 Vp-p, G = +1, R_F = 25 Ω			375		MHz
	V_O < 0.2 Vp-p, G = +2			200		
	V_O < 0.2 Vp-p, G = –1			200		
Gain-bandwidth product (G ≥ +5)	V_O < 0.2 Vp-p			230		MHz
Gain peaking	V_O < 0.2 Vp-p, G = +1, R_F = 25 Ω			7		dB
Bandwidth for 0.1-dB gain flatness	V_O < 0.2 Vp-p			30		MHz
Large signal bandwidth	V_O = 2 Vp-p			200		MHz
Slew rate	2 V step			820		V/µs
Rise and fall time	0.2 V step			1.9		ns
Settling time to 0.05%	1 V step			12		ns
Spurious free dynamic range	V_O = 2 Vp-p, f = 5 MHz			64		dB
Input noise, voltage noise density	f > 1 MHz			5.7		nV/√Hz
Input noise, current noise density	f > 1 MHz			2.3		pA/√Hz
DC PERFORMANCE						
Open-loop voltage gain (AVOL)	V_O = ±0.4 V	T_A = 25°C	52	57		dB
		T_A = Full range	43			
Input offset voltage (V_{IO})		T_A = 25°C		±4	±8	mV
		T_A = Full range			±12	
Input bias current (I_{IB})(2)		T_A = 25°C		±3	±10	µA
		T_A = Full range			±15	
Input offset current (I_{IO})		T_A = 25°C		±0.4	±3	µA
		T_A = Full range			±4	
INPUT						
Common-mode rejection ratio (CMRR)	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	50	57		dB
		T_A = Full range	45			
Common-mode input voltage range (V_{ICR})(3)		T_A = 25°C	V_{ICM} ±0.7	V_{ICM} ±0.8		V
		T_A = Full range	V_{ICM} ±0.6			
Input impedance, differential mode				0.32 1		MΩ pF

(1) All typical limits are at T_A = 25°C unless otherwise specified.
(2) Current is considered positive out of node.
(3) CMIR tested as < 3-dB degradation from minimum CMRR at specified limits.

ELECTRICAL CHARACTERISTICS (continued)

V_S = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input impedance, common mode				3.5 1		MΩ pF
OUTPUT						
Output voltage range (V_{OH}, V_{OL})	$V_H = V_{ICM}$ + 1.8 V, $V_L = V_{ICM}$– 1.8 V, $R_L \geq$ 500 Ω	T_A = 25°C	V_{ICM} ±1.4	V_{ICM} ±1.6		V
		T_A = Full range	V_{ICM} ±1.3			
Current output, sourcing (I_{OH})	V_S = ±2.5 V, R_L = 20 Ω	T_A = 25°C	70	105		mA
		T_A = Full range	60			
Current output, sinking (I_{OL})	V_S = ±2.5 V, R_L = 20 Ω	T_A = 25°C	–60	–90		mA
		T_A = Full range	–50			
Closed-loop output impedance	G = +1, R_F = 25 Ω, f < 100 kHz			0.2		Ω
POWER SUPPLY						
Operating voltage (V_S)				5	12	V
Quiescent current (I_S)		T_A = 25°C	13.5	14.3	15	mA
		T_A = Full range	12		16.5	
Power supply rejection ratio (PSRR)	Input referred, V_S = 4 V to 6 V	T_A = Full range	58	72		dB
OUTPUT VOLTAGE LIMITERS (pins 5 and 8)						
Default output limited voltage	Limiter pins open	T_A = 25°C	V_{ICM} ±0.8	V_{ICM} ±1.1		V
		T_A = Full range	V_{ICM} ±0.6			V
Limiter output offset voltage	(V_O – V_H) or (V_O – V_L)	T_A = Full range		±15	±50	mV
Limiter input bias current magnitude (4)	V_O = 2.5 V	T_A = 25°C	40	50	65	µA
		T_A = Full range	35		70	
Limiter input bias current drift				30		nA/°C
Limiter input impedance				3.4 1		MΩ pF
Limiter feedthrough (5)	f = 5 MHz			–60		dB
Maximum limiter voltage					V_{ICM} ±1.8	V
Minimum limiter voltage separation			400			mV
Op amp bias current shift (2)				5		µA
Limiter small signal bandwidth	$V_I = V_{ICM}$ ± 1.2 V, V_O < 0.02 Vp-p			450		MHz
Limter slew rate (6)				100		V/µA
Limiter step response, overshoot	$V_I = V_{ICM}$ ± 1.2 V			55		mV
Limiter step response, recovery time	$V_I = V_{ICM}$ ± 1.2 V			3		ns
Linearity guardband (7)	V_O = 2 Vp-p, f = 5 MHz			30		mV

(4) I_{VH}(V_H bias current) is positive and I_{VL} (V_L bias current) is negative under these conditions. See Note 2, Figure 47 and Figure 66.
(5) Limiter feedthrough is the ratio of the output magnitude to the sine wave added to V_H (or V_L) when VIN = 0.
(6) V_H slew rate conditions are: $V_{IN} = V_{ICM}$ +4 V, G = +2, $V_L = V_{ICM}$ – 2 V, V_H = stepped between V_{ICM} + 1.2 V and V_{ICM}. V_L slew rate conditions are similar.
(7) Linearity Guardband is defined for an output sinusoid (f = 5 MHz, V_O = 0 V_{DC} ±1 VP-P) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3 dB (see Figure 67).

TYPICAL CHARACTERISTICS — V_S = ±5 V

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

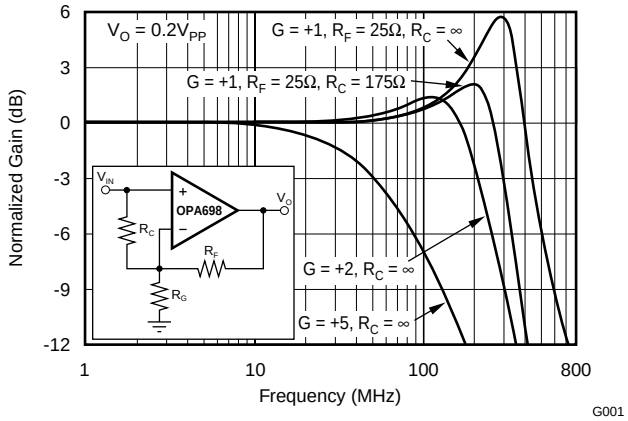

Figure 1.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

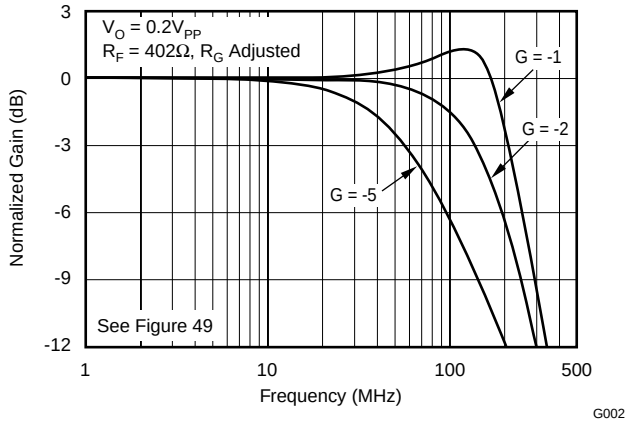

Figure 2.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

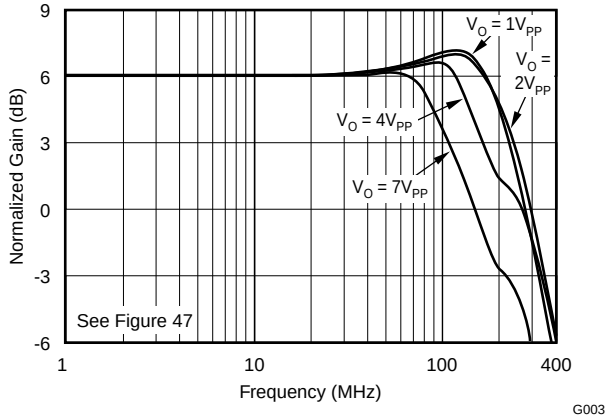

Figure 3.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

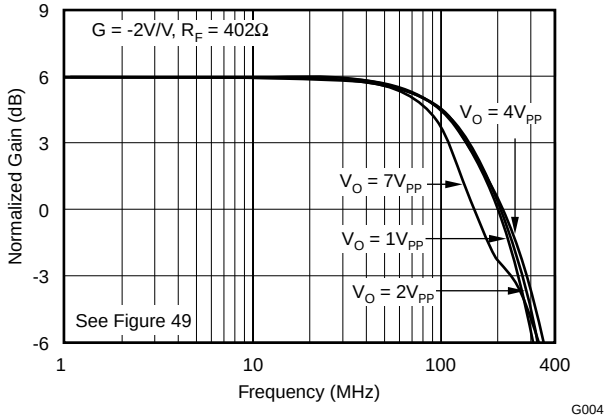

Figure 4.

V_H–LIMITER SMALL-SIGNAL FREQUENCY RESPONSE

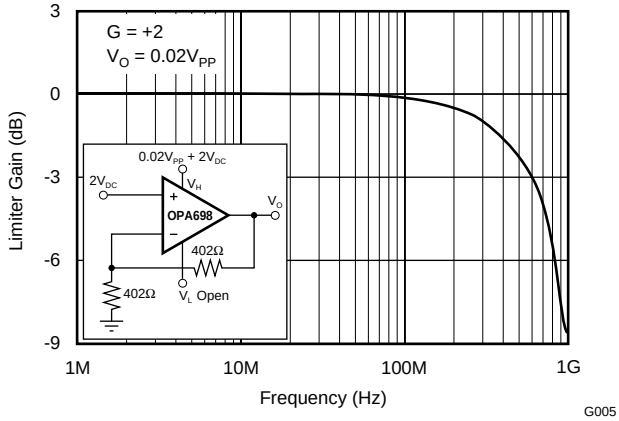

Figure 5.

V_I–LIMITER SMALL-SIGNAL FREQUENCY RESPONSE

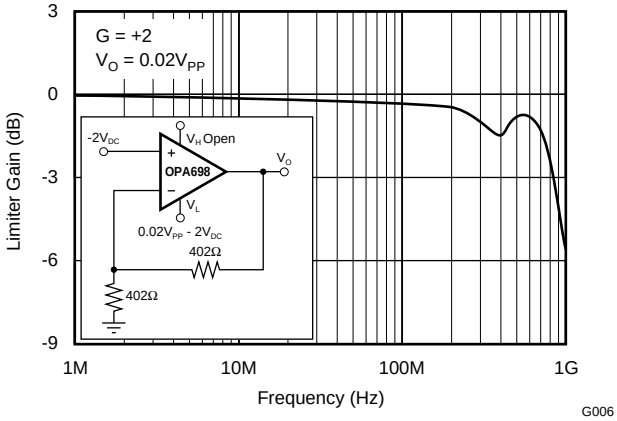

Figure 6.

TYPICAL CHARACTERISTICS — V_S = ±5 V (continued)

SMALL-SIGNAL PULSE RESPONSE

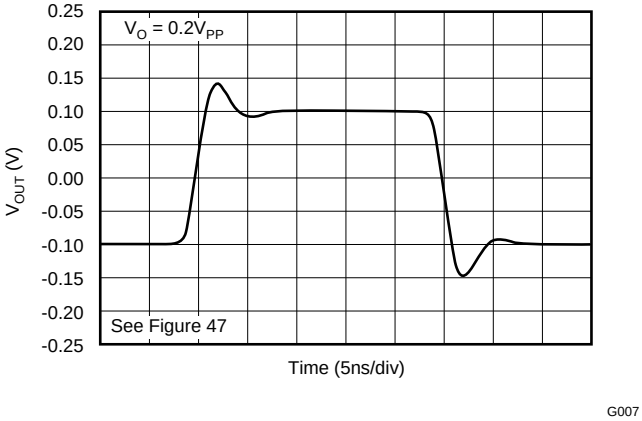

Figure 7.

LARGE-SIGNAL PULSE RESPONSE

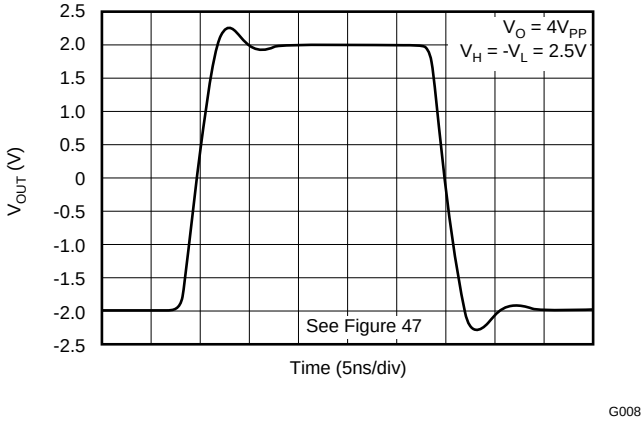

Figure 8.

V_H–LIMITER PULSE RESPONSE

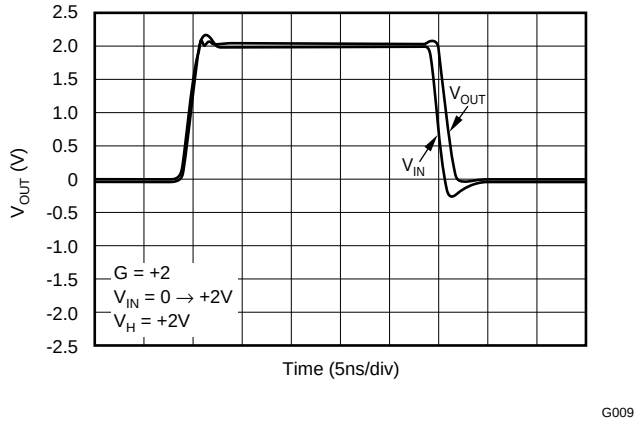

Figure 9.

V_L–LIMITER PULSE RESPONSE (20 MHz)

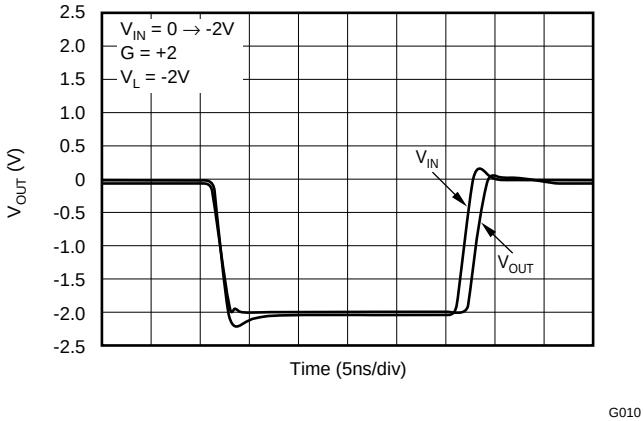

Figure 10.

LIMITED OUTPUT RESPONSE

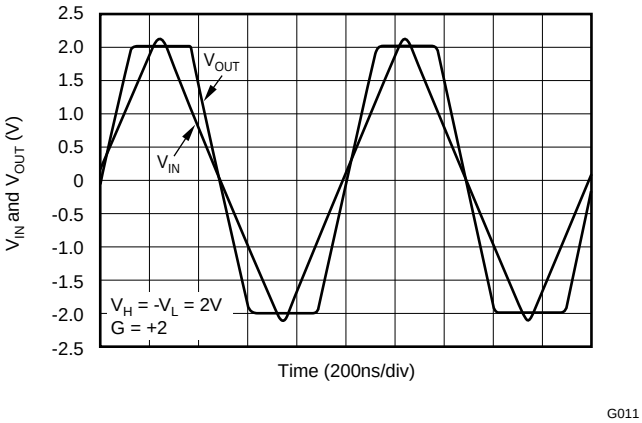

Figure 11.

DETAIL OF LIMITED OUTPUT VOLTAGE

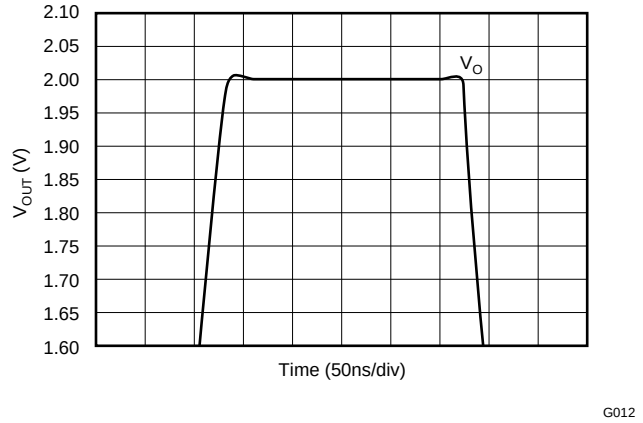

Figure 12.

TYPICAL CHARACTERISTICS — V_S = ±5 V (continued)

5 MHz HARMONIC DISTORTION vs LOAD RESISTANCE

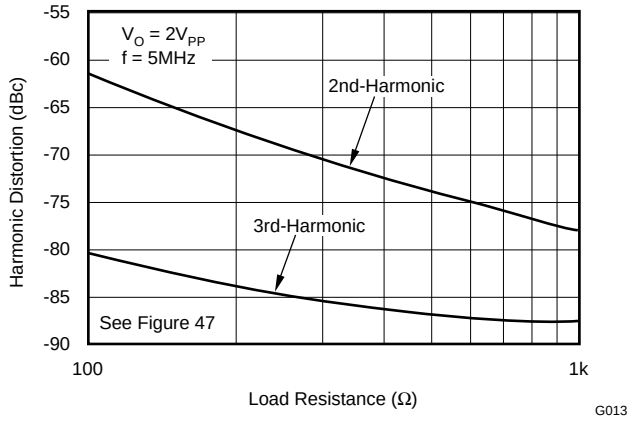

Figure 13.

5 MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

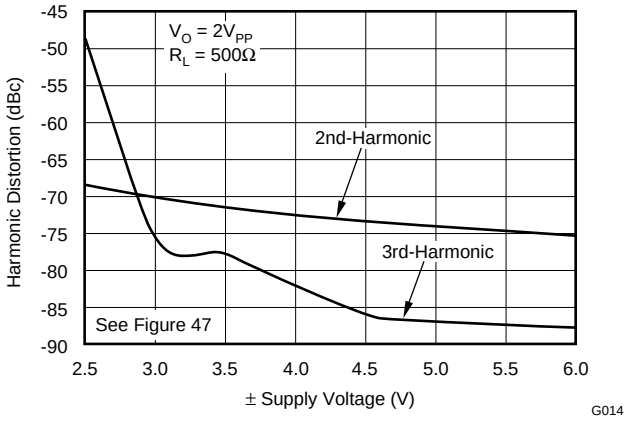

Figure 14.

HARMONIC DISTORTION vs FREQUENCY

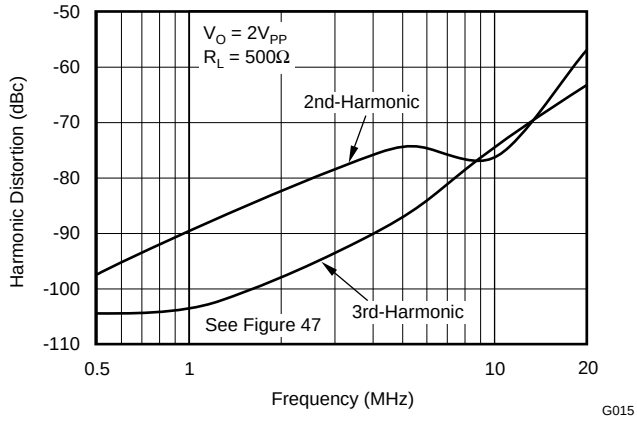

Figure 15.

5 MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

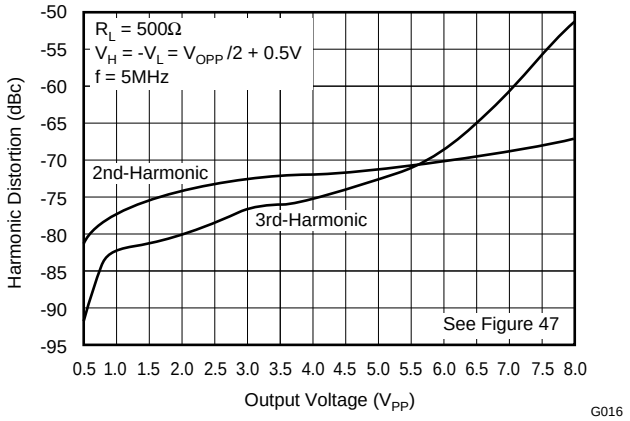

Figure 16.

HARMONIC DISTORTION vs NONINVERTING GAIN

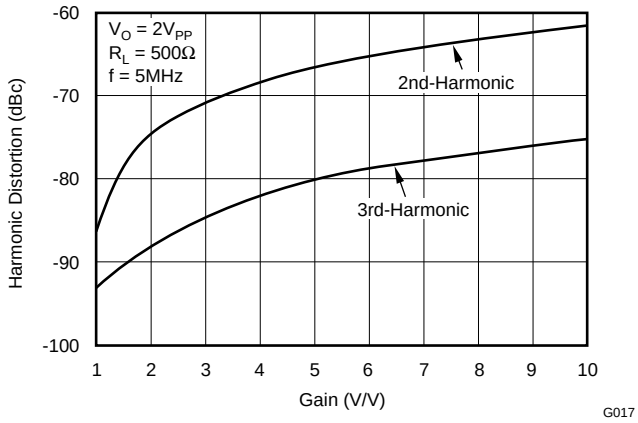

Figure 17.

HARMONIC DISTORTION vs INVERTING GAIN

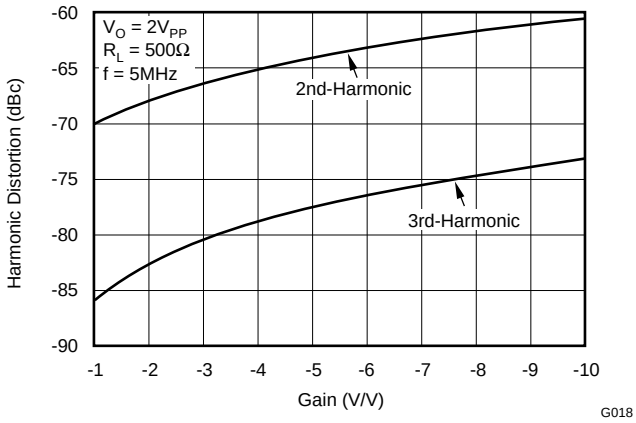

Figure 18.

TYPICAL CHARACTERISTICS — V_S = ±5 V (continued)

HARMONIC DISTORTION NEAR LIMITING VOLTAGES

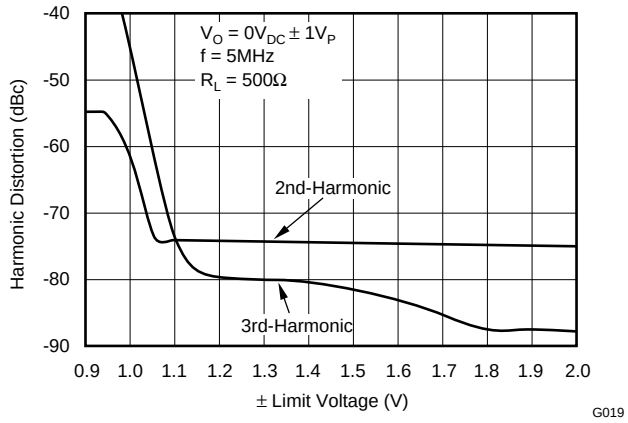

Figure 19.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT ±5 V 500 Ω

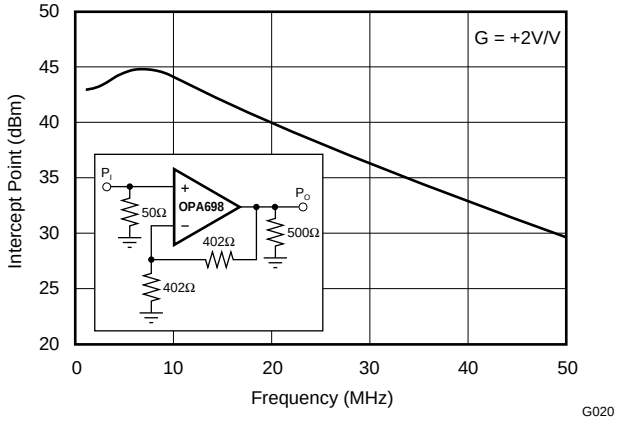

Figure 20.

RECOMMENDED R_S vs CAPACITIVE LOAD

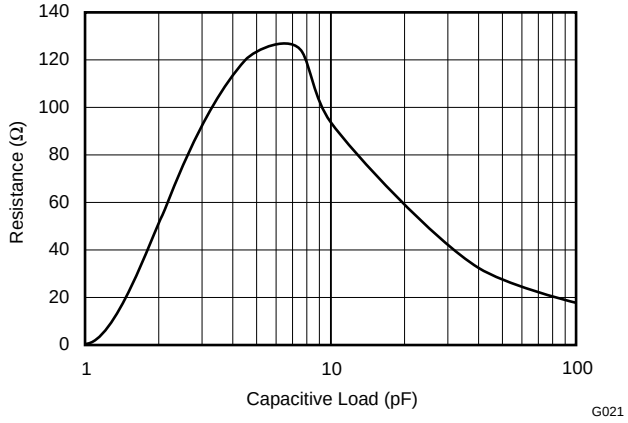

Figure 21.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

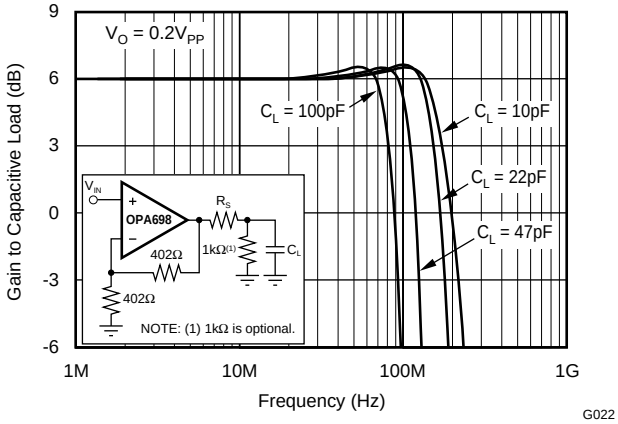

Figure 22.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

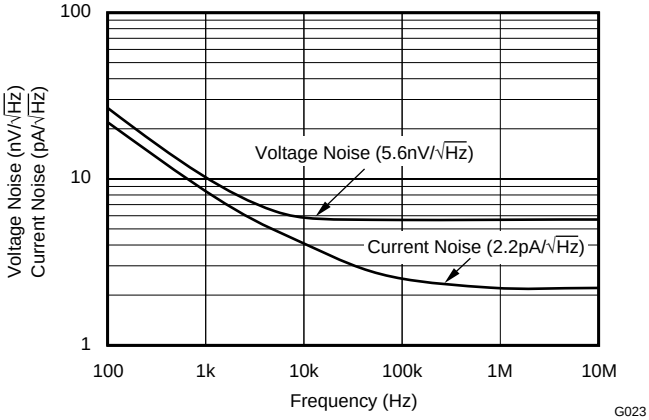

Figure 23.

OPEN-LOOP FREQUENCY RESPONSE

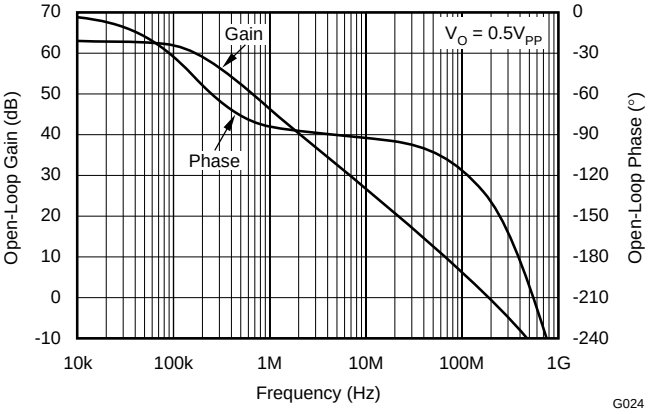

Figure 24.

TYPICAL CHARACTERISTICS — V_S = ±5 V (continued)

VOLTAGE RANGE vs TEMPERATURE

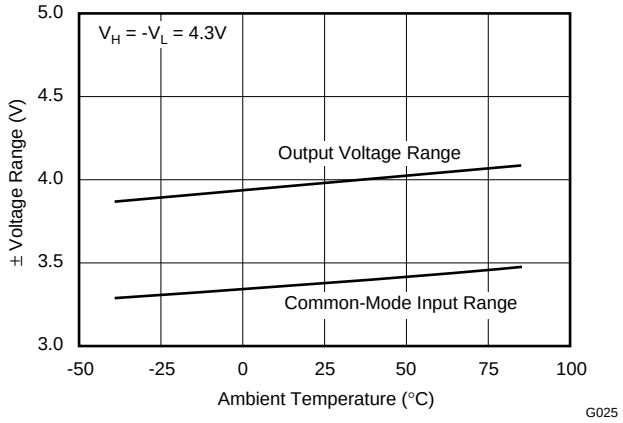

Figure 25.

LIMITED VOLTAGE RANGE vs TEMPERATURE

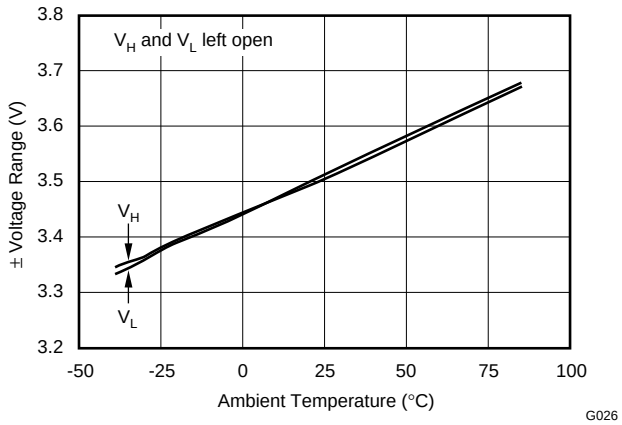

Figure 26.

LIMITED INPUT BIAS CURRENT vs BIAS VOLTAGE

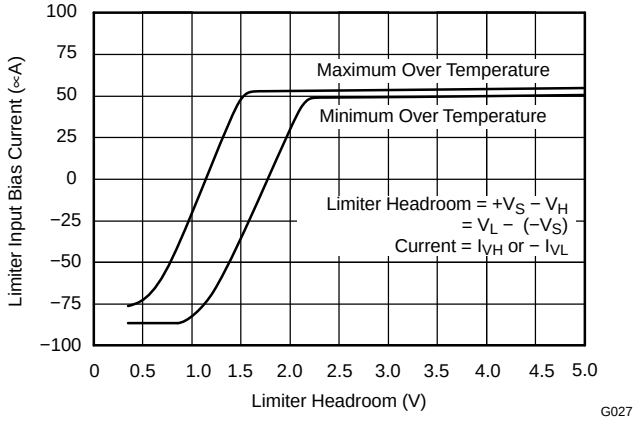

Figure 27.

SUPPLY AND OUTPUT CURRENTS vs TEMPERATURE

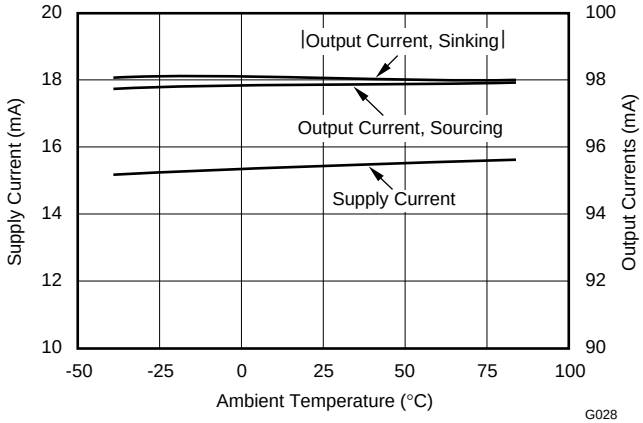

Figure 28.

CMMR AND POWER-SUPPLY REJECTION vs FREQUENCY

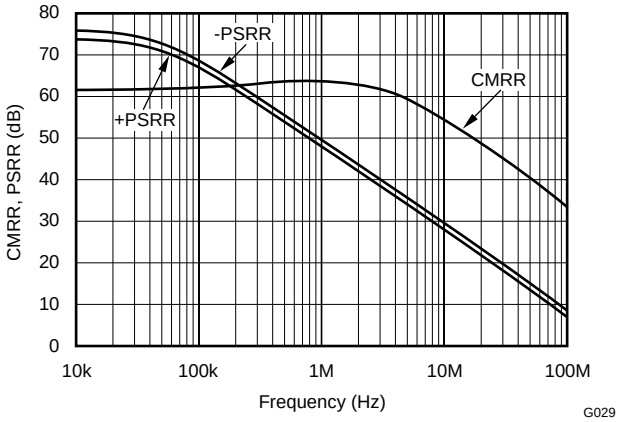

Figure 29.

TYPICAL DC DRIFT OVER TEMPERATURE

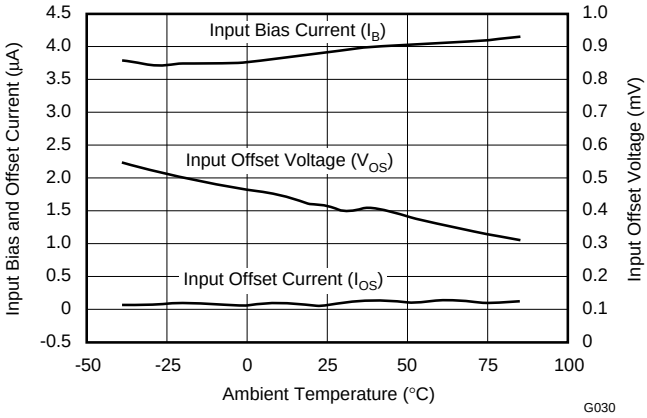

Figure 30.

TYPICAL CHARACTERISTICS — V_S = ±5 V (continued)

LIMITER FEEDTHROUGH

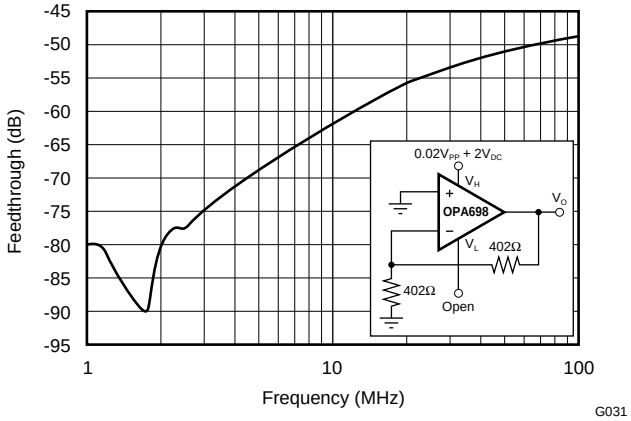

Figure 31.

CLOSED-LOOP OUTPUT IMPEDANCE

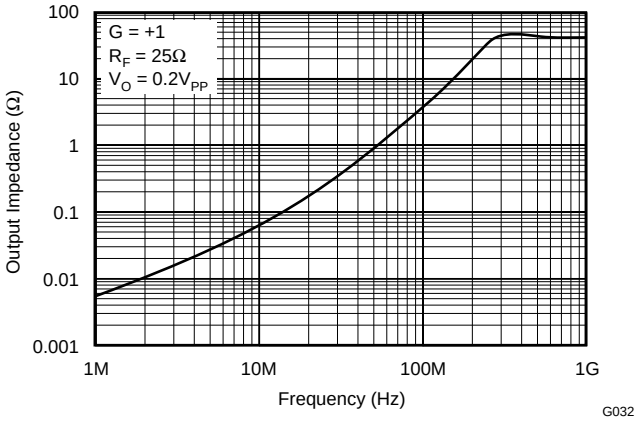

Figure 32.

±PSRR AND CMRR vs TEMPERATURE

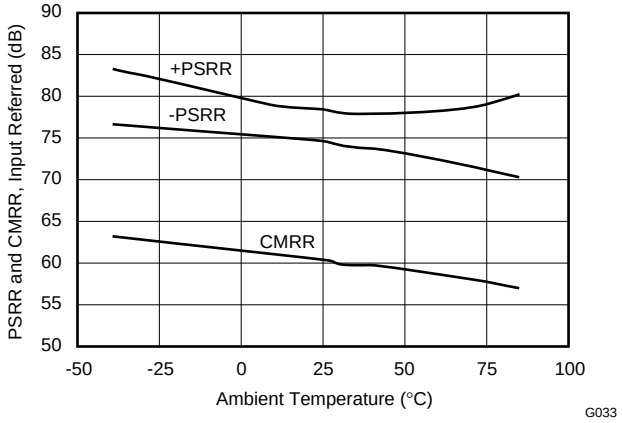

Figure 33.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

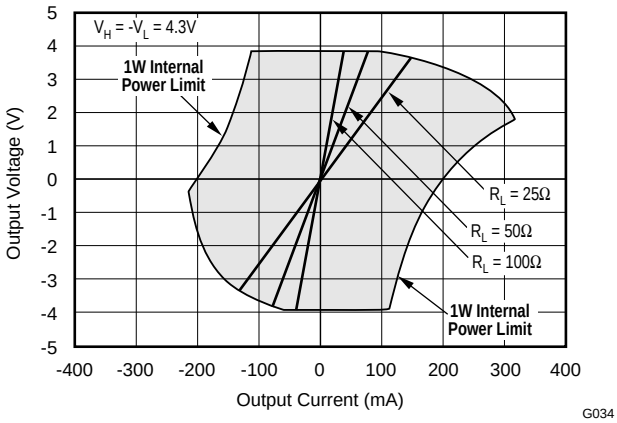

Figure 34.

TYPICAL CHARACTERISTICS — V_S = +5 V

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

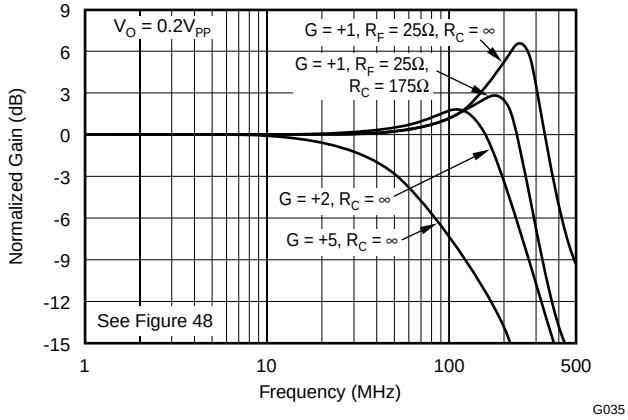

Figure 35.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

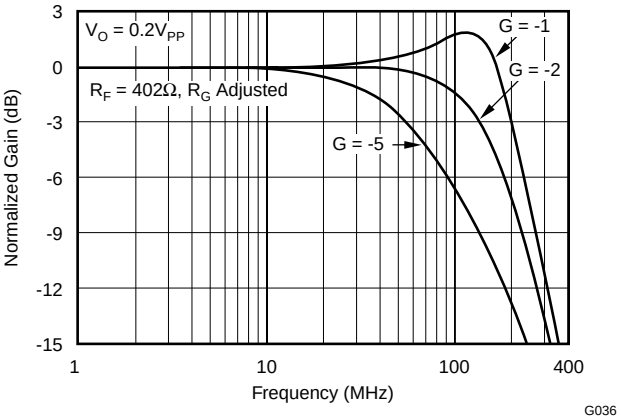

Figure 36.

TYPICAL CHARACTERISTICS — V_S = +5 V (continued)

LARGE-SIGNAL FREQUENCY RESPONSE

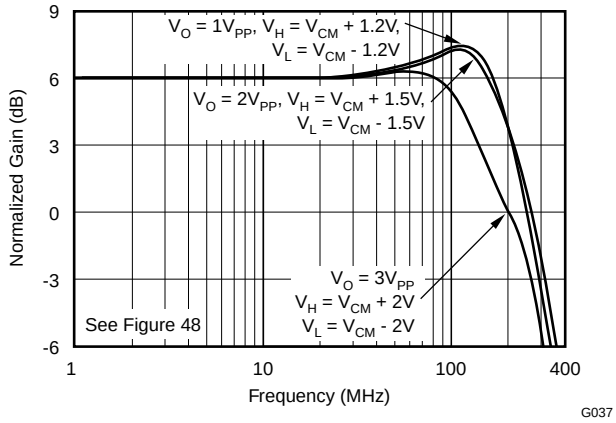

Figure 37.

SMALL-SIGNAL PULSE RESPONSE

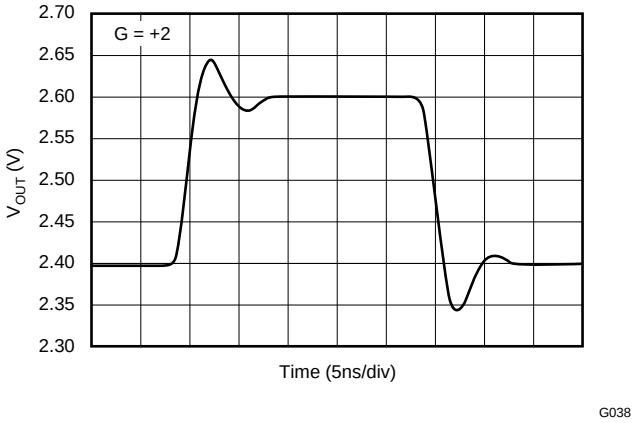

Figure 38.

LARGE-SIGNAL PULSE RESPONSE

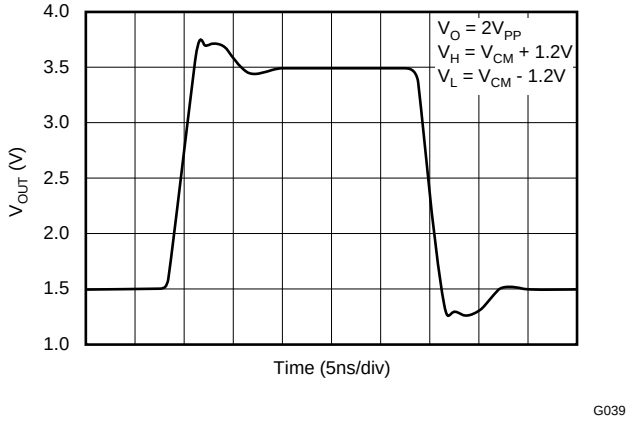

Figure 39.

V_H AND V_L– LIMITED PULSE RESPONSE

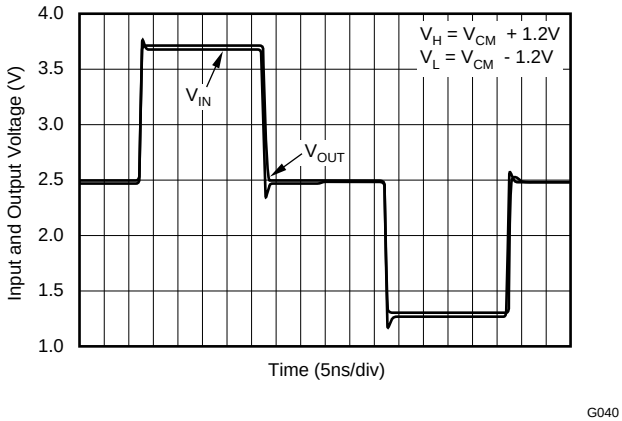

Figure 40.

HARMONIC DISTORTION vs LOAD RESISTANCE

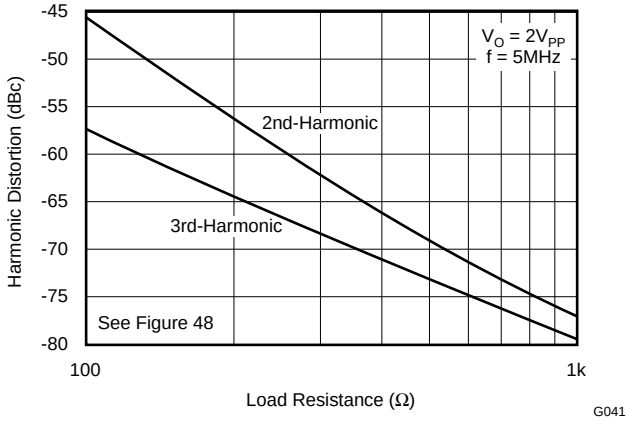

Figure 41.

HARMONIC DISTORTION vs FREQUENCY

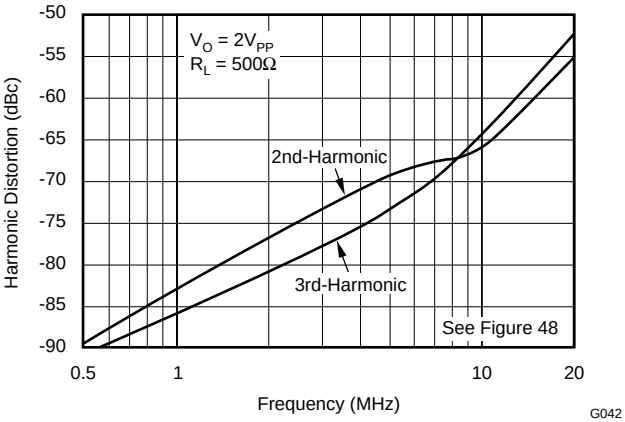

Figure 42.

TYPICAL CHARACTERISTICS — V_S = +5 V (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE

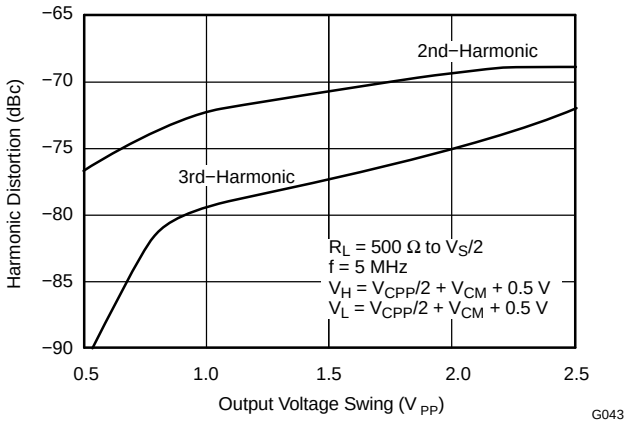

Figure 43.

2-TONE, 3RD ORDER INTERMODULATION INTERCEPT

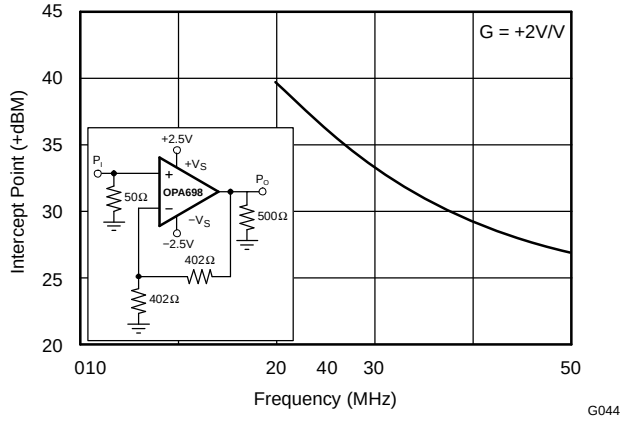

Figure 44.

HARMONIC DISTORTION NEAR LIMITING VOLTAGES

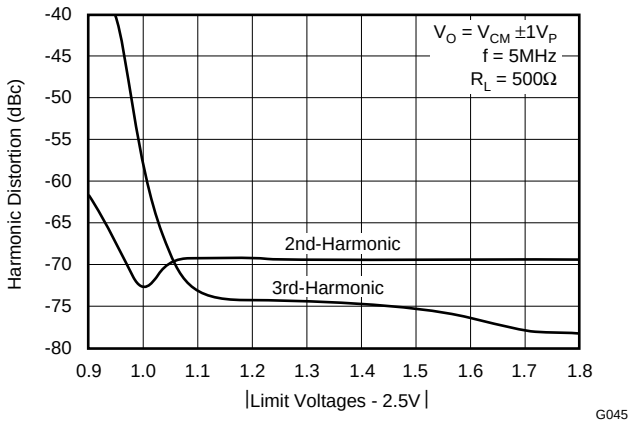

Figure 45.

LIMITER INPUT BIAS CURRENT vs BIAS VOLTAGE

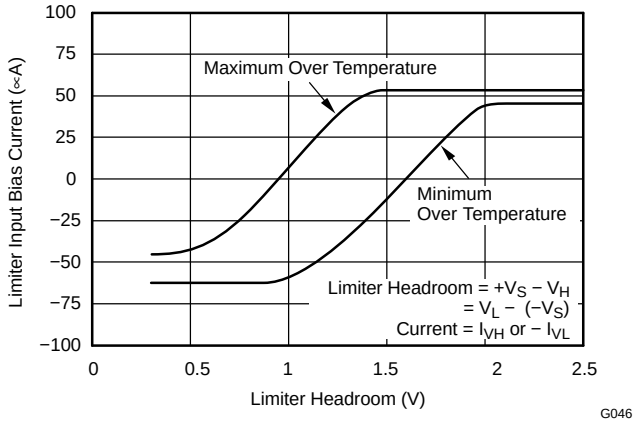

Figure 46.

TYPICAL APPLICATIONS

Wideband Voltage Limiting Operation

The OPA698 is a voltage feedback amplifier that combines features of a wideband, high slew rate amplifier with output voltage limiters. Its output can swing up to 1 V from each rail and can deliver up to 120 mA. These capabilities make it an ideal interface to drive ADC, while adding overdrive protection for the ADC inputs.

Figure 47 shows the dc-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5-V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50 Ω with a resistor to ground and the output impedance is set to 500 Ω. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 47, the total output load is 500 Ω || 804 Ω = 308 Ω. The voltage limiting pins are set to ±2 V through a voltage divider network between the $+V_S$ and ground for V_H and between $–V_S$ and ground for V_L. These limiter voltages are adequately bypassed with a 0.1-µF ceramic capacitor to ground. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. One additional component is included in Figure 47. An additional resistor (174 Ω) is included in series with the noninverting input. Combined with the 25-Ω dc-source resistance looking back towards the signal generator, this gives an input bias current-cancelling resistance that matches the 200-Ω source resistance seen at the inverting input (see the dc accuracy and offset control section). The power-supply bypass

TYPICAL APPLICATIONS (continued)

for each supply consists of two capacitors: one electrolytic 2.2 µF and one ceramic 0.1 µF. The supply bypass capacitors are shown explicitly in Figure 47 and Figure 48, but is assumed in the other figures. An additional 0.01-µF power-supply decoupling capacitor (not shown here) can be included between the two power-supply pins. In practical PC board layouts; this optional-added capacitor typically improves the 2nd harmonic distortion performance by 3 dB to 6 dB.

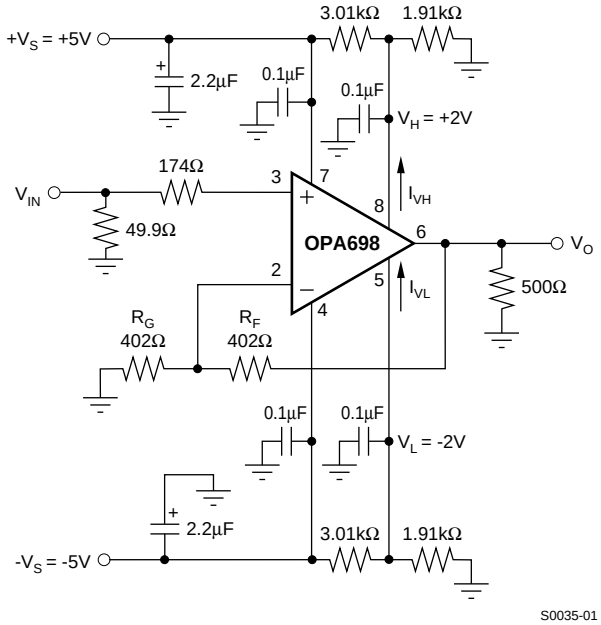

Figure 47. DC-Coupled, Dual-Supply Amplifier

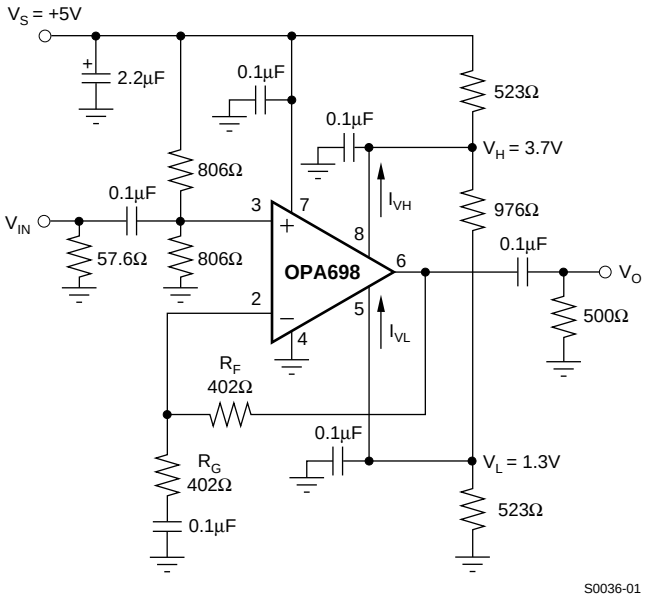

Figure 48. AC-Coupled, Single-Supply Amplifier

Single Supply, Noninverting Amplifier

Figure 48 shows an ac-coupled, noninverting gain amplifier for single +5-V supply operation. This circuit was used for ac characterization of the OPA698, with a 50-Ω source (which it matches) and a 500-Ω load. The

TYPICAL APPLICATIONS (continued)

mid-point reference on the noninverting input is set by two 806-Ω resistors. This gives an input bias current-canceling resistance that matches the 402-Ω dc-source resistance seen at the inverting input (see the dc accuracy and offset control section). The power-supply bypass for the supply consists of two capacitors: one electrolytic 2.2 µF and one ceramic 0.1 µF. The power-supply bypass capacitors are shown explicitly in Figure 47 and Figure 48, but is assumed in the other figures. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. These limiter voltages are adequately bypassed with a 0.1 µF ceramic capacitor to ground. Notice that the single-supply circuit can use three resistors to set V_H and V_L, where the dual-supply circuit usually uses four to reference the limit voltages to ground. While this circuit shows +5-V operation, the same circuit may be used for single supplies up to +12 V.

Wideband Inverting Operation

Operating the OPA698 as an inverting amplifier has several benefits and is particularly useful when a matched 50-Ω source and input impedance are required. Figure 49 shows the inverting gain of –2 circuit used as the basis of the inverting mode typical characteristics.

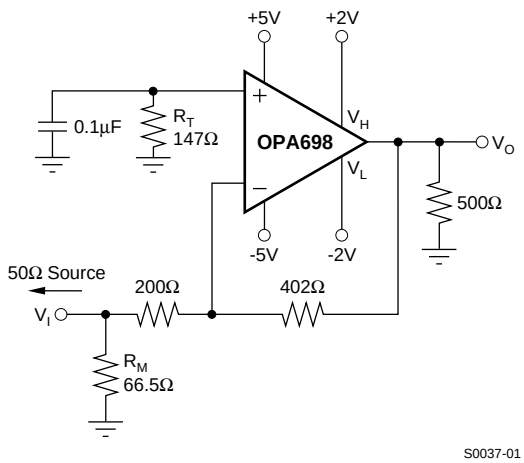

Figure 49. Inverting G = –2 Specifications and Test Circuit

In the inverting case, only the feedback resistor appears as part of the total output load in parallel with the actual load. For a 500-Ω load used in the typical characteristics, this gives a total load of 222 Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case, 200 Ω for a gain of –2); while an additional input resistor (R_M) can be used to set the total input impedance equal to the source, if desired. In this case, R_M = 66.5 Ω in parallel with the 200-Ω gain setting resistor gives a matched input impedance of 50 W. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 49.

For bias current-cancellation matching, the noninverting input requires a 147-Ω resistor to ground. The calculation for this resistor includes a dc-coupled 50-Ω source impedance along with R_G and R_M. Although this resistor provides cancellation for the bias current, it must be well decoupled (0.1 µF in Figure 49) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50 Ω at higher gains, the bandwidth for the circuit in Figure 49 far exceeds the bandwidth at that same gain magnitude for the noninverting circuit of Figure 47. This occurs due to the lower noise gain for the circuit of Figure 49 when the 50-Ω source impedance is included in the analysis. For instance, at a signal gain of –8 (R_G = 50 Ω, R_M = open, R_F = 402 Ω) the noise gain for the circuit of Figure 49 will be 1 + 402 Ω/(50 Ω + 50 Ω) = 5 due to the addition of the 50-Ω source in the noise gain equation. This approach gives considerably higher bandwidth than the noninverting gain of +8. Using the 250-MHz gain bandwidth product for the OPA698, an inverting gain of –8 from a 50-Ω source to a 50 Ω R_G gives 52-MHz bandwidth, whereas the noninverting gain of +8 gives 28 MHz, as shown in Figure 50.

TYPICAL APPLICATIONS (continued)

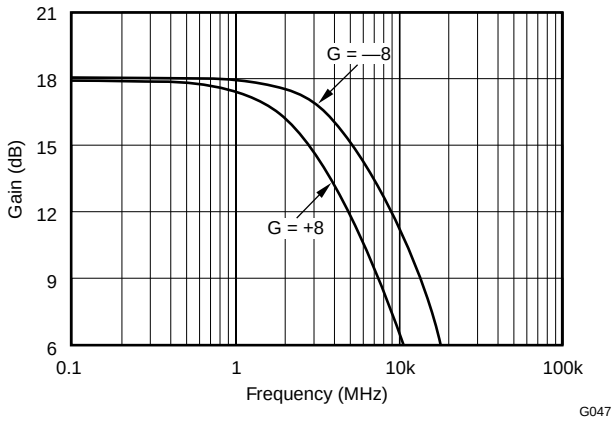

Figure 50. G = +8 and –8 Frequency Response

Limited Output, ADC Input Driver

Figure 51 shows a simple ADC driver that operates on a single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive. Note that the limiting voltages have been set 100 mV above/below the corresponding reference voltage from the converter.

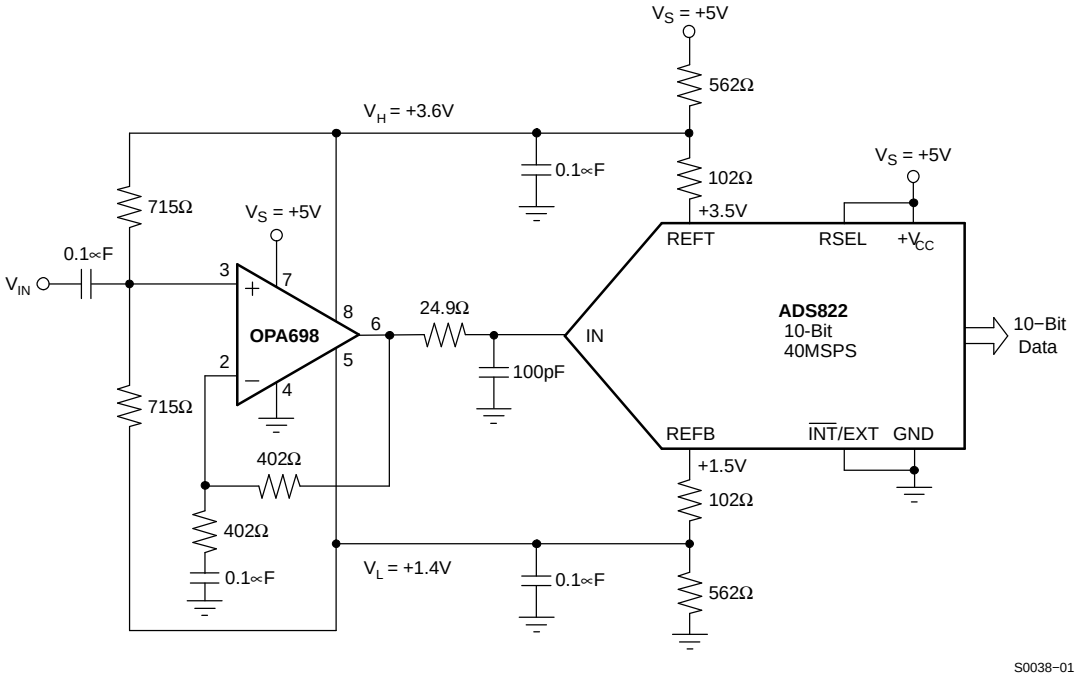

Figure 51. Single Supply, Limiting ADC Input Driver

Limited Output, Differential ADC Input Driver

Figure 52 shows a differential ADC driver that takes advantage of the OPA698 limiters to protect the input of the ADC.

TYPICAL APPLICATIONS (continued)

Two OPA698s are used. The first one is an inverting configuration at a gain of –2. The second one is in a noninverting configuration at a gain of +2. Each amplifier is swinging 2 V_{PP} providing a 4-V_{PP} differential signal to drive the input of the ADC. Limiters have been set 100 mV away from the magnitude of each amplifier's maximum signal to provide input protection for the ADC, while maintaining an acceptable distortion level.

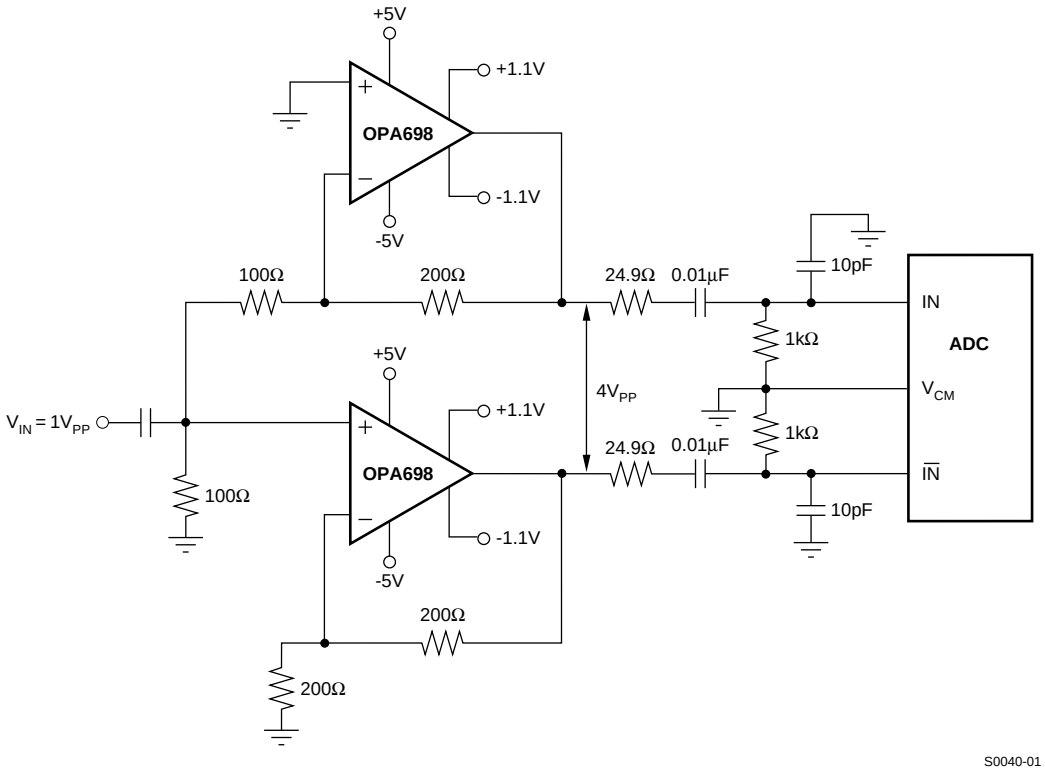

Figure 52. Single-to-Differential AC-Coupled, Output Limited ADC Driver

Precision Half-Wave Rectifier

Figure 53 shows a half-wave rectifier with outstanding precision and speed. V_H (pin 8) defaults to a voltage between 3.1 V and 3.8 V if left open, while the negative limit is set to ground.

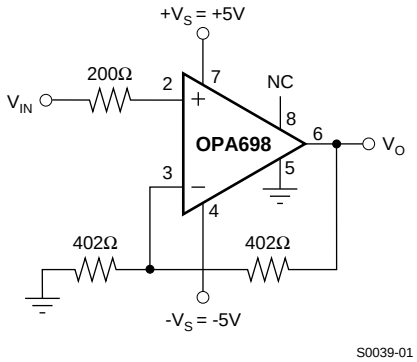

Figure 53. Precision Half-Wave Rectifier

The gain for the circuit in Figure 53 is set at +2. Figure 54 shows a 100-MHz sine-wave amplifier, with a gain of +2 and rectified.

TYPICAL APPLICATIONS (continued)

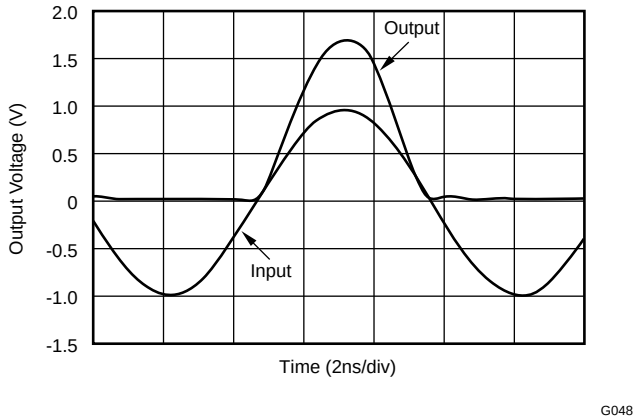

Figure 54. 100-MHz Sine Wave Rectified

High-Speed Full-Wave Rectifier

There are two methods shown here to build a high-speed full-wave rectifier with a limiting amplifier: use the half-wave rectifier described previously with another amplifier to obtain the full-wave rectified, or use the input to set the limiting voltage.

High-Speed Full-Wave Rectifier #1

The circuit shown in Figure 55 uses only one amplifier, in an inverting gain of –1 configuration. The upper limiting voltage is left open, resulting in an upper limiting voltage of +3.5 V. The lower limiting voltage is connected to the input signal, resulting in the following behavior. When the input voltage is negative, the amplifier is not limiting, resulting in the inversion of the input sine wave to the output. During the positive excursion of the input signal, the output signal is being driven by the limiting input pin. Since the output is driven from the limiter input pin from positive inputs, the lower slew rate in the input path restricts the application of this approach to lower amplitude and/or frequencies. A 2-MHz fully rectified sine wave is shown in Figure 56.

In order to reach higher frequencies, a second method is recommended.

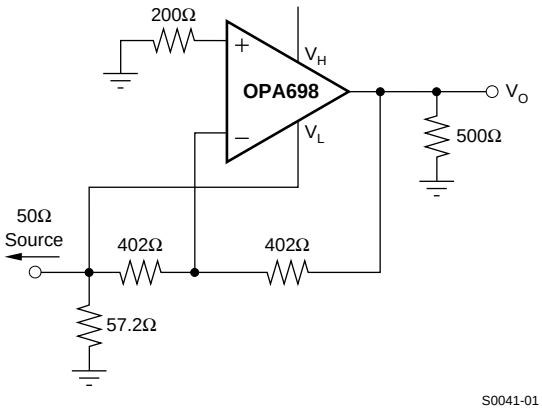

Figure 55. High-Speed Full-Wave Rectifier #1

TYPICAL APPLICATIONS (continued)

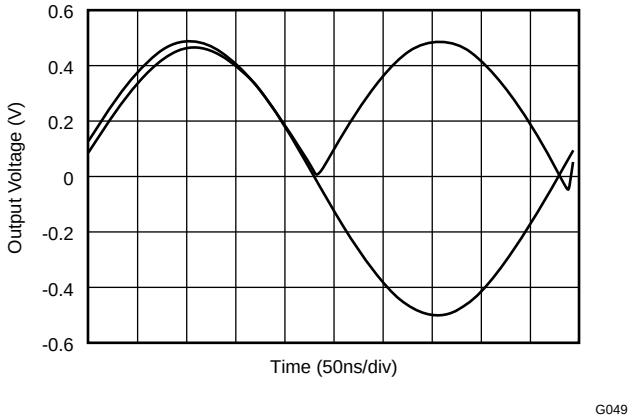

Figure 56. 2-MHz Sinewave Rectified

High-Speed Full-Wave Rectifier #2

The circuit shown in Figure 57 combines a half-wave rectifier driving the OPA693 in an inverting configuration, while the input signal drives the noninverting input of the fixed gain amplifier OPA693, resulting in a full-wave rectifier function. Results are shown in Figure 58.

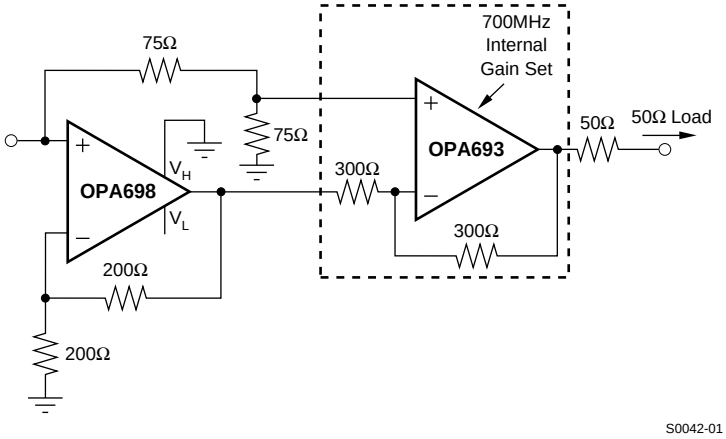

Figure 57. High-Speed Full-Wave Rectifier #2

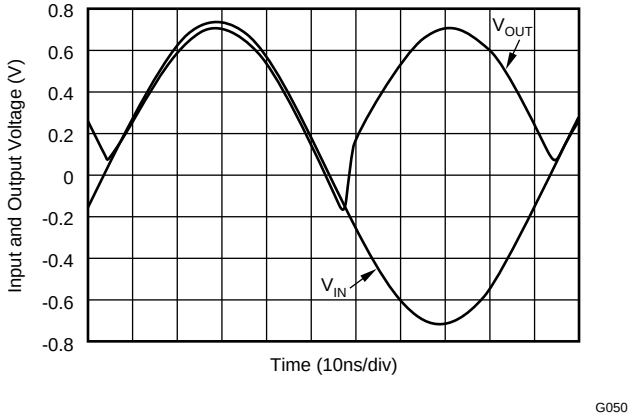

Figure 58. 10-MHz Sinewave Rectified

TYPICAL APPLICATIONS (continued)

If the negative excursion of the rectified signal is not desired, it can easily be removed by replacing the OPA693 with the OPA698 configured as a difference amplifier with V_L connected to ground and V_H left floating.

Soft-Clipping (Compression) Circuit

Figure 59 shows a soft-clipping circuit. As soon as the input voltage exceeds either V_{CH} or V_{CL}, the limiting voltages are driven by Equation 1 and Equation 2.

$$V_H = \frac{R2 \times V_{CH} + R1 \times V_{IN}}{R1 + R2} \quad (1)$$

$$V_L = \frac{R4 \times V_{CL} + R3 \times V_{IN}}{R3 + R4} \quad (2)$$

As the amplifier is operating in the limiting mode, the output voltage is compressed with a gain of R1+R2/R1 for the positive excursion above V_{CH} and by a gain of R3+R4/R3 for the negative excursion below V_{CL}. Figure 60 shows a 5 V_{PP} on the input being compressed above ±1 V with a compression gain of one third.

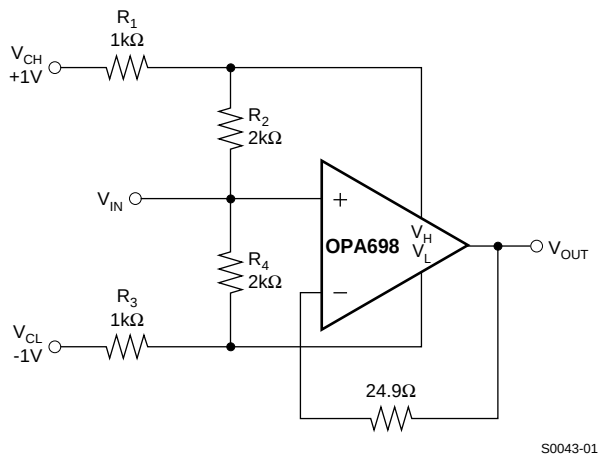

Figure 59. Soft-Clipping Circuit

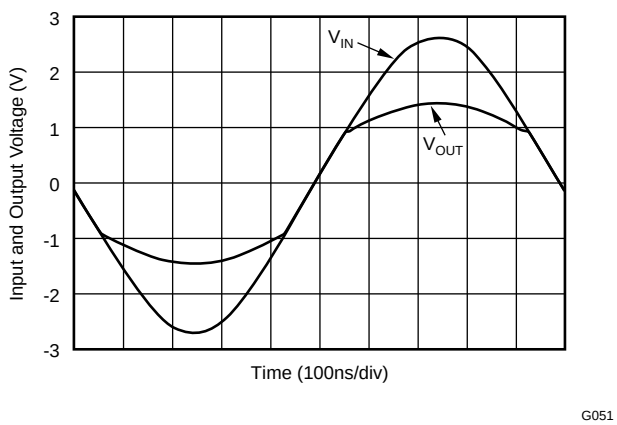

Figure 60. Soft-Clipping With A Gain of 1/3 Above the Clamp Level (±1 V)

High-Speed Schmitt Trigger

Figure 61 shows a high-speed Schmitt Trigger. The output levels are precisely defined and the switching time is exceptional. The output voltage swings between V_H and V_L.

TYPICAL APPLICATIONS (continued)

The circuit operates as follow. When the input voltage is less than V_{HL} then the output is limiting at V_H. When the input is greater than V_{HH} then the output is limiting at V_L, with V_{HL} and V_{HH} defined as the following:

$$V_{HL,HH} = \frac{R1 \parallel R2 \parallel R3}{R1} \times V_{REF} + \frac{R1 \parallel R2 \parallel R3}{R2} \times V_{OUT} \quad (3)$$

Due to the inverting function realized by the Schmitt Trigger, V_{HL} corresponds to $V_{OUT} = V_H$ and V_{HH} corresponds to $V_{OUT} = V_L$.

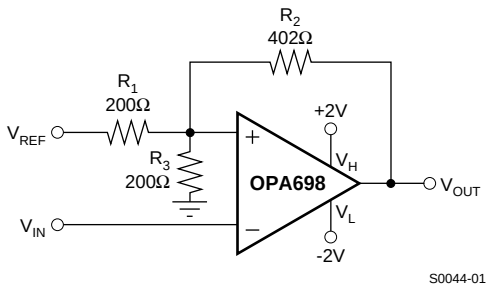

Figure 61. High-Speed Schmitt Trigger

Figure 62 shows the Schmitt Trigger operating with V_{REF} = +5 V. This gives us V_{HH} = 2.4 V and V_{HL} = 1.6 V. The propagation delay for the OPA698 in a Schmitt Trigger configuration is 6 ns from high-to-low and 5 ns from low-to-high.

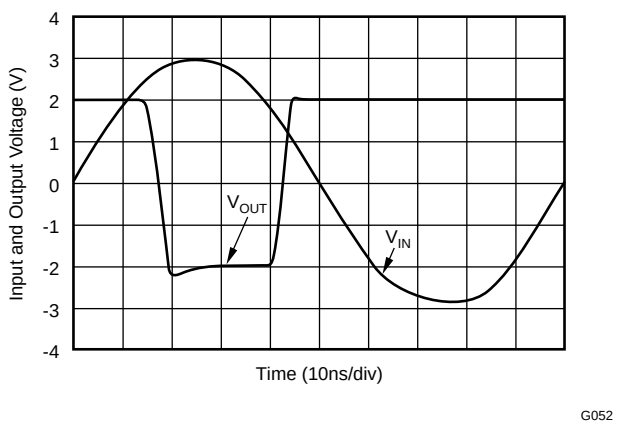

Figure 62. Schmitt Trigger Time Domain Response for a 10-MHz Sinewave

Unity-Gain Buffer

Figure 63 shows a unity-gain voltage buffer using the OPA698. The feedback resistor (R_F) isolates the output from the input capacitance at the inverting input. R_F = 24.9 Ω is recommended for unity-gain buffer applications. R_C is an optional compensation resistor that reduces the peaking typically seen at G = +1. Choosing $R_C = R_S + R_F$ gives a unity-gain buffer with approximately the G = +2 frequency response. The frequency response for this circuit is shown in the electrical characteristics curves.

TYPICAL APPLICATIONS (continued)

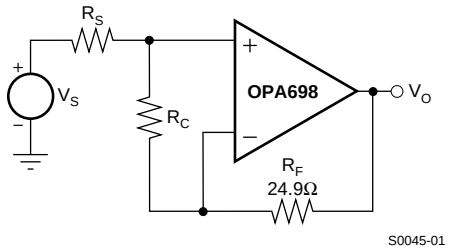

Figure 63. Unity-Gain Buffer

DC Restorer

Figure 64 shows a dc-restore circuit using the OPA698 and OPA660. The buffer element of the OPA660 is used to buffer the input signal, while the transconductance element is used to restore the dc level after the decoupling capacitor C1. The dc level is set using R1 and R2. The OPA698 is configured at a gain of two to compensate for the 75-Ω series into a 75-Ω load. The OPA698 also limits the output to ground.

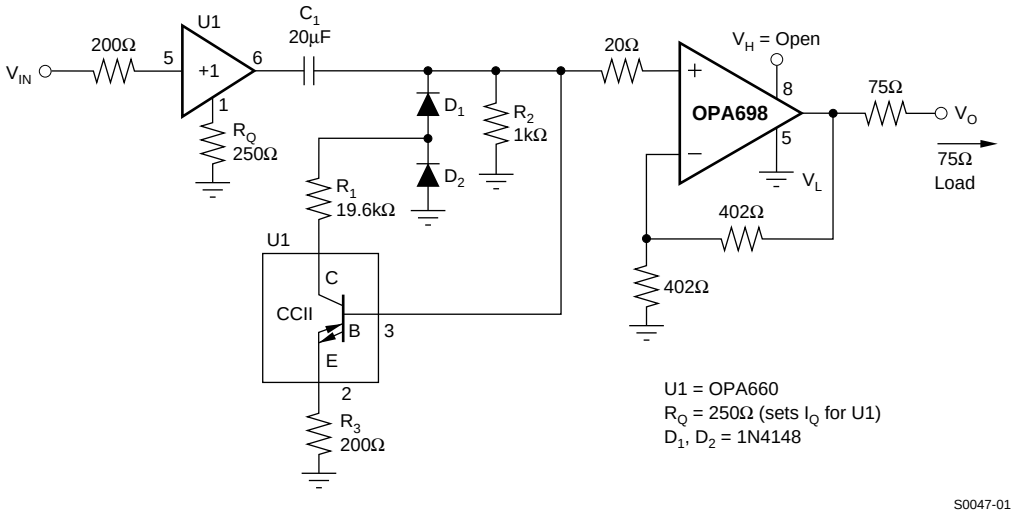

Figure 64. DC Restore to Ground

Video Sync Stripper

Figure 65 shows a sync stripper using two OPA698 output-limiting op amps. One OPA698 is configured as a limiting inverting comparator. Referring to the input, the negative excursions lower than –0.2 V are clipped to ground and all excursions greater than –0.2 V generate an output voltage set by the default limiting value (–3.5 V). The second OPA698 is using this waveform to effectively remove the sync pulse from the video signal.

TYPICAL APPLICATIONS (continued)

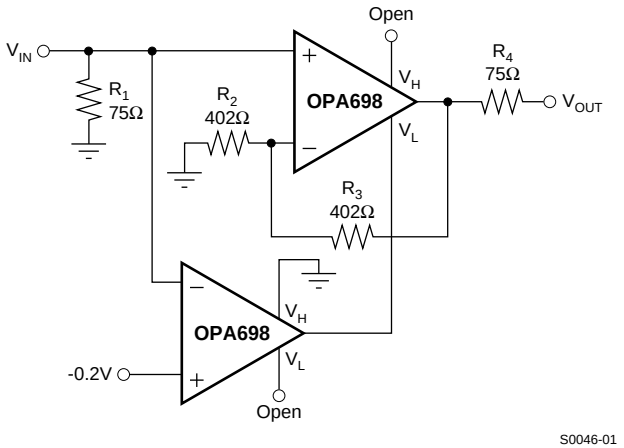

Figure 65. Sync Stripper Circuit

DESIGN-IN TOOLS

Applications Support

The Texas Instruments Applications Department is available for design assistance at 1-972-644-5580. The Texas Instruments web site (www.ti.com) has the latest product data sheets and other design aids.

Demonstrations Boards

A PC board is available to assist in the initial evaluation of circuit performance of the OPA698ID. It is available as an unpopulated PCB with descriptive documentation. See the demonstration board literature for more information. The summary information for this board is shown in Table 1.

Table 1. Demo Board Summary Information

PRODUCT	PACKAGE	BOARD PART NO.	LITERATURE REQUEST NO.
OPA698ID	SO-8	DEM-OPA-SO-1A	SBOU009

This board can be requested through the Texas Instruments web site.

OPERATING SUGGESTIONS

Theory of Operation

The OPA698 is a voltage-feedback op amp that is unity-gain stable. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This action from the limiters avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain. The limiters have a sharp transition from the linear region of operation to output limiting. This transition allows the limiter voltages to be set near (<100 mV) the desired signal range. The distortion performance is also good near the limiter voltages.

Output Limiters

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L. Because the limiters act on the output, their accuracy does not change with gain. The transition from the linear region of operation to output limiting is sharp-the desired output signal can safely come to within 30 mV of V_H or V_L with no onset of non-linearity. The limiter voltages can be set to within 0.7 V of the supplies ($V_L \geq -V_S + 0.7$ V, $V_H \leq +V_S - 0.7$ V). They must also be at least 400 mV apart ($V_H - V_L \geq 0.4$ V). When pins 5 and 8 are left open, V_H and V_L go to the default voltage limit; the minimum values are given in the electrical specifications. Looking at Figure 66 for the zero bias current case shows the expected range of (V_S– default limit voltages) = headroom.

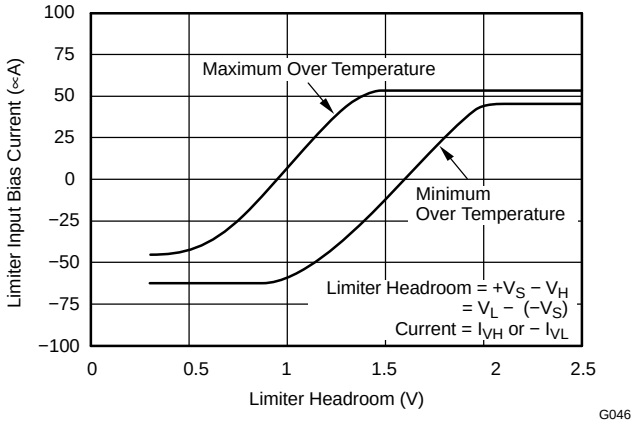

Figure 66. Limiter Bias Current vs Bias Voltage

When the limiter voltages are more than 2.1 V from the supplies ($V_L \geq -V_S + 2.1$ V or $V_H \leq +V_S - 2.1$ V), you can use simple resistor dividers to set V_H and V_L (see Figure 47). Make sure to include the limiter input bias currents (see Figure 54) in the calculations (that is, I_{VL} = –50 µA out of pin 5 and I_{VH} = +50 µA out of pin 8). For good limiter voltage accuracy, run at least 1-mA quiescent bias current through these resistors. When the limiter voltages need to be within 2.1 V of the supplies ($V_L \leq -V_S + 2.1$ V or $V_H \geq +V_S - 2.1$ V), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This condition is typically the case for single-supply operation (V_S = +5 V). Figure 48 runs 2.5 mA through the resistive divider that sets V_H and V_L. This limits errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages. The limiters' dc accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (for example, ±5%). Using a more accurate source and bypassing pins 5 and 8 with good capacitors improves limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.
- Other error sources also contribute, but should have little impact on the limiters' dc accuracy:
- Reduce offsets caused by the limiter input bias currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path dc errors as contributing to uncertainty in the usable output swing.
- The limiter offset voltage only slightly degrades limiter accuracy. Figure 67 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages.

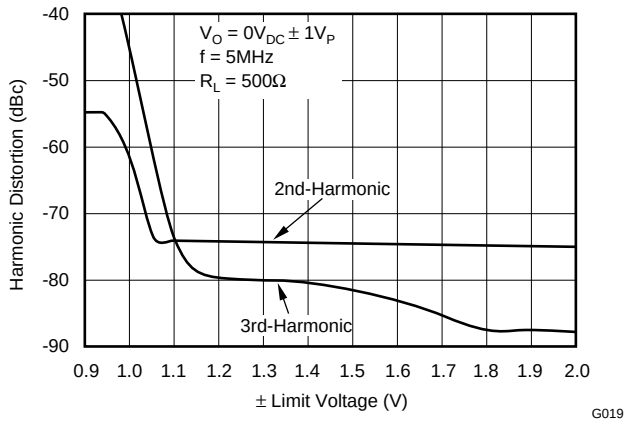

Figure 67. Harmonic Distortion Near Limit Voltages

Output Drive

The OPA698 has been optimized to drive 500-Ω loads, such as ADCs. It still performs well driving 100-Ω loads; the specifications are shown for the 500-Ω load. This makes the OPA698 an ideal choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. As shown in the typical performance curve Output Impedance vs Frequency, the OPA698 maintains low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency, since loop gain decreases with frequency.

Thermal Considerations

The OPA698 does not require heat sinking under most operating conditions. Maximum desired junction temperature sets a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}), while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage and not in the load, that determines internal power dissipation.

The operating junction temperature is: $T_J = T_A + P_D \times \theta_{JA}$, where T_A is the ambient temperature. For example, the maximum T_J for a OPA698ID with G = +2, R_F = 402 Ω, R_L = 100 Ω, and $\pm V_S = \pm 5$ V at T_A = +85°C is calculated as:

$$P_{DO} = (10\ V \times 15.5\ mA) = 155\ mW$$

$$P_{DL} = \frac{(5V)^2}{4 \times (100\ \Omega \parallel 804\ \Omega)} = 70\ mW$$

$$P_D = 155\ mW + 70\ mW = 225\ mW$$

$$T_J = 85^oC + 225\ mW \times 125^oC/W = 113^oC \quad (4)$$

This would be the maximum T_J from $V_O = \pm 2.5\ V_{DC}$. Most applications will be at a lower output stage power and have a lower T_J. Care must be taken when operating at higher ambient temperatures.

Capacitive Loads

Capacitive loads, such as the input to ADCs, decreases the amplifier phase margin, which may cause high-frequency peaking or oscillations. Capacitive loads ≥2 pF should be isolated by connecting a small resistor in series with the output, as shown in Figure 68. Increasing the gain from +2 improves the capacitive drive capabilities due to increased phase margin.

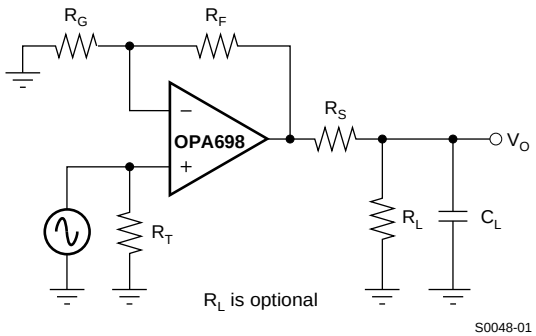

Figure 68. Driving Capacitive Loads

In general, capacitive loads should be minimized for optimum high-frequency performance. The capacitance of coax cable (29 pF/ft for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

Frequency Response Compensation

The OPA698 is internally compensated to be unity-gain stable, and has a nominal phase margin of 60° at a gain of +2. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes (that is, noise gain = 2). Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a wide bandwidth at high gains, cascade several op amps, or use the high-gain optimized OPA699.

In applications where a large feedback resistor is required, such as photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high-gain applications, use a three resistor Tee network to reduce the RC time constants set by the parasitic capacitances. Be careful not to increase the noise generated by this feedback network too much.

Pulse Settling Time

The OPA698 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve RS vs Capacitive Load. Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics, when recovering from overdrive, are good.

Distortion

The OPA698 distortion performance is specified for a 500-Ω load, such as an ADC. Driving loads with smaller resistance increases the distortion, as illustrated in Figure 69. Remember to include the feedback network in the load resistance calculations.

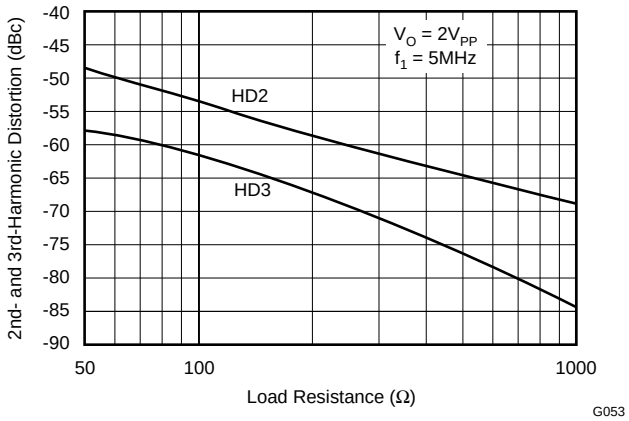

Figure 69. 5-MHz Harmonic Distortion vs Load Resistance

Noise Performance

High slew rate, unity-gain stable, voltage feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 5.6-nV/√Hz input voltage noise for the OPA698, however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 70 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

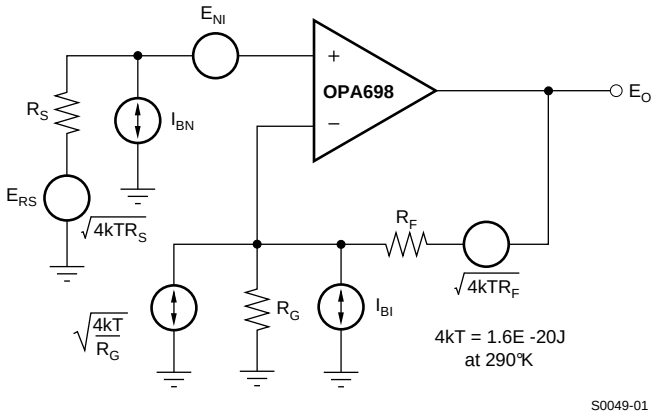

Figure 70. 5-MHz Harmonic Distortion vs Load Resistance

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 5 shows the general form for the output noise voltage using the terms shown in Figure 70.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_F NG} \quad (5)$$

Dividing this expression by the noise gain [NG = $(1+R_F/R_G)$] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 6.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (6)$$

Evaluating these two equations for the OPA698 circuit and component values (see Figure 47) gives a total output spot noise voltage of 11.9 nV/√Hz and a total equivalent input spot noise voltage of 6 nV/√Hz. This total input-referred spot noise voltage is only slightly higher than the 5.6 nV/√Hz specification for the op amp voltage noise alone. This is the case as long as the impedances appearing at each op amp input is limited to a maximum value of 300 Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300 Ω satisfies both noise and frequency response flatness considerations. Since the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_T) for the inverting op amp configuration of Figure 49 is not required, but is still desirable.

DC Accuracy and Offset Control

The balanced input stage of a wideband voltage feedback op amp allows good output dc accuracy in a large variety of applications. The power-supply current trim for the OPA698 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically ±8 µA at each input terminal), the close matching between them may be used to reduce the output dc error caused by this current. The total output offset voltage may be considerably reduced by matching the dc source resistances appearing at the two inputs. This reduces the output dc error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 47, using a worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

– (NG = noninverting signal gain)

$\pm$ (NG × $V_{IO(MAX)}$) ± [R_F x $I_{IO(MAX)}$]

= ±(2 × 8 mV) ± (402 Ω × 3 µA)

= ±17.2 mV

A fine-scale output offset null or dc operating point adjustment is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques eventually reduce to adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the dc offset voltage on the summing junction sets up a dc current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a dc-coupled inverting amplifier, Figure 71 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the dc offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This insures that the adjustment circuit has minimal effect on the loop gain as well as the frequency response.

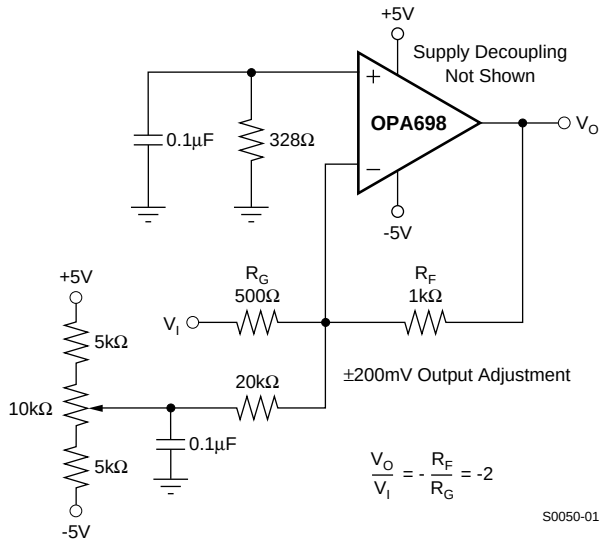

Figure 71. DC-Coupled, Inverting Gain of -2, With Offset Adjustment

Board Layout Guidelines

Achieving optimum performance with the high-frequency OPA698 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

1. **Minimize parasitic capacitance to any ac ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins and leave the ground and power planes unbroken elsewhere.
2. **Provide a high quality power supply.** Use linear regulators, ground plane and power planes to provide power. Place high frequency 0.1-µF decoupling capacitors < 0.2" away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2 µF to 6.8 µF) high-frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.
3. **Place external components close** to the OPA698. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.
4. **Use high-frequency components** to minimize parasitic elements. Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wire-wound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances. Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work well. Use R_F type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2 µF to 6.8 µF) should be tantalum for better high frequency and pulse performance.
5. **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2-pF parasitic parallel capacitance. For resistors > 1.5 kΩ, this adds a pole and/or zero below 500 MHz. Make sure that the output loading is not too heavy. The recommended 402-Ω feedback resistor is a good starting point in most designs.
6. **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the typical performance curve, *R_S vs Capacitive Load*. Parasitic loads < 2 pF may not need the isolation resistor.
7. **When long traces are necessary**, use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω transmission line is not required on board—higher characteristic impedance helps reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line and a matched load resistor at the other end to make the line appear as a resistor. If the 6 dB of attenuation that the matched load produces is not acceptable and the line is not too long, use the series resistor at the source only. This isolates the source from the reactive load presented by the line, but the frequency response is degraded. Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors alters the transmission line match and can cause unwanted signal reflections and reactive loading.
8. **Do not use sockets** for high-speed parts like the OPA698. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

Power Supplies

The OPA698 is nominally specified for operation using either ±5-V supplies or a single +5-V supply. The maximum specified total supply voltage of 12 V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common-mode voltage constraints are observed. The common-mode input and output voltage specifications can be interpreted as required headroom to the supply voltage. Observing this input and output headroom requirement allows design of non-standard or single-supply operation circuits. Figure 48 shows one approach to single-supply operation.

Input and ESD Protection

ESD damage has been known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This is particularly true for high-speed, fine geometry processes. ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA698.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA698MJD	Active	Production	CDIP SB (JD) | 8	45 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	OPA698MJD
OPA698MJD.A	Active	Production	CDIP SB (JD) | 8	45 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	OPA698MJD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF OPA698M :

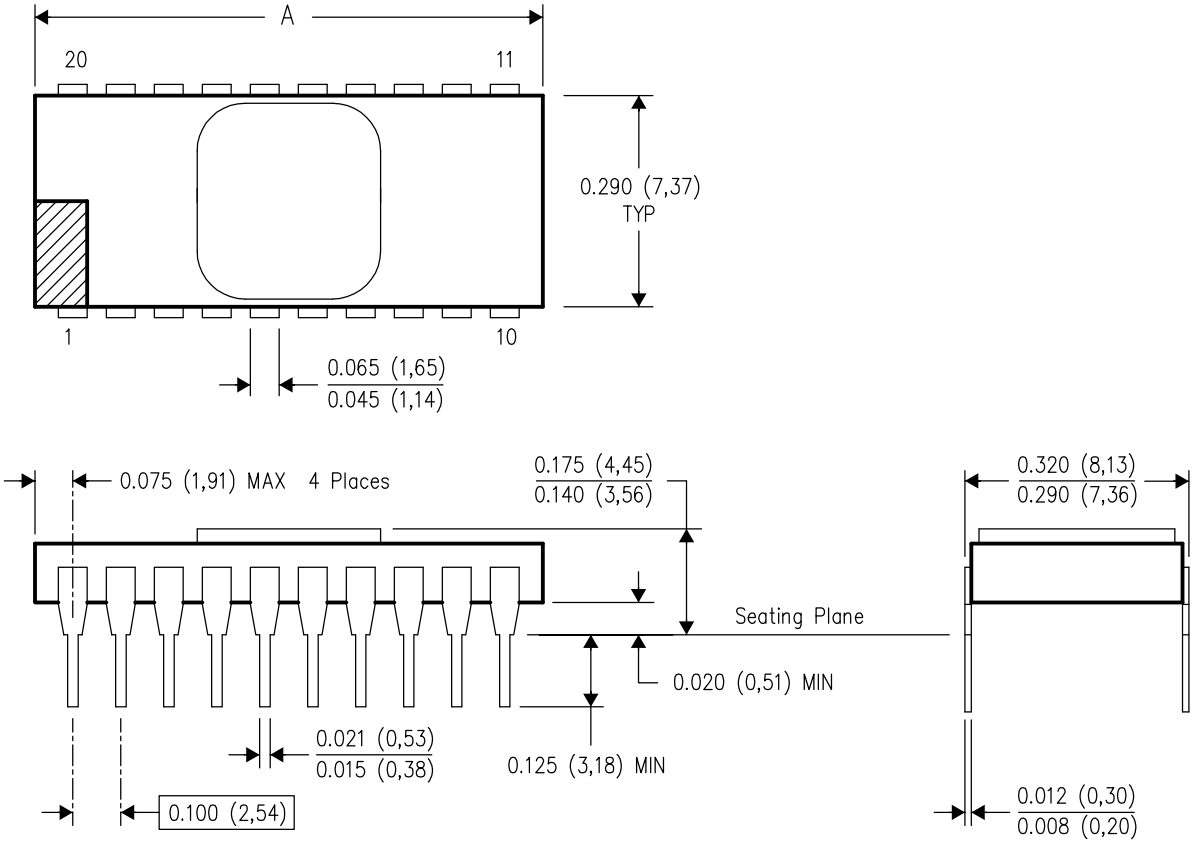
- Catalog : OPA698

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

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