



## *e-trim*<sup>™</sup> 20MHz, High Precision CMOS Operational Amplifier

### FEATURES

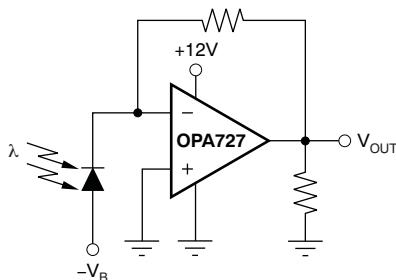
- **OFFSET:** 15 $\mu$ V (typ), 150 $\mu$ V (max)
- **DRIFT:** 0.3 $\mu$ V/ $^{\circ}$ C (typ), 1.5 $\mu$ V/ $^{\circ}$ C (max)
- **BANDWIDTH:** 20MHz
- **SLEW RATE:** 30V/ $\mu$ s
- **BIAS CURRENT:** 500pA (max)
- **LOW NOISE:** 6nV/ $\sqrt{\text{Hz}}$  at 100kHz
- **THD+N:** 0.0003% at 1kHz
- **QUIESCENT CURRENT:** 4.3mA/ch
- **SUPPLY VOLTAGE:** 4V to 12V
- **SHUTDOWN MODE (OPA728):** 6 $\mu$ A

### APPLICATIONS

- OPTICAL NETWORKING
- TRANSIMPEDANCE AMPLIFIERS
- INTEGRATORS
- ACTIVE FILTERS
- A/D CONVERTER DRIVERS
- I/V CONVERTER FOR DACs
- HIGH PERFORMANCE AUDIO
- PROCESS CONTROL
- TEST EQUIPMENT

### OPAx727 AND OPAx728 RELATED PRODUCTS

FEATURES	PRODUCT
20MHz, 3mV, 4 $\mu$ V/ $^{\circ}$ C (non- <i>e-trim</i> version of OPA727)	<a href="#">OPA725</a>
20MHz, 3mV, 4 $\mu$ V/ $^{\circ}$ C, Shutdown (non- <i>e-trim</i> version of OPA728)	<a href="#">OPA726</a>



### DESCRIPTION

The OPA727 and OPA728 series op amps use a state-of-the-art 12V analog CMOS process and *e-trim*, a package-level trim, offering outstanding dc precision and ac performance. The extremely low offset (150 $\mu$ V max) and drift (1.5 $\mu$ V/ $^{\circ}$ C) are achieved by trimming the IC digitally after packaging to avoid the shift in parameters as a result of stresses during package assembly. To correct for offset drift, the OPA727 and OPA728 family is trimmed over temperature. The devices feature very high CMRR and open-loop gain to minimize errors.

Excellent ac characteristics, such as 20MHz GBW, 30V/ $\mu$ s slew rate and 0.0003% THD+N make the OPA727 and OPA728 well-suited for communication, high-end audio, and active filter applications. With a bias current of less than 500pA, they are well suited for use as transimpedance (I/V-conversion) amplifiers for monitoring optical power in ONET applications.

Optimized for single-supply operation up to 12V, the input common-mode range extends to GND for true single-supply functionality. The output swings to within 150mV of the rails, maximizing dynamic range. The low quiescent current of 4.3mA makes it well-suited for use in battery-operated equipment. The OPA728 shutdown version reduces the quiescent current to typically 6 $\mu$ A and features a reference pin for easy shutdown operation with standard CMOS logic in dual-supply applications.

For ease of use, the OPA727 and OPA728 op amp families are fully specified and tested over the supply range of 4V to 12V. The OPA727 (single) and OPA728 (single with shutdown) are available in MSOP-8 and DFN-8; the OPA2727 (dual) is available in DFN-8 and SO-8; and the quad version OPA4727 in TSSOP-14. All versions are specified for operation from  $-40^{\circ}$ C to  $+125^{\circ}$ C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PACKAGE/ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
<b>Non-Shutdown</b>			
OPA727	MSOP-8	DGK	AUE
	DFN-8	DRB	NSF
OPA2727	DFN-8	DRB	NSD
	SO-8	D	O2727A
OPA4727	TSSOP-14	PW	OPA4727
<b>Shutdown</b>			
OPA728	MSOP-8	DGK	AUF
	DFN-8	DRB	NSG

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

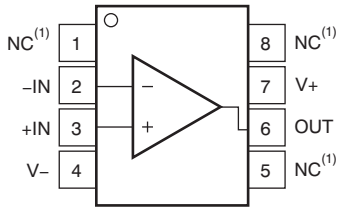
**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

		OPA727, OPA2727 OPA4727, OPA728	UNIT
Supply Voltage		+13.2	V
Signal Input Terminals	Voltage <sup>(2)</sup>	-0.5 to (V+) + 0.5	V
	Current <sup>(2)</sup>	±10	mA
Output Short-Circuit <sup>(3)</sup>		Continuous	
Operating Temperature		-55 to +125	°C
Storage Temperature		-55 to +150	°C
Junction Temperature		+150	°C
ESD Rating	Human Body Model	2000	V
	Charged Device Model	1000	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

**PIN CONFIGURATIONS**

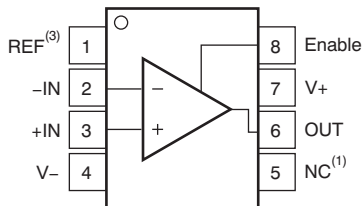
**OPA727  
MSOP-8  
(TOP VIEW)**



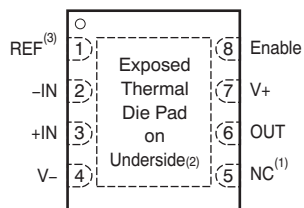
**OPA727  
DFN-8  
(TOP VIEW)**



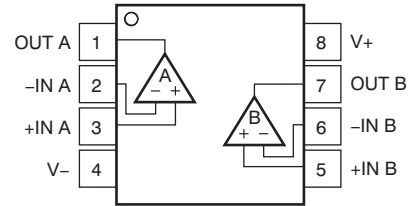
**OPA728  
MSOP-8  
(TOP VIEW)**



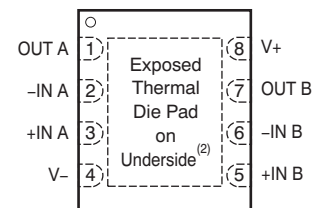
**OPA728  
DFN-8  
(TOP VIEW)**



**OPA2727  
SO-8  
(TOP VIEW)**



**OPA2727  
DFN-8  
(TOP VIEW)**



**OPA4727  
TSSOP-14  
(TOP VIEW)**



**Notes:**

1. NC denotes no internal connection.
2. Connect thermal die pad to V-.
3. REF is the reference voltage for ENABLE pin.

**ELECTRICAL CHARACTERISTICS:  $V_S = +4V$  to  $+12V$  or  $V_S = \pm 2V$  to  $\pm 6V$**

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA727, OPA728, OPA2727, OPA4727			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage	$V_{OS}$ $V_S = \pm 5V, V_{CM} = 0V$				
OPA727 DFN, OPA728 DFN Packages			15	150	$\mu\text{V}$
OPA727 MSOP, OPA728 MSOP Packages			15	300	$\mu\text{V}$
OPA2727			15	150	$\mu\text{V}$
OPA4727			15	175	$\mu\text{V}$
Drift	$dV_{OS}/dT$ $0^\circ\text{C}$ to $+85^\circ\text{C}$		0.3	1.5	$\mu\text{V}/^\circ\text{C}$
	$-40^\circ\text{C}$ to $+125^\circ\text{C}$		<b>0.6</b>	<b>3</b>	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	PSRR $V_S = \pm 2V$ to $\pm 6V, V_{CM} = V-$		30	150	$\mu\text{V}/\text{V}$
<b>Over Temperature</b>	$V_S = \pm 2V$ to $\pm 6V, V_{CM} = V-$			<b>150</b>	$\mu\text{V}/\text{V}$
Channel Separation, dc			1		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>					
Input Bias Current			$\pm 85$	$\pm 500$	pA
<b>Over Temperature</b>			See Typical Characteristics		
Input Offset Current	$I_{OS}$		$\pm 10$	$\pm 100$	pA
<b>NOISE</b>					
Input Voltage Noise, $f = 0.1\text{Hz}$ to $10\text{Hz}$	$e_n$ $V_S = \pm 6V, V_{CM} = 0V$		10		$\mu\text{V}_{PP}$
Input Voltage Noise Density, $f = 10\text{kHz}$	$e_n$ $V_S = \pm 6V, V_{CM} = 0V$		10		$\text{nV}/\sqrt{\text{Hz}}$
Input Voltage Noise Density, $f = 100\text{kHz}$	$e_n$ $V_S = \pm 6V, V_{CM} = 0V$		6		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density, $f = 1\text{kHz}$	$i_n$ $V_S = \pm 6V, V_{CM} = 0V$		2.5		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range	$V_{CM}$	(V-)		(V+)-2.5	V
Common-Mode Rejection Ratio	CMRR	$(V-) \leq V_{CM} \leq (V+) - 2.5V$	86	94	dB
<b>Over Temperature</b>		$(V-) \leq V_{CM} \leq (V+) - 2.5V$	<b>84</b>		<b>dB</b>
		$(V-) \leq V_{CM} \leq (V+) - 3V$	94	100	dB
<b>Over Temperature</b>		$(V-) \leq V_{CM} \leq (V+) - 3V$	<b>84</b>		<b>dB</b>
<b>INPUT IMPEDANCE</b>					
Differential			$10^{11} \parallel 5$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{11} \parallel 4$		$\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>					
Open-Loop Voltage Gain	$A_{OL}$	$R_L = 100\text{k}\Omega, 0.15V < V_O < (V+) - 0.15V$	110	120	dB
<b>Over Temperature</b>		$R_L = 100\text{k}\Omega, 0.15V < V_O < (V+) - 0.15V$	<b>100</b>		<b>dB</b>
		$R_L = 1\text{k}\Omega, 0.25V < V_O < (V+) - 0.25V$	106	116	dB
<b>Over Temperature, OPA727, OPA728</b>		$R_L = 1\text{k}\Omega, 0.25V < V_O < (V+) - 0.25V$	<b>96</b>		<b>dB</b>
<b>Over Temperature, OPA2727, OPA4727</b>		$R_L = 1\text{k}\Omega, 0.35V < V_O < (V+) - 0.35V$	<b>96</b>		<b>dB</b>
<b>FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	GBW	$C_L = 20\text{ pF}$		20	MHz
Slew Rate	SR	$G = +1$		30	V/ $\mu\text{s}$
Settling Time, 0.1%	$t_s$	$V_S = \pm 6V, 5V$ Step, $G = +1$		350	ns
0.01%		$V_S = \pm 6V, 5V$ Step, $G = +1$		450	ns
Overload Recovery Time		$V_{IN} \times \text{Gain} > V_S$		50	ns
Total Harmonic Distortion + Noise	THD+N	$V_S = \pm 6V, V_{OUT} = 2V_{RMS}, R_L = 600\Omega, G = +1, f = 1\text{kHz}$		0.003	%

**ELECTRICAL CHARACTERISTICS:  $V_S = +4V$  to  $+12V$  or  $V_S = \pm 2V$  to  $\pm 6V$  (continued)**

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA727, OPA728, OPA2727, OPA4727			UNIT
		MIN	TYP	MAX	
<b>OUTPUT</b>					
Voltage Output Swing from Rail					
	$R_L = 100\text{k}\Omega$ , $A_{OL} > 110\text{dB}$		100	150	mV
<b>Over Temperature</b>	<b><math>R_L = 100\text{k}\Omega</math>, <math>A_{OL} &gt; 100\text{dB}</math></b>			<b>150</b>	<b>mV</b>
	$R_L = 1\text{k}\Omega$ , $A_{OL} > 106\text{dB}$		200	250	mV
<b>Over Temperature, OPA727, OPA728</b>	<b><math>R_L = 1\text{k}\Omega</math>, <math>A_{OL} &gt; 96\text{dB}</math></b>			<b>250</b>	<b>mV</b>
<b>Over Temperature, OPA2727, OPA4727</b>	<b><math>R_L = 1\text{k}\Omega</math>, <math>A_{OL} &gt; 96\text{dB}</math></b>			<b>350</b>	<b>mV</b>
Output Current	$I_{OUT}$ $ V_S - V_{OUT}  < 1V$		40		mA
Short-Circuit Current	$I_{SC}$		$\pm 55$		mA
Capacitive Load Drive	$C_{LOAD}$	See <a href="#">Typical Characteristics</a>			
Open-Loop Output Impedance	$f = 1\text{MHz}$ , $I_O = 0$		40		$\Omega$
<b>ENABLE/SHUTDOWN (OPA728)</b>					
$t_{OFF}$			5		$\mu\text{s}$
$t_{ON}$			80		$\mu\text{s}$
Enable Reference (Ref Pin) Voltage Range		$V_-$		$(V_+) - 2$	V
$V_L$ (amplifier is disabled)				$< V_{DGND} + 0.8V$	V
$V_H$ (amplifier is enabled)		$> V_{DGND} + 2V$			V
Input Bias Current of Enable Pin			5		pA
$I_{QSD}$	Amplifier Disabled		6	15	$\mu\text{A}$
<b>POWER SUPPLY</b>					
Specified Voltage Range	$V_S$	4		12	V
Operating Voltage Range	$V_S$		3.5 to 13.2		V
Quiescent Current (per amplifier)	$I_Q$		4.3	6.5	mA
<b>Over Temperature</b>				<b>6.5</b>	<b>mA</b>
<b>TEMPERATURE RANGE</b>					
Specified Range		-40		+125	$^\circ\text{C}$
Operating Range		-55		+125	$^\circ\text{C}$
Storage Range		-55		+150	$^\circ\text{C}$
Thermal Resistance	$\theta_{JA}$				
MSOP-8, SO-8			150		$^\circ\text{C/W}$
TSSOP-14			100		$^\circ\text{C/W}$
DFN-8			46		$^\circ\text{C/W}$

**TYPICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



Figure 1.



Figure 2.

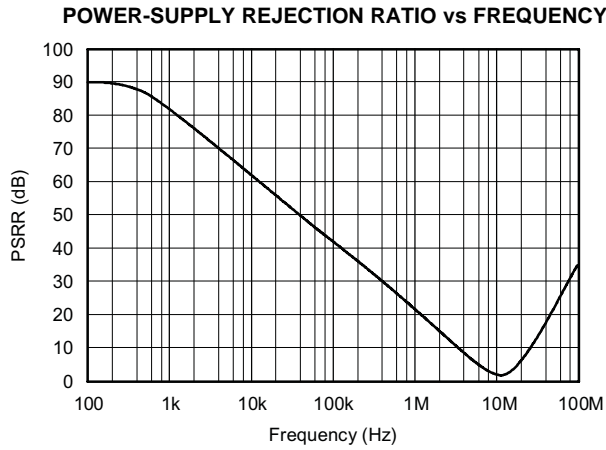


Figure 3.

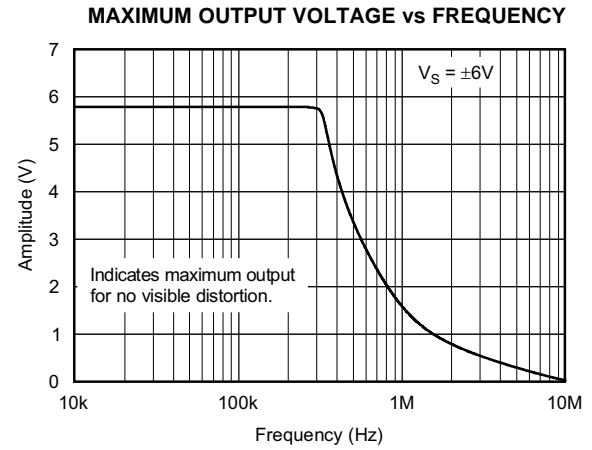


Figure 4.

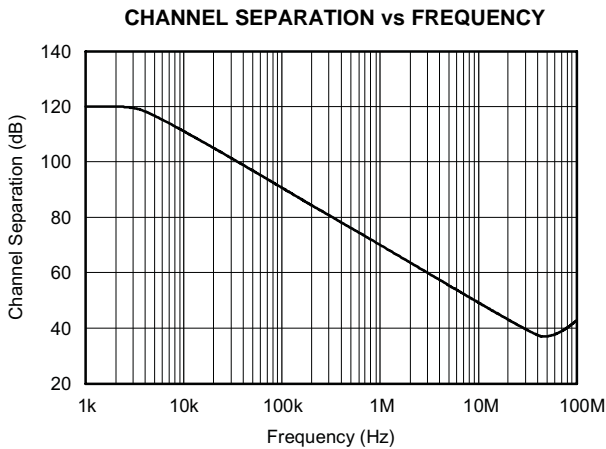


Figure 5.

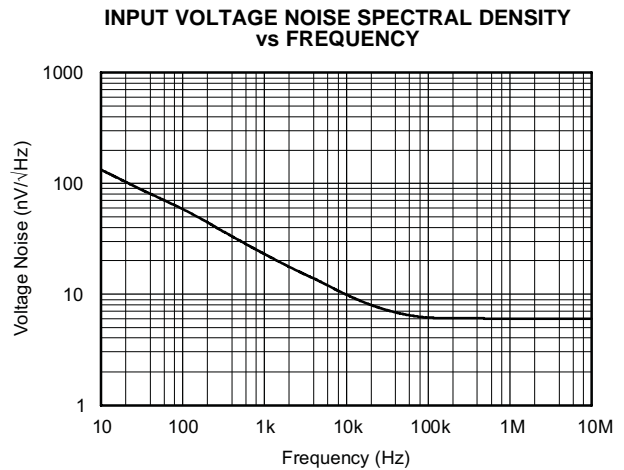


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



Figure 7.



Figure 8.



Figure 9.



Figure 10.

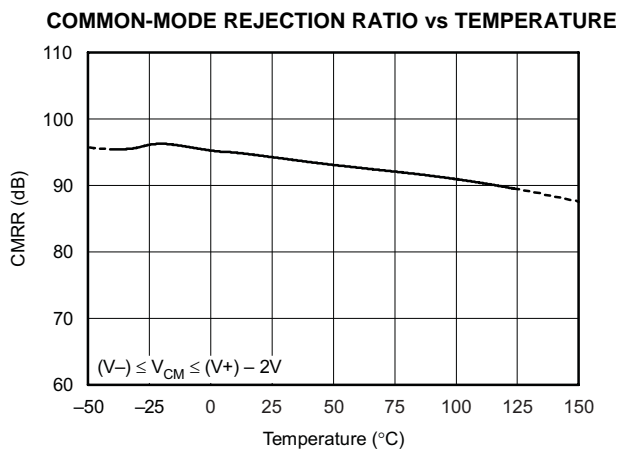


Figure 11.

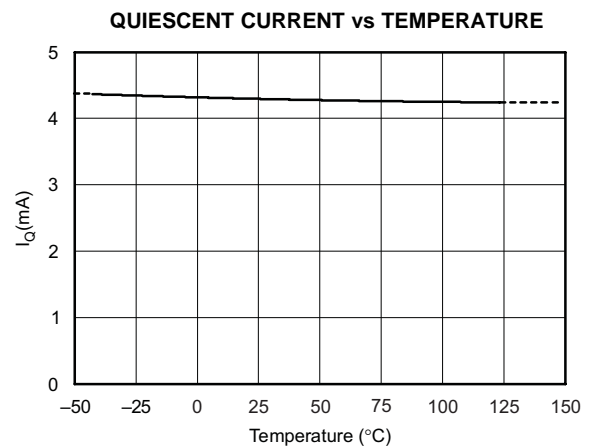


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

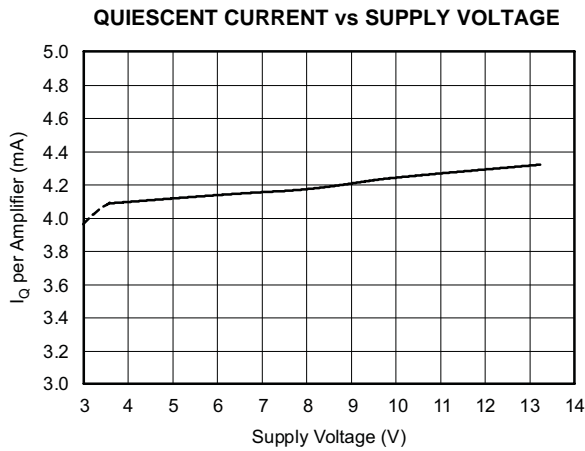


Figure 13.



Figure 14.

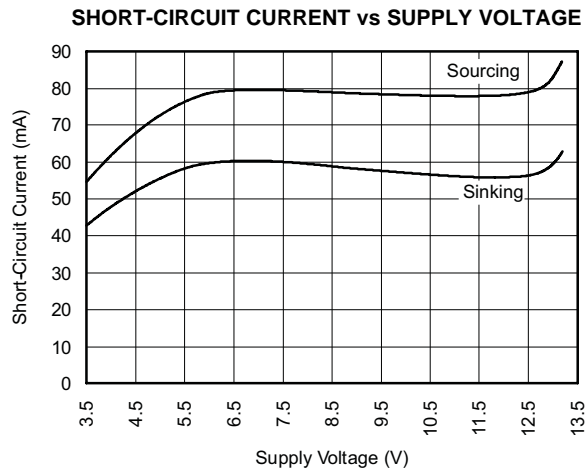


Figure 15.

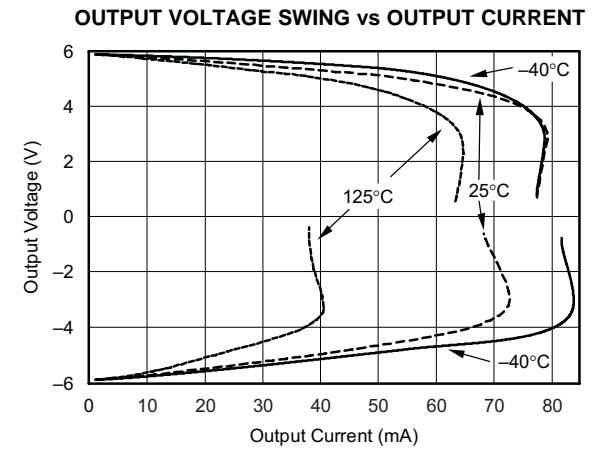


Figure 16.

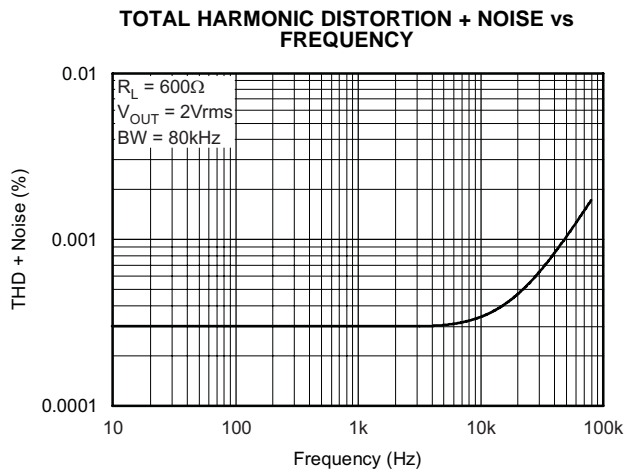


Figure 17.

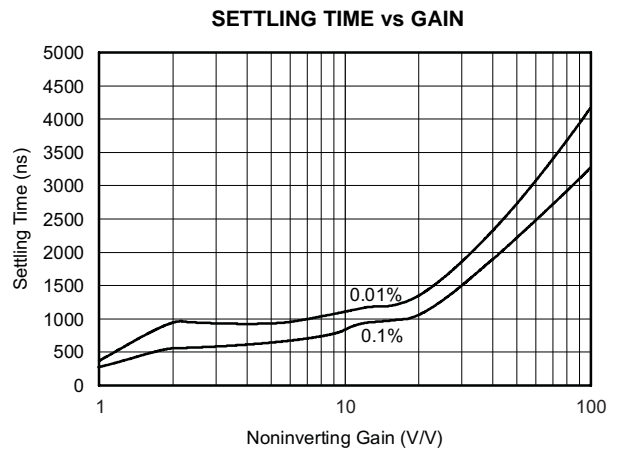


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



Figure 19.

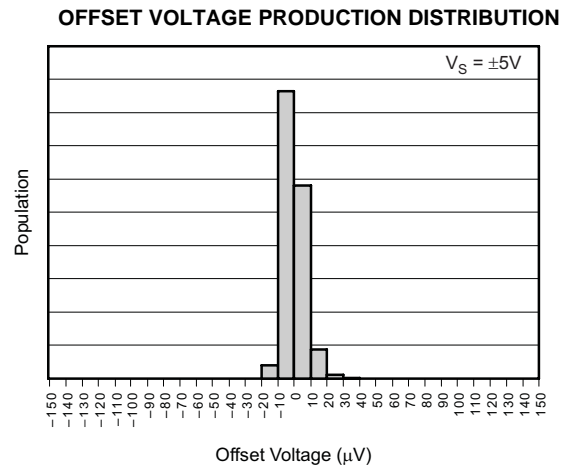


Figure 20.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION (0°C TO +85°C)

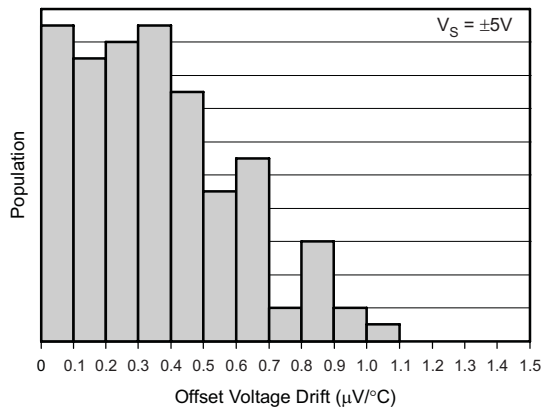


Figure 21.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION (-40°C TO +125°C)

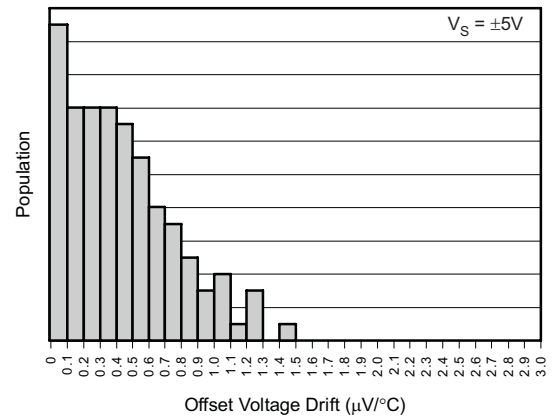


Figure 22.

OFFSET VOLTAGE vs TEMPERATURE

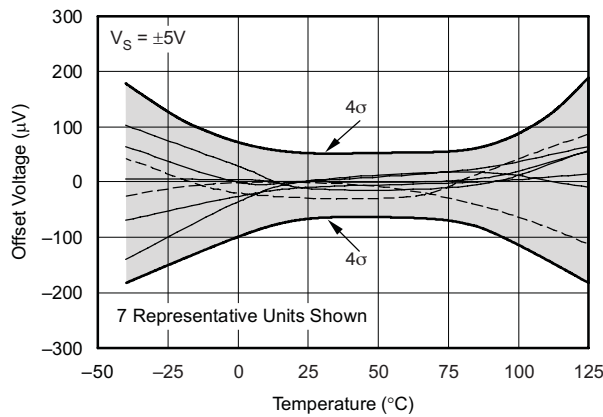


Figure 23.

SMALL-SIGNAL STEP RESPONSE

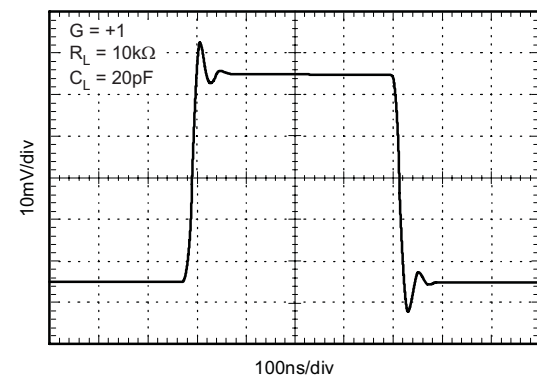
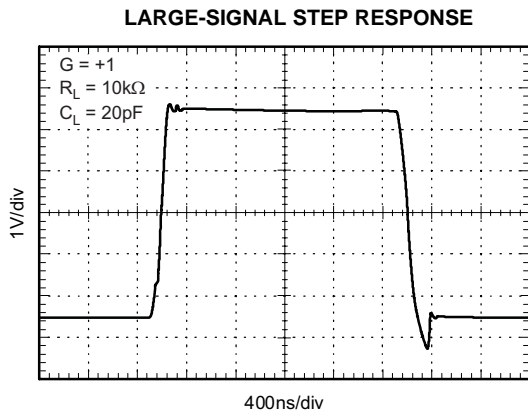


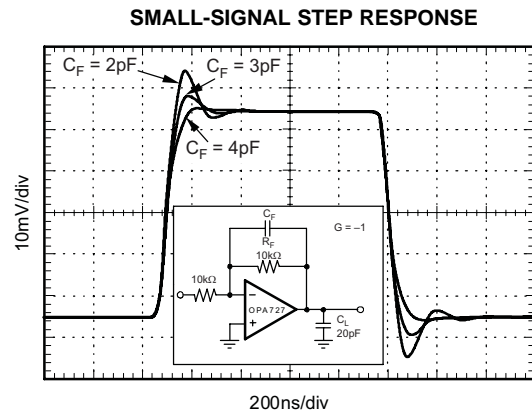
Figure 24.

**TYPICAL CHARACTERISTICS (continued)**

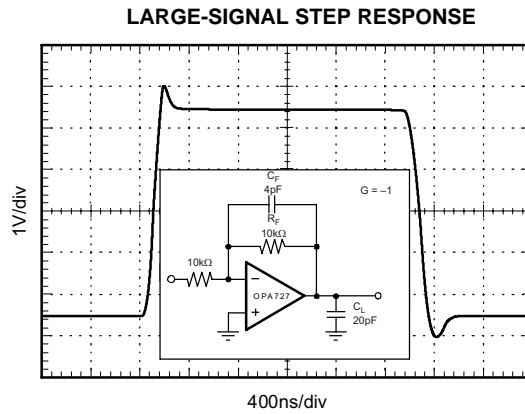
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



**Figure 25.**



**Figure 26.**



**Figure 27.**

## APPLICATIONS INFORMATION

The OPA727 and OPA728 family of op amps use *e-trim*, an adjustment to offset voltage and temperature drift made during the final steps of manufacturing after the plastic molding is completed. This compensates for performance shifts that can occur during the molding process. Through *e-trim*, the OPA727 and OPA728 deliver excellent offset voltage (150 $\mu$ V max) and extremely low offset voltage drift (1.5 $\mu$ V/ $^{\circ}$ C). Additionally, these 20MHz CMOS op amps have a fast slew rate, low noise, and excellent PSRR, CMRR, and  $A_{OL}$ . They can operate on typically 4.3mA quiescent current from a single (or split) supply in the range of 4V to 12V ( $\pm$ 2V to  $\pm$ 6V), making them highly versatile and easy to use. They are stable in a unity-gain configuration.

Power-supply pins should be bypassed with 1nF ceramic capacitors in parallel with 1 $\mu$ F tantalum capacitors.

### OPERATING VOLTAGE

OPA727 series op amps are specified from 4V to 12V supplies over a temperature range of  $-40^{\circ}$ C to  $+125^{\circ}$ C. They will operate well in  $\pm$ 5V or +5V to +12V power-supply systems. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

### ENABLE/SHUTDOWN

OPA727 series op amps require approximately 4.3mA quiescent current. The enable/shutdown feature of the OPA728 allows the op amp to be shut off to reduce this current to approximately 6 $\mu$ A.

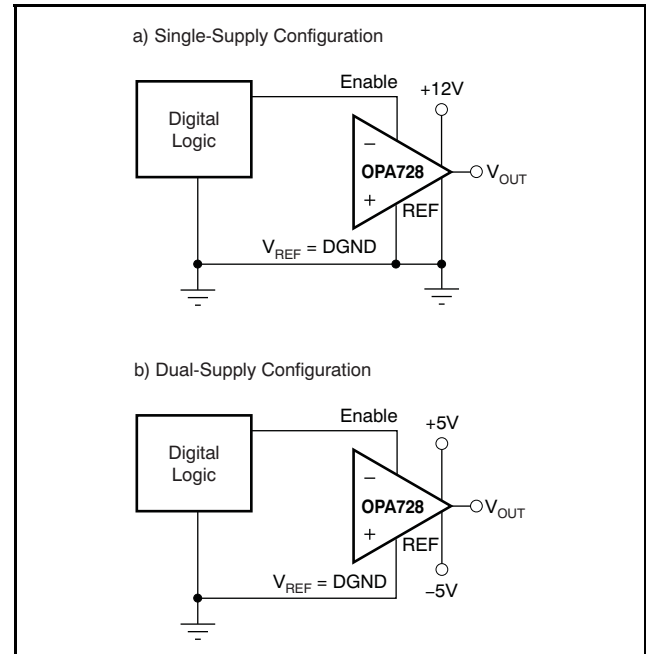
The enable/shutdown input is referenced to the Enable Reference Pin, REF (see [Pin Configurations](#)). This pin can be connected to logic ground in dual-supply op amp configurations to avoid level-shifting the enable logic signal, as shown in [Figure 28](#).

The Enable Reference Pin voltage,  $V_{REF}$ , must not exceed  $(V+) - 2V$ . It may be set as low as  $V-$ . The amplifier is enabled when the Enable Pin voltage is greater than  $V_{REF} + 2V$ . The amplifier is disabled (shutdown) if the Enable Pin voltage is less than  $V_{REF} + 0.8V$ . The Enable Pin is connected to internal pull-up circuitry and will enable the device if left unconnected.

### COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA727 and OPA728 series extends from  $V-$  to  $(V+) - 2.5V$ .

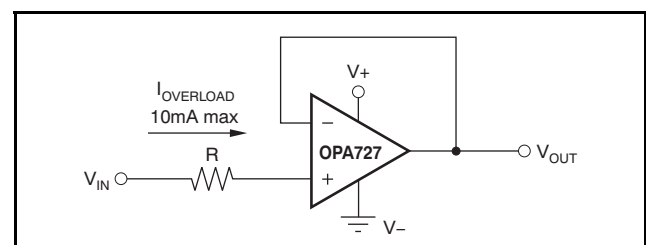
Common-mode rejection is excellent throughout the input voltage range from  $V-$  to  $(V+) - 3V$ . CMRR decreases somewhat as the common-mode voltage extends to  $(V+) - 2.5V$ , but remains very good and is tested throughout this range. See the [Electrical Characteristics](#) table for details.



**Figure 28. Enable Reference Pin Connection for Single- and Dual-Supply Configurations**

### INPUT OVER-VOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current is limited to 10mA. This is easily accomplished with an input resistor in series with the op amp, as shown in [Figure 29](#). The OPA727 series features no phase inversion when the inputs extend beyond supplies, if the input is current limited.



**Figure 29. Input Current Protection for Voltages Exceeding the Supply Voltage**

## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving heavy loads connected to any point between V+ and V-. For light resistive loads (>100k $\Omega$ ), the output voltage can swing to 150mV from the supply rail, while still maintaining excellent linearity ( $A_{OL} > 110\text{dB}$ ). With 1k $\Omega$  resistive loads, the output is specified to swing to within 250mV from the supply rails with excellent linearity (see the Typical Characteristics curve, [Output Voltage Swing vs Output Current](#)).

## CAPACITIVE LOAD AND STABILITY

Capacitive load drive is dependent upon gain and the overshoot requirements of the application. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see the Typical Characteristics curve, [Small-Signal Overshoot vs Capacitive Load](#)).

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10 $\Omega$  to 20 $\Omega$  resistor inside the feedback loop, as shown in [Figure 30](#). This reduces ringing with large capacitive loads while maintaining DC accuracy.

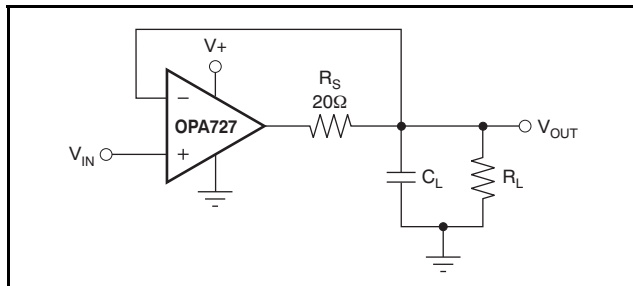


Figure 30. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

## DRIVING FAST 16-BIT ADCs

The OPA727 series is optimized for driving fast 16-bit ADCs such as the [ADS8342](#). The OPA727 op amps buffer the converter input capacitance and resulting charge injection, while providing signal gain. [Figure 31](#) shows the OPA727 in a single-ended method of interfacing to the ADS8342 16-bit, 250kSPS, 4-channel ADC with an input range of  $\pm 2.5\text{V}$ . The OPA727 has demonstrated excellent settling time to the 16-bit level within the 600ns acquisition time of the ADS8342. The RC filter, shown in [Figure 31](#), has been carefully tuned for best noise and settling performance. It may need to be adjusted for different op amp configurations. Refer to the [ADS8342 data sheet](#) (available for download at [www.ti.com](http://www.ti.com)) for additional information on this product.

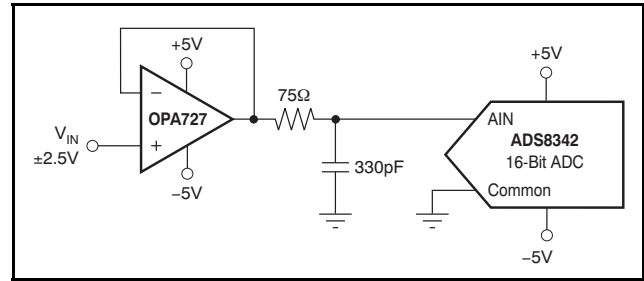


Figure 31. OPA727 Driving an ADC

## TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA727 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in [Figure 32](#), are the expected diode capacitance ( $C_D$ ), which should include the parasitic input common-mode and differential-mode input capacitance (4pF + 5pF for the OPA727); the desired transimpedance gain ( $R_F$ ); and the GBW for the OPA727 (20MHz). With these three variables set, the feedback capacitor value ( $C_F$ ) can be set to control the frequency response.  $C_F$  includes the stray capacitance of  $R_F$ , which is 0.2pF for a typical surface-mount resistor.

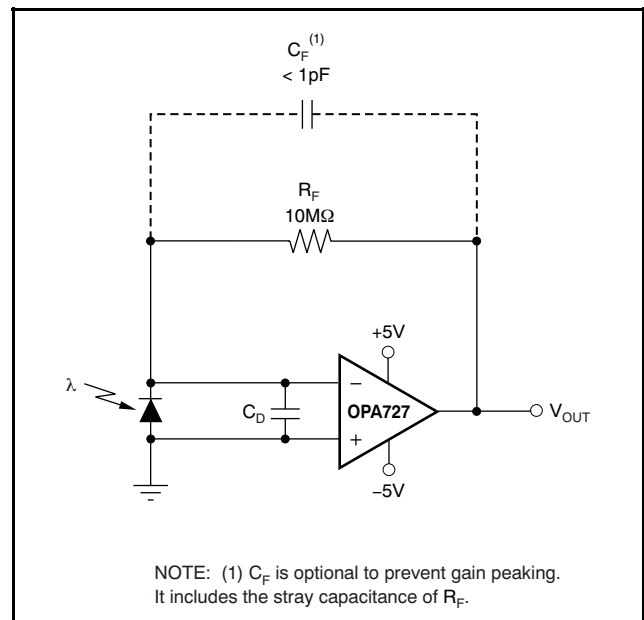


Figure 32. Dual-Supply Transimpedance Amplifier

To achieve a maximally-flat, 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \quad (1)$$

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS [OPA380](#) (90MHz GBW), [OPA354](#) (100MHz GBW), [OPA300](#) (180MHz GBW), [OPA355](#) (200MHz GBW), or [OPA656](#), [OPA657](#) (400MHz GBW) may be used.

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this is shown in [Figure 33](#). This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



**Figure 33. Single-Supply Transimpedance Amplifier**

For additional information, refer to Application Bulletin ([SBOA055](#)), *Compensate Transimpedance Amplifiers Intuitively*, available for download at [www.ti.com](#).

## OPTIMIZING THE TRANSIMPEDANCE CIRCUIT

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select  $R_F$  to create the total required gain. Using a lower value for  $R_F$  and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by  $R_F$  increases with the square-root of  $R_F$ , whereas the signal increases linearly. Therefore, signal-to-noise ratio is improved when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the  $R_F$  to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the Application Bulletins *Noise Analysis of FET Transimpedance Amplifiers* ([SBOA060](#)), and *Noise Analysis for High-Speed Op Amps* ([SBOA066](#)), available for download at the TI web site.



Note: FilterPro is a low-pass filter design program available for download at no cost from TI's web site ([www.ti.com](http://www.ti.com)). The program can be used to determine component values for other cutoff frequencies or filter types.

**Figure 34. Four-Pole Butterworth Sallen-Key Low-Pass Filter**

## DFN PACKAGE

The OPA727 series uses the DFN-8 (also known as SON), which is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note, *QFN/SON PCB Attachment (SLUA271)* and Application Report, *Quad Flatpack No-Lead Logic Packages (SCBA017)*, both available for download at [www.ti.com](http://www.ti.com).

**The exposed leadframe die pad on the bottom of the package should be connected to V–.**

## LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2727AID</a>	Last Time Buy	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	O2727A 2727A
OPA2727AID.B	Last Time Buy	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	O2727A 2727A
<a href="#">OPA2727AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	O2727A 2727A
OPA2727AIDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	O2727A 2727A
<a href="#">OPA2727AIDRBR</a>	Active	Production	SON (DRB)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	NSD
OPA2727AIDRBR.B	Active	Production	SON (DRB)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	NSD
OPA2727AIDRBRG4	Active	Production	SON (DRB)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	NSD
OPA2727AIDRBRG4.B	Active	Production	SON (DRB)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	NSD
<a href="#">OPA2727AIDRBT</a>	Last Time Buy	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	NSD
OPA2727AIDRBT.B	Last Time Buy	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	NSD
OPA2727AIDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	O2727A 2727A
OPA2727AIDRG4.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	O2727A 2727A
<a href="#">OPA4727AIPW</a>	Last Time Buy	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4727
OPA4727AIPW.B	Last Time Buy	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4727
<a href="#">OPA4727AIPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4727
OPA4727AIPWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4727
OPA4727AIPWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4727
OPA4727AIPWRG4.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4727
<a href="#">OPA727AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI   Nipdau	Level-2-260C-1 YEAR	-40 to 85	AUE
OPA727AIDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	AUE
OPA727AIDGKRG4	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 85	AUE
OPA727AIDGKRG4.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 85	AUE

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA727AIDGKT</a>	Last Time Buy	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	Call TI   Nipdau	Level-2-260C-1 YEAR	-40 to 85	AUE
OPA727AIDGKT.B	Last Time Buy	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AUE
<a href="#">OPA727AIDRBT</a>	Active	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSF
OPA727AIDRBT.B	Active	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSF
<a href="#">OPA728AIDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	Call TI   Nipdauag   Nipdau	Level-2-260C-1 YEAR	-40 to 125	AUF
OPA728AIDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AUF
<a href="#">OPA728AIDRBT</a>	Active	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NSG
OPA728AIDRBT.B	Active	Production	SON (DRB)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NSG

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2727AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2727AIDRBR	SON	DRB	8	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2727AIDRBRG4	SON	DRB	8	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2727AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2727AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4727AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4727AIPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA727AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA727AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA727AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA728AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA728AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

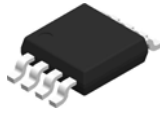
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2727AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2727AIDRBR	SON	DRB	8	2500	353.0	353.0	32.0
OPA2727AIDRBRG4	SON	DRB	8	2500	353.0	353.0	32.0
OPA2727AIDRBT	SON	DRB	8	250	213.0	191.0	35.0
OPA2727AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA4727AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
OPA4727AIPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
OPA727AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA727AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA727AIDRBT	SON	DRB	8	250	213.0	191.0	35.0
OPA728AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA728AIDRBT	SON	DRB	8	250	213.0	191.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2727AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2727AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4727AIPW	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4727AIPW.B	PW	TSSOP	14	90	508	8.5	3250	2.8

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

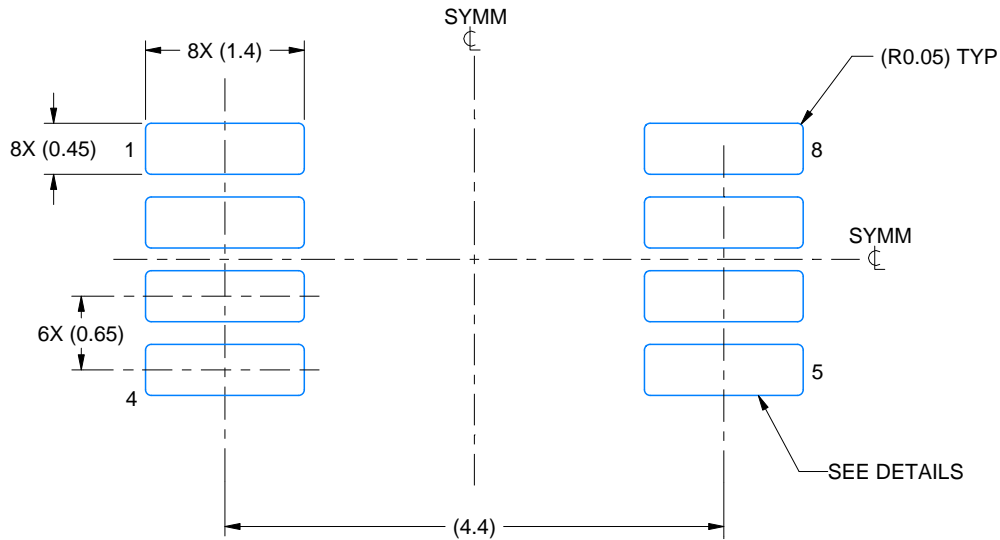
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

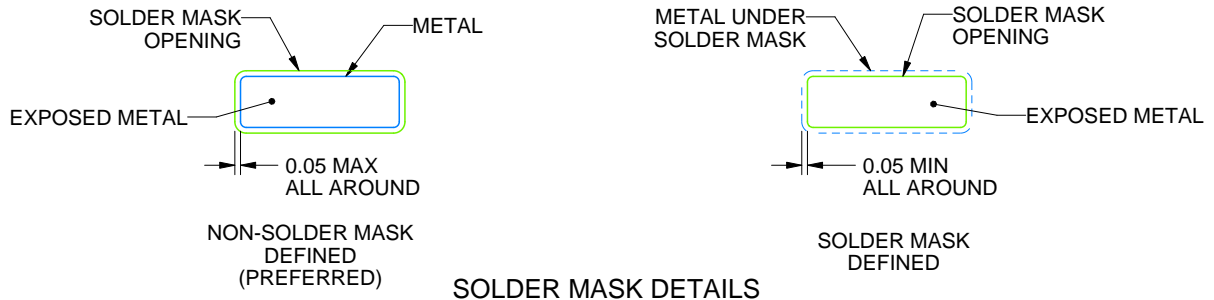
DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

**DRB 8**

**GENERIC PACKAGE VIEW**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203482/L

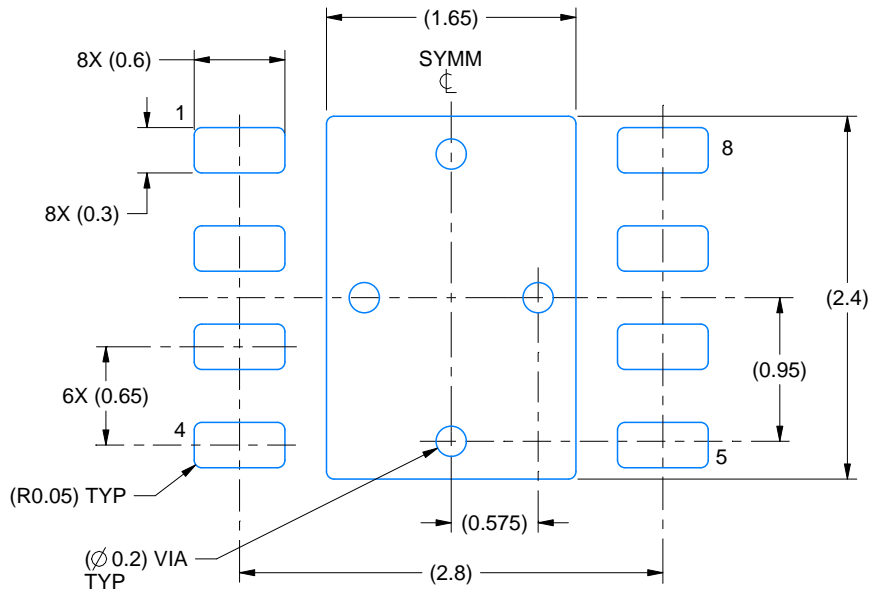


# EXAMPLE BOARD LAYOUT

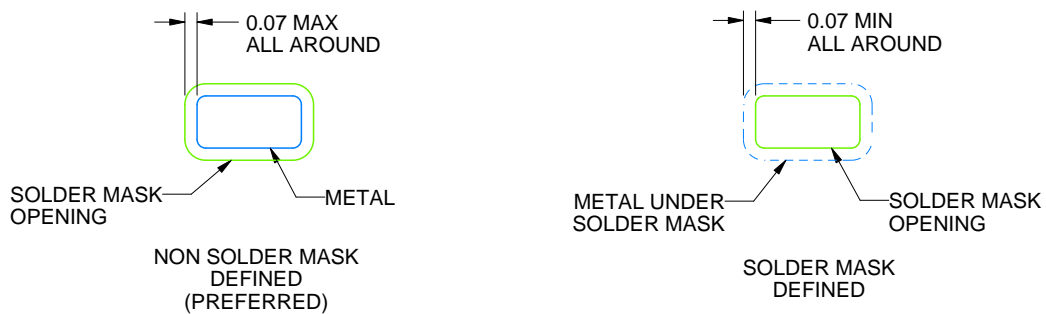
DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

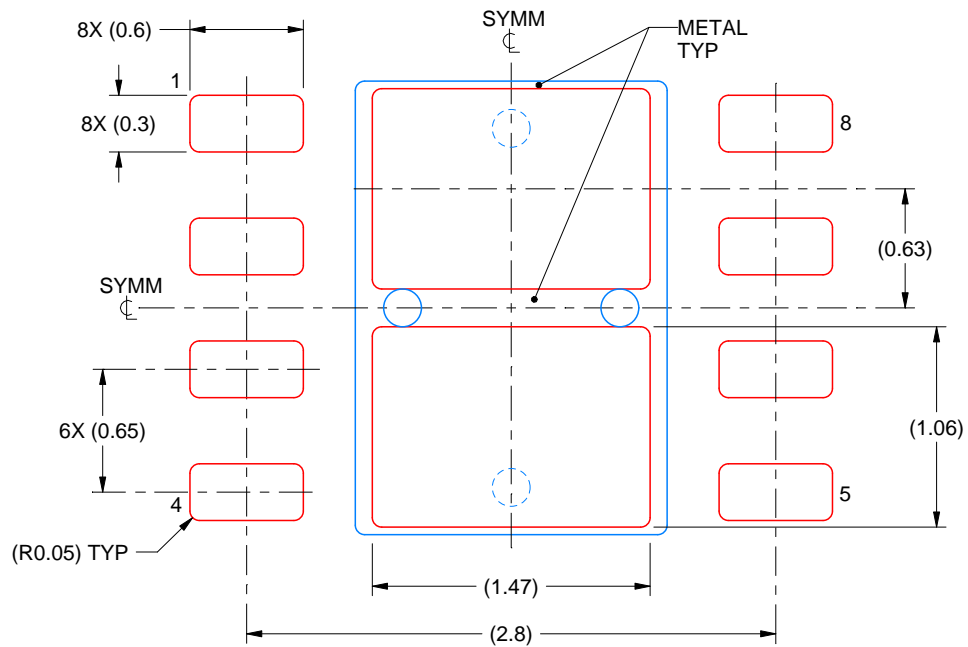
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
81% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

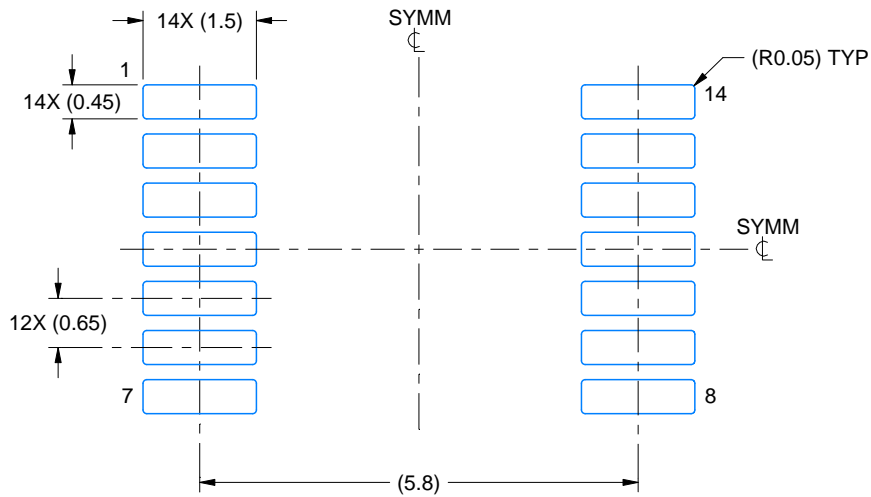
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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