

0.05 $\mu\text{V}/^\circ\text{C}$ max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series

FEATURES

- LOW OFFSET VOLTAGE: 5 μV (max)
- ZERO DRIFT: 0.05 $\mu\text{V}/^\circ\text{C}$ max
- QUIESCENT CURRENT: 750 μA (max)
- SINGLE-SUPPLY OPERATION
- LOW BIAS CURRENT: 200pA (max)
- SHUTDOWN
- *Micro*SIZE PACKAGES
- WIDE SUPPLY RANGE: 2.7V to 12V

APPLICATIONS

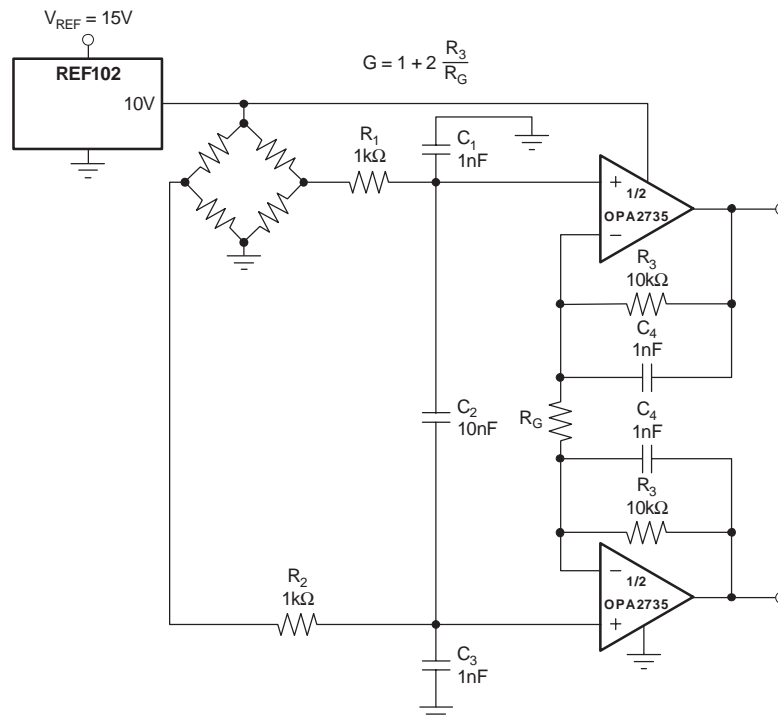
- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENTS
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

DESCRIPTION

The OPA734 and OPA735 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide low offset voltage (5 μV max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 50mV of the rails. Either single or bipolar supplies can be used in the range of +2.7V to +12V ($\pm 1.35\text{V}$ to $\pm 6\text{V}$). They are optimized for low-voltage, single-supply operation.

The OPA734 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current that is 9 μA (max) and the output placed in a high-impedance state.

The single version is available in the *Micro*SIZE SOT23-5 (SOT23-6 for shutdown version) and the SO-8 packages. The dual version is available in the MSOP-8 and SO-8 packages (MSOP-10 only for the shutdown version). All versions are specified for operation from -40°C to $+85^\circ\text{C}$.



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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+13.2V
Signal Input Terminals, Voltage ⁽²⁾	(V-) – 0.5V to (V+) + 0.5V
Current ⁽²⁾	±10mA
Output Short Circuit ⁽³⁾	Continuous
Operating Temperature	–40°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model), OPA734	1000V
ESD Rating (Human Body Model), OPA735, OPA2734, OPA2735	2000V



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown Version						
OPA734	SOT23-6	DBV	–40°C to +85°C	NSB	OPA734AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA734AIDBVR	Tape and Reel, 3000
OPA734	SO-8	D	–40°C to +85°C	OPA734A	OPA734AID	Rails, 100
"	"	"	"	"	OPA734AIDR	Tape and Reel, 2500
OPA2734	MSOP-10	DGS	–40°C to +85°C	BGO	OPA2734AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2734AIDGSR	Tape and Reel, 2500
Non-Shutdown Version						
OPA735	SOT23-5	DBV	–40°C to +85°C	NSC	OPA735AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA735AIDBVR	Tape and Reel, 3000
OPA735	SO-8	D	–40°C to +85°C	OPA735A	OPA735AID	Rails, 100
"	"	"	"	"	OPA735AIDR	Tape and Reel, 2500
OPA2735	SO-8	D	–40°C to +85°C	OPA2735A	OPA2735AID	Rails, 100
"	"	"	"	"	OPA2735AIDR	Tape and Reel, 2500
OPA2735	MSOP-8	DGK	–40°C to +85°C	BGN	OPA2735AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2735AIDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ ($V_S = +10V$)

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

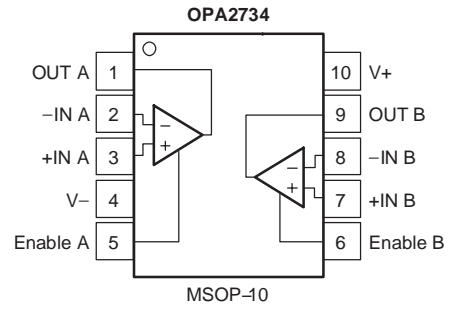
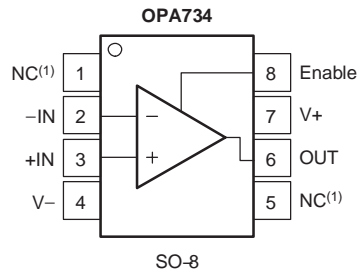
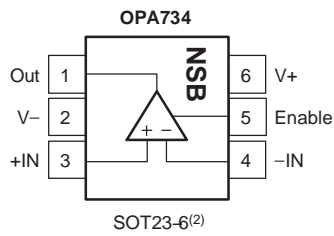
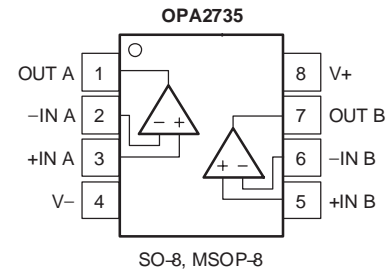
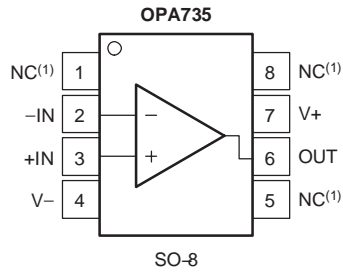
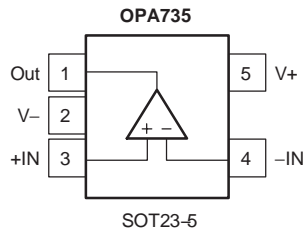
At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA734, OPA2734, OPA735, OPA2735			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply Long-Term Stability Channel Separation, dc	V_{OS} dV_{OS}/dT PSRR $V_S = 2.7V$ to $12V$, $V_{CM} = 0V$		1 0.01 0.2 Note (1) 0.1	5 0.05 1.8	μV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
INPUT BIAS CURRENT Input Bias Current over Temperature Input Offset Current	I_B $V_{CM} = V_S/2$ I_{OS} $V_{CM} = V_S/2$		See Typical Characteristics		pA pA pA
NOISE Input Voltage Noise, $f = 0.01\text{Hz}$ to 1Hz Input Voltage Noise, $f = 0.1\text{Hz}$ to 10Hz Input Voltage Noise Density, $f = 1\text{kHz}$ Input Current Noise Density, $f = 1\text{kHz}$	e_n e_n e_n i_n		0.8 2.5 135 40		μV_{PP} μV_{PP} $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio	V_{CM} CMRR $(V^-) - 0.1V < V_{CM} < (V^+) - 1.5V$	$(V^-) - 0.1$ 115	130	$(V^+) - 1.5$	V dB
INPUT CAPACITANCE Differential Common-Mode			2 10		pF pF
OPEN-LOOP GAIN Open-Loop Voltage Gain	A_{OL} $(V^-) + 100\text{mV} < V_O < (V^+) - 100\text{mV}$	115	130		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate	GBW SR $G = +1$		1.6 1.5		MHz V/ μs
OUTPUT Voltage Output Swing from Rail Short-Circuit Current Open-Loop Output Impedance Capacitive Load Drive	I_{SC} $R_L = 10\text{k}\Omega$ $f = 1\text{MHz}$, $I_O = 0$ C_{LOAD}		20 ± 20 125	50	mV mA Ω
ENABLE/SHUTDOWN t_{OFF} $t_{ON}^{(2)}$ V_L (amplifier is shutdown) V_H (amplifier is active) I_{QSD} (per amplifier) Input Bias Current of Enable Pin		V^- $(V^-) + 2$	1.5 150 4 3	$(V^-) + 0.8$ V^+ 9	μs μs V V μA μA
POWER SUPPLY Operating Voltage Range Quiescent Current (per amplifier)	V_S I_Q $I_Q = 0$		2.7 to 12 (± 1.35 to ± 6) 0.6		V mA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT23-5, SOT23-6 MSOP-8, MSOP-10, SO-8	θ_{JA}	-40 -40 -65		+85 +150 +150	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

(1) 300-hour life test at 150°C demonstrated randomly distributed variation in the range of measurement limits—approximately $1\mu\text{V}$.

(2) Device requires one complete auto-zero cycle to return to V_{OS} accuracy.

PIN CONFIGURATIONS



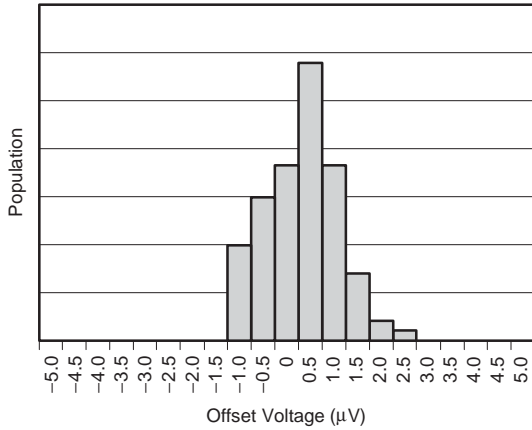
(1) NC = No Connection

(2) Pin 1 of the SOT23-6 is determined by orienting the package marking as shown in the diagram.

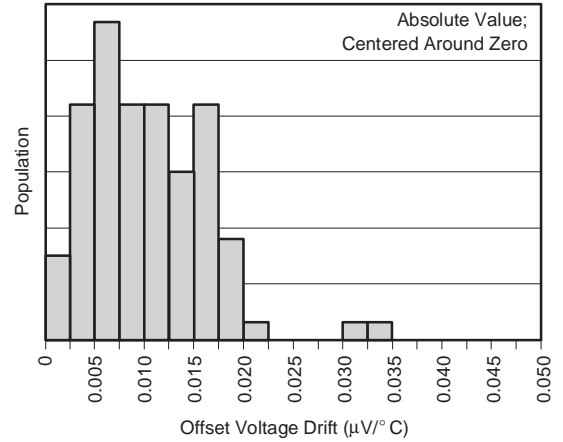
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as $+10\text{V}$).

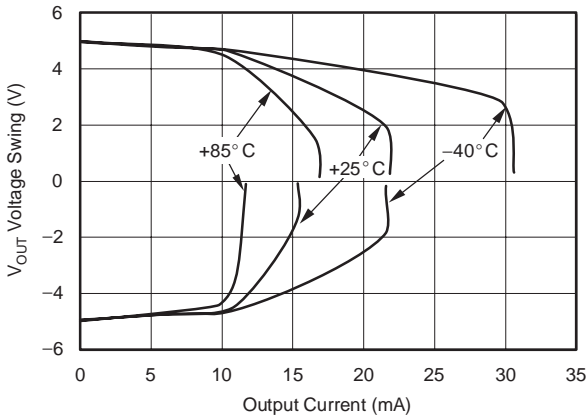
OUTPUT VOLTAGE PRODUCTION DISTRIBUTION



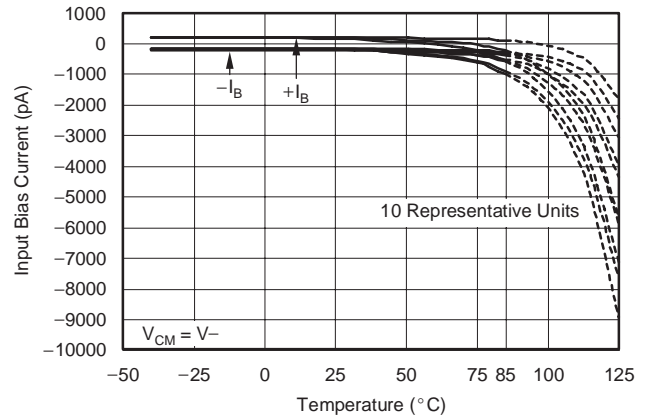
OUTPUT VOLTAGE DRIFT PRODUCTION DISTRIBUTION



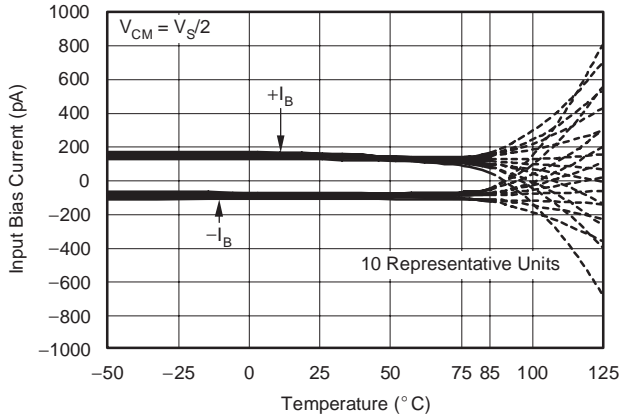
OUTPUT VOLTAGE SWING TO RAIL
vs OUTPUT CURRENT



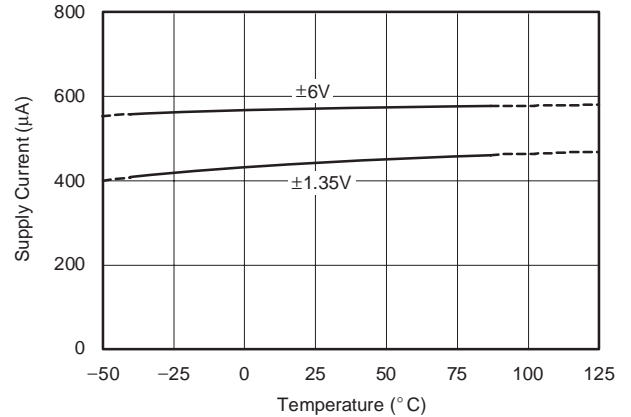
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE

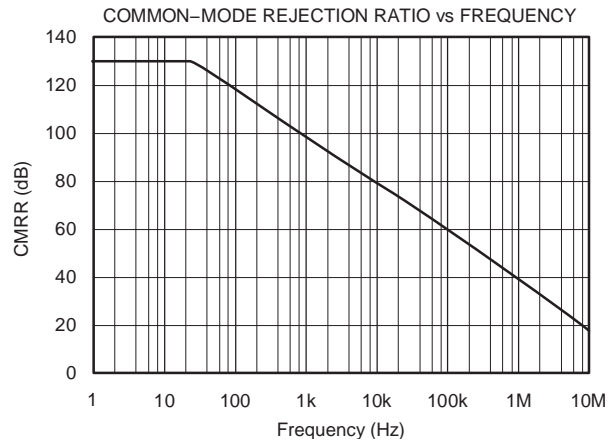
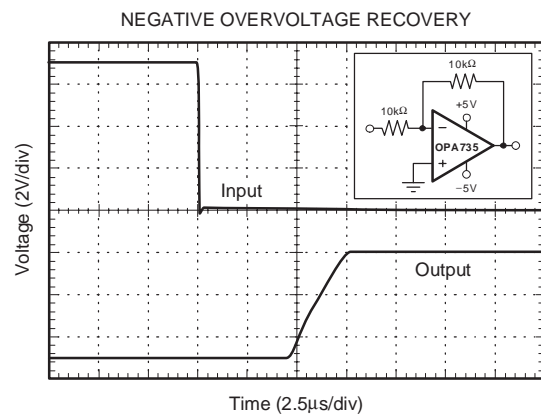
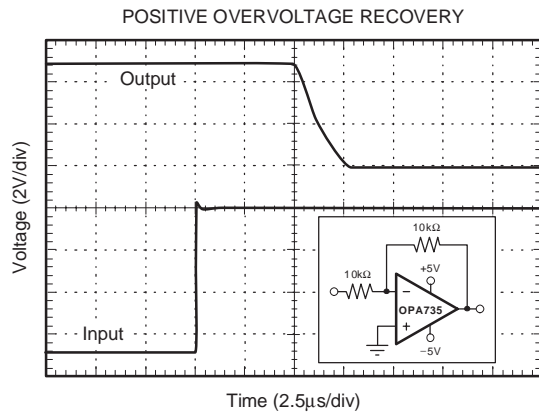
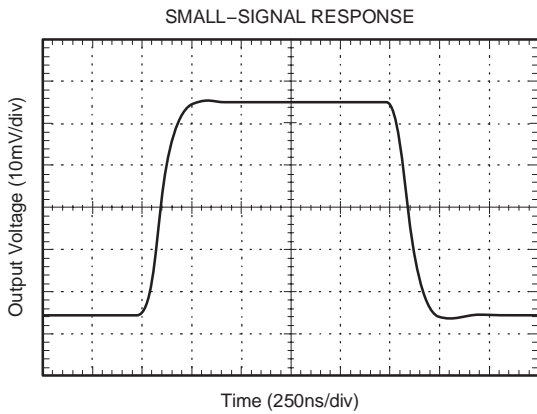
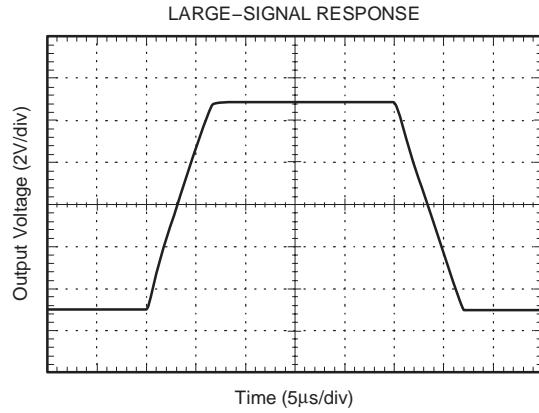
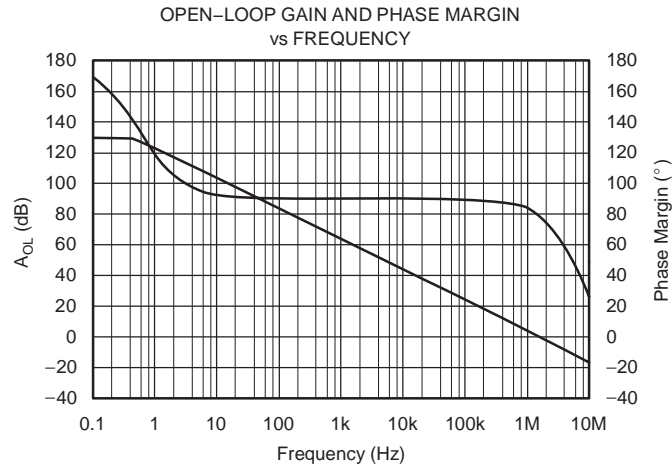


SUPPLY CURRENT vs TEMPERATURE



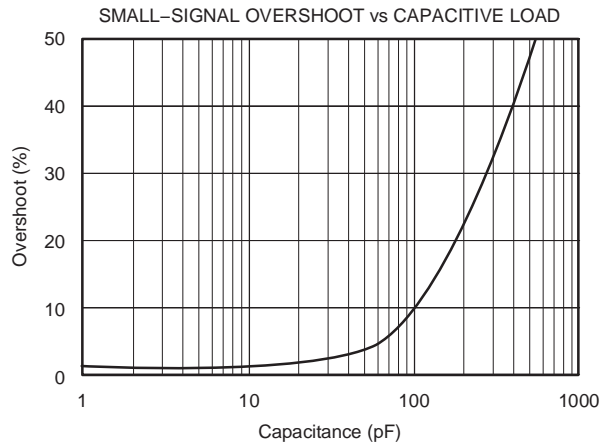
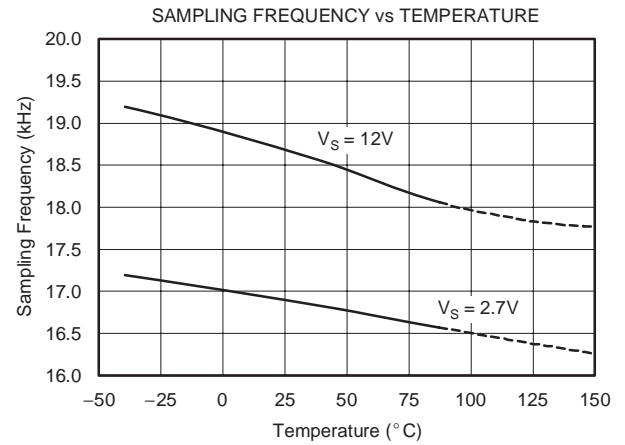
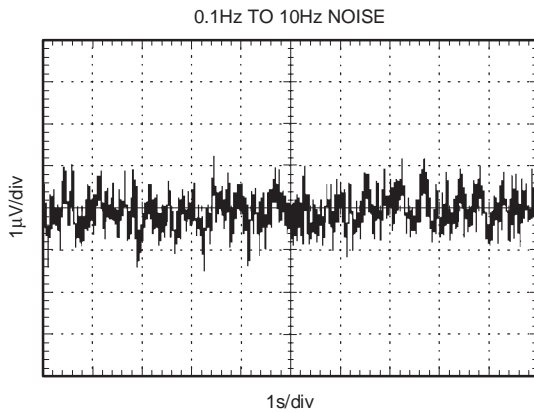
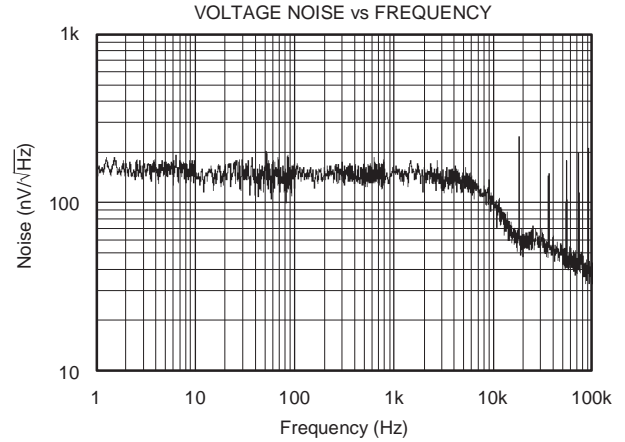
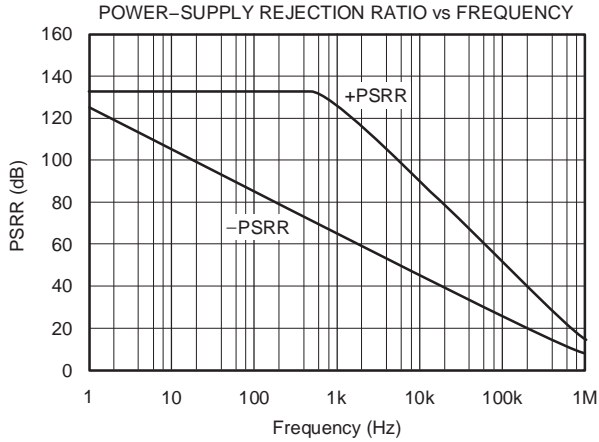
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as +10V).



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as +10V).



APPLICATIONS INFORMATION

The OPA734 and OPA735 series of op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and demonstrate very low drift over time and temperature.

Good layout practice mandates the use of a 0.1 μ F capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals:

1. Use low thermoelectric-coefficient connections (avoid dissimilar metals).
2. Thermally isolate components from power supplies or other heat sources.
3. Shield op amp and input circuitry from air currents such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μ V/ $^{\circ}$ C or higher, depending on the materials used.

OPERATING VOLTAGE

The OPA734 and OPA735 op amp family operates with a power-supply range of +2.7V to +12V (\pm 1.35V to \pm 6V). Supply voltages higher than +13.2V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA734 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V_{-} supply voltage of the op amp. A logic HIGH enables the op amp. A valid logic HIGH is defined as $> (V_{-}) + 2V$. The valid logic HIGH signal can be up to the positive supply, independent of the negative power supply voltage. A valid logic LOW is defined as $< 0.8V$ above the V_{-} supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin is connected to internal pull-up circuitry and will enable the device if this pin is left open circuit.

The logic input is a CMOS input. Separate logic inputs are provided for each op amp on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is 150 μ s, which includes one full auto-zero cycle required by the amplifier to return to V_{OS} accuracy. Prior to returning to full accuracy, the amplifier may function properly, but with unspecified offset voltage.

Disable time is 1.5 μ s. When disabled, the output assumes a high-impedance state. The disable state allows the OPA734 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from $(V_{-}) - 0.1V$ to $(V_{+}) - 1.5V$. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the specified input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.

Normally, input bias current is approximately 100pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

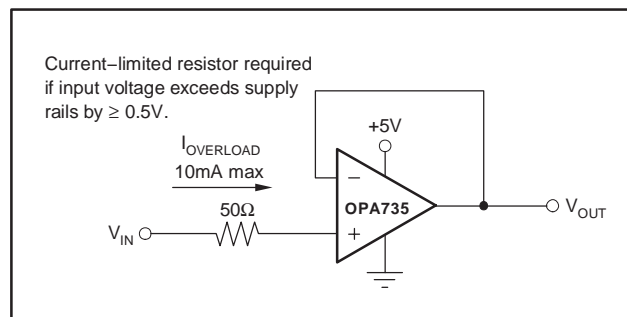


Figure 1. Input Current Protection

INTERNAL OFFSET CORRECTION

The OPA734 and OPA735 series of op amps use an auto-zero topology with a time-continuous 1.6MHz op amp in the signal path. This amplifier is zero-corrected every 100 μ s using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100 μ s in addition to the start-up time for the bias circuitry to achieve specified V_{OS} accuracy. Prior to this time, the amplifier may function properly but with unspecified offset voltage.

Low-gain (< 20) operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.1% of a full-scale input step change, one calibration cycle (100μs) can be required to achieve full accuracy.

The term *clock feedthrough* describes the presence of the clock frequency in the output spectrum. In auto-zeroed op amps, clock feedthrough may result from the settling of the internal sampling capacitor, or from the small amount of charge injection that occurs during the sample-and-hold of the op amp offset voltage. Feedthrough can be minimized by keeping the source impedance relatively low (< 1kΩ) and matching the source impedance on both input terminals. If the source resistance is high (> 1kΩ) feedthrough can generally be reduced with a capacitor of 1nF or greater in parallel with the source or feedback resistors. See the circuit application examples.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

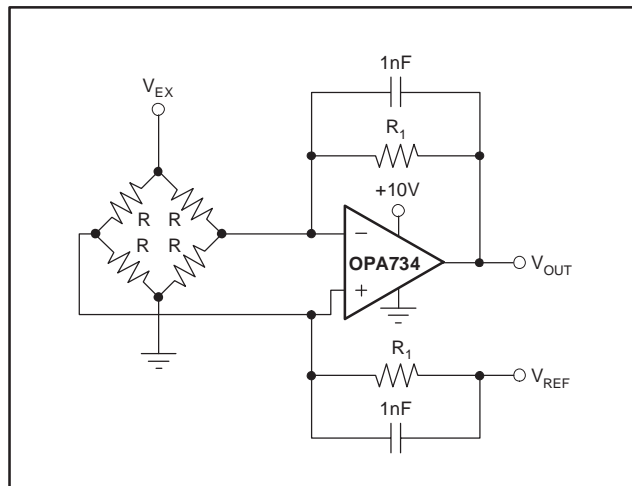


Figure 2. Single Op Amp Bridge Amplifier Circuit

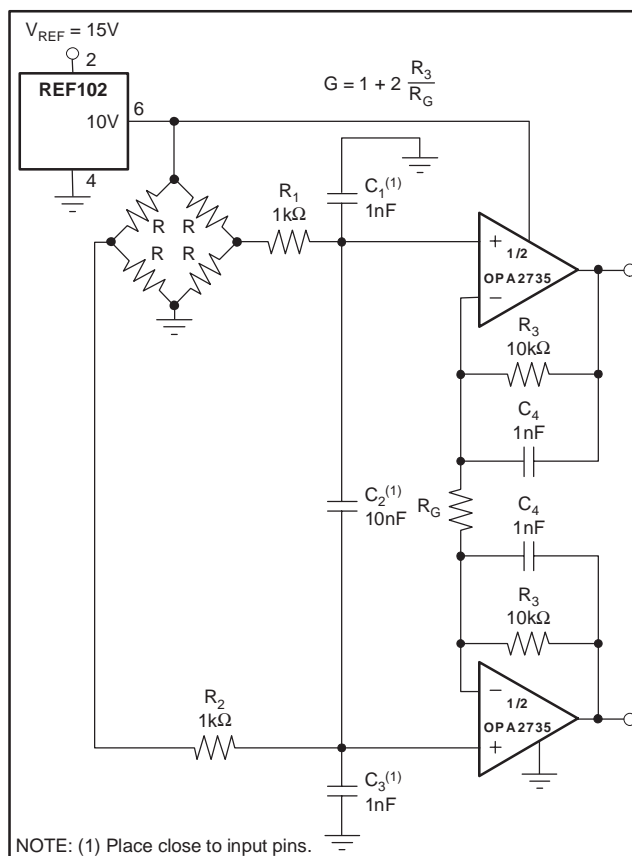


Figure 3. Differential Output Bridge Amplifier

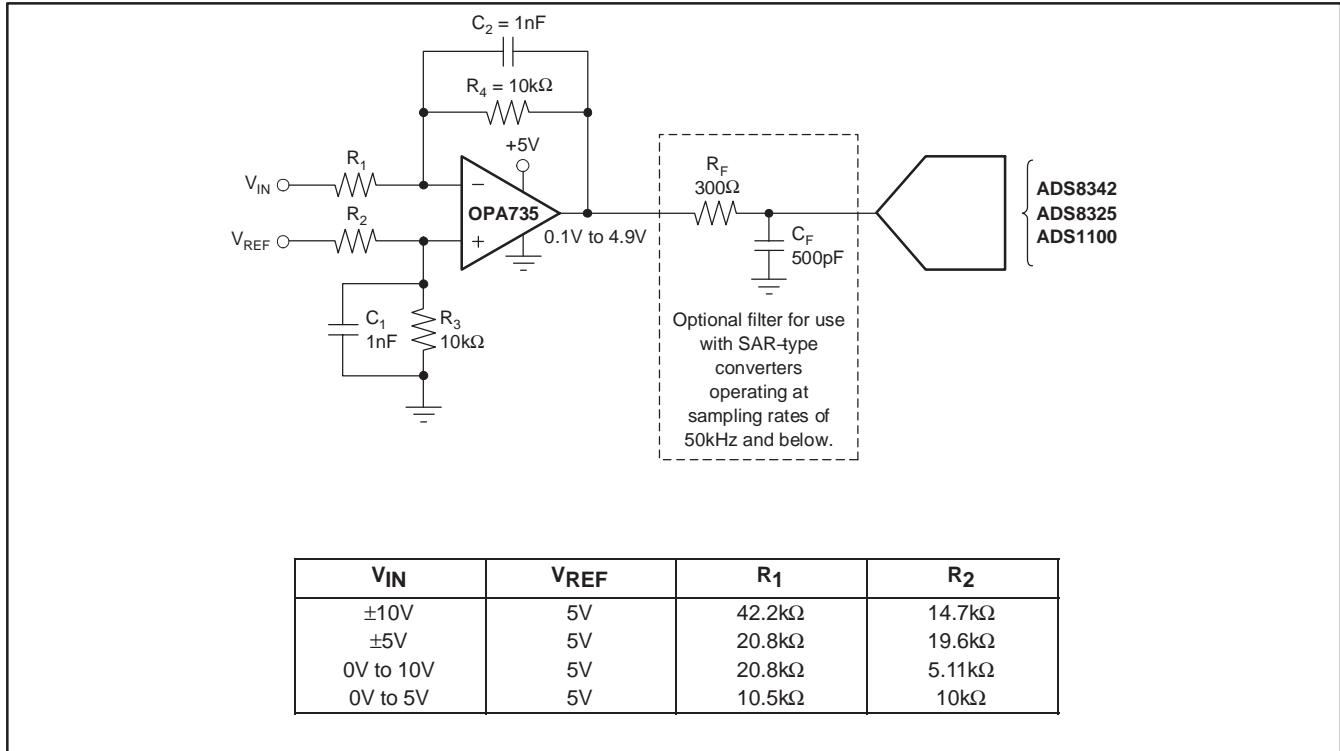


Figure 4. Driving ADC

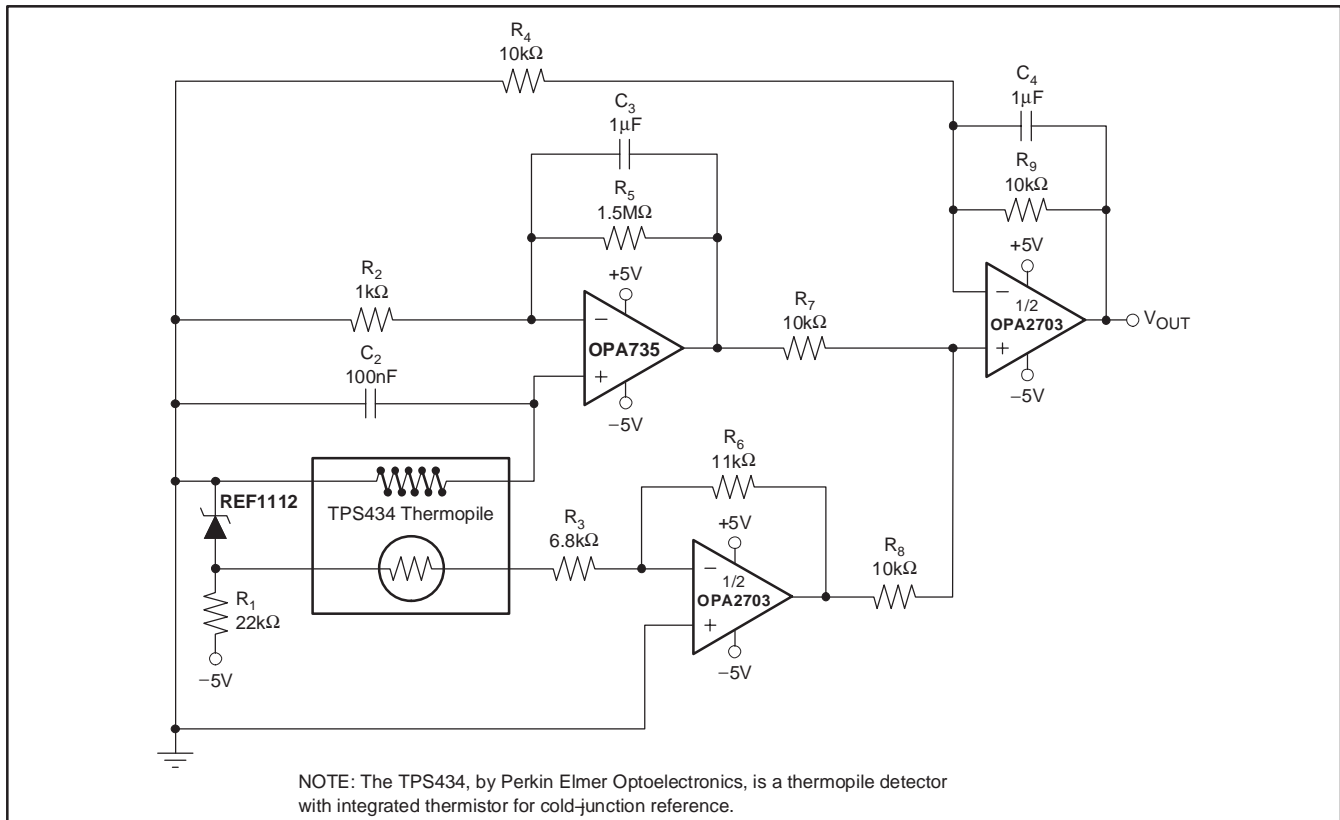


Figure 5. Thermopile Non-Contact Surface Temperature Measurement

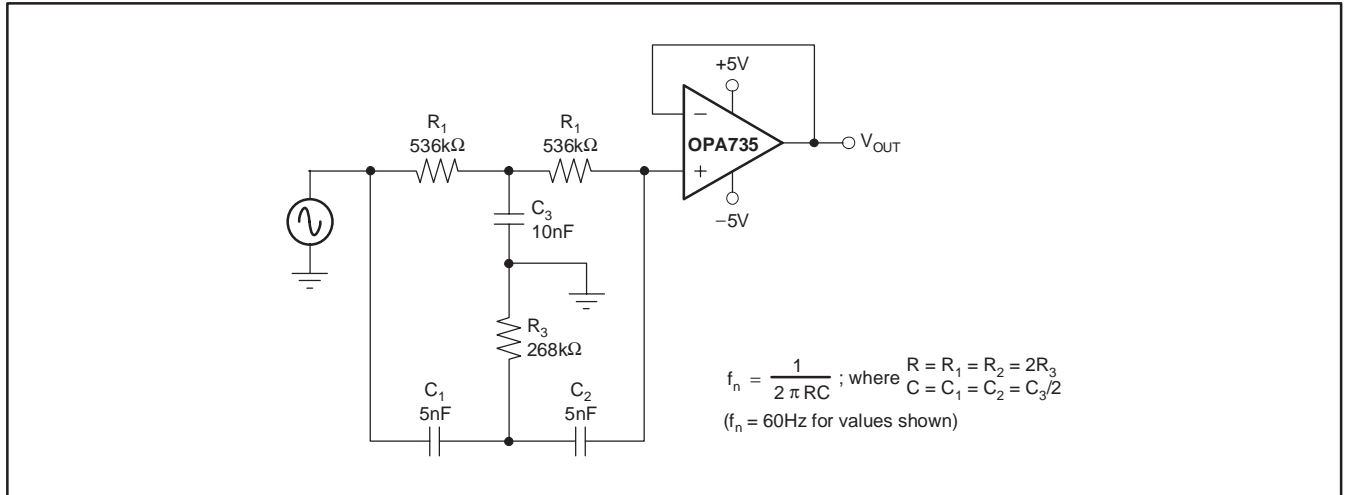


Figure 6. Twin-T Notch Filter

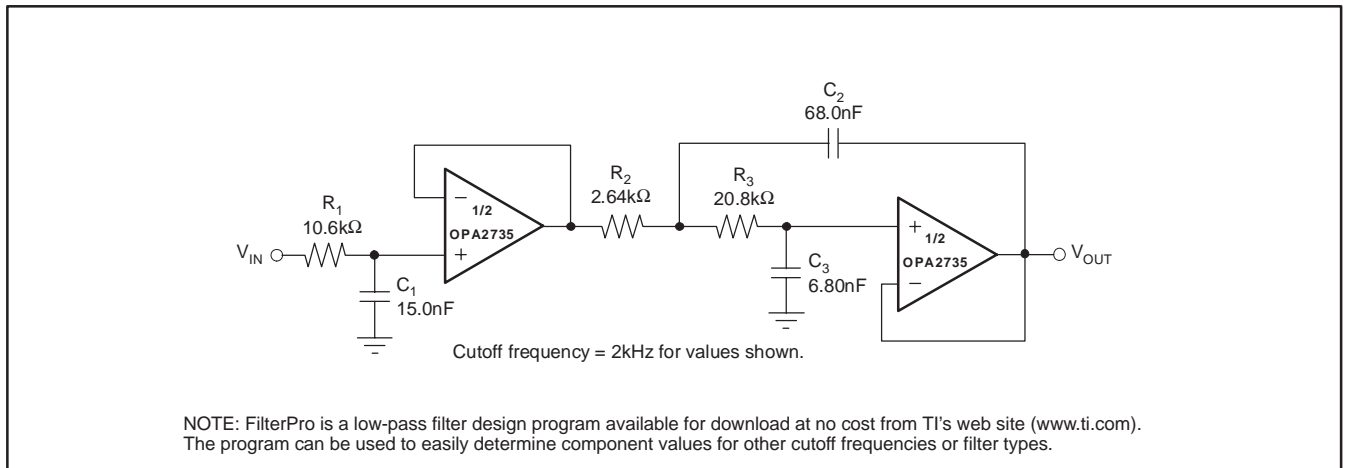


Figure 7. High DC Accuracy, 3-Pole Low-Pass Filter

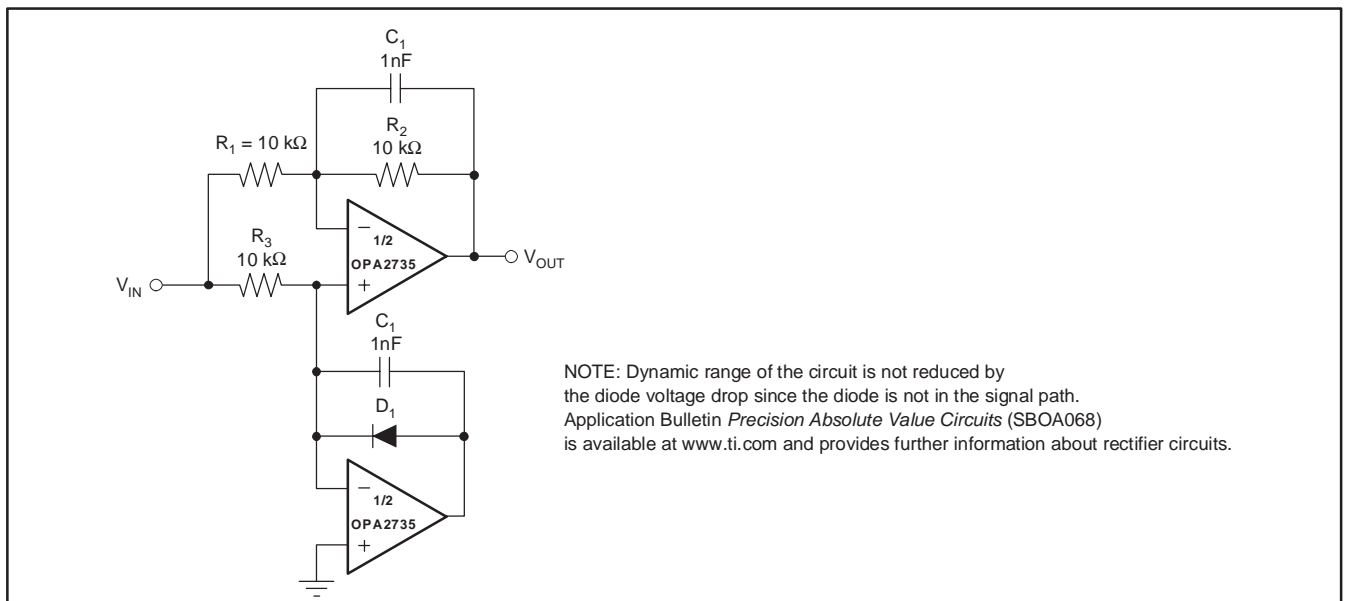
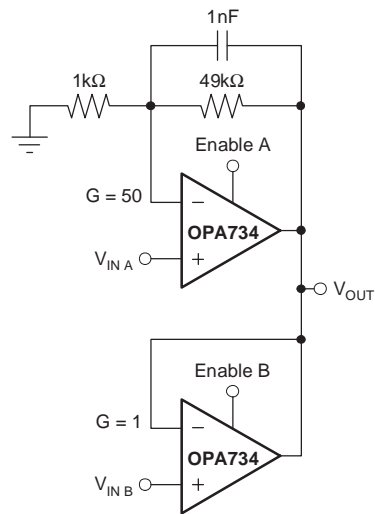


Figure 8. Precision Full-Wave Rectifier with Full Dynamic Range



Enable inputs are CMOS logic compatible.

Figure 9. High-Precision 2-Input MUX for Programmable Gain

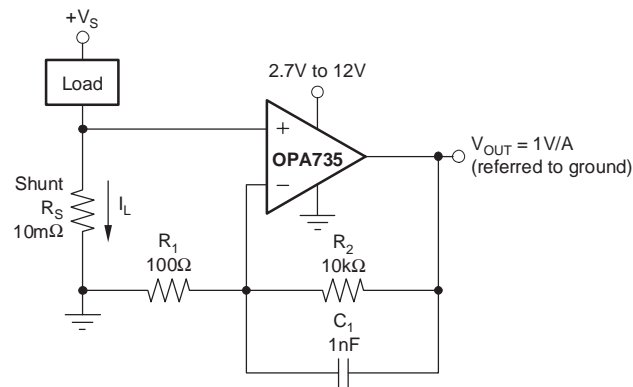


Figure 10. Low-Side Power-Supply Current Sensing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2734AIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	Call TI NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2734AIDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	Call TI NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2735AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA734AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 734A	Samples
OPA734AIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA734AIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA735AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples
OPA735AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA734AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA734AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA735AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA735AIDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2735AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA734AIDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
OPA734AIDBVT	SOT-23	DBV	6	250	445.0	220.0	345.0
OPA735AIDBVR	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA735AIDBVT	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA735AIDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2735AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2735AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA734AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA735AID	D	SOIC	8	75	506.6	8	3940	4.32

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

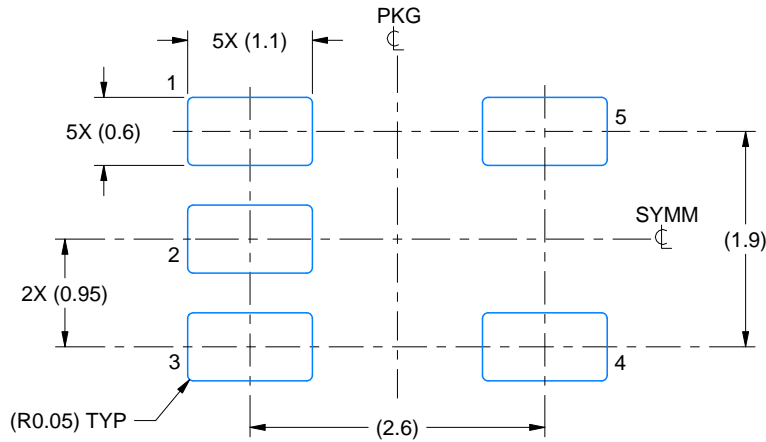
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

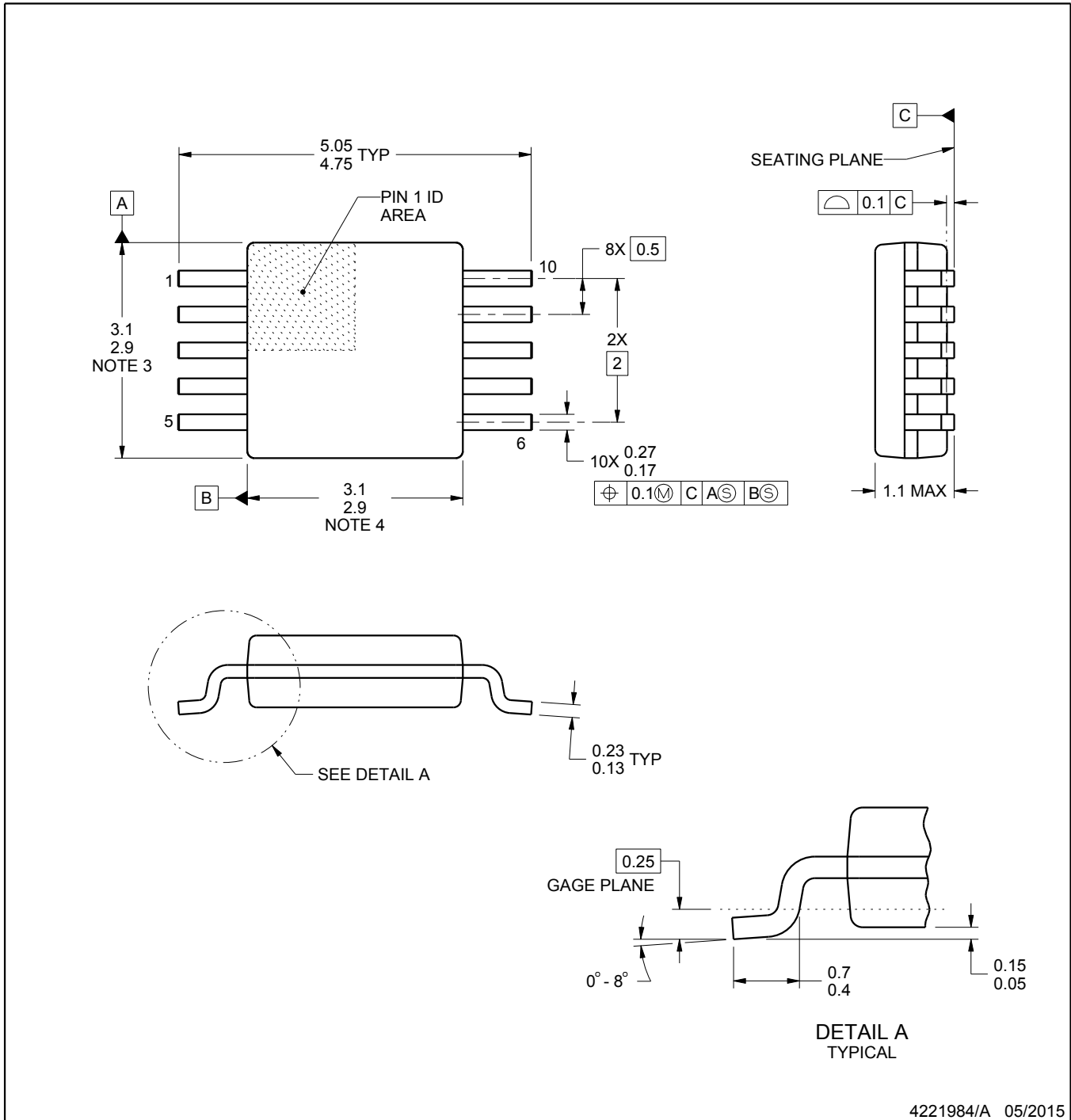
DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

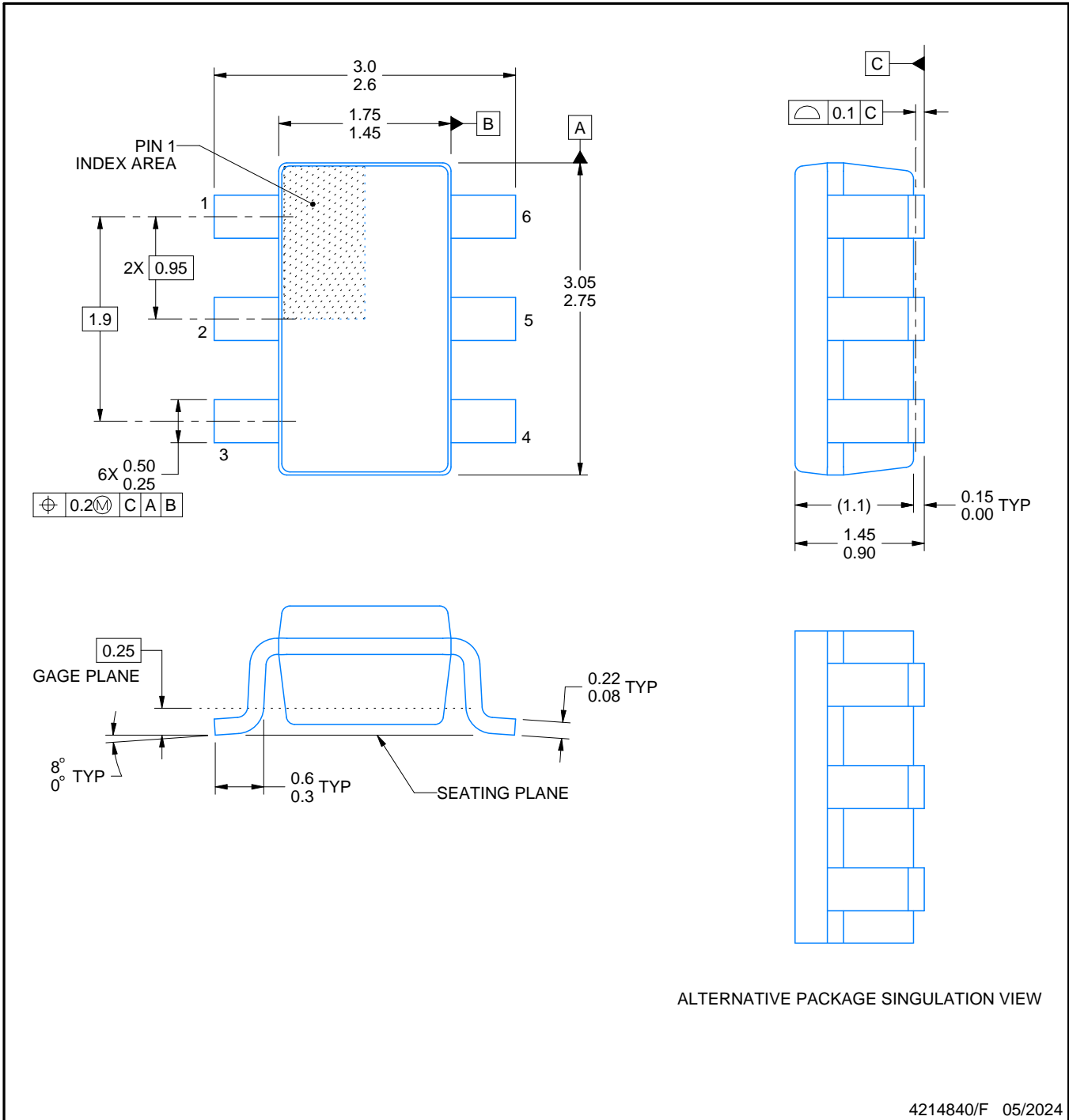
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0006A



PACKAGE OUTLINE SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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