PCA9306H Dual Bidirectional I²C Bus and SMBus Voltage-Level Translator

1 Features

- 2-Bit bidirectional translator for SDA and SCL lines in mixed-mode I²C Applications
- I²C and SMBus compatible
- Less than 1.5ns maximum propagation delay to accommodate standard-mode and fast-mode I²C devices and multiple controllers
- Negative glitch immunity on the I²C lines when EN = 0V
- Allows voltage-level translation between
  - 1.2V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  - 1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  - 2.5V V_{REF1} and 3.3V or 5V V_{REF2}
  - 3.3V V_{REF1} and 5V V_{REF2}
- Provides bidirectional voltage translation with no direction pin
- Low 3.5Ω ON-state resistance between input and output ports provides less signal distortion
- Open-drain I²C I/O ports (SCL1, SDA1, SCL2, and SDA2)
- 5V Tolerant I²C I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2, and SDA2 pins for EN = low
- Lockup-free operation for isolation when EN = low
- Flow-through pinout for ease of printed-circuit-board trace routing
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000V Human-body model (A114-A)
  - 1000V Charged-device model (C101)

2 Applications

- I²C, SMBus, PMBus, MDIO, UART, low-speed SDIO, GPIO, and other two-signal interfaces
- Servers
- Routers (telecom switching equipment)
- Optical Modules
- Enterprise
- Personal Computers
- Industrial Automation

3 Description

The PCA9306H device is a dual bidirectional I²C and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2V to 3.3V V_{REF1} and 1.8V to 5.5V V_{REF2}.

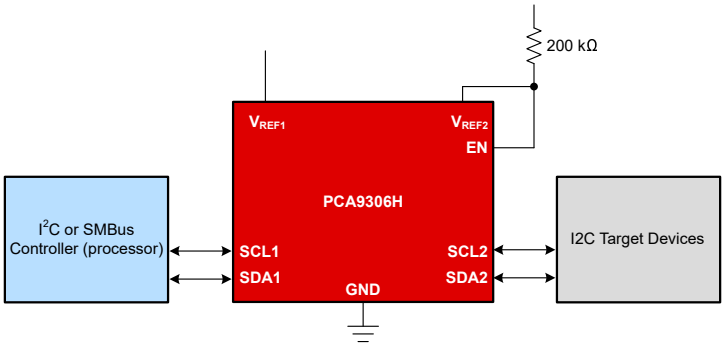
The PCA9306H device allows bidirectional voltage translations between 1.2V and 5V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In addition to voltage translation, the PCA9306H device can be used to separate a 400kHz bus from a 100kHz bus by controlling the EN pin to disconnect the slower bus during fast-mode communication.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
PCA9306H	X2SON (8)	1.4mm × 1mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....5
5.5 Electrical Characteristics....5
5.6 Switching Characteristics (Translating Down)....6
5.7 Switching Characteristics (Translating Up)....6
5.8 Typical Characteristics....7
6 Parameter Measurement Information....8
7 Detailed Description....9
7.1 Overview....9
7.2 Functional Block Diagram....14
7.3 Feature Description....14
7.4 Device Functional Modes....15
8 Application and Implementation....15
8.1 Application Information....15
8.2 Typical Application....15
8.3 Power Supply Recommendations....17
8.4 Layout....17
9 Device and Documentation Support....19
9.1 Receiving Notification of Documentation Updates....19
9.2 Support Resources....19
9.3 Trademarks....19
9.4 Electrostatic Discharge Caution....19
9.5 Glossary....19
10 Revision History....19

4 Pin Configuration and Functions

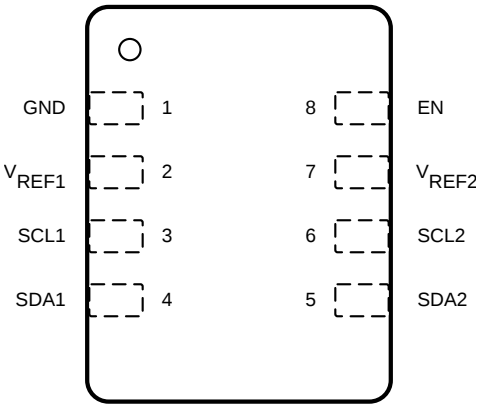


Figure 4-1. DQE Package 8-Pin X2SON (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
	DQE		
GND	1	—	Ground
VREF1	2	I	Low-voltage-side reference supply voltage for SCL1 and SDA1
SCL1	3	I/O	Serial clock, low-voltage side
SDA1	4	I/O	Serial data, low-voltage side
SDA2	5	I/O	Serial data, high-voltage side
SCL2	6	I/O	Serial clock, high-voltage side
V_{REF2}	7	I	High-voltage-side reference supply voltage for SCL2 and SDA2
EN	8	I	Switch enable input

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{REF1}	DC reference voltage range	–0.5	7	V
V_{REF2}	DC reference bias voltage range	–0.5	7	V
V_I	Input voltage range (2)	-0.5	7	V
$V_{I/O}$	Input-output voltage range (2)	-0.5	7	V
$V_{I/O(glitch)}$	Input-output voltage range for glitch transients (3)	-3.3	7	V
	Continuous channel current		128	mA
I_{IK}	Input Clamp Current (V_I < 0)		–50	mA
$T_{J(Max)}$	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and input-output negative voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The time of the transient must not exceed 50 nanoseconds in length. The minimum pulse that PCA9306H can reject is -3.3V for 50ns.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{I/O}$	Input-output voltage	SCL1, SDA1, SCL2, SDA2	0	5.5	V
V_{REF1} (1)	Reference Voltage		0	5.5	V
V_{REF2} (1)	Reference Voltage		0	5.5	V
EN-Switch(2)	Switch mode enable voltage (Switch mode enable voltage)		1.5	5.5	V
EN	Enable input voltage		0	5.5	V
I_{PASS}	Pass switch current			64	mA
T_A	Ambient temperature		–40	85	°C

(1) To support translation, V_{REF1} supports 0.85 V to VREF2 - 0.6V. V_{REF2} must be between VREF1 + 0.6V to 5.5V. See Typical Application for more information.
(2) To support switching, V_{REF1} and V_{REF2} Do not need to be connected. EN pin should use a voltage not less than 1.5V when the switch mode is to be enabled. Enabled voltage on this pin must be equal to 1.5V or I/O supply voltage, whichever is higher.

5.4 Thermal Information

THERMAL METRIC(1)	PCA9306H	UNIT
	DQE	
	8 Pins	
$R_{\theta JA}$	297.0	°C/W
$R_{\theta JC(top)}$	139.4	°C/W
$R_{\theta JB}$	192.7	°C/W
Ψ_{JT}	14.4	°C/W
Ψ_{JB}	192.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP (1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = -18mA	EN = 0V		-1.2		0	V
I_{IH}	Input leakage current		V_I = 5V, V_O = 0V	EN = 0V				5	µA
V_T	Threshold voltage		I_O = 500µA	V_I = 0.1V, V_O = 0V, Find V_{EN} where IO = 500 µA			0.8	1.0	V
$C_{I(EN)}$	Input capacitance		V_I = 3V or 0V				21	30	pF
$C_{IO(off)}$	Off capacitance	SCLn, SDAn	V_O = 3V or 0V	EN = 0V			4.2	4.6	pF
$C_{IO(on)}$	On capacitance	SCLn, SDAn	V_O = 3V or 0V	EN = 3V			20.5	22	pF
R_{ON} (2)	On-state resistance	SCLn, SDAn (-40to 85C)	V_I = 0V(3)	I_O = 64mA	EN = 4.5V		2.9	5.5	Ω
			V_I = 0V(3)	I_O = 64mA	EN = 3V		4	7	Ω
			V_I = 0V(3)	I_O = 64mA	EN = 2.3V		7.1	12	Ω
			V_I = 0V(3)	I_O = 15mA	EN = 1.5V		10	32	Ω
			V_I = 2.4V(4)	I_O = 15mA	EN = 4.5V		8.5	15	Ω
			V_I = 1.7V(4)	I_O = 15mA	EN = 2.3V		60	140	Ω
			V_I = 2.4V(4)	I_O = 15mA	EN = 3V		60	140	Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two terminals.
(3) Measured in current source configuration only.
(4) Measured in current sink configuration only.

5.6 Switching Characteristics (Translating Down)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	EN = 3.3V, V_{IH} = 3.3V, V_{IL} = 0, V_M = 1.15V(2)	C_L = 15pF			0.8	ns
			C_L = 30pF			0.9	
			C_L = 50pF			1.0	
T_{PHL}	High to low propagation delay		C_L = 15pF			2.1	ns
			C_L = 30pF			3.2	
			C_L = 50pF			5.9	
T_{PLH}	Low-to-high propagation delay	EN = 2.5V, V_{IH} = 3.3V, V_{IL} = 0, V_M = 0.75V(2)	C_L = 15pF			0.6	ns
			C_L = 30pF			0.7	
			C_L = 50pF			0.8	
T_{PHL}	High to low propagation delay		C_L = 15pF			4.3	ns
			C_L = 30pF			9.1	
			C_L = 50pF			15.7	

(1) Guaranteed by simulation, not tested in production
(2) Translating Down: the high-voltage side driving toward the low-voltage side.

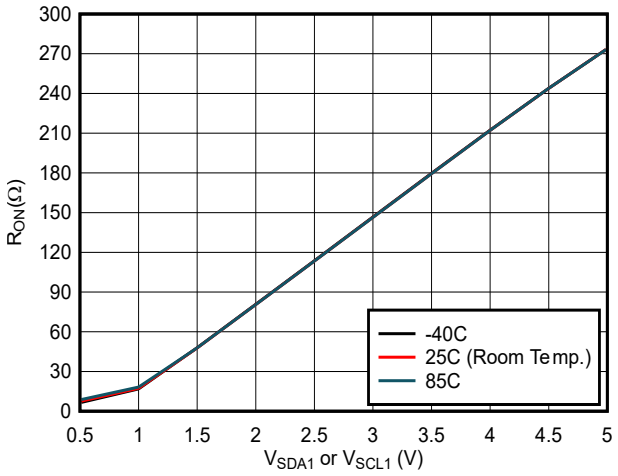
5.7 Switching Characteristics (Translating Up)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	EN = 3.3V, V_{IH} = 2.3V, V_{IL} = 0V, V_T = 3.3V, V_M = 1.15V, R_L = 300Ω(2)	C_L = 15pF			0.7	ns
			C_L = 30pF			1.1	
			C_L = 50pF			2.3	
T_{PHL}	High to low propagation delay		C_L = 15pF			3.5	ns
			C_L = 30pF			6.0	
			C_L = 50pF			9.1	
T_{PLH}	Low-to-high propagation delay	EN = 2.5V, V_{IH} = 2.3V, V_{IL} = 0V, V_T = 3.3V, V_M = 0.75V, R_L = 300Ω(2)	C_L = 15pF			0.2	ns
			C_L = 30pF			0.4	
			C_L = 50pF			3.3	
T_{PHL}	High to low propagation delay		C_L = 15pF			18.9	ns
			C_L = 30pF			23.5	
			C_L = 50pF			30	

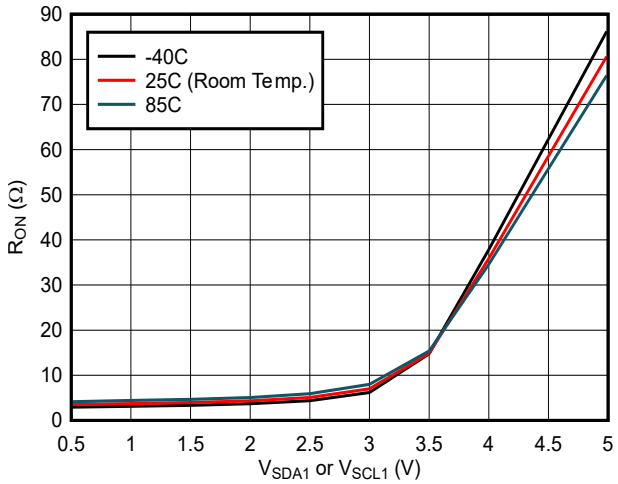
(1) Guaranteed by simulation, not tested in production
(2) Translating up: the low-voltage side driving toward the high-voltage side.

5.8 Typical Characteristics



V_{EN} = 1.5 V I_I = 15 mA

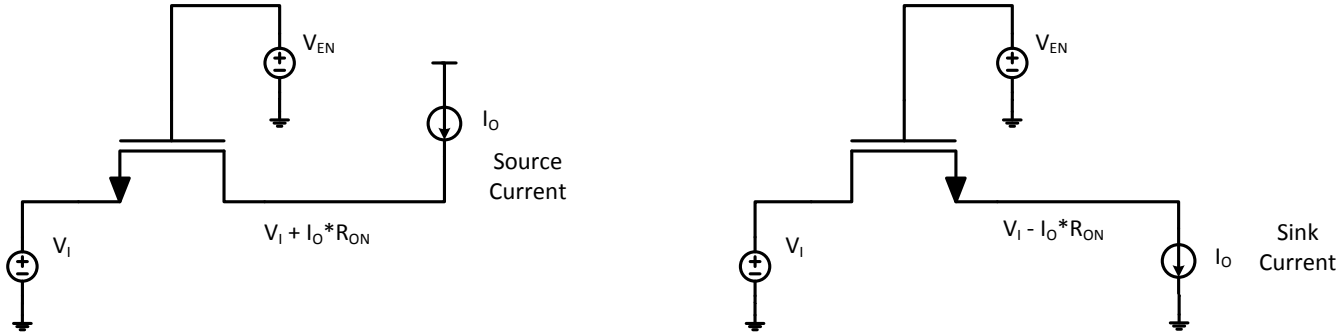
Figure 5-1. On-Resistance (R_{ON}) vs Input Voltage (V_{SDA1} or V_{SCL1})



V_{EN} = 4.5 V I_I = 15 mA

Figure 5-2. On-Resistance (R_{ON}) vs Input Voltage (V_{SDA1} or V_{SCL1})

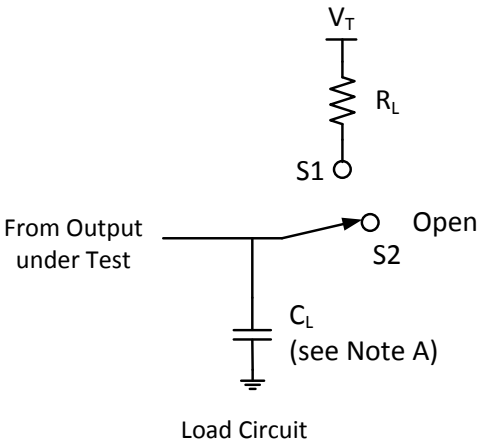
6 Parameter Measurement Information



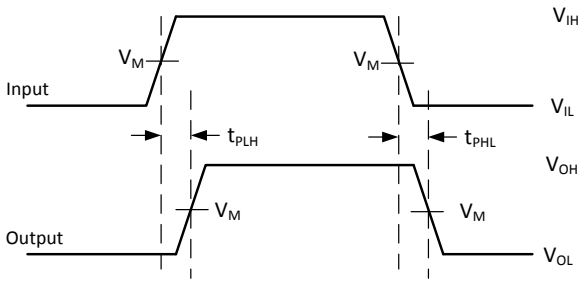
a) Current Source Configuration

b) Current Sink Configuration

Figure 6-1. Current Source and Current Sink Configurations for R_{ON} Measurements



USAGE	SWITCH
Translating up	S1
Translating down	S2



NOTES: A. C_L includes probe and jig capacitance
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 6-2. Load Circuit for Outputs

7 Detailed Description

7.1 Overview

The PCA9306H device is a dual bidirectional I^2C and SMBus voltage-level translator with an enable (EN) input and operates without use of a direction pin. The voltage supply range for V_{REF1} is 1.2V to 3.3V and the supply range for V_{REF2} is 1.8V to 5.5V.

The PCA9306H device can also be used to run two buses, one at 400kHz operating frequency and the other at 100kHz operating frequency. If the two buses are operating at different frequencies, the 100kHz bus must be disconnected by using the EN pin when the 400kHz operation of the main bus is required. If the controller is running at 400kHz, the maximum system operating frequency can be less than 400kHz because of the delays added by the level shifter.

In I^2C applications, the bus capacitance limit of 400pF restricts the number of devices and bus length. The capacitive load on both sides of the PCA9306H device must be taken into account when approximating the total load of the system, ensuring the sum of both sides is under 400pF.

Both the SDA and SCL channels of the PCA9306H device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete-transistor voltage-translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less-ESD-resistant devices.

7.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as V_{th}, which appears multiple times throughout this document when discussing the NFET between V_{REF1} and V_{REF2}. The value of V_{th} is approximately 0.6V at room temperature.

7.1.2 Correct Device Set Up

In a normal set up shown in Figure 7-1, the enable pin and V_{REF2} are shorted together and tied to a 200kΩ resistor, and a reference voltage equal to V_{REF1} plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

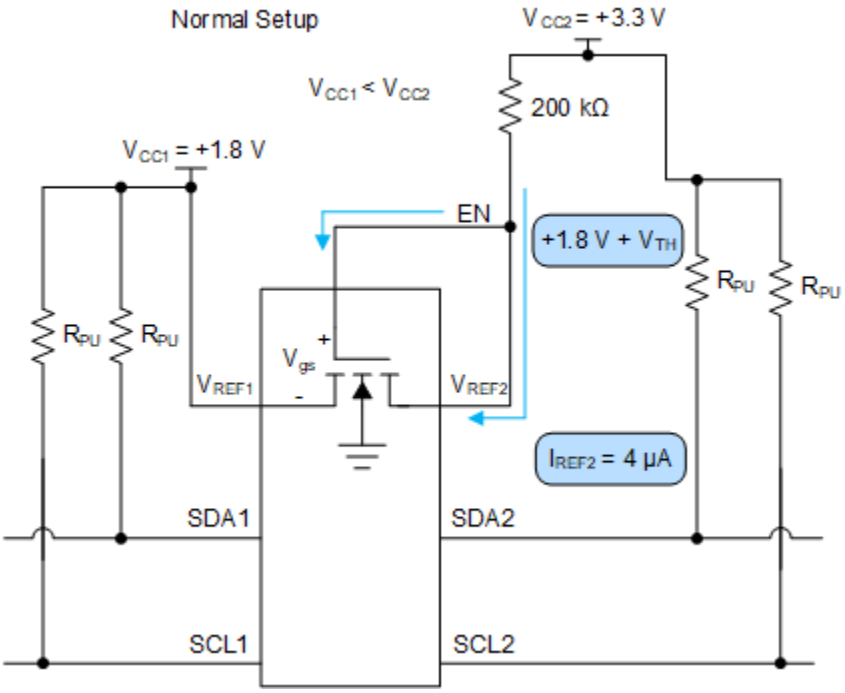


Figure 7-1. Normal Setup

Care should be taken to make sure V_{REF2} has an external resistor tied between it and V_{CC2}. If V_{REF2} is tied directly to the V_{CC2} rail without a resistor, then there is no external resistance from the V_{CC2} to V_{CC1} to limit the current such as in Figure 7-2. This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 6.1. The continuous channel current is larger with a higher voltage difference between V_{CC1} and V_{CC2}.

Figure 7-2 shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th}, the impedance between V_{CC1} and V_{CC2} is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th}. During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

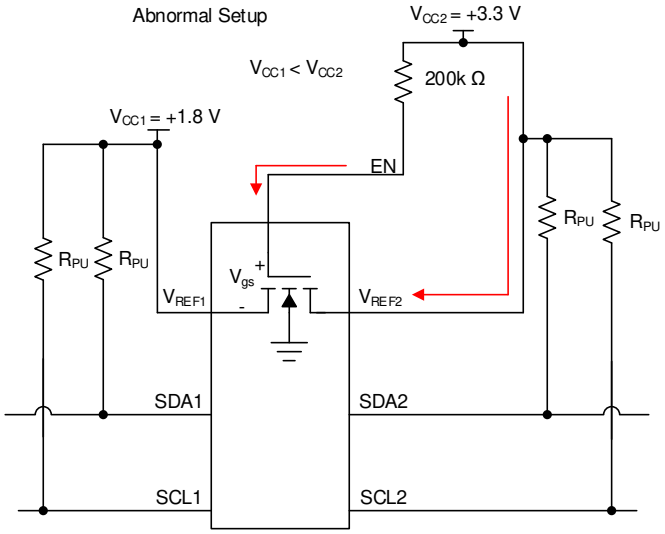


Figure 7-2. Abnormal Setup

7.1.3 Switch and Translation Configuration

PCA9306H has the capability of being used with its V_{REF1} voltage equal to V_{REF2}. This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in Figure 7-3 and translation mode is shown in Figure 7-4.

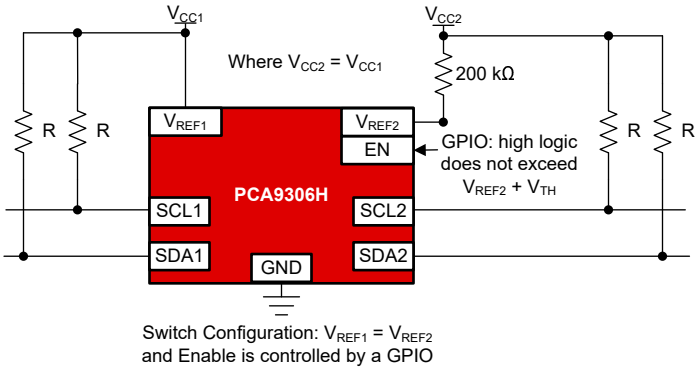


Figure 7-3. Switch Configuration

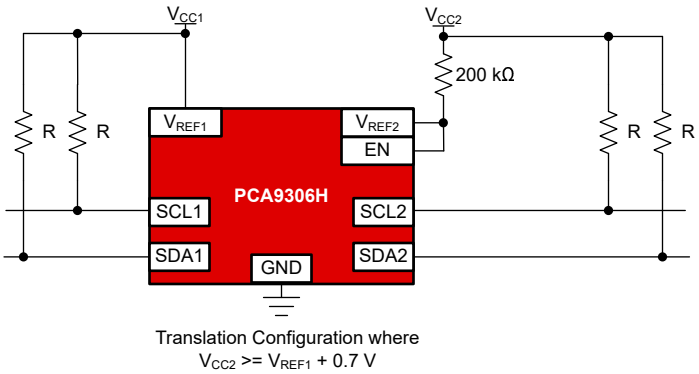


Figure 7-4. Translation Configuration

When PCA9306H is in the switch configuration (V_{REF1} = V_{REF2}), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the PCA9306H has the same propagation delay from side one to two and side two to one. The propagation delays become lower when V_{CC1}/V_{CC2} is larger. For example, the propagation delay at 1.8V is longer than at 5V in the switching configuration. When PCA9306H is in translation mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between V_{CC2} and V_{CC1} becomes.

7.1.4 Negative Glitch Immunity

PCA9306H is designed to reject negative glitch artifacts resulting from a hot-plug event. The device is able to reject up to a 50ns, 3.3V to -3.3V input swing from coupling to the output. The negative voltage spike is a result of uncharged parasitic capacitance and parasitic inductance on a separate module that is being hot-plugged into the live PCA9306H level translator. The sudden connection of this parasitic capacitance on the I2C lines causes the voltage to dip. The combination of parasitic capacitance and inductance can cause undershoot past GND which is rejected by PCA9306H, allowing uninterrupted I2C communication on the output side.

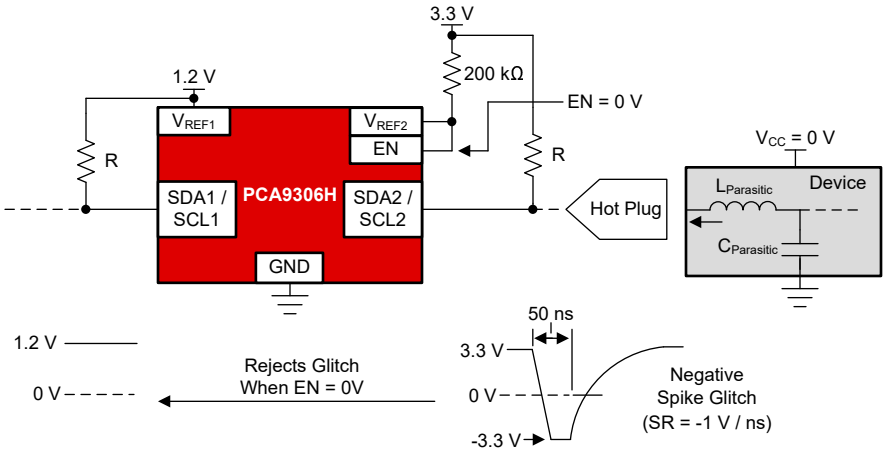


Figure 7-5. Negative Spike Rejection During Hot-Plug Event

7.1.5 Controller on Side 1 or Side 2 of Device

I2C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. PCA9306H was designed to allow for signals to be able to be transmitted from either side, thus allowing for the controller to be able to placed on either side of the device. Figure 7-6 shows the controller on side two as opposed to the diagram on page 1 of this data sheet.

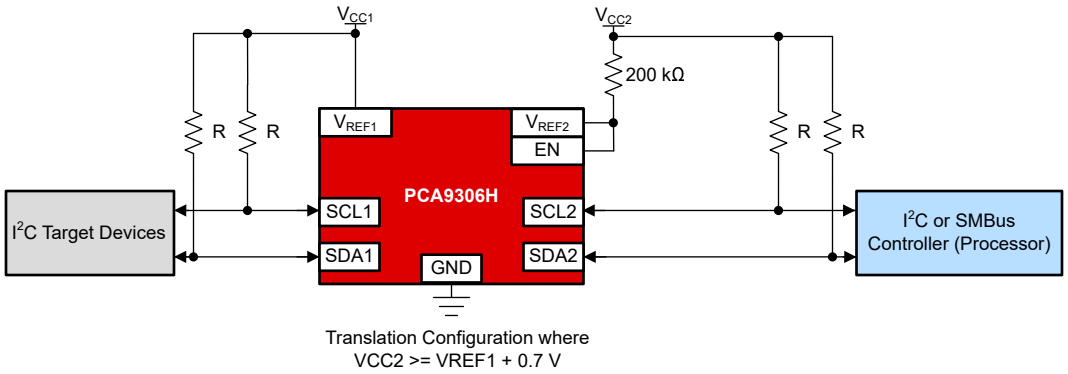


Figure 7-6. Controller on side 2 of PCA9306H

7.1.6 LDO and PCA9306H Concerns

The V_{REF1} pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO can lose its regulation because of the bias current from V_{REF2} to V_{REF1}. If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the V_{REF1} node (both external and parasitic). This results in an increase in voltage on the V_{REF1} node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the V_{REF1} node), then the V_{REF1} voltage ends up stabilizing when V_{gs} of the pass FET is equal to V_{th}. This means V_{REF1} node voltage is V_{CC2} - V_{th}. Note that any targets/controllers running off of the LDO now see the V_{CC2} - V_{th} voltage which can cause damage to those targets/controllers if they are not rated to handle the increased voltage.

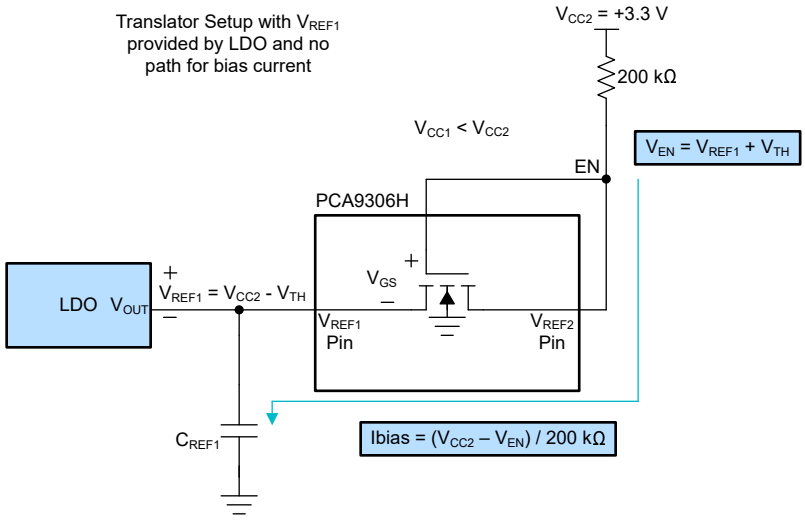


Figure 7-7. Example of no leakage current path when using LDO

To make sure the LDO does not lose regulation due to the bias current of PCA9306H, a weak pull down resistor can be placed on V_{REF1} to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by Equation 4 where 0.75 gives about 25% margin for error incase bias current increases during operation.

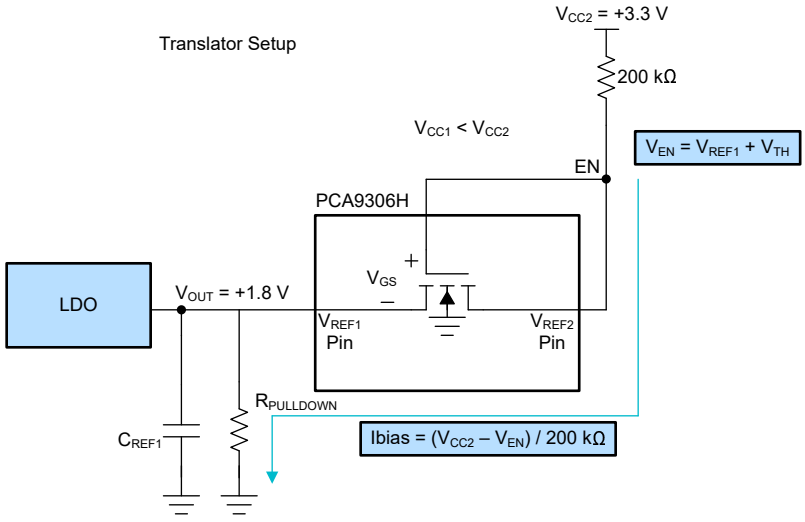


Figure 7-8. Example with Leakage current path when using an LDO

$$V_{en} = V_{REF1} + V_{th} \quad (1)$$

where

- V_{th} is approximately 0.6V

$$I_{bias} = (V_{CC2} - V_{en})/200k \quad (2)$$

$$R_{pulldown} = V_{OUT}/I_{bias} \quad (3)$$

$$\text{Recommended } R_{pulldown} = R_{pulldown} \times 0.75 \quad (4)$$

7.1.7 Current Limiting Resistance on V_{REF2}

The resistor is used to limit the current between V_{REF2} and V_{REF1} (denoted as R_{CC}) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = (V_{CC2} - V_{en})/R_{CC} : V_{en} = V_{REF1} + V_{th} \quad (5)$$

where

- V_{th} is approximately 0.6V

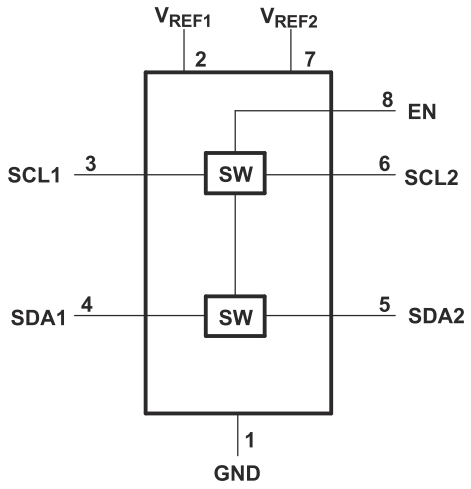
Keep in mind R_{CC} should not be sized low enough that I_{CC} exceeds the absolute maximum continuous channel current specified in section 6.1 which is described in Equation 6.

$$R_{CC}(min) \geq (V_{CC2} - V_{en})/0.128 : V_{en} = V_{REF1} + V_{th} \quad (6)$$

where

- V_{th} is approximately 0.6V

7.2 Functional Block Diagram



Block Diagram of PCA9306H

7.3 Feature Description

7.3.1 Enable (EN) Pin

The PCA9306H device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In Figure 8-1, the PCA9306H device is always enabled when power is applied to V_{REF2}. In Figure 8-2, the device is enabled when a control signal from a processor is in a logic-high state.

7.3.2 Voltage Translation

The primary feature of the PCA9306H device is translating voltage from an I^2C bus referenced to V_{REF1} up to an I^2C bus referenced to V_{DPU}, to which V_{REF2} is connected through a 200kΩ pullup resistor. Translation on a standard, open-drain I^2C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to V_{REF1} and connecting pullup resistors from SCL2 and SDA2 to V_{DPU}. Information on sizing the pullup resistors can be found in the *Sizing Pullup Resistors* section.

7.4 Device Functional Modes

INPUT EN(1)	TRANSLATOR FUNCTION
H	Logic Lows are propagated from one side to the other, Logic Highs blocked (independent pull up resistors passively drive the line high)
L	Disconnect

(1) The SCL switch conducts if EN is ≥ 0.6V higher than SCL1 or SCL2. The same is true of SDA.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 General Applications of I²C

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices in addition to SMBus devices. Standard-mode I²C devices only specify 3mA in a generic I²C system where standard-mode devices and multiple controllers are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

8.2 Typical Application

Figure 8-1 and Figure 8-2 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

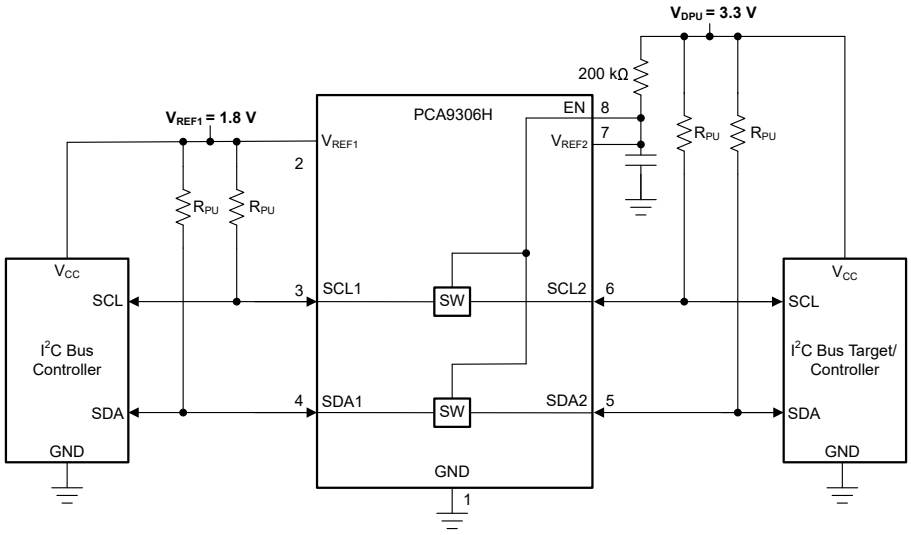


Figure 8-1. Typical Application Circuit (Switch Always Enabled)

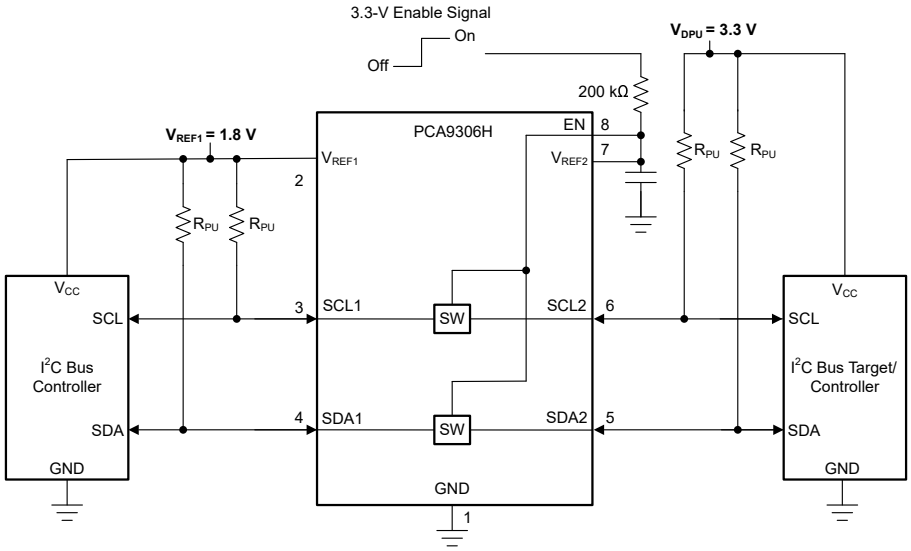


Figure 8-2. Typical Application Circuit (Switch Enable Control)

8.2.1 Design Requirements

		MIN	TYP(1)	MAX	UNIT
V_{REF2}	Reference voltage	V_{REF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	1.2	1.5	4.4	V
I_{PASS}	Pass switch current		6		mA
I_{REF}	Reference-transistor current		5		µA

(1) All typical values are at T_A = 25°C.

8.2.2 Detailed Design Procedure

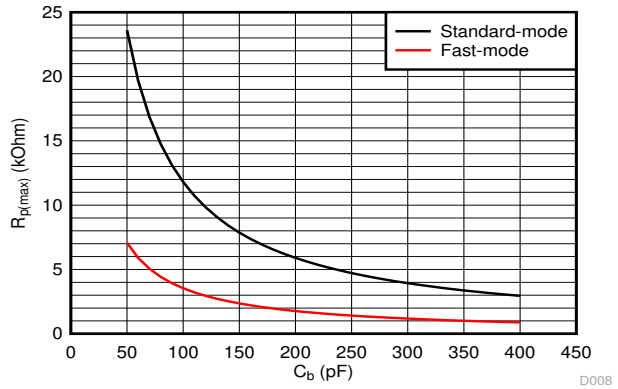
8.2.2.1 Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200kΩ). This allows V_{REF2} to regulate the EN input. A 100pF filter capacitor connected to V_{REF2} is recommended. The I^2C bus controller output can be push-pull or open-drain (pullup resistors may be required) and the I^2C bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

8.2.2.2 Sizing Pullup Resistors

To get an estimate for the range of values that can be used for the pullup resistor, please refer to the application note I2C Bus Pullup Resistor Calculation. Figure 8-3 and Figure 8-4 respectively show the maximum and minimum pullup resistance allowable by the I^2C specification for standard-mode (100kHz) and fast-mode (400kHz) operation.

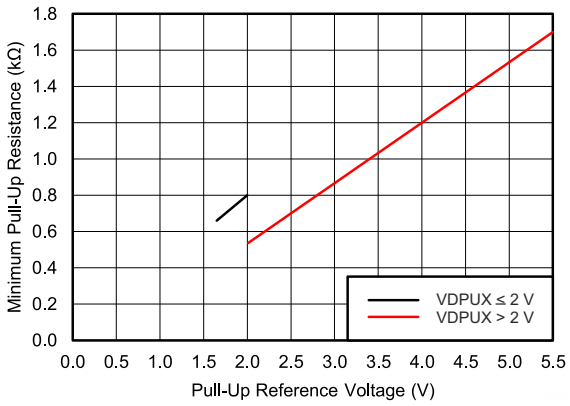
8.2.3 Application Curve



Standard mode (f_{SCL} = 100 kHz, t_r = 1 µs)

Fast mode (f_{SCL} = 400 kHz, t_r = 300 ns)

Figure 8-3. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 x V_{DPUX} , I_{OL} = 2 mA when V_{DPUX} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

Figure 8-4. Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage (V_{DPUX})

8.3 Power Supply Recommendations

For supplying power to the PCA9306H device, the V_{REF1} pin can be connected directly to a power supply. The V_{REF2} pin must be connected to the V_{DPU} power supply through a 200kΩ resistor. Failure to have a high-impedance resistor between V_{REF2} and V_{DPU} results in excessive current draw and unreliable device operation. It is also worth noting, that to support voltage translation, the PCA9306H must have the EN and VREF2 pins shorted and then pulled up to V_{DPU} through a high-impedance resistor.

8.4 Layout

8.4.1 Layout Guidelines

For printed-circuit board (PCB) layout of the PCA9306H device, common PCB layout practices must be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100pF filter capacitor must be placed as close to V_{REF2} as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200kΩ resistor results in longer turnon and turnoff times for the PCA9306H device. These best practices are shown in Figure 8-5.

For the layout example provided in Figure 8-5, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to V_{CC} or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in Figure 8-5.

8.4.2 Layout Example

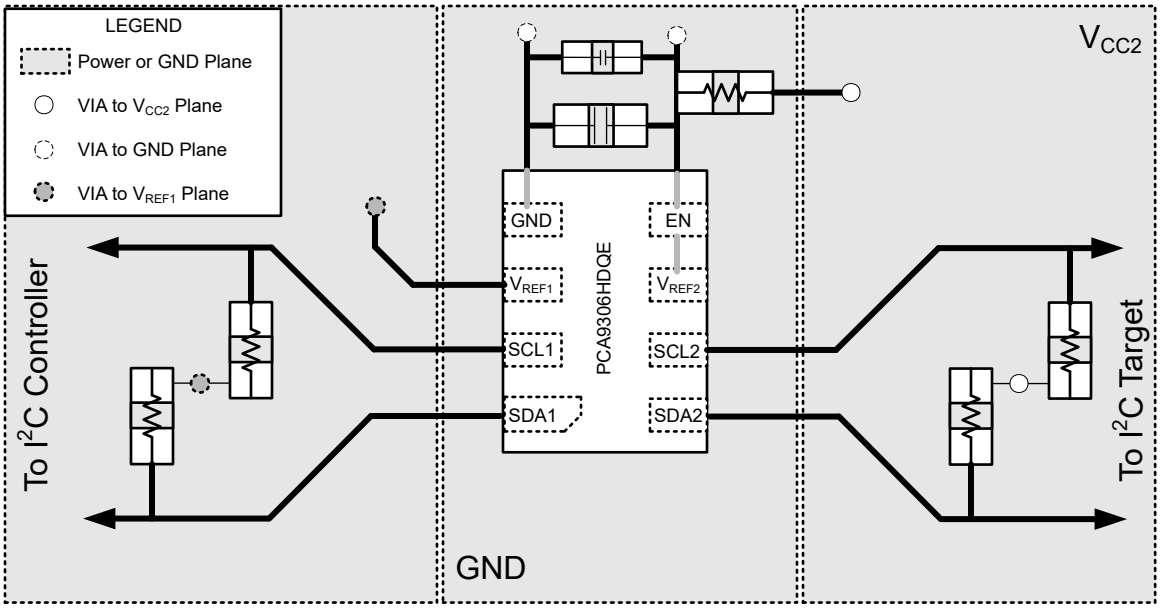


Figure 8-5. PCA9306H Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, select *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9306HDQER	Active	Production	X2SON (DQE) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

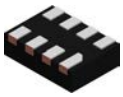
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

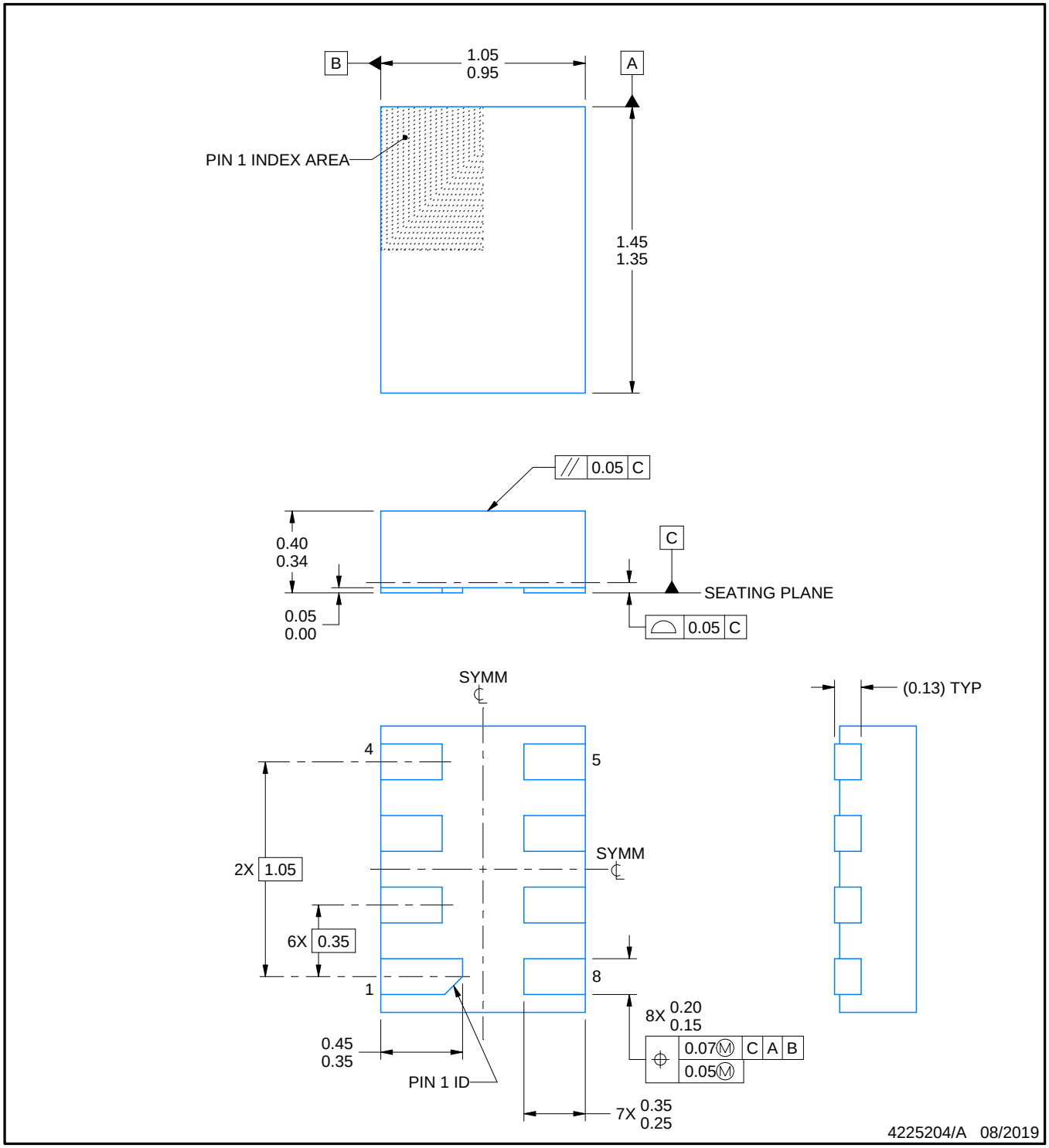
PACKAGE OUTLINE

DQE0008A



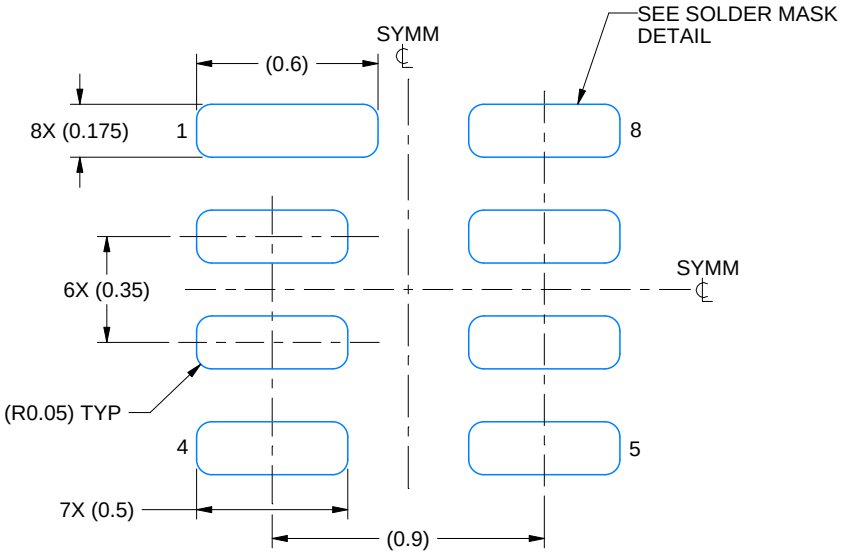
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

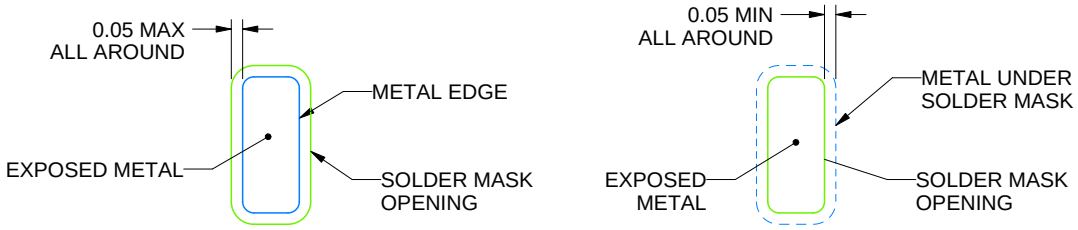


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

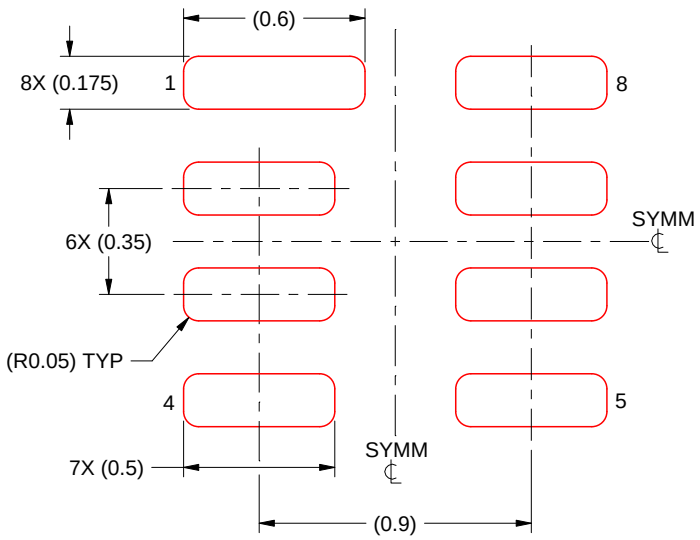


SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025