



## 3.3-V DUAL PLL MULTICLOCK GENERATOR

### FEATURES

- 27-MHz Master Clock Input
- Generated Audio System Clock (PLL1707):
  - SCKO0:  $768 f_S$  ( $f_S = 44.1$  kHz)
  - SCKO1:  $768 f_S$ ,  $512 f_S$  ( $f_S = 48$  kHz)
  - SCKO2:  $256 f_S$  ( $f_S = 32, 44.1, 48, 64, 88.2, 96$  kHz)
  - SCKO3:  $384 f_S$  ( $f_S = 32, 44.1, 48, 64, 88.2, 96$  kHz)
- Generated Audio System Clock (PLL1708):
  - SCKO0:  $768 f_S$  ( $f_S = 44.1$  kHz)
  - SCKO1:  $768 f_S$ ,  $512 f_S$ ,  $384 f_S$ ,  $256 f_S$  ( $f_S = 48$  kHz)
  - SCKO2:  $256 f_S$  ( $f_S = 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, 96$  kHz)
  - SCKO3:  $384 f_S$  ( $f_S = 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, 96$  kHz)
- Zero PPM Error Output Clocks
- Low Clock Jitter: 50 ps (Typical)
- Multiple Sampling Frequencies (PLL1707):
  - $f_S = 32, 44.1, 48, 64, 88.2, 96$  kHz
- Multiple Sampling Frequencies (PLL1708):
  - $f_S = 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, 96$  kHz
- 3.3-V Single Power Supply
- PLL1707: Parallel Control  
PLL1708: Serial Control
- Package: 20-Pin SSOP (150 mil), Lead-Free Product

### APPLICATIONS

- HDD + DVD Recorders
- DVD Recorders
- HDD Recorders
- DVD Players
- DVD Add-On Cards for Multimedia PCs
- Digital HDTV Systems
- Set-Top Boxes

### DESCRIPTION

The PLL1707<sup>†</sup> and PLL1708<sup>†</sup> are low cost, phase-locked loop (PLL) multiclock generators. The PLL1707 and PLL1708 can generate four system clocks from a 27-MHz reference input frequency. The clock outputs of the PLL1707 can be controlled by sampling frequency-control pins and those of the PLL1708 can be controlled through serial-mode control pins. The device gives customers both cost and space savings by eliminating external components and enables customers to achieve the very low-jitter performance needed for high performance audio DACs and/or ADCs. The PLL1707 and PLL1708 are ideal for MPEG-2 applications which use a 27-MHz master clock such as DVD recorders, HDD recorders, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

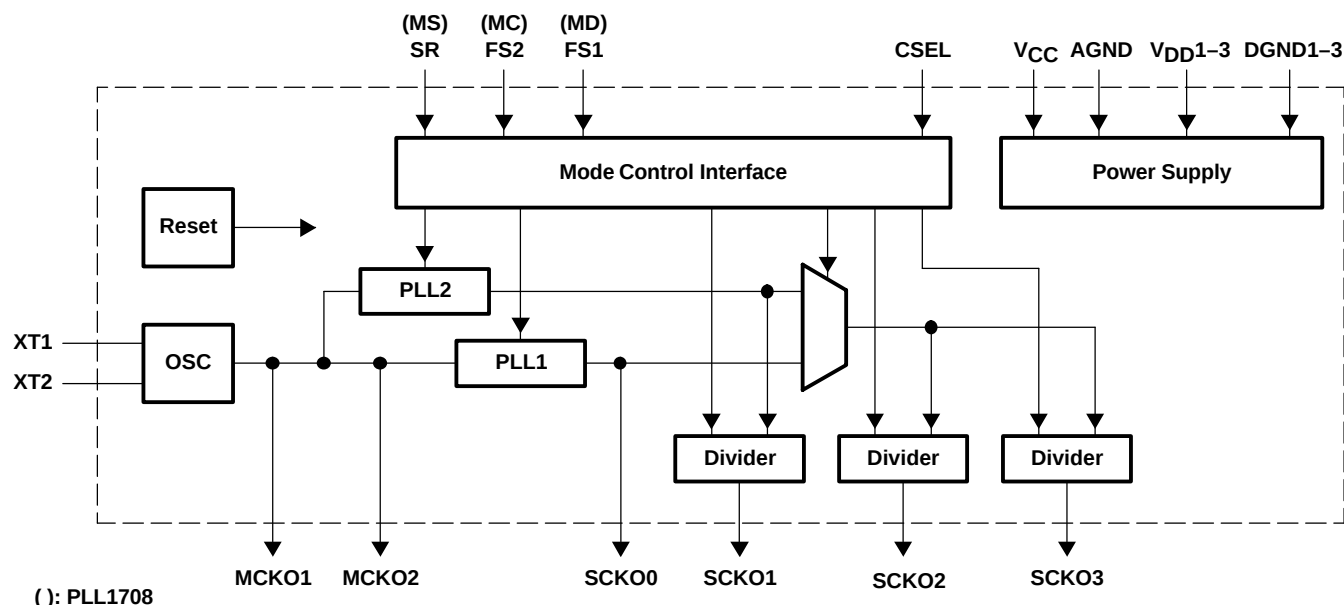
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

<sup>†</sup>The PLL1707 and PLL1708 use the same die and they are electrically identical except for mode control.

## FUNCTIONAL BLOCK DIAGRAM



## PACKAGE/ORDERING INFORMATION

| PRODUCT    | PACKAGE | PACKAGE CODE | OPERATION TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|------------|---------|--------------|-----------------------------|-----------------|-----------------|-----------------|
| PLL1707DBQ | SSOP 20 | 20DBQ        | –25°C to 85°C               | PLL1707         | PLL1707DBQ      | Tube            |
|            |         |              |                             |                 | PLL1707DBQR     | Tape and reel   |
| PLL1708DBQ | SSOP 20 | 20DBQ        | –25°C to 85°C               | PLL1708         | PLL1708DBQ      | Tube            |
|            |         |              |                             |                 | PLL1708DBQR     | Tape and reel   |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

|                                                              | PLL1705 AND PLL1706            |
|--------------------------------------------------------------|--------------------------------|
| Supply voltage: $V_{CC}$ , $V_{DD1}$ – $V_{DD3}$             | 4 V                            |
| Supply voltage differences: $V_{CC}$ , $V_{DD1}$ – $V_{DD3}$ | ±0.1 V                         |
| Ground voltage differences: AGND, DGND1–DGND3                | ±0.1 V                         |
| Digital input voltage: FS1 (MD), FS2 (MC), SR (MS), CSEL     | –0.3 V to ( $V_{DD} + 0.3$ ) V |
| Analog input voltage, XT1, XT2                               | –0.3 V to ( $V_{CC} + 0.3$ ) V |
| Input current (any pins except supplies)                     | ±10 mA                         |
| Ambient temperature under bias                               | –40°C to 125°C                 |
| Storage temperature                                          | –55°C to 150°C                 |
| Junction temperature                                         | 150°C                          |
| Lead temperature (soldering)                                 | 260°C, 5 s                     |
| Package temperature (IR reflow, peak)                        | 260°C                          |

<sup>(1)</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

all specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1}-V_{DD3} (= V_{DD}) = V_{CC} = 3.3\text{ V}$ ,  $f_M = 27\text{ MHz}$ , crystal oscillation,  $f_S = 48\text{ kHz}$  (unless otherwise noted)

| PARAMETER                                                                                                                                                 |                               |         | TEST CONDITIONS                   |  | MIN                     | TYP    | MAX    | UNIT |    |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|---------|-----------------------------------|--|-------------------------|--------|--------|------|----|
| DIGITAL INPUT/OUTPUT                                                                                                                                      |                               |         |                                   |  |                         |        |        |      |    |
| Logic input                                                                                                                                               |                               |         |                                   |  | CMOS compatible         |        |        |      |    |
| V <sub>IH</sub> <sup>(1)</sup>                                                                                                                            | Input logic level             |         |                                   |  | 0.7V <sub>DD</sub>      |        | 3.6    | Vdc  |    |
| V <sub>IL</sub> <sup>(1)</sup>                                                                                                                            |                               |         |                                   |  | 0.3 V <sub>DD</sub>     |        |        |      |    |
| I <sub>IH</sub> <sup>(1)</sup>                                                                                                                            | Input logic current           |         | V <sub>IN</sub> = V <sub>DD</sub> |  | 65                      |        | 100    | μA   |    |
| I <sub>IL</sub> <sup>(1)</sup>                                                                                                                            |                               |         | V <sub>IN</sub> = 0 V             |  | ±10                     |        |        |      |    |
| Logic output                                                                                                                                              |                               |         |                                   |  | CMOS                    |        |        |      |    |
| V <sub>OH</sub> <sup>(2)</sup>                                                                                                                            | Output logic level            |         | I <sub>OH</sub> = −4 mA           |  | V <sub>DD</sub> − 0.4 V |        |        | Vdc  |    |
| V <sub>OL</sub> <sup>(2)</sup>                                                                                                                            |                               |         | I <sub>OL</sub> = 4 mA            |  | 0.4                     |        |        | Vdc  |    |
| Sampling frequency                                                                                                                                        |                               | PLL1707 | Standard f <sub>S</sub>           |  | 32                      | 44.1   | 48     | kHz  |    |
|                                                                                                                                                           |                               |         | Double f <sub>S</sub>             |  | 64                      | 88.2   | 96     |      |    |
|                                                                                                                                                           |                               | PLL1708 | Half f <sub>S</sub>               |  | 16                      | 22.05  | 24     |      |    |
|                                                                                                                                                           |                               |         | Standard f <sub>S</sub>           |  | 32                      | 44.1   | 48     |      |    |
|                                                                                                                                                           |                               |         | Double f <sub>S</sub>             |  | 64                      | 88.2   | 96     |      |    |
| MASTER CLOCK (MCKO1, MCKO2) CHARACTERISTICS (f <sub>M</sub> = 27 MHz, C <sub>1</sub> = C <sub>2</sub> = 15 pF, C <sub>L</sub> = 20 pF on measurement pin) |                               |         |                                   |  |                         |        |        |      |    |
| Master clock frequency                                                                                                                                    |                               |         |                                   |  | 26.73                   | 27     | 27.27  | MHz  |    |
| V <sub>IH</sub>                                                                                                                                           | Input level(3)                |         |                                   |  | 0.7 V <sub>CC</sub>     |        |        | V    |    |
| V <sub>IL</sub>                                                                                                                                           |                               |         |                                   |  | 0.3 V <sub>CC</sub>     |        |        |      |    |
| I <sub>IH</sub>                                                                                                                                           | Input current(3)              |         | V <sub>IN</sub> = V <sub>CC</sub> |  | ±10                     |        |        | μA   |    |
| I <sub>IL</sub>                                                                                                                                           |                               |         | V <sub>IN</sub> = 0 V             |  | ±10                     |        |        |      |    |
| Output voltage <sup>(4)</sup>                                                                                                                             |                               |         |                                   |  | 3.5                     |        |        | Vp-p |    |
| Output rise time                                                                                                                                          |                               |         | 20% to 80% of V <sub>DD</sub>     |  | 2.0                     |        |        | ns   |    |
| Output fall time                                                                                                                                          |                               |         | 80% to 20% of V <sub>DD</sub>     |  | 2.0                     |        |        | ns   |    |
| Duty cycle                                                                                                                                                |                               |         | For crystal oscillation           |  | 45%                     | 51%    | 55%    |      |    |
|                                                                                                                                                           |                               |         | For external clock                |  | 50%                     |        |        |      |    |
| Clock jitter <sup>(5)</sup>                                                                                                                               |                               |         |                                   |  | 50                      |        |        | ps   |    |
| Power-up time <sup>(6)</sup>                                                                                                                              |                               |         |                                   |  | 0.5                     |        |        | 1.5  | ms |
| PLL AC CHARACTERISTICS (SCKO0–SCKO3) (f <sub>M</sub> = 27 MHz, C <sub>L</sub> = 20 pF on measurement pin)                                                 |                               |         |                                   |  |                         |        |        |      |    |
| SCKO0                                                                                                                                                     | Output system clock frequency | PLL1707 | Fixed                             |  | 33.8688                 |        |        | MHz  |    |
| SCKO1                                                                                                                                                     |                               |         | Selectable for 48 kHz             |  | 24.576                  |        | 36.864 |      |    |
| SCKO2                                                                                                                                                     |                               |         | 256 f <sub>S</sub>                |  | 8.192                   | 12.288 | 24.576 |      |    |
| SCKO3                                                                                                                                                     |                               |         | 384 f <sub>S</sub>                |  | 12.288                  | 18.432 | 36.864 |      |    |
| SCKO0                                                                                                                                                     |                               | PLL1708 | Fixed                             |  | 33.8688                 |        |        |      |    |
| SCKO1                                                                                                                                                     |                               |         | Selectable for 48 kHz             |  | 12.288                  | 24.576 | 36.864 |      |    |
| SCKO2                                                                                                                                                     |                               |         | 256 f <sub>S</sub>                |  | 4.096                   | 12.288 | 24.576 |      |    |
| SCKO3                                                                                                                                                     |                               |         | 384 f <sub>S</sub>                |  | 6.144                   | 18.432 | 36.864 |      |    |
| Output rise time                                                                                                                                          |                               |         | 20% to 80% of V <sub>DD</sub>     |  | 2.0                     |        |        | ns   |    |
| Output fall time                                                                                                                                          |                               |         | 80% to 20% of V <sub>DD</sub>     |  | 2.0                     |        |        | ns   |    |
| Output duty cycle                                                                                                                                         |                               |         |                                   |  | 45                      | 50     | 55     | %    |    |

(1) Pins 5, 6, 7, 12: FS1/MD, FS2/MC, SR/MS, CSEL (Schmitt-trigger input with internal pulldown, 3.3-V tolerant)

(2) Pins 2, 3, 14, 15, 18, 19: SCKO2, SCKO3, MCKO1, MCKO2, SCKO0, SCKO1

(3) Pin 10: XT1

(4) Pin 11: XT2

(5) Jitter performance is specified as standard deviation of jitter for 27-MHz crystal oscillation and default SCKO frequency setting. Jitter performance varies with master clock mode, SCKO frequency setting and load capacitance on each clock output.

(6) The delay time from power on to oscillation

(7) The settling time when the sampling frequency is changed

(8) The delay time from power on to lockup

(9)  $f_M = 27\text{-MHz}$  crystal oscillation, no load on MCKO1, MCKO2, SCKO0, SCKO1, SCKO2, SCKO3. Power supply current varies with sampling frequency selection and load condition.

(10) While all bits of CE[6:1] are 0, the PLL1708 goes into power-down mode.

## ELECTRICAL CHARACTERISTICS (continued)

all specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1}-V_{DD3} (= V_{DD}) = V_{CC} = 3.3\text{ V}$ ,  $f_M = 27\text{ MHz}$ , crystal oscillation,  $f_S = 48\text{ kHz}$  (unless otherwise noted)

| PARAMETER                        | TEST CONDITIONS                                          | MIN                                                      | TYP | MAX | UNIT               |
|----------------------------------|----------------------------------------------------------|----------------------------------------------------------|-----|-----|--------------------|
| Output clock jitter (5)          | SCKO0, SCKO1                                             |                                                          | 58  | 100 | ps                 |
|                                  | SCKO2, SCKO3                                             |                                                          | 50  | 100 | ps                 |
| Frequency Settling Time(7)       | PLL1707, to stated output frequency                      |                                                          | 50  | 150 | ns                 |
|                                  | PLL1708, to stated output frequency                      |                                                          | 80  | 300 |                    |
| Power-up time (8)                | To stated output frequency                               |                                                          | 3   | 6   | ms                 |
| <b>POWER SUPPLY REQUIREMENTS</b> |                                                          |                                                          |     |     |                    |
| $V_{CC}, V_{DD}$                 | Supply voltage range                                     |                                                          | 2.7 | 3.3 | 3.6 Vdc            |
| $I_{DD} + I_{CC}$                | Supply current (9)                                       | $V_{DD} = V_{CC} = 3.3\text{ V}$ , $f_S = 48\text{ kHz}$ | 19  | 25  | mA                 |
|                                  | Power down(10)                                           |                                                          | 350 | 550 | $\mu\text{A}$      |
| Power dissipation                | $V_{DD} = V_{CC} = 3.3\text{ V}$ , $f_S = 48\text{ kHz}$ |                                                          | 63  | 90  | mW                 |
| <b>TEMPERATURE RANGE</b>         |                                                          |                                                          |     |     |                    |
|                                  | Operating temperature                                    |                                                          | -25 | 85  | $^\circ\text{C}$   |
| $\theta_{JA}$                    | Thermal resistance                                       | PLL1707/8DBQ: 20-pin SSOP (150 mil)                      | 150 |     | $^\circ\text{C/W}$ |

(1) Pins 5, 6, 7, 12: FS1/MD, FS2/MC, SR/MS, CSEL (Schmitt-trigger input with internal pulldown, 3.3-V tolerant)

(2) Pins 2, 3, 14, 15, 18, 19: SCKO2, SCKO3, MCKO1, MCKO2, SCKO0, SCKO1

(3) Pin 10: XT1

(4) Pin 11: XT2

(5) Jitter performance is specified as standard deviation of jitter for 27-MHz crystal oscillation and default SCKO frequency setting. Jitter performance varies with master clock mode, SCKO frequency setting and load capacitance on each clock output.

(6) The delay time from power on to oscillation

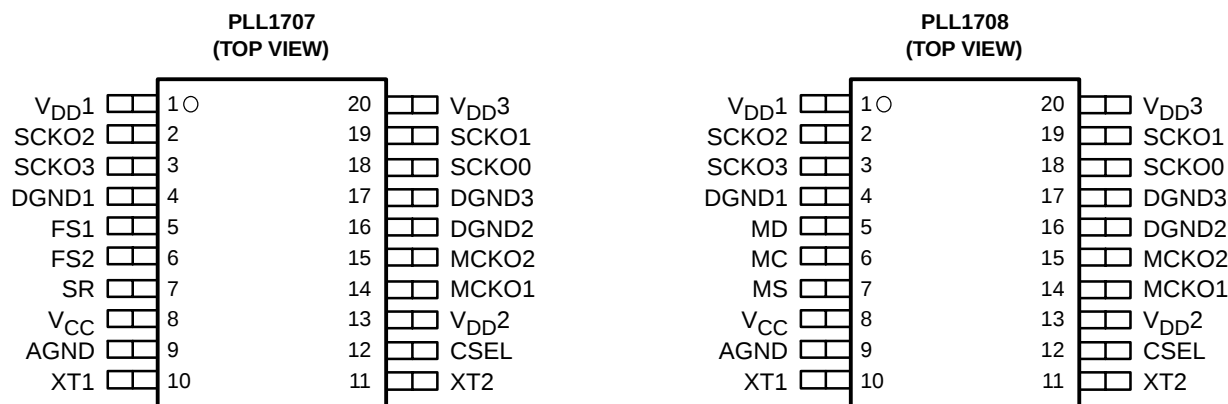
(7) The settling time when the sampling frequency is changed

(8) The delay time from power on to lockup

(9)  $f_M = 27\text{ MHz}$  crystal oscillation, no load on MCKO1, MCKO2, SCKO0, SCKO1, SCKO2, SCKO3. Power supply current varies with sampling frequency selection and load condition.

(10) While all bits of CE[6:1] are 0, the PLL1708 goes into power-down mode.

## PIN ASSIGNMENTS



### PLL1707 Terminal Functions

| TERMINAL<br>NAME | NO. | I/O | DESCRIPTION                                                           |
|------------------|-----|-----|-----------------------------------------------------------------------|
| AGND             | 9   | –   | Analog ground                                                         |
| CSEL             | 12  | I   | SCKO1 frequency selection control <sup>(1)</sup>                      |
| DGND1            | 4   | –   | Digital ground 1                                                      |
| DGND2            | 16  | –   | Digital ground 2                                                      |
| DGND3            | 17  | –   | Digital ground 3                                                      |
| FS1              | 5   | I   | Sampling frequency group control 1 <sup>(1)</sup>                     |
| FS2              | 6   | I   | Sampling frequency group control 2 <sup>(1)</sup>                     |
| MCKO1            | 14  | O   | 27-MHz master clock output 1                                          |
| MCKO2            | 15  | O   | 27-MHz master clock output 2                                          |
| SCKO0            | 18  | O   | System clock output 0 (33.8688 MHz fixed)                             |
| SCKO1            | 19  | O   | System clock output 1 (selectable for 48 kHz)                         |
| SCKO2            | 2   | O   | System clock output 2 (256 f <sub>S</sub> selectable)                 |
| SCKO3            | 3   | O   | System clock output 3 (384 f <sub>S</sub> selectable)                 |
| SR               | 7   | I   | Sampling rate control <sup>(1)</sup>                                  |
| V <sub>CC</sub>  | 8   | –   | Analog power supply, 3.3 V                                            |
| V <sub>DD1</sub> | 1   | –   | Digital power supply 1, 3.3 V                                         |
| V <sub>DD2</sub> | 13  | –   | Digital power supply 2, 3.3 V                                         |
| V <sub>DD3</sub> | 20  | –   | Digital power supply 3, 3.3 V                                         |
| XT1              | 10  | I   | 27-MHz crystal oscillator, or external clock input                    |
| XT2              | 11  | O   | 27-MHz crystal oscillator, must be OPEN for external clock input mode |

<sup>(1)</sup> Schmitt-trigger input with internal pulldown.

### PLL1708 Terminal Functions

| TERMINAL<br>NAME | NO. | I/O | DESCRIPTION                                                           |
|------------------|-----|-----|-----------------------------------------------------------------------|
| AGND             | 9   | –   | Analog ground                                                         |
| CSEL             | 12  | I   | SCKO1 frequency selection control <sup>(1)</sup>                      |
| DGND1            | 4   | –   | Digital ground 1                                                      |
| DGND2            | 16  | –   | Digital ground 2                                                      |
| DGND3            | 17  | –   | Digital ground 3                                                      |
| MC               | 6   | I   | Bit clock input for serial control <sup>(1)</sup>                     |
| MCKO1            | 14  | O   | 27-MHz master clock output 1                                          |
| MCKO2            | 15  | O   | 27-MHz master clock output 2                                          |
| MD               | 5   | I   | Data input for serial control <sup>(1)</sup>                          |
| MS               | 7   | I   | Chip select input for serial control <sup>(1)</sup>                   |
| SCKO0            | 18  | O   | System clock output 0 (33.8688 MHz fixed)                             |
| SCKO1            | 19  | O   | System clock output 1 (selectable for 48 kHz)                         |
| SCKO2            | 2   | O   | System clock output 2 (256 f <sub>S</sub> selectable)                 |
| SCKO3            | 3   | O   | System clock output 3 (384 f <sub>S</sub> selectable)                 |
| VCC              | 8   | –   | Analog power supply, 3.3 V                                            |
| VDD1             | 1   | –   | Digital power supply 1, 3.3 V                                         |
| VDD2             | 13  | –   | Digital power supply 2, 3.3 V                                         |
| VDD3             | 20  | –   | Digital power supply 3, 3.3 V                                         |
| XT1              | 10  | I   | 27-MHz crystal oscillator, or external clock input                    |
| XT2              | 11  | O   | 27-MHz crystal oscillator, must be OPEN for external clock input mode |

<sup>(1)</sup> Schmitt-trigger input with internal pulldown.

## TYPICAL PERFORMANCE CURVES

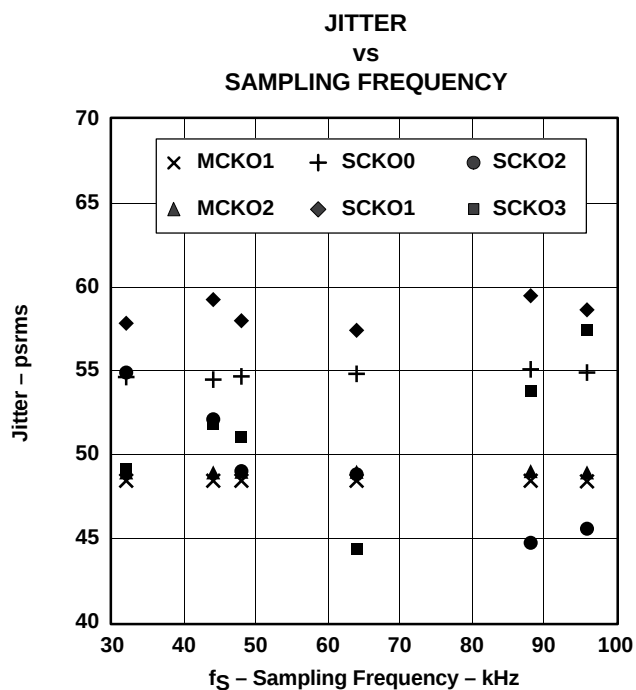


Figure 1

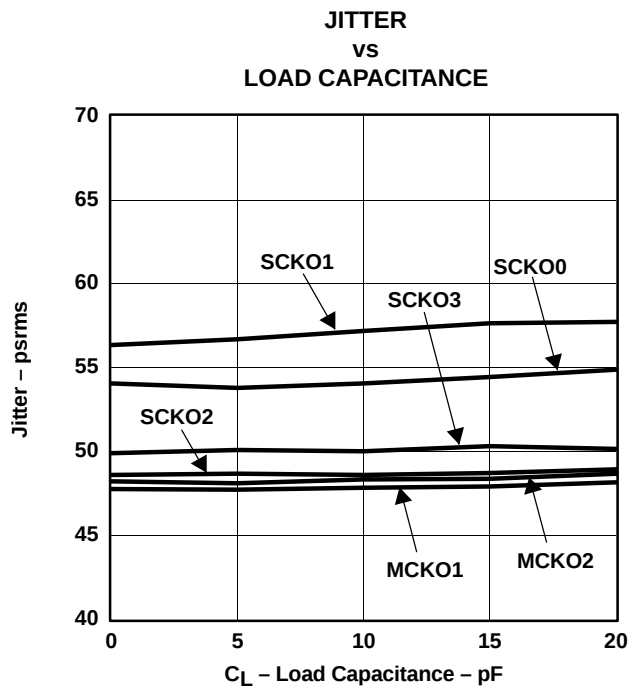


Figure 2

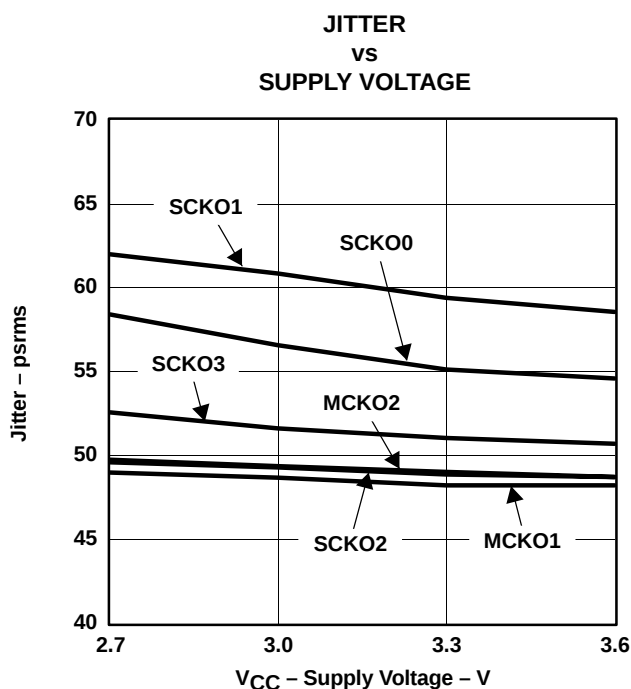


Figure 3

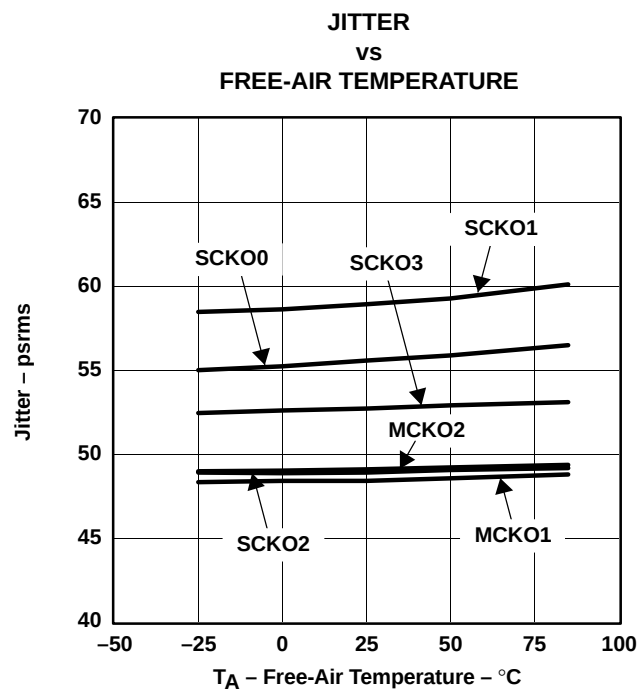
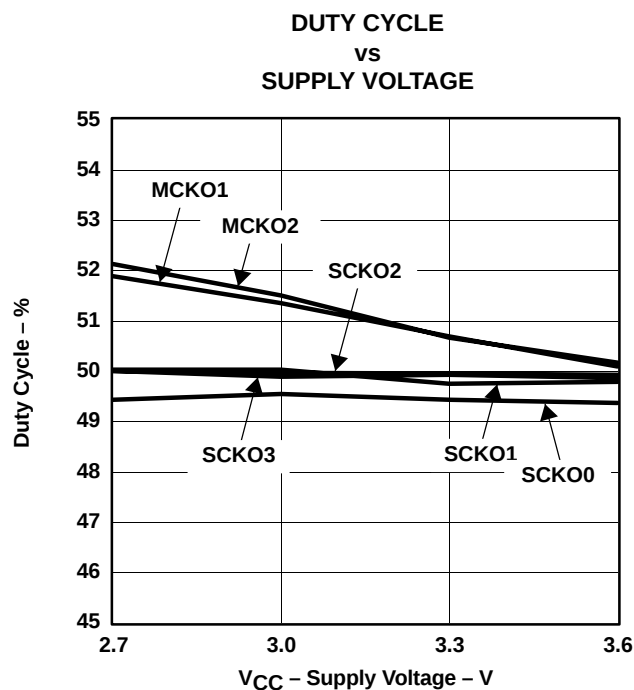
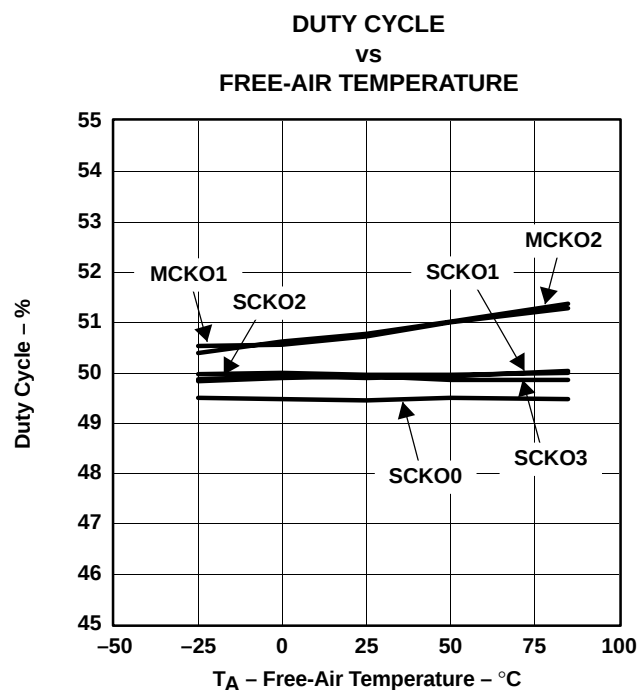


Figure 4

NOTE: All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1-3} (= V_{DD}) = V_{CC} = +3.3\text{ V}$ ,  $f_M = 27\text{ MHz}$ , crystal oscillation,  $C_1, C_2 = 15\text{ pF}$ , default frequency (33.8688 MHz for SCKO0, 36.864 MHz for SCKO1,  $256 f_s$  and  $384 f_s$  of 48 kHz for SCKO2 and SCKO3),  $C_L = 20\text{ pF}$  on measurement pin, unless otherwise noted.



**Figure 5**



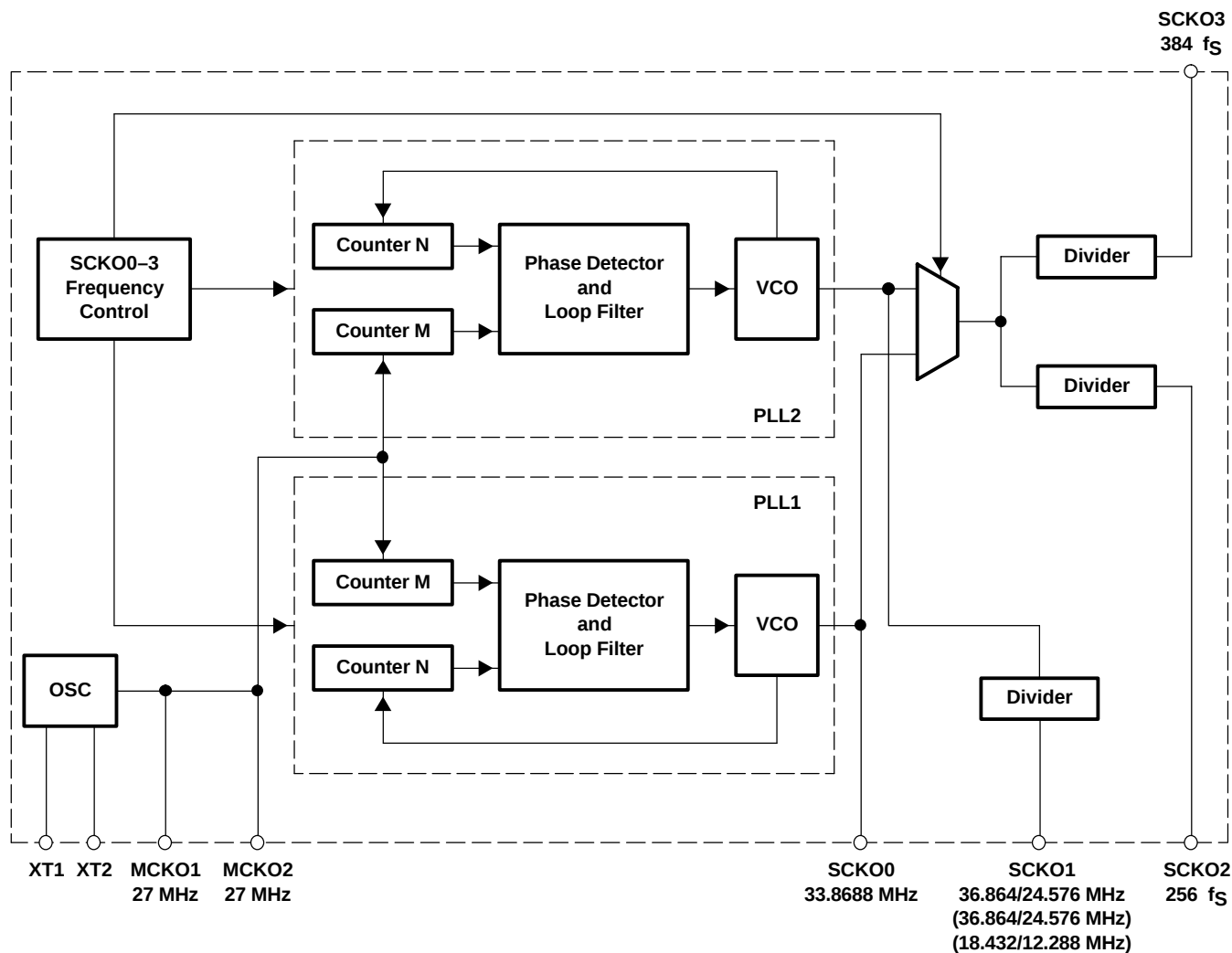
**Figure 6**

NOTE: All specifications at T<sub>A</sub> = 25°C, V<sub>DD1-3</sub> (= V<sub>DD</sub>) = V<sub>CC</sub> = +3.3 V, f<sub>M</sub> = 27 MHz, crystal oscillation, C<sub>1</sub>, C<sub>2</sub> = 15 pF, default frequency (33.8688 MHz for SCKO0, 36.864 MHz for SCKO1, 256 f<sub>S</sub> and 384 f<sub>S</sub> of 48 kHz for SCKO2 and SCKO3), C<sub>L</sub> = 20 pF on measurement pin, unless otherwise noted.

## THEORY OF OPERATION

### MASTER CLOCK AND SYSTEM CLOCK OUTPUT

The PLL1707/8 consists of a dual PLL clock and master clock generator which generates four system clocks and two buffered 27-MHz clocks from a 27-MHz master clock. Figure 7 shows the block diagram of the PLL1707/8. The PLL is designed to accept a 27-MHz master clock.



( ): PLL1708

Figure 7. Block Diagram

The master clock can be either a crystal oscillator placed between XT1 (pin 10) and XT2 (pin 11), or an external input to XT1. If an external master clock is used, XT2 must be open. Figure 8 illustrates possible system clock connection options, and Figure 9 illustrates the 27-MHz master clock timing requirement.

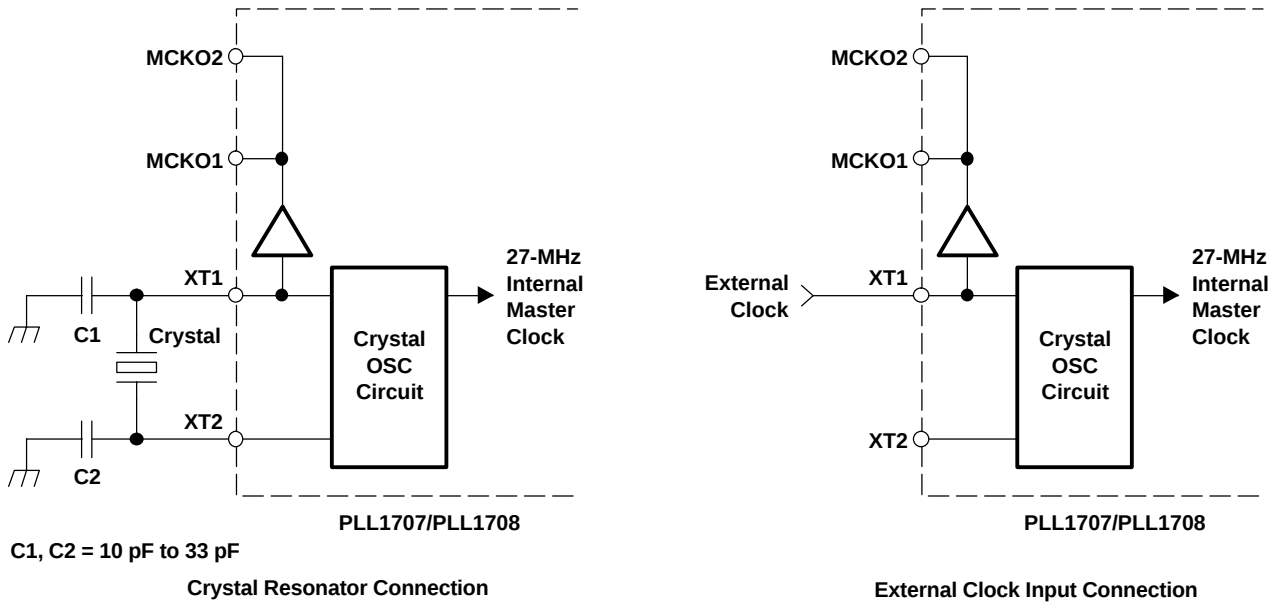
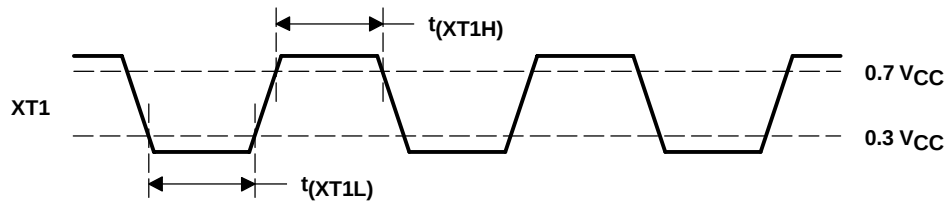


Figure 8. Master Clock Generator Connection Diagram



| DESCRIPTION                      | SYMBOL       | MIN | MAX | UNIT |
|----------------------------------|--------------|-----|-----|------|
| Master clock pulse duration HIGH | $t_{(XT1H)}$ | 10  |     | ns   |
| Master clock pulse duration LOW  | $t_{(XT1L)}$ | 10  |     | ns   |

Figure 9. External Master Clock Timing Requirement

The PLL1707/8 provides a very low-jitter, high-accuracy clock. SCKO0 outputs a fixed 33.8688-MHz clock, SCKO1 outputs  $256 f_S$ ,  $384 f_S$ ,  $512 f_S$ , or  $768 f_S$  ( $f_S = 48$  kHz) which is selected by hardware or software control. The output frequency of the remaining clocks is determined by the sampling frequency ( $f_S$ ) under hardware or software control. SCKO2 and SCKO3 output  $256 f_S$  and  $384 f_S$  system clocks, respectively. Table 2 shows each sampling frequency which can be programmed. The system clock output frequencies for programmed sampling frequencies are shown in Table 3. The half sampling frequencies on SCKO2 and SCKO3 and  $256 f_S$  and  $384 f_S$  on SCKO1 are supported only on the PLL1708.

Table 1. Generated System Clock SCKO1 Frequency

| $f_S$             | SCKO1 FREQUENCY |
|-------------------|-----------------|
| $256 f_S^\dagger$ | 12.288 MHz      |
| $384 f_S^\dagger$ | 18.432 MHz      |
| $512 f_S$         | 24.576 MHz      |
| $768 f_S$         | 36.864 MHz      |

$^\dagger$  PLL1708 only

Table 2. Sampling Frequencies

| SAMPLING RATE                          | SAMPLING FREQUENCY (kHz) |       |    |
|----------------------------------------|--------------------------|-------|----|
| Half sampling frequencies <sup>†</sup> | 16                       | 22.05 | 24 |
| Standard sampling frequencies          | 32                       | 44.1  | 48 |
| Double sampling frequencies            | 64                       | 88.2  | 96 |

<sup>†</sup> PLL1708 only

Table 3. Sampling Frequencies and System Clock Output Frequencies

| SAMPLING FREQUENCY (kHz) | SAMPLING RATE | 256 f <sub>S</sub><br>SCKO2 (MHZ) | 384 f <sub>S</sub><br>SCKO3 (MHZ) |
|--------------------------|---------------|-----------------------------------|-----------------------------------|
| 16 <sup>†</sup>          | Half          | 4.096                             | 6.144                             |
| 22.05 <sup>†</sup>       | Half          | 5.6448                            | 8.4672                            |
| 24 <sup>†</sup>          | Half          | 6.144                             | 9.216                             |
| 32                       | Standard      | 8.192                             | 12.288                            |
| 44.1                     | Standard      | 11.2896                           | 16.9344                           |
| 48                       | Standard      | 12.288                            | 18.432                            |
| 64                       | Double        | 16.384                            | 24.576                            |
| 88.2                     | Double        | 22.5792                           | 33.8688                           |
| 96                       | Double        | 24.576                            | 36.864                            |

<sup>†</sup> PLL1708 only

Response time from power on (or applying the clock to XT1) to SCKO settling time is typically 3 ms. Delay time from sampling frequency change to SCKO settling is 300 ns maximum. Figure 10 illustrates SCKO transient timing in the PLL1708.

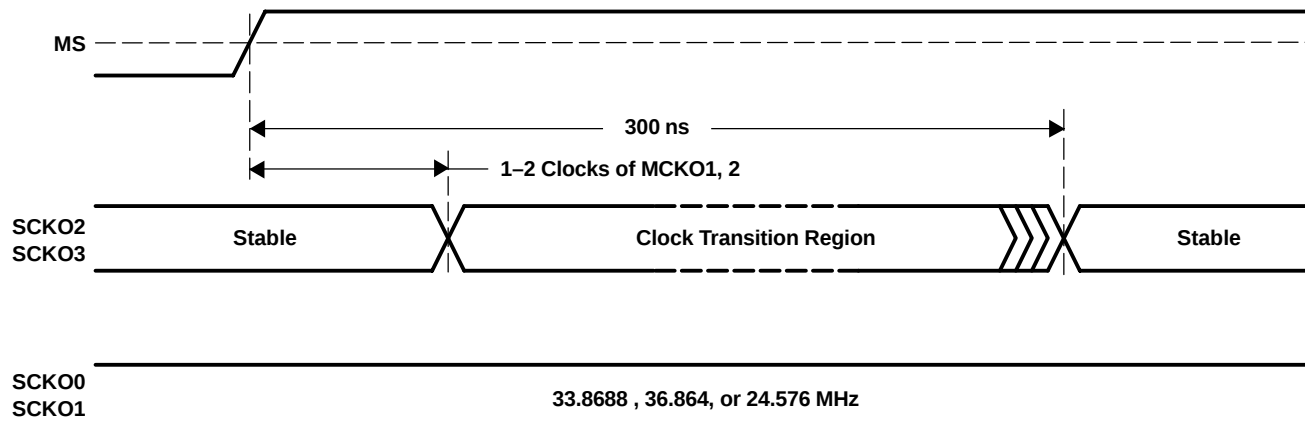


Figure 10. System Clock Transient Timing

The delay time for hardware control to use SR, FS2, FS1, or CSEL is 150 ns maximum. Figure 11 illustrates SCKO transient timing in the PLL1707. Clock transient timing is not synchronized with the SCKOs. External buffers are recommended on all output clocks in order to avoid degrading the jitter performance of the PLL1707/8.

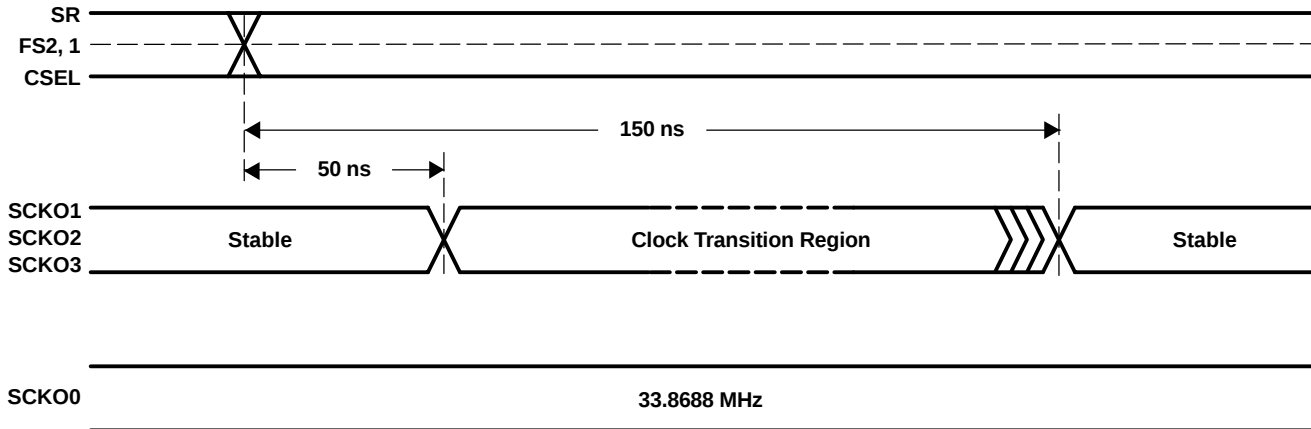


Figure 11. SCKO Transient Timing

## POWER-ON RESET

The PLL1707/8 has an internal power-on reset circuit. The mode register of the PLL1708 is initialized with default settings by power-on reset. Throughout the reset period, all clock outputs are enabled with the default settings after power-up time. Initialization by internal power-on reset is done automatically during 1024 master clocks at  $V_{DD} > 2.0$  V (TYP). Power-on reset timing is shown in Figure 12.

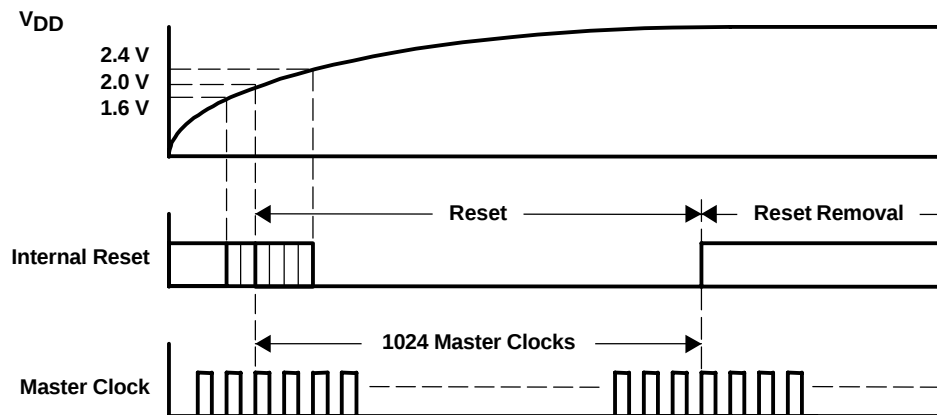


Figure 12. Power-On Reset Timing

## FUNCTION CONTROL

The built-in functions of the PLL1707 can be controlled in the parallel mode (hardware mode), which uses SR (pin 7), FS1 (pin 5) and FS2 (pin 6). The PLL1708 can be controlled in the serial mode (software mode), which has a three-wire interface using MS (pin 7), MC (pin 6), and MD (pin 5). The selectable functions are shown in Table 4.

**Table 4. Selectable Functions**

| SELECTABLE FUNCTION                                  | PARALLEL MODE | SERIAL MODE |
|------------------------------------------------------|---------------|-------------|
| Sampling frequency select (32 kHz, 44.1 kHz, 48 kHz) | Yes           | Yes         |
| Sampling rate select (standard/double)               | Yes           | Yes         |
| Sampling rate select (half)                          | No            | Yes         |
| Each clock output enable/disable                     | No            | Yes         |
| Power down                                           | No            | Yes         |
| SCKO1 configuration                                  | No            | Yes         |

### PLL1707 (Parallel Mode)

In the parallel mode, the following functions can be selected:

#### **Sampling Frequency Group Select**

The sampling frequency group can be selected by FS1 (pin 5) and FS2 (pin 6).

| FS2 (PIN 6) | FS1 (PIN 5) | SAMPLING FREQUENCY |
|-------------|-------------|--------------------|
| LOW         | LOW         | 48 kHz             |
| LOW         | HIGH        | 44.1 kHz           |
| HIGH        | LOW         | 32 kHz             |
| HIGH        | HIGH        | Reserved           |

#### **Sampling Rate Select**

The sampling rate can be selected by SR (pin 7)

| SR (PIN 7) | SAMPLING RATE |
|------------|---------------|
| LOW        | Standard      |
| HIGH       | Double        |

#### **System Clock SCKO1 Frequency Select**

System clock SCKO1 frequency can be selected by CSEL (pin 12).

| CSEL (PIN 12) | SCKO1 FREQUENCY |
|---------------|-----------------|
| LOW           | 36.864 MHz      |
| HIGH          | 24.576 MHz      |

### PLL1708 (Serial Mode)

The built-in functions of the PLL1708 are shown in Table 5. These functions are controlled using the MS, MC, and MD serial control signals.

**Table 5. Selectable Functions**

| SELECTABLE FUNCTION                                  | DEFAULT                |
|------------------------------------------------------|------------------------|
| Sampling frequency select (32 kHz, 44.1 kHz, 48 kHz) | 48-kHz group           |
| Sampling rate select (half, standard, double)        | Standard               |
| Each clock output enable/disable                     | Enabled                |
| Power down                                           | Disabled               |
| SCKO1 configuration                                  | 36.864 MHz, 24.576 MHz |

## Program-Register Bit Mapping

The built-in functions of the PLL1708 are controlled through a 16-bit program register. This register is loaded using MD, MC and MS. After the 16 data bits are clocked in using the rising edge of MC, MS is used to latch the data into the register. Table 6 shows the bit mapping of the register. The serial mode control format and control data input timing are shown in Figure 13 and Figure 14, respectively.

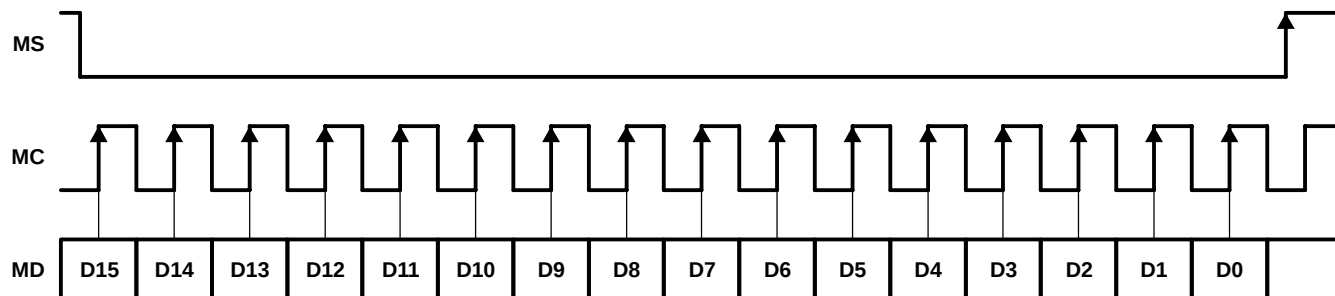
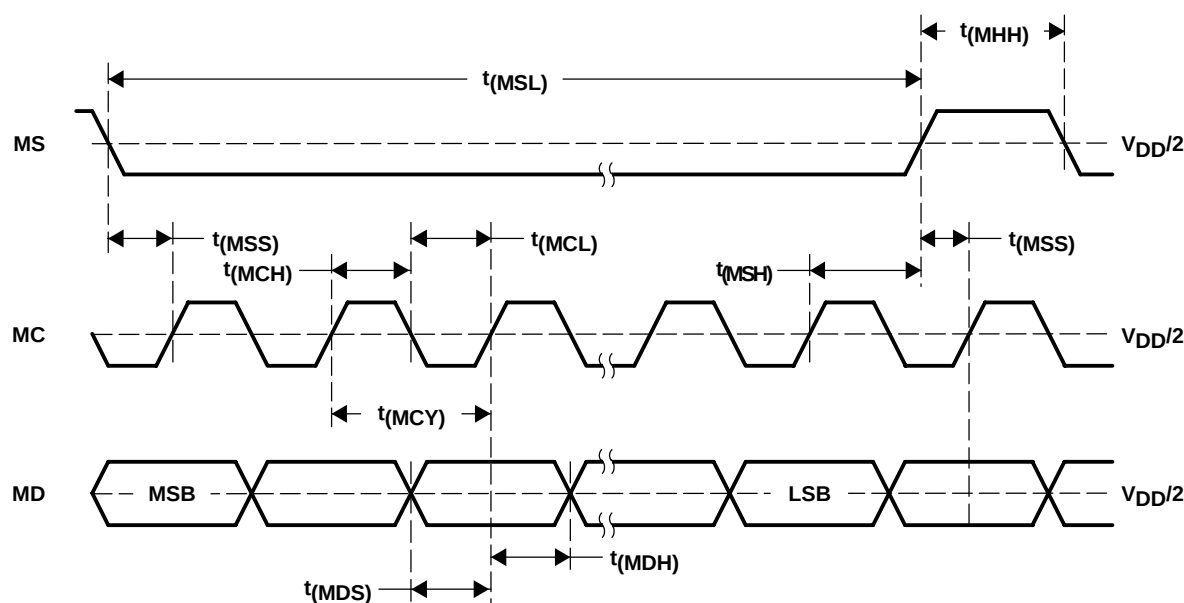


Figure 13. Serial Mode Control Format



| DESCRIPTION                  | SYMBOL   | MIN | TYP | MAX | UNIT                     |
|------------------------------|----------|-----|-----|-----|--------------------------|
| MC pulse cycle time          | $t(MCY)$ | 100 |     |     | ns                       |
| MC pulse duration LOW        | $t(MCL)$ | 40  |     |     | ns                       |
| MC pulse duration HIGH       | $t(MCH)$ | 40  |     |     | ns                       |
| MD hold time                 | $t(MDH)$ | 40  |     |     | ns                       |
| MD setup time                | $t(MDS)$ | 40  |     |     | ns                       |
| MS low-level time            | $t(MSL)$ | 16  |     |     | MC clocks <sup>(1)</sup> |
| MS high-level time           | $t(MHH)$ | 200 |     |     | ns                       |
| MS hold time <sup>(2)</sup>  | $t(MSH)$ | 40  |     |     | ns                       |
| MS setup time <sup>(3)</sup> | $t(MSS)$ | 40  |     |     | ns                       |

(1) MC clocks: MC clock period

(2) MC rising edge for LSB to MS rising edge

(3) MS rising edge to the next MC rising edge. If the MC clock is stopped after the LSB, any MS rise time is accepted.

Figure 14. Control Data Input Timing

## Mode Register

| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 1   | 1   | 1   | 0   | 0   | CE6 | CE5 | CE4 | CE3 | CE2 | CE1 | SR2 | SR1 | FS2 | FS1 |

**Table 6. Mode Register Mapping**

| REGISTER     | BIT NAME | DESCRIPTION                 |
|--------------|----------|-----------------------------|
| Mode control | CE6      | MCKO2 output enable/disable |
|              | CE5      | MCKO1 output enable/disable |
|              | CE4      | SCKO1 output enable/disable |
|              | CE3      | SCKO3 output enable/disable |
|              | CE2      | SCKO2 output enable/disable |
|              | CE1      | SCKO0 output enable/disable |
|              | SR[2:1]  | Sampling rate select        |
|              | FS[2:1]  | Sampling frequency select   |

FS[2:1]: Sampling Frequency Group Select

| FS2 | FS1 | SAMPLING FREQUENCY |
|-----|-----|--------------------|
| 0   | 0   | 48 kHz (default)   |
| 0   | 1   | 44.1 kHz           |
| 1   | 0   | 32 kHz             |
| 1   | 1   | Reserved           |

SR[2:1]: Sampling Rate Select

| SR2 | SR1 | SAMPLING RATE      |
|-----|-----|--------------------|
| 0   | 0   | Standard (default) |
| 0   | 1   | Double             |
| 1   | 0   | Half               |
| 1   | 1   | Reserved           |

CE [6:1]: Clock Output Control

| CE1–CE6 | CLOCK OUTPUT CONTROL          |
|---------|-------------------------------|
| 0       | Clock output disable          |
| 1       | Clock output enable (default) |

While all the bits of CE [6:1] are 0, the PLL1708 goes into the power-down mode, all dynamic operation including PLLs and the oscillator halts, but serial mode control is enabled for resumption.

## Configuration Register

| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4   | D3  | D2  | D1  | D0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-----|
| 0   | 1   | 1   | 0   | 1   | 1   | RSV | RSV | RSV | RSV | RSV | CFG1 | RSV | RSV | RSV | RSV |

**Table 7. Configuration Register Mapping**

| REGISTER      | BIT NAME | DESCRIPTION         |
|---------------|----------|---------------------|
| Configuration | RSV      | Reserved, must be 0 |
|               | CFG1     | SCKO1 configuration |

CFG1: SCKO1 Configuration Control

| CFG1 | CONFIGURATION 1                            |
|------|--------------------------------------------|
| 0    | 36.864 MHz, 24.576 MHz for SCKO1 (default) |
| 1    | 18.432 MHz, 12.288 MHz for SCKO1           |

The system clock SCKO1 frequency can be selected by CSEL (pin 12) and CFG1 (register).

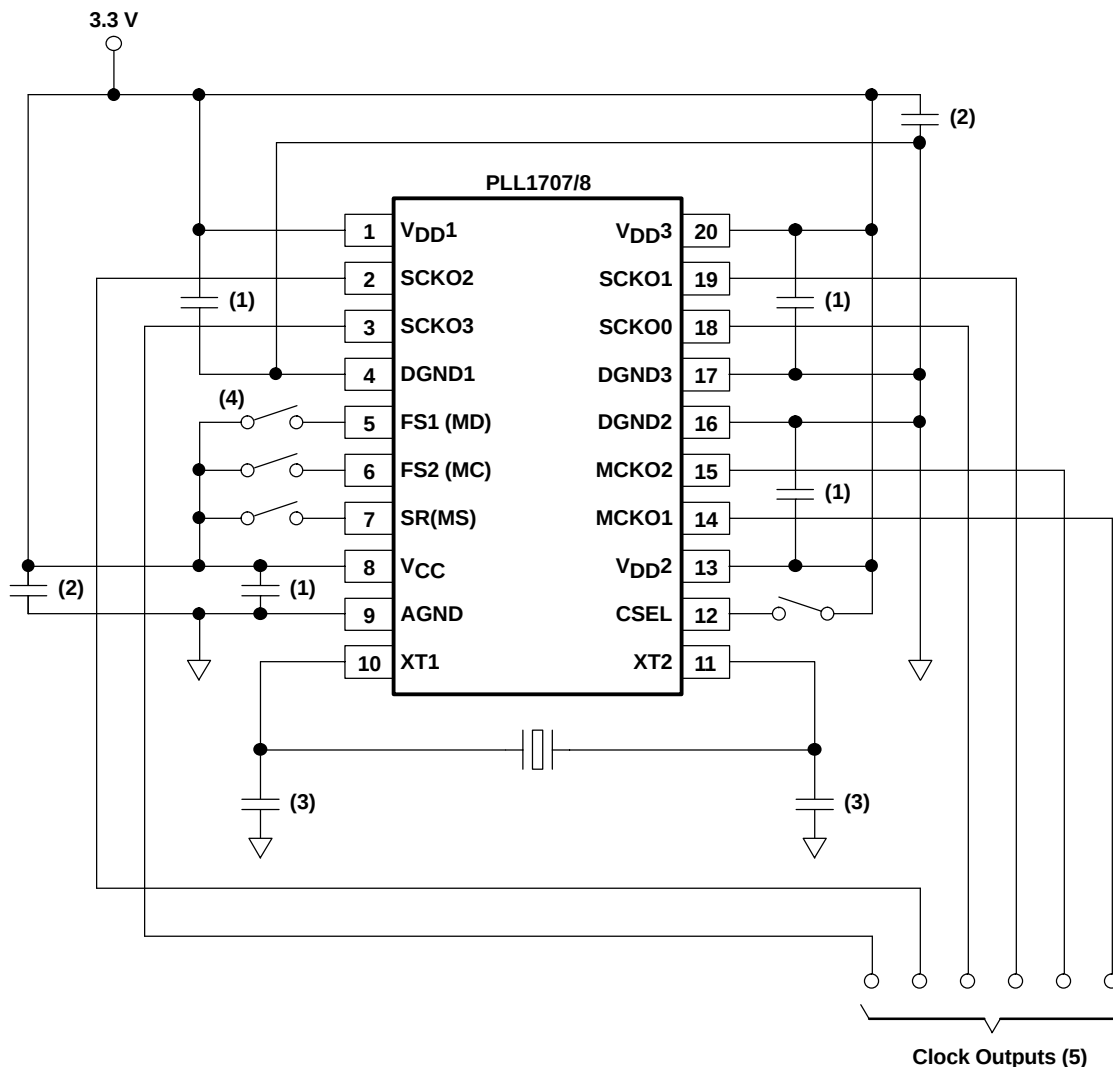
| CFG1<br>(REGISTER) | CSEL<br>(PIN 12) | SCKO1      |
|--------------------|------------------|------------|
| 0                  | LOW              | 36.864 MHz |
| 0                  | HIGH             | 24.576 MHz |
| 1                  | LOW              | 18.432 MHz |
| 1                  | HIGH             | 12.288 MHz |

## CONNECTION DIAGRAM

Figure 15 shows the typical connection circuit for the PLL1707. There are four grounds for digital and analog power supplies. However, the use of one common ground connection is recommended to avoid latch-up or other power-supply-related troubles. Power supplies should be bypassed as close as possible to the device.

## MPEG-2 APPLICATIONS

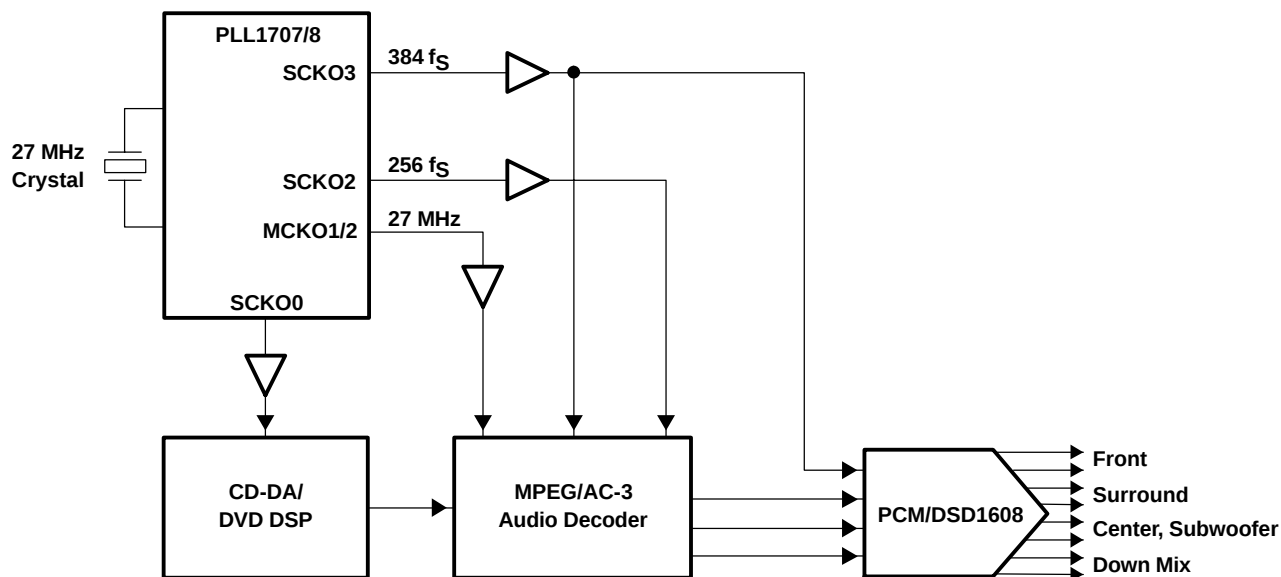
Typical applications for the PLL1707/8 are MPEG-2 based systems such as DVD recorders, HDD recorders, DVD players, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes. The PLL1707/8 provides audio system clocks for a CD-DA DSP, DVD DSP, Karaoke DSP, ADC(s), and DAC(s) from a 27-MHz video clock.



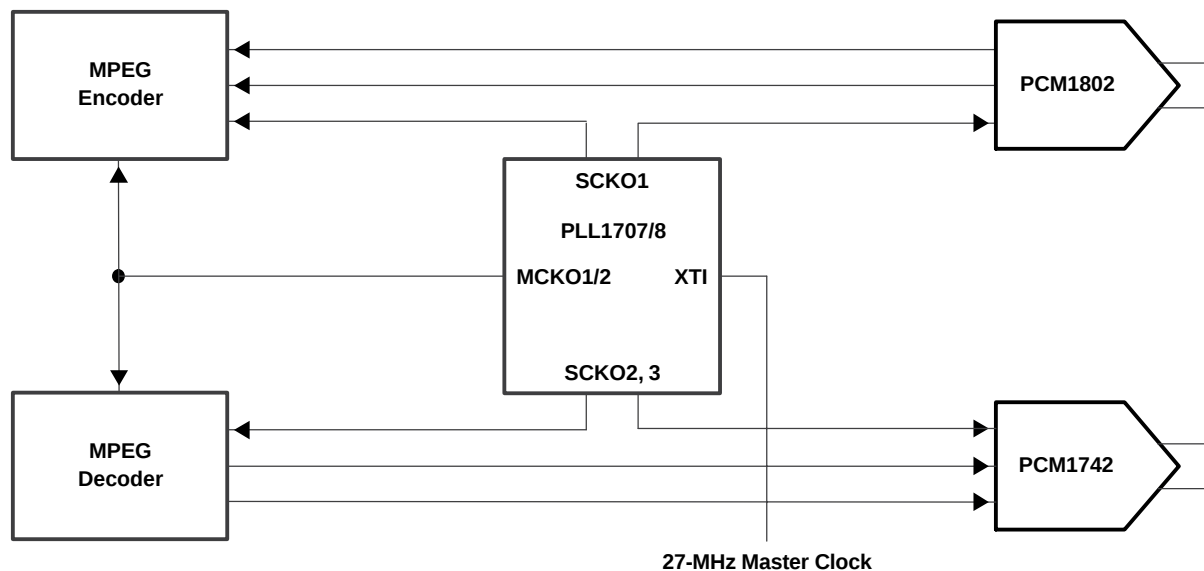
- (1) 0.1-μF ceramic capacitor typical, depending on quality of power supply and pattern layout
- (2) 10-μF aluminum electrolytic capacitor typical, depending on quality of power supply and pattern layout
- (3) 27-MHz quartz crystal and 10–33 pF × 2 ceramic capacitors, which generate the appropriate amplitude of oscillation on XT1/XT2
- (4) This connection is for PLL1707 (parallel mode); when PLL1708 (serial mode) is to be used, control pins must be connected to serial interfaced controller.
- (5) For good jitter performance, minimize the load capacitance on the clock output. It is recommended to drive the clock outputs through buffers, especially if there are heavy loads on SCKO0 and SCKO1, and to minimize mutual interference by separating them or inserting a guard pattern between them.

Figure 15. Typical Connection Diagram

## BLOCK DIAGRAM OF DVD PLAYER APPLICATION



## BLOCK DIAGRAM OF HDD+DVD RECORDER APPLICATION



## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">PLL1707DBQ</a>  | Active        | Production           | SSOP (DBQ)   20 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1707             |
| PLL1707DBQ.B                | Active        | Production           | SSOP (DBQ)   20 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1707             |
| <a href="#">PLL1707DBQR</a> | Active        | Production           | SSOP (DBQ)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1707             |
| PLL1707DBQR.B               | Active        | Production           | SSOP (DBQ)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1707             |
| <a href="#">PLL1708DBQ</a>  | Active        | Production           | SSOP (DBQ)   20 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1708             |
| PLL1708DBQ.B                | Active        | Production           | SSOP (DBQ)   20 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1708             |
| PLL1708DBQG4                | Active        | Production           | SSOP (DBQ)   20 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1708             |
| PLL1708DBQG4.B              | Active        | Production           | SSOP (DBQ)   20 | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1708             |
| <a href="#">PLL1708DBQR</a> | Active        | Production           | SSOP (DBQ)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1708             |
| PLL1708DBQR.B               | Active        | Production           | SSOP (DBQ)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1708             |
| PLL1708DBQRG4               | Active        | Production           | SSOP (DBQ)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85    | PLL1708             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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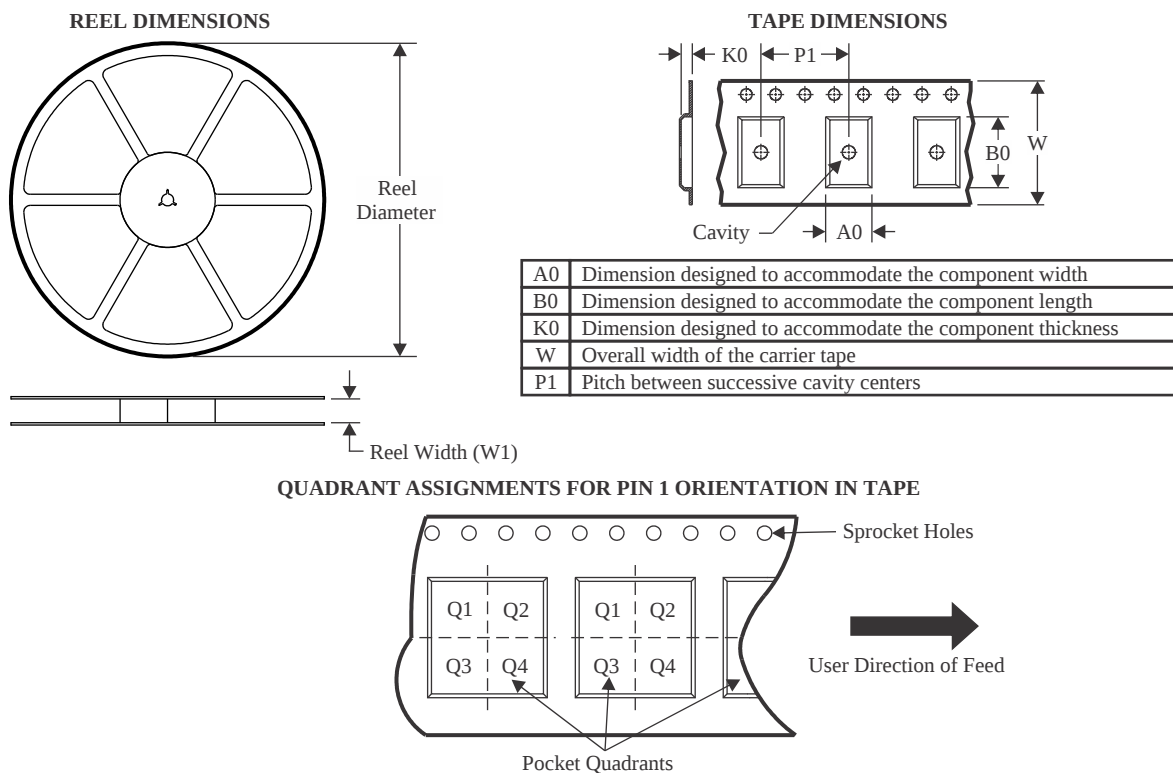
**OTHER QUALIFIED VERSIONS OF PLL1707 :**

- Automotive : [PLL1707-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

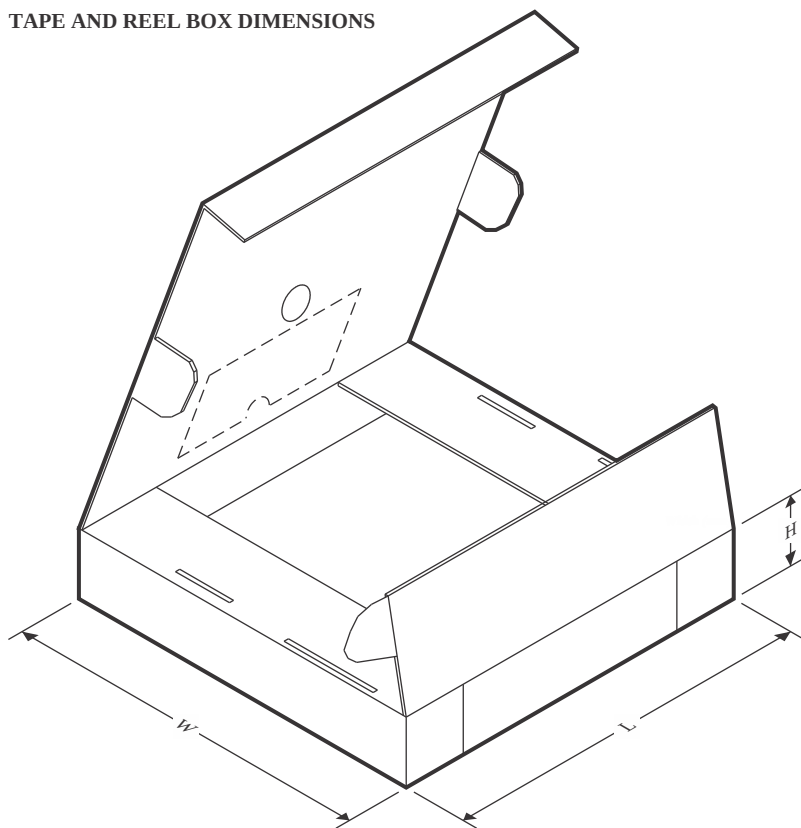
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PLL1707DBQR | SSOP         | DBQ             | 20   | 2000 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| PLL1708DBQR | SSOP         | DBQ             | 20   | 2000 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PLL1707DBQR | SSOP         | DBQ             | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| PLL1708DBQR | SSOP         | DBQ             | 20   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE

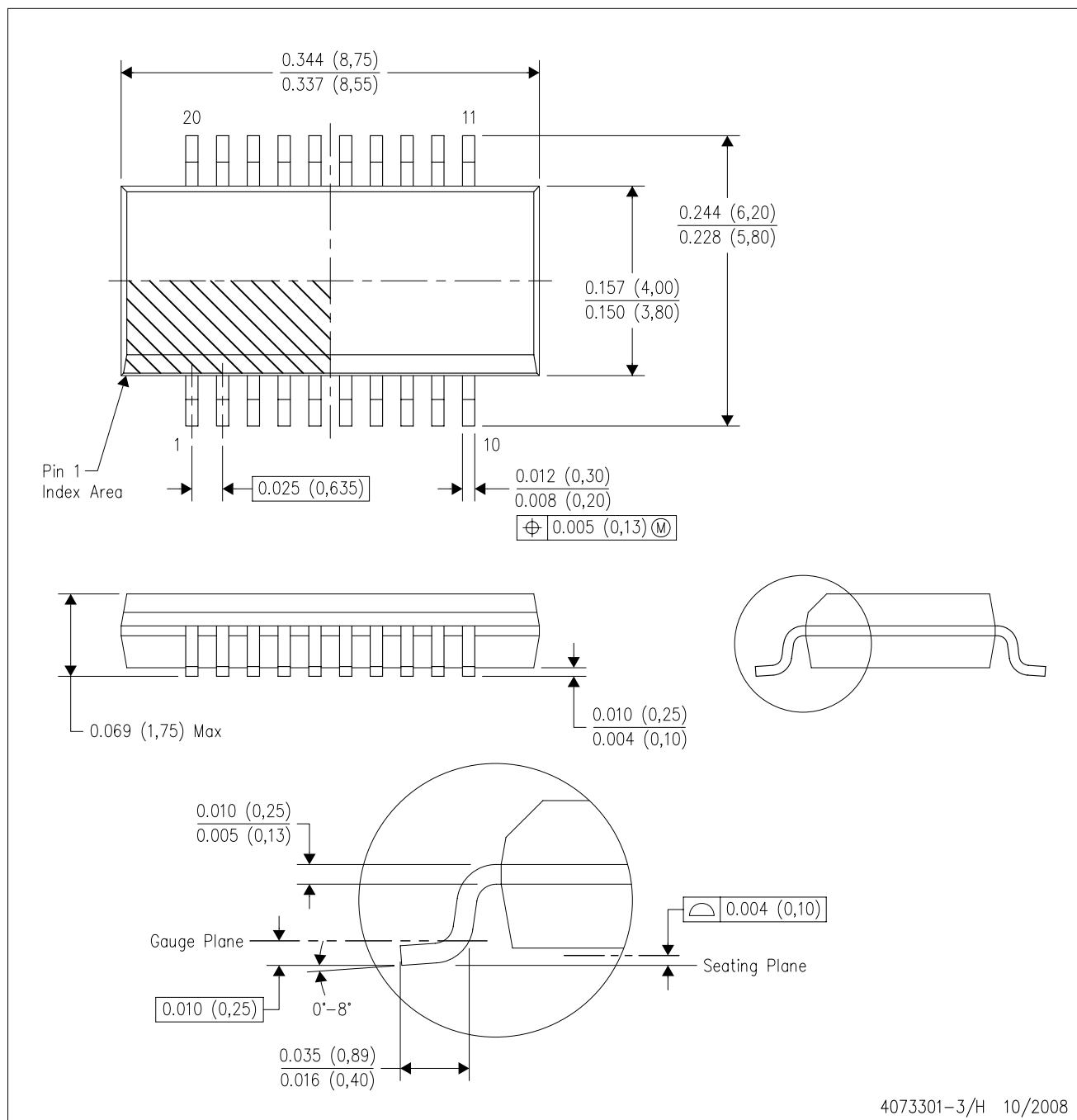


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| PLL1707DBQ     | DBQ          | SSOP         | 20   | 50  | 506.6  | 8      | 3940   | 4.32   |
| PLL1707DBQ.B   | DBQ          | SSOP         | 20   | 50  | 506.6  | 8      | 3940   | 4.32   |
| PLL1708DBQ     | DBQ          | SSOP         | 20   | 50  | 506.6  | 8      | 3940   | 4.32   |
| PLL1708DBQ.B   | DBQ          | SSOP         | 20   | 50  | 506.6  | 8      | 3940   | 4.32   |
| PLL1708DBQG4   | DBQ          | SSOP         | 20   | 50  | 506.6  | 8      | 3940   | 4.32   |
| PLL1708DBQG4.B | DBQ          | SSOP         | 20   | 50  | 506.6  | 8      | 3940   | 4.32   |

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4073301-3/H 10/2008

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AD.

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