30-A, 5-V INPUT, NON-ISOLATED, WIDE OUTPUT ADJUST, POWER MODULE w/ TURBOTRANS™ POLA™

FEATURES

- Up to 30-A Output Current
- 4.5-V to 5.5-V Input Voltage
- Wide-Output Voltage Adjust (0.7 V to 3.6 V)
- Efficiencies up to 96%
- ±1.5% Total Output Voltage Variation
- On/Off Inhibit
- Differential Output Voltage Remote Sense
- Adjustable Undervoltage Lockout
- Output Overcurrent Protection (Nonlatching, Auto-Reset)
- Operating Temperature: –40°C to 85°C
- POLA™ Compatible
- TurboTrans™ Technology
- Designed to meet Ultra-Fast Transient Requirements up to 300 A/μs
- Auto-Track™ Sequencing
- Multi-Phase, Switch-Mode Topology
- Safety Agency Approvals:
  - UL/IEC/CSA-22.2 60950-1

APPLICATIONS

- Complex Multi-Voltage Systems
- Microprocessors
- Bus Drivers

DESCRIPTION

The PTH05T210W is a high-performance 30-A rated, non-isolated power module which utilizes a multi-phase, switch-mode topology. This module represents the 2nd generation of the PTH series power modules which includes a reduced footprint and improved features.

Operating from an input voltage range of 4.5 V to 5.5 V, the PTH05T210W requires a single resistor to set the output voltage to any value over the range, 0.7 V to 3.6 V. The module uses double-sided surface mount construction to provide a low profile and compact footprint. Package options include both through-hole and surface mount configurations that are lead (Pb) – free and RoHS compatible.

A new feature included in this 2nd generation of PTH modules is TurboTrans™ technology (patent pending). TurboTrans allows the transient response of the regulator to be optimized externally, resulting in a reduction of output voltage deviation following a load transient and a reduction in required output capacitance. This feature also offers enhanced stability when used with ultra-low ESR output capacitors.

The PTH05T210W incorporates a comprehensive list of standard features. They include on/off inhibit, a differential remote output voltage sense which ensures tight load regulation, and an output overcurrent and overtemperature shutdown to protect against load faults. A programmable undervoltage lockout allows the turn-on voltage threshold to be customized. AutoTrack™ sequencing is a feature which simplifies the simultaneous power-up and power-down of multiple modules in a power system by allowing the outputs to track a common voltage.

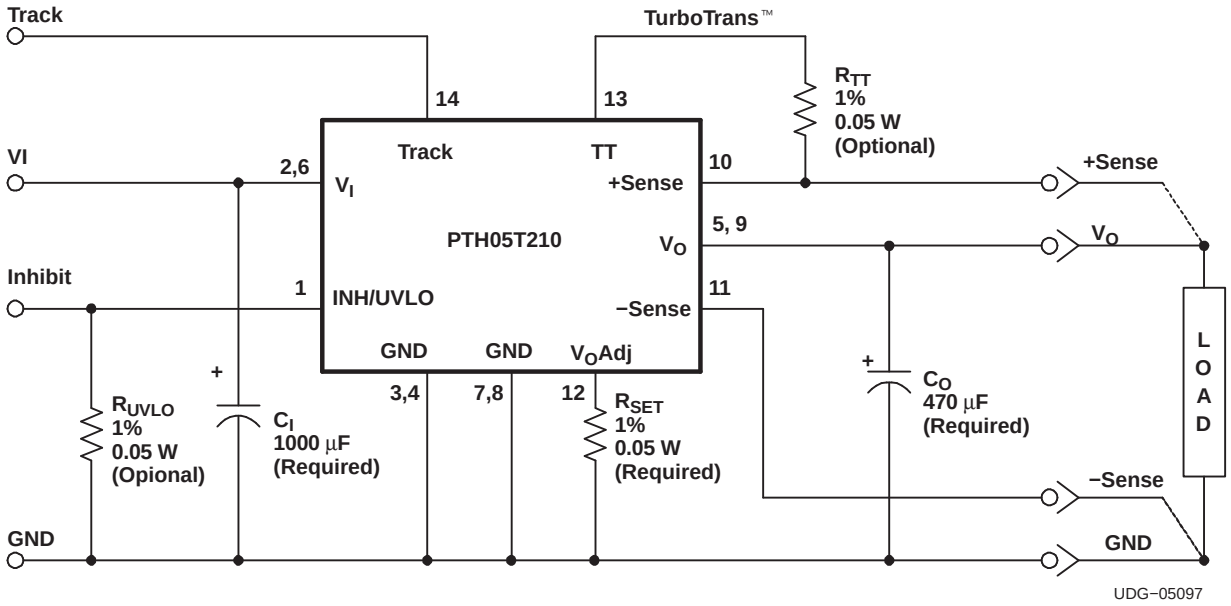
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



A. R_{SET} is required to set the output voltage higher than 0.7 V. See the *Electrical Characteristics* table.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

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DATASHEET TABLE OF CONTENTS

DATASHEET SECTION	PAGE NUMBER
ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS	3
ELECTRICAL CHARACTERISTICS TABLE (PTH05T210W)	4
TERMINAL FUNCTIONS	6
TYPICAL CHARACTERISTICS (V_I = 5V)	7
ADJUSTING THE OUTPUT VOLTAGE	8
INPUT & OUTPUT CAPACITOR RECOMMENDATIONS	10
TURBOTRANS™ INFORMATION	14
UNDERVOLTAGE LOCKOUT (UVLO)	19
SOFT-START POWER-UP	20
REMOTE SENSE	20
OUTPUT INHIBIT	21
OVER-CURRENT PROTECTION	21
OVER-TEMPERATURE PROTECTION	22
AUTO-TRACK SEQUENCING	22
TAPE & REEL AND TRAY DRAWINGS	25

ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

				UNIT	UNIT
	Signal input voltage	Track control (pin 14)		–0.3 to V_I + 0.3	V
T_A	Operating temperature range	Over V_I range		–40 to 85	°C
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins **(5 seconds maximum)**	PTH05T210WAH	260	
			PTH05T210WAD		
T_{reflow}	Solder reflow temperature	Surface temperature of module body or pins	PTH05T210WAS	235(1)	
			PTH05T210WAZ	260(1)	
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package		–55 to 125	
T_{pkg}	Packaging temperature	Shipping Tray or Tape and Reel storage or bake temperature		45	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3 1 msec, sine, mounted		250	G
	Mechanical vibration	Mil-STD-883D, Method 2007.2 20-2000 Hz		15	
	Weight			8.5	grams
	Flammability	Meets UL94V-O			

(1) During reflow of surface mount package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

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ELECTRICAL CHARACTERISTICS

T_A =25°C, V_I = 5 V, V_O = 3.3 V, C_I = 1000 µF, C_O = 470 µF OS-CON, and I_O = I_O max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_O	Output current	25°C, natural convection			0		30	A
		60°C, 200 LFM			0		30	
V_I	Input voltage range	Over I_O range			4.5		5.5	V
V_{OADJ}	Output voltage adjust range	Over I_O range			0.7		3.6	V
V_O	Set-point voltage tolerance						±1 (1)	$\%V_o$
	Temperature variation	–40°C < T_A < 85°C				±0.3		$\%V_o$
	Line regulation	Over V_I range				±4		mV
	Load regulation	Over I_O range				±7		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C					±1.5 (1)	$\%V_o$
η	Efficiency	I_O = 26 A	R_{SET} = 1.62 kΩ, V_O = 3.3 V			95%		
			R_{SET} = 5.23 kΩ, V_O = 2.5 V			94%		
			R_{SET} = 12.7 kΩ, V_O = 1.8 V			92%		
			R_{SET} = 19.6 kΩ, V_O = 1.5 V			91%		
			R_{SET} = 35.7 kΩ, V_O = 1.2 V			89%		
			R_{SET} = 63.4 kΩ, V_O = 1.0 V			87%		
			Open, V_O = 0.7 V			83%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth				10		mV_{PP}
I_{LIM}	Overcurrent threshold	Reset, followed by auto-recovery				55		A
t_{tr}	Transient response	2.5 A/µs load step 50 to 100% $I_O$max	w/o TurboTrans C_O = 470µF	Recovery time		50		µs
ΔV_{tr}				V_O over/undershoot		140		mV
t_{tr}			w/o TurboTrans C_O = 940µF, Type C	Recovery time		50		µs
ΔV_{tr}				V_O over/undershoot		120		mV
t_{trTT}			w/ TurboTrans C_O = 940µF, Type C	Recovery time		5		µs
ΔV_{trTT}				V_O over/undershoot		80		mV
I_{IL}	Track input current (pin 14)	Pin to GND					–130 (2)	µA
dV_{track}/dt	Track slew rate capability	C_O ≤ C_O (max)					1	V/ms
$UVLO_{ADJ}$	Adjustable Undervoltage lockout (pin 1)	Pin 1 open	V_I increasing		4.00	4.25	4.45	V
			V_I Turn–Off Hysterisis			0.150		
	Inhibit control (pin 1)	Input high voltage (V_{IH})			V_I – 0.5		Open (3)	V
		Input low voltage (V_{IL})			-0.2		0.6	
		Input low current (I_{IL})				125		µA
I_{in}	Input standby current	Inhibit (pin 1) to GND, Track (pin 14) open				3		mA
f_s	Switching frequency	Over V_I and I_O ranges				640		kHz
C_I	External input capacitance				1000 (4)			µF

(1) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/C or better temperature stability.
(2) A low-leakage (<100 nA), open-drain device, such as MOSFET or voltage supervisor IC, is recommended to control pin 14. The open-circuit voltage is less than 5 Vdc.
(3) This control pin has an internal pullup to the input voltage V_I. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended for control. For additional information, see the related application note.
(4) A 1000 µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimum of 1000 mA rms of ripple current.

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ELECTRICAL CHARACTERISTICS (continued)

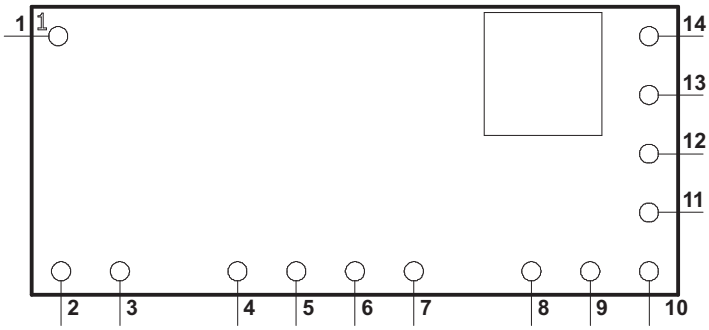
T_A =25°C, V_I = 5 V, V_O = 3.3 V, C_I = 1000 µF, C_O = 470 µF OS-CON, and I_O = I_O max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
C_O	External output capacitance	w/out TurboTrans	Capacitance Value	Nonceramic	470 (5)		12,000 (6)	µF
				Ceramic			5000	
			Equivalent series resistance (nonceramic)		3 (7)			mΩ
		w/ TurboTrans	Capacitance Value		See TT chart (8)		12,000 (9)	µF
			Capacitance × ESR product (C_O × ESR)				10,000 (10)	µF × mΩ
MTBF	Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign			3.6			10^6 Hr

(5) A minimum value of external output capacitor is required for proper operation. Adding additional capacitance at the load further improves transient response. See the Capacitor Application Information section for more guidance.
(6) This is the calculated maximum. This value includes both ceramic and non-ceramic capacitors. The minimum ESR requirement often results in a lower value. See the related Application Information for more guidance.
(7) This is the minimum ESR for all the electrolytic (nonceramic) capacitance. Use 5 mΩ as the minimum when using manufacturer's max-ESR values to calculate.
(8) Minimum capacitance is determined by the transient deviation requirement. A corresponding resistor, R_{TT} is required for proper operation. See the TurboTrans Selection section for guidance in selecting the capacitance and R_{TT} value.
(9) This is the calculated maximum. This value includes both ceramic and non-ceramic capacitors.
(10) When calculating the Capacitance × ESR product use the capacitance and ESR values of a single capacitor. For an output capacitor bank of several capacitor types and values, calculate the C × ESR product using the values of the capacitor that makes up the majority of the capacitance.

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PTH05T210W
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	2, 6	The positive input voltage power node to the module, which is referenced to common GND.
V_O	5, 9	The regulated positive power output with respect to the GND.
GND	3, 4 7, 8	This is the common ground connection for the V_I and V_O power connections. It is also the 0 V_{dc} reference for the control inputs.
Inhibit(1)/ UVLO adjust	1	The Inhibit pin is an open-collector/drain, negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. This input is not compatible with TTL logic devices and should not be tied to V_I or any other voltage. This pin is also used for input undervoltage lockout (UVLO) programming. Connecting a resistor from this pin to GND (pin 3) allows the ON threshold of the UVLO to be adjusted higher than the default value. For more information, see the Application Information section.
V_o Adjust	12	A 0.05 W, 1% resistor must be directly connected between this pin and pin 8 (GND) to set the output voltage to a value higher than 0.7 V. The temperature stability of the resistor should be 100 ppm/°C (or better). The setpoint range for the output voltage is from 0.7 V to 3.6 V. If left open circuit, the output voltage defaults to its lowest value. For further information, on output voltage adjustment see the related application note. The specification table gives the preferred resistor values for a number of standard output voltages.
+ Sense	10	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, +Sense must be connected to V_O , very close to the load.
– Sense	11	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, –Sense must be connected to GND (pin 8), very close to the load.
Track	14	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the module's output voltage follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I. NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the related application note.
TurboTrans™	13	This input pin adjusts the transient response of the regulator. To activate the *TurboTrans*™ feature, a 0.05 W, 1% resistor must be connected between this pin and pin 10 (+Sense) very close to the module. For a given value of output capacitance, a reduction in peak output voltage deviation is achieved by using this feature. If unused, this pin must be left open-circuit. External capacitance must never be connected to this pin. The resistance requirement can be selected from the TurboTrans™ resistor table in the Application Information section.

(1) Denotes negative logic: Open = Normal operation, Ground = Function active

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TYPICAL CHARACTERISTICS(1)(2)

CHARACTERISTIC DATA (V_I = 5 V)

EFFICIENCY VS LOAD CURRENT

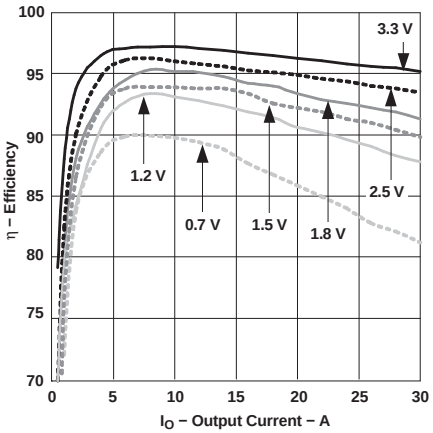


Figure 1.

OUTPUT RIPPLE VS LOAD CURRENT

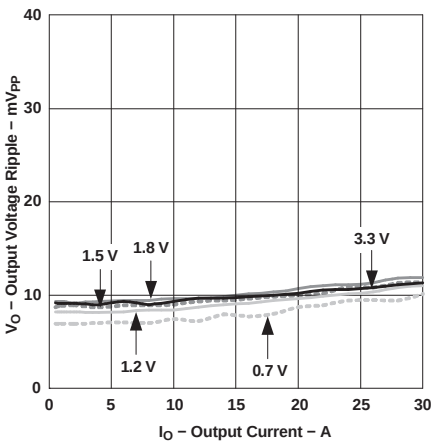


Figure 2.

POWER DISSIPATION VS LOAD CURRENT

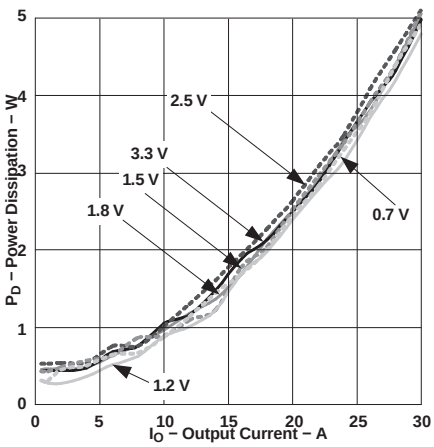


Figure 3.

AMBIENT TEMPERATURE VS OUTPUT CURRENT

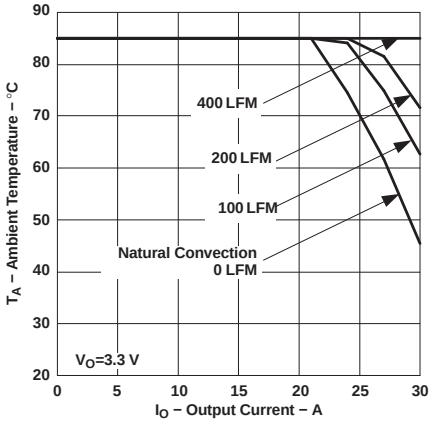


Figure 4.

AMBIENT TEMPERATURE VS OUTPUT CURRENT

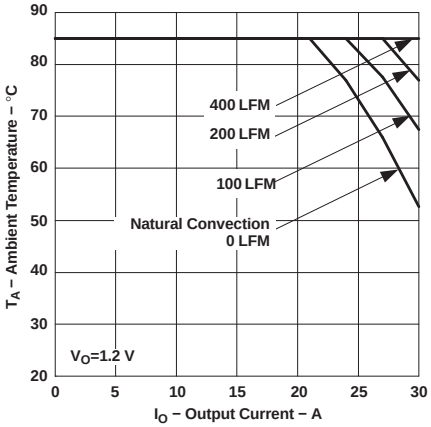


Figure 5.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm × 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 4 and Figure 5.

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APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

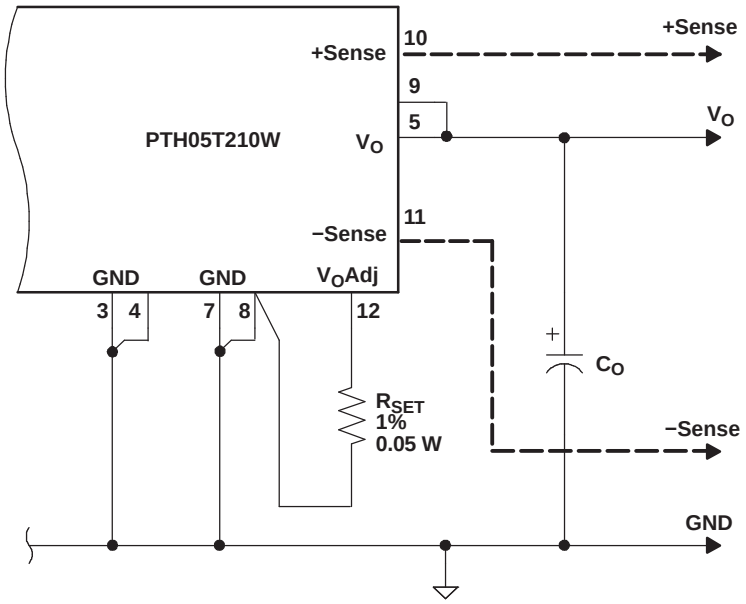
The V_O Adjust control (pin 12) sets the output voltage of the PTH05T210W. The adjustment range of the PTH05T210W is 0.7V to 3.6V. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the V_o Adjust and GND pins. Table 1 gives the standard value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 6 shows the placement of the required resistor.

$$R_{SET} = 30.1\ k\Omega \times \frac{0.7}{V_O - 0.7} - 6.49\ k\Omega \quad (1)$$

Table 1. Standard Values of R_{SET} for Standard Output Voltages

V_O (Standard) (V)	R_{SET} (Standard Value) (Ω)	V_O (Actual) (V)
3.3	1.62 k	3.298
2.5	5.23 k	2.498
2	9.76 k	1.997
1.8	12.7 k	1.798
1.5	19.6 k	1.508
1.2	35.7 k	1.199
1	63.4 k	1.001
0.7	Open	0.700



(1) Use a 0.05 W resistor. The tolerance should be 1%, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 12 and 8 using dedicated PCB traces.

(2) Never connect capacitors from V_O Adjust to either GND or V_O. Any capacitance added to the V_O Adjust pin affects the stability of the regulator.

Figure 6. V_O Adjust Resistor Placement

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Table 2. Output Voltage Set-Point Resistor Values

V_O Required	R_{SET} (kΩ)	V_O Required	R_{SET} (kΩ)
0.70	Open	2.10	8.66
0.75	412	2.20	7.50
0.80	205	2.30	6.65
0.85	133	2.40	5.90
0.90	97.6	2.50	5.23
0.95	78.7	2.60	4.64
1.00	63.4	2.70	4.02
1.10	46.4	2.80	3.57
1.20	35.7	2.90	3.09
1.30	28.7	3.00	2.67
1.40	23.7	3.10	2.26
1.50	19.6	3.20	1.96
1.60	16.9	3.30	1.62
1.70	14.7	3.40	1.30
1.80	12.7	3.50	1.02
1.90	11.0	3.60	.768
2.00	9.76		

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CAPACITOR RECOMMENDATIONS FOR THE PTH05T210W POWER MODULE

Input Capacitor (Required)

The size and value of the input capacitor is determined by the converter's transient performance capability. The minimum amount of required input capacitance is 1000 µF, with an RMS ripple current rating of 1000 mA. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes.

For high-performance/transient applications, or wherever the input source performance is degraded, 2000 µF of input capacitance is recommended. The additional input capacitance above the minimum level insures an optimized performance.

Ripple current (rms) rating, less than 100 mΩ of equivalent series resistance (ESR), and temperature are the main considerations when selecting input capacitors. The ripple current reflected from the input of the PTH05T210W module is moderate to low. Therefore any good quality, computer-grade electrolytic capacitor has an adequate ripple current rating.

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement. When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, Os-Con, poly-aluminum, and polymer-tantalum types should be considered. Adding one or two ceramic capacitors to the input attenuates high-frequency reflected ripple current.

TurboTrans Output Capacitor

The PTH05T210W requires a minimum output capacitance of 470 µF. The required capacitance above 470µF is determined by actual transient deviation requirements.

TurboTrans allows the designer to optimize the capacitance load according to the system transient design requirement. High quality, ultra-low ESR capacitors are required to maximize TurboTrans effectiveness. Capacitors with a capacitance (µF) × ESR (mΩ) product of ≤10,000mΩ×µF are required.

Working Example:

A bank of 6 identical capacitors, each with a capacitance of 680µF and 5mΩESR, has a C×ESR product of 3400µFxmΩ (680µF × 5mΩ).

Using TurboTrans in conjunction with the high quality capacitors (capacitance (µF) × ESR (mΩ)) reduces the overall capacitance requirement while meeting the minimum transient amplitude level.

Table 3 includes a preferred list of capacitors by type and vendor. See the Output Bus / TurboTrans column.

Note: See the TurboTrans Technology Application Notes within this document for selection of specific capacitance.

Non-TurboTrans Output Capacitor

The PTH05T210W requires a minimum output capacitance of 470µF. Non-TurboTrans applications must observe minimum output capacitance ESR limits.

A combination of 200µF of ceramic capacitors plus low ESR (15mΩ to 30mΩ) Os-Con electrolytic/tantalum type capacitors can be used. When using Polymer tantalum types, tantalum type, or Oscon types only, the capacitor ESR bank limit is 3mΩ to 5mΩ. (Note: no ceramic capacitors are required). This is necessary for the stable operation of the regulator. Additional capacitance can be added to improve the module's performance to load transients. High quality computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above -20°C. For operation below -20°C, tantalum, ceramic, or Os-Con type capacitors are necessary.

When using a combination of one or more non-ceramic capacitors, the calculated equivalent ESR should be no lower than 2mΩ (4mΩ when calculating using the manufacturer's maximum ESR values). A list of preferred low-ESR type capacitors, are identified in Table 3.

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Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

When used on the output their combined ESR is not critical as long as the total value of ceramic capacitors, with values between 10 µF and 100 µF, does not exceed 5000 µF (non-TurboTrans). In TurboTrans applications, when ceramic capacitors are used on the output bus, total capacitance including bulk and ceramic types is not to exceed 12,000 µF.

Tantalum, Polymer-Tantalum Capacitors

Tantalum type capacitors are only used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS series and Kemet capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable due to their reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

Capacitor Table

Table 3 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 2.5A/µs. The typical voltage deviation for this load transient is given in the Electrical Characteristics table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability.

If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional low ESR ceramic capacitor decoupling. Generally, with 50% load steps at > 100A/µs, adding multiple 10µF ceramic capacitors, 3225 case size, plus 10×1µF, including numerous high frequency ceramics (≤0.1µF) are all that is required to soften the transient higher frequency edges. Special attention is essential with regards to location, types, and position of higher frequency ceramic and lower ESR bulk capacitors. DSP, FPGA and ASIC vendors identify types, location and capacitance required for optimum performance of the high frequency devices. The details regarding the PCB layout and capacitor/component placement are important at these high frequencies. Low impedance buses and unbroken PCB copper planes with components located as close to the high frequency processor are essential for optimizing transient performance. In many instances additional capacitors may be required to insure and minimize transient aberrations.

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Table 3. Input/Output Capacitors(1)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			
	Working Voltage	Value (µF)	Max. ESR at 100 kHz	Max Ripple Current at 85°C (Irms)	Physical Size (mm)	Input Bus	Output Bus		Vendor Part No.
							No TurboTrans	TurboTrans (Cap Type)(2)	
Panasonic	25 V	1000	0.043Ω	>1690 mA	16 × 15	1	≥ 2(3)	N/R(4)	EEUFC1E102S
FC (Radial)	25 V	1800	0.029Ω	2205 mA	16 × 20	1	≥ 1(3)	N/R(4)	EEUFC1E182
FC(SMD)	25 V	2200	0.028Ω	>2490 mA	18 × 21,5	1	≥ 1(3)	N/R(4)	EEVFC1E222N
FK(SMD)	25 V	1000	0.060Ω	1100 mA	12,5×13,5	1	≥ 2(5)	N/R(4)	EEVFK1V102Q
United Chemi-Con									
PTB(SMD) Polymer Tantalum	6.3 V	470	0.025Ω	2600 mA	7,3x 4,3x 2.8	2(6)	≥ 2 ~ ≤ 4(3)	C ≥ 2(2)	6PTB477MD8TER
LXZ, Aluminum (Radial)	25 V	680	0.068Ω	1050 mA	10 × 16	2	≥ 1 ~ ≤ 3(3)	N/R(4)	LXZ25VB681M10X20LL
PS, Poly-Aluminum(Radial)	16 V	330	0.014Ω	5060 mA	10 × 12,5	3(6)	≥ 2 ~ ≤ 3	B ≥ 2(2)	16PS330MJ12
PXA, Poly-Aluminum (SMD)	16 V	330	0.014Ω	5050 mA	10 × 12,2	3(6)	≥ 2 ~ ≤ 3	B ≥ 2(2)	PXA16VC331MJ12TP
PS, Poly-Aluminum(Radial)	6.3 V	680	0.010Ω	5500 mA	10 × 12,5	2	≥ 1 ~≤ 2	C ≥ 1(2)	6PS680MJ12
PXA, Poly-Aluminum(Radial)	6.3 V	470	0.012Ω	4770 mA	8 × 12,2	2(6)	≥ 1 ~ ≤ 2	C ≥ 1(2)	PXA6.3VC471MH12TP
Nichicon, Aluminum	25 V	470	0.070Ω	985 mA	12,5 × 15	2(6)	≥ 2(3)	N/R(4)	UPM1E471MHH6
HD (Radial)	25 V	470	0.038Ω	1430 mA	10 × 16	2(6)	≥ 2(3)	N/R(4)	UHD1E471MHR
PM (Radial)	35 V	560	0.048Ω	1360 mA	16 × 15	2	≥ 2(3)	N/R(4)	UPM1V561MHH6
Panasonic, Poly-Aluminum:	2.0 V	390	0.005Ω	4000 mA	7,3 L×4,3 W ×4,2H	N/R(7)	N/R(7)	B ≥ 2(2)	EEFSE0J391R(V_O≤1.6V)(8)

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.
RoHS, Lead-free and Material Details
See the capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.

(2) Required capacitors with TurboTrans. See the TransTrans Application information for Capacitor Selection
Capacitor Type Groups by ESR (Equivalent Series Resistance) :
a. Type A = (100 < capacitance × ESR ≤ 1000)
b. Type B = (1,000 < capacitance × ESR ≤ 5,000)
c. Type C = (5,001 < capacitance × ESR ≤ 10,000)

(3) Total bulk nonceramic capacitors on the output bus with ESR of ≥ 15mΩ to ≤ 30mΩ requires an additional ≥ 200 µF of ceramic capacitor.

(4) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher ESR × capacitance products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.

(5) Output bulk capacitor's maximum ESR is ≥ 30 mΩ. Additional ceramic capacitance of ≥ 200 µF is required.

(6) The minimum capactiance on the input bus can be less than 1000 µF when using this type of capacitor. Insure that the minimum rms ripple current rating is met.

(7) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.

(8) The voltage rating of this capacitor only allows it to be used for output voltage that is equal to or less than 80% of the working voltage.

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Table 3. Input/Output Capacitors (continued)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			
	Working Voltage	Value (µF)	Max. ESR at 100 kHz	Max Ripple Current at 85°C (Irms)	Physical Size (mm)	Input Bus	Output Bus		Vendor Part No.
							No TurboTrans	TurboTrans (Cap Type)(2)	
Sanyo									
TPE, Poscap (SMD)	6.3 V	470	0.018Ω	3500 mA	7,3 × 4,3	N/R(9)	≥ 1 ~ ≤ 3	C ≥ 1(10)	6TPE470MI
TPE Poscap(SMD)	2.5 V	470	0.007Ω	4400 mA	7,3 × 4,3	N/R(9)	≥ 1 ≤ 2	B ≥ 2(10)	2R5TPE470M7(V_O ≤ 1.8 V)(11)
TPD Poscap (SMD)	2.5 V	1000	0.005Ω	6100 mA	7,3 × 4,3	N/R(9)	≤ 1	B ≥ 1(10)	2R5TPD1000M5(V_O ≤ 1.8 V)(11)
SA, Os-Con (Radial)	16 V	470	0.020Ω	>6080 mA	16 × 23	2(12)	≥ 1 ~ ≤ 4	N/R(13)	16SA470M
SP Oscon (Radial)	10 V	470	0.015	>4500 mA	10 × 11,5	2(12)	≥ 1 ~ ≤ 3	C ≥ 2(10)	10SP470M
SEPC, Os-Con (Radial)	6.3 V	1500	0.010Ω	>5500 mA	10 × 13	1	≥ 1 ~ ≤ 2	B ≥ 1(10)	6SEPC1500M
SVPA, Os-Con (SMD)	6.3 V	470	0.020Ω	4700mA	10 × 10,3	2(12)	≥ 1 ~ ≤ 4(14)	C ≥ 1(10)(14)	6SVPA470M
AVX, Tantalum, Series III TPM Multianode	6.3 V 6.3 V	680 470	0.035Ω 0.018Ω	>2400 mA >3800 mA	7,3 L × 4,3 W × 4,1 H	N/R(9) N/R(9)	≥ 2 ~ ≤ 7(14) ≥ 2 ~ ≤ 3(14)	N/R(13) C ≥ 2(10)(14)	TPSE477M010R0045 TPME687M006#0018
TPS Series III (SMD)	4 V	1000	0.035Ω	2405	7,3 L ×5,7 W	N/R(9)	≥ 2 ~ ≤ 7(14)	N/R(13)	TPSV108K004R0035 (V_O ≤ 2.2 V)(11)
Kemet, Poly-Tantalum	6.3 V	470	0.018Ω	2700 mA	4,3 W	N/R(9)	≥ 1 ~ ≤ 3(14)	C ≥ 2(10)	T520X477M06ASE018
T520 (SMD)	6.3 V	470	0.010Ω	>5200 mA	× 7,3 L	N/R(9)	≥ 1 ~ ≤2	B ≥ 1(10)	T530X477M006ASE010
T530 (SMD)	6.3 V	470	0.005Ω	7300 mA	× 4 H	2(12)	≤ 1	B ≥ 1(10)	T530X477M006ASE005
T530 (SMD)	2.5 V	1000	0.005Ω	7300 mA	4,3 w × 7,3 L	2(12)	≤ 1	B ≥ 1(10)	T530X108M2R5ASE005 (V_O ≤ 2.0 V)(11)
Vishay-Sprague									
594D, Tantalum (SMD)	6.3 V	1000	0.030Ω	2890 mA	7,2L ×5,7 W ×4,1H	N/R(9)	≥ 1 ~ ≤ 6	N/R(13)	594D108X06R3R2TR2T
94SA, Os-con (Radial)	16 V	1000	0.015Ω	9740 mA	16 × 25	1	≥ 1 ~ ≤ 3	N/R(13)	94SA108X0016HBP
94SVP Os-Con(SMD)	16 V	330	0.017Ω	>4500 mA	10 × 12,7	2	≥ 2 ~ ≤ 3	C ≥ 1(10)	94SVP827X06R3F12
Kemet, Ceramic X5R (SMD)	16 V	10	0.002Ω	–	3225	1(15)	≥ 1(16)	A(10)	C1210C106M4PAC
	6.3 V	47	0.002Ω			N/R(9)	≥ 1(16)	A(10)	C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3 V	100	0.002Ω	–	3225	N/R(9)	≥ 1(16)	A(10)	GRM32ER60J107M
	6.3 V	47				N/R(9)	≥ 1(16)	A(10)	GRM32ER60J476M
	25 V	22				1(15)	≥ 1(16)	A(10)	GRM32ER61E226K
	16 V	10				1(15)	≥ 1(16)	A(10)	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 V	100	0.002Ω	–	3225	N/R(9)	≥ 1(16)	A(10)	C3225X5R0J107MT
	6.3 V	47				N/R(9)	≥ 1(16)	A(10)	C3225X5R0J476MT
	16 V	10				1(15)	≥ 1(16)	A(10)	C3225X5R1C106MT0
	16 V	22				1(15)	≥ 1(16)	A(10)	C3225X5R1C226MT

(9) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(10) Required capacitors with TurboTrans. See the TransTrans Application information for Capacitor Selection
Capacitor Type Groups by ESR (Equivalent Series Resistance) :
a. Type A = (100 < capacitance × ESR ≤ 1000)
b. Type B = (1,000 < capacitance × ESR ≤ 5,000)
c. Type C = (5,001 < capacitance × ESR ≤ 10,000)
(11) The voltage rating of this capacitor only allows it to be used for output voltage that is equal to or less than 80% of the working voltage.
(12) The minimum capactiance on the input bus can be less than 1000 µF when using this type of capacitor. Insure that the minimum rms ripple current rating is met.
(13) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher ESR × capacitance products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.
(14) Total bulk nonceramic capacitors on the output bus with ESR of ≥ 15mΩ to ≤ 30mΩ requires an additional ≥ 200 µF of ceramic capacitor.
(15) In addition to the required input capacitance , ceramic capacitors can be added to attenuate high-frequency reflected ripple current.
(16) Maximum ceramic capacitance on the output bus is ≤ 3000 µF. Any combination of the ceramic capacitor values is limited to 3000 µF for non-TurboTrans applications. The total capacitance is limited to 14,000 µF which includes all ceramic and non-ceramic types.

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TurboTrans™ Technology

TurboTrans technology is a feature introduced in the T2 generation of the PTH/PTV family of power modules. TurboTrans optimizes the transient response of the regulator with added external capacitance using a single external resistor. The, benefits of this technology include: reduced output capacitance, minimized output voltage deviation following a load transient, and enhanced stability when using ultra-low ESR output capacitors. The amount of output capacitance required to meet a target output voltage deviation, is reduced with TurboTrans activated. Likewise, for a given amount of output capacitance, with TurboTrans engaged, the amplitude of the voltage deviation following a load transient is reduced. Applications requiring tight transient voltage tolerances and minimized capacitor footprint area benefit from this technology.

TurboTrans™ Selection

Utilizing TurboTrans requires connecting a resistor, R_{TT}, between the +Sense pin (pin10) and the TurboTrans pin (pin13). The value of the resistor directly corresponds to the amount of output capacitance required. All T2 products require a minimum value of output capacitance whether or not TurboTrans is used. For the PTH05T210W, the minimum required capacitance is 470µF. When using TurboTrans, capacitors with a capacitance × ESR product below 10,000µF × mΩ are required. (Multiply the capacitance (in µF) by the ESR (in mΩ) to determine the capacitance × ESR product.) See the Capacitor Selection section of the datasheet for a variety of capacitors that meet this criteria.

Figure 7 through Figure 9, show the amount of output capacitance required to meet a desired transient voltage deviation with and without TurboTrans for several capacitor types; TypeA (e.g.ceramic), TypeB (e.g.polymer-tantalum), and TypeC (e.g.OS-CON). To calculate the proper value of R_{TT}, first determine the required transient voltage deviation limits and magnitude of the transient load step. Next, determine what type of output capacitors to be used. (If more than one type of output capacitor is used, select the capacitor type that makes up the majority of the total output capacitance.) Knowing this information, use the chart in Figure 7 through Figure 9 that corresponds to the capacitor type selected. To use the chart, begin by dividing the maximum voltage deviation limit (in mV) by the magnitude of the load step (in Amps). This gives a mV/A value. Find this value on the Y-axis of the appropriate chart. Read across the graph to the *'With TurboTrans*' plot. From this point, read down to the X-axis which lists the minimum required capacitance, C_O, to meet the transient voltage deviation. The required R_{TT} resistor value can then be calculated using Equation 2 or selected from the TurboTrans table. The TurboTrans tables include both the required output capacitance and the corresponding R_{TT} values to meet several values of transient voltage deviation for 25%(7.5A), 50%(15A), and 75%(22.5A) output load steps.

The chart can also be used to determine the achievable transient voltage deviation for a given amount of output capacitance. Selecting the amount of output capacitance along the X-axis, reading up to the *'With TurboTrans'* curve, and then over to the Y-axis, gives the transient voltage deviation limit for that value of output capacitance. The required R_{TT} resistor value can be calculated using Equation 2 or selected from the TurboTrans table.

As an example, let's look at a 12-V application requiring a 60mV deviation during a 15A, 50% load transient. A majority of 330µF, 10mΩ output capacitors are used. Use the 12V, TypeB capacitor chart, Figure 8. Dividing 60mV by 15A gives 4mV/A transient voltage deviation per amp of transient load step. Select 4mV/A on the Y-axis and read across to the *'With TurboTrans*' plot. Following this point down to the X-axis gives us a minimum required output capacitance of approximately 1350µF. The required R_{TT} resistor value for 1350µF can then be calculated or selected from Figure 8. The required R_{TT} resistor is approximately 9.31kΩ.

To see the benefit of TurboTrans, follow the 4mV/A marking across to the *'Without TurboTrans*' plot. Following that point down shows that more than 10,000µF of output capacitance is required to meet the same transient deviation limit. This is the benefit of TurboTrans. A typical TurboTrans application schematic is shown in Figure 10.

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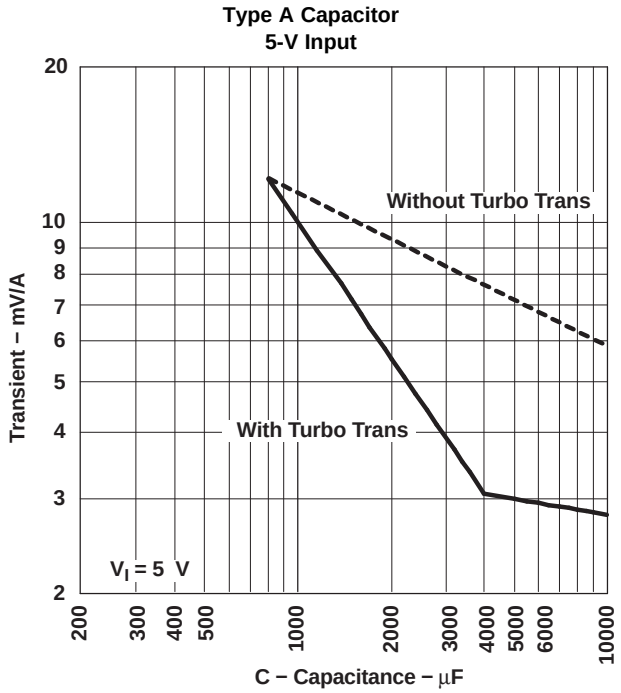


Figure 7. Capacitor Type A, 100 ≤ C µF × ESR ≤ 1000 mΩ (e.g. Ceramic)

Table 4. Type A TurboTrans C_O Values & Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			5-V Input	
25% Load Step (7.5 A)	50% Load Step (15 A)	75% Load Step (22.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
90	180	270	800	open
80	160	240	950	165
70	140	210	1100	75.0
60	120	180	1350	40.2
50	100	150	1650	22.1
40	80	120	2150	11.3
30	60	90	3000	3.65
25	40	60	3700	0.825

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming equation, see Equation 2.

$$R_{TT} = 40 \times \frac{1 - \left(\frac{C_O}{4000}\right)}{5 \times \left(\frac{C_O}{4000}\right) - 1} \text{ k}\Omega \quad (2)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 4000 µF require R_{TT} to be a short, 0Ω. (Equation 2 results in a negative value for R_{TT} when $C_O \geq 4000$ µF.)

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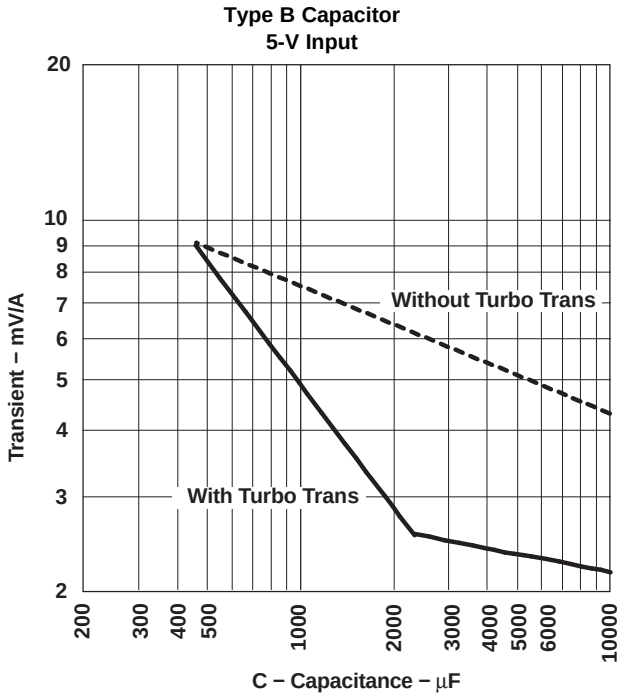


Figure 8. Capacitor Type B, 1000 ≤ C (µF) × ESR (mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

Table 5. Type B TurboTrans C_O Values & Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			5-V Input	
25% Load Step (7.5 A)	50% Load Step (15 A)	75% Load Step (22.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
70	140	210	470	open
60	120	180	560	174
50	100	150	700	57.6
40	80	120	950	24.9
35	70	105	1100	15.8
30	60	90	1350	9.31
25	50	75	1700	4.42
20	40	60	2250	0.523

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming equation, see Equation 3.

$$R_{TT} = 40 \times \frac{1 - \left(\frac{C_O}{2350}\right)}{5 \times \left(\frac{C_O}{2350}\right) - 1} \text{ k}\Omega \quad (3)$$

C_O values greater than or equal to 2350 µF require R_{TT} to be a short, 0Ω. (Equation 3 result sin a negative value for R_{TT} when $C_O \geq 2350$ µF.)

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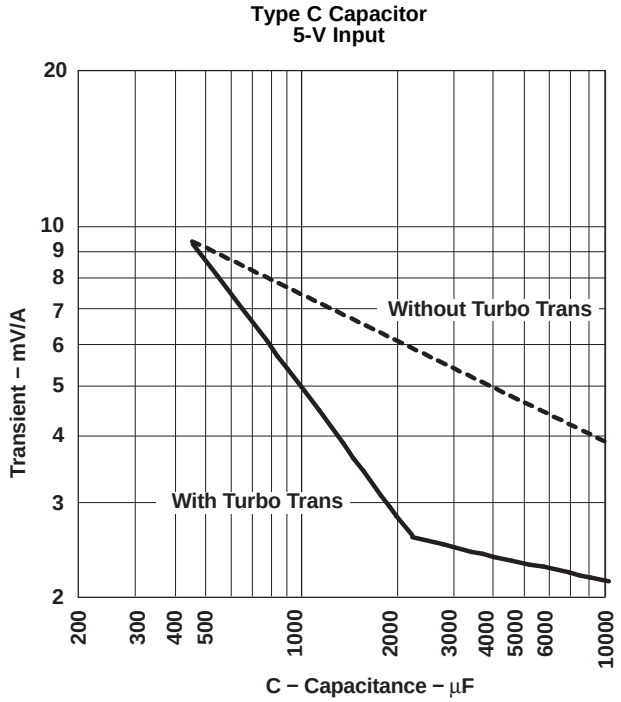


Figure 9. Capacitor Type C, 5000 ≤ C(µF)xESR(mΩ) ≤ 10,000 (e.g. Os-Con)

Table 6. Type C TurboTrans C_O Values & Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			5-V Input	
25% Load Step (7.5 A)	50% Load Step (15 A)	75% Load Step (22.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
70	140	210	470	open
60	120	180	600	130
50	100	150	750	51.1
40	80	120	950	22.6
35	70	105	1150	14.3
30	60	90	1400	8.45
25	50	75	1750	3.83
20	40	60	2300	0.182

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming equation, see Equation 4.

$$R_{TT} = 40 \times \frac{1 - \left(\frac{C_O}{2350}\right)}{5 \times \left(\frac{C_O}{2350}\right) - 1} \text{ k}\Omega \quad (4)$$

C_O values greater than or equal to 2350 µF require R_{TT} to be a short, 0Ω. (Equation 4 results in a negative value for R_{TT} when $C_O \geq 2350$ µF.)

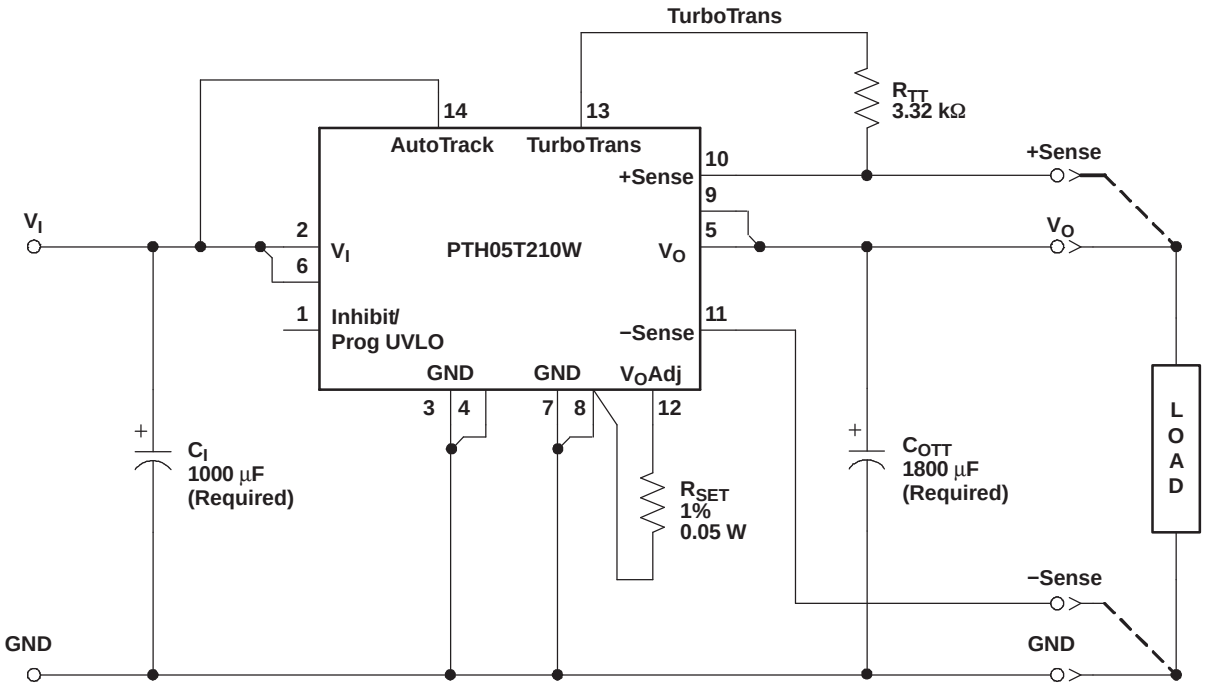


Figure 10. Typical TurboTrans Application Schematic

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UNDERVOLTAGE LOCKOUT (UVLO)

The PTH05T210W power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator's input source during the power-up sequence.

The UVLO characteristic is defined by the *ON* threshold (V_{THD}) voltage. Below the *ON* threshold, the Inhibit control is overridden, and the module does not produce an output. The hysterisis voltage, which is the difference between the *ON* and *OFF* threshold voltages, is nominally set at 150mV. The hysterisis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

UVLO Adjustment

The UVLO feature of the PTH05T210W module allows for limited adjustment of the *ON* threshold voltage. The adjustment is made via the *Inhbit/UVLO Prog* control pin (pin 1) using a single resistor (see figure below). When pin 1 is left open circuit, the *ON* threshold voltage is internally set to its default value. The *ON* threshold has a nominal voltage of 4.25 V, and a hysterisis of 150 mV. Adjusting the threshold voltage prevents the module from operating if the input bus fails to completely rise to its specified regulation voltage.

Equation 5 determines the value of R_{THD} required to adjust V_{THD} to a new value. The default value is 4.25 V, and it may only be adjusted to a higher value.

$$R_{UVLO} = \frac{101 - V_{THD}}{V_{THD} - 1} \ k\Omega \quad (5)$$

Table 7 lists the standard resistor values for R_{UVLO} for different values of the ON-threshold (V_{THD}) voltage.

Table 7. Standard Values of R_{UVLO} for Various Values of V_{THD}

V_{THD}	5.00 V	4.75 V	4.50 V	4.25 V
R_{UVLO}	24.3 kΩ	25.5 kΩ	27.57 kΩ	OPEN

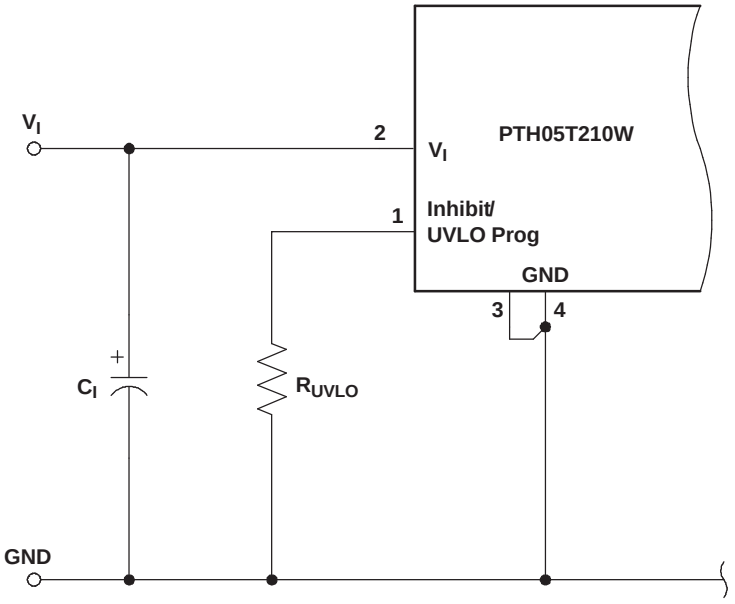


Figure 11. UVLO Program Resistor Placement

Soft-Start Power Up

The Auto-Track feature allows the power-up of multiple PTH/PTV modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_I. (see Figure 12)

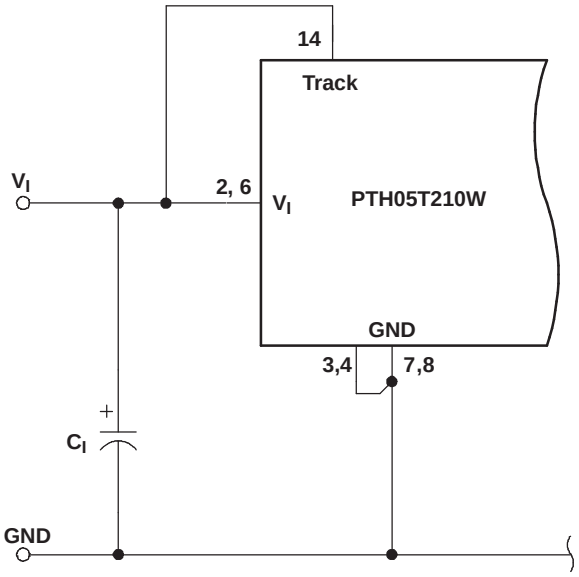


Figure 12. Power-Up Application Circuit

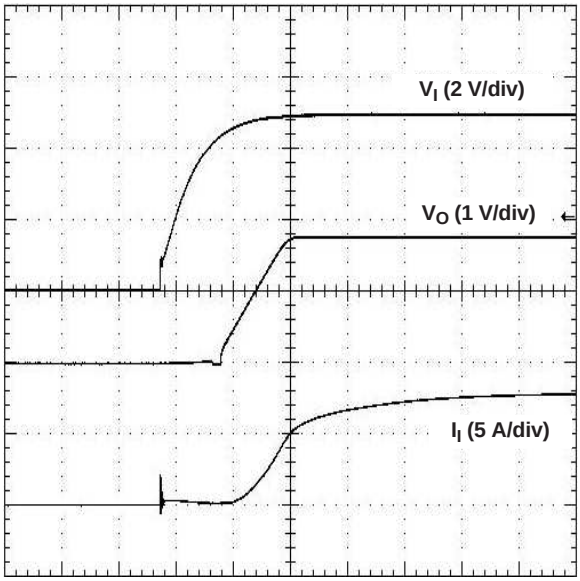


Figure 13. Power-Up Waveform

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate. From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8 ms–15ms) before allowing the output voltage to rise. The output then progressively rises to the module's setpoint voltage.

Figure 13 shows the soft-start power-up characteristic of the PTH05T210W operating from a 5-V input bus and configured for a 1.8-V output. The waveforms were measured with a 20-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 25 ms.

Remote Sense

Products with this feature incorporate one or two remote sense pins. Remote sensing improves the load regulation performance of the module by allowing it to compensate for any IR voltage drop between its output and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance.

To use this feature simply connect the Sense pins to the corresponding output voltage node, close to the load circuit. If a sense pin is left open-circuit, an internal low-value resistor (15-Ω or less) connected between the pin and the output node, ensures the output remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_O and GND pins, and that measured at the Sense pins, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

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Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTH05T210W incorporates an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 14 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit input has its own internal pull-up to a potential of 5 V. The input is not compatible with TTL logic devices and should not be tied to V_I. An open-collector (or open-drain) discrete transistor is recommended for control.

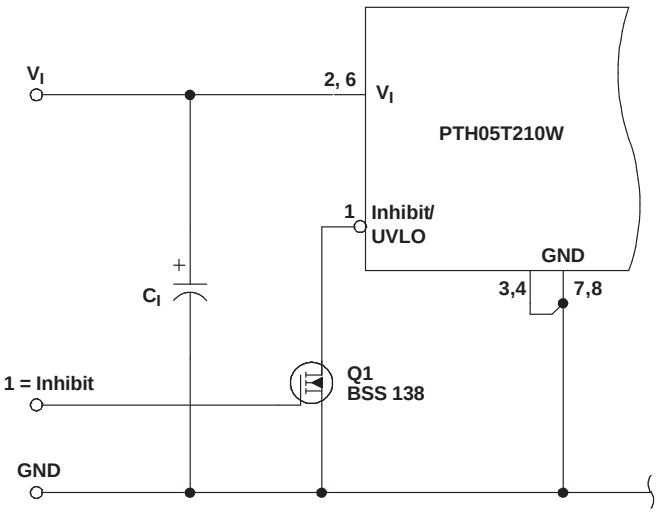


Figure 14. On/Off Inhibit Control Circuit

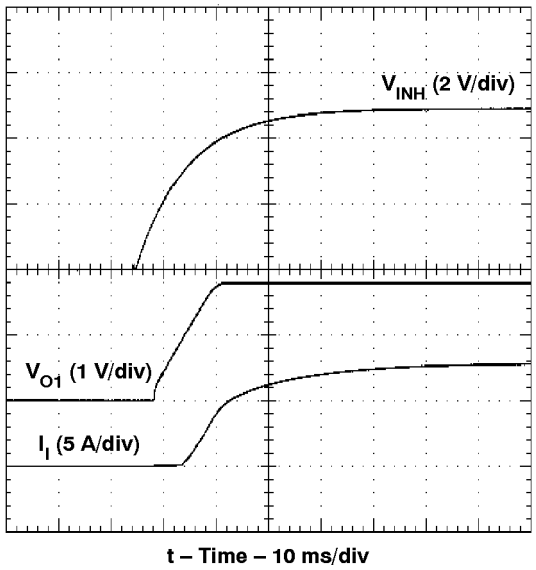


Figure 15. Power-Up Response from Inhibit Control

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 25 ms. Figure 15 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_{INH}. The waveforms were measured with a 20-A resistive load.

NOTE: When applying a low voltage (≤0.6 V) to the Inhibit control pin to turn off the module, the low side FET will immediately discharge any capacitance on the output bus. Depending on the amount and type of capacitors, this may induce a negative voltage transient that can momentarily go below GND potential. If turn-off control is desired, the Auto-Track pin can be used to the control ramp up and ramp down of the output voltage.

Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

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Overtemperature Protection (OTP)

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 18.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

Figure 18 shows how a TPS3808 supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of 5-V PTH modules. The output of the TPS3808 supervisor becomes active above an input voltage of 0.8 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 27ms after the input voltage has risen above U3's voltage threshold, which is 4.65V. The 27-ms time period is controlled by the capacitor C3. The value of 4700pF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

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Figure 16 shows the output voltage waveforms after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in Figure 17. Power down is normally complete before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that an input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the Auto-Track slew rate capability.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.

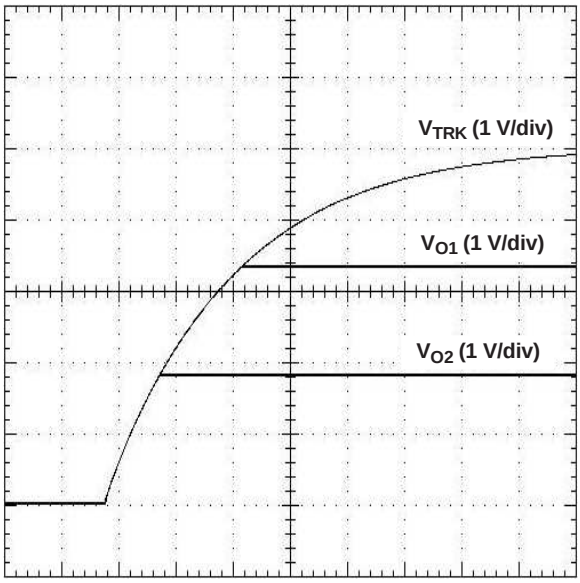


Figure 16. Simultaneous Power Up With Auto-Track Control

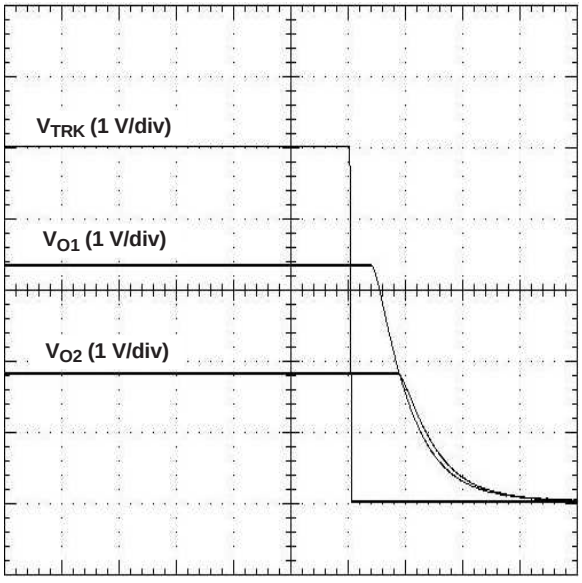


Figure 17. Simultaneous Power Down With Auto-Track Control

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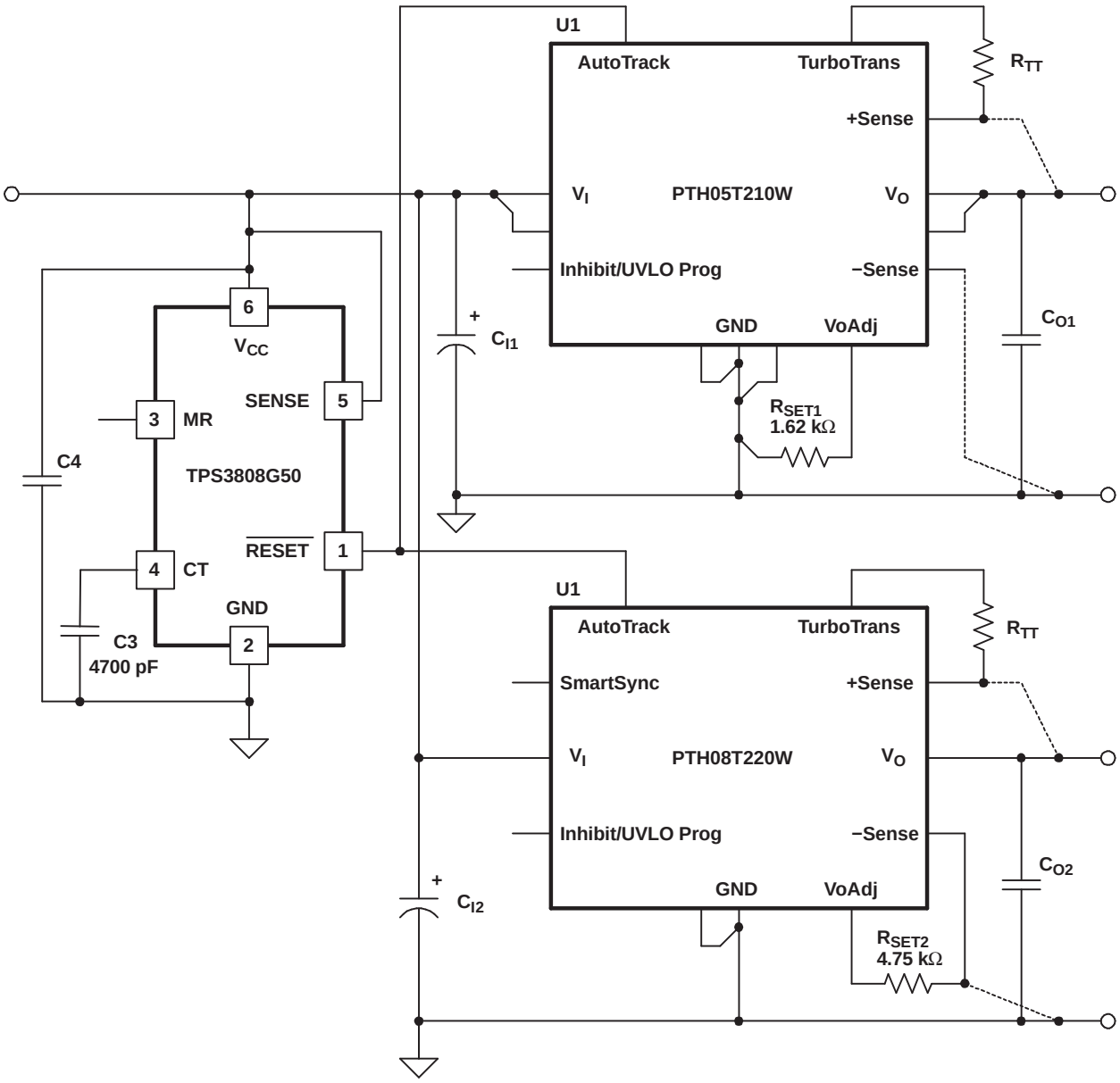
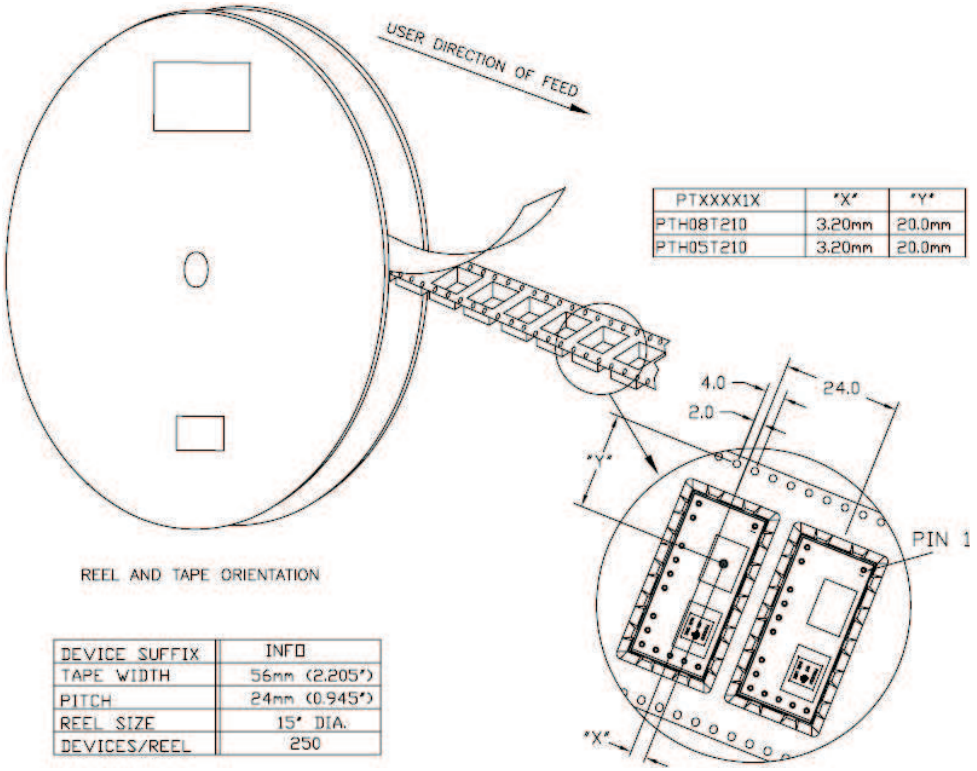


Figure 18. Sequenced Power Up and Power Down Using Auto-Track

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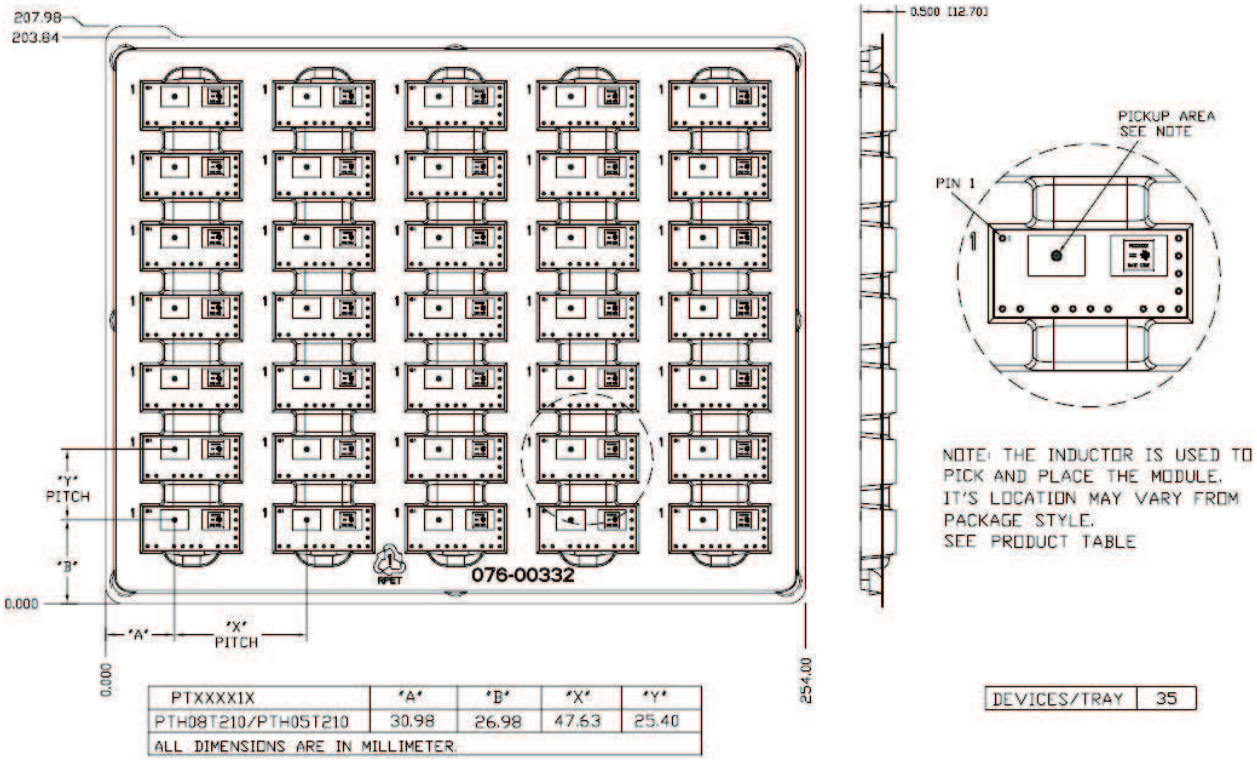
TAPE & REEL AND TRAY DRAWINGS



PTXXXX1X	"X"	"Y"
PTH08T210	3.20mm	20.0mm
PTH05T210	3.20mm	20.0mm

REEL AND TAPE ORIENTATION

DEVICE SUFFIX	INFO
TAPE WIDTH	56mm (2.205")
PITCH	24mm (0.945")
REEL SIZE	15" DIA.
DEVICES/REEL	250



PTXXXX1X	"A"	"B"	"X"	"Y"
PTH08T210/PTH05T210	30.98	26.98	47.63	25.40
ALL DIMENSIONS ARE IN MILLIMETER.				

DEVICES/TRAY	35

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTH05T210WAD	Last Time Buy	Production	Through-Hole Module (ECP) | 14	35 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
PTH05T210WAD.B	Last Time Buy	Production	Through-Hole Module (ECP) | 14	35 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
PTH05T210WAH	Last Time Buy	Production	Through-Hole Module (ECP) | 14	35 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
PTH05T210WAH.B	Last Time Buy	Production	Through-Hole Module (ECP) | 14	35 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
PTH05T210WAS	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	35 | TIW TRAY	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTH05T210WAS.B	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	35 | TIW TRAY	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTH05T210WAST	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	250 | SMALL T&R	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTH05T210WAST.B	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	250 | SMALL T&R	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTH05T210WAZ	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	35 | TIW TRAY	In-Work	SNAGCU	Level-3-260C-168 HR	-40 to 85	
PTH05T210WAZ.B	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	35 | TIW TRAY	In-Work	SNAGCU	Level-3-260C-168 HR	-40 to 85	
PTH05T210WAZT	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	250 | SMALL T&R	In-Work	SNAGCU	Level-3-260C-168 HR	-40 to 85	
PTH05T210WAZT.B	Last Time Buy	Production	Surface Mount Module (ECQ) | 14	250 | SMALL T&R	In-Work	SNAGCU	Level-3-260C-168 HR	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

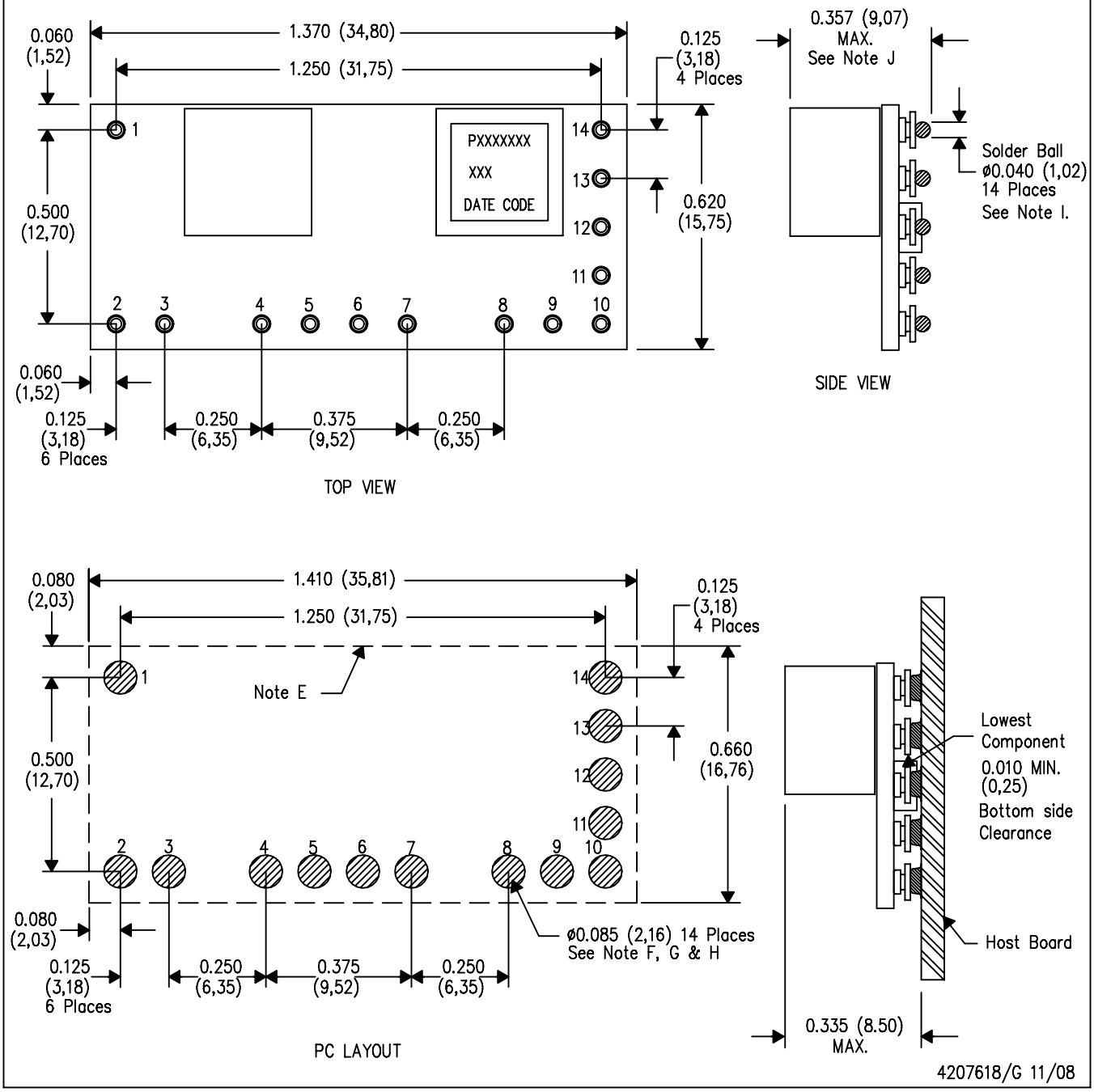
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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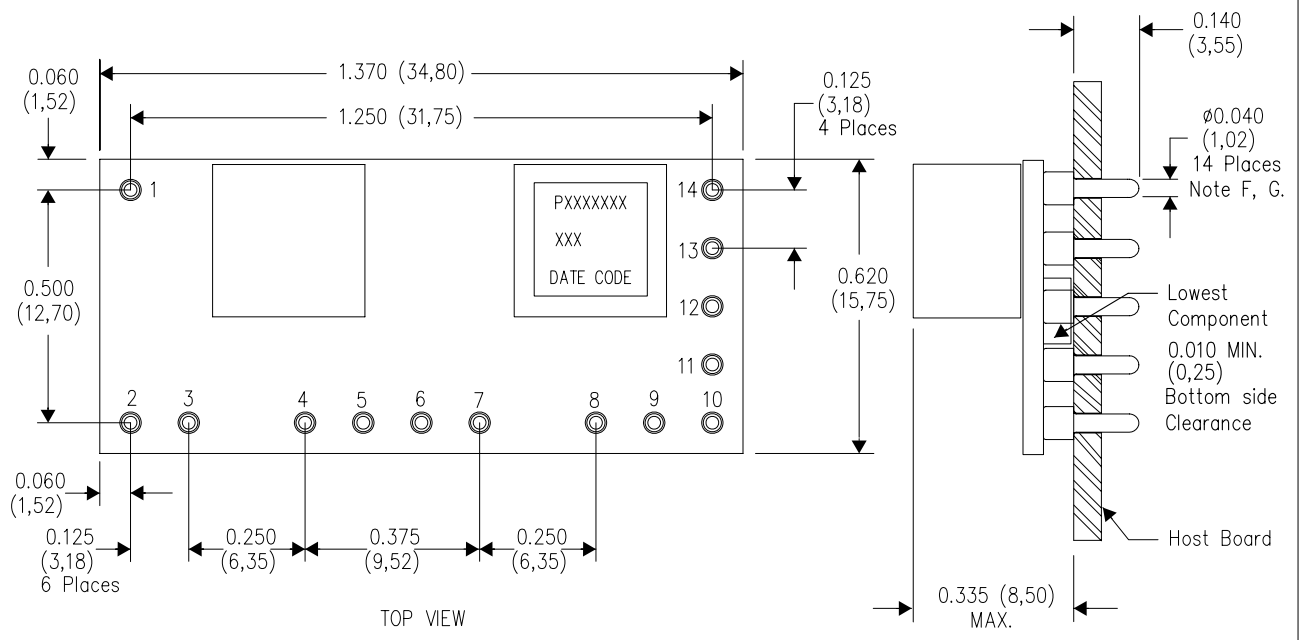
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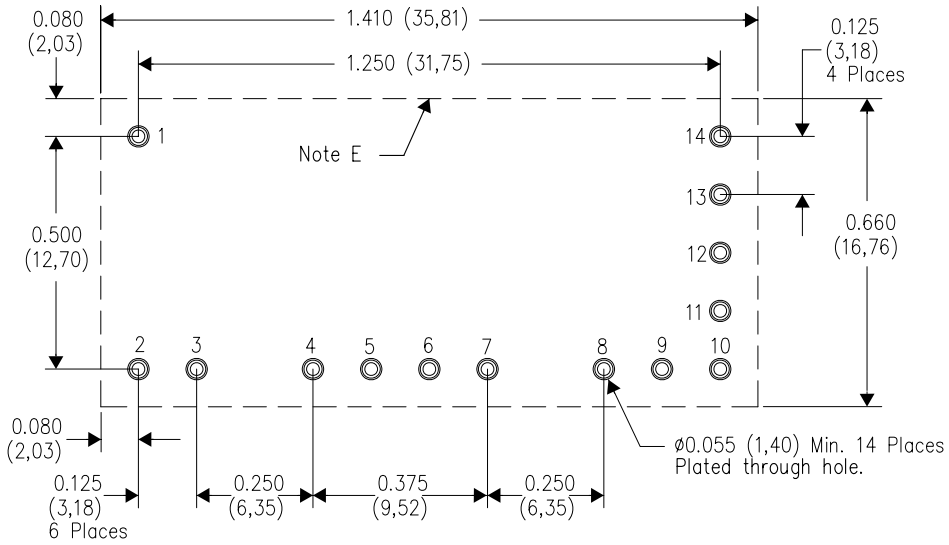
ECQ (R–PDSS–B14) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

ECP (R–PDSS–T14) DOUBLE SIDED MODULE

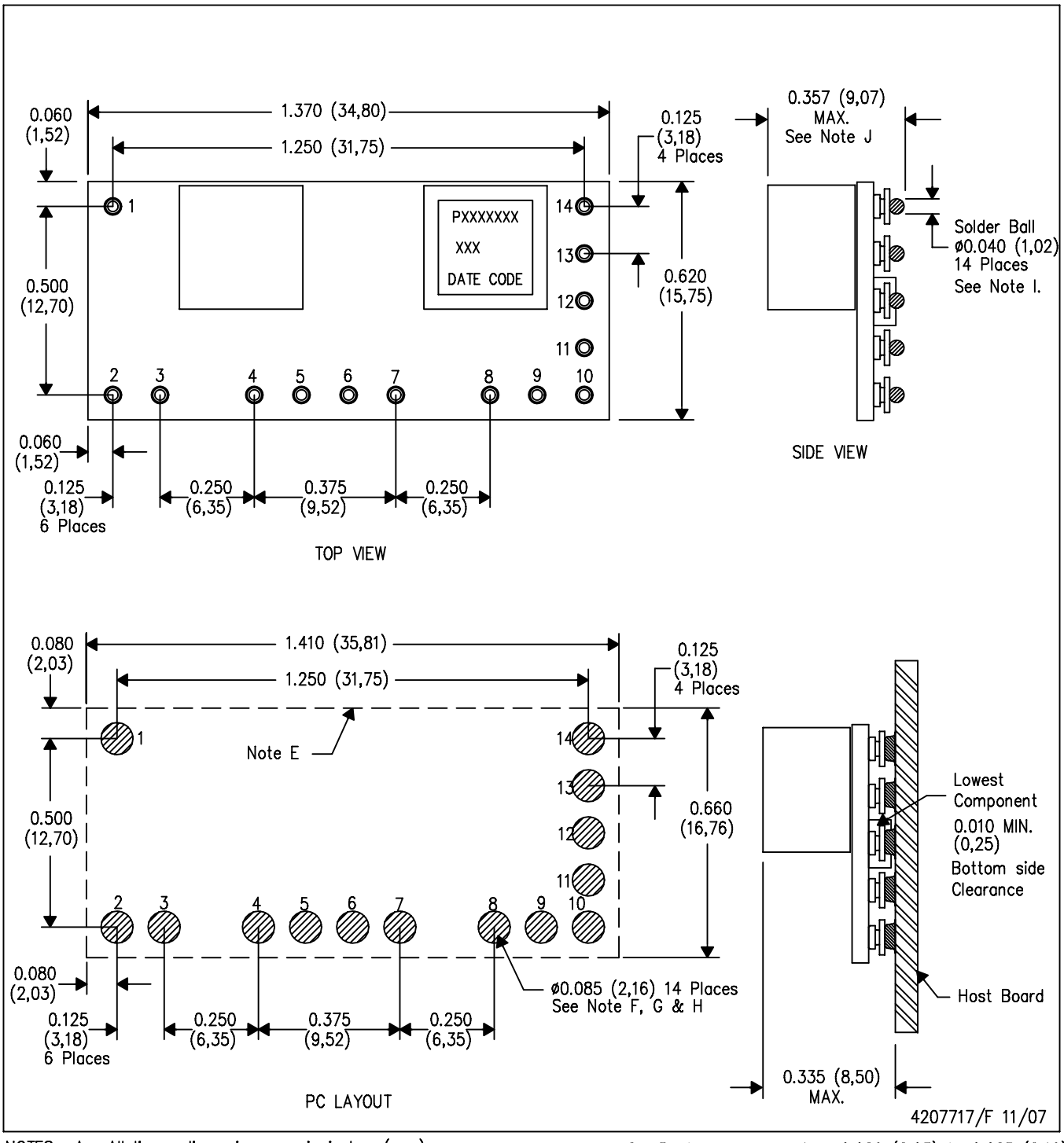




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NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

BCQ (R–PDSS–B14) DOUBLE SIDED MODULE



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ±0.030 (±0,76mm).
- D. 3 place decimals are ±0.010 (±0,25mm).
- E. Recommended keep out area for user components.
- F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. This is a lead–free solder ball design.
  Finish: Tin (100%) over Nickel plate
  Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
- J. Dimension prior to reflow solder.

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